

國立交通大學

材料科學與工程學系

碩士論文

利用一新穎位移曝光技術所製造之 $0.1 \mu\text{m}$
 Γ 形閘極 AlGaAs/InGaAs 高電子遷移率功
率電晶體

**A AlGaAs/InGaAs Power PHEMT with $0.1 \mu\text{m}$
Using a Novel Shift Exposure Method**



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摘 要



此論文中，本人利用位移曝光法以達到閘極線寬有效縮小，以利微波元件之應用。在實驗中，使用電子束微影系統為曝光系統，藉由位移曝光法中的位移大小來調控閘極線寬的解析力，以達到線寬為 80 奈米的閘極的製程目標。

閘極線寬的控制倚賴曝光位移大小，而曝光位移主要來自於二次曝光區域間的位移量。而製程方法及結果將在論文中詳盡的介紹。此製程中，僅須改變電子束微影系統的閘極圖檔，即可控制曝光位移量並產生多種不同閘極線寬。同時，在統計數據中，亦可證實此閘極製程有極高的良率並可重複製造。

實驗中，閘級的製程主要是在 PHEMT AlGaAs/InGaAs 雙層摻雜及銦含量為 0.22 通道層的砷化鎵晶圓上加工，此元件主要作為功率放大器之用。考慮功率放大器所需高崩潰電壓之條件下，曝光位移法可藉由閘極作為場調變電極板以提高崩潰電壓，即可達到所需功率放大器之要求。藉由改變光阻堆疊次序並佐以曝光位移法，即可同時達到較小閘極線寬及產生場調變電極板，以達到更高的崩潰電壓及更高的轉導值(G_m)。此實驗所產生的崩潰電壓約為 13 伏特，相較於傳統 T 型閘極所產生的 6 伏特，其約為 2 倍左右。此實驗中轉導值(G_m)亦提高為 450 mS/mm，相較於傳統 T 型閘極的轉導值(G_m)325 mS/mm，亦大幅提高。此實驗中，由於其可產生更高的崩潰電壓及更高的轉導值(G_m)，故可使元件特性效能大為提高，使其作為功率放大器能發揮更大效能。

A AlGaAs/InGaAs Power PHEMT with 0.1 μm Using a Novel Shift Exposure Method

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Abstract

In this dissertation, the focus is on the fabrication of submicron T-gate using shift exposure method for millimeter wave device application. In this method, the shifting magnitude was used to control the gate footprint resolution, gate length as small as 80 nm has been demonstrated using e-beam lithography system as the exposure system. Resolution of the e-beam system is limited to 160 nm, for high frequency applications, gate length smaller than this magnitude is sometimes required due to the limitation of the lithography system used; the Shift exposure method was required to achieve gate length smaller than 160 nm.

The gate footprint resolution depends on the shift magnitude, due to two different exposures. The fabrication method and result are described in detail in this dissertation. Several different gate lengths were fabricated by control's of the shift magnitude two different exposures. And the

statistical data show that the gate process is highly reliable and reproducible.

This gate fabrication technology was used on the AlGaAs/InGaAs double delta doped power PHEMT with the channel layer In content of 0.22 as the channel layer. To achieve high breakdown voltage for the power devices, the gate fabrication can also be used to produce field modulating plate. Changing the Photo resist stacking sequence combined with the shift exposure method, the small gate footprint with field modulation plate been fabricated simultaneously. Compare with the conventional T-gate, the breakdown voltage is doubled from 6V to 13V after the application of the Field Modulation Plate on the same devices. The Gm also increases significantly as compared with the conventional T-gate without shift and with smaller gate footprint Γ gate. (Gm = 485 mS/mm vs 325 mS/mm).

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