Chapter 1
The Introduction

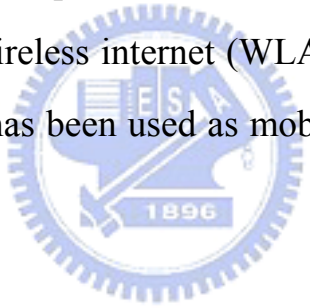
Since 1947, the 1st diode has been invented; semiconductor electronics has been advancing and evolving enormously. From the pn-junction diode to the MESFET and then to the MOSFET, the first HEMT (high electron mobility transistor) invented in 1979, by Dr. Takashi Mimura and coworker Yokoyama at Fujitsu laboratory. From the invention begins, the microwave has begin to enter a new concept, from the MESFET to HEMT which has the better performance and same process integration with MESFET.

The development of microwave transistors went almost unnoticed till 1980 because there were no high demands on market for microwave systems. Mostly applications of microwave transistor had been military and scientifically project, such as missile guidance, radar system, electronic warfare systems, high security communication systems, and etc. Around 1985s, satellite television broadcast using low-noise transistor

operating around 12 GHz was the first civil application of microwave devices.

When military applications were dominant in microwave electronics, performance is the important aspects rather than economic aspects. But it was changes when the consumer electronic philosophy is sufficient performance at lowest cost.

As we can see for nowadays, microwave systems has large impacts on our daily lives, civil communication technology such as mobile communication (e.g. cellular phones, PDA and other advanced systems.) and internet, especially wireless internet (WLAN) has widespread. Radar systems used in military has been used as mobile vehicles collision radar in consumer product.



And as for the future trend the application of microwave systems will be communication related and space communication related. While the operating frequencies of most commercial microwave products are in lower GHz range (several GHz to a hundred GHz), the space related covers the higher frequency up to 100 GHz.

As the impact, the performance of microwave transistors has been improved continuously such as higher operating frequency, noise figures and power amplification. The progress can be achieved by scaling reduces of the intrinsic device dimensions (gate length, Lg), minimizing undesired parasitic components of the transistor; such as parasitic source

and gate resistances, and development of new material with better carrier transport properties (higher mobility and velocities), better carrier confinement and other properties.

1.1 **III-V Devices overview**.

In the past, there is a great demand in developing high performance GaAs transistors for wireless communication applications. As compared with the silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistor (BJTs), GaAs transistors exhibit inherent advantages over Si-based transistors for high frequency applications due to the semi insulating substrate and other natural behavior such as high drift velocity and wide band gap. The special epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer and band-gap discontinuity to separate the ionized donors from the channel to increase the electron mobility. Consequently, GaAs HEMTs have superior carrier transport properties.

Conventional HEMT structure consists of AlGaAs/GaAs heterostructure. The band gap discontinuity between AlGaAs/GaA increases as the Al content increases and the large discontinuity in the band gap results in better confinement of the electrons in the channel. However, the deep-complex center (DX center) phenomenon exists while

Al content is over 20%. The DX center traps the electrons and degrades the device performance. To avoid the DX center phenomenon and increase electron mobility, AlGaAs/InGaAs/GaAs pseudomorphic HEMT (PHEMT) structure was introduced. InGaAs is a preferred channel material for HEMT's because of its excellent electron transport properties. The In content in the channel has been increased to enhance the electron transport properties and the confinement of the carrier in the channel. However, InGaAs channel in PHEMTs is limited to an In content of 25% to avoid lattice relaxation of the channel that will induce the dislocation and degrade the electronic properties of devices. (1)

1.2 Electron Beam Lithography and Layout system.

Lithography is the most important patterning step for semiconductor device fabrication, due to its critical influence to the devices. Almost all steps involved in device fabrication require lithography patterning for defining specific regions in devices.

For conventional optical lithography systems, the light source is defined as the critical parameter to enhance the processing critical dimension (CD). Shorter wavelength produces higher resolution. Wavelength of the conventional optical lithography source evolved from h-line with 450 nm, g-line with 405 nm, i-line with 320 nm to Deep-UV with 193 nm.

In Electron Beam Lithography system, electrons act as the source, due to the electron duality, the wavelength depends on the acceleration energy applied to the beam source. Higher energy will result in shorter wavelength, with non relativistic calculation as:

$$E_k = \frac{p^2}{2m} \tag{1.1}$$

$$\lambda = \frac{h}{p} \tag{1.2}$$

E_k : accelerated energy (J)

p : electron momentum (kg m/s)

m :electron mass (9.11x10-31 kg)

λ : wavelength (m)

For 40 KV acceleration voltage, it gives 0.04Å wavelength. Since the diffraction matter is not significant at the short wavelengths, the resolution enhanced drastically.

Thus, it is clear that E-beam lithography system will give smaller pattern size than optical lithography system. However the resolution is constricted by other factors such as electron scattering, proximity effect and various aberrations properties in its electron optics.

The electron beam lithography system used in this experiment is Leica Qplus 300 series with LaB_6 as the cathode source. The high temperature thermionic excitation applied to the cathode to extract the electrons. And

then the electron beam accelerated by the high voltage (40KV) from anode, passing by the magnetic alignment lens C1, C2 and C3 and then reach the below part of the focus coil and deflection coil, and then reach the chuck where the wafer placed.

As described electron beam lithography system consist of:

1. An electron gun chambers that supplies electron; in which contains of cathode (LaB_6), charge supplier, and extraction anode that grounded.
2. Electron columns chamber that shapes and focuses the electron beam.
3. Mechanical stages that moves wafer under electron beam for exposuring.
4. Wafer handling system that automatically feeds wafer from the exchange chamber into exposure chamber. Airlock chamber function as the chamber that being air pressure to exchange wafer for maintaining the main chamber vacuum pressure.
5. Computer system that controls the lithography system, vacuum system and exposure steps control.

1.2.1 Electron gun chamber

Electron beam lithography system has the similar backbone with SEM as the electron is the main source, usually the cathode included: Tungsten and LaB6. The electron emission divided by thermionic and field emission.

- Thermionic: the electron emitted from the cathode source by applied high temperature and gives the electron enough energy to overcome the work energy, so it can jump from source to vacuum.

As from Richardson's equation, I is a function of absolute temperature:

$$I = AT^2 e^{-(B/T)} \qquad (1.3)$$

I : current (A/cm^2)

A,B : constant

T :temperature (K)

Figure 1.1 is the structure of the source cathode inside the Wehnelt's. As we can see that the applied current will heating the filament and extracting electrons. Anode is grounded and cathode is applied to high voltage.

- Cold emission: the electron is emitted from source by applied 3-5 KV. This potential energy gives the electron enough energy to overcome the work energy at low temperature. The advantage is cleaner chamber due to lower chamber temperature, so several molecules didn't vaporize and longer life of the cathode without thermal stress. The other advantage is higher tunneling transmission probability due to the applied potential energy over

cathode.

Other key parameters of the source are source beam diameter and the brightness. Size is important due to the amount of the demagnification the lenses must provides in order to form a small spot on the target. Brightness can be compared to the intensity in the light optics; higher brightness produces higher current in electron beam. Table below gives several comparison of source type with its important properties.

Source type	Brightness [$A/cm^2/st$]	Source size	Vacuum requires (torr)
W (thermionic)	$\sim 10^5$	$\sim 25\ \mu m$	10^{-6}
LaB_6	$\sim 10^6$	$\sim 10\ \mu m$	10^{-8}
Schottky	$\sim 10^8$	~ 20 nm	10^{-9}
W (cold FE)	$\sim 10^9$	5 nm	10^{-10}

Tungsten is used at the early development for its ability to withstand high temperature without melting or evaporating. Unfortunately, the source is not so bright due to its higher work function, so the LaB_6 has been chosen for substituting the tungsten cathode for its lower work function and lower operating temperature (1800 K) compare to tungsten at 2700 K. Although it seems the cold

field emission has better performance than thermionic, it can't be used as in the lithography process due to their instability with regard to short term noise as well as long term drift. The noise is caused by the atoms that adsorb on the surface of the tip, affecting the work function and greatly reduced the beam current. Heating the tip (flashing) can clean it, but it fluctuated as the new atoms quickly reabsorb. This can caused high fluctuation when using this source as the lithography system that will had large affect on yield and reproducibility. Thermal field emission (Schottky emission) is the new technology been introduced. It combines the sharp tungsten needle with thermal and field emission, operating at 1800 K make it less sensitive to the environment and last longer than 2700 K thermionic source temperature.

There is an aperture that place in near the cathode that is Molybdenum made. It controls the beam convergence angle, decrease the effect of lens aberration. It is best to have beam limiting aperture as close to the gun to limit the effects of the space charge caused by electrons repulsion that will decrease the brightness.

The electron gun chamber is separated by a V4 valve, which separated it with column chamber, and pumped by an ion pump to establish the high vacuum requirement.

1.2.2 Column Chamber

Column chamber consists of electron lenses that functions as beam focusing and shaping that has the same principle with optical lenses. But the electron lenses can only be made only to converge, not diverge and also the quality is not nearly as good as optical lenses in term of aberrations, such as spherical and chromatic aberrations. Both types can be minimized by reducing the convergence angle of system so the electrons are confined to the center of the lenses, but can greatly reduced beam current. A magnetic lens is formed from two circularly symmetric iron polepieces with a copper wind-in. The divergence of the magnetic flux imparts a force on electrons back toward the Z axis, resulting in focusing action. As a result of Lorentz force equation on magnetic field as can be seen on Fig 1.2 is the schematic diagram of the magnetic lenses.

$$F = q (E + v \times B) \qquad (1.4)$$

F : magnetic force

q : electron charge

E : the electric field

B : the magnetic field

v : the velocity

There are several others optical elements included apertures, deflection systems, blanking plates and stigmators.

Apertures are small holes through which the beam passes on its way down to the column. Column apertures have several choices to

fits the resolution; 100 μm, 200μm, 300 μm and 400 μm. Smallest aperture not always results in best resolution. It depends on the ways of focusing. Selection of the perfect apertures with focusing parameter is needed for having the best resolution.

Deflection systems as shown on Fig 1.3 are used to scan the beam across the surface of the wafer. The coils or plates are arranged so that the fields are perpendicular to the optical axis. Deflecting the beam off axis introduces additional aberrations that cause increase in beam diameter. This effect limits the maximum field size that can be used. Usually one field size is defined as an area that deflected beam can reach without moving the substrate. Larger field size will reduce exposure time but decrease the resolution; usually the large field size has the dynamic correction tools which mathematically calculated. Recently using smaller than 1.6μm x 1.6μm field size is used for high resolution, due to the smaller aberration.

Beam blanking system acts as a switch, which turns the beam on and off. It consists of a pair of plates set up as a simple electrostatic deflector. Turning the beam off is by applying a voltage across the plates which will sweeps the beam off axis and is intercepted by below aperture.

Stigmator is a special type of lens used to compensate for imperfections in the construction and alignment of the column. These

imperfections can result in astigmatism, with the shape of normally round beam becomes oblong resulting in smeared images in the resist. The stigmator cancels out the effect of the astigmatism, forcing the beam back into its optimum shape.

Other components such as faraday cage (cup) located at the chuck to measure the beam current in order to ensure the correct dose for resist exposure. The system had a silicon solid state detector for focusing and deflection calibration with channel plate detector with photomultiplier tubes for electron imaging.

1.2.3. Vacuum system

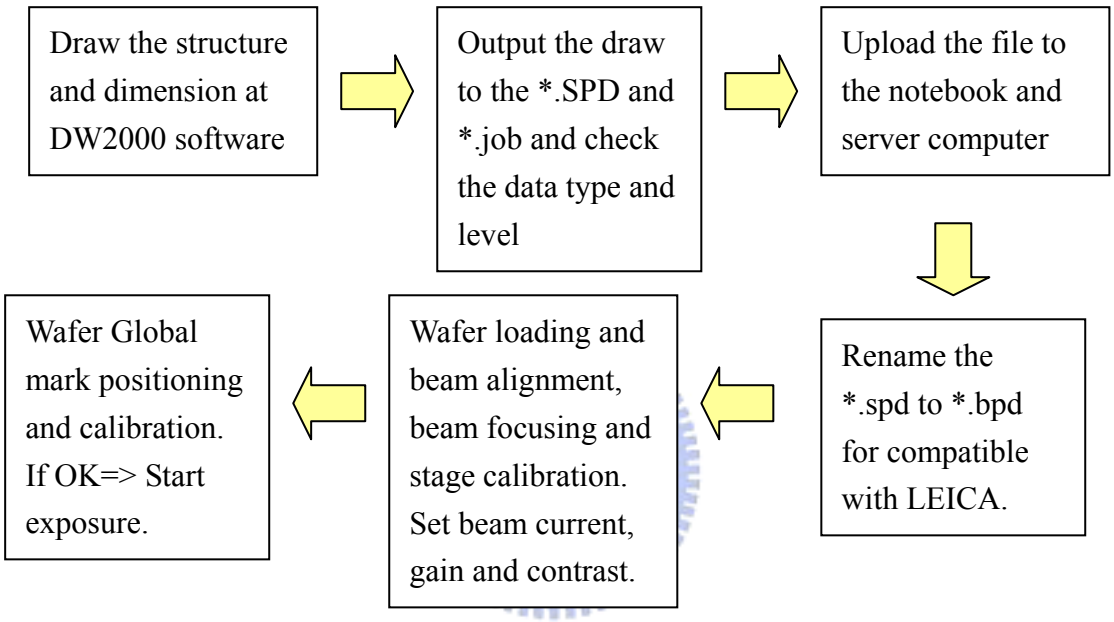
This system consists of one mechanical pump that for rough pumping, three diffusion pumps that responsible for chamber, airlock and gun chamber vacuum condition, for lower pressure, it used three ion pumps for reached 10^{-7} torr, the gauge consists 5 pirani gauge for higher pressure and 3 penning gauge that responsible for lower pressure.

1.2.4 Layout system

The layout software used DW2000 Physical Layout Design Software provided by Design Workshop Technologies Corp. The layout has been created by the software and then export to the files with the form that can be read by EBML system. The layout not only compiles the

application order text, but also the mask design picture, that is going to be written by EBML. The scanning type is using the vector scan rather than raster scan for having the high speed of writing.

The entire steps from drawing the structure to the direct writing on LEICA is shown below:



1.3. Dissertation outline

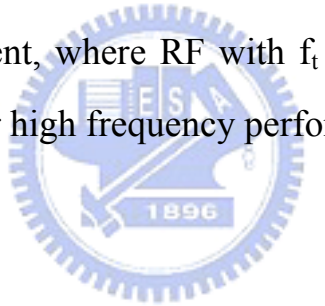
At the introduction, I have described the brief history of the III-V and the development of the semiconductor devices. In chapter II, the theoretical basis of the electron beam lithography, resist material and chemical reaction, and the process integration on devices are introduced. The electronic properties of the process technique also integrated with other similar process in the review paper, such as Field modulation Plate on Silicon Nitride by K.Asano et.al. from NEC corporation that this integration increase the breakdown voltage of the devices and also the

shrinkage gate that increased the high frequency characteristic.

Chapter III covers the experimental procedures for OEM gate process in detail with comparison made to that of the conventional T-gate process.

In Chapter IV, details of device structure for high power applications are introduced. Fabrication process with integrated OEM gate technique to prove the improved performance of such devices is also included.

In Chapter V, the DC and RF characteristics of the devices that being fabricated is discussed in detail with the DC for the Gm, IDss, breakdown voltage and leakage current, where RF with f_t and f_{max}, PAE and MAG, and noise performance for high frequency performance.



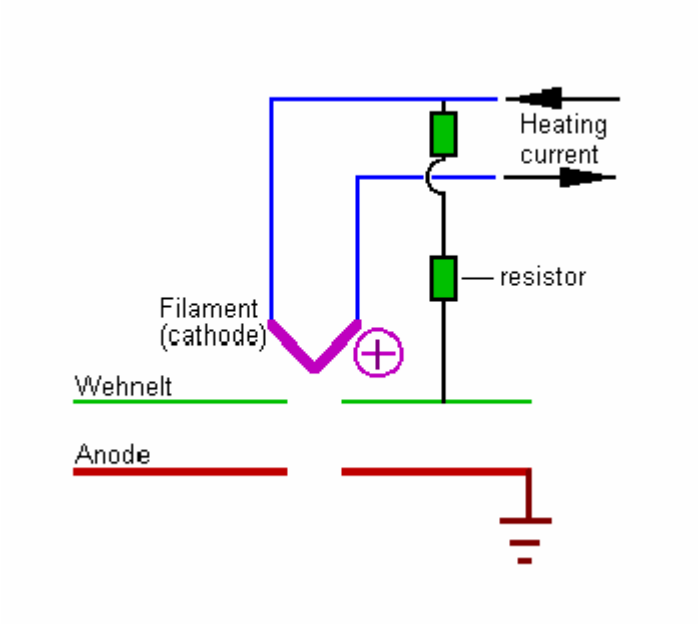


Figure 1.1 is the structure of the source cathode inside the Wehnelt's.

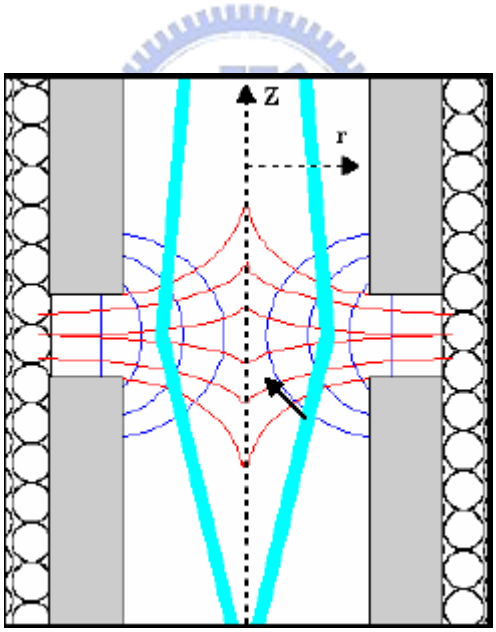


Figure 1.2. Cross section of magnetic lenses.

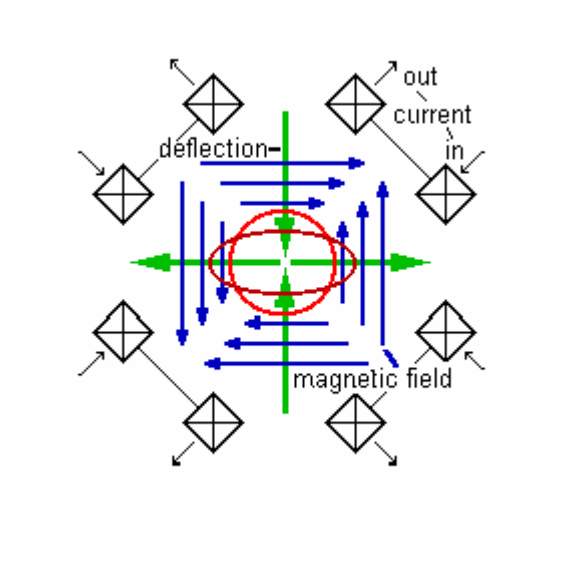


Figure 1.3 is the beam deflection system.

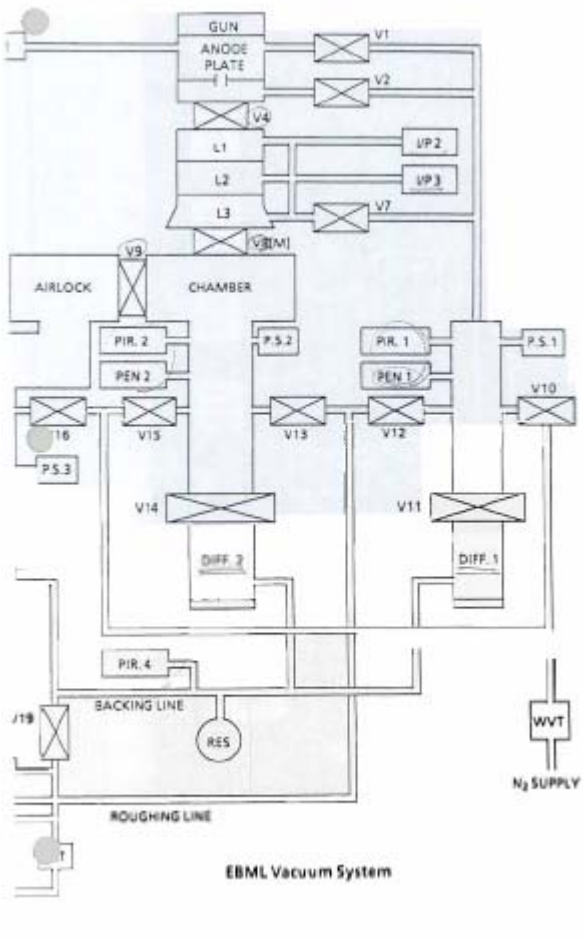


Figure 1.4 E-beam vacuum system

Chapter II
Theoretical Basis of The Device and Electron Substrate Interaction

This chapter introduces the Physics of the devices operated at the high frequency. Physically understand the background of the device and the field modulation plate are discussed in detail with several paper reviews and also the review of the gate shrinking method from several other groups that work on III-V and in our groups itself.

2.1 Gate shrinking for high frequency performance.

Great improvement of device performance due to device size reduction from macro scale to nano scale has made the big impact on semiconductor technology. The electron transit time below gate can be expressed as:

$$\tau = \frac{C_g}{g_m} = \frac{L_g}{\upsilon} \qquad (2\text{-}1)$$

Thus, for the same drift velocity, the transit time is lower for the smaller L_g. The Gm transconductance also increases due to the reduction of the gate footprint of the devices.

$$f_t = \frac{Gm}{[2\,(Cgs+Cgd)]} = \frac{v_{sat}}{[2\,Lg]} \qquad (2\text{-}2)$$

From the above, It is clear that reducing L_g will increase f_t with the same device saturation velocity. Furthermore, f_{max} is also related to f_t in the manner as:

$$f_{max} = f_T \Big/ \left\{ 4\frac{G_{ds}}{G_m}\left(G_m R_i + \frac{R_s + R_g}{1/G_m + R_s} \right) + \frac{4}{5}\frac{C_{gd}}{C_{gs}}\left(1 + \frac{2.5C_{gd}}{C_{gs}} \right)(1 + G_m R_s)^2 \right\}^{1/2}$$

(2-3)

In the above expressions, it is seen that decreasing C_{gd}/C_{gs} will increasef_{max}/f_t. C_{gd} is the gate to drain capacitance, and can be decreased in the following ways: (1) using the lower dielectric constant material of the passivation layer, (2) increasing the distance between gate and drain. C_{gs} increased also with the same way, due to the capacitance constant formula is the same, but the matter is, if the gate is shift from the center near to the source, C_{gd}/C_{gs} will decrease significantly and can increase the f_{max}/f_t ratio. Decrease the R_g also a choice by the substitution of the gate alloy using the lower resistance of the gate metal, such as Copper.

Using “T-shaped” gate will effectively decrease the resistance by applied larger head and retaining the small gate contact. Further reduction in gate resistance can be achieved by shifting the gate towards the source region. But the shift magnitude is the critical parameter due to the larger

head of the gate, shift made the head move near to the source and bounce the source if the process parameter is not precisely controlled as described by Hae-Sung Kim et.al. (2).

Several techniqueshave been developed to shrink the gate. For example, using higher sensitivity photo resist; ZEP520 was proposed by S.C. Kim et.al.(3). Kim used ZEP520 as the gate-foot resist pattern, and stacked the PMMA-MMA/PMMA for forming the gate-head pattern. As can be seen from Fig 2.1 the resolution reached is around 70 nm after lift off.

Yamashita et.al has successfully developed a 25nm gate on lattice matched InAlAs/InGaAs by using two step back etched dielectric method. After E-beam lithography of ZEP520, the SiO_2 is etched back to reduce the gate length, due to the slower etch rate on the smaller opening (4). The result is shown in figure 2.2.

Suemitsu et.al successfully decreased the gate length by using the nanocomposite photo resist ZEP-520 mixed with fullerene C_{60}. Fig 2.3 shows the difference between the ZEP with and without fullerene. Reduction of the gate length resulted in as reported a 350 Ghz cutoff frequency. (5)

Several other techniques have also been showed, such as thermally reflowed gate by H.M. Lee et al. The conventional PMMA/PMMA-MMA resist was used for T-gate with post applied bake (PAB) to reduce the

Critical Dimension from around 163 nm to below 50 nm.(6)The result is shown in the Fig 2.4. This method has been successfully being fabricated on MHEMT devices by Y.C. Lien et.al and increased the RF performance significantly due to the Lg reduction.(7)

H.L.Chen et al. showed the chemical shrink technique for the contact holes using e-beam lithography. Chemical amplified resist is used to reduce the dimension, due to the intermixing of the interface with the reagent forming the compound that reduced the CD of the holes. Temperature is the mixing parameter for enhancing the reactivity of the solution with the photo resist as shown in Fig 2.5(8)

Szu-Hung Chen et al. [1.9] developed a phase shift mask (PSM) technique to define the 0.16μm gate length by I-line lithography. The 2000Å SiN_x was first deposited by chemical vapor deposition (CVD). Then the 8% half-tone PSM was used for the definition of the SiN_x opening. After the PSM exposure, the SiN_x was etched by RIE, and a 0.2-μm-wide opening was formed. In order to further reduce the dimension of opening, an additional SiN_x was deposited by CVD and etched back by RIE without any mask. Using the silicon nitride re-deposition and etch-back technologies could reduce the dimension of the openings. Finally the T-shaped gate with a length of 0.16 μm was achieved. The overall process is depicted in Fig. 2.6.

2.2 Surface charge effect and Field Modulation Plate.

III-V devices have gate on the Schottky layer for the formation of the Schottky contact. Surface characteristics have important effect on the gate performance, due to the surface contact below gate. The devices performance will degrade because of the surface enhanced leakage if the surface has defects Gate leakage will thus increase significantly and degrade the performances of the gate in modulating the electron at the channel. Surface traps also have the advantages for increasing the breakdown voltage of the devices.

There are two breakdown mechanisms for the III-V devices. One is the surface breakdown, the other is avalanche breakdown. Avalanche breakdown occurs frequently at the channel, due to the narrower band gap of the channel material such as InGaAs. Electrons are generated in the active region when voltage is applied at the device Electrons will move from source to drain and controlled by the gate voltage. With increasing voltage, the electron generation will be increased due to the energy applied. Holes are also generated as electrons are. At high voltages, the electrons and the holes have sufficient kinetic energy to be able to break the covalent bonds in atoms with which they collide. The carriers liberated by this process may have sufficient energy to be able to cause other carriers liberated in another ionizing collision. As the result many carriers are created that are able to support any value of the reverse current, as determined by the external circuit, with a negligible change in

the voltage drop across the junction.

Surface breakdown occurs when Vd is applied, the electrons from the gate tunnel through the passivation layer to the drain side. The Nitride passivation layer plays a key role in the enhancement of the breakdown voltage. Usually surface breakdown occurs when applied voltage is higher than 10V, with avalanche breakdown usually occurs at 7-8 V. Several studies have been done for enhancing the surface breakdown, such as recess method. Recess method can induce the surface traps, due to the chemically etch away the Capping layer of HEMT. The surface traps will catch electron flowing from gate to drain. As been simulated in (9), the single recess and double recess reduce the generation number of electrons and holes at the gate edge between drain. This surface trap induced method has been used to improve up to about the breakdown voltages of AlGaAs/InGaAs pHEMT for single recess 6V and double recess about 8V with the Lgd=0.95μm.

Field modulating plate (FMP) has been introduced to further enhance the surface trap effect and breakdown performance of the devices. In conventional HEMT with recess topology, there existed high concentration of the traps at the surface of the channel. When the channel is off, these traps become negatively charged, which effectively reduce the electric field at the gate edge between drain, resulting in high breakdown voltage.

However, when the gate bias is turned on as RF signal is applied, the slow response of the traps near the gate freezes the channel modulation. The surface traps needs longer time to neutralize compare with the channel. This channel constriction due to the surface traps resulted in the degraded RF performance. As can be seen from Fig 2.7, larger breakdown voltage resulted in the increase of the lag time due to the larger number of the negatively charge trap at the surface due to the recess topology.

Adding a field plate between gate and drain improves the RF performance and DC breakdown voltage. A field modulating plate is located on the surface passivation layer in the gate drain recessed region. Field modulating plate not only reduces the channel constrictions which occurs at gate open, but also reduces of the electric field at the gate edge under pinch off conditions as shown in Fig 2.8. Comparing the I-t graph of the structures with and without field modulating plate as plotted in Fig 2.9, it shows that the delay of I_{ds} is negligible with FMP. The delay time reduction will significantly improve the RF performance. The plate also contributes on reducing the gate leakage current of the device, due to the neutralizing of the surface trap when the gate is pinched off. Gate leakage current has been shown to be lower than the conventional HEMT as shown in Fig 2.10. Highest breakdown voltage reported using this technique was 47 V (10) for Lgd 2.5 μm .

2.3 Interaction Between Electrons and Substrate .

When the electron beam strikes the substrate, it interacts with solid substrate and produces both elastic and inelastic scattering which tend to broaden the initial beam diameter. Elastic scattering is defined as single, plural or multiple scattering (diffusion). When the electrons penetrate through the resist into substrate, they undergo large angle scattering events (backscattering) and cause the proximity effect, where the current pattern receives several dosage from the neighbor's patterns. During this process the electrons are slowing down and producing low energy cascade electrons, called secondary electrons.

As the electrons penetrate the resists, some of them will undergo small angle scattering events, which can result in a significant broader beam profile at the bottom of the resist than at the top. The increase in effective beam diameter is given empirically by:

$$d_f=0.9(R_t/V_b)^{1.5} \qquad (2\text{-}4)$$

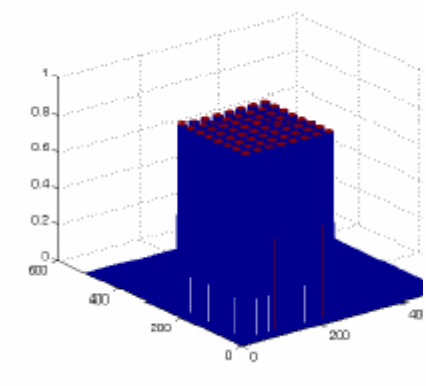
; where: R_t is the resist thickness(nm) and V_b is the beam accelerating voltage(KV).

When the electrons continue to penetrate through the resist into substrate, many of them will experience large angle scattering events. The electrons may return back through the resist at a significant distance from

the incident beam, as back scattering electron causing additional resist exposure. The range of the electron travels before losing its energy depends on both the energy of the primary electrons and the type of the substrate. Low atomic number material usually gives less back scattered electrons.

As the primary electrons slow down, much of their energy is dissipated in the form of secondary electrons with energies from 2 to 50 eV. They are responsible for the bulk of the actual resist exposure process. Since their range in resist is only a few nanometers and contribute little to the proximity effect, the result can be considered to have an effective widening of beam to around to 10 nm.

From Monte Carlo simulation, it can be seen that the background electron has high distribution on the proximity effect.



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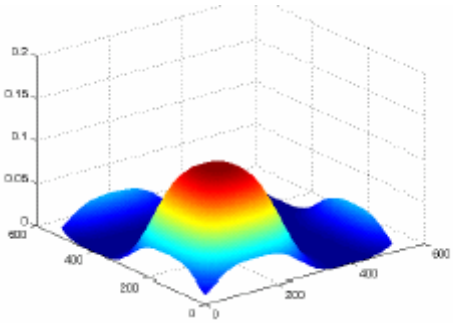

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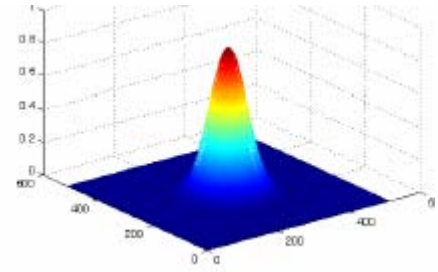

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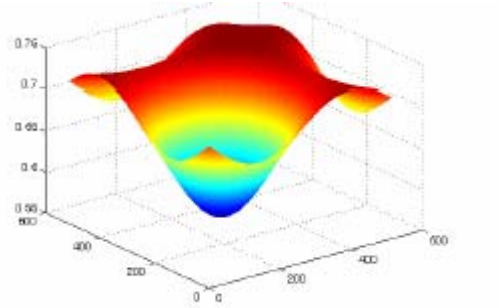

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The 1st graph is the original pattern generating from layout design. The 2nd is the background dosage and the 3rd is forward electron dosage, generating a higher dosage than expected as can be seen from 4th picture, due to the convolution of forward electron scattering and backward scattering electron.

Usually to avoide the proximity effect, the correction is made due to the pattern correction or dosage correction at the edge of the pattern. Pattern is designed smaller than expected resulted pattern and the dosage controlled for having the exact pattern without enhanced the resulted pattern size.

Experiments are performed on different substrates such as Si, GaAs

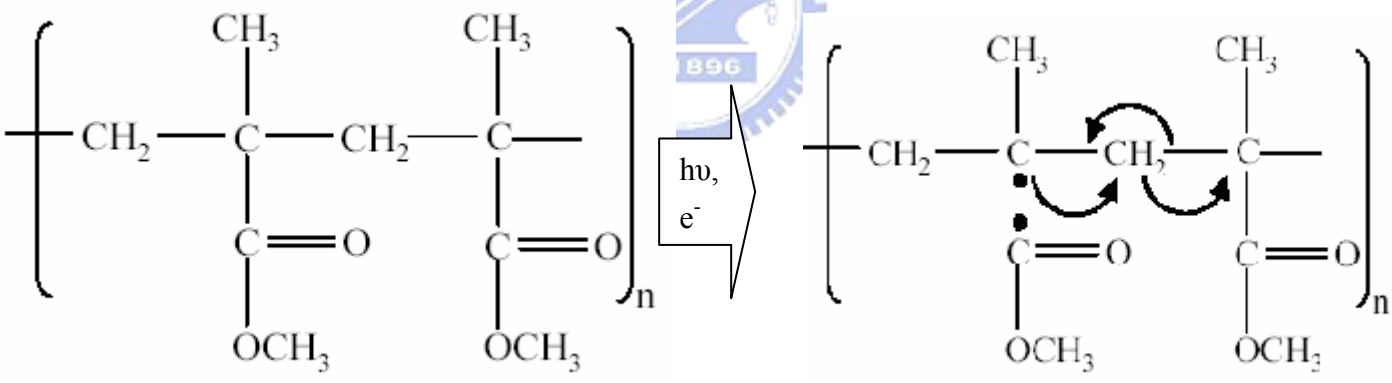
and Si_xN_y to determine the effect of the electron scattering on the resist dosage. Graph 2.1 (a) is the dosage vs PMMA resist opening resolution on Si substrate, (b) on GaAs and (c) on Si_xN_y. As can be seen, the backscattered effect is larger on Si than GaAs, so it needs larger dosage for the resist on the GaAs to open. At the same dosage, the resist resulted in the residue at the lower profile of the resist. Si_xN_y resulted in the lower backscattered electron due to the porosity of the film higher than the GaAs or Si substrate, it needs larger dosage for resist on the Si_xN_y for the critical opening resolution.

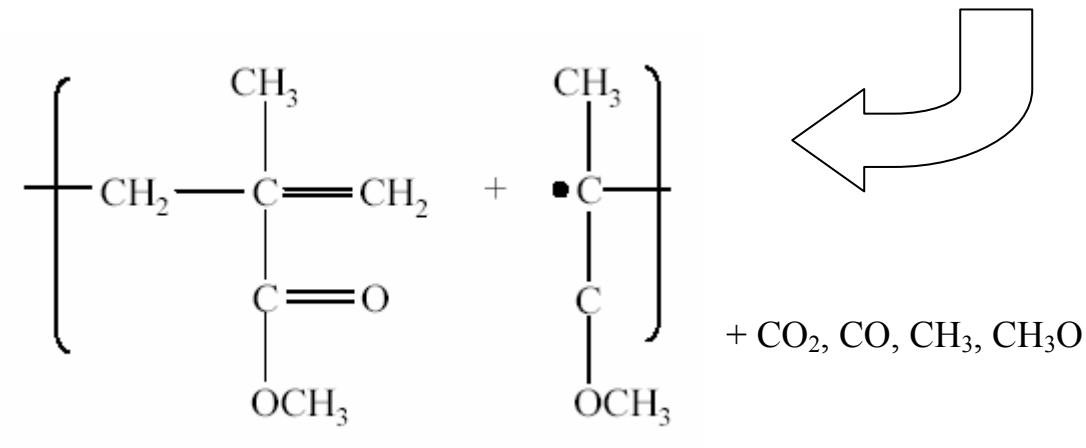
As we know, the design pattern is transferred on the resist. There are two kinds of resist material, positive and negative resist. PMMA (poly metyl meta acrylate) and P(MMA-MMA) are positive resist that the exposed area is dissolved in solvent and leaving the unexposed area. P(MMA-MMA) has the lower resolution and higher sensitivity compared to PMMA due to the electron beam exposure.

There are two main effects on PMMA due to the electron beam exposure; side chain scission and cross linking. Side chain scission of PMMA is formed, and then the polymer chains become shorter and more soluble. Chain scission in PMMA is initiated by cleavage of the main chain carbon to carbonyl carbon bond. The radical that is formed along the main chain undergoes a rapid rearrangement resulting in the cleavage of the main chain and producing the small molecule volatile products and radical species. If the cross linking formed, the polymer chains became three dimensional network and insoluble. Normally PMMA is used as a

positive resist, so side chain scission is more dominate than cross linking. Cross-linked PMMA needs a very high electron beam exposure dosage (10 times higher) due to the higher energy needed than side chain. It can know from the local marks that are frequently exposed to electron beam, the resist on there behave negatively.

Below is the chemistry of PMMA exposed by electron:



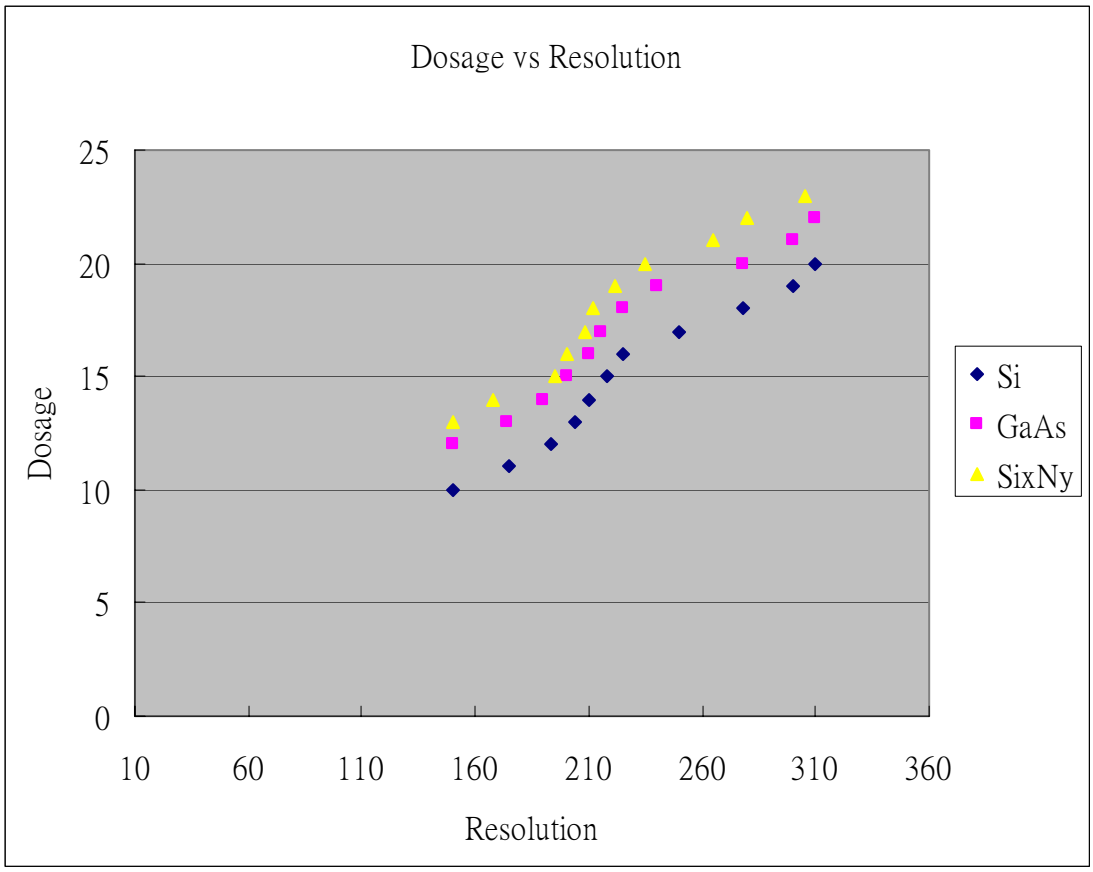


PMMA is purchased with 495 K high molecular weight forms. The processing method described below:

1. Substrate preparation and cleaning (ACE + IPA + N_2 blow).
2. Spin coated PMMA resist layer with conventional method (600 rpm 10" 2500 rpm 60").
3. Prebake with hot plate at 250 ^{o}C for 3'.
4. For producing T-gate, usually bilayer or trilayer resist is used. So after PMMA as bottom film, copolymer usually as upper film, due to its higher sensitivity to electron beam will result in larger pattern compared to PMMA. Coating copolymer at 600 rpm 10" 3000 rpm 60".
5. Prebake at 180^{0}C for 3'.
6. Exposure using electron beam with sufficient dosage.
7. Pattern definition with MIBK:IPA=1:3 produces high contrast, high resolution but low sensitivity.

It gives the result as shown below the bilayer resist for forming T-shaped gate in Fig 2.11. Sometimes trilayer resist is used for enhancing the lift-off properties of the gate metal, with PMMA-copolymer-PMMA (three layers) coated with different temperature and different thickness

parameter as shown Fig 2. 12.



Graph 2-1 Dosage vs Resolution at Si substrate, GaAs and Si_xN_y thin film

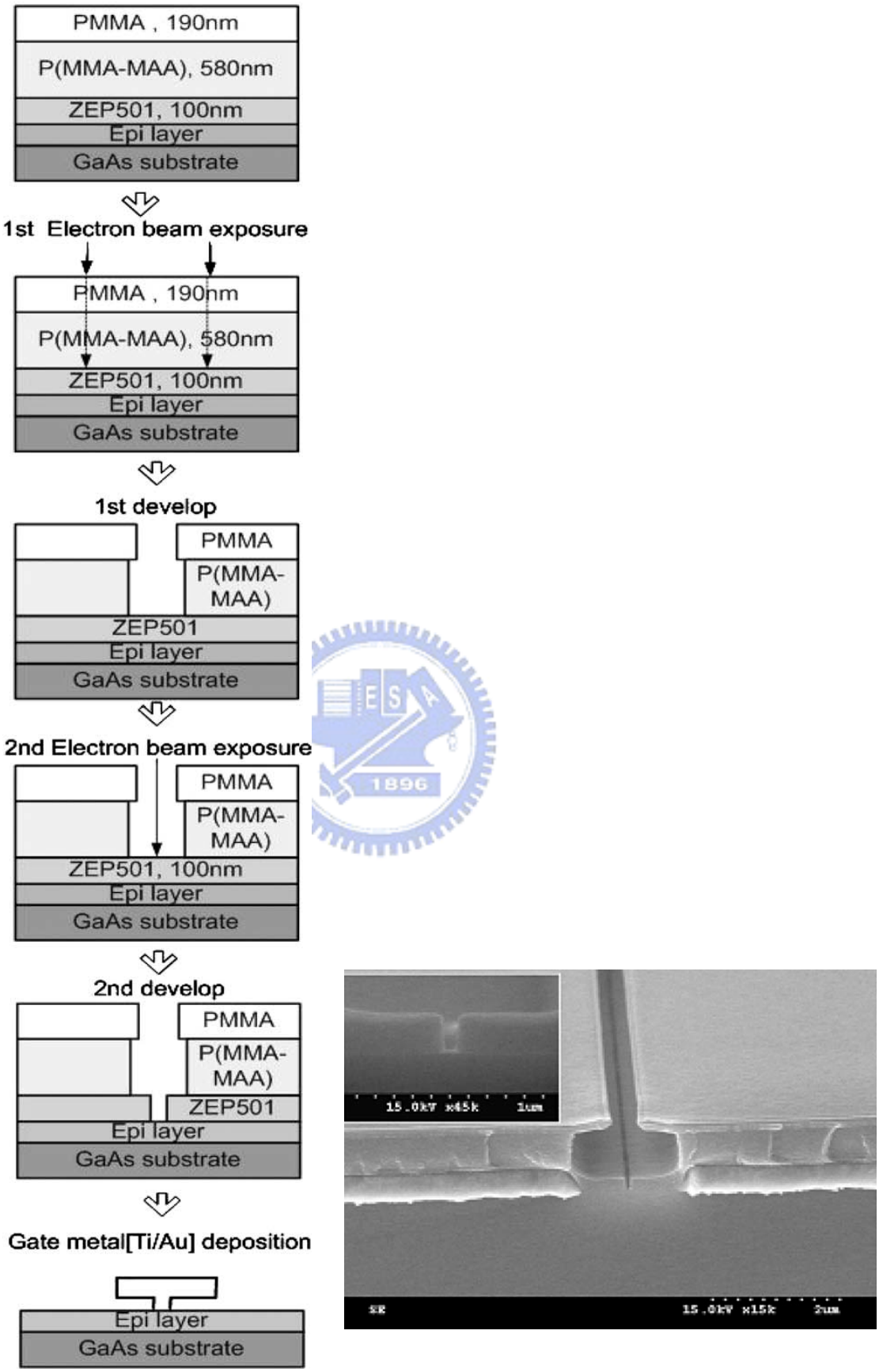


Fig 2.1a for the Fabrication step and b for the result of the photo resist.

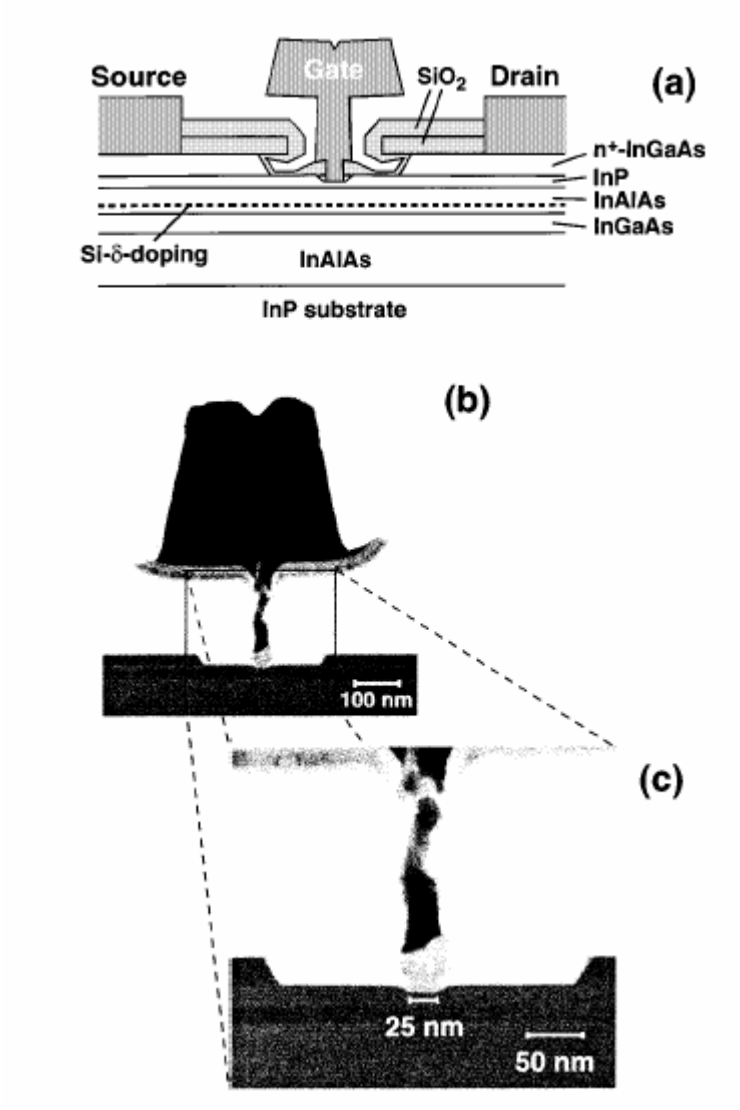


Fig. 2.2 (a) Schematic cross-section view of the HEMT,(b) Cross-sectional TEM image of the 25-nm-long T-shaped gate, and (c) Magnification of the TEM image around the bottom of the 25-nm-long T-shaped gate.

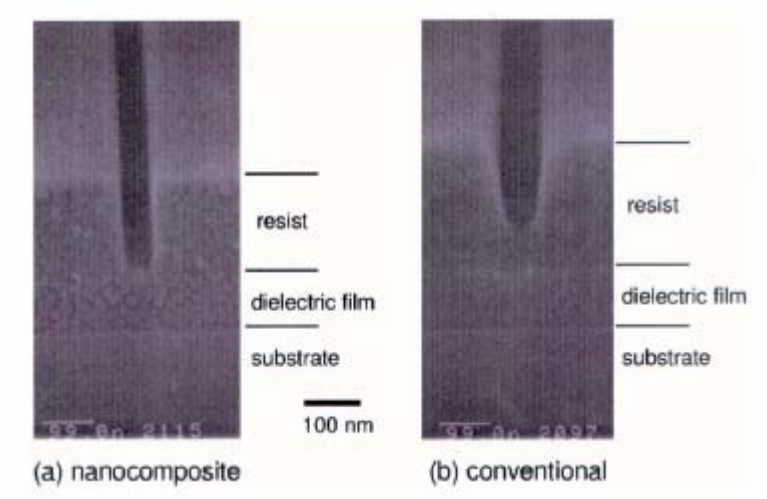
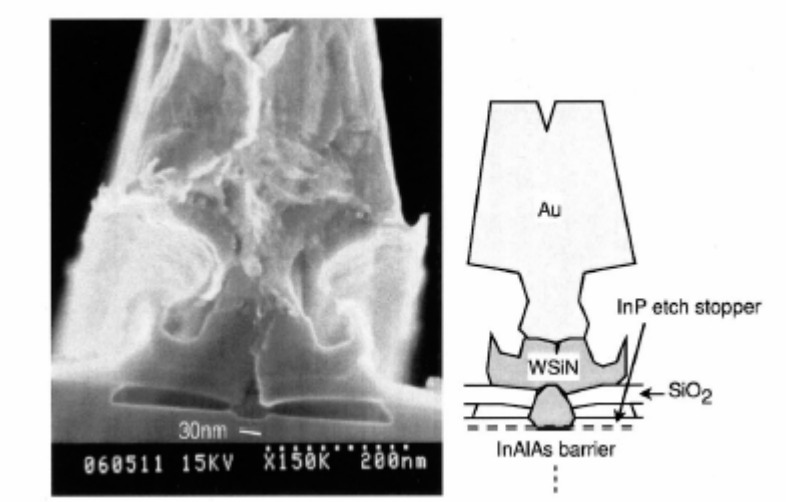
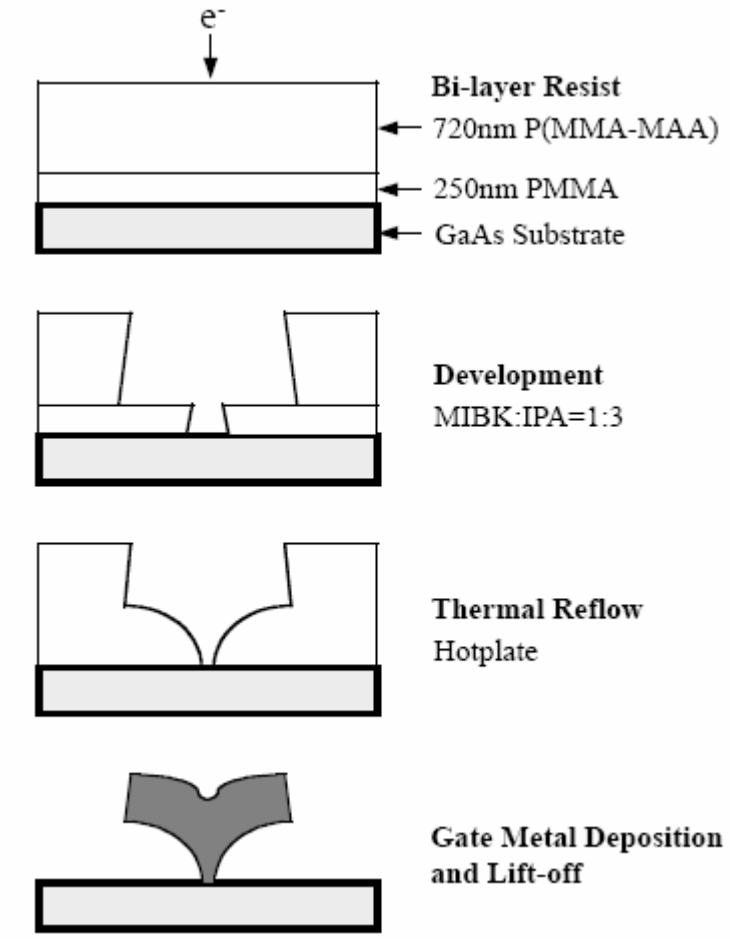
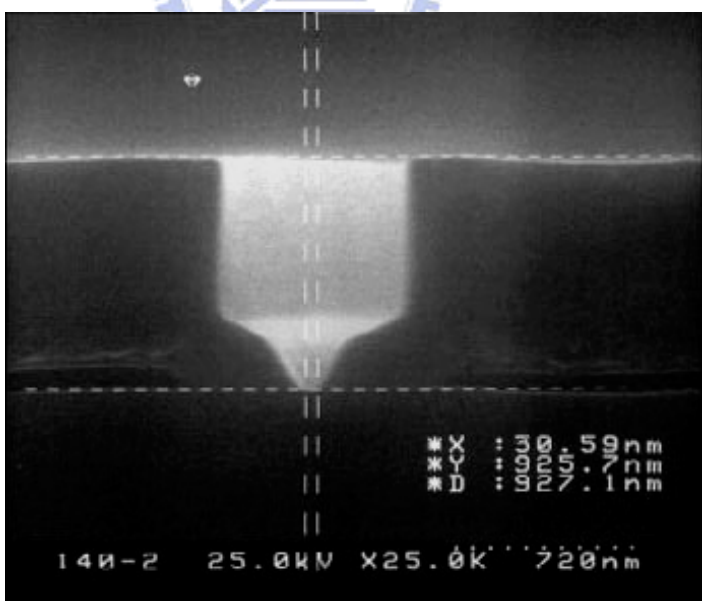


Fig 2.3 Yamashita with C_{60} added to photo resist and etched back method at Fig 2.3c.




e-
Bi-layer Resist
720nm P(MMA-MAA)
250nm PMMA
GaAs Substrate
Development
MIBK:IPA=1:3
Thermal Reflow
Hotplate
Gate Metal Deposition
and Lift-off


*X :30.59nm
*Y :925.7nm
*D :927.1nm
140-2 25.0kV X25.0K 720nm

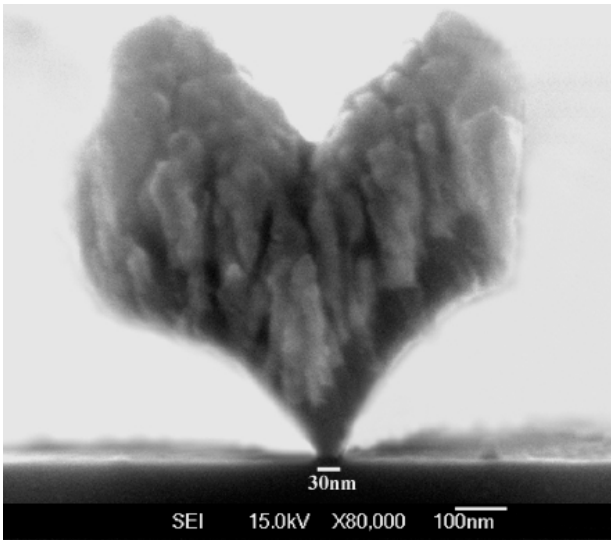
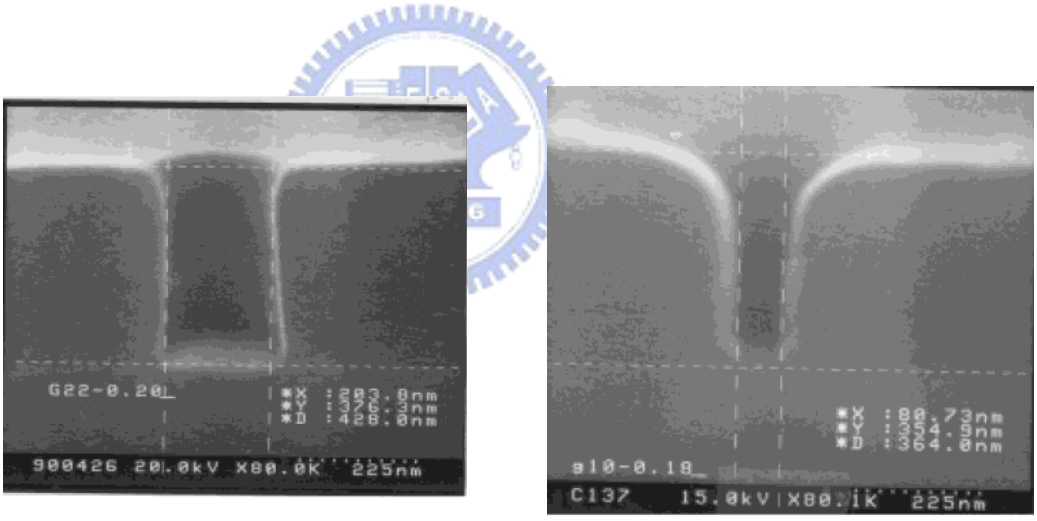


Fig. 2.4 Process flow of the thermally reflowed T-gate and its result.



(a) (b)

Fig 2.5 a. 200 nm UV-86 contact hole and b. 80 nm contact hole.

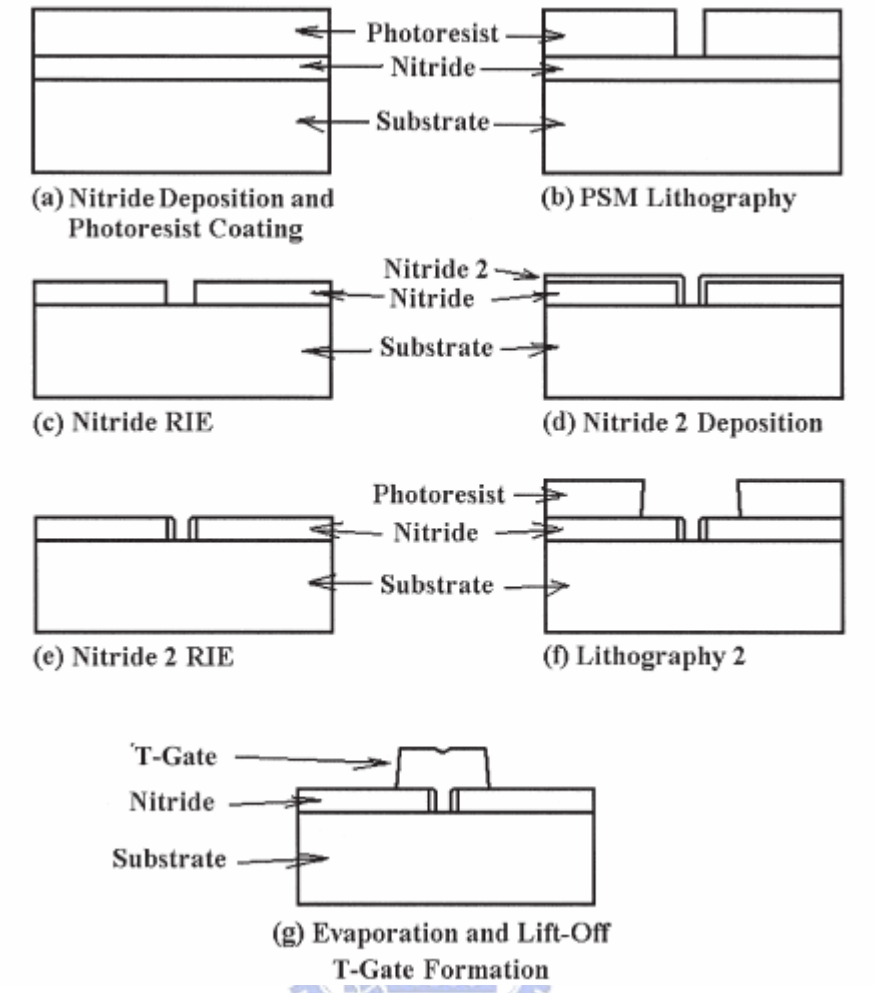


Fig. 2.6 T-gate process flow of the PSM technique

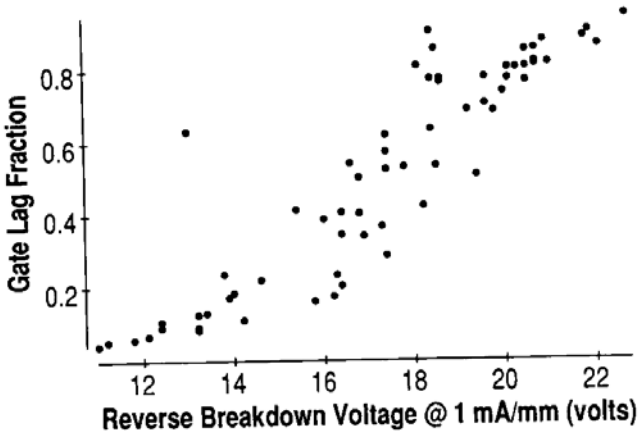


Fig 2-7. Measured gate lag fraction Vs Breakdown Voltage.

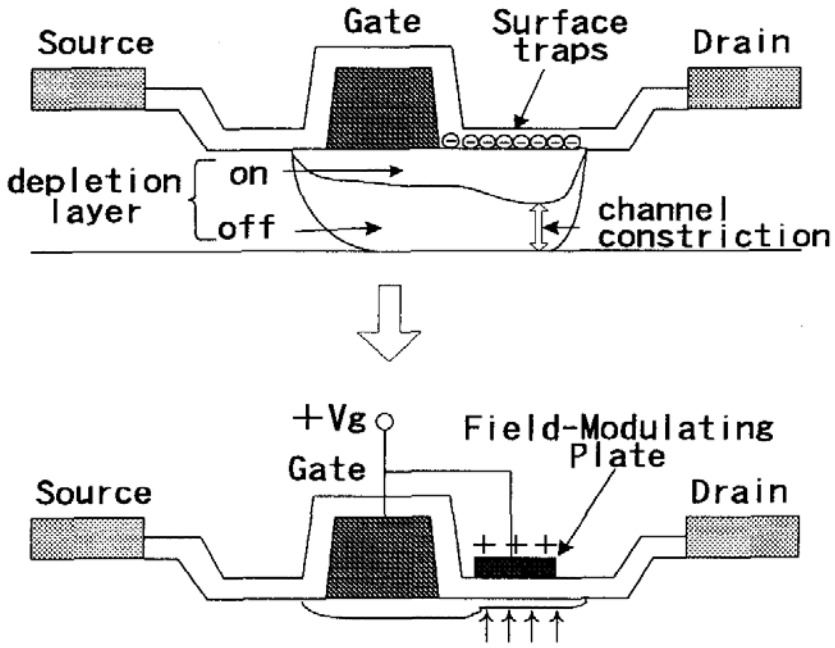


Fig 2-8. Schematic of channel constrictions caused by surface trap and after adding a field modulating plate, the channel constriction reduces.

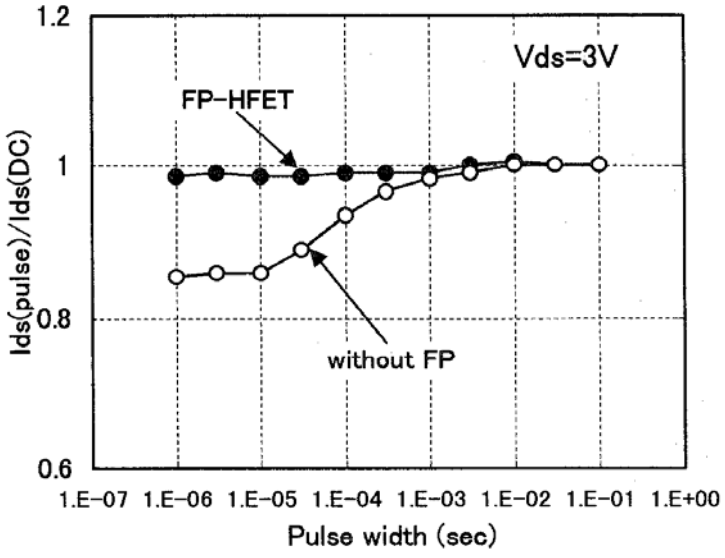


Fig 2-9. Pulse Drain current comparison between FP and conventional gate.

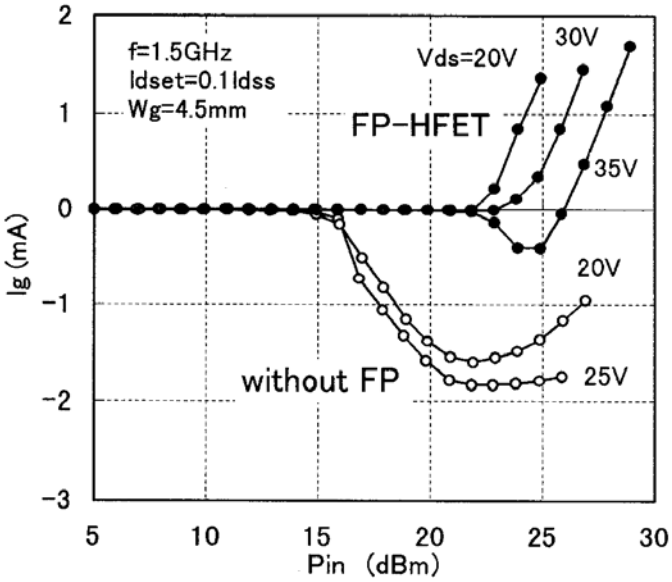
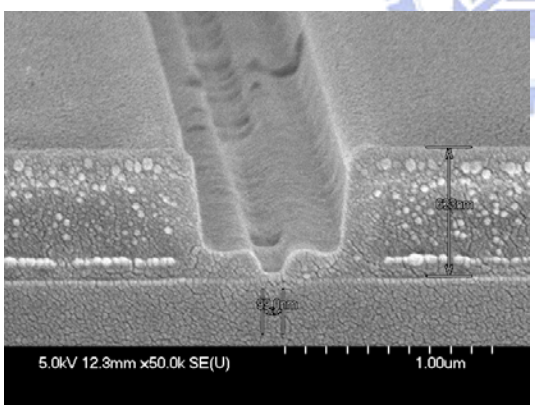
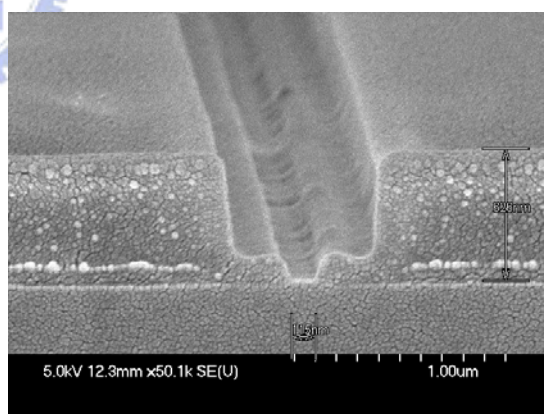
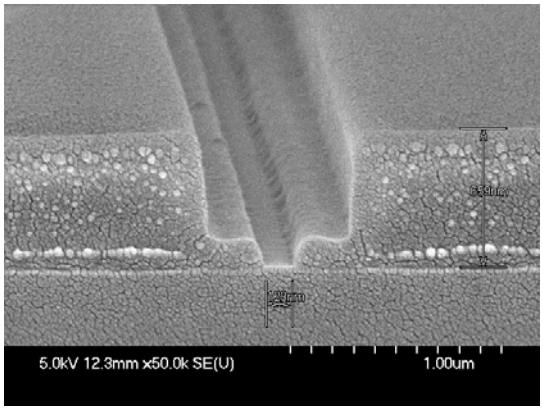


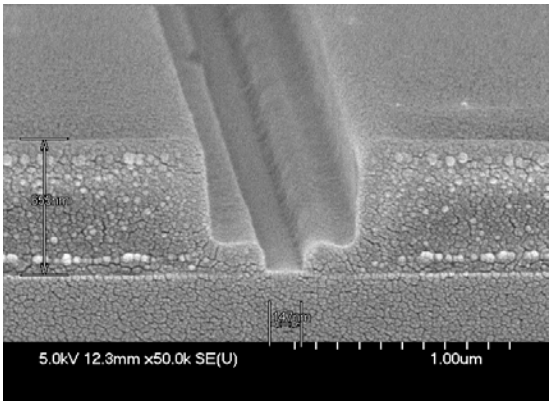
Fig 2-10 Gate leakage at several drain voltage, showing FMP-HEMT has lower gate leakage.

Fig 2.11 Dosage controlled T-gate photo resist foot print.









Chapter III
Gate Fabrication

Gate fabrication specifically discussed in detail at this chapter. Schematic diagram will make the experiment step easily being understood and reproducible even after period of time. At sub chapter 1, the OEM gate step discussed in detail and sub chapter 2 for the conventional T-gate.

3.1. Offset exposure method (OEM) gate

This idea comes out from the laser jet printing idea when it printed the test print of the printer. It has several lines which decide the precision of the printer at present time. Lithography is a kind of printing process that using the different source and processing equipment and method but has the same result.

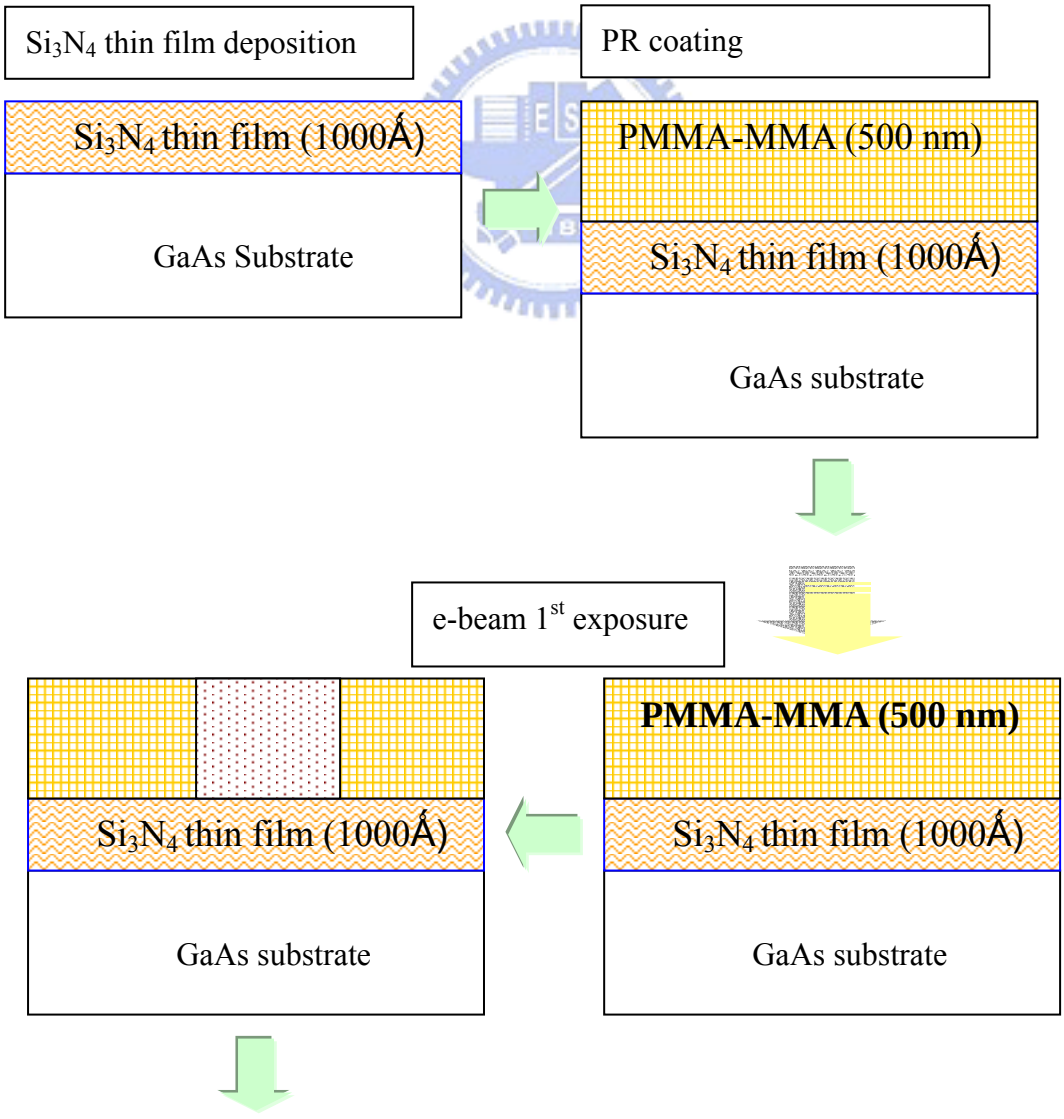
Offset exposure method adopted twice exposures using electron beam lithography system with the same dosage amount. The second exposure decides the dimensionof Lg by shifting the exposure place

neighboring the 1st exposure target area. The magnitude of shift will control the final Lg target of the photo resist. As can be seen at the schematic process flow and the figure below:

1. GaAs mechanical wafer with ohmic metal is prepared and growth with PECVD for 1000Å thickness of Si_3N_4 thin film. (Uniformity is about 1000 ± 100 Å).
2. GaAs substrate coated with single layer of PMMA-MMA, with thickness around 500 nm and baking at 200 ℃ for 3 minutes.
3. E-beam dosage test experiment has been done for 8 different dosages from 1700 μC/cm^2 to 2500μC/cm^2. The best result for the dosage is around 2300μC/cm^2 with the width around 450 nm.
4. After the 1st exposure step, the etching of Si_3N_4 thin film is the next critical step due to the radical of the reaction gas will react and influence the surface state of the GaAs. Etching rate determination test has been done using ICP (inductive Couple Plasma) etch system. ICP is being selected due to the lower surface damage after etch process compare with other systems, such as RIE and sputter. Etch rate determination experiment has been done by preparing 10 piece part wafer with same area and same pattern. Different etching time for different piece part wafer will produce the different thickness of after etch thin film thickness. The film thickness is determined by SEM cross section tilted at 45^0.
5. The etch rate has been determined from previous work, the next is the 2nd exposure step of the lithography with the shift from the first

exposure step, dosage is 2300 μC/cm^2. The 2nd exposure step used the dosage magnitude of the 1st exposure, due to the control of the Lg is limited at the shift magnitude not by other parameter such as dosage control. The PMMA-MMA is used as the same with 1st exposure, with the same temperature 200℃ soft bake for 3 minutes.

6. The result is shown in SEM picture in Chapter V. It is concluded that larger shift magnitude degrades the Lg in the senses of stability, linearity and reproduciblity.



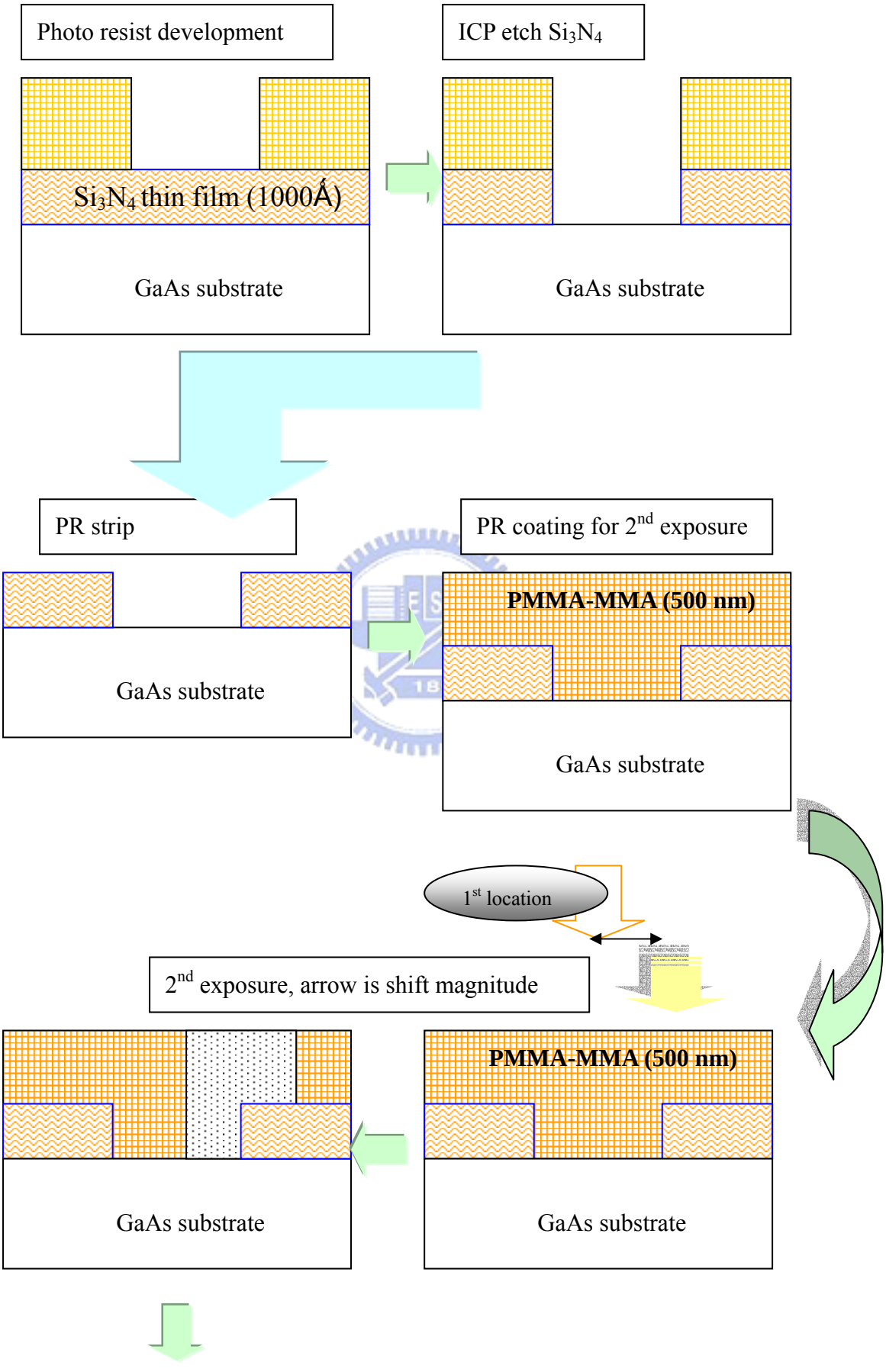
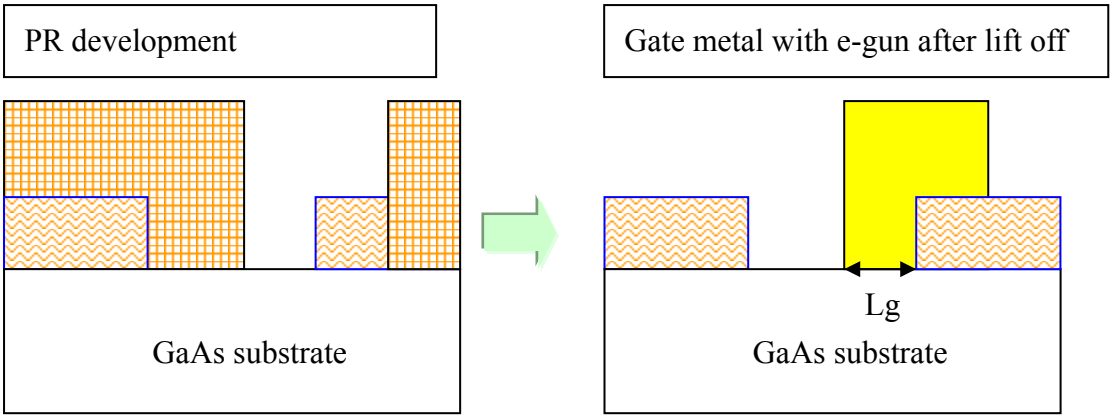


Photo resist development
ICP etch Si_3N_4
Si_3N_4 thin film (1000Å)
GaAs substrate
GaAs substrate
PR strip
PR coating for 2nd exposure
GaAs substrate
PMMA-MMA (500 nm)
GaAs substrate
1st location
2nd exposure, arrow is shift magnitude
GaAs substrate
PMMA-MMA (500 nm)
GaAs substrate



As can be seen above, the Lg determination is independent on the e-beam dosage control, but dependent on the shift magnitude. A resolution of 100 nm lower than the best of the e-beam system (200 nm)can be achieved through this method. Theoretically, it can be unlimited decrease to the smallest Lg as the magnitude increase.

3.2. Conventional T-gate

Process flow of the T-gate has been widely used in our CSDLAB. As described below, the steps are:

1. GaAs wafer coated with PMMA resist with 1st step spin speed 600 rpm for 10 sec and 2nd step 2500 rpm for 60 sec. And soft bake using hot plate at 250℃ for 3 minutes.
2. After PMMA, PMMA-MMA is coated on GaAs wafer with 600 rpm

for 10 sec and 3000 rpm for 60 sec, soft bake at 180℃ for 3 minutes. Overall photo resist thickness is measured around 7000Å± 5%.

3. E-beam exposures with the dosage around 1800 μC/cm^2 being applied for T-gate and 400 μC/cm^2 for gate pad.
4. Developed using MIBK:IPA=1:3 for 100 sec and rinse with IPA for 30 sec.
5. Gate metal Ti/Pt/Au being evaporated on the devices with thickness around 5000 Å.

Chapter IV
Device Structure and Fabrication

To study the effect of the gate fabrication, the gate is applied on the GaAs PHEMT wafer with three types of gate length. Double delta doped of GaAs PHEMT for power amplifier application has been applied for this study. The device is fabricated at CSDLAB from front side mesa to airbridge interconnect. Fabrication flow is listed at the end of this chapter step by step in detail.

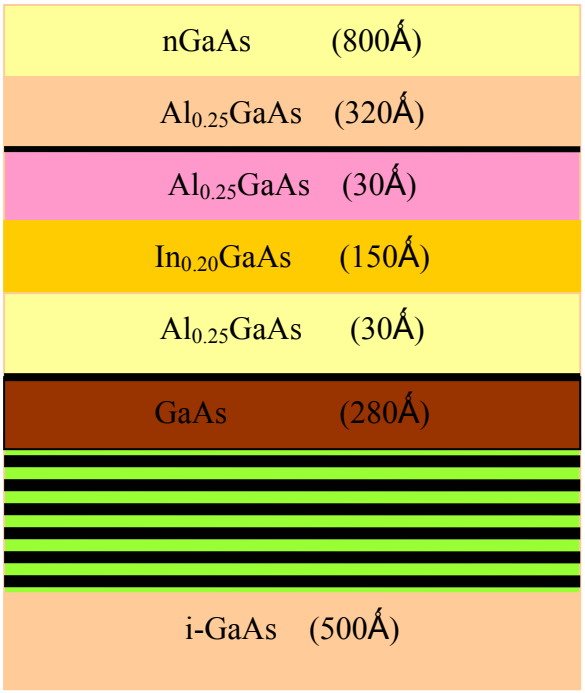
4.1. Device structure

The device is grown with MBE (molecular beam epitaxy), with the GaAs as the substrate. This Pseudomorphic HEMT (P-HEMT) structure is based on AlGaAs/InGaAs. InGaAs as the channel has the narrower band gap, so it increase the ΔEg and has better electron confinement compared to AlGaAs/GaAs base structure. AlGaAs/InGaAs is lattice mismatched by 1 to 2 %, and limited the thickness of the InGaAs to below 200Å to have the dislocation free P-HEMT. Using thicker InGaAs and higher than 25% In concentration will result in strain relaxed

dislocation that degrades the electronic properties of the channel. The maximum Al composition is also restricted below 30% because the excess DX-center will also degrade the electronic properties of the devices.

The AlGaAs is doped with Silicon using the planar doping to increase the electron concentration in the quantum well channel and electron transfer efficiency. The 30Å spacer is placed below the doping layer to increase the conduction band difference resulted in better electron confinement and higher electron velocity due to the smaller coulomb interaction between dopant and channel electron. Noise performance will be better with the addition of spacer layer between dopant layer and channel layer.

Power device structure has the double delta doped of the donor and double heterojunction device structure, which is used to increase the sheet charge density at the channel. High sheet charge enables higher current drive and power handling capability. For the power devices, the superlattice buffer layer is thicker than low noise structure, due to the breakdown voltage improvement consideration. Higher breakdown voltage enables devices to work at higher drain voltage and result in better power performance of the device. The structure is shown bwlow and the Fermi energy level in plotted in Fig4.1.



4.2 Device Fabrication

Power device has been fabricated with the 3 kinds of the gate length and field plate area for comparison. The devices are fabricated simultaneously to reduce the unnecessary parameters for the comparison data.

4.2.1 Mesa isolation

Isolation process defines the active region on the wafer for the fabrication of the device on the top of it. In these specific areas, the current flow is restricted to the desired path and the fabricated devices are isolated from each other. There are three typical ways to achieve device isolation: wet etching, ion bombardment, and selective implantation,

shallow trench isolation (STI), etc. The wet etching is the simplest way among them. Mesa isolation was done by a fluoride based solution. According to the device structure, the device was etched to the buffer layer to provide a good isolation. Finally, the etching depth was measured by α-step or surface profiler after the photo-resist was stripped and the etched profile was checked by Scanning electron microscopy (SEM).

4.2.2 Ohmic contact

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner were used to define the ohmic region and form undercut profile. Then the ohmic metals Au/Ge/Ni/Au were deposited in the appropriate composition by e-gun evaporation system with the various thickness (Au 750Å/ Ge 350Å/ Ni 200 Å/ Au 2800 Å). After lift-off process, the wafer alloyed with RTA (Rapid Thermal Anneal) at 406℃ for 30 sec in nitrogen atmosphere, source and drain ohmic contacts were formed. Au-Ge system is used due to the process stability. Au act as an adhesion layer, Ge used for doping the GaAs wafer during alloying formation to decrease the schottky barrier and easily forming ohmic contact, Ni act as the diffusion barrier layer of the As out-diffusion and the upper Au layer inward diffusion. Au is used to enhance the conductivity.

After ohmic formation, the contact resistance was measured by the transmission line model (TLM) in the process control pattern monitor

(PCM). The typical measured contact resistance was < 1 X10^{-6} Ω-cm^2

4.2.3 OEM gate process

T-shaped gates are essential to improve high frequency performance of the HEMTs. The small gate foot forms the Schottky contact with the HEMT, while the wider gate head provides a low gate resistance. For base film a 100 nm thick SiN_x film, which provides good resist adhesion and higher resolution, deposited by PECVD. Then, the copolymer is coated on nitride layer as etching barrier layer. The open size of Copolymer was about 450 nm. The resist opening was transferred into the nitride layer by dry etching as shown on Fig 4.2. The ICP etching conditions were optimized previously by Lien et.al.

Due to the power amplifier, to enhance the breakdown voltage and Power performance, double recess processing method is applied. The first recess is applied after the etching of the Nitride layer, with the nitride layer act as the etching barrier, the first recess was wet etched with Succinic Acid (SA):NH_4OH:H_2O_2:H_2O solution for having the "_/" cleavage on the cap layer (n^+-GaAs).

After the first recess formed, the resist is applied on the nitride layer for the second exposure. The numbers of the PR layer depend on the device structure, three layer for low noise amplifier structure and double layer for power amplifier structure.

4.2.4 Gate recess

After patterning the OEM gate, the 2nd recess etching was performed using pH-adjusted solution of citric acid (C.A.) and H_2O_2 mixture to etch the heavily doped GaAs cap layer and AlGaAs schottky layer. The target current after the gate recess is a critical parameter affecting the HEMT performance. In order to get the desired recess depth, the recess process was controlled by monitoring the non-gated $I_{ds.}$ After recess etching, Ti/Pt/Au gate metal was evaporated and lifted off. Chapter V shows the SEM micrograph of the cross-section of the OEM gate structure before and after gate metal deposition.

4.2.5 Device passivation and contact via formation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spaces between source-to-drain and gate-to-drain become smaller. Under such conditions, the devices are very sensitive to the contaminations (such as chemicals, gases, and particles) and damages. The passivation layer protects the device from damage during process handling (such as “airbridge”) and wafer probing. The dielectric layer for device passivation is usually SiN_x.

The SiN_x film was grown by the PECVD system. The precursors were SiH_4/Ar, NH_3 and N_2, the deposition temperature was 300℃ while

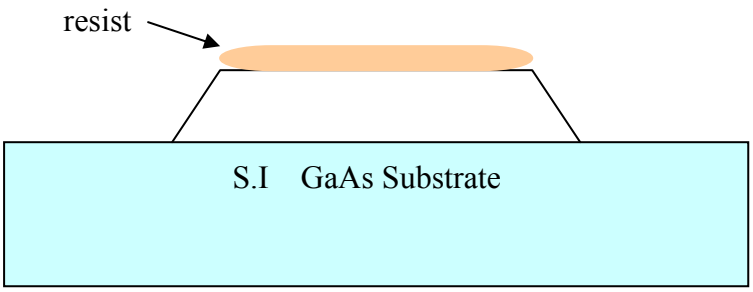
the RF power was 35 W. The thickness of the silicon nitride film was 1000Å and the reflection index was about 2.0, which was inspected by Ellipsometer. Then the contact openings of the devices were formed by photo lithography. The RIE was used to open the contact via hole region of the source and drain pads for interconnection. The plasma gases source to etch SiN_x were CF_4 and O_2.

4.2.6 Airbridge formation

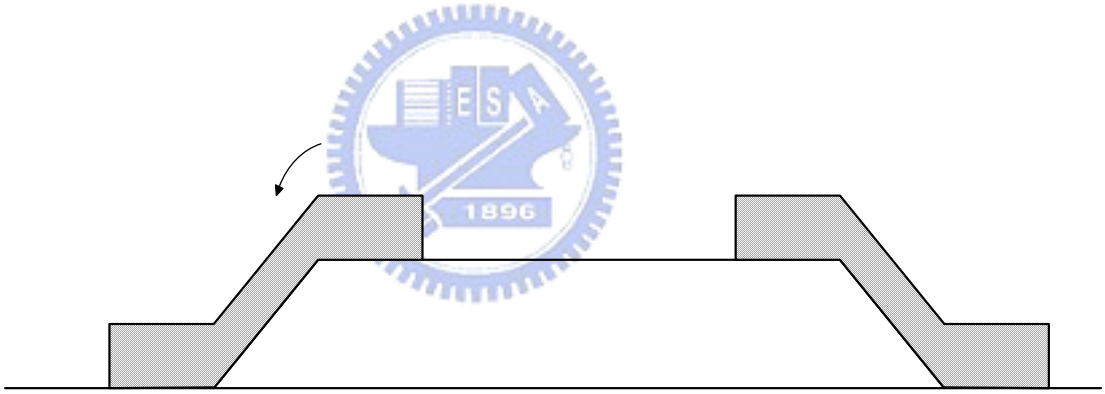
In order to reduce the total device area, finger-type layout was adopted. As a result, airbridge process was necessary to contact the fingers. The use of airbridge had several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents. The airbridge process flow is shown in the Fig. below. The first layer of photo-resist was opened at the regions of the source and drain pads. The thin seed-metal Ti/Au/Ti was deposited by e-gun evaporation system. Ti serves as the adhesion layer and Au serves as the seed layer and conductive layer for electroplating. The second layer of photo-resist was defined for the regions of the gold plated. Then, airbridge were formed after the remove of thin metal and photo-resists. The air-gap could be formed beneath the bridge, and all source pads could be connected by bridge pier. After airbridge formation, the RF characteristics of the devices were measured. The SEM micrograph of the air-bridge profile is given in Fig. 4.3. And Fig 4.4 shows the top view of the fabricated device with 8 gate fingers.

Diagram flow of the device process as shown below:

(I) Mesa isolation

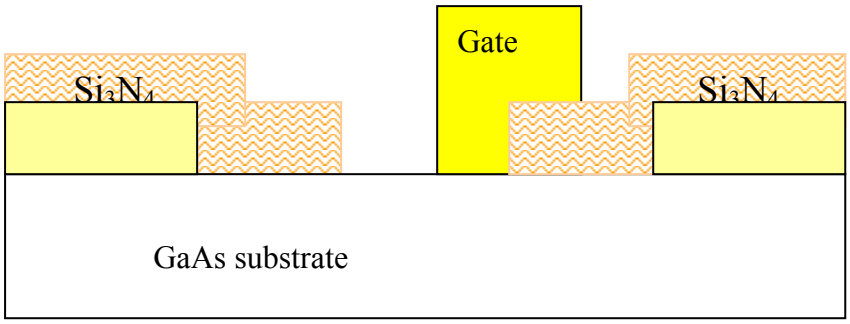


(II) Ohmic contact formation

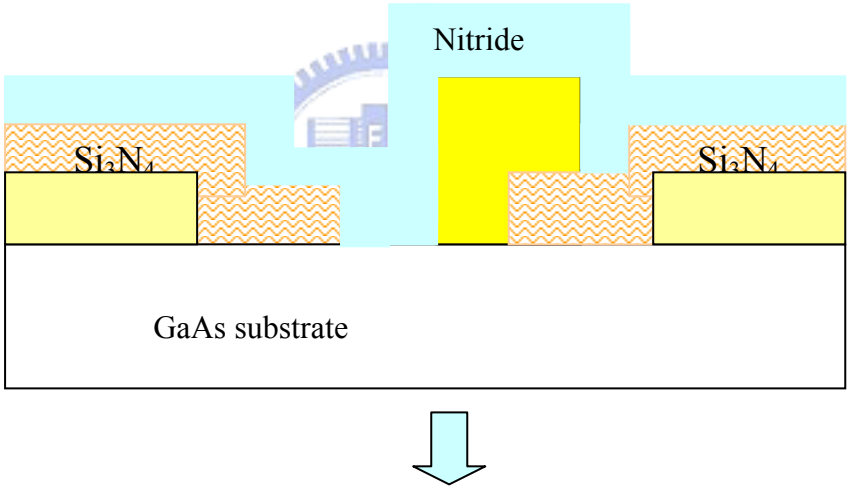


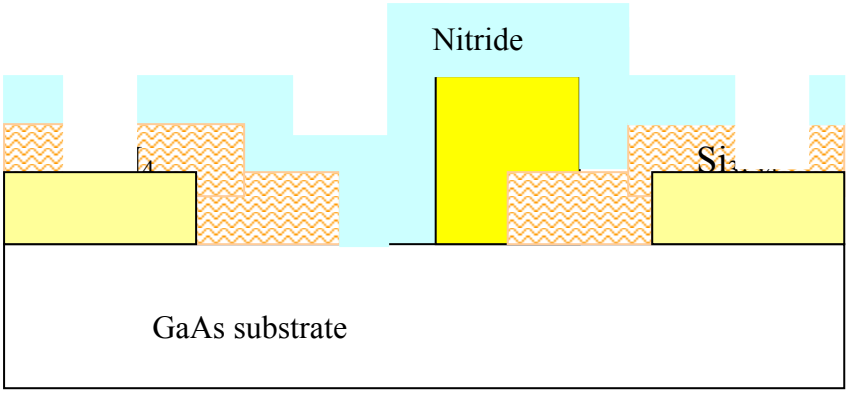
(III) OEM gate process and recess

The process has been described at the chapter III, the result diagram is shown below:

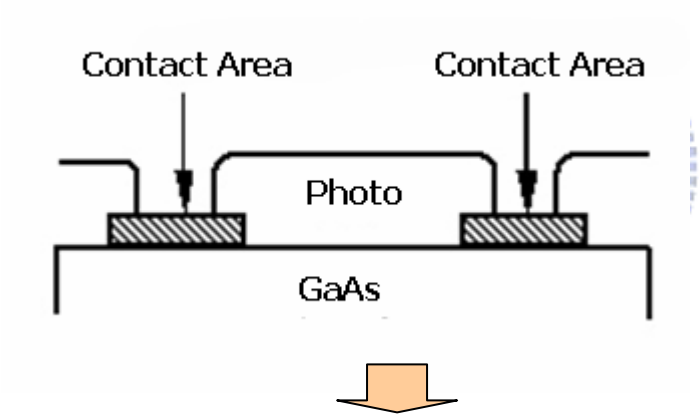


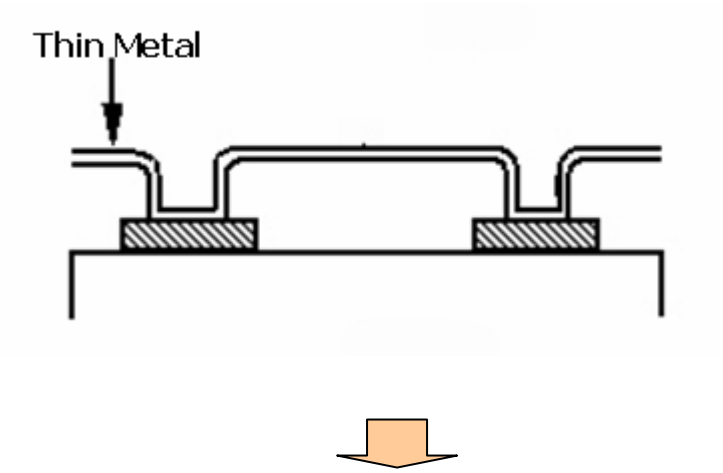
(IV) Nitride passivation and contact via





(V) Airbridge formation





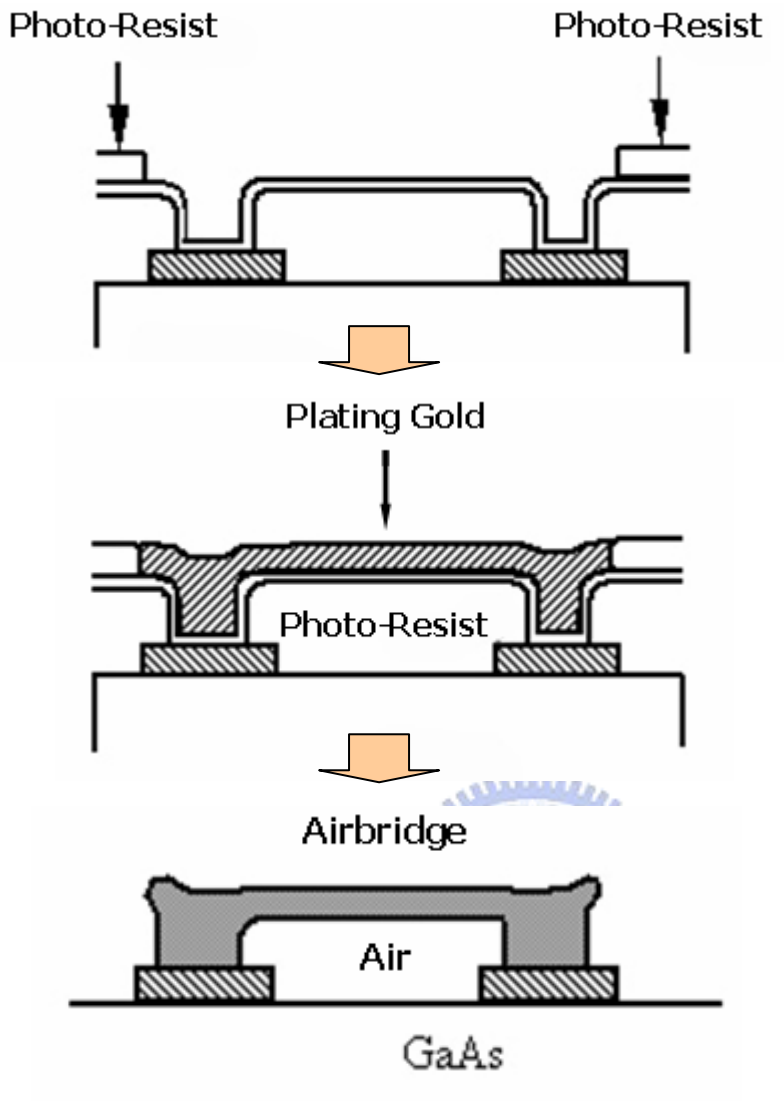


Photo-Resist
Photo-Resist
Plating Gold
Photo-Resist
Airbridge
Air
GaAs

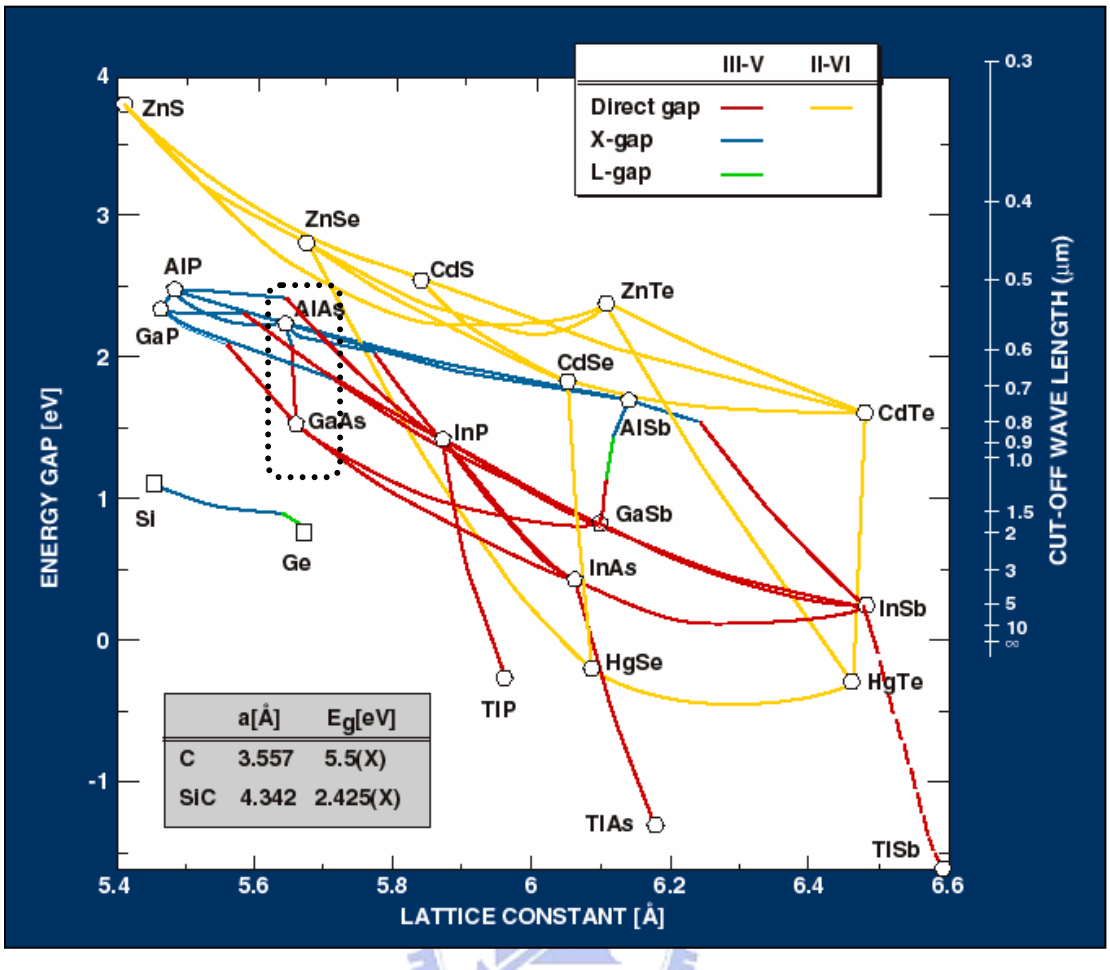


Fig 4.1(a) Lattice constant and the energy gap of PHEMT GaAs.

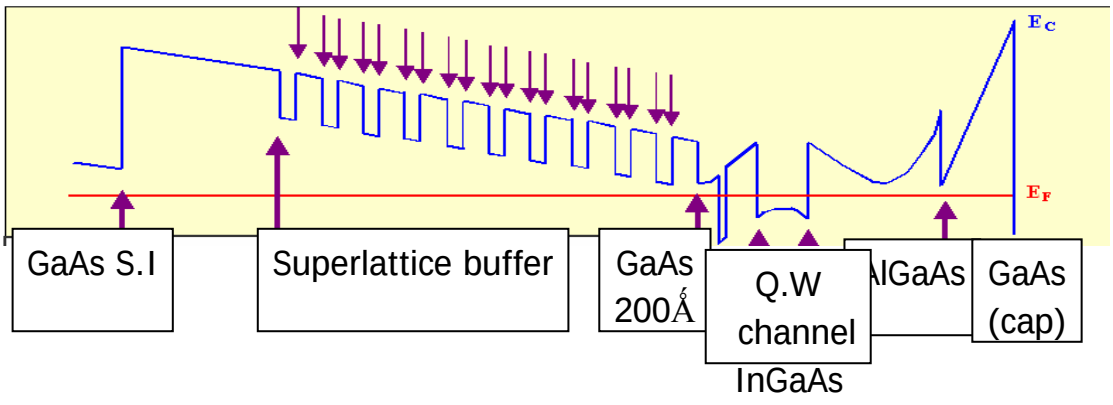


Fig 4.1(b) Fermi level distribution from cap layer to Semi insulating substrate.

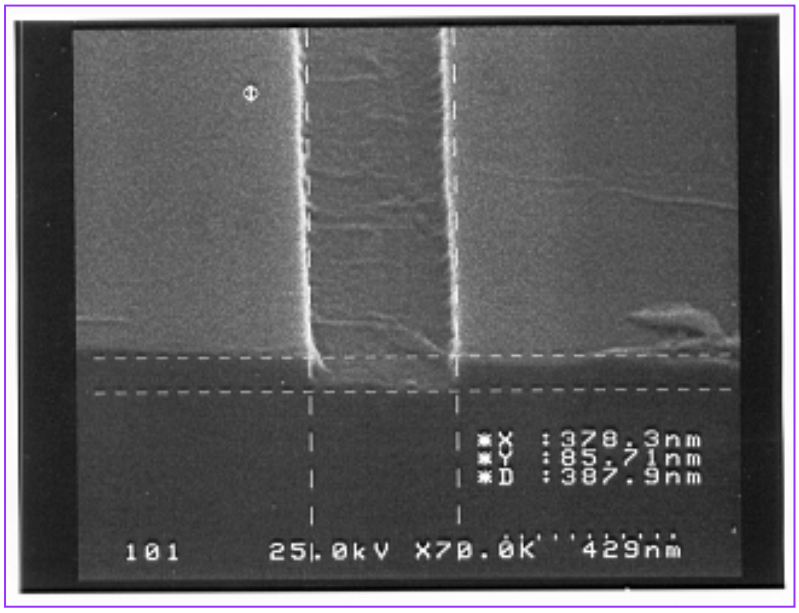
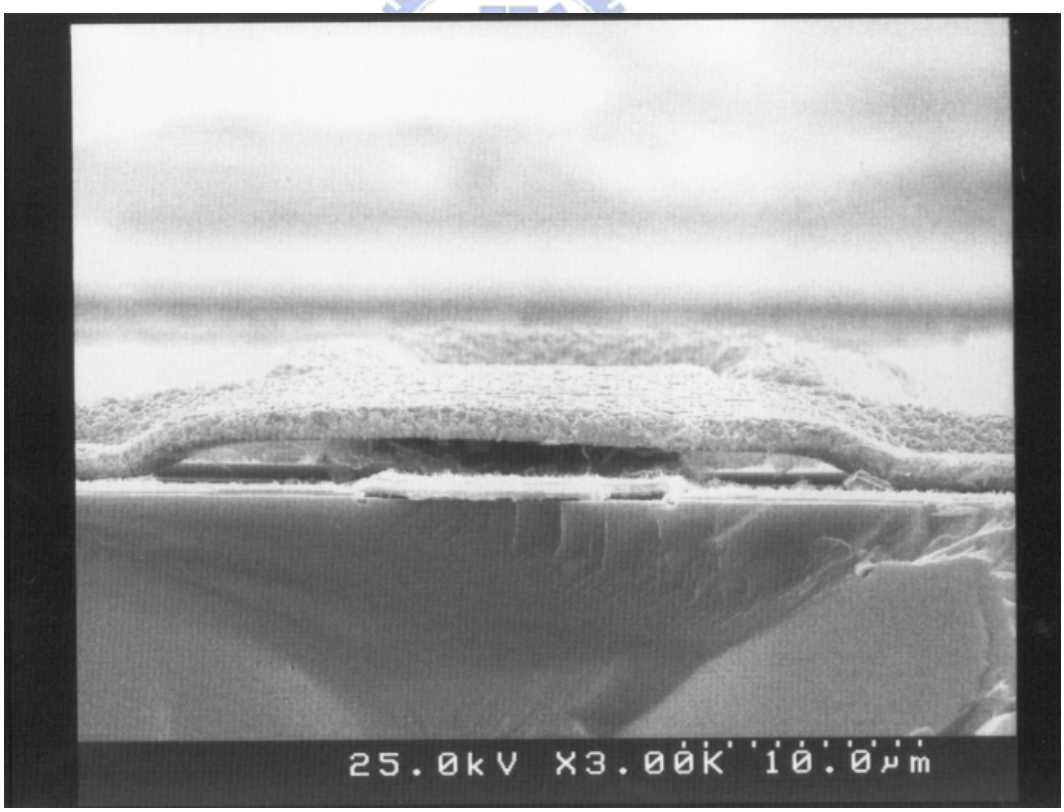


Fig 4.2 Nitride layer after etch with vertical sidewall achieved.



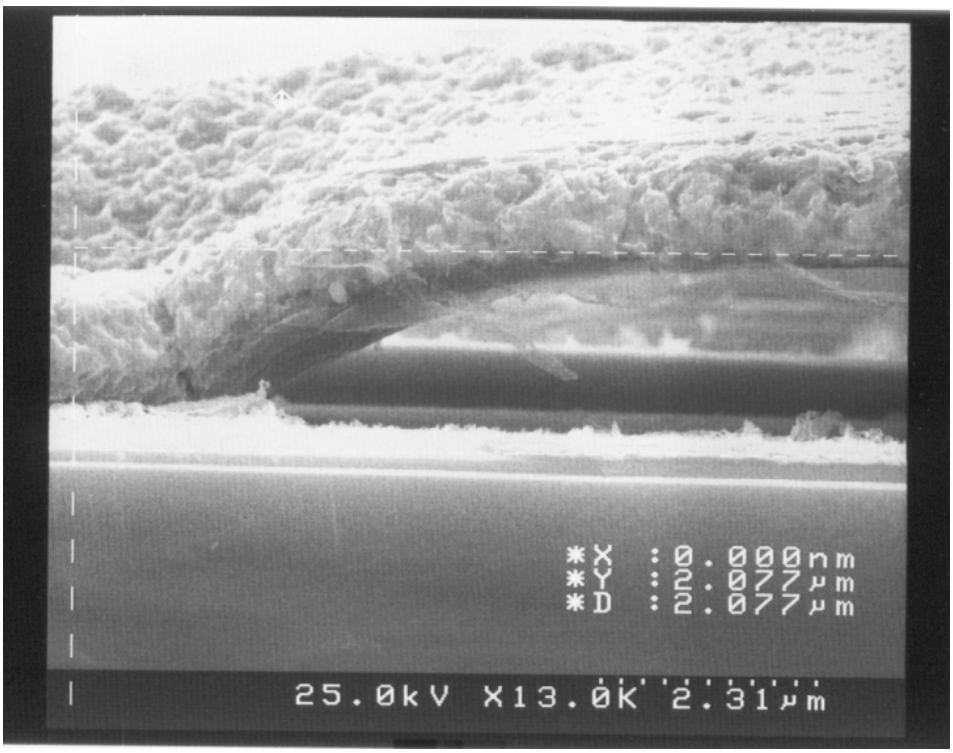


Fig 4.4 Side view of the airbridge with 2.1 μm height

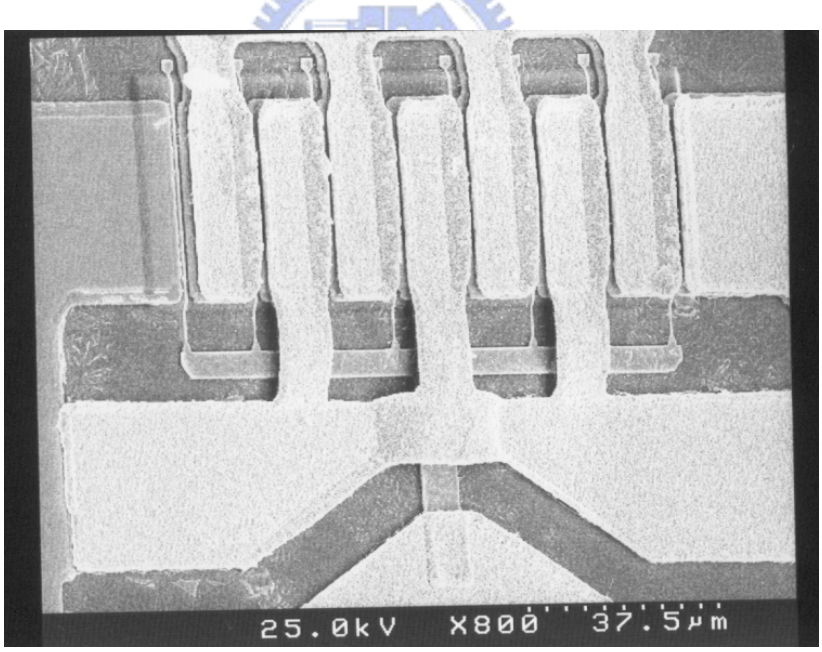


Fig 4.5 Fabricated device top view

Chapter V
Result and Discussion

This chapter discussed the devices DC and RF characteristics of the device after being fabricated and specially the gate fabrication in detail. The gate shown on SEM graph has the as small as 80 nm gate length. And three types of different gate length devices have been fabricated successfully; 80 nm 200 nm and 300 nm.

5.1 OEM gate

The gate has been successfully fabricated with different gate lengths. For the comparison purpose, I developed three types of gate with different gate length; 80 nm, 150 nm and 250 nm. The gate length is controlled by the shift magnitude, not by the electron beam dosage. The 1st step of the e-beam exposure resulted in 450 nm using PMMA-MMA (Copolymer) with the photo resist thickness around 500 nm. Copolymer is being used due to the etch resistance with thickness larger than PMMA 100 nm. The Si_xN_y thickness is around 100 nm. For the comparison between PMMA and PMMA-MMA, the

PMMA resolution is higher but not etched resisted, PMMA-MMA etching resistance performed better than PMMA.

Etching rate of the nitride has been measured with the α stepper and checked with SEM. Etch rate is 28.57Å/s, as can seen from the Fig 5.1. The depth reaches 100 nm at 35 s as been determined. Using PMMA resulted in the resist thinning, and being determined that if over etched the PMMA will be etched and resulted in the non-selectivity etch. Copolymer is thick enough for etch resistance and is used at this experiment. The resolution of the nitride after etch is similar with the photo resist, which means the side etch is not determined, From the SEM figure 5.1, we also realized that the etched profile of Nitride was smooth and asymmetric due to the optimization of ICP process. Figure 5.2 shows the etching rate determination graph.

After the 1st exposure, the 2nd exposure has been performed using the same dosage as the first exposure. The dosage has been tested from 1600μC/cm^2 to 2500μC/cm^2. The critical dosage for the photo resist opened at 1800μC/cm^2. 2300μC/cm^2 has better step profile and without residue of the resist left, with the resolution around 450 nm. Photo resist step profile has the important part compared with the resolution. Fig 5.3 shows the photo resist without the residue left.

Shift magnitude determines the gate length, shift magnitude for 100 nm has resulted 250 nm gate length resolution; shift for 200 nm

resulted 150 nm and shift 300 nm for below 100 nm gate length. The machine accuracy has been determined with the exposure of the two single lines. First line and the second line are vertical with a space between them. Exposure the first line repeatedly at the wafer, then the stage being set to zero, then the second line exposed and being checked for the shift for zero shift magnitude, the offset of the line, 32 nm, is being determined as the machine accuracy limit.

Fig 5.4 and Fig 5.5 show the side view and the top view of the resist profile and gate metal after evaporation achieved 80 nm. Statistical data has been determined from the top view of the resist profile, with the high scan rate. For the 80 nm gate length, the 3σ=44 nm; 150 nm gate length, 3σ=32 nm; and 250 nm gate length, 3σ=28 nm.

As can be seen from the statistical data above, the 3σ for the larger gate length, 150 nm and 250 nm, are around 30 nm, which is significantly due to the contribution of the machine accuracy limitation. For below 100 nm gate length, the 3σ is 14 nm larger than machine failure, due to the more critical process control.

For gate length smaller than 100 nm, tight process control should be achieved, such as etching time, gas control, chamber cleanness and photo resist dosage accuracy. Over-etching will result in the wider opening for 1st exposure due to the gas bounce back. The accurate etch parameter should be achieved for reducing this effect.

SEM inspection also affects the result due to the lower scan rate which will expose the opening and widening the photo resist profile. So high scan rate for inspection has to be used for reducing this effect. For comparison, the conventional T-gate also being fabricated with bilayer and trilayer resist shown at Fig 5.6

5.2. Device DC performance

Mesa isolation being inspected has the depth ≈ 8000 Å, Ohmic contact with Ω=5 x 10^{-7} ohm.cm^2 is measured and calculated by TLM method shown in Fig 5.7. Recess target has been selected at 625 mA/mm for ungated source drain with etch depth being inspected by SEM at 75 nm as shown in Fig 5.8. The device has been fabricated for three types of gate length; 300 nm, 180 nm and 80 nm with the gate width 40 nm for each finger. Active region area has been defined with 50 x 200 μm^2.

For the 280 nm Shift exposure gate length, the Gm and Idss are 375 mS/mm and 275 mA/mm, V pinch off at 1.2 V. 180 nm gate lengths, Gm and Idss are 424 mS/mm and 325 mA/mm. With the 80 nm gate length, the Gm behave slightly higher 485 mS/mm and Idss at 335 mA/mm. Higher Gm has been achieved for the 80 nm gate length devices. Fig 5.9 show the I-V curve of the each gate length devices with the Gm and Id_{ss} comparison.

Another important DC characteristic, breakdown voltages has been enhanced due to the application of the field modulating plate. The smaller gate length came from the smallest shift magnitude. The area of the gate on the nitride degrades as the exposure width is being set. For the largest exposure of 80 nm gate width, the enhanced gate area acts as field modulating plates (FMP).

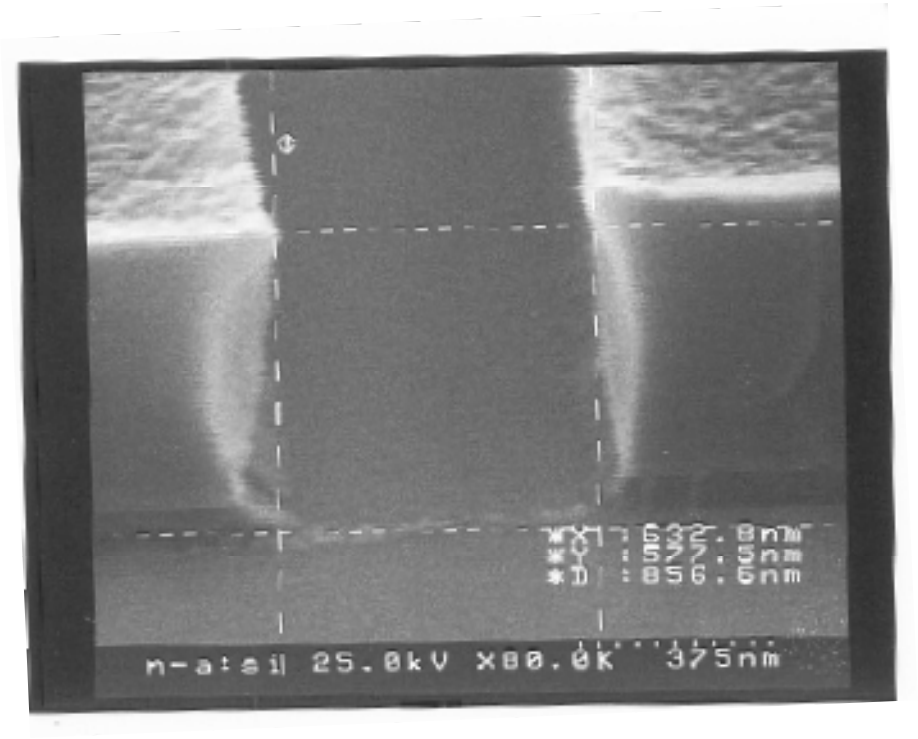
For 300 nm gate with 150 nm x 40 nm area on the nitride as FMP, the BV_{gd}=6V @ 1mA/mm, 180 nm gate with 250 nm x 40 nm on nitride, the BV_{gd} = 12V@ 1mA/mm, and 80 nm gate with 350 nm x 40 nm has the largest BV_{gd} = 18 V@ 1mA/mm. Breakdown voltage BV_{gd} enhanced as the area of the FMP increased. And it's doubled as the gate length is smallest as it has been summarized at the Table 1. and shown in Figure 5.10.

5.3. RF performance

5.3.1 Unit current gain cutoff frequency (f_T) & maximum frequency of oscillation (f_{max})

Before RF measurements, we must find the optimum DC bias to obtain the maximum current gain and power gain. *S*-parameters were extracted from 1 to 40 GHz under optimum DC bias. The extrinsic current gain cutoff frequency f_T and maximum unilateral gain cutoff

frequency f_{max} are determined from the unit current gain and the unilateral gain by extrapolating with a -20 dB/decade slope. As shown in Fig. 5-11, ft and fmax at 55 GHz and 108 GHz for 80 nm gate length. And for 280 nm gate length, the ft and fmax at 45 GHz and 105 GHz, respectively, under the bias conditions of V_{ds} = 2 V and V_{gs} = -0.35 V. Apparently, the f_T for 80 nm gate is higher than that for 280 nm gate that due to the higher transconductance value. From the load pull measurement at 2.4 Ghz, the power performance of the device has Pout = 15.85 dBm with PAE = 50% at the bias point Vg = -0.6 V and Vd = 2 V as shown in Fig 5.12. The device also measured at bias point as high as Vd = 4.5 V to prove the high voltage operation mode. Pout has reach 18.25 dBm at Vg = -0.5 V and Vd = 4.5 V with PAE = 29.7 % as shown in Fig 5.13. Lower PAE has been achieved due to the heat produced lower the device performance as the measurement is on wafer measurement. For better performance, the RF packaging for thermal treatment can be applied in the future work.



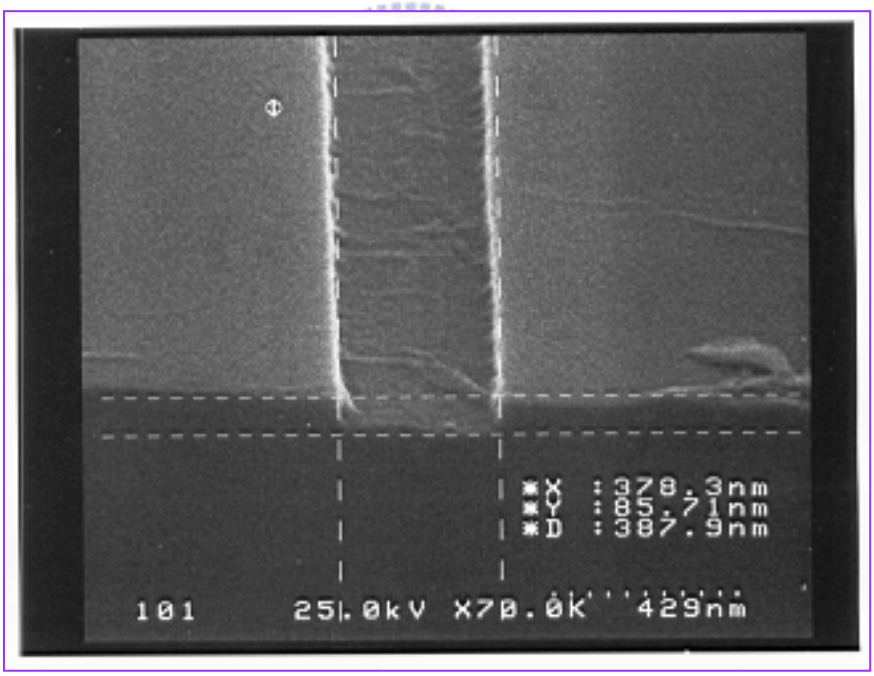


Fig 5.1 SEM picture of nitride film after etch, before and after photo resist stripped.

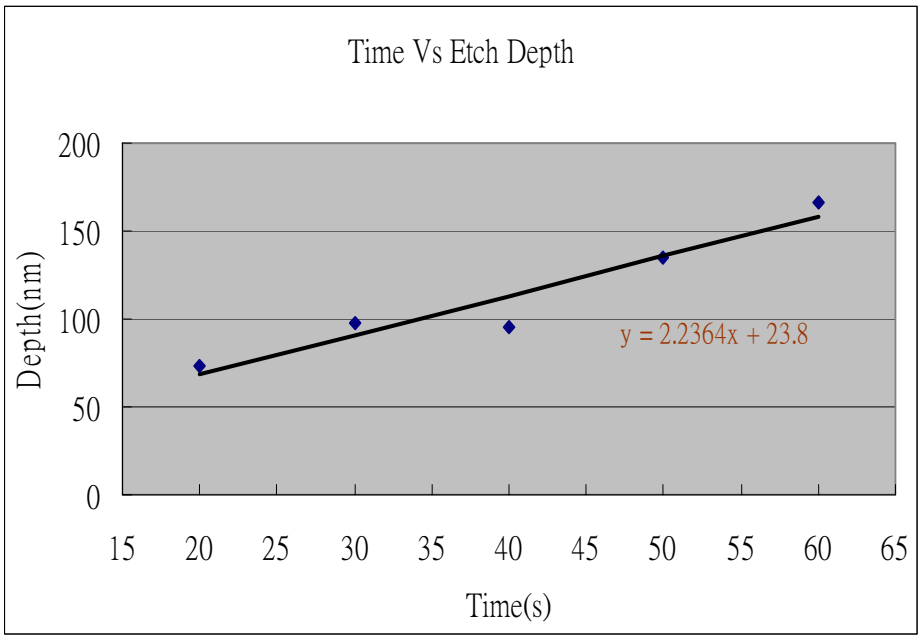


Fig 5.2 Etching depth vs time of Nitride layer using ICP with SF6 + Ar based gas system.

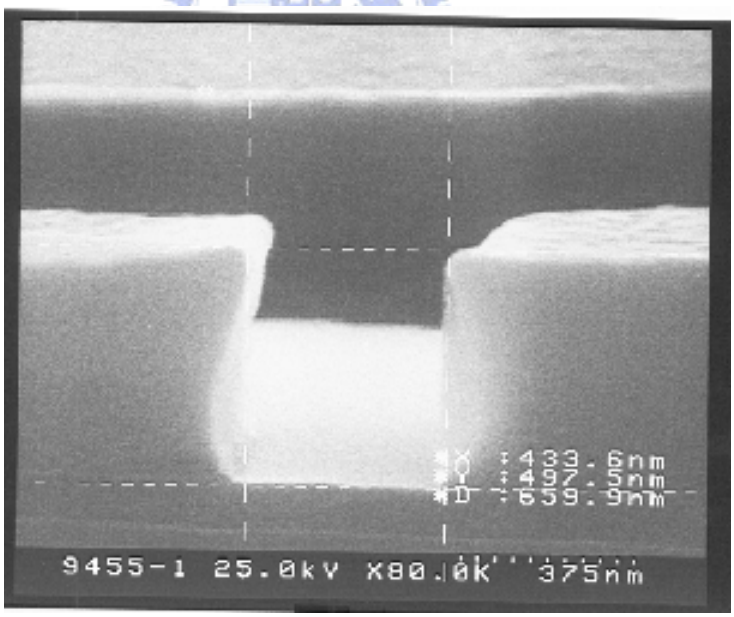


Fig 5.3 Copolymer resist after exposure on the Si_xN_y

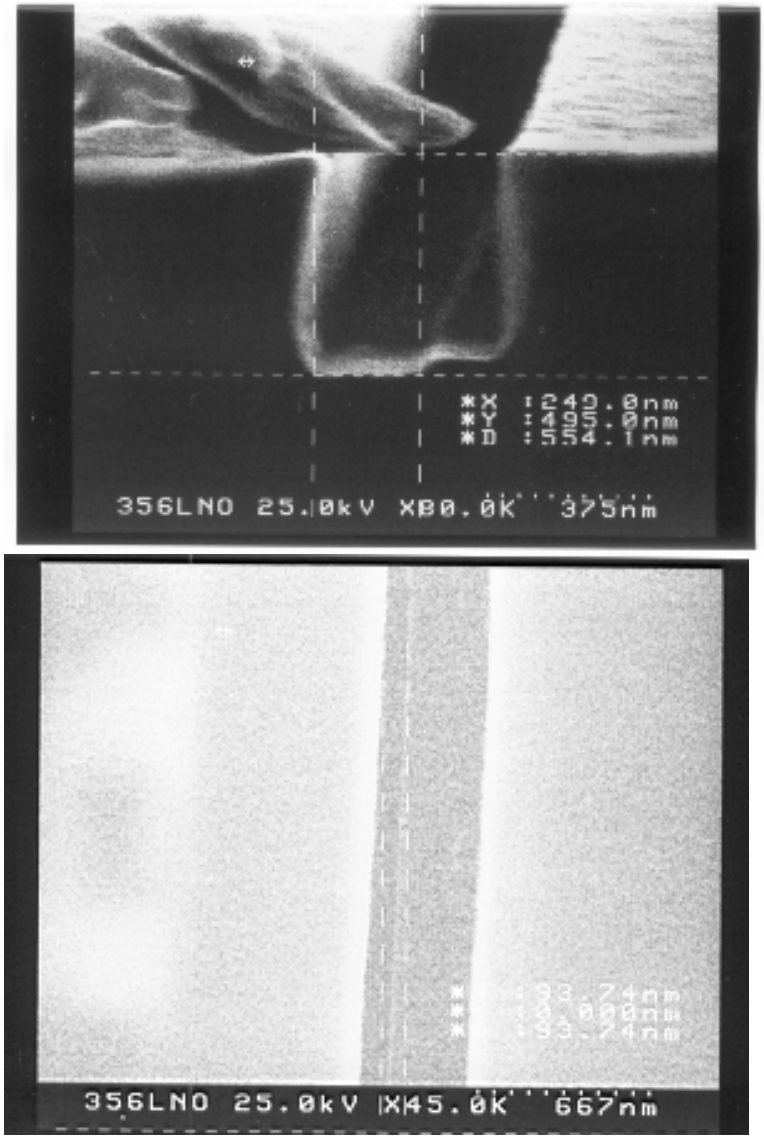
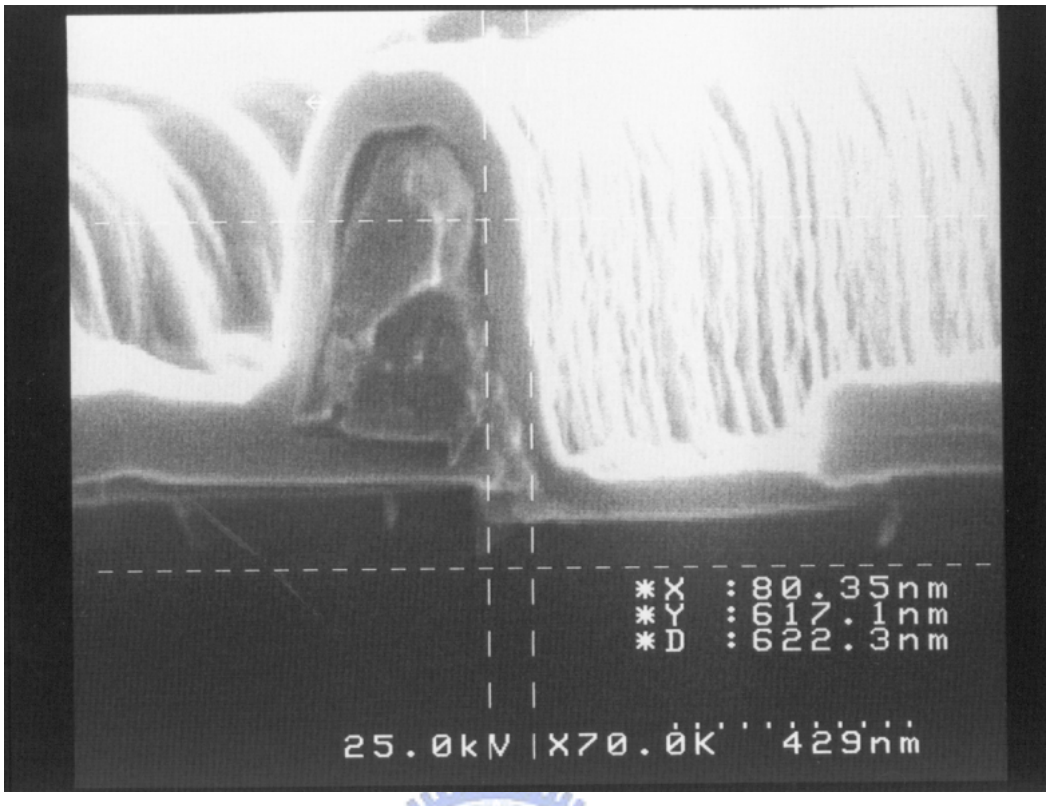
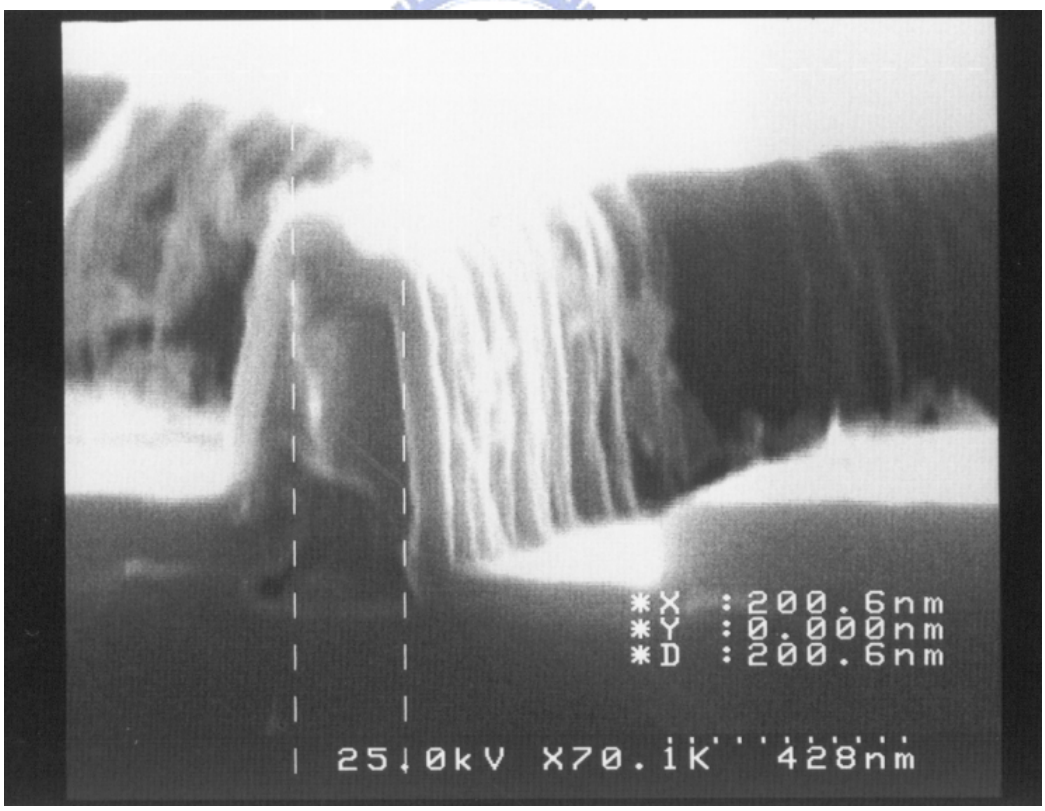


Fig 5.4 Photo resist side view and top view of the OEM gate


*X :80.35nm
*Y :617.1nm
*D :622.3nm
25.0kV X70.0K 429nm


*X :200.6nm
*Y :0.000nm
*D :200.6nm
25.0kV X70.0K 428nm

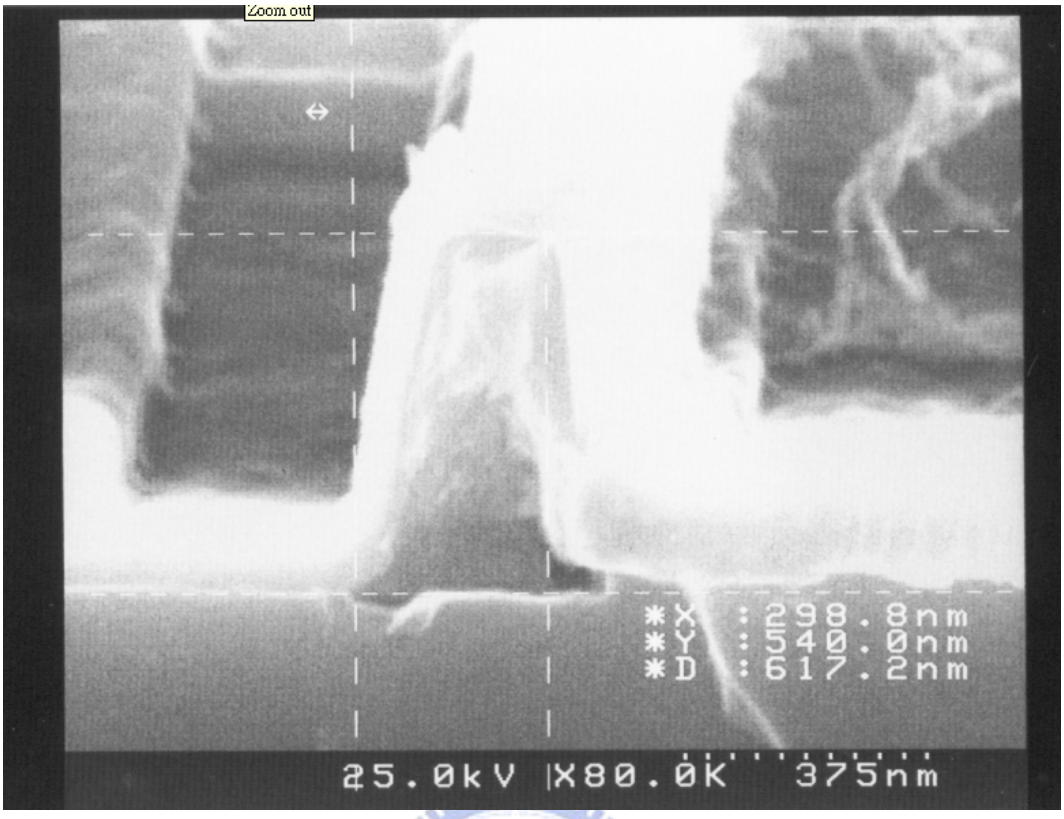
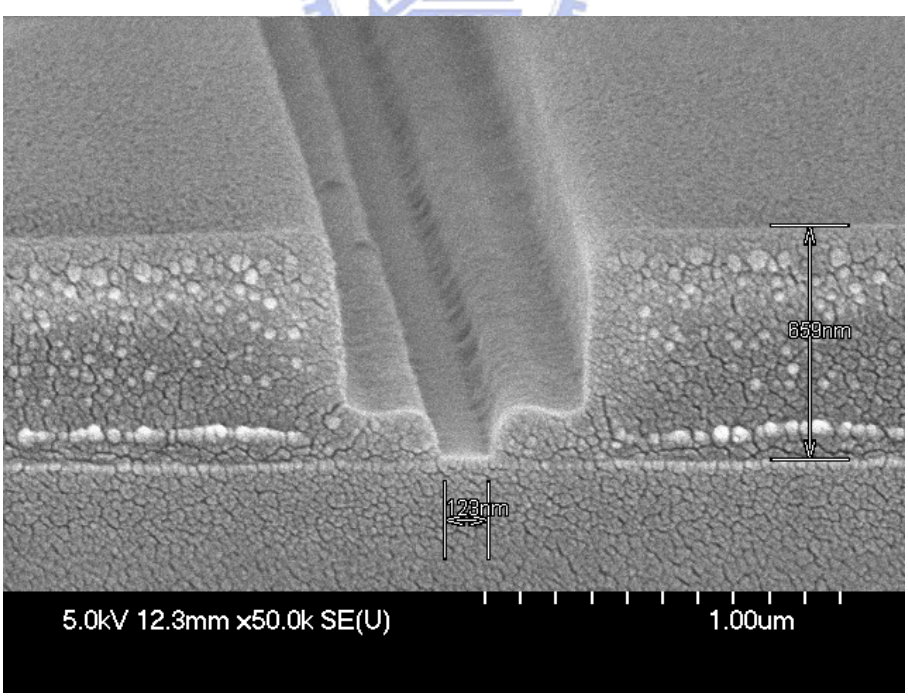


Fig 5.5 Gate after metallization with three different gate length



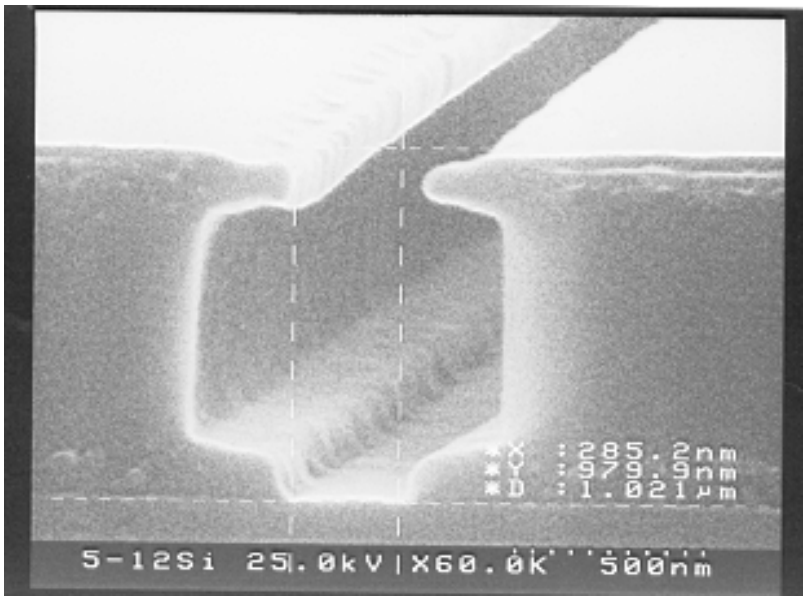
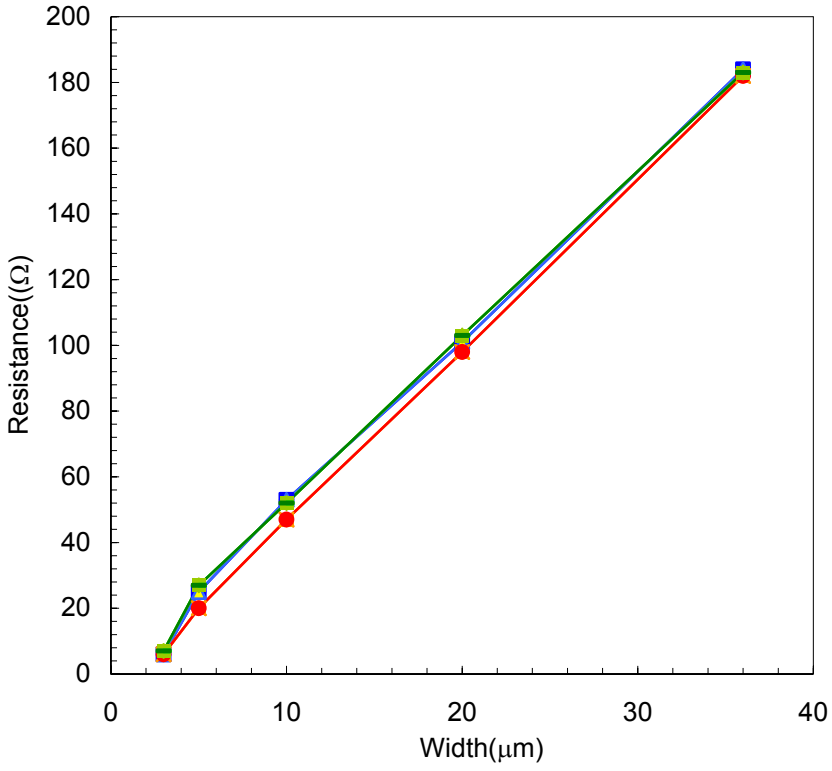


Fig 5.6 The conventional T-gate also being fabricated with bilayer and trilayer resist



6	25	53	101	184
6	20	47	98	182
7	27	52	103	183

Fig 5.7 TLM measurement with the ohmic contact at 5 x 10^{-7} Ω.cm^2

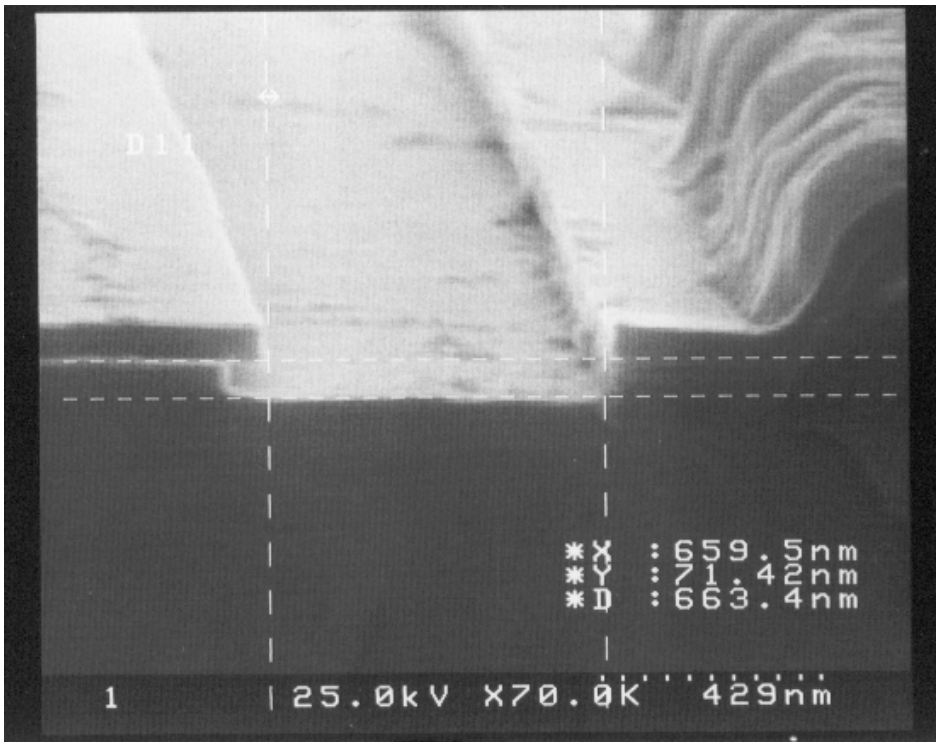
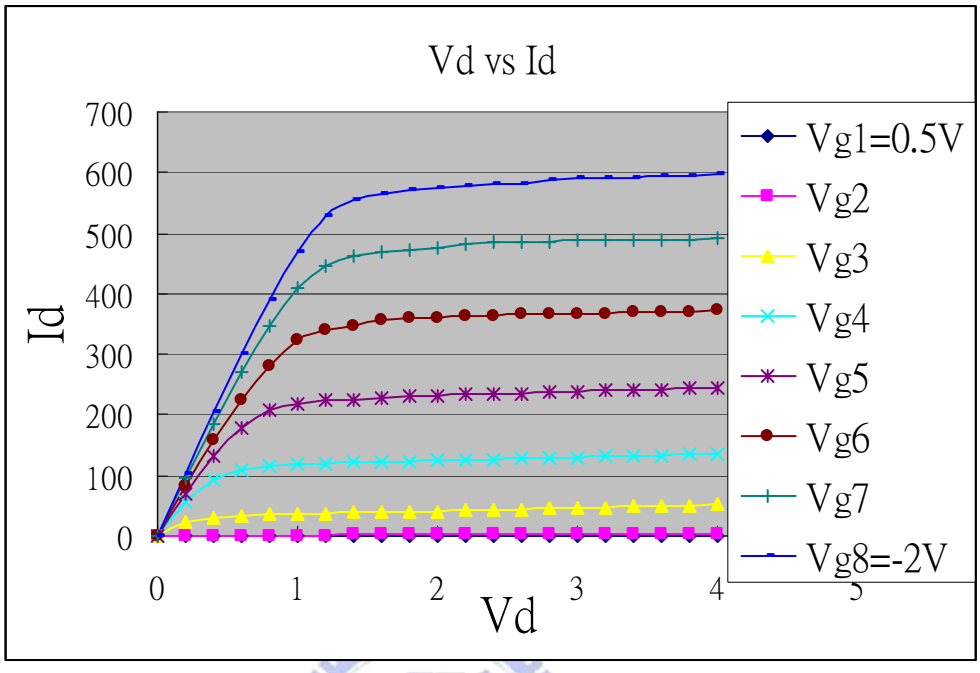


Fig 5.8 Recess depth after SEM inspection has shown the clear surface, where Nitride on the surface.

Fig 5.9(a)


Vd vs Id
Id
Vd
700
600
500
400
300
200
100
0
0
1
2
3
4
5
Vg1=0.5V
Vg2
Vg3
Vg4
Vg5
Vg6
Vg7
Vg8=-2V

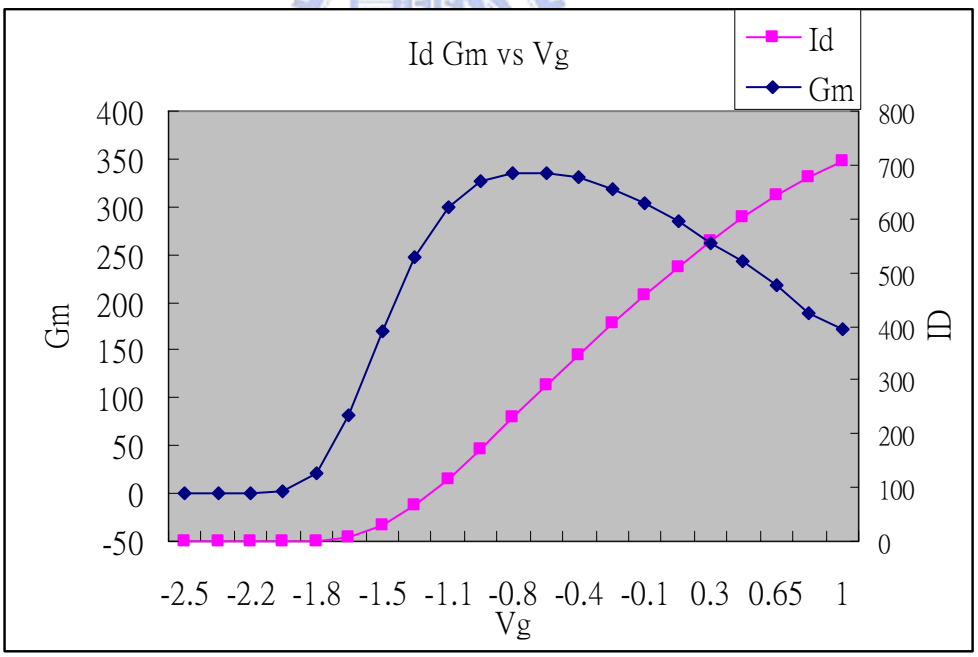
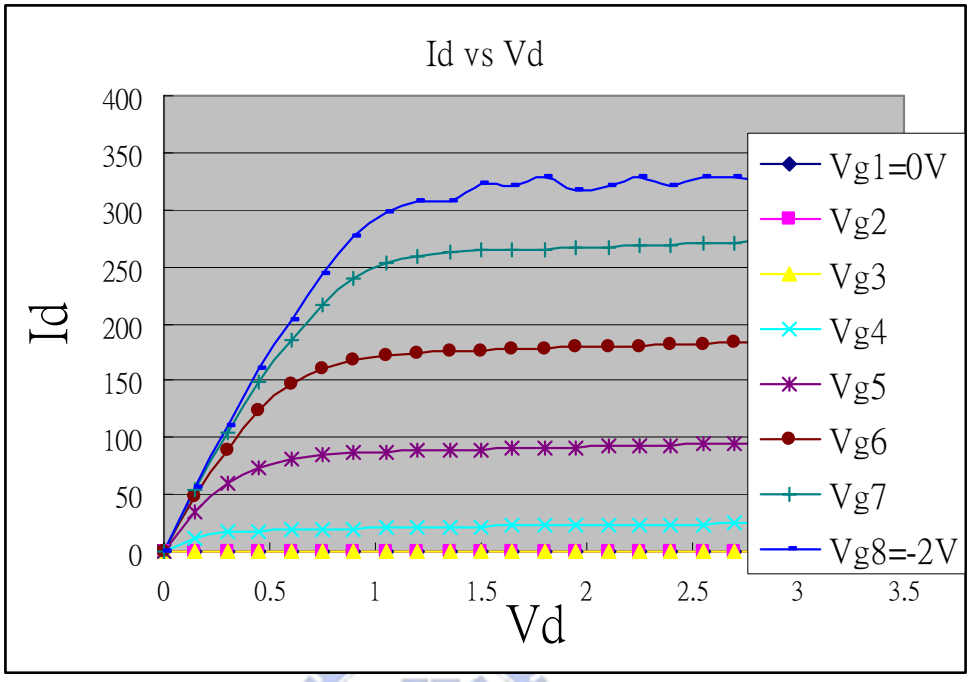

Id Gm vs Vg
Id
Gm
Gm
ID
Vg
400
350
300
250
200
150
100
50
0
-50
800
700
600
500
400
300
200
100
0
-2.5
-2.2
-1.8
-1.5
-1.1
-0.8
-0.4
-0.1
0.3
0.65
1

Fig 5.9(b)


Id vs Vd
Id
Vd
400
350
300
250
200
150
100
50
0
0
0.5
1
1.5
2
2.5
3
3.5
Vg1=0V
Vg2
Vg3
Vg4
Vg5
Vg6
Vg7
Vg8=-2V

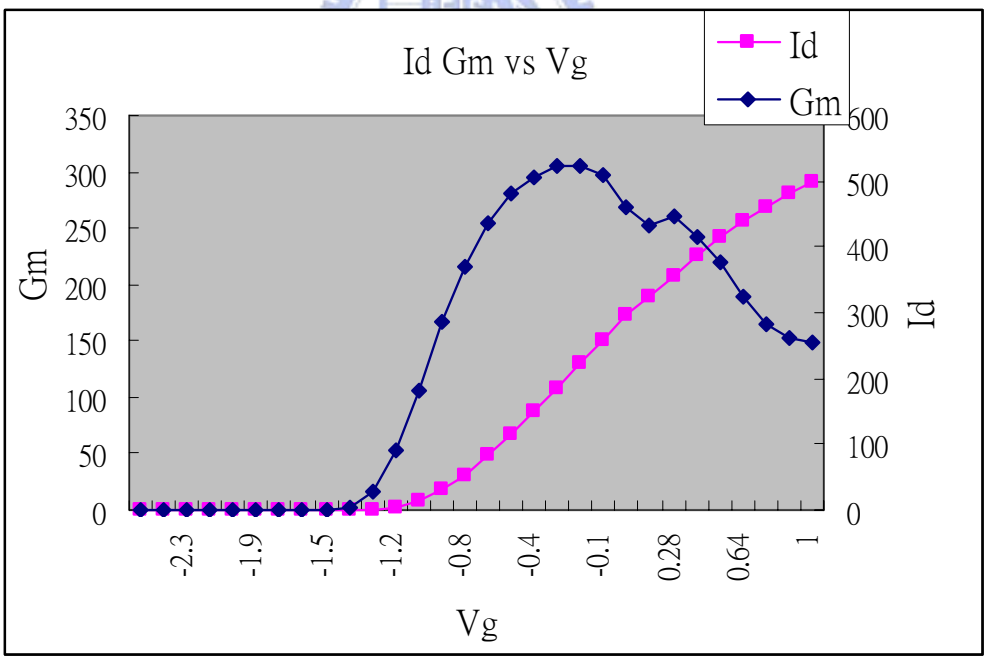
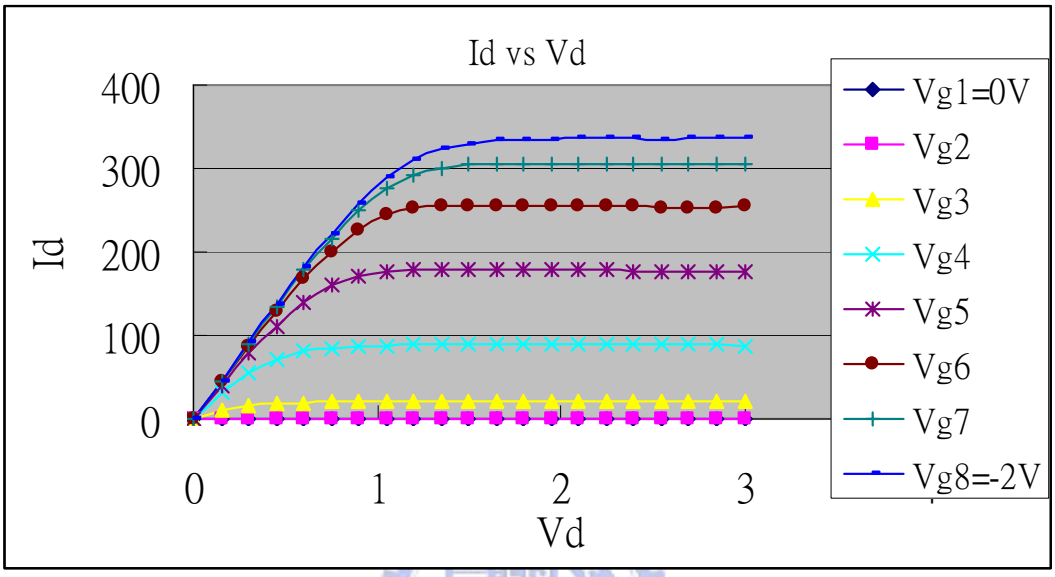

Id Gm vs Vg
Gm
Id
Vg
350
300
250
200
150
100
50
0
600
500
400
300
200
100
0
-2.3
-1.9
-1.5
-1.2
-0.8
-0.4
-0.1
0.28
0.64
1
Id
Gm

Fig 5.9(c)



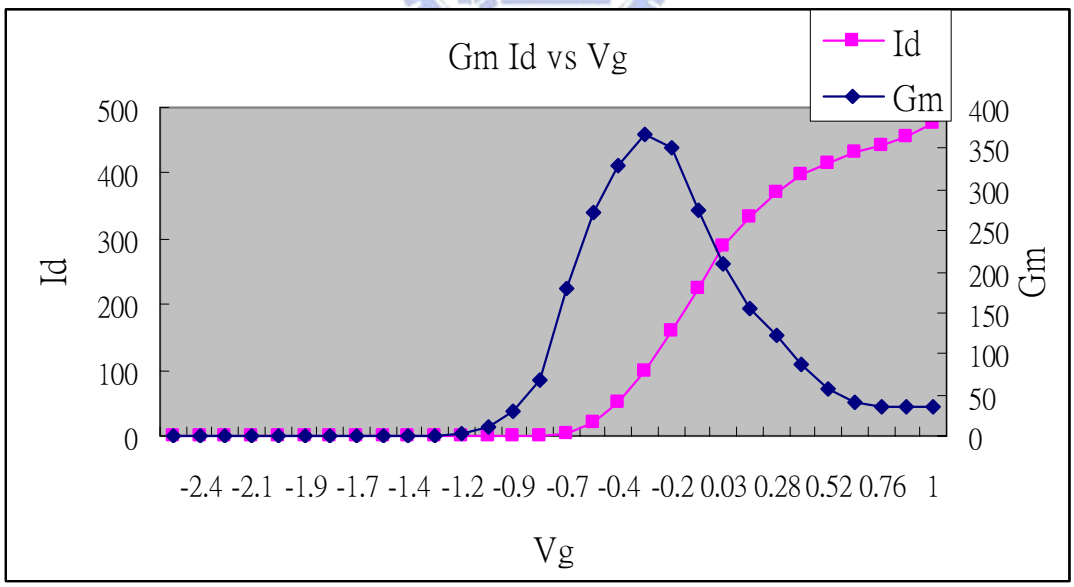
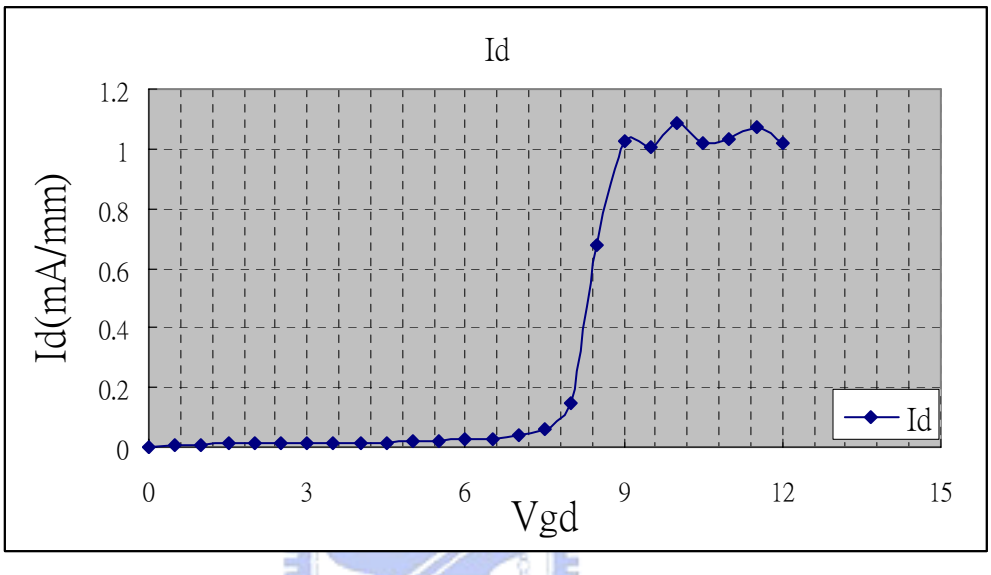
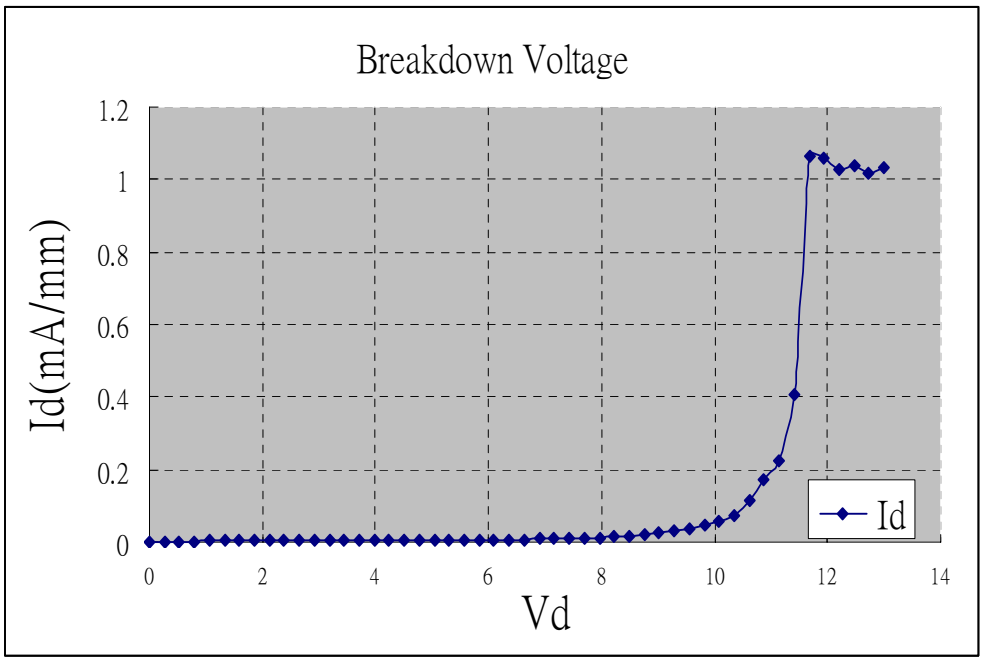


Fig 5.9 (a) I-V curve of the 280 nm gate length and ,(b) 180 nm gate length (c) 80 nm Gm and Id_{ss} for each others.

5.10(a)


Id
Id(mA/mm)
1.2
1
0.8
0.6
0.4
0.2
0
0
3
6
9
12
15
Vgd
Id

5.10(b)


Breakdown Voltage
Id(mA/mm)
1.2
1
0.8
0.6
0.4
0.2
0
0
2
4
6
8
10
12
14
Vd
Id

5.10(c)

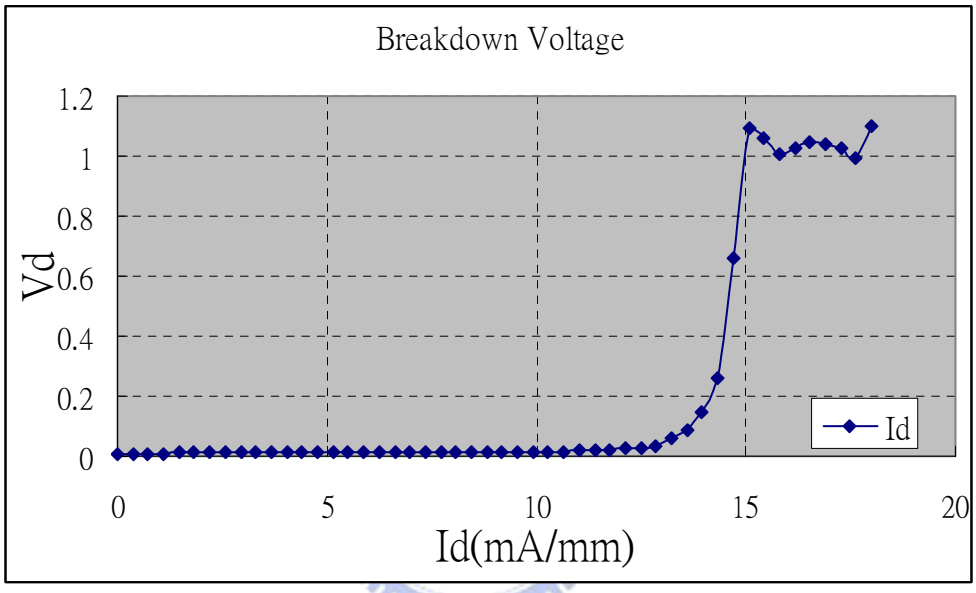


Fig 5.10 Breakdown voltage for (a) 200 nm shift with smaller area of FMP (b) 300 nm shift and (c) 350 nm shift with largest FMP area resulted in highest BV_{gd}.

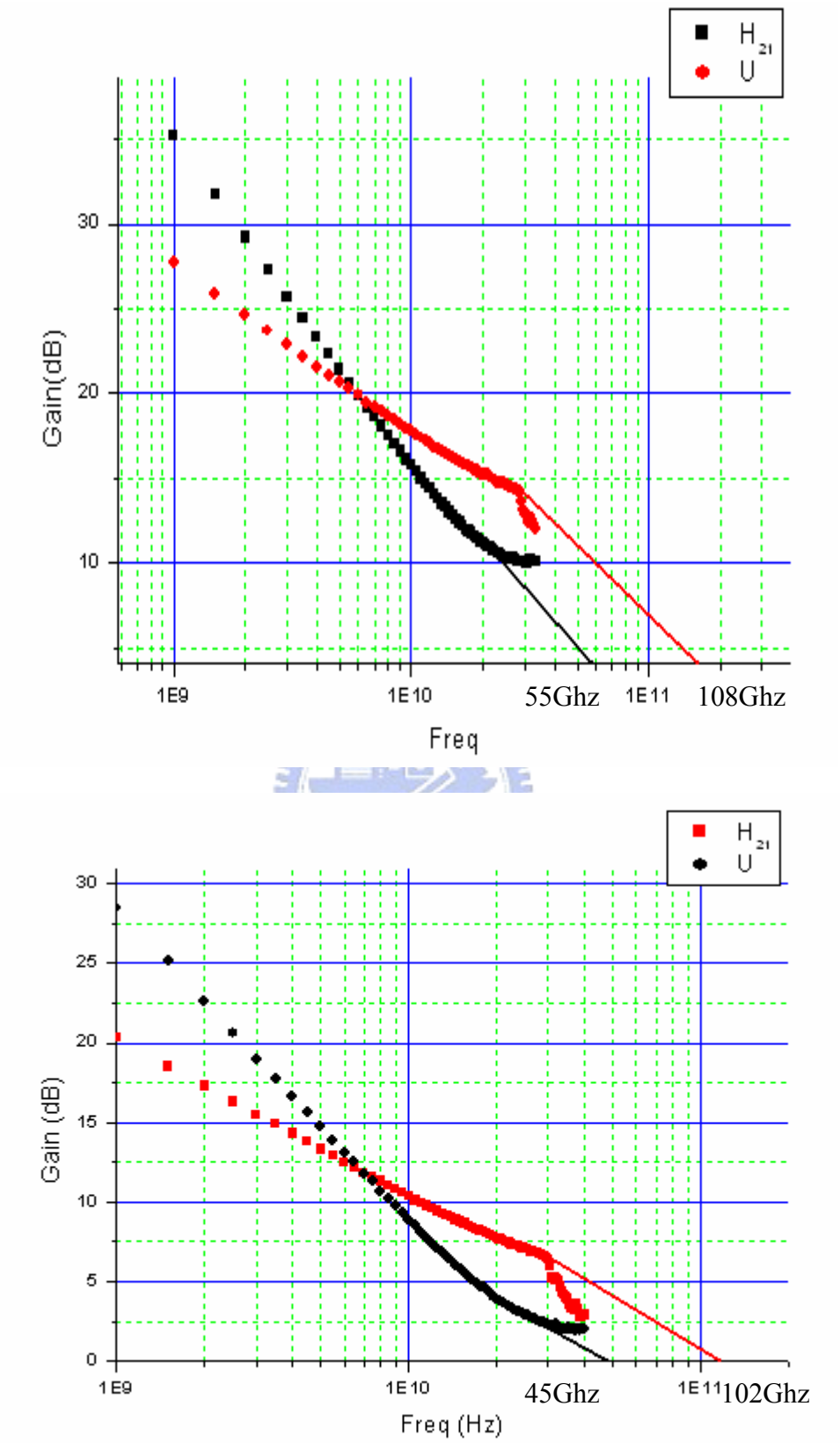


Fig 5.11 (a) 80 nm power PHEMT ft = 55GHz and fmax = 108 Ghz (b) 280 nm Power PHEMT ft = 45 GHz fmax = 102 GHz.

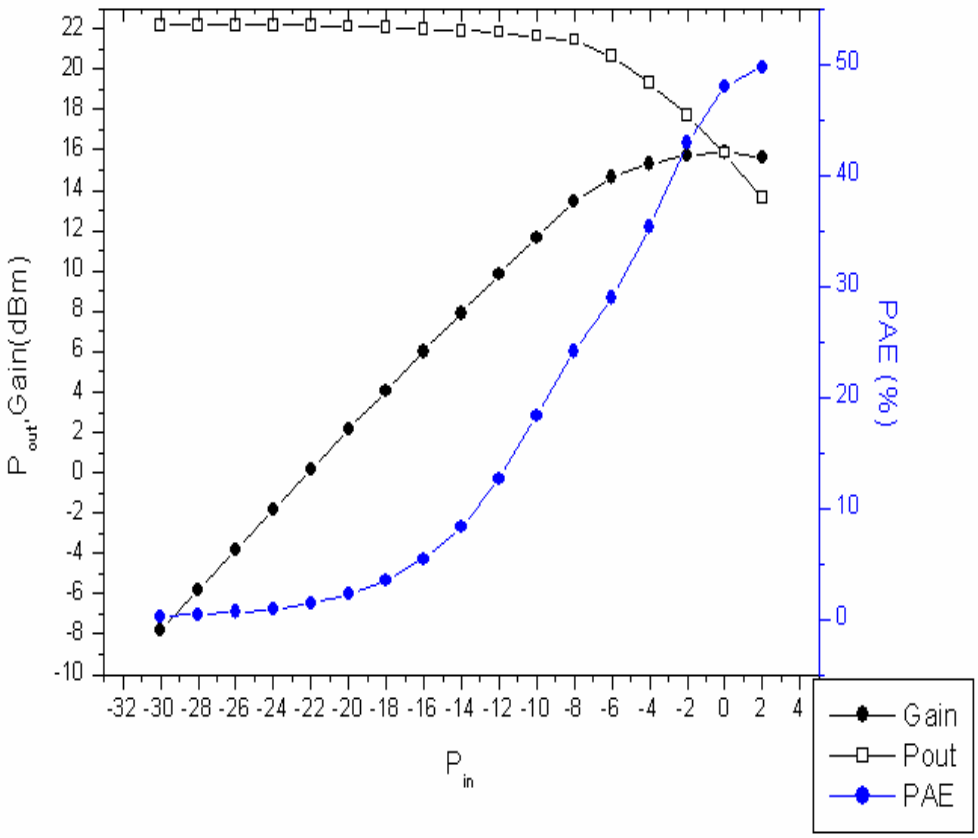


Fig 5.12 Load pull measurement at Vd = 0.5 V, Vg = -0.6 V with PAE max at 50% and Pout = 15.85 dBm

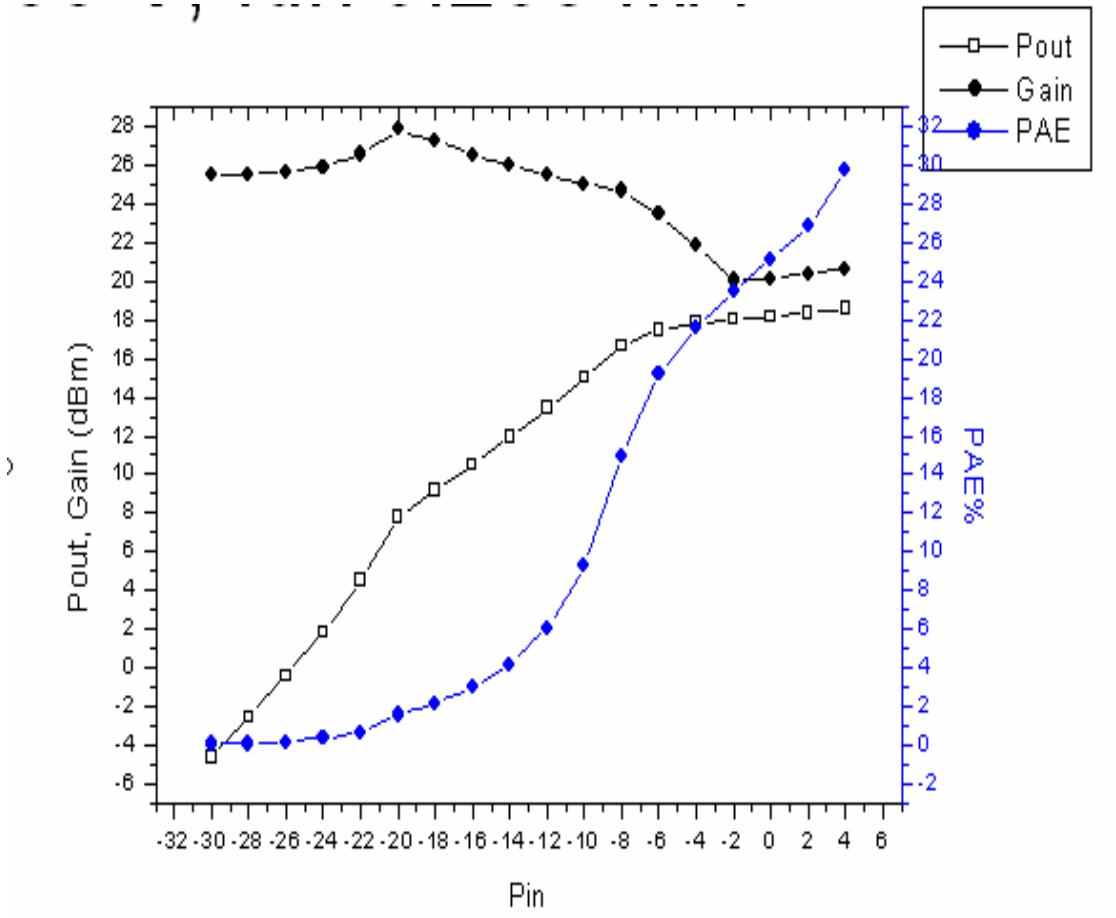


Fig 5.13 Load pull measurement at Vd = 4.5 V, Vg = -0.5 V with PAE max at 29.7% and Pout = 18.25 dBm

Chapter 6
Conclusion

The 85 nm gate length using OEM (Offset Exposure Method) has been successfully developed in this work. This method not only reduces the gate footprint of the devices but also can be used as Field Modulating plate that can enhanced the Breakdown voltage of the devices twice compared with conventional T-gate from 6 V to as high as 16 V is also being measured.

Tuning the etching parameter and the layout was the important properties at the first step of this experiment. By controlling the shift of the second exposure that being draw in the layout by using DW2000 software, the gate shrinking has been controlled without the constraint on the e beam lithography resolution. Gate lengths from 300 nm to 180 nm and to the as small as 80 nm gate has been fabricated.

Stability of this fabrication method and the reproducibility on the devices after period of time also observed. The used of the thicker resist made it being etch resisted and could not damage the Nitride thin film. Using the larger dosage and the shift controlled is the benefits due to the residue free resist at the footprint made it have the low leakage current and high through output at the gate fabrication.

Lift off property also enhanced due to the addition of the PMMA photo resist at the top of the resist that will enhanced the photo resist undercut profile without difficulty in the dosage control of the photo resist.

DC characteristics has shown that the Idss = 350mA/mm and the Gm enhanced from 375 mS/mm for 280 nm gate length to 424 mS/mm for 180nm gate length and with the 80 nm gate length, the Gm behave slightly higher 485 mS/mm and Idss at 325 mA/mm. Gm increased due to the gate length decreasing has been confirmed with the SEM picture of the device after fabricated.

RF performance also showed that the device has the ft and fmax at 55 GHz and 108 GHz for 80 nm gate length. And for 280 nm gate length, the ft and fmax at 45 GHz and 102 GHz. It proves that the gate shrinkage has improved the RF performance as been expected.

In conclusion, this fabrication method was successfully applied on the AlGaAs/InGaAs PHEMT manufacturing. The gate fabrication

has show the high stability benefit and reproducible. And the fabricated PHEMT devices have show the good DC and RF performances and were a best option for the future application on devices.