Chapter 1

Introduction

In nowadays' technical and business world, there are sharply increasing demands of military and commercial applications on low noise, high frequency amplification owing to the release of military-controlled channels and the use of these bands for signal processing. Since the signal transmission quality of the wireless communication system depends on device performance, high electron mobility transistors (HEMTs) are becoming increasingly important for high quality wireless communication and high speed electronic applications. Generally, HEMT device has superior transport properties of electrons moving along the two-dimensional electron gas (2DEG) formed at the heterojunction interface between two compound semiconductor materials, which give rise to high transconductance for operation at a millimeter-wave frequency range with lower noise.

InGaP/InGaAs pseudomorphic high electron mobility transistor (PHEMT) devices have been investigated recently for wireless communication applications. The InGaP/InGaAs PHEMT device structure consists of a thin strained InGaAs channel layer between the InGaP Schottky layer and the GaAs or AlGaAs buffer layer. The advantages of using InGaAs as the channel layer material include the greater electron mobility in InGaAs than that in GaAs, the large conduction band discontinuity which allows a higher two-dimensional

electron gas (2DEG) carrier density and thus higher current, and the improved confinement of carriers due to the quantum well. Further, the InGaP gated HEMT is selected on account of the following characteristics: (1) InGaP has wider energy gap (see Figure 1.1), hence leads to less shot noise and higher device gate-to-drain breakdown voltage; (2) the InGaP Schottky layer also does not form deep-complex (DX) center at the desired doping level as the conventionally used AlGaAs layer does; (3) the excellent etch selectivity between InGaP and GaAs materials results in better controllability for device fabrication and performance [1]. As a result, owing to the higher electron velocity and improved carrier confinement, the PHEMT device exhibits multi-functional characteristics such as higher gain, lower noise figure, higher power density and higher efficiency than a comparable MESFET or traditional AlGaAs/GaAs HEMT. Moreover, PHEMT device pretains relatively constant capacitance and tsansconductance (gm) characteristics which are necessary to attain high linearity performance. The high linearity implies that low output distortion, low harmonic level, low intermodulation distortion and high saturated output power can be achieved. These are especially significant for wireless communication applications. Therefore, PHEMT devices promise to be used in applications that demand quite low level of third order intermodulation distortion.

Multi-channel transmission is a common practice used for signal transmission in modern wireless communication systems. Nevertheless, as the operating frequencies of the system are more than two and the neighboring frequencies are located closely to each other, the device used

in this system will produce intermodulation distortion which may lead to degradation of system signal-to-noise ratio (SNR) during signal transmission. To minimize nonlinear distortion induced by the devices, device structures have to be designed and optimized for lowest third order intermodulation distortion (IM3) levels. In this study, low noise InGaP/InGaAs PHEMT devices are researched to achieve high device linearity for the wireless communication applications.

Previously published results revealed that the variation of Gm with respect to gate bias plays a dominant part in IM3 levels [4-7]. Therefore, improving the flatness of Gm profile will lead to lower IM3 levels, and thus improve the device linearity [2]. In this thesis, two different approaches, namely, the "δ-doped InGaP/InGaAs PHEMT with lightly-doped channel" and the "δ-doped InGaP/InGaAs PHEMT with uniformly doped InGaP layer", for linearity improvement of InGaP/InGaAs pseudomorphic high-electron-mobility transistor (PHEMT) devices are presented.

The DC and RF characterizations of the InGaP/InGaAs PHEMT devices with lightly-doped channel and uniformly-doped InGaP layer were measured and compared with that of the conventional δ-doped InGaP/InGaAs PHEMT. The measured performance of such devices exhibit lower IM3 level and higher IP3 attributed by the flatter extrinsic transconductance profile compared to the conventional δ-doped device. In addition, the very high IP3 to P_{DC} ratio of the lightly doped channel and uniformly doped device will have great potential for low-voltage high-linearity applications in modern wireless communications as well.

In the following chapters, the theoretical equivalent circuit analysis will be performed for IM3 estimation. Detailed fabrication process of the two different structures will be introduced. Tested DC and RF performances will be summarized followed by the conclusion of this study.

Chapter 2

Overviews of IM3 & IP3

Among all the intermodulation distortions incurred by the devices, the third-order intermodulation distortion (IM3) will dominate and determine the device linearity, therefore, the third-order Intercept point (IP3) becomes an important figure of merit for the devices linearity specification used in the wireless communication applications.

2-1 One-Tone Input Signal Test [9]

In ideal and noiseless situation, transmitted signal can be recovered at receiver. When a one-tone signal consisting of a sinusoid as shown in equation: (2.1) is inputted into a linear device,

$$V_i = A_i \cos(wt) \qquad (2.1)$$

Ideally for extremely linear device, a frequency sweep of the stimulus can only produce output signal with changes in amplitude at the same input frequency, and the output signal can be expressed as

$$V_o = A_o(w) \cos(wt) \qquad (2.2)$$

However, in real transceivers, nonlinear devices generate nonlinear distortion. This one-tone sinusoid test can be also directly applied to a nonlinear device under test but the output becomes consequently more

complicated due to the nonlinear behavior of a real device.

The nonlinear device's output voltage may be approximated by the polynomial expansion as:

$$Vo = k1Vi + k2Vi^2 + k3Vi^3 + \cdots\cdots \qquad (2.3)$$

then substitute equation (2.1) into (2.3) gives

$$V_o = \frac{1}{2}k2Ai^2 + \left(k1Ai + \frac{3}{4}k3Ai^3\right)\cdot coswt$$

$$+\frac{1}{2}k2Ai^2\cdot cos2wt + \frac{1}{4}k3Ai^3\cdot cos3wt + \cdots\cdots$$

$$= \sum_{k=0}^{\infty} A_{ok}(w, A_i)\cos(kwt) \qquad (2.4)$$

As a result, the output signal amplitude will no longer be a scaled replica of the input signal level A_i, A_o will be determined by the frequency of the input signal and will also nonlinearly vary with the input signal level. Moreover, the device will generate new frequency components located accurately at the harmonics of the input signal.

As observed, the nonlinear device could convert input signal amplitude variations into output signal amplitude. The relation between the output signal amplitude of the fundamental frequency, k=1 in form (2.4), with the input signal amplitude of the fixed input signal frequency could be examined. Therefore, an important figure of merit called the 1-dB compression point, P1dB can be used to characterize gain compression of a nonlinear device. It is defined as the output signal

power level at which the signal output is compressed by 1 dB, as compared to the output power that would be obtained by directly extrapolating the small signal's linear characteristic as shown in Figure 2.1

$$P_{1dB}(dBm)=G_{1dB}(dB)+P_{IN}(dBm) \tag{2.5}$$

where G_{1dB} is defined as the power gain where the nonlinearities of the device reduces the power gain by 1dB over the small-signal linear power gain [10]:

$$G_{1dB}(dB)=G_0(dB)-1 \tag{2.6}$$

Substituting Eq. (2.6) into (2.5) yields

$$P_{1dB}(dBm)-P_{IN}(dBm)=G_0(dB)-1 \tag{2.7}$$

where $G_0(dB)$ is the small-signal linear power gain in decibels.

2-2 Two-Tone Input Signal Test [9]

Since single-tone signal input into well-behaved nonlinear devices can just produce new output components located harmonically to the input frequency, this test is not a good tool to characterize significant nonlinear distortion figures of merit. That is, no spectral regrowth can be observed in narrowband wireless communication systems. So, any interference inside the tested spectral channel or in other closely located channel can neither be measured.

The two-tone characterization test is adopted to overcome the problem. In this test, the input signal is consisted of two signals with the same amplitude (A) but with two different but closely located frequencies as:

$$Vi = A\cos\omega_1 t + A\cos\omega_2 t \tag{2.8}$$

Substitution of the two-tone input signal into (2.3) gives the following expression

$$V_o = k_1 A \cdot \left(\cos\omega_1 t + \cos\omega_2 t\right) + \cdots\cdots + k_1 A^2 \cos(\omega_1 - \omega_2)t$$

$$+k_2 A^2 \cos(\omega_1 + \omega_2)t + \frac{1}{2}k_2 A^2 \left(\cos 2\omega_1 t + \cos 2\omega_2 t\right)$$

$$+\frac{3}{4}k_3 A^3 \cos(2\omega_1 - \omega_2)t + \frac{3}{4}k_3 A^3 \cos(2\omega_2 - \omega_1)t + \cdots$$

$$+\frac{1}{4}k_3 A^3 \cos 3\omega_1 t + \frac{1}{4}k_3 A^3 \cos 3\omega_2 t + \cdots\cdots \tag{2.9}$$

$$=\sum_{k=1}^{\infty} A_{ok}\cos\left(w_k t\right) \quad \text{where } w_k = aw_1 + bw_2 \text{ and } a,b \in Z$$

which shows that the output signal would be detected at frequencies of all possible combinations of $\pm w_1$ and $\pm w_2$. Thus, the inband and the out-of-band intermodulation distortion components' evaluation can be extracted through the two-tone test.

Inband distortion components are the mixing products that obey

$$a+b=1 \tag{2.10}$$

the odd-order combinations appear exactly over or very close to the output fundamental frequencies. These products, for instance, would have to be measured at the fundamental frequencies: w_1, w_2; third-order components at: $2w_1-w_2$, $2w_2-w_1$; fifth-order components at: $3w_1-2w_2$, $3w_2-2w_1$; and so on. They constitute a very large number of lower and upper sidebands, separated from the output fundamental signals and from each other by w_1-w_2 and w_2-w_1. Figure 2.2 shows an illustration of the output power spectrum. These inband intermodulation distortion components are the main sources of nonlinear distortions that play an important role in narrowband wireless communication systems.

For most microwave and wireless communication systems, the fundamental output power at linear small-signal levels increases 1dB for each decibel rise of input signal, while a 3dB per decibel rate for the third-order IMD power is observed. This led the definition of an important figure of merit for characterizing the intermodulation distortion in nonlinear devices as the third-order intercept point (IP3). IP3 is a imaginary point that is defined as the intersect of the 1-dB/dB slope line of the output fundamental power with the 3-dB/dB slope line of the

third-order IMD power as shown in Figure 2.3. The lower level of the third-order IMD is, the higher the IP3 is. Later in section 2-3-3, the analysis and estimation of the IM3 and IP3 will be discussed in detail.

In the other hand, out-of-band distortion frequencies will be those satisfying

$$a+b \neq 1 \qquad (2.11)$$

As their name indicates, out-of-band distortion components are the mixing terms locating quite far from the fundamental frequencies signals. Therefore, their importance is not evident on modern narrowband wireless communication systems since they can be filtered out easily.

2-3 Analysis and Estimation of IM3 &IP3

A simple device circuit model as shown in Fig. 2.4 was used for the IP3 estimation of the PHEMT used in this study. The non-linear circuit elements include the Schottky-barrier junction capacitance at the gate (Cgs), the gate to drain capacitance (Cgd), the intrinsic transconductance (gm) and the drain conductance (Rds). Among them, Cgs and gm are dependent on the input voltage (Vi), and Rds is dependent on the output voltage (Vo) [4].

There are several steps for the IM3 & IP3 estimation. First, the relation equation between the output voltage and the input voltage must be determined. Assume wCgd·Rds can be neglected, the relation equation is shown as equation (2.13), where w is 2πf, f is the operating frequency. j is the imaginary number.

$$\frac{Vi - Vo}{\dfrac{1}{jwCgd}} = gm \cdot Vi + \frac{Vo}{Rds}$$

$$(Vi\text{-}Vo) \cdot jwC_{gd} \cdot Rds = gm \cdot Vi \cdot Rds + Vo \qquad (2.12)$$

$$Vo \cdot \left(1 + jwC_{gd}Rds\right) = \left(jwC_{gd} \cdot Rds - gm \cdot Rds\right) \cdot Vi$$

assume $jwC_{gd}Rds \ll 1$, then we can get :

$$Vo = \left(jwCgs \cdot Rds - gm \cdot Rds\right) \cdot Vi \qquad (2.13)$$

Secondly, the output voltage was expanded as power series form as shown in equation (2.14).

$$V_o = k_1 V_i + k_2 V_i^2 + k3 V_i^3 + \dots. \qquad (2.14)$$

From equation (2.13) & use Taylor's expansion：：

$$Vo' = -gm' \cdot Rds \cdot Vi - gm \cdot Rds$$
$$Vo'' = -gm'' \cdot Rds \cdot Vi - 2gm' \cdot Rds \qquad (2.15)$$
$$Vo''' = -gm''' \cdot Rds \cdot Vi - 3gm'' \cdot Rds$$

and

$$Vo = Vo(Vi = 0) + Vo'(Vi = 0) \cdot Vi + \frac{Vo''(Vi = 0)}{2!} \cdot Vi^2 + \frac{Vo'''(Vi = 0)}{3!} \cdot Vi^3 + \dots$$

then we can get Vo：

$$Vo = -gm \cdot Rds \cdot Vi - gm' \cdot Rds \cdot Vi^2 - \frac{gm'' \cdot Rds}{2} \cdot Vi^3 + \dots \quad (2.16)$$

Comparing equation (2.14) with equation (2.16), it can be obtained that k1 = – gm·Rds, k2 = – gm'·Rds and k3 = – (1/2)gm''·Rds (gm' and gm'' are the first and the second derivatives of the intrinsic transconductance respectively).

Third, assume the input signal consists of two signals with the same amplitude (A) but with two different but closely located frequencies as shown

$$Vi = A\cos\omega_1 t + A\cos\omega_2 t \quad (2.17)$$

Then, substitute equation (2.17) into equation (2.14), yields following expression for the IM3 level at frequencies $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ [5]:

$$Vo = \frac{3}{4} k3A^3 \cos(2w1\text{-}w2)t + \frac{3}{4} k3A^3 \cos(2w2\text{-}w1)t \quad (2.18)$$

then IM3 magnitude which is equal to 3/4 k3A^3 can be determined [5].

Thus, the power levels of IM3 in dBm units can be expressed in terms of the intrinsic transconductance gm as:

$$PIM_3 = 10 \log \left\{ \left(\frac{3}{8\sqrt{2}} \cdot gm'' \cdot Rds \cdot A^3 \right)^2 \cdot \frac{1000}{RL} \right\} \qquad (2.19)$$

where R_L is the load impedance in ohms unit.

Fourth, using IP3 definition with linear part equals to the third-order intermodulation distortion to obtain A as shown in equation (2.20).

$$k1A = \frac{3}{4} k3A^3 \qquad (2.20)$$

Finally, assume the load impedance (R_L) is equal to Rds, the device IP3 can be obtained from equation (2.21)

$$
\begin{aligned}
IP3 &= \frac{Vo^2}{2R_L} \\
&= \frac{(k1A)^2}{2Rds} \\
&= \frac{k1^2 \cdot \dfrac{4k1}{3k3}}{2Rds} \\
&= \frac{4\left(-gm^3 \cdot Rds^3\right)}{6Rds \cdot \left(-\dfrac{gm'' \cdot Rds}{2}\right)} \\
&= \frac{4}{3} \cdot \frac{gm^3 Rds}{gm''}, \quad where \quad gm'' = \frac{d^2 gm}{dVgs^2}
\end{aligned} \qquad (2.21)
$$

As a result, IM3 is proportional to gm'', and IP3 is inversely

proportional to gm″, thus, when gm remains constant on the gm vs Vgs curve, the IM3 level will be lowered and IP3 can be maximized. Because parasitic effect is limited, parasitic impedances of the device are ignored in this paper for linearity analysis. Therefore, the magnitude of the extrinsic transconductance (Gm) will change in the same direction as the magnitude of the intrinsic transconductance (gm) with applied Vgs. As a result, a flat extrinsic transconductance (Gm) distribution across the gate bias region will cause lower IM3 and higher IP3 for the PHEMT device.

Chapter 3

Experiment

Two device structures, the "lightly-doped channel", and the "uniformly-doped InGaP layer", added to the conventional δ-doped InGaP/InGaAs PHEMT respectively for linearity improvement are designed and adopted in this study. Different from the conventional δ-doped structure, the extra channel doping concentration for the channel doped device was $n = 5 \times 10^{17} cm^{-3}$, and that uniform Schottky layer doping concentration for the uniformly-doped layer was 1.0×10^{18} cm^{-3}. The device structures presented in this study are shown in Figures 3.1~3.3.

3-1 Device structure

The epitaxial wafers used in this study were grown on the GaAs substrate by molecular beam epitaxy (MBE). The MBE is selected because it is a highly refined form of vacuum deposition with precise control of the beam fluxes and deposition conditions. Therefore, better controllability of epitaxy thickness, smoother surface morphology and excellent abruptness of interface can be obtained.

Common to the structures used in this study, the first cap layer is n^+-GaAs layer with highly doping concentration to form good ohmic contact with the multilayered Au-Ge-Ni-Au deposited metal systems. The second layer is the InGaP Schottky layer used to control the device current by modulating the recess depth. The third layer is the Si δ-doped

layer which acts as electron-providing layer. Dual δ-doped layers instead of single δ-doped above and below the quantum well were used to provide uniform electron distribution in the quantum well, which leads to the raise of the electron concentration and improved device linearity and power density. The fourth layer is the InGaP layer followed by the InGaAs channel layer. This InGaP layer is referred to as a spacer layer and serves to separate the electrons flowing in the 2-DEG from the dopant ions in the wide-band-gap material. Without such a layer, electrons in the 2-DEG are scattered as they pass close the innized donors. Hence, increased electron mobility and reduced noise figures can be achieved in presence of the spacer layer. The band diagram of the InGaP/InGaAs HEMT is shown in Figure 3.4. Then the AlGaAs/GaAs "superlattice" layer is used to reduce the leakage current from the substrate. Further, undoped GaAs "buffer" layer is used to enhance the isolation between channel layer and substrate, and then restrict the impurity atoms in the substrate from diffusing to the channel and affecting the electron transport properties.

3-2 Device Fabrication process [11]

There are five major fabrication process steps for the InGaP/InGaAs PHEMTs fabrication including device isolation, ohmic contact metal deposition and annealing, wet chemical recess, gate formation by electron beam (EB) lithography and lift-off process and gold plating of the airbridges for the interconnects. In this study, we use

InGaP/InGaAs/GaAs epitaxial structure to fabricate the low noise PHEMTs with high linearity. The detailed fabrication process of the InGaP PHEMT devices will be introduced in the following section. The fabrication process flow of the InGaP/InGaAs PHEMT device is shown in Figure 3.5.

3-2.1 Wafer cleaning

Cleaning and Cleanliness are crucible to achieving high yields and good reproducibility in the production of semiconductor devices. Undesired impurities can degrade any aspect of the fabrication process: resist pattering, wet and dry etching, metal adhesion and plating, etc. Organic solvents are effective in removing oils, greases, and organic material. Organic solvents are also not harmful to almost materials which would be existed perpetually on GaAs devices such as ohmic contact metals, Schottky barrier gate metal, the airbridge plating gold, dielectrics, and so on. The wafers fabricated in this study were dipped in acetone (ACE) and isopropyl alcohol (IPA) organic solution for five minutes, and blown dry by nitrogen gas before almost each process.

3-2.2 Device isolation

GaAs has a major superiority over Si with respect to its semi-insulating property, so that better electrical isolation can be achieved easily than silicon. Therefore, only the surface layers of the GaAs wafer need to be taken into consideration for electrical isolation. Isolation

means restricting the electrically conductive part of the wafer to specific parts of its surface as "active region", so that electrical current is limited from flowing to other undesired areas, and the separate devices can be also isolated from each other. Almost all devices fabricated on GaAs substrate will require some form of isolation near the first of the process and it serves plenty of purposes. If some portion of the current between source and grain electrodes, for example, were not to flow under the gate metal, the current would represent a parasitic resistance which would degrade the RF performance of the devices. Besides reducing parasitic resistance, the gate bonding pad formed on inactive electrically insulating material can also greatly minimize the parasitic capacitance associated with the pad.

"Mesa isolation" is the simplest means to achieve isolation and was used in this study. The active region of the devices was defined with an etch mask in the suitable pattern by photolithography, then the portions of the electrically active surface in the unmasked areas were etched away by wet chemical etching, and "mesas" of the active layer were left in the desired locations. For the InGaP/InGaAs PHEMTs fabricated in this study, the mesa wet etch was achieved by using $HF/H_2O_2/H_2O$ (2:3:10) solution to etch the GaAs cap layer, then HCl/H_2O (1:1) solution to etch the Schottky InGaP layer, and finally the $HF/H_2O_2/H_2O$ (2:3:10) solution was used again to etch other layers down to the epitaxial buffer layer or semi-insulating GaAs substrate for a effective isolation. The etching depth in this study was about 6300Å measured by α-stepper.

3-2.3 Ohmic contact formation

Ohmic contacts are needed in all semiconductor devices in order to allow a link through which current can flow and bias can be applied, and to reduce (parasitic) resistance as little as possible. The lower resistance also benefits the devices' power consumption and noise figure performance. Ohmicity implies that the current is proportional to voltage, both in sign and magnitude. This can only occur over a limited current or bias range for the reason of limitations on linearity. Contacts based on tunneling exhibit linearity over a larger range than thermionic emission and thermionic field emission do. Hence, the major strategy employed to achieve best quality ohmic contact, is to heavily dope the cap layer between the metallization and the lower doped semiconductor to certify that the dominant current transport mechanism is field emission (tunneling).

Of all the metalizations, the Au-Ge-Ni multilayered, alloyed thin film system exhibits the lowest contact resistance and the highest reliability. During alloying, the Ge is used for doping the GaAs heavily to produce a linear current-voltage characteristics as a result of tunneling at the contact interface. The Au provides a low eutectic temperature and is compatible with microelectronic processing. The Ni assists the wetting of the molten Au-Ge films and improves the surface uniformity of the contact.

In this fabrication process, the ohmic contact windows were defined by photolithography with image reversal resist AZ 5214E. The advantage of the reversal process is that an undercut edge profile suitable for lift-off processing can be achieved automatically. Further, to maintain the surface

as clean as possible, O_2 plasma descum was applied to remove the residual photo-resist, and HCl/H2O (1:10) solution was dipped for 30 seconds to etch surface oxide away before depositing the ohmic metal. Finally, Au/Ge/Ni/Au metal with total thickness of 4100Å was deposited by e-gun evaporation system. The wafer, immediately after lift-off procedure, was thermally alloyed at 355℃ for 30 seconds by using rapid thermal anneal system (RTA). The contact resistance was measured via the transmission line method (TLM). The typical contact resistance measured was approximately $6X10^{-6}$ Ω-cm^2 in this study.

3-2.4 Recess and gate formation

The series resistance at the metal-semiconductor interface of the Schottky barrier gate has a high-resistance region devoid of mobile carriers. This is the depletion region, and the resulting junction exhibits rectifying properties. The size and placement of the gate is dominant to HEMT performance, especially for high frequency operation. Almost power and low noise HEMTs use a recessed gate geometry in which the gate stripe is placed in an etched slot to locate it slightly below the surface of the GaAs cap layer. The gate recess has several advantages. The recessed gate geometry places the bottom of the gate below the surface depletion region so that there is no restriction to current flow under forward gate bias. The extra channel thickness on either side of the

gate slot leads to decreased source-to-gate and gate-to-drain parasitic resistances. Besides, double recess was also used for superior device linearity [6].

Short gate lengths are specifically important for high frequency performance. As gate length is shortened, the cross-sectional area of the gate is also reduced which makes the gate resistance raise obviously. This problem can be counterbalanced by constructing gates having a large cross-sectional area at the top of the gate, yet retaining a short gate length in contact with the wafer. This gate is called "T-gate" because of the shape of the cross-sectional area. The "T-gate" technique was applied in this study.

In this InGaP/InGaAs PHEMTs fabrication process, the 1st recess slot was defined by e-beam photolithography to form the photo-resist layer with 1μm length. Then, the gate recess was performed using a highly selective citric acid/H_2O_2/H_2O solution to selectively remove the cap GaAs material, and HCl/H_2O solution was used for the etching of the InGaP Schottky layer. The drain-to-source current was measured during the whole etching process until the target current was reached.

After removing the 1st recess photo-resist, the gate openings were defined by using the electron-beam resists to form the dual photo-resist layers. Poly methyl methacrylate (PMMA) as the bottom layer, copolymer P(MMA-MAA) as the top layer were used to achieve the fabrication of the T-shaped gate as a result of the higher sensitivity of copolymer than that of PMMA. Then the wafers were dipped in the HCl/H_2O (1:4) solution for 15 seconds to double recess and remove the native oxide from the surface before the gate deposition.

Ti/Pt/Au=1000/1000/3000Å gate metal was deposited by e-gun evaporation system. Titanium provides the adhesion, platinum serves as a barrier to prevent gold diffusing into GaAs, and gold supplies high enough electrical conductivity. Finally the wafers were soaked into acetone (ACE) solvent to lift-off the undesired metals. The gate length of the InGaP/InGaAs PHEMTs in this study was 0.25μm.

3-2.5 Device passivation

Dielectric films are used in GaAs processing for protective encapsulation, capacitor dielectrics, and crossover insulators. For HEMT devices, the gate area is particularly sensitive to surface effects. Any particles, chemicals, and even gases emerged in other processes will degrade device performance. Consequently, the first purpose of dielectric formation is merely to protect critical parts of the wafer from environmental contamination and mechanical damage. Plasma enhanced CVD (PECVD) silicon nitride dielectric has been widely used to passivate GaAs based devices on account of its stable electrical and thermal characteristics, and minimal drift in the device RF performance. Further, silicon nitride is also less permeable to ions than silicon dioxide, therefore makes the superior encapsulant.

The dielectric film, on the other hand, is also usually used to fabricate MIM (metal-insulator-metal) capacitors. The higher dielectric constant of the silicon nitride makes it applicable for use in capacitor formation. However, improper passivation can result in conflicting degradation on

device performance. If the nitride film is too thin, the mechanical strength will be less; if the nitride film is too thick, the undesirable feedback capacitance between gate and drain will increase. Therefore, the optimized dielectric film thickness is usually between 1000 and 4000Å based on these considerations.

In this study, the silicon nitride dielectric film was deposited by PECVD after gate formation and lift-off process. The silicon nitride film was grown at the conditions under 250℃ temperature, 35W RF power, and SiH_4/Ar, NH_3, N_2 as precursors .The film thickness was about 1000Å.

3-2.6 Nitride via etching

After the passivation process, the contact vias through the interlevel dielectric was defined by photolithography for the subsequent airbridge interconnections. After the photo-reist was patterned, the uncovered silicon nitride films were etched away by reactive ion etching (RIE) system to expose the metal below. The reactive plasmas were CF_4 and O_2, the RF power was 98W, and the pressure was 30 mtorr. The resist then remained on the wafer for the following application of the thin metal layer. The thickness of the photo-resist also determines the spacing between the bridge and the dielectric films beneath.

3-2.7 Air-bridge plating

The most general application of platting is used in interconnections with bridges. Plating on GaAs devices is almost always gold. In addition to its high electrical conductivity, gold is also resistant to attack by most acids, to oxidation, to electromigration at high current density, and is free from intermetallic compounds formation, make it the superior choice for the interconnect metal system. However, gold is hardly to adhere on GaAs and the dielectrics, thin titanium has to be deposited to provide the adhesion for Au.

Airbridge crossovers are less capacitive because air has a much lower dielectric constant than other dielectrics, and the space under the airbridge tends to be larger than the thickness of typical dielectrics. Hence, lower capacitance can be achieved, which result in higher device speed. Low parasitic capacitances, freedom from edge profile problems, and the capability to carry large current have been advocated as excellences of an airbridge interconnect. Air-bridges, therefore, are commonly used to interconnect source pads of HEMTs, or to cross over a low level of metalization.

The air-bridge process flow is described in detail as following: first, a layer of photo-resist was patterned to open contact windows over metal pads. Then, a thin coating of Ti/Au/Ti=300/500/300Å was evaporated to the entire wafer. This trilevel metal is usually chosen to be very thin, enough to give good stability and provide conduction for the necessary plating current to all parts of the wafer. Next, another coat of photo-resist was applied and patterned, such that only the pads to be interconnected

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would be exposed during the plating operation. The electroplated gold thickness was 2μm. The major steps of air-bridge formation are shown in Figure 3.6.

After the plating was completed, both top and lower resist layers were removed by soaking in acetone solvents, the thin Ti and Au metal were in turn etched by $HF/H_2O(1:100)$ and KI/I_2 solution individually, leaving only the plated thick gold layer to form bridges of interconnect between support posts, with only air beneath the metal bridges. UP to now, the front-side process of the InGaP/InGaAs PHEMTs was completed, and the DC and RF characteristics of the devices could be measured. The accomplished PHEMT device is shown in Figure 3.7.

Chapter 4

Characterization

Electrical performance (DC & RF) are characterized for each fabricated device. The DC characteristics such as ohmic contact resistance, I_{ds}-V_{gs} polynomial curve fitting, and extrinsic transconductance will be discussed in this chapter. However, the dc measurements alone are not sufficient to characterize microwave devices completely. Therefore, the small-signal S-parameters, noise figure measurements, load-pull measurements and measurements of output harmonic content as a function of input power are also introduced to measure the related radio-frequency dependent characteristics.
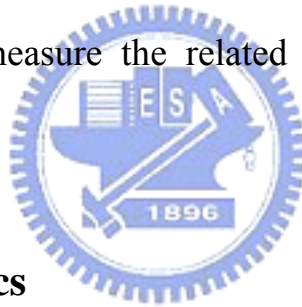
4-1 DC Characteristics

4-1.1 ohmic contact resistance

The transmission line model (TLM) is commonly used to measure the contact resistance and identify the contact property. A test pattern consists of linear array of pads spaced at unequal distances as shown in Fig 4.1. The distances between TLM electrodes were 3 μ m, 5 μ m, 10 μ m, 20 μ m, and 36 μ m respectively in this study. The contacts have a width, W, and the patterns are isolated from each other such that the current flow is limited within in the distance L in between the patterns. The resistance

consists of the two contact resistances plus the resistance of the semiconductor layer between two adjacent electrodes that can be expressed by,

$$R = 2R_c + \frac{R_s L}{W}$$
(4.1)

R: measured resistance

R_c: contact resistance

R_s: sheet resistance of the channel region

W: electrodes width

L: space between electrodes

Assuming sheet resistance R_s is constant, as shown in Figure 4.2, a plot of measured resistance R as a function of spacing, L, will yields a straight line. The slope of the line gives the value, $\frac{R_s}{W}$, and the intersect with R-axis gives the value $2R_c$.

Another important parameter related to the contact property is the specific contact resistivity ρ_c, which is defined by

$$\rho_c = \frac{W^2 R_c^2}{R_s}$$
(4.2)

This specific contact resistance is an important figure of merit for contact resistance. It involves the total resistance of the metal-semiconductor interface and the epitaxial layer under the contact, current crowding effects, spreading resistance, and any interfacial oxide that may present between the metal and the semiconductor.

4-1.2 I_{ds}-V_{gs} polynomial curve fitting

To further investigate the linearity performance of the two devices, polynomial curve fitting technique was applied on the transfer characteristic functions of these devices. The I_{ds}-V_{gs} curves were expressed in terms of a fifth order polynomial as [7,8]:

$$I_{ds} = a_0 + a_1 V_{gs} + a_2 V_{gs}^2 + a_3 V_{gs}^3 + a_4 V_{gs}^4 + a_5 V_{gs}^5 \qquad (4.3)$$

Moreover, substitute the two-tone input signal $V_{gs} = A(\cos w_1 t + \cos w_2 t)$ into equation (4.3), the IM3 levels incurred by the device can then be readily derived as [7,8]:

$$IM3 = \frac{3}{8} a_3 A^3 + \frac{50}{32} a_5 A^5 \qquad (4.4)$$

For a device with high IP3 and good linearity, the IM3 levels should be reduced as possible, therefore, the higher order constants of a_3 and a_5 should be minimized.

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4-1.3 extrinsic transconductance (G_m)

The device transconductance is defined as the slope of the Ids-Vgs characteristics with the drain-source voltage held constant. The transconductance of the HEMTs indicates the capability of the gate voltage controllability on the drain current, and can be expressed as

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{Vds = cons\tan t} = \frac{\varepsilon}{w} Z_G v_{sat} \qquad (4.5)$$

where ε is the dielectric constant, w is the depletion region depth under the Schottky gate, Z_G is total gate width, and v_{sat} is the electron velocity of the "two dimensional electron gas" (2-DEG).

As all other characteristics are equal, a device with high transconductance will provide greater gains and superior high-frequency performance. The transconductance of the device is one of the most important indicators of device performance for microwave and millimeter wave applications.

4-2 RF Characteristics

4-2.1 Scattering parameters

The most common RF measurements utilized for the characterization of HEMTs for parameter extraction are microwave S-parameter measurements. In this case, the two-port is connected to transmission lines that extend to an impedance termination on the output side and a signal source on the input side. The relation of the microwave signals and s-parameters can be described as,

s-parameters: $\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} * \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$ $\qquad (4.6)$

The a_i and b_i represent normalized complex voltage waves incident and reflected at the *i*th port shown in Figure 4.3.

Then, by the definition,

$$s11 = \left.\frac{b1}{a1}\right|_{a2\,=\,0} \qquad\qquad s21 = \left.\frac{b2}{a1}\right|_{a2\,=\,0}$$

$$s12 = \left.\frac{b1}{a2}\right|_{a1\,=\,0} \qquad\qquad s22 = \left.\frac{b2}{a2}\right|_{a1\,=\,0} \qquad\qquad (4.7)$$

S_{11} = input reflection coefficient with the output matched.

S_{22} = output reflection coefficient with the input matched.

S_{21} = forward transmission coefficient with the output matched.

S_{12} = reverse transmission coefficient with the input matched.
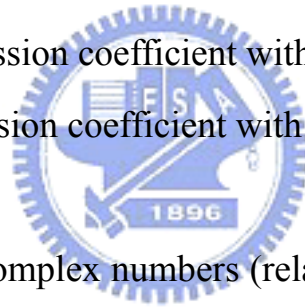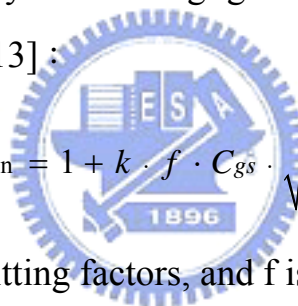
Note that the S_{ij} are complex numbers (relating quantities having both magnitude and phase) and functions of frequency.

4-2.2 Noise figure

Noise in electric systems is the internal generation of signals that cause degradation from the desired response. The drain circuit noise is caused by two phenomena: thermal fluctuations, and carriers traveling at saturated velocity, which is interpreted as diffusion noise. Further, the

gate circuit noise is caused by fluctuations in the active channel. These fluctuations are capacitively coupled to the gate electrode and cause the channel current to be modulated, which then appears as noise at the output of the device.

The physical noise model proposed by Pucel *et al*. derived from general principles in terms of fundamental physical parameters shows good agreement with measured and predicted results. The model is simplified with appropriate current and voltage sources added to model noise effects (Figure 4.4). The parasitic drain resistance R_d, C_{gd}, C_{ds}, and parasitic reactance on the source, drain, and gate terminals are neglected in this model because they have a negligible effect on noise. The noise figure is derived as [12] [13] :

$$F_{min} = 1 + k \cdot f \cdot C_{gs} \cdot \sqrt{\frac{R_g + R_s}{g_m}}$$
(4.8)

where k is empirical fitting factors, and f is the operating frequency.

4-2.3 Third-order intercept point (IP3)

An alternative direct measurement of nonlinear device behavior is a two-tone harmonic content measurement. To make the measurement, two signal sources with the same amplitude but with two different but closely located frequencies f_1 and f_2 are set to a specific input power level. The signals are power combined and applied to the device under test. Results

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are typically displayed as x-y plots of output power for each frequency component of the output signal (harmonic) as a function of input signal power. The third-order intercept point (IP3) is a fictitious point that is obtained when the extrapolated 1-dB/dB slope line of the output fundamental power intersects the extrapolated 3-dB/dB slope line of the third-order IMD power. The lower level the IM3 is, the higher the IP3 is, and thus the greater the linearity is.

Chapter 5

Results and Discussion

In this chapter, the electrical performances of the fabricated InGaP/InGaAs PHEMT devices are described and summarized. The DC characteristics include I-V curve, and extrinsic transconductance G_m. The RF characteristics consist of equivalent circuit parameters extracted from the measured S-parameters, noise figure, and the third-order intercept point (IP3).

The gate length of the measured InGaP/InGaAs PHEMT devices was 0.25 μm, and the gate width was 160 μm.
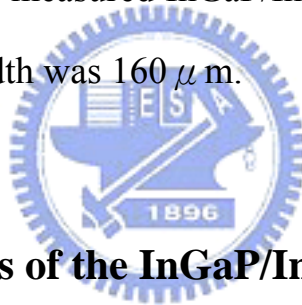
5-1 DC characteristics of the InGaP/InGaAs PHEMTs

5-1.1 Current-voltage curves (I-V curves)

Figure 5.1~5.3 show the Ids-Vds curves of the InGaP/InGaAs PHEMT devices at different gate bias voltage. The I_{dss} measured of the conventional δ-doped, lightly-doped channel, and uniformly-doped layer devices were 376.30 mA/mm, 368.03 mA/mm, and 497.99mA/mm respectively.

Figure 5.4 shows the Ids-Vgs curve of InGaP/InGaAs PHEMT devices at V_{ds} 1.5V. The curves of the lightly-doped channel and uniformly-doped

layer devices show less current suppression into forward bias region which indicates better device linearity.

As described in chapter 4-1.2, the smaller third order coefficient a_3 of the lightly-doped channel, and uniformly-doped layer devices were (-0.00354) and (-0.00537) compared to that of the conventional δ-doped one (-0.01085), which also implies lower IM3 levels. Although the fifth order coefficient a_5 of these two devices were larger, the input power amplitude A, is a decimal much smaller than unity, hence A^5 is also much smaller than A^3. Therefore, the fifth order coefficient a_5 would have less influence on the IM3 levels than that of the coefficient a_3.

5-1.2 extrinsic transconductance (G_m)

Figure 5.5 shows the g_m as a function of gate bias of the InGaP/InGaAs PHEMT devices at V_{ds} 1.5V.

The maximum g_m measured of the conventional δ-doped, lightly-doped channel, and uniformly-doped layer devices were 384.13 mS/mm, 378.38 mS/mm, and 308.5 mS/mm respectively. As is observed clearly, the lightly-doped channel, and uniformly-doped devices have a much flatter Gm profile across the gate biases compared to the conventional δ-doped one, also indicating better device linearity.

Table 5.1 summarizes the measured DC characteristics of the three devices for comparisons.

5-2 RF characteristics of the InGaP/InGaAs PHEMTs

5-2.1 Extraction of small-signal equivalent circuits

Equivalent circuit parameters (ECPs) were extracted from the measured devices S-parameters using a small-signal equivalent circuit model as shown in Figure 5.6. From the equivalent circuit, the bias-dependent RF element values of parasitic inductances L_s, L_d, L_g, parasitic resistances R_s, R_d, R_g, capacitances C_{gs}, C_{gd}, C_{ds}, drain-source resistance R_{ds}, charging resistance R_i, and intrinsic transconductance g_m can be obtained. The S-parameters measurement was carried out with the devices biased at Vds= 1.5V and Ids = 20% Idss in this study.

Figure 5.7~5.9 show the measured *versus* modeled S-parameters for the InGaP/InGaAs PHEMT devices. Frequency range is 1 to 6 GHz with 0.1 GHz step.

Table 5.2 summarizes the extracted equivalent circuit parameters of the three devices for comparisons.

5-2.2 Noise figure

Figure 5.10 shows the noise figure of the InGaP/InGaAs PHEMT devices biased at V_{ds} 1.5V and Ids = 20% Idss. Frequency range is 1 to 18 GHz with 1 GHz step.

The measured noise figure of the uniformly-doped layer, and the conventional δ-doped device was 0.82 dB, and 0.69 dB, while that of the lightly-doped channel device was 2.26 dB at 6GHz frequency.

The higher noise figure of the lightly-doped channel device is due to the impurity scattering in channel region, and much larger gate-source capacitance C_{gs}(634.6fF) and parasitic gate resistance R_g(2.746Ohm) comparing with those of the conventional δ-doped device (C_{gs}:230.4fF, R_g:1.895Ohm).

5-2.3 Third-order intercept point (IP3)

Figure 5.11~5.13 show the measured OIP3 of the InGaP/InGaAs PHEMT devices. The third-order intermodulation measurement was carried out by injecting two signals at two different frequencies; 6.000GHz and 6.001GHz.

The measured OIP3 of the lightly-doped channel device was 21.02 dBm biased at V_{ds} 1.5V and I_{ds}=16.96 mA. The measured OIP3 of the uniformly-doped layer device was 18.76 dBm biased at V_{ds} 1.5V and I_{ds}=8.74 mA. The devices measured both exhibit higher OIP3 values than that of 17.08 dBm for the conventional δ-doped device biased at V_{ds} 1.5V

and I_{ds}=19.24 mA. Higher $\triangle$(IP3-P1dB) of 14.23 dB and 11.49 dB was observed for the lightly-doped channel and uniformly-doped layer devices compared to that of 10.76 dB for the conventional δ-doped one. In addition, as for the IP3 to DC power consumption ratio (IP3/P_{DC}), both the lightly-doped channel and uniformly-doped layer devices demonstrate much better performance of 4.97 and 5.73 over that of 1.77 for the conventional δ-doped device.

Figure 5.14 shows the measured IM3 levels *versus* power backed off from P_{1dB}. Lower IM3 level incurred by both the lightly-doped channel and uniformly-doped layer devices as compared to the conventional δ-doped one is clearly observed.

Based on the equation (2.21) derived in chapter 2-3.3, the higher OIP3 of the lightly-doped channel and uniformly-doped layer devices are achieved because of the flatter extrinsic transconductance (G_m) distribution across the gate bias region obtained. In addition, the larger drain-source resistance (R_{ds}) of 452.8 Ohm and 342.8 Ohm for the lightly-doped channel, and uniformly-doped layer devices compared to that of 249.4 Ohm for the conventional δ-doped one also attribute to higher OIP3.

Table 5.3 summarizes the measured RF characteristics of the three devices for comparisons.

Chapter 6

Conclusions

The G_m flatness improvement reduces the third-order intermodulation distortion (IM3) of the HEMT device, which in turn results in higher IP3, this relationship was proven through the theoretical analysis and experimental work in this dissertation.

An InGaP/InGaAs PHEMT with light doping in the channel to improve the device linearity was demonstrated. The method of light doping in the channel of the device modifies the electron distribution in the channel region which in turn contributes to a flatter extrinsic transconductance (Gm) profile.

Uniform doping technique in the Schottky layer of the InGaP/InGaAs PHEMT device for linearity improvement was also proposed. This added uniformly doped layer raises the Fermi level of the Schottky layer of the device which enables the device to possess flatter G_m across the G_m versus V_{gs} curve.

The measured performance of these two devices exhibit much higher OIP3 attributed by the flatter extrinsic transconductance profile compared to the conventional δ-doped device. The very high IP3 to P_{DC} ratio of the lightly-doped channel and uniformly-doped layer devices are very useful for the low-voltage high-linearity applications in wireless communications systems.

The devices developed are of great use for modern digital wireless communication systems which impose very stringent linearity

requirement for devices.

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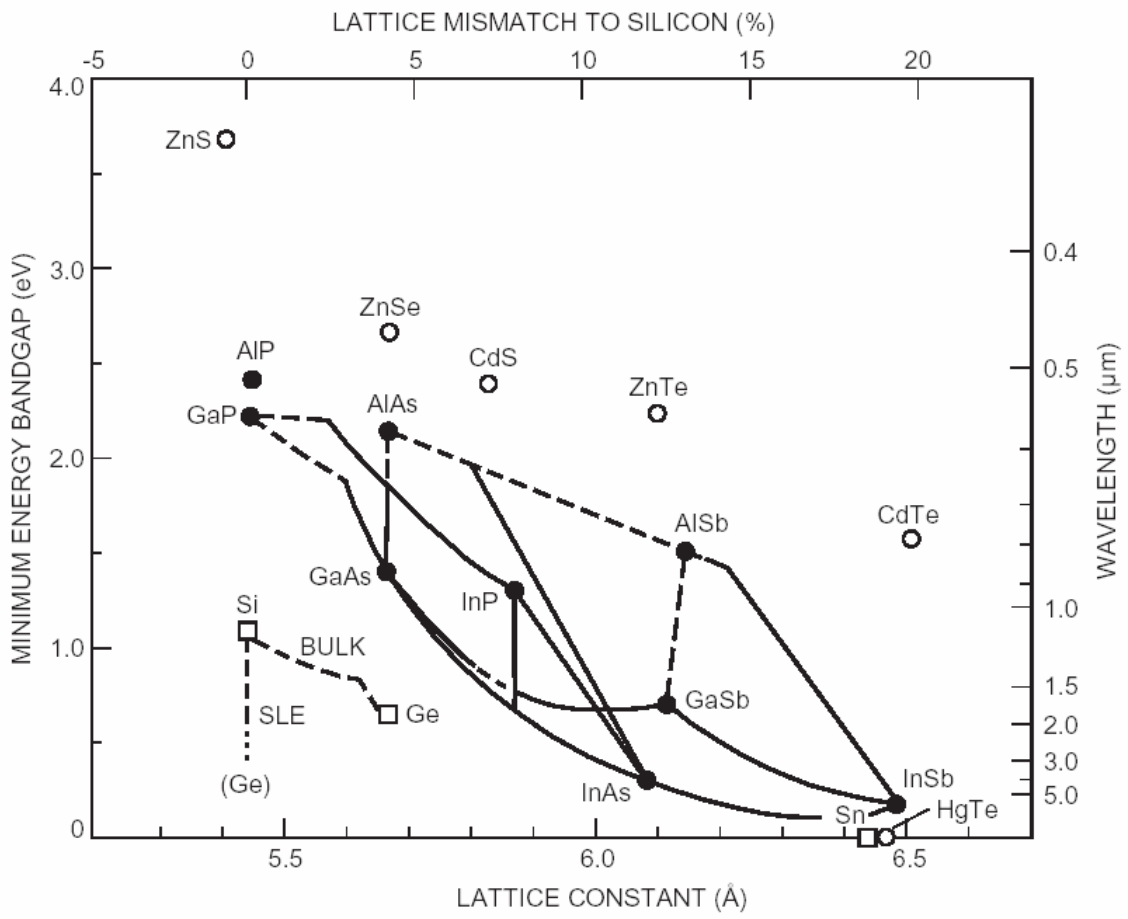
Figure 1.1　Band-gap energy versus lattice constant diagram.
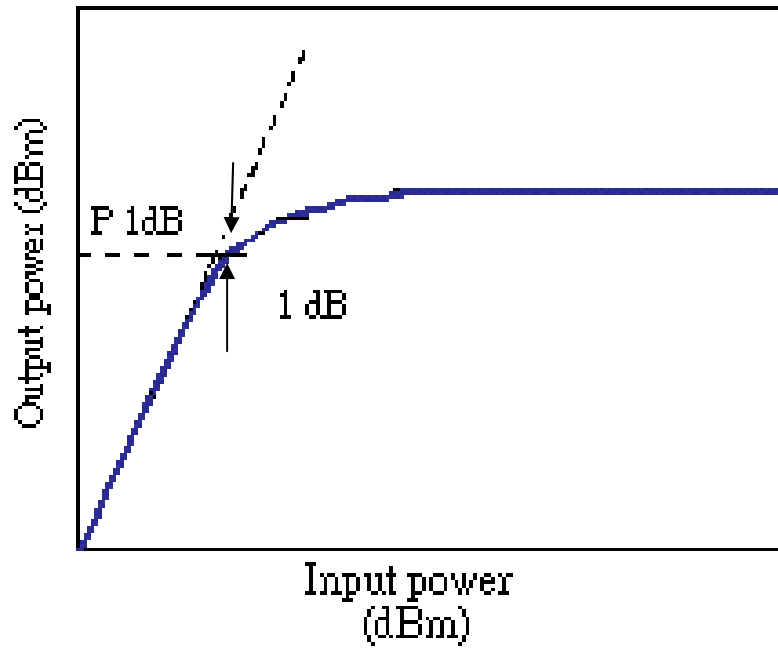
Figure 2.1   Illustration of the 1-dB Compression point.
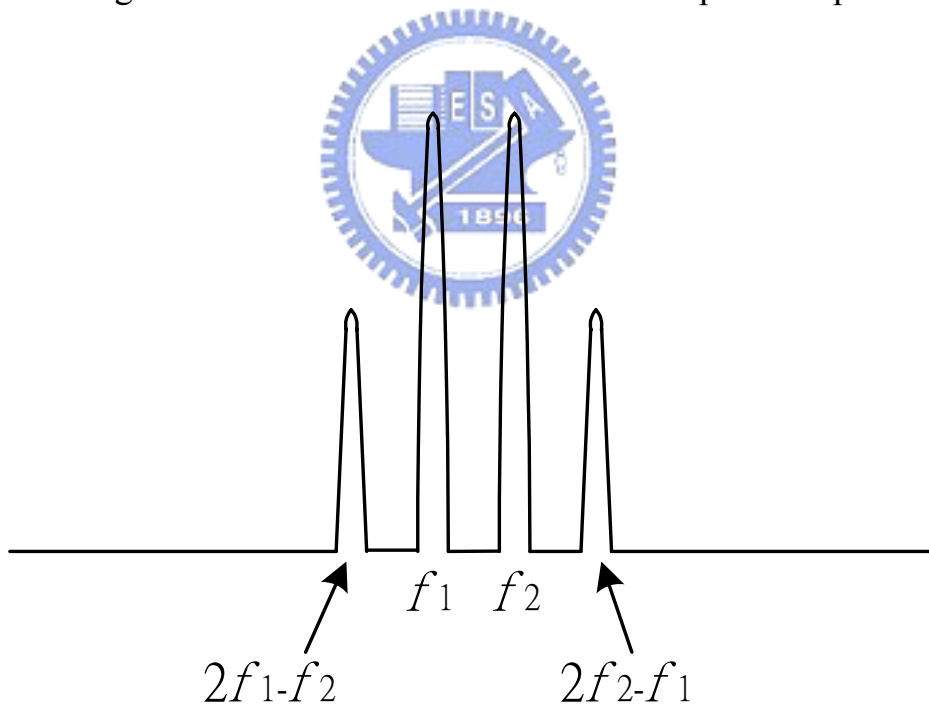
Figure 2.2   Output power spectrum of the two-tone input signal.
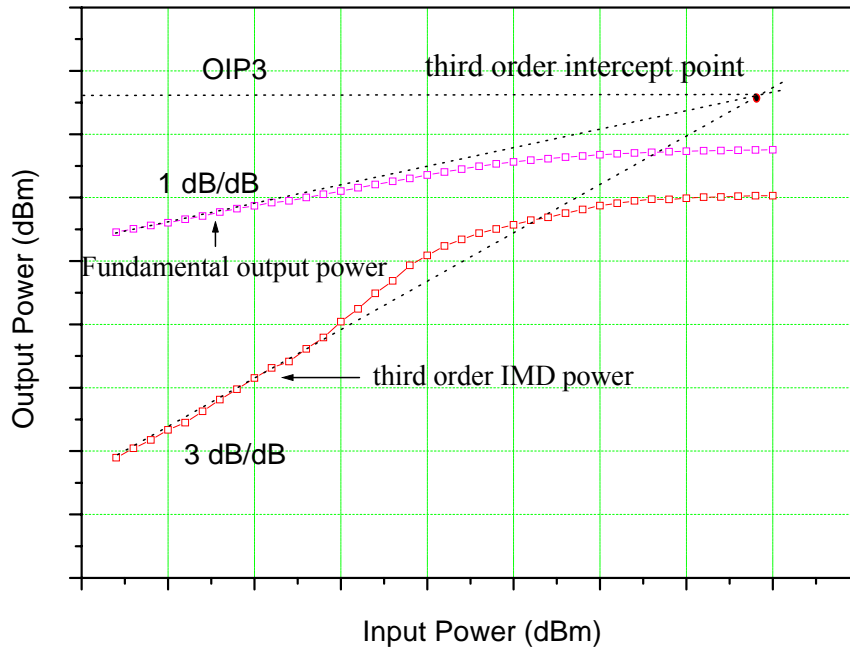
Figure 2.3　Output fundamental power and third-order IMD power

for an equal amplitude two-tone excitation.
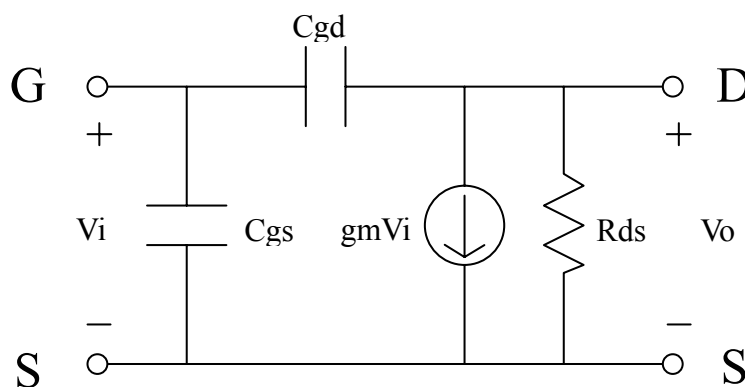
Figure 2.4　A simple device equivalent circuit for linearity analysis.

Au/Ge/Ni/Au   Ti/Pt/Au   Au/Ge/Ni/Au

n+-GaAs

i-In$_{0.49}$Ga$_{0.51}$P

i-InGaP

i-InGaAs   Si δ -doping

i-AlGaAs

i-AlGaAs

i-AlGaAs

AlGaAs/GaAs supperlattice

GaAs buffer

SI GaAs
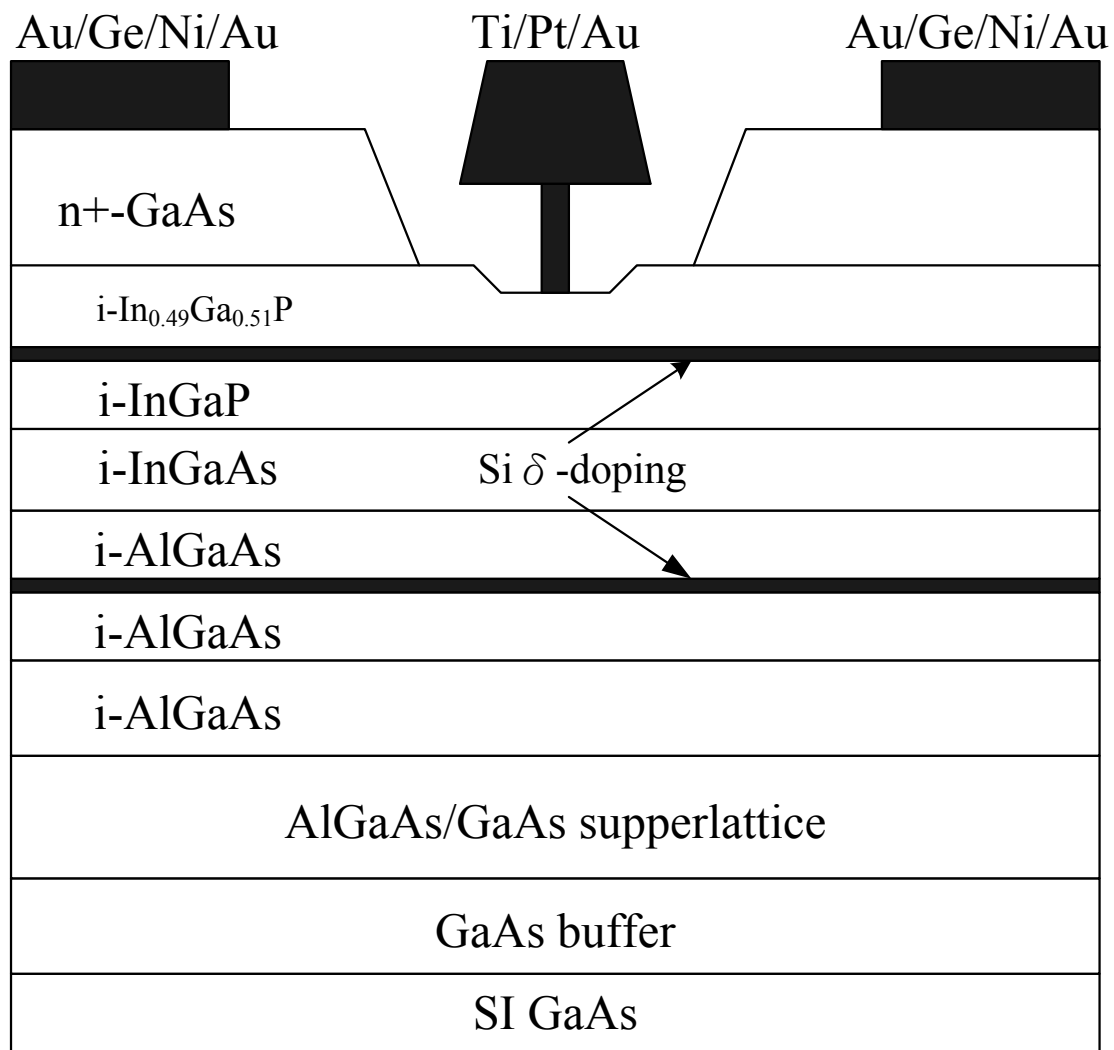
Figure 3.1   Structure of the conventional delta doped InGaP/InGaAs

PHEMT.

Au/Ge/Ni/Au   Ti/Pt/Au   Au/Ge/Ni/Au

n+-GaAs

i-In$_{0.49}$Ga$_{0.51}$P

i-InGaP

InGaAs   Si δ -doping   5 X 10^{17} cm $^{-3}$

i-AlGaAs

i-AlGaAs

i-AlGaAs

AlGaAs/GaAs supperlattice

GaAs buffer

SI GaAs
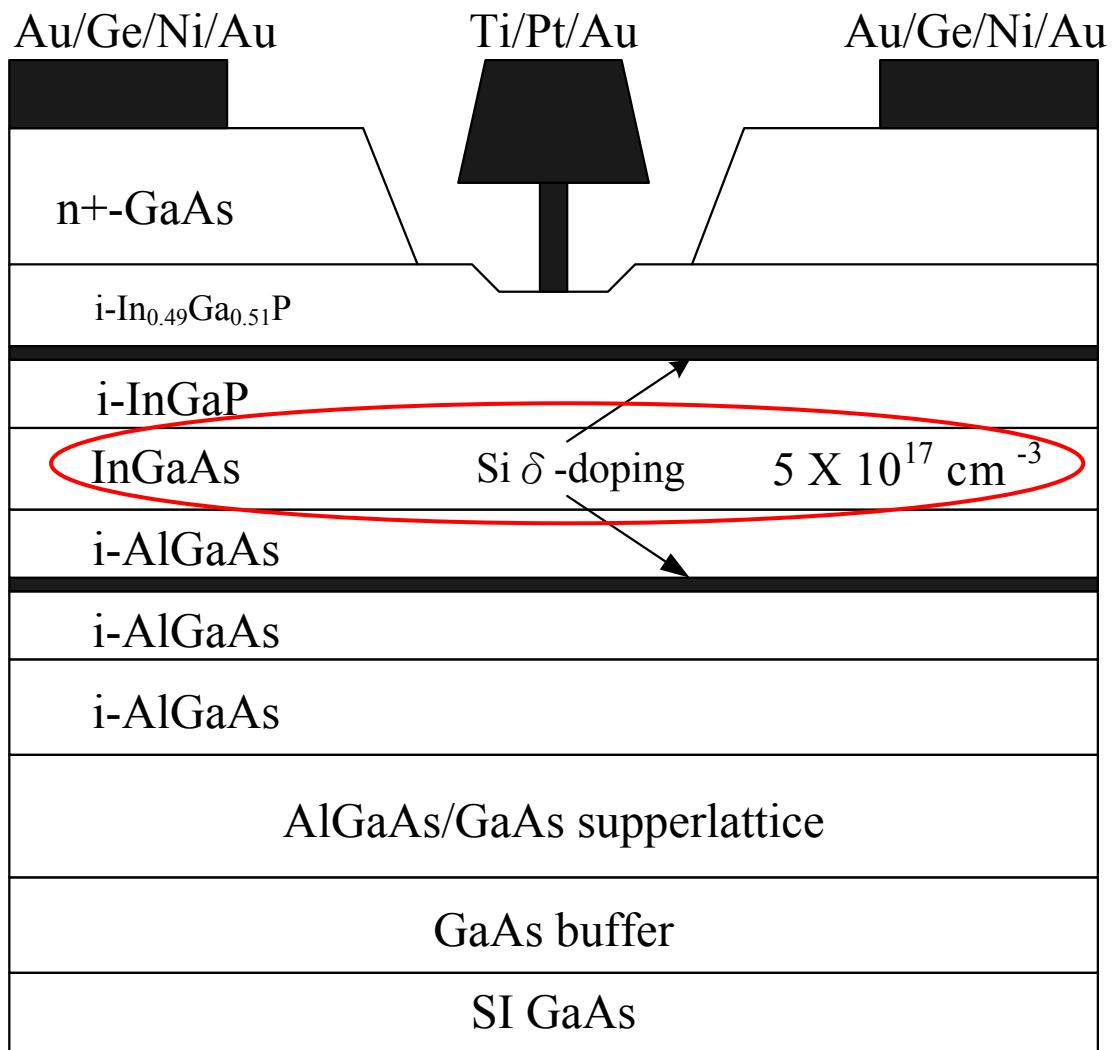
Figure 3.2   Structure of the delta doped InGaP/InGaAs PHEMT with

lightly doped channel.

Au/Ge/Ni/Au	Ti/Pt/Au	Au/Ge/Ni/Au

n+-GaAs

$In_{0.49}Ga_{0.51}P$ 1×10^{18} cm $^{-3}$

i-InGaP

i-InGaAs   Si δ -doping

i-AlGaAs

i-AlGaAs

i-AlGaAs

AlGaAs/GaAs supperlattice

GaAs buffer

SI GaAs
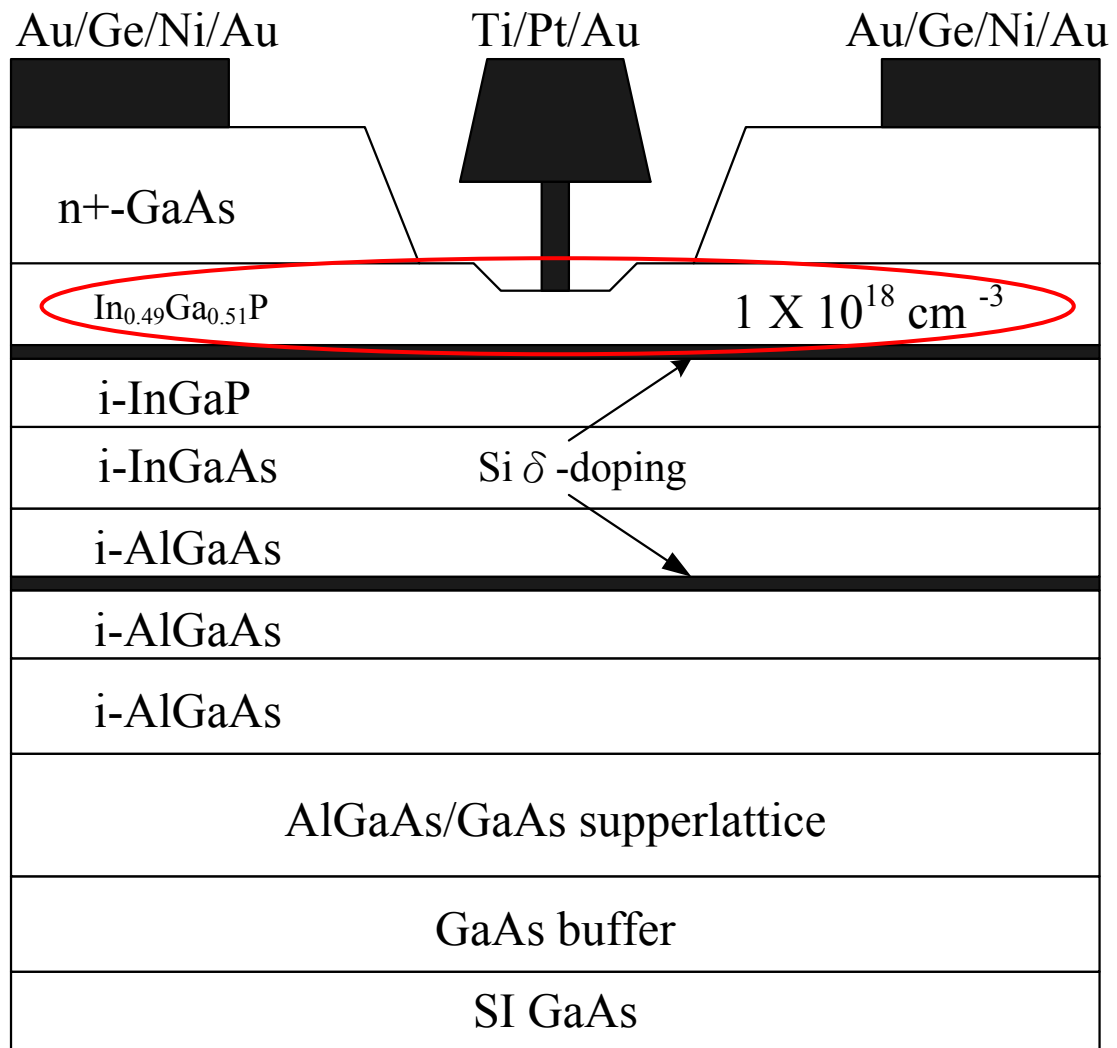
Figure 3.3   Structure of the delta doped InGaP/InGaAs PHEMT with

uniform doping layer.

$e\varphi_b$

$-eV_G$

ΔE_C

2 DEG

Si δ doped →

| Gate Metal | InGaP | InGaP Spacer | InGaAs Channel | AlGaAs Buffer | S.I. Substrate |
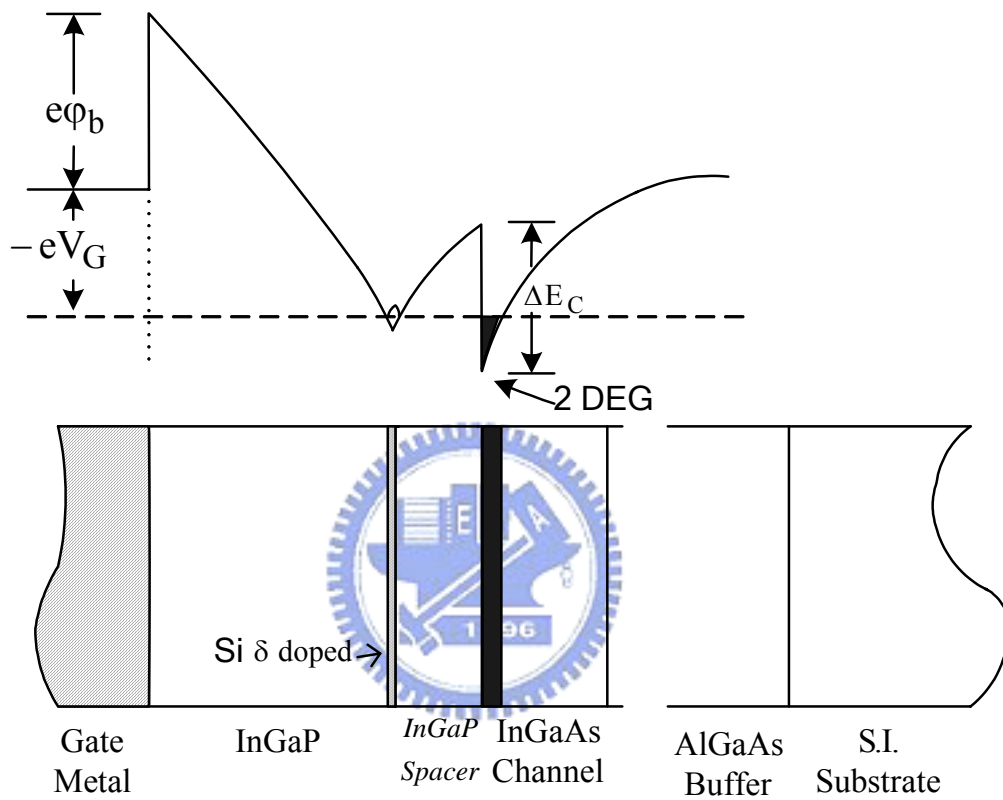
Figure 3.4   The band diagram of the InGaP/InGaAs PHEMT.

(a)
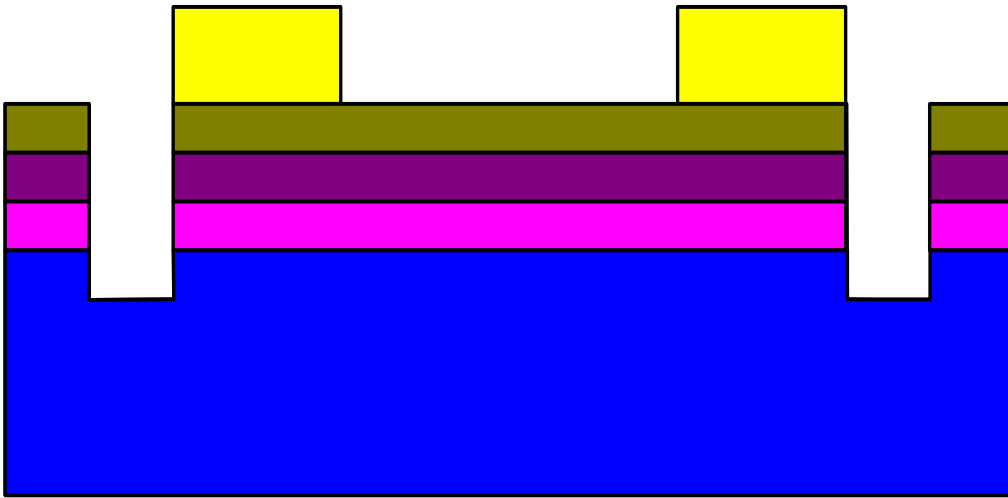
(b)
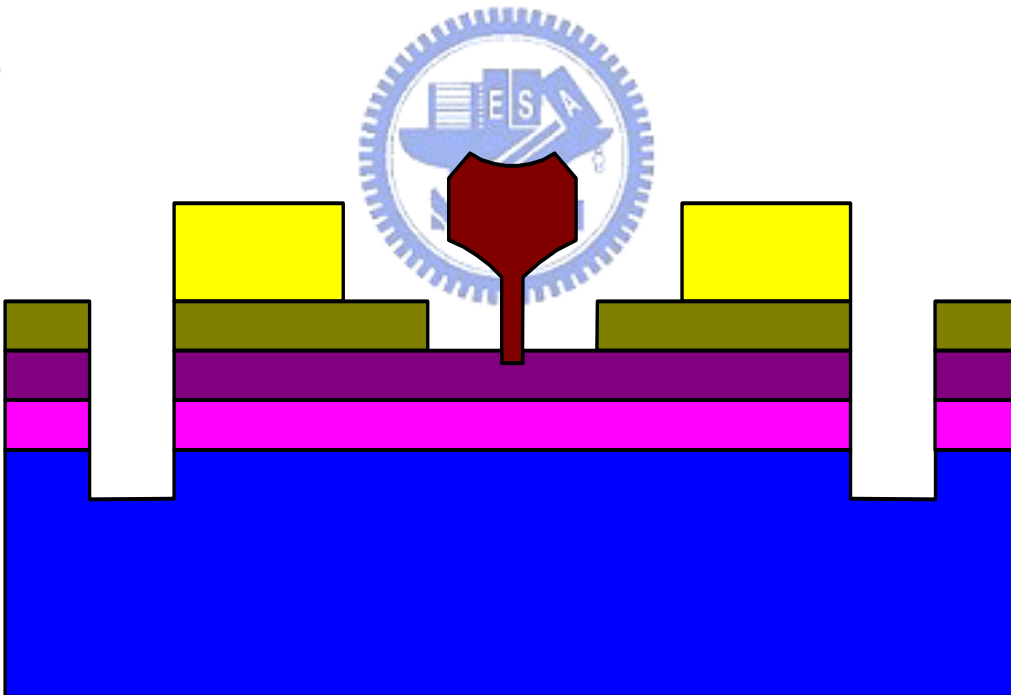
(c)
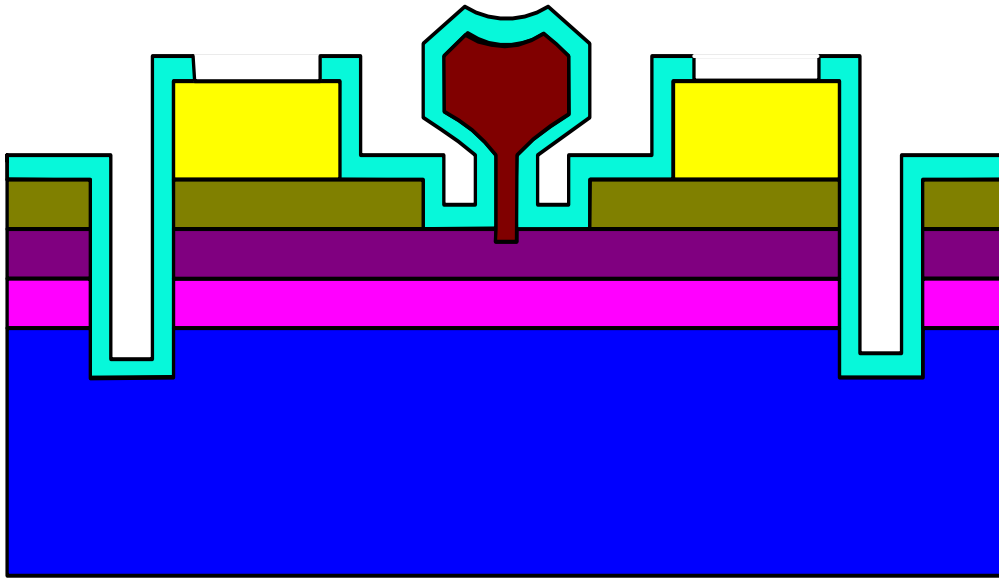
(d)
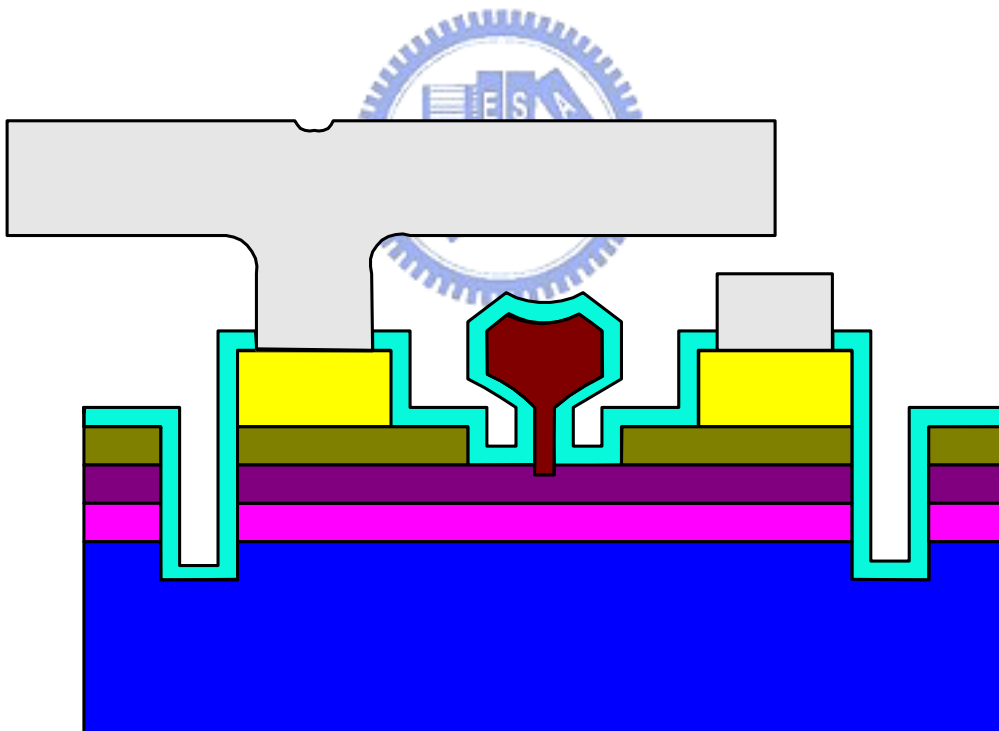
Figure 3.5 Process flow of the InGaP PHEMTs : (a) Mesa isolation and

ohmic contact formation, and (b) gate recess and gate formation.

(c) Device passivation and contact via formation, and (d) air-bridge

plating.

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AB1 RESIST   THIN METAL LAYER

METAL PADS
(a)

AB2 RESIST   THIN METAL LAYER

(b)

PLATED GOLD

(c)

COMPLETED BRIDGE
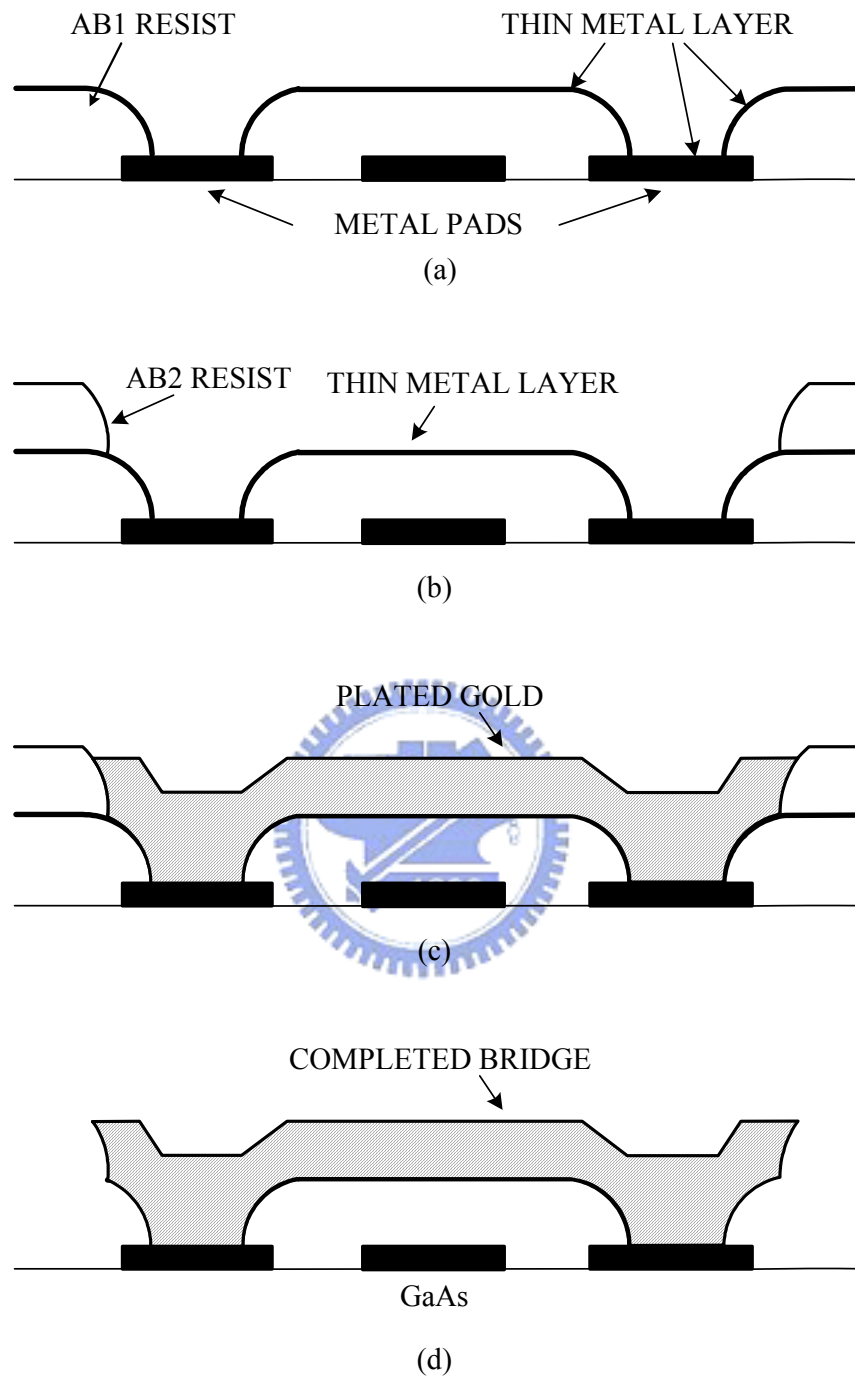
GaAs
(d)

Figure 3.6   The major steps of air-bridge formation.
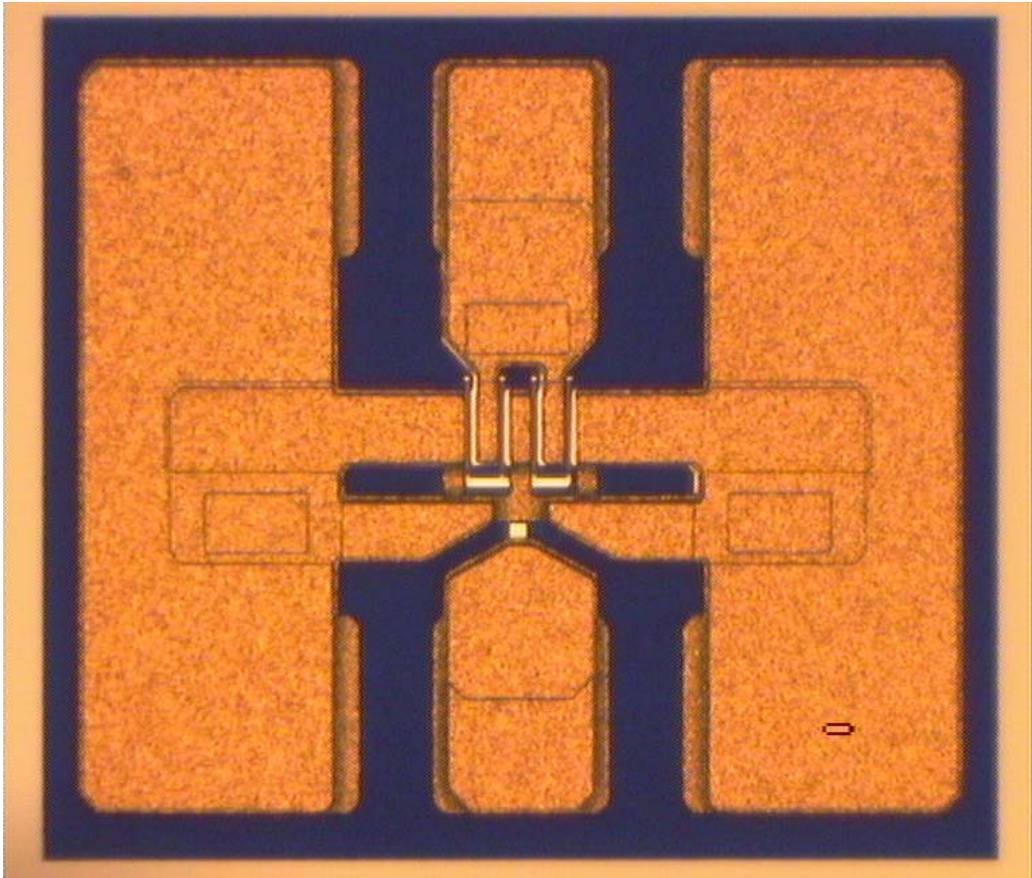
Figure 3.7   The Image of the Finished 0.25x$160\,\mu\,\text{m}^2$ InGaP/InGaAs

PHEMT device

Active Region   Contact Pads
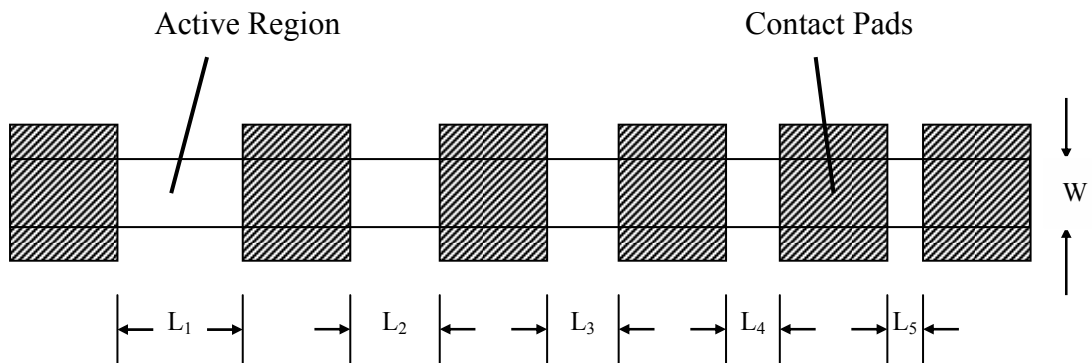
Figure 4.1   The transmission line model (TLM) patterns.

$$\frac{dR}{dL} = \frac{Rs}{W}$$
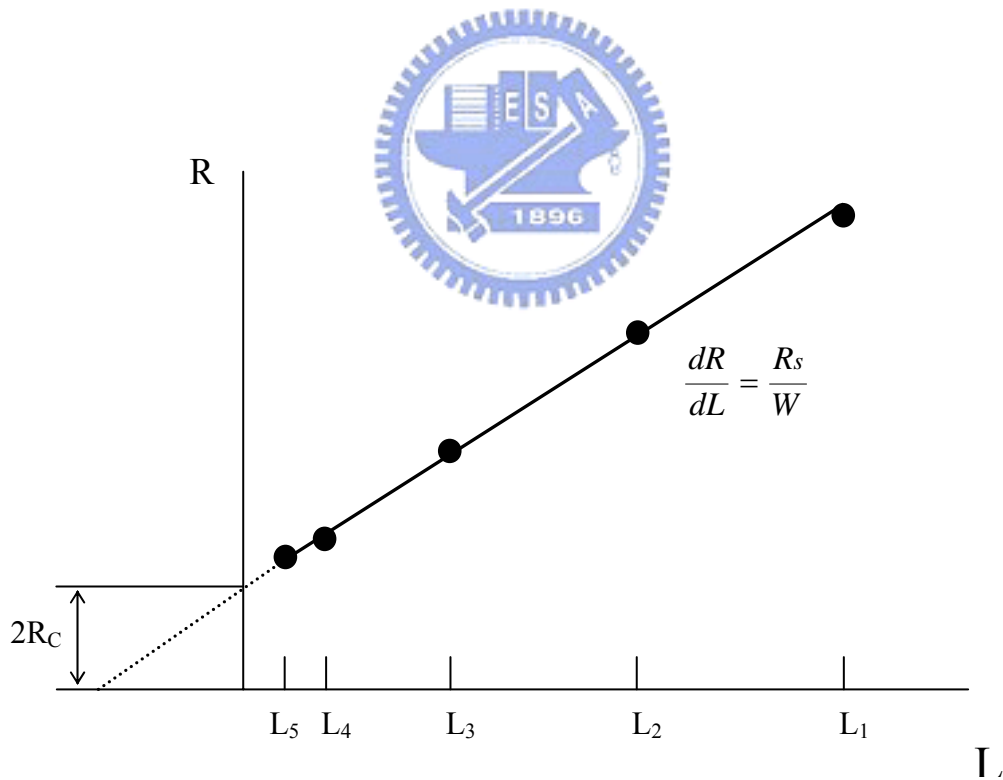
Figure 4.2   Plot of measured resistance as a function of contact

separation yields sheet resistance and contact resistance.
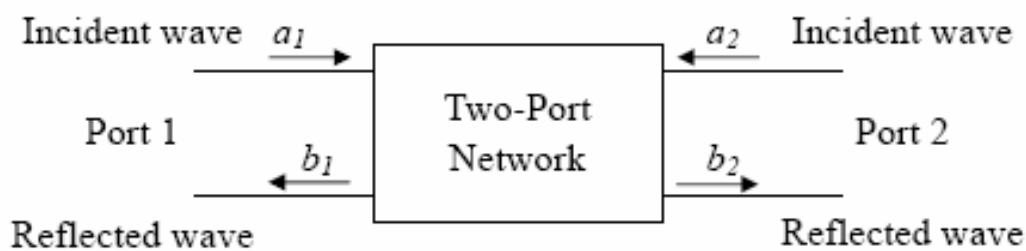
Figure 4.3　The equivalent two-port network schematic and the incident

and reflected signals that occur.
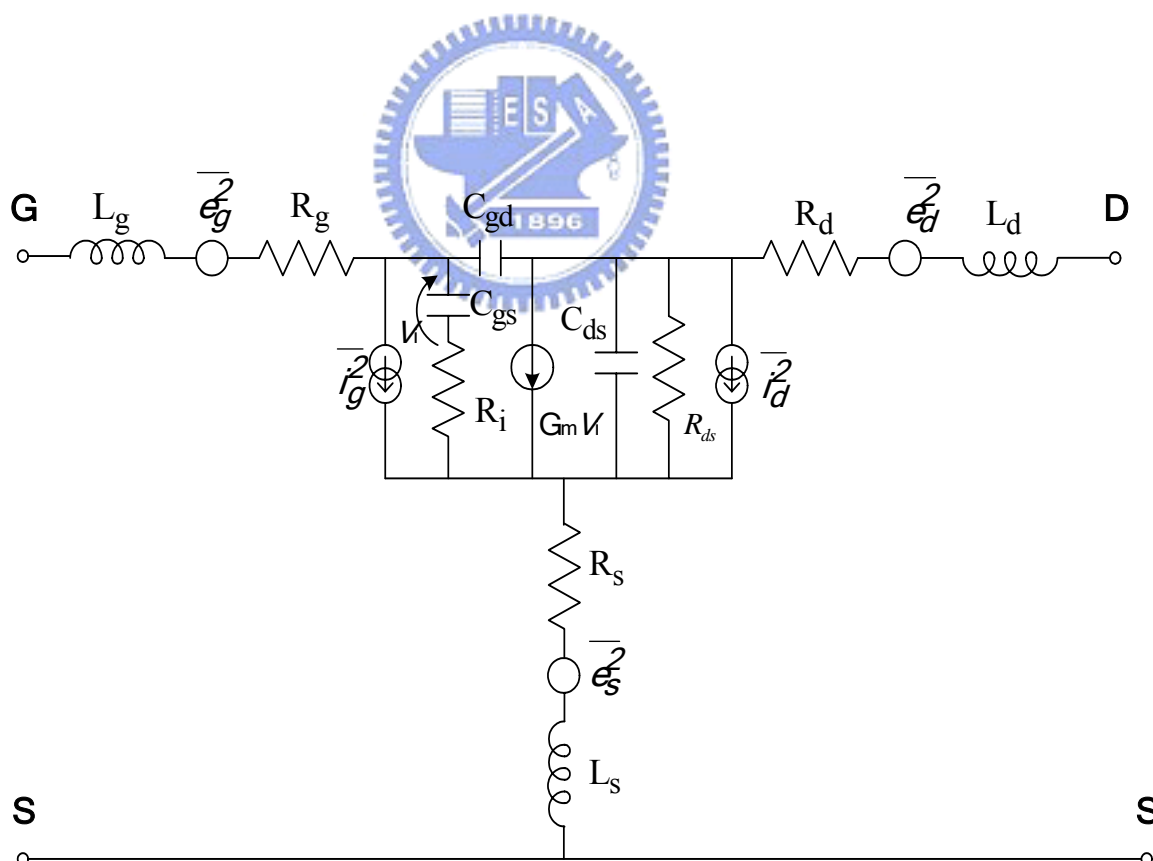
Figure 4.4　PHEMT equivalent circuit with noise sources

represented by voltage and current sources.
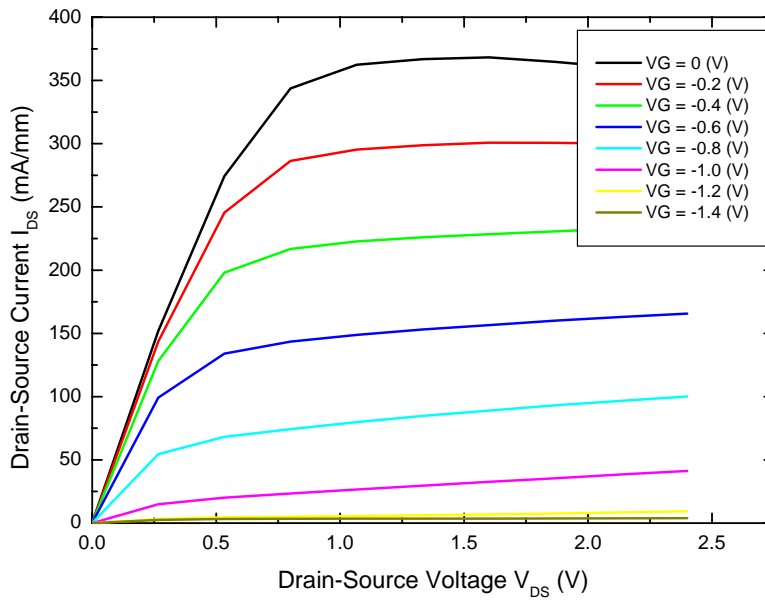
Figure 5.1   Ids-Vds curve of the conventional delta doped
InGaP/InGaAs PHEMT.
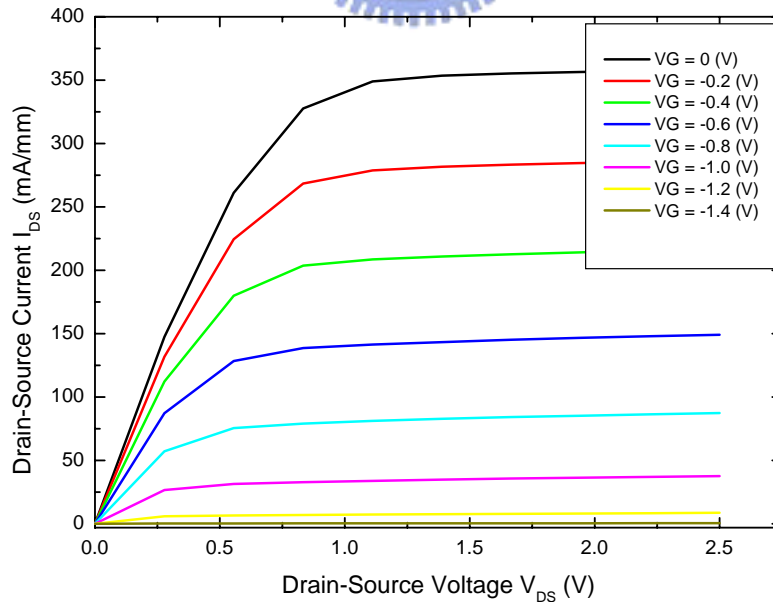
Figure 5.2   Ids-Vds curve of the delta doped InGaP/InGaAs PHEMT
with lightly doped channel.
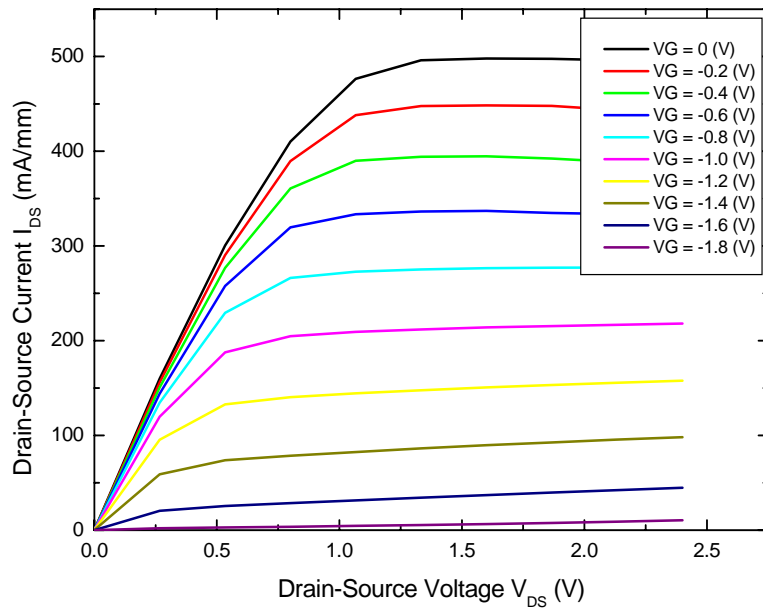
Figure 5.3   Ids-Vds curve of the delta doped InGaP/InGaAs PHEMT
with uniform doping layer.
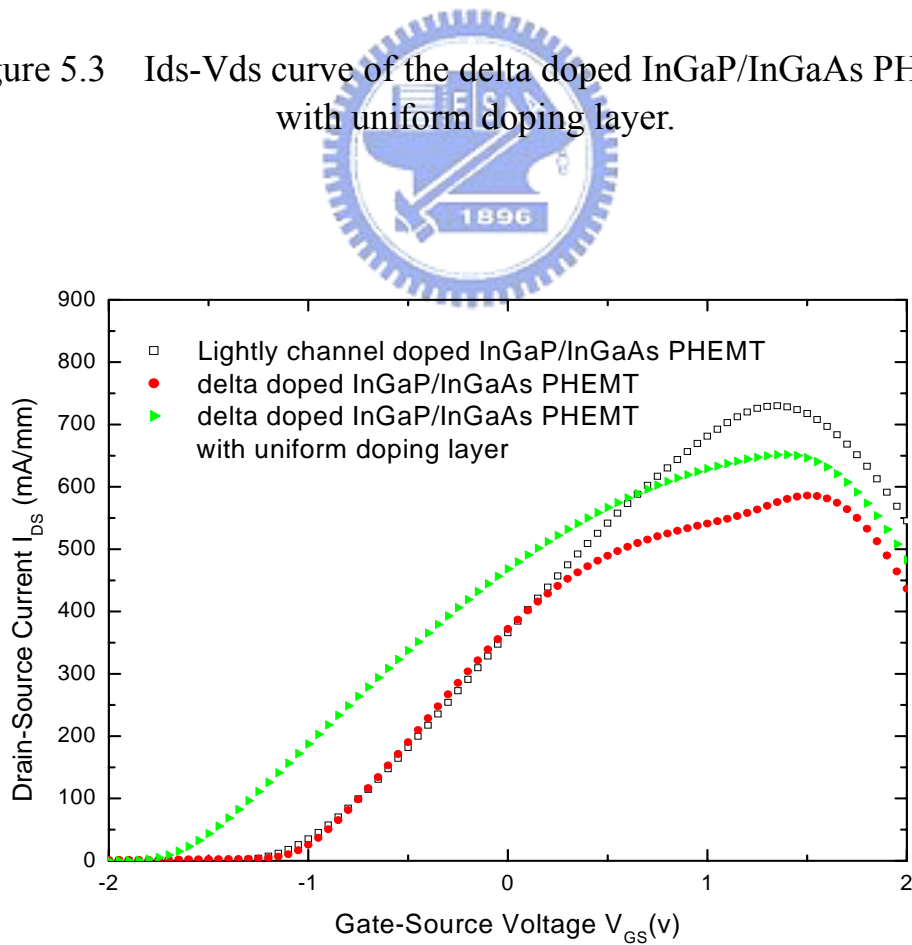
Figure 5.4   Ids-Vgs curve of the three InGaP/InGaAs PHEMT devices at
V_{ds} 1.5V.
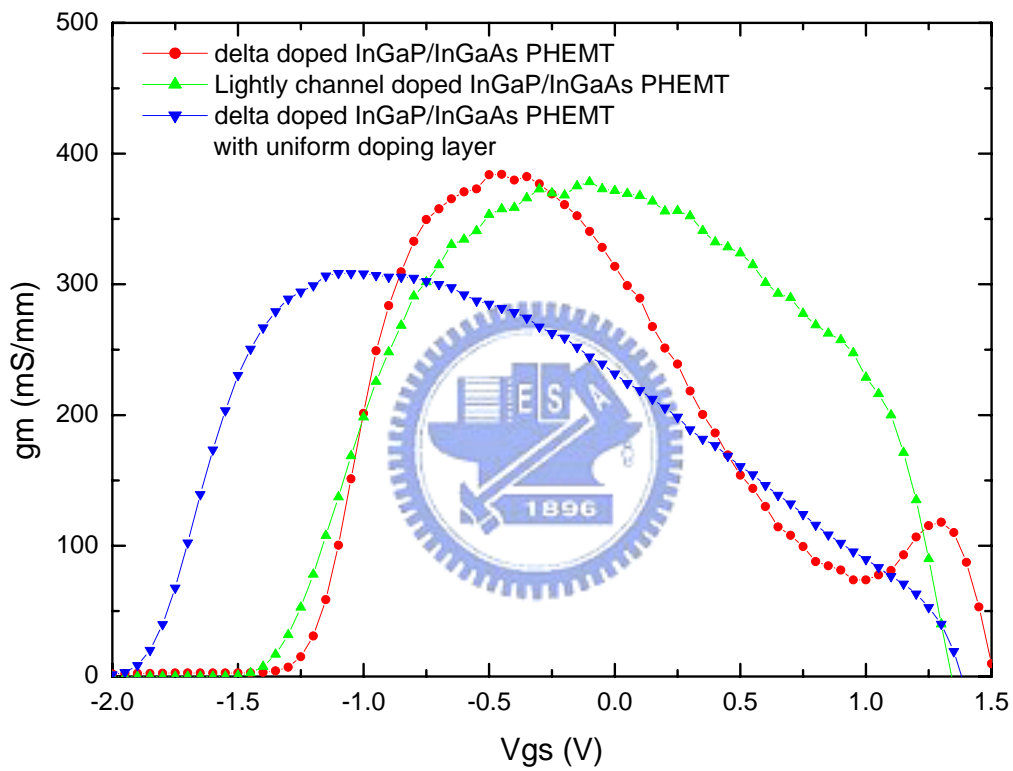
Figure 5.5 g_m curve as a function of gate bias of the InGaP/InGaAs PHEMT devices at V_{ds} 1.5V.

Device Type	Idss (Ids @ Vgs=0, mA/mm)	Ids-max (mA/mm)	Gm-max @Vds=1.5 V (mS/mm)	Ids first order constant: a_1	Ids third order constant: a_3	Ids fifth order constant: a_5	$|a_3/a_1|$	$|a_5/a_1|$
Conventional δ-doped InGaP PHEMT	376.30	585.94	384.13	0.0507	-0.0109	0.0011	0.2140	0.0995
Lightly-doped channel InGaP PHEMT	368.03	729.88	378.38	0.0586	-0.0035	-0.0042	0.0604	0.0711
Uniformly -doped layer InGaP PHEMT	497.99	651.56	308.5	0.0379	-0.0054	0.0046	0.1419	0.1226

Table 5.1 Comparisons of the DC characteristics of the three

InGaP/InGaAs PHEMT devices.
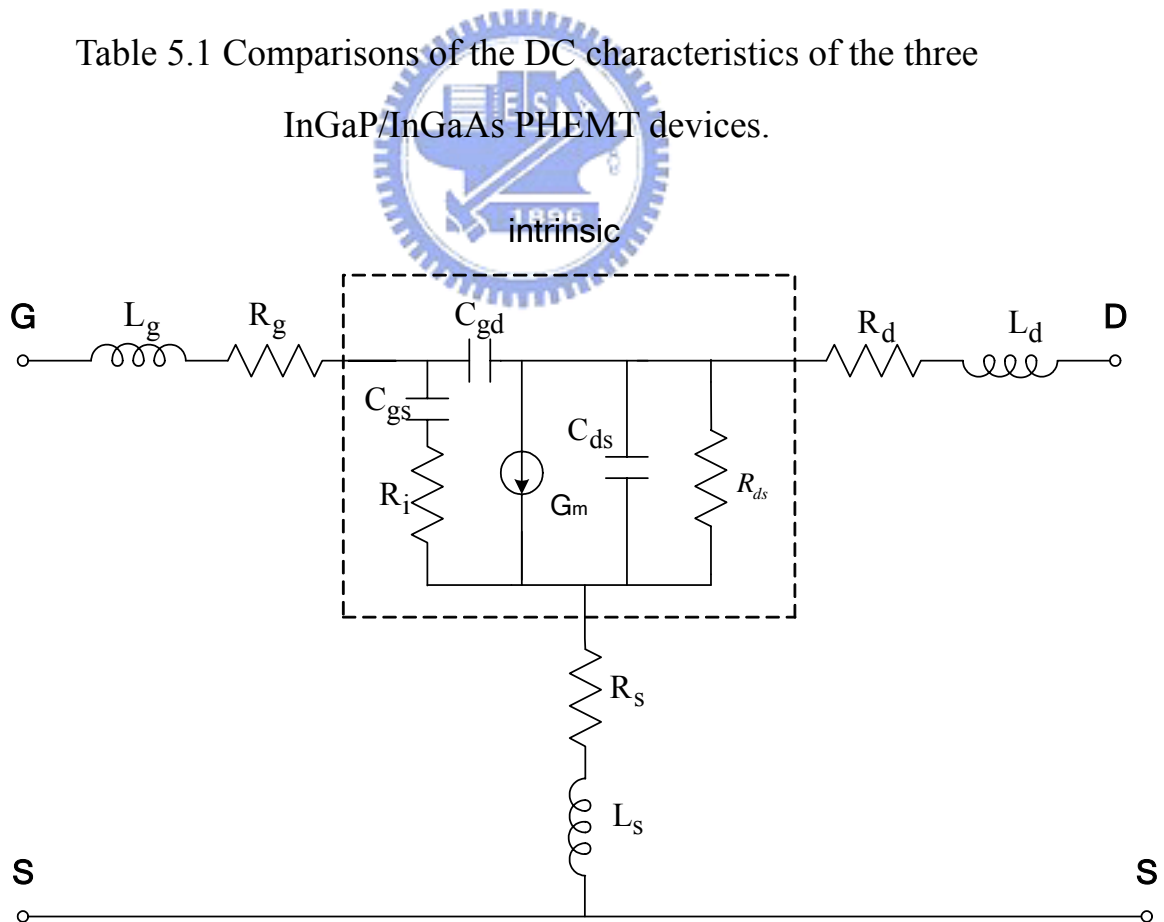
Figure 5.6   PHEMT small-signal equivalent circuit model.

(a)

S11 and S22

Swp Max
6GHz

Swp Min
1GHz

(b)

S12

Swp Max
6GHz

Swp Min
1GHz

59
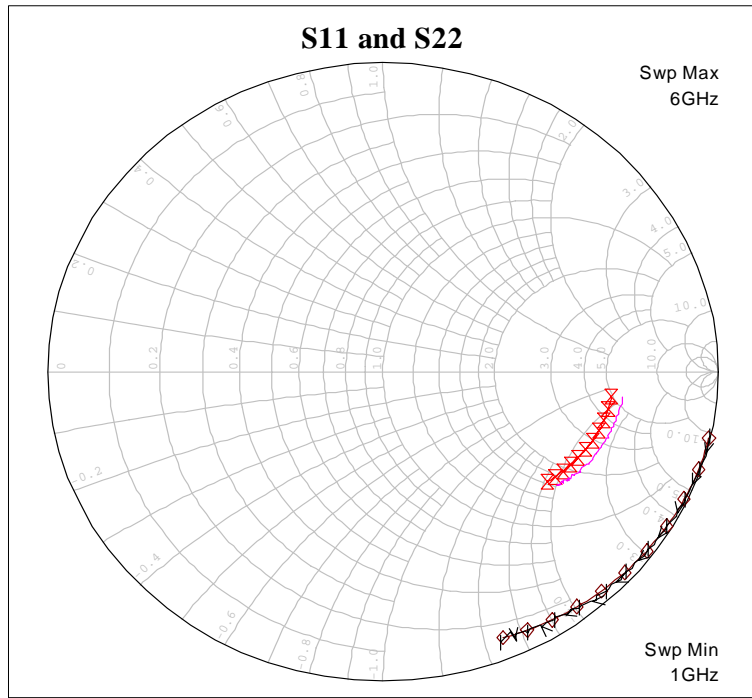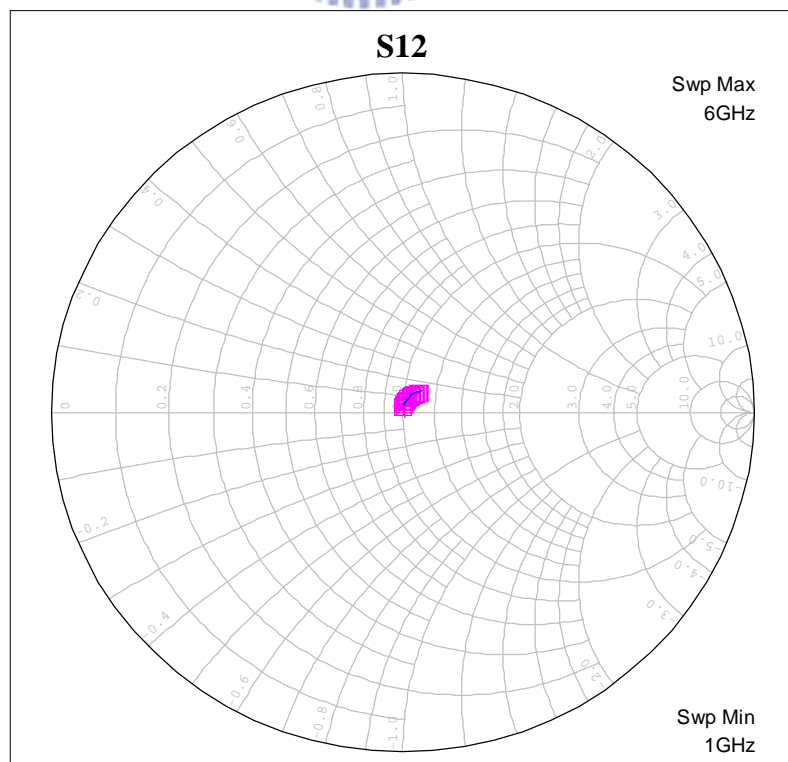
(c)
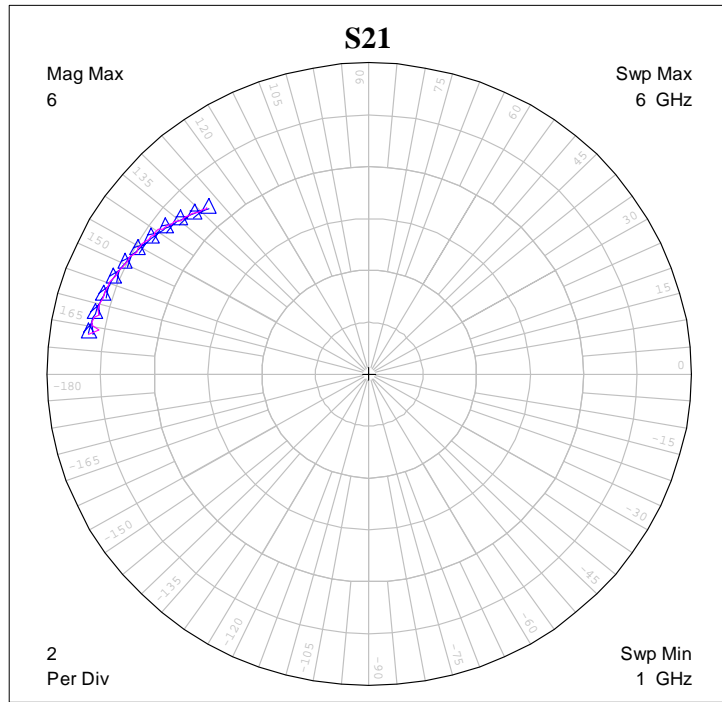
Figure 5.7   Measured *versus* modeled S-parameters for the conventional

δ-doped InGaP/InGaAs PHEMT device. (a) S_{11} and S_{22} (b) S_{12} (c) S_{21}

(Line: Measured, Line with marker: Modeled)

(a)
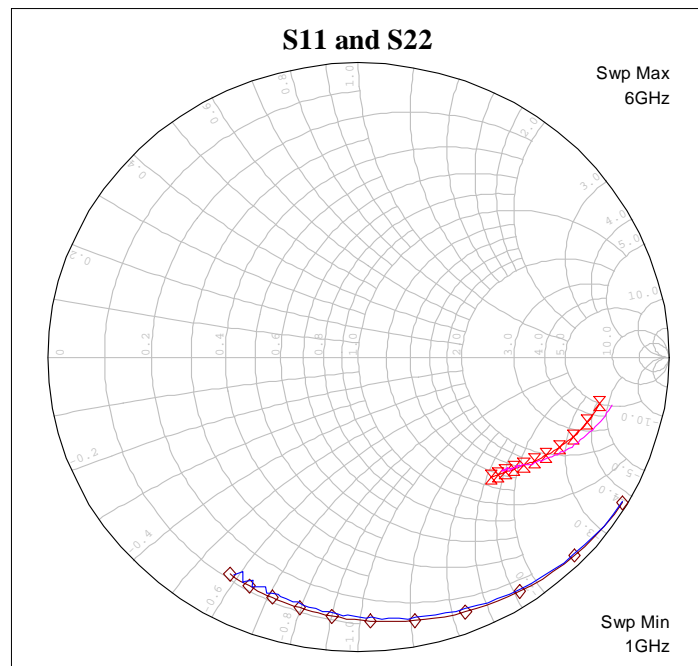
(b)
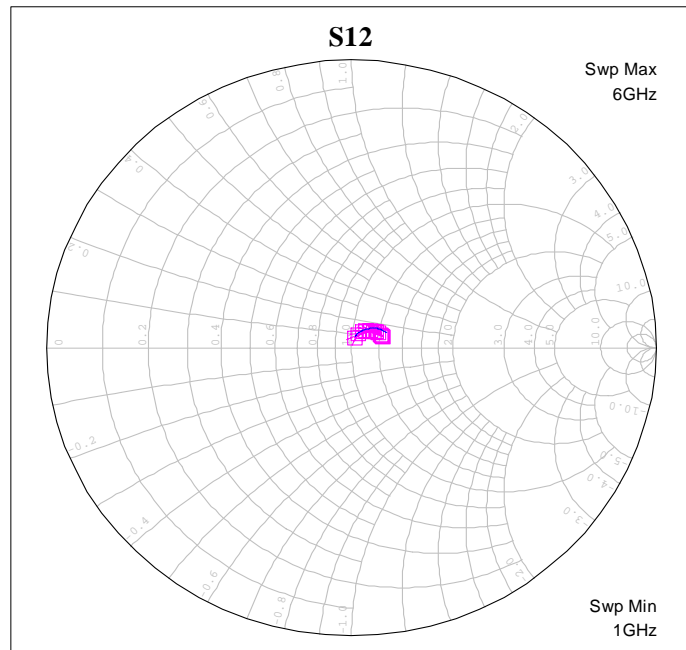
(c)
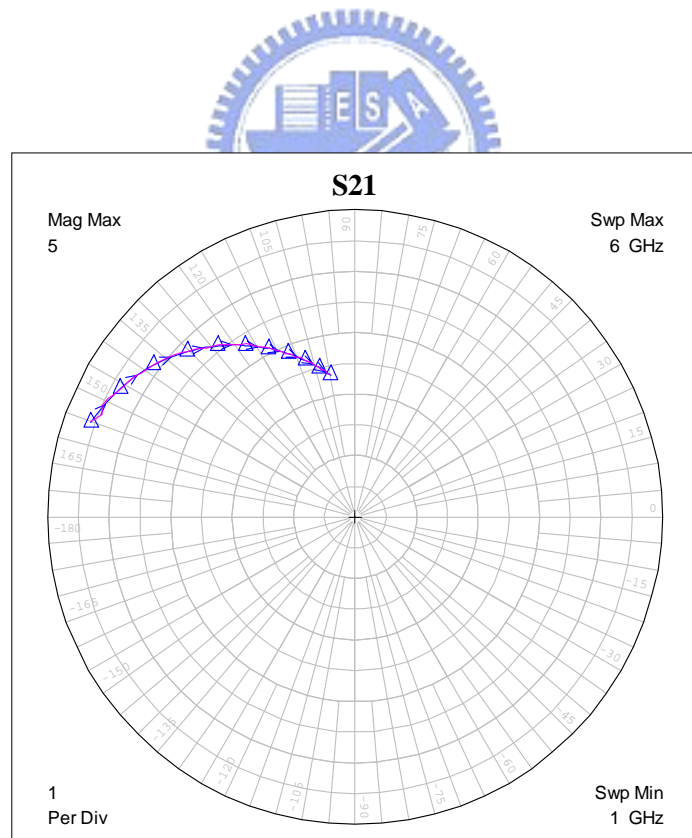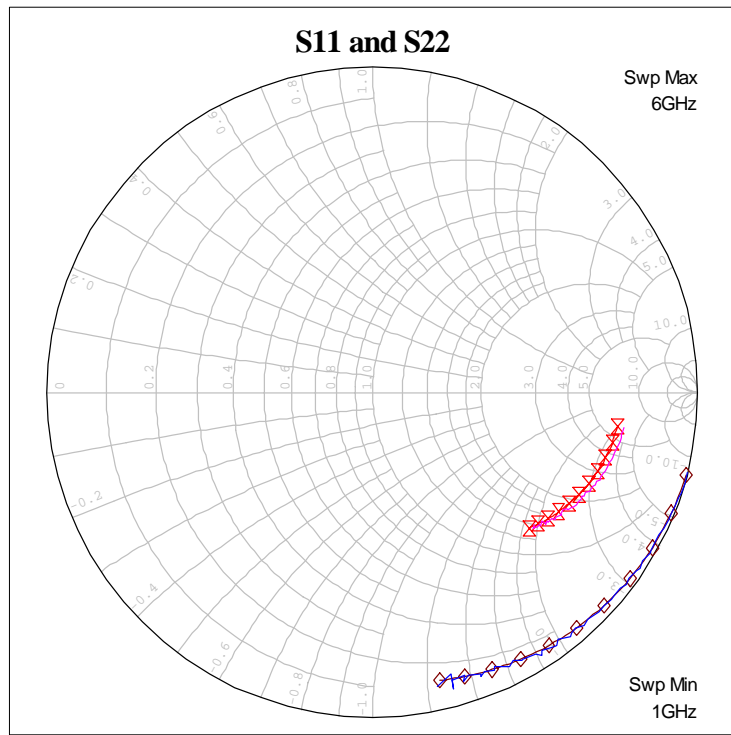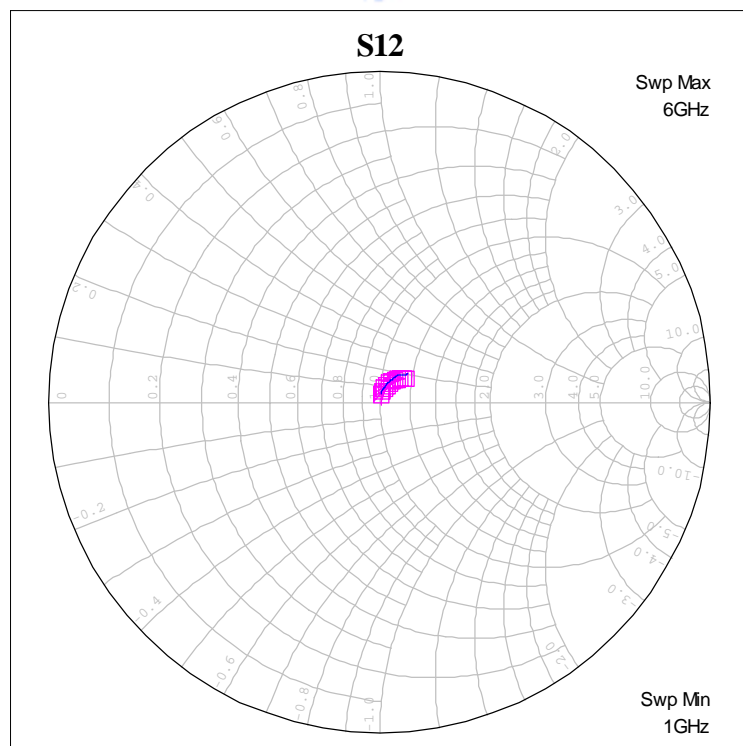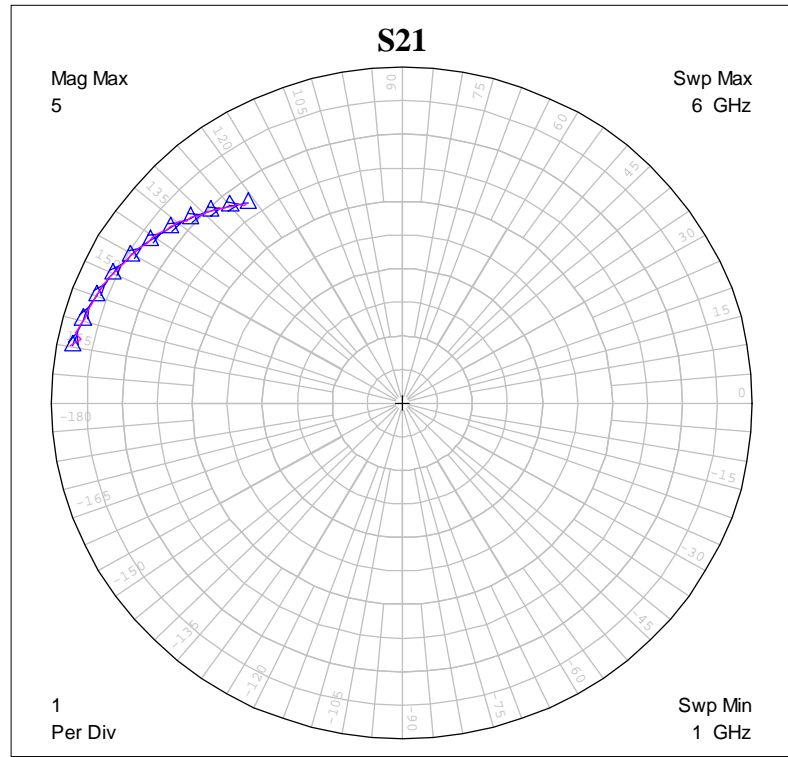

Figure 5.8   Measured *versus* modeled S-parameters for the lightly-doped

channel InGaP/InGaAs PHEMT device. (a) S_{11} and S_{22} (b) S_{12} (c) S_{21}

(Line: Measured, Line with marker: Modeled)

(a)

S11 and S22

Swp Max
6GHz

Swp Min
1GHz

(b)

S12

Swp Max
6GHz

Swp Min
1GHz

(c)

Figure 5.9   Measured *versus* modeled S-parameters for the
uniformly-doped layer InGaP/InGaAs PHEMT device.(a)S_{11} and S_{22} (b)
S_{12} (c) S_{21} (Line: Measured, Line with marker: Modeled)

Device Type	Cdg (fF)	Cgs (fF)	Cds (fF)	Rds (Ohm)	Ri (Ohm)	gm (mS)
Conventional δ-doped InGaP PHEMT	28.16	230.4	39.37	249.4	0.4990	69.04
Lightly-doped channel InGaP PHEMT	65.85	634.6	56.24	452.8	0.4743	56.43
Uniformly-doped layer InGaP PHEMT	41.10	258.1	40.32	346.8	0.4989	59.36

Device Type	Lg (pH)	Ld (pH)	Ls (pH)	Rg (Ohm)	Rd (Ohm)	Rs (Ohm)
Conventional δ-doped InGaP PHEMT	2.516	0.00144	4.113	1.895	2.296	1.202
Lightly-doped channel InGaP PHEMT	2.537	0.00144	4.590	2.746	3.003	1.157
Uniformly-doped layer InGaP PHEMT	2.513	0.00144	4.130	1.893	2.341	1.258

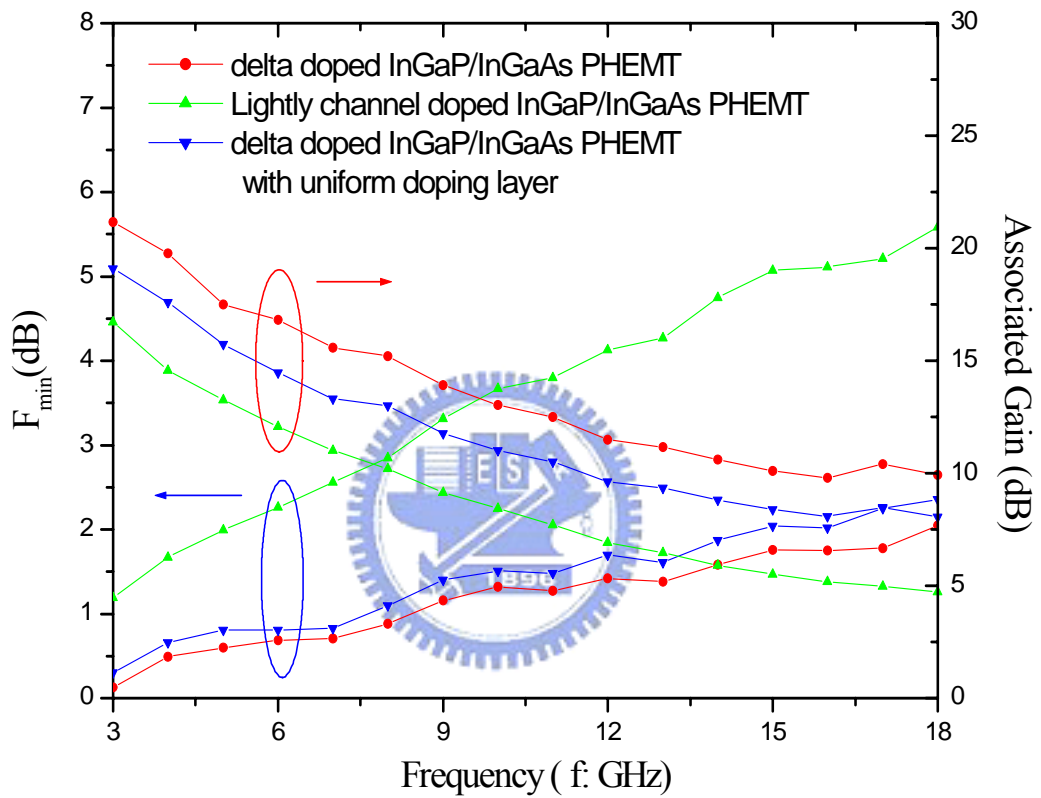Table 5.2   Extracted equivalent circuit parameters of the three devices

for comparisons.

Figure 5.10   Noise figure of the InGaP/InGaAs PHEMT devices biased

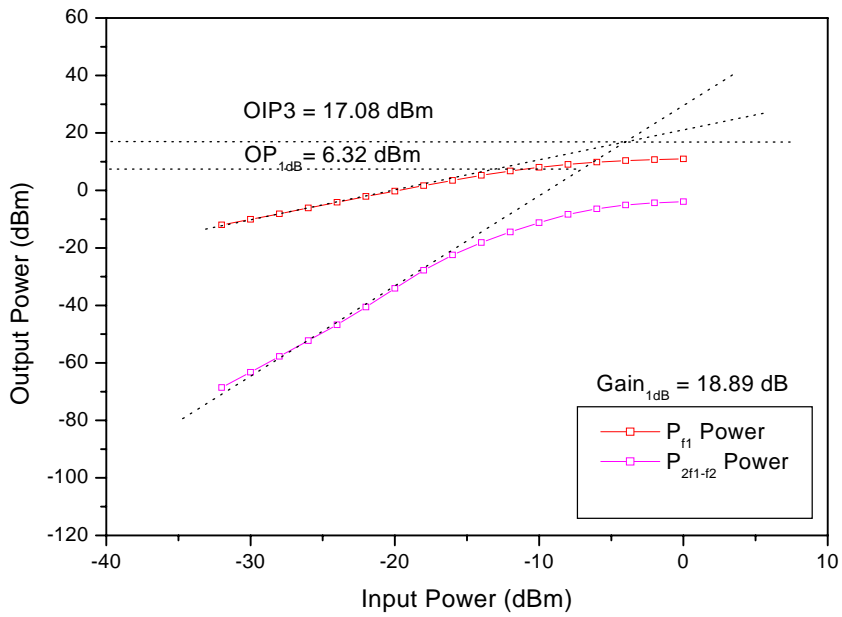at V_{ds} 1.5V and Ids = 20% Idss.

Figure 5.11   Measured OIP3 of the conventional delta doped
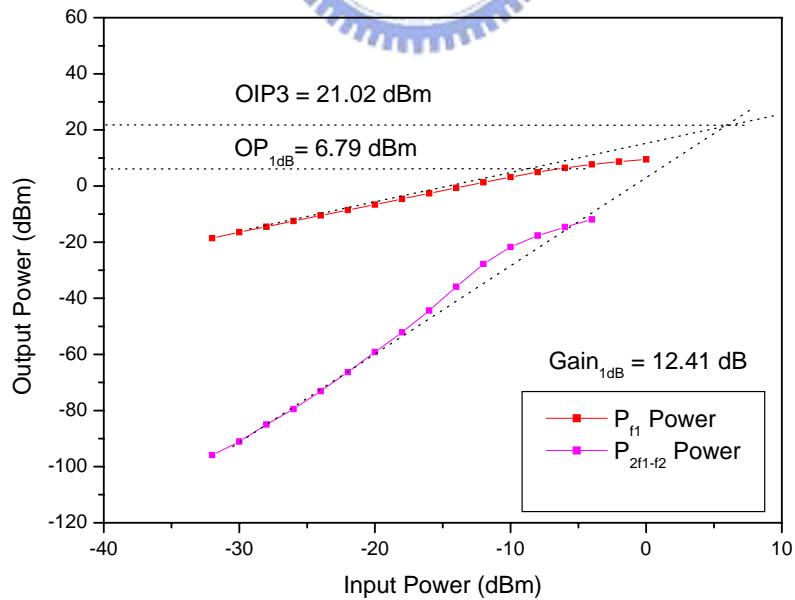
InGaP/InGaAs PHEMT.

Figure 5.12   Measured OIP3 of the delta doped InGaP/InGaAs
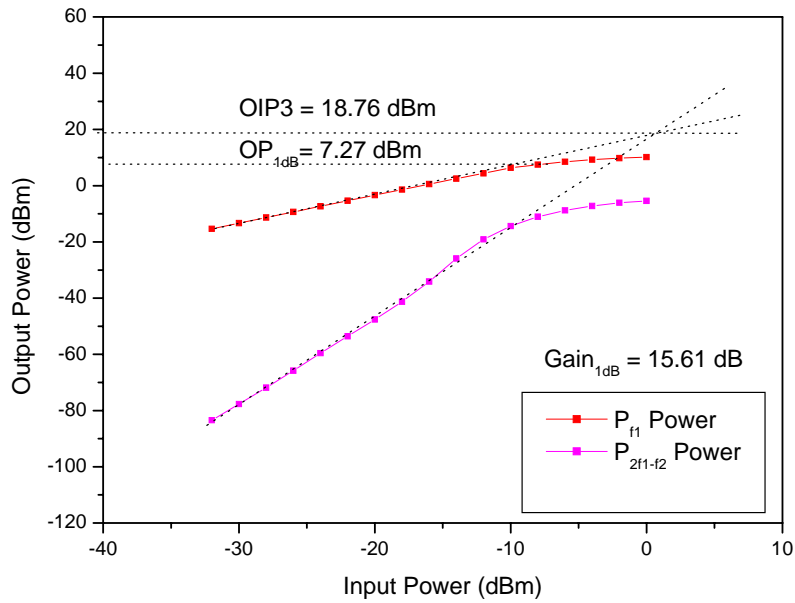
PHEMT with lightly doped channel.

Figure 5.13   Measured OIP3 of the delta doped InGaP/InGaAs
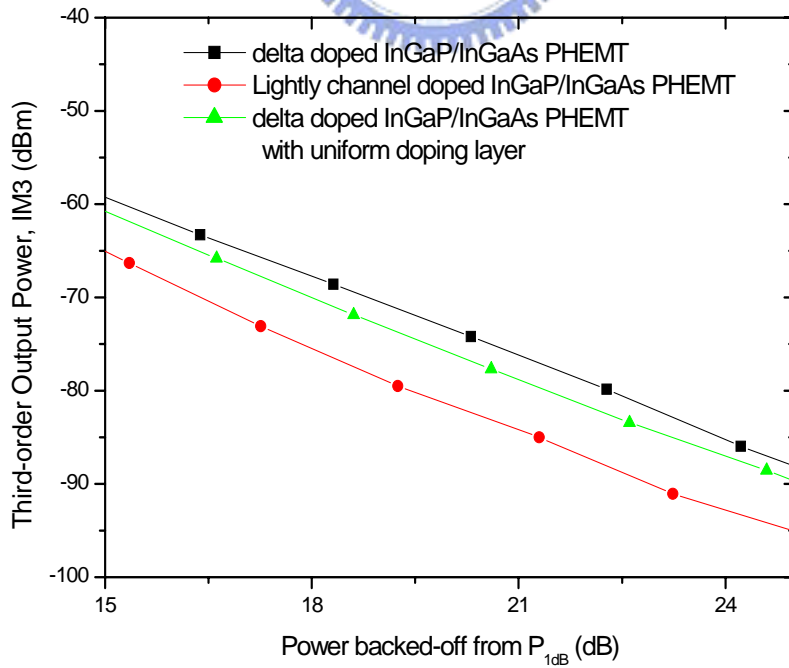
PHEMT with uniform doping layer.

Figure 5.14   Measured IM3 levels *versus* power backed off from P_{1dB}.

Device Type	P_{1dB} (dBm)	IP3 @6GHz (dBm)	Δ(IP3-P_{1dB}) (dB)	IP3/P_{DC}	F_{min} @6Ghz (dB)
Conventional δ -doped InGaP PHEMT	6.32	17.08	10.76	1.77	0.69
Lightly-doped channel InGaP PHEMT	6.79	21.02	14.23	4.97	2.26
Uniformly-doped layer InGaP PHEMT	7.27	18.76	11.49	5.73	0.82

Table 5.3 Comparisons of the RF characteristics of the three

InGaP/InGaAs PHEMT devices.