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Cobalt nanodots formed by annealing the CoSiO layer for the application of the nonvolatile memory

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Co nanodot memory devices formed by oxidation processes were studied. Transmission electron microscopy and x-ray photoelectron spectroscopy analyses showed that overoxidation of the cobalt and silicon degraded the charge-storage ability seriously. However, a precapped oxide can mildly oxidize the $CoSi_2$ film to protect the overoxidation to occur. In addition, an oxygen-incorporated $CoSi_2$ film is proposed to improve the oxidation process further. Through incorporating the limited oxygen during sputtering process, the Co nanodot memory device obtains a larger memory window. Also, the reliability characteristic of the Co nanodot memory device formed by annealing the oxygen-incorporated $CoSi_2$ film has been demonstrated. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3097810]

Recently, nonvolatile memory (NVM) devices attract much attention as the demand of portable electronic products increasingly. However, the conventional floating gate (FG) memory invented by Kahng and Sze[1] will face many issues such as retention, endurance, and power consumption as the memory devices scale down.[2,3] Therefore, Tiwari *et al.* presented nanodot (ND) structure instead of the FG as the next generation NVM structure.[4] In the reported literature, the metallic ND memory devices show superior charge-storage ability due to its available work functions, better channel coupling, and lower quantum confinement.[5,6] In addition, Co is the potential material for applying into the NDs structure by its compatibility and low resistivity.[7,8] In the reported method, the method of forming Co NDs by direct oxidation of $CoSi_2$ layer is advantageous to control the uniformity and distribution of NDs.[9–12] However, the oxidation process during the Co NDs formation is a main parameter for the charge-storage properties of the memory devices.

In our work, Co NDs as the charge-storage centers were formed by oxidation process for three kinds of structures. Electrical and material analyses indicate that the charge-storage ability and Co NDs formation were related to the $CoSi_2$ oxidation process. A precapped oxide structure is confirmed to restrain the $CoSi_2$ film overoxidation. In addition, we also proposed a Co ND formation by annealing an oxygen-incorporated $CoSi_2$ (CoSiO) film. The trapping layer formed by annealing CoSiO film shows good memory effect and reliability characteristics. Furthermore, it is easier to control the oxidation process by the CoSiO film than by the precapped oxide.

First, a 5-nm-thick oxide was grown on the *p*-type silicon wafer in atmospheric pressure chemical vapor deposition furnace. Afterward, a 6-nm-thick $CoSi_2$ thin film was deposited by sputtering system in Ar ambient. Then, the samples were divided into two groups with (sample A) and without a 20 nm precapped oxide (sample B). Subsequently, the 700 °C rapidly thermal annealing process in O_2 ambient (RTO) was performed for 60 s to oxidize the Si and form the Co NDs. Then, plasma enhanced chemical vapor deposition (PECVD) was used to form the total 50-nm-thick blocking oxide. In addition, a 6-nm-thick CoSiO thin film was also prepared to investigate the oxidation behavior further. The

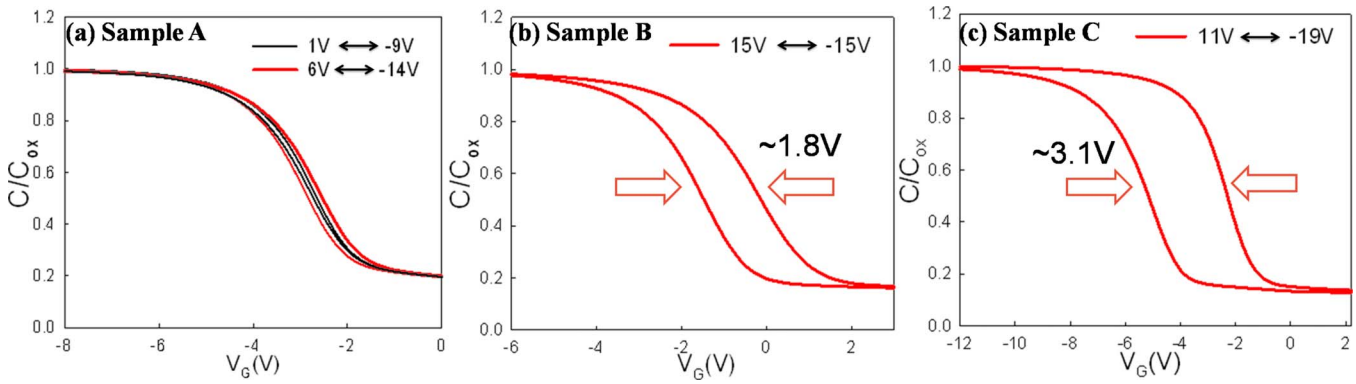

FIG. 1. (Color online) *C-V* hysteresis of (a) sample A (without a precapped oxide), (b) sample B (with a precapped oxide), and (c) sample C (CoSiO method).

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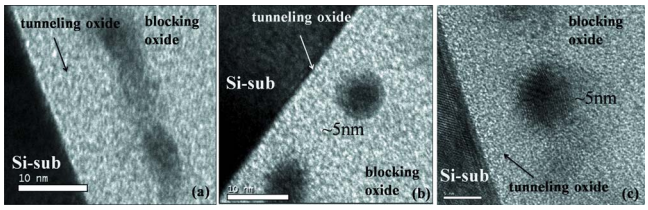

FIG. 2. (Color online) Cross-sectional TEM image of (a) sample A, (b) sample B, and (c) sample C.

TABLE I. List of the formed Co ND density, size, and memory window in samples A, B, and C.

	Annealing process	Size range (nm)	Density (cm^{-2})	Memory window (V)
Sample A	RTO			~0.2
Sample B	RTO	4–5	2.7×10^{11}	1.8
Sample C	RTA	4–5	3.2×10^{11}	3.1

CoSiO thin film was deposited by sputtering the $CoSi_2$ target in Ar/O_2 [24/10 SCCM (SCCM denotes standard cubic centimeter per minute at STP)] environment (sample C). After the rapid thermal annealing (RTA) process and blocking oxide deposition, the top and bottom Al gate electrode were patterned. Capacitance-voltage (*C-V*) measurement was used to study the memory characteristics of these samples. Also, transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) were also adopted for Co ND formation.

Figure 1 exhibits the *C-V* characteristics of (a) sample A, (b) sample B, and (c) sample C. It is found a negligible flatband voltage (V_{FB}) shift was obtained in sample A after bidirectional gate voltage sweep. The memory window does not enlarge obviously even the voltage operation is increased. However, samples B and C show a V_{FB} shift of 1.8 and 3.1 V under ±15 V gate voltage operation, respectively.

Figure 2 shows the TEM images of (a) sample A, (b) sample B, and (c) sample C. We find that the sample A causes no Co ND formation. However, the Co NDs are located at the interface of tunneling oxide in samples B and C obviously. Table I lists the Co NDs size, density, and the memory window of samples A, B, and C. Through comparing with the results of the *C-V* and TEM analyses, the oxidation process indeed affects the memory effect and NDs formation.

Figure 3 demonstrates the Co 2*p* XPS results of samples A, B, and C. Figure 3(a) shows that the main composition of the $CoSi_2$ layer after RTO process is Co–O binding

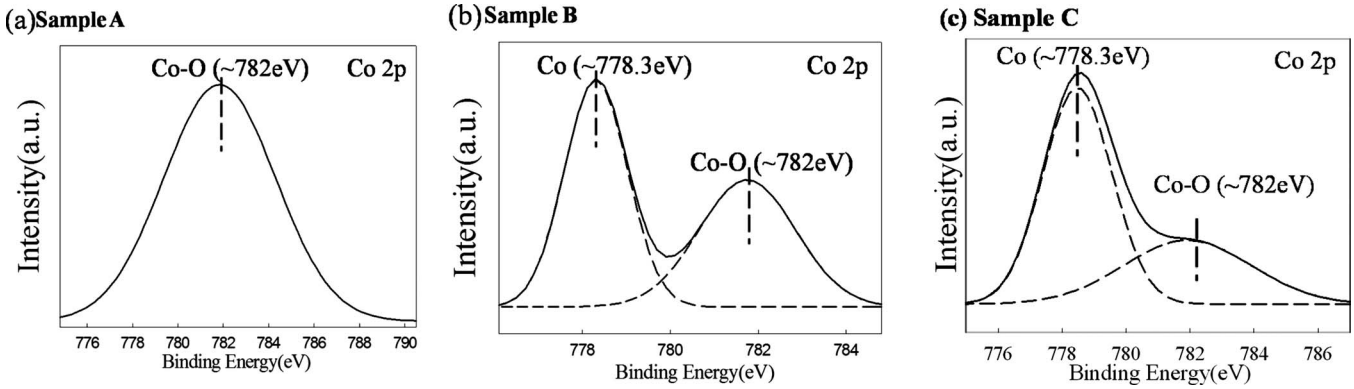

FIG. 3. Co 2*p* XPS analysis of (a) sample A, (b) sample B, and (c) sample C.

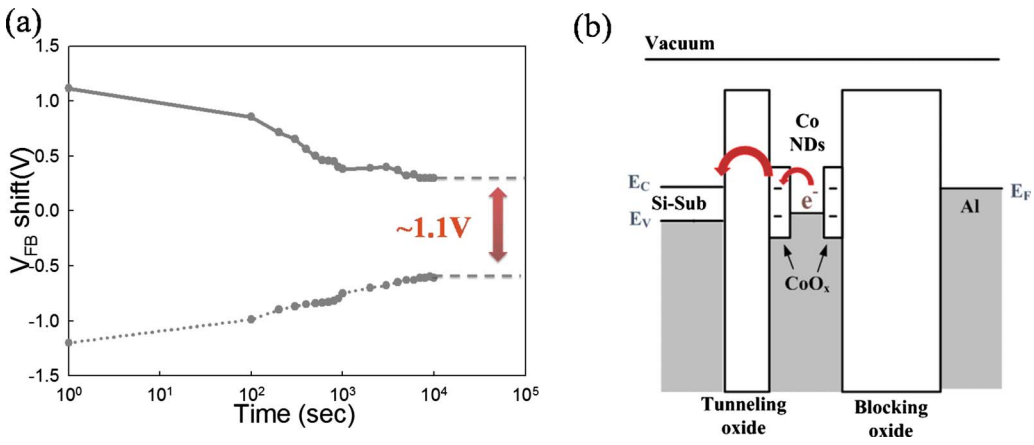

FIG. 4. (Color online) The (a) measurement results and (b) energy band diagram of sample C about the retention characteristics.

(~782 eV). It means that the RTO process completely oxidized the trapping layer and retarded the Co NDs formation. Compared with samples A and B, we confirmed that the precapped oxide improves the formation of Co NDs. The $CoSi_2$ in sample B was transferred to partially CoO_x and Co (~778.3 eV), as shown in the Fig. 3(b). From the consideration of Gibbs free energy, the thermodynamics theory indicates that Si is easier to be oxidized than Co during RTO process.[13–15] The lower oxidation free energy for SiO_2 cause the formation of Co NDs embedded in SiO_2 dielectrics layer. However, the oxidation condition is difficult to be controlled for Co ND formation by the RTO system.[16] The softer oxidation condition by the precapped oxide only oxidize the Si and a small amount of Co. Nevertheless, the precapped oxide method needs an additional PECVD deposition. The CoSiO method to form Co NDs is easier and more effective. The XPS result in Fig. 3(c) indicates that the Co–O binding in sample C is lower than sample B because the oxygen content is limited by the sputtering parameter. The $CoSi_2$ oxidation only depends on the internal oxygen content of the CoSiO film. With the limited oxygen content, the Co element in the CoSiO layer prefers to form Co NDs, instead of forming CoO_x, which provides enough charge-storage sites.[13]

The reliability characteristic of sample C was also tested in the following experiment. The retention measurement was performed at room temperature by operating a ± 15 V gate voltage stress for 10 s and measured up to 10^4 s. It is found that sample C reveals obvious decay at the initial 10^3 s, as shown in Fig. 4(a). The decay at the initial duration resulted from some charges, which passed through the defect of the CoO_x are easier to tunnel back to the substrate as shown as the energy-band diagram of Fig. 4(b).[17] Nevertheless, the memory device maintains 1.1 V for 10^4 s steady after 10^3 s. The Co ND memory device using the annealed CoSiO film as trapping layer exhibits a good reliability characteristic for the application of NVM device.

In conclusion, Co ND memory devices formed by three kinds of structures have been shown in this work. Oxidation control during the Co ND formation is indicated as the important parameter to affect the charge-storage ability. The memory window was degraded because that the Si and Co were completely oxidized in the virgin $CoSi_2$ layer for over-oxidation. With a limited oxygen flow by preoxide deposition, the Co ND performance is improved obviously. Furthermore, the Co ND formation can be more easily controlled by incorporating oxygen elements into $CoSi_2$ layer during sputtering process. The Co–O content in annealed CoSiO layer is lower than in oxidized $CoSi_2$ layer. Hence, Co NDs embedded in CoO_x and SiO_x layer contributes larger memory window than oxidizing $CoSi_2$ layer with or without oxide capping.

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[1] D. Kahng and S. M. Sze, Bell Syst. Tech. J. **46**, 1288 (1967).
[2] J. De Blauwe, IEEE Trans. Nanotechnol. **1**, 72 (2002).
[3] Z. Tan, S. K. Samanta, W. J. Yoo, and S. Lee, Appl. Phys. Lett. **86**, 013107 (2005).
[4] S. Tiwari, F. Rana, K. Chan, H. Hanafi, C. Wei, and D. Buchanan, Tech. Dig. - Int. Electron Devices Meet. **1995**, 521.
[5] A. Chandra and B. M. Clemens, Appl. Phys. Lett. **87**, 253113 (2005).
[6] K. S. Seol, S. J. Choi, J. Y. Choi, E. J. Jang, B. K. Kim, S. J. Park, D. G. Cha, I. Y. Song, J. B. Park, Y. Park, and S. H. Choi, Appl. Phys. Lett. **89**, 083109 (2006).
[7] M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J.C. Shim, H. Kurino and M. Koyanagi, Tech. Dig. - Int. Electron Devices Meet. **2003**, 22.5.1.
[8] S. Vaidya, S. P. Murarka, and T. T. Sheng, J. Appl. Phys. **58**, 971 (1985).
[9] M. V. Rastei, R. Meckenstock, J. P. Bucher, E. Devaux, and Th. Ebbesen, Appl. Phys. Lett. **85**, 2050 (2004).
[10] D. Zhao, Y. Zhu, and J. Liu, Solid-State Electron. **50**, 268 (2006).
[11] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, Appl. Phys. Lett. **90**, 132102 (2007).
[12] J. Y. Yang, K. S. Yoon, W. J. Choi, Y. H. Do, J. H. Kim, C. O. Kim, and J. P. Hong, Curr. Appl. Phys. **7**, 147 (2007).
[13] J. Chevallier and A. N. Larson, Appl. Phys. A: Solids Surf. **39**, 141 (1986).
[14] I. Barin and O. Knacke, *Thermochemical Properties of Inorganic Substances* (Springer, Berlin, 1977).
[15] M. Bartur and M. A. Nicolet, J. Appl. Phys. **54**, 5404 (1983).
[16] F. M. Yang and M. C. Chen, Thin Solid Films **207**, 75 (1992).
[17] A. Miura, Y. Uraoka, T. Fuyuki, S. Yoshii, and I. Yamashita, J. Appl. Phys. **103**, 074503 (2008).