# Improved Current Sharing Performance by Dynamic Droop Scaling Technique in Multiple Power Systems

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***Abstract*** **- This paper presents a novel dynamic droop scaling (DDS) technique for paralleled power modules. The major concern is the uniform current distribution of each module in multiple power systems. The droop method relies on the slope characteristic of load regulation to achieve current sharing accuracy. Owing to the trade-off between error percentages of current sharing and output voltage variation, conventional droop technique can't provide good load regulation and current balance at the same time. However, the proposed DDS technique can break through the limitation of the conventional droop method by the implementation of dual current sensing loops. The dual current sensing loops not only increase the droop gain but also compensate the extra output dropout voltage automatically according to the steeper slope value of the novel method. Simulation results verify the error percentage of current sharing accuracy can be improved from 42.5% to 8.2% by DDS technique.**

***Keywords*** **- Droop technique, dual loop, and current sharing.**

## I. INTRODUCTION

Paralleling of DC-DC converter modules offers a number of advantages over a single centralized power supply. The benefits of paralleled powered supplies include expandability of output power, effective thermal management and ease of maintenance [1] [2].

When several DC-DC converters are connected in parallel, the major concern is the uniform current distribution of each converter. If the current-sharing mechanism of the converter system is not designed well, one or more modules will bear higher load current and so as temperature. As the result the reliability of the system will be reduced and the merits of paralleled powered supplies will not be as significant as expected. Many current sharing methods with different complexity and current-sharing performance were proposed in the past [3~12]. Among these methods, the simplest and without any interconnections between the paralleled connected modules is the droop method.

The output voltage of the power supply using droop method drops as the load current increases [3] [6].The current-sharing mechanism of this method relies on the slope of the load regulation characteristic of the paralleled connected modules. There are many different ways to implement the output voltage droop characteristic: with serial resistor, output current feedback, and current mode with low DC gain. However, the slope of the conventional droop method will be limited to the specified output-voltage regulation range. Therefore, this method exhibits poor current accuracy among current sharing mechanism.

In this paper, we propose a novel dynamic droop scaling technique to break through the limitation of conventional droop method. We describe the limitation of conventional droop method in section II and propose the new droop method in section III. In section IV, we describe the implementation of the DDS technique. Simulation results show the good current-sharing performance between two separate power supply modules in section V. We make a conclusion in section VI.

## II. DISADVANTAGES OF CONVENTIONAL DROOP METHOD

Two major control parameters are the value of difference voltage ($\Delta V_{o(set)}$) at no load and the value of droop slope when we adapt conventional droop method in parallel systems. The former is the variations between different power supply modules. The tolerance of $\Delta V_{o(set)}$ is usually controlled within $\pm 1\%$ value of output set-voltage $V_{o(set)}$. Thus, the design margin for droop method is limited to $\Delta V_{o(drp)}$, which is written as equation (1). Fig. 1 shows the relationship between output current and voltage for the droop method.

$$\Delta V_{o(drp)} = I_{o(rate)} \cdot K = \Delta V_{o(\max)} - \Delta V_{o(set)} \quad (1)$$

$$\Delta I_o = I_{o1} - I_{o2} = \frac{\Delta V_{o(set)}}{K} \quad (2)$$

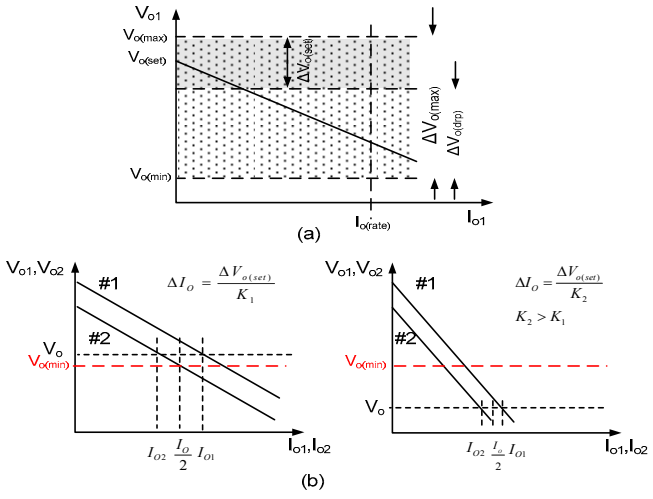


Fig. 1. Specification of current sharing technique.

$I_{o(rate)}$ is rated current load, $\Delta V_{o(max)}$ is maximum acceptable output voltage variation of the system, and $K$ is the droop slope. From Fig. 1, the maximum current deviation between two power supply modules is inversely proportional to the value of $K$. It means that the larger the value of K is, the smaller the deviation between two power supply modules is. However, owing to the steeper slope of droop method, the voltage variation will exceed the allowable minimum output value $V_{o(min)}$ at rated current load. In other words, there is trade-off between error percentage of current sharing and output voltage variation. Our proposed method breaks through the limitation of conventional droop method.

## III. Dynamic Droop Scaling Technique

### A. Principle of dual current sensing loop

The major problem of conventional droop method is the limitation of the value of droop slope. Thus, dynamic droop scaling (DDS) circuit shown in Fig. 2 is added to the conventional external resistor method to exceed the limitation of conventional droop method. The external resistor is composed of the on-resistance of ORing MOSFET, which is used to prevent the individual power supply module from burning out because of short circuit [13]. The increment of load current increases the value of $\Delta V_C$ by flowing through the $R_{ds(on)}$ of ORing MOSFET, and therefore the output current of transconductor Gm also increases. Because the negative terminal of the error amplifier is close to the value of $V_{ref}$, the current generated by transconductor flows through resistor R1 to generate a voltage drop, which is equal to $\Delta V_d$. The total voltage drop due to the increment of load current is the sum of $\Delta V_C$ and $\Delta V_d$. In Fig. 3, we can write the new droop slope $K_a$ as equation (3):

$$K_a = \frac{\Delta V_c + \Delta V_d}{I_{o(rate)}} = \frac{I_o R_s + I_o R_s g_m R_1}{I_{o(rate)}} = R_s(1 + g_m R_1) = R_s \cdot (1 + C_a) \quad (3)$$

where $C_a$ is equal to $g_m R_1$

It means that the value of new droop slope is $(1+C_a)$ times of conventional droop slope in Fig. 4. The variations of $R_{ds(on)}$ values for different ORing MOSFETs can be compensated by the term of $g_m R_1$ in equation (3). We don't need to put much effort on the selection of external components for whole multiple-supplies system. Furthermore, owing to the larger value of droop slope $K_a$, the error percentage of current-sharing performance is reduced by a factor $(1+C_a)$.

$$\Delta I_{o(\max)} = \frac{\Delta V_{o(set)}}{K_a} = \frac{\Delta V_{o(set)}}{K \cdot (1 + C_a)} \quad (4)$$

Compared with conventional droop method, the new DDS technique consumes less power because only $\Delta V_{o(drp)}/(C_a+1)$ is dissipated by ORing MOSFET. The rest voltage drop $[\Delta V_{o(drp)} C_a/(C_a+1)]$ is dissipated by resistor $R_1$. Fortunately, the current flowing through resistor $R_1$ is only $I_o R_s g_m$, which is smaller than $I_o$.

### B. Incremental output voltage circuit

Generally speaking, the enhancement of droop slope deteriorates the minimum allowable output voltage at rated load current. Therefore, within the range of minimum allowable output voltage and maximum allowable rated current, we need to raise the output voltage about $\Delta V_{o(drp)}$ for every $I_{o(rate)}/(C_a+1)$. In Fig. 4, when the load current transits from region I to II, we raise the output voltage about $\Delta V_{o(drp)}$ in order to meet the specification. Equation (5) and (6) describes the operation between two regions.

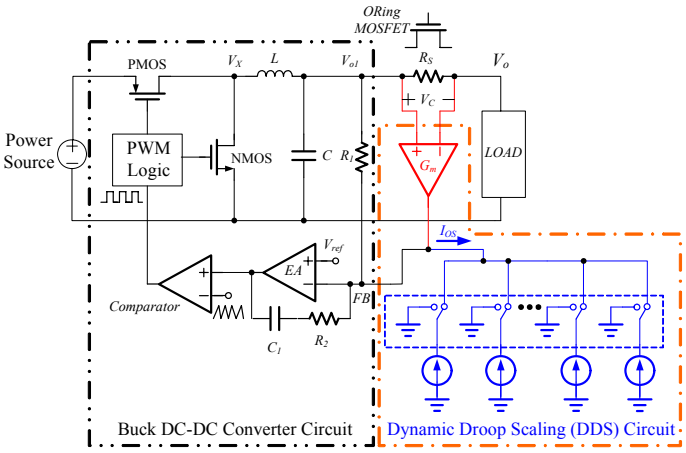


Fig. 2. Current sharing controller with DDS technique in single power supply module.

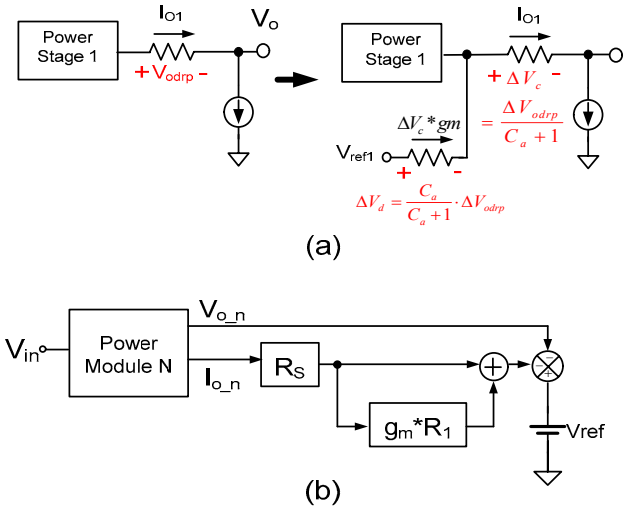


Fig. 3. Modified droop technique to reduce the power dissipation on sensing resistor $R_s$ (a) Insertion of another sensing loop to conventional droop technique. (b) Flow diagram of new dual sensing loop of DDS technique.

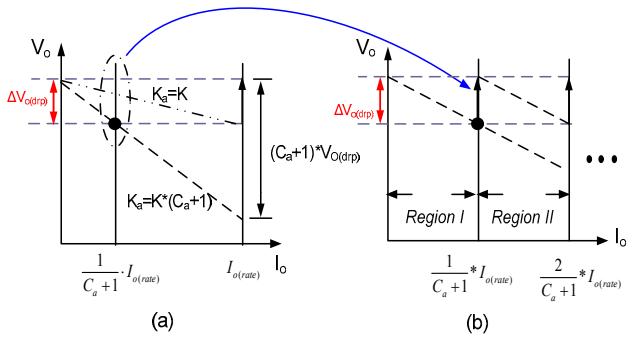


Fig. 4. Operation of DDS technique.

$$V_o = V_{ref} - I_o \cdot K_a \text{ where } I_o < \frac{1}{(C_a+1)} \cdot I_{o(rate)} \quad (5)$$

$$V_o = V_{ref} + \Delta V_{o(drp)} - I_o K_a \text{ where } \frac{1}{(C_a+1)} \cdot I_{o(rate)} < I_o < \frac{2}{(C_a+1)} \cdot I_{o(rate)} \quad (6)$$

By extending two raising regions to $C_a$+1 raising regions according to the new drop slope, we show the relationship between load current and output voltage in Fig. 5. Owing to the compensation for extra voltage drop of $C_a$+1 raising region, the error percentage of current-sharing performance can be shrunk to only 1/($C_a$+1) times that of the conventional droop method.

## IV. Implementation of DDS Technique

The implementation of dynamic droop scaling technique is composed of the high linearity transconductor and the circuit of incremental output voltage. High linearity transconductor defines low power dissipation performance of droop technique and the circuit of incremental output voltage surpasses the limitation of conventional droop technique.

### *A. High linearity transconductor*

As we know, the linearity of transconductor is important in our proposed dynamic droop scaling technique. In Fig. 6, the output current of transconductor decides the droop slope of every supply module. Thus, for the system with the $i^{th}$ power module shown in Fig. 6, the linearity of transconductor decides the error current among these supply modules. In order to improve the linearity of the transconductor, we use the flipped voltage follower (FVF) technique to reduce the output impedance [14, 15]. In Fig. 7, input differential pairs are composed of flipped voltage follower pairs, which are (M1, M3) and (M2, M6). It means that the linearity of the transconductor can be improved by the characteristic of low output impedance of FVF. Furthermore, after the conversion of transconductor $G_m$, S/H circuit samples the load current every switching period and hold this value as $I_{ogm,avg}$, which is written as equation (7) and shown in Fig.6.

$$I_{ogm,avg} = I_o R_s g_m \quad (7)$$

This average current is mirrored to two current branches. One is sent to error amplifier for the operation of droop method in Fig. 6. The other one is sent to incremental output circuit to decide the operating region in Fig. 8.

### *B. Circuit of incremental output voltage*

Fig. 8 shows the circuit of incremental output voltage, which contains a current mirror, a current comparator array, and an adder of raising current. The average current $I_{ogm,avg}$ is sent to compare with reference current sources from $1/(C_a+1)I_{REF}$ to $C_a/(C_a+1)I_{REF}$ to determine the increment current of $I_{os}$. The raising current $I_{os}$ flows through resistor $R_1$ in Fig. 2 to generate constant voltage $\Delta V_{o(drp)}$, and therefore provides the extra compensation voltage $\Delta V_{os}$ in $C_a$+1 raising regions. The value of $\Delta V_{os}$ relies on the new drop slope as equation (8):

$$\Delta V_{OS} = \Delta V_{o(drp)} \cdot (C_a + 1) \quad (8)$$

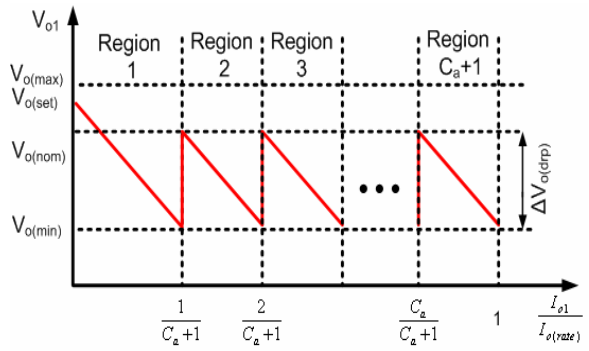


Fig. 5. $C_a$+1 raising voltage region for breaking through the limitation of conventional droop technique.

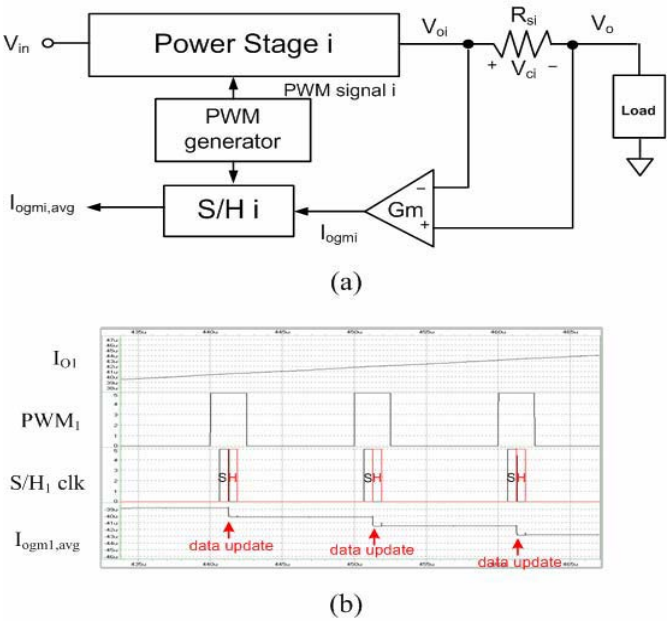


Fig. 6. (a) Proposed dynamic droop scaling technique in the $i^{th}$ power module. (b) Output current waveform after the sample/hold circuit.

For example, if factor $C_a$ is set to 1, 2 or 3 times the value resulted form the conventional method ($C_a$=0), offset current source is composed of twelve identical current sources from $I_{os1}$ to $I_{os12}$. As the result, the decision codes ($SW_0$~$SW_{11}$) will be sent to current mirror array with a sequence. The switches from switch 0 to switch 11 are turned on according to the operating region. In other words, the larger the load current is, the more switches are turned on. Owing to the implementation of incremental output voltage circuit, the output voltage will not exceed the allowable minimum output voltage at rated load current.

## V. Simulation Results

The proposed DDS circuit has been implemented in TSMC double-poly quadruple-metal 0.35- $\mu$ m CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 V and 0.65 V, respectively. The chip micrograph is shown in Fig. 9.

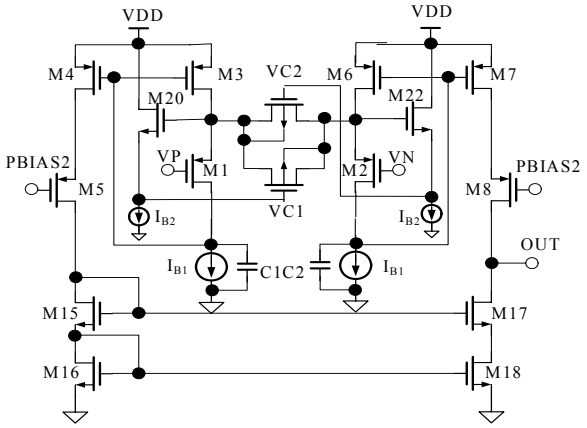


Fig. 7. Modified FVF technique [15] in transconductor $G_m$ to improve the linearity of transconductor.

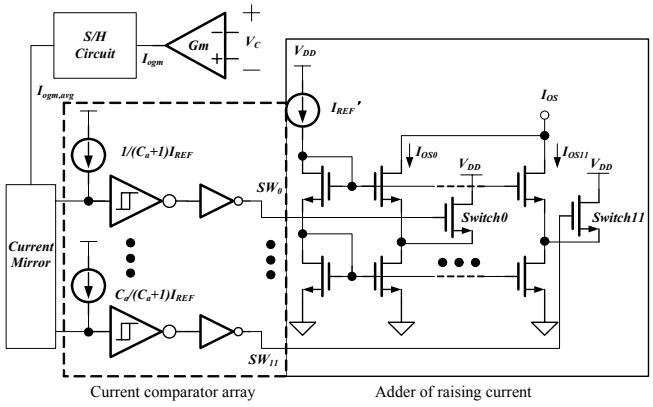


Fig. 8. Schematic of circuit of incremental output voltage is composed of a current mirror, a current comparator array, and a adder of raising current.

A simple and fast test circuit is set up to verify the function of the DDS technique in Fig. 10. Input terminals of OP1 and OP2 are connected to different reference voltages, $V_{REF1}$ and $V_{REF2}$, which represent the output voltages of individual power modules at no load condition. Amplifiers OP1 and OP2 are used to convert input currents to individually proportional output voltages. Two RC low-pass filters are added to output nodes $V_{O1A}$ and $V_{O2A}$ of voltage followers OP3 and OP4, respectively, for attenuating high-frequency noise. Moreover, amplifiers OP5 and OP6 act as two comparators to detect the directions of current, which are flowing through resistors $R_{S1}$ and $R_{S2}$. When the current flows from nodes $V_{O1}$ and $V_{O2}$ to node $V_O$, the voltages across resistors $R_{S1}$ and $R_{S2}$ are positive, and then transistors M1 and M2 are turned on. On the contrary, when current flows reversely, the output voltages of OP5/OP6 go low to turn off transistors M1 and M2. Current load $I_o$ is used to simulate the output current variation of the system.

We can quickly verify the performance of current sharing by the test circuit in Fig. 10. For example, when $V_{REF1}$, $V_{REF2}$ is set to 3.03V and 3.0V individually, the values of $R_{S1}$ and $R_{S2}$ are 1KΩ, and $C_a$ is selected to 3. The difference between $I_{O1}$ and $I_{O2}$ will be 7.5uA according to equation (4), as show in Fig.11.Compared with conventional droop method, the current sharing error will be improved by four times. The incremental voltage circuit raises the output voltage to meet the allowable minimum output voltage every transition of load current. Table I summarizes the measured current sharing error with the proposed DDS technique.

We use the set-up shown in Fig. 12 to verify the function of DDS circuit for the system application. Parameters and component values of the system are shown in Table II. In Fig. 13, the current difference between two supply modules can be improved from 12.5A to 2.9A when each module supplies 20A to the system. Owing to the large droop slope, the improved performance of current sharing is notable. Table IV summarizes the measured and the predicted current difference between two power modules with the proposed DDS technique. The error percentage of current sharing can be improved from 42.5% to 8.2%. However, if we use larger value of $C_a$, we can get better current sharing performance.

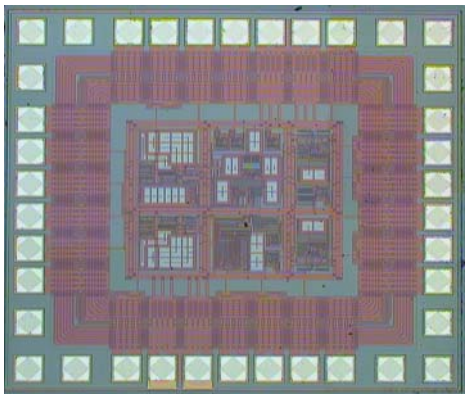

Fig. 9. Chip micrograph of current sharing controller with DDS technique.

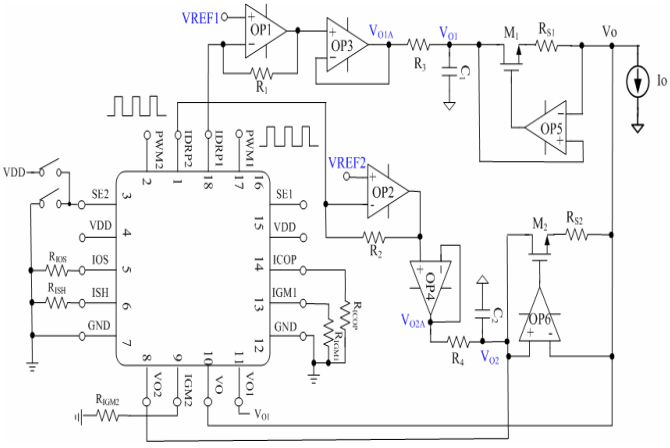


Fig. 10. A simple test circuit is used to verify the chip function.

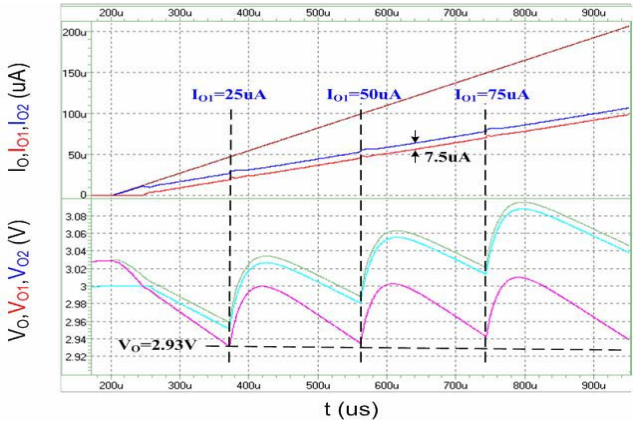


Fig. 11. Error current between two supply modules is limited within 7.5uA, which is 0.25 times of conventional droop method.

TABLE I: Error percentages of current sharing results by using the proposed DDS technique.

| $C_a$ | $I_{O1}$ (uA) | $I_{O2}$ (uA) | $I_{o,avg}$ (uA) | Error (%) | $I_{O1}$ | $I_{O2}$ | $I_{o,avg}$ (uA) | Error (%) |
|---|---|---|---|---|---|---|---|---|
| 0 | 49.8 | 20.1 | 34.95 | 42.5 | 100.1 | 70.4 | 85.25 | 17.4 |
| 1 | 50.0 | 34.9 | 42.45 | 17.8 | 100.1 | 84.7 | 92.4 | 8.3 |
| 2 | 49.8 | 39.8 | 44.8 | 11.2 | 100.2 | 89.8 | 95 | 5.6 |
| 3 | 50 | 42.4 | 46.2 | 8.2 | 100.2 | 92.2 | 96.2 | 4.1 |

## VI. CONCLUSIONS

A novel dynamic droop scaling technique uses dual current sensing loop to reduce the power dissipation on sensing resistor compared with conventional droop technique. Besides, DDS technique not only increases droop slope but also eliminates the selection of expensive and accurate external components. Furthermore, DDS technique uses incremental output voltage circuit to raise output voltage to meet the requirement of allowable minimum output voltage according to increment of load current. It means that the DDS can break through the limitation of conventional droop technique. The current difference between two supply modules can be shrunk from 12.5A to 2.9A. In other words, the error percentage of current sharing performance can be improved from 42.5% to 8.2%.

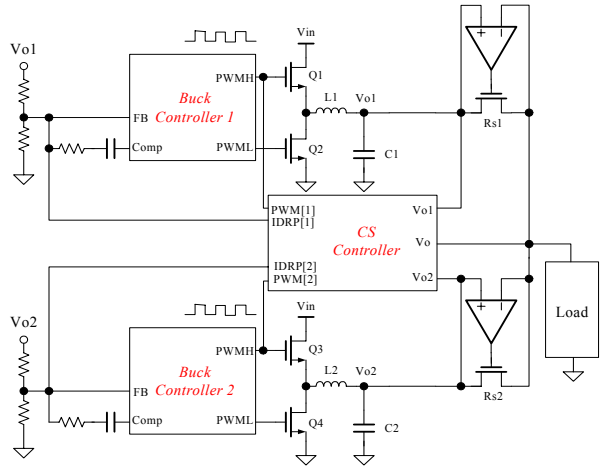


Fig. 12. The set-up of current sharing controller with DDS technique in two supply modules.

TABLE II: Operating parameters.

| Parameter | Value | Ttolerance |
|---|---|---|
| $V_{in}$ | 12V | |
| $V_{out}$@ no load | 3V | ±1% |
| $V_{out}$ | 3V | ±3% |
| Rated current | 20A | |
| Frequency | 100KHz | |

TABLE III: The values of components in DDS implementation.

| Parameter | value |
|---|---|
| L | 3uH |
| C | 8000uF |
| $R_{C,ESR}$ | 5m Ω |

TABLE IV: Measured and predicted current by DDS technique.

| $V_{O1(no\ load)}$-$V_{O2(no\ load)}$=60mV, $R_s$=5mΩ | | | |
|---|---|---|---|
| $C_a$ | $K_a$ | Prediction | Measurement |
| 0 | 5mΩ | 12A | 12.5A |
| 1 | 10mΩ | 6A | 6.5A |
| 2 | 15mΩ | 4A | 3.54A |
| 3 | 20mΩ | 3A | 2.9A |

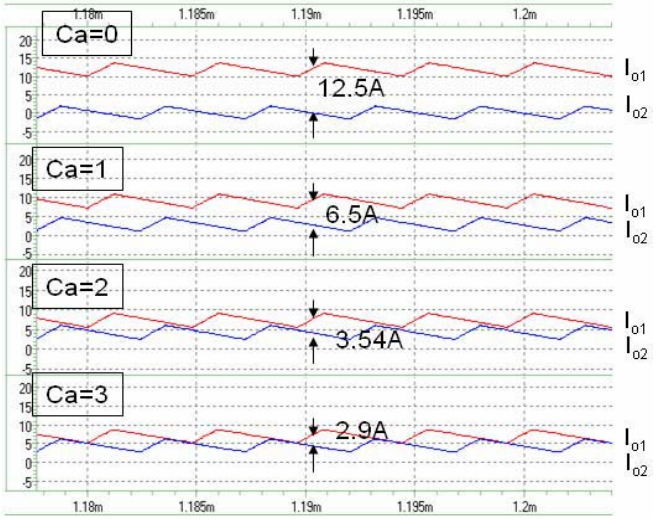


Fig. 13. Current difference between two supply module when DDS technique uses zero, one, two, or three raising division regions ($C_a$=0,1, 2, 3).

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