國立交通大學

材料科學與工程學研究所

碩士論文

# 使用 I-line 步進機與電子束微影並應用在 MHEMT 元件的新穎 T-形閘極製作方法之研究

**Study of Novel T-gate Fabrication Methods Using I-line Stepper and Electron Beam System with Application to MHEMT Devices**

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中華民國 九十四年八月

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本授權書所授權之學位論文，為本人於國立交通大學材料科學與工程系所乙組，九十四學年度第二學期取得碩士學位之論文。

論文題目：使用 I-line 步進機與電子束微影並應用在 MHEMT 元件的新穎 T-形閘極製作方法之研究

指導教授：張翼

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**中華民國　　94 年　9 月　7 日**

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國立交通大學材料科學與工程學系

## 摘要

本論文仲介紹了兩種嶄新的三五族半導體高頻元件的 T-型閘極製程方法。 第一個方法是利用 I-line 步進機加上位移的方法來縮小閘極線寬， 此方法可縮小線寬到其原先的二分之一甚或更小的尺寸。 在這個研究裡，我們成功的製作完成 0.2μm 與 0.3μm 大小的元件閘極長度。 利用這個新方法， 平均的誤差是±23nm 並且有 89%的誤差是在 45nm 之內。

第二個方法是利用電子束曝光系統來製作 T-型閘極。 我們利用了化學放大型光阻來取代傳統的閘極光阻 PMMA/PMMA-MAA。在本研究中,所能達到的最小元件閘極線寬為 127nm。 本次實驗使用含有銦含量為 0.55 的 MHEMT 元件來驗證這個新製程方法。 其中閘極長度為 0.25μm 的 MHEMT 元件其飽和電流為 360mA/mm，崩潰電壓為 5.1V， 以及其互導係數為 760mS/mm（當源極-汲極偏壓等於 1.5V 時）。 當與傳統閘極光阻 PMMA/PMMA-MAA 比較時，運用化學放大型光阻所需之曝光時間僅是其所需的 1/37 倍。

在本論文中所發展的兩種新穎閘極製程方法都可以達到高效率以及高良率。 此兩種製程方法都被推薦作為往後三五高頻元件的閘極提供了極佳的低成本高良率之製作方式。

# Study of Novel T-gate Fabrication Methods Using I-line Stepper and Electron Beam System with Application to MHEMT Devices

**Student: P. Y. Lin** **Advisor: Dr. Edward Y. Chang**

**Institute of Materials Science and Engineering**

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Two novel methods of fabricating T-gate for III-V semiconductor high frequency devices had been developed in this study. The first method used an I-line stepper and shifting mechanism to shrink the gate length to half or less of its original resolution. In this study, gates with gate length of 0.2μm and 0.3μm had been developed easily using I-line stepper. With this method, the average feature size error was only ±23nm and 89% of the error is less than 45nm.

For the second method, electron beam lithography system was used to develop T-shaped gate. Instead of PMMA/PMMA-MAA, the traditional resists for T-shaped gate fabrication, the chemical amplified resist was used to increase the throughput of gate processing. A MMEMT device with 0.55 indium content in the channel layer was used for demonstration. The smallest gate length we were able to achieve was 127nm. For a sample with a gate length of 0.25μm, the saturation drain current was 360mA/mm, the breakdown voltage was 5.1V and the transcondutance was 760mS/mm when the source-to-drain bias was 1.5V. Compared to PMMA/PMMA-MAA, the exposure time for chemical amplified resist was 37 times shorter.

The proposed new methods in this study both offer better efficiency and good reliability in gate pattern definition. They are recommended for future gate fabrication for III-V semiconductor high frequency devices.

# 致謝 (Acknowledgments)

2 years sounds like a long time but it past by like 2 minutes. It felt like only yesterday I was stepping into the campus of National Chiao Tung University for the first time, but today, I am getting my master degree. I am lucky to have the opportunity to enter and study in CSDLab, where I have met lost of interesting, friendly and kind people. In two years, I have made many friends.

The very first friend I made in NCTU is Calvin C. (張家源學長). I met him in the semiconductor fabrication class. First, I thought he was the teaching assistance, but later, I saw him sitting down beside me and starting to take notes. We later chatted and I learned that he was a first year Ph. D student who's taking the same class as I. Just like me, he was new to NCTU. We became very good friends and he helped me a lot with both school work and some small details of my daily life. Calvin has extensive knowledge about computers and electronics. I often wondered "hm…. maybe he's from a shopping channel or something". He's very good at helping and teaching people. I believe one day he'll become a great teacher. **Calvin! Thank you!**

The second friend I made in NCTU is Rainboy K. (郭建億學長). So why the strange name "Rainboy"? Because he believes that it's romantic to walk in the rain. HAHAHAHA weird ay. Anyway, I met him in front of meeting room before our weekly meeting. He was standing there looking out of the window trying to be cool for some reason. First, I thought he was not an easy going person. Maybe it's because the way he talks is always straightforward or maybe it's because he is always in a hurry. But I later discovered that he's an extremely hard working and reliable person. Rainboy later became my group leader. Under his leadership, I was able to graduate smoothly. Without Rainboy and Calvin's help, I am probably still in the fab. doing experiments right now. **Rainboy! Thank you!** (PS. The reason you are mentioned after Calvin is because I met him first. It is definitely not in the order of importance. Please don't kick my butt.)

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# Chapter 1

## *Introduction*

Communication is one of the key elements to our daily life. As technology advances, all types of communication technologies have transferred from wire to wireless. With the release of military channels, data and voice transfer through these bands has become possible. As the importance of wireless communication raises, communication quality and speed have turned into major issues; therefore, high frequency device is the key component for the realization nowadays of high-quality and high-data rate wireless communication system.

High frequency communication devices are usually made of compound semiconductors because compound semiconductors offer many advantages over Si devices. To be exact, GaAs (Gallium arsenide) is the most common compound semiconductor used for making high frequency devices. Compared to Si, GaAs devices have higher mobility and high saturated drift velocity; these advantages allow GaAs devices to operate at microwave frequency where Si devices could not function normally. In addition, a GaAs device is more radiation-tolerant than Si MOS devices. Many researches have been done on GaAs devices. Good reliability has been achieved and although expensive, it is not impossible anymore. Typical GaAs devices include MESFETs for analog and digital use, HEMTs (high electron mobility transistors) and HBTs (heterojunction bipolar transistors).[1]

In this study, the main focus is on using different approaches, different from traditional gate fabrication methods, of lithography to make T-shaped

gates for the high frequency device applications. In this study, MHEMTs had been fabricated using the proposed method. The device shows good electrical performances. The results demonstrate the possibilities of using these gate fabrication methods for high-frequency device fabrications.

# Chapter 2

*Literature Reviews*

## 2.1 HEMT

For a typical MESFET (Metal Semiconductor FET) structure, since the donor impurities are doped in the channel layer, impurity scattering in the channel layer will cause the mobility of electron to decay. For this reason, HEMT structure was invented to prevent electrons from decaying. HEMT is short for "High Eecton Mobility Transistor" and is also known as MODFET, "Modulation Doped FET" or HFET, "Heterostructure FET." Basically, the new structure uses materials with different band gaps to form a discontinuity of conduction band. Due to this energy band discontinuity, a quantum well is formed near the interface of the narrow band gap material. The electrons from the dopants in the wide band gap material will then drift into this quantum well. A thin layer of concentrated carriers is formed at the quantum well and this is called 2DEG, which will be discussed in more detail later. With this structure, the mobility of electrons can be improved greatly because of the lack of impurities in the channel layer. HEMT is short for "High Electron Mobility Transistor" and is also known as MODFET, "Modulation Doped FET" or HFET, "Heterostructure FET.[1]

From 30 to 300GHz is called the millimeter wave bands. Some important applications within these bands include broad band radio communications, high data rate fiber systems, automotive collision warning, passive imaging, concealed weapon detection, passive imaging systems

capable of seeing through rain, snow and fog, environmental, atmospheric and pollution monitoring systems. Most of these applications operate at the frequencies of around 100GHz or above. A large share of the market is focused on imaging and sensing; hence, noise performance of the devices is particularly important for this kind of application. For this reason, HEMT seems to be the best performer.[1]

Figure 2-1 is a cross section diagram of a typical III-V HEMT device. As seen from the figure, the current flows from the source to drain through the channel. This current is controlled by changing the voltage applied to the Schottky gate contact.[1]

## 2.2 MHEMT, PHEMT and InP HEMT

Conventional HEMT structure is consisted of AlGaAs/GaAs based heterjunction. When the amount of Al increases, the band gap discontinuity will increase and the confinement of electrons in the channel will improve. However, if the Al content is higher than 20%, an effect called the DX center phenomenon will occur. A DX center will trap electrons and will lower electrical performance. In order to increase electron mobility, the DX center phenomenon must be avoided. To avoid this phenomenon, a HEMT with AlGaAs/InGaAs structure was introduced. Electron mobility increases as indium content in $In_xGa_{1-x}As$ increases. An AlGaAs/InGaAs/GaAs pseudomorphic structure was developed to allow high indium content in the channel layer. Because the lattice mismatch between InGaAs and AlGaAs is large when In content is increasing, pseudomorphic structure is hard to control. In addition, the thickness of the channel is limited to avoid formation of

dislocation. This kind of pseudomorphic structure HEMT is usually short for "PHEMT".

For higher In content in the channel layer, InP based HEMT was introduced. The In content of InGaAs channel layer of an InP-based HEMT is typically in the range of 53-80%. InP-based HEMTs had been demonstrated to achieve higher $f_T$ and $f_{max}$ than GaAs-based PHEMTs. However, InP HEMT is still not very popular due to its high cost, size limitation, fragility, and difficulty of back-side process.

As epitaxial technology advances, composition graded InAlAs buffer is used to accommodate lattice mismatch of high In-content InGaAs channel and GaAs substrate. This kind of structure is called a metamorphic HEMT or MHEMT.

MHEMT and InP-based HEMT shared similar properties like low noise, high power, high linearity and low DC power consumption. Compared to InP-based HEMT, MHEMT is lower in cost, has higher thermal resistance and is easier to handle since it is less fragile. Therefore, in this study, MHEMT will be the main focus.

## 2.3 Characteristics of a HEMT device

In this section of the report, several important characteristics that determine the performance of a HEMT device will be introduced. They are transconductance, $f_T$ and $f_{max}$.

### 2.3.1 Transconductance, $g_m$

The transconductance, $g_m$, is a very significant factor of determining the quality of a device. $g_m$ is a measure of the efficiency of the channel current control, which means the amount of channel current change for a given gate voltage change. It is the ability of gate voltage on controlling drain current. To improve the efficiency ($g_m$), often, a well controlled recess geometry is necessary.

The transconductance of a device is defined as the slope of the $I_{DS}$-$V_g$ characteristics with the drain-source voltage held constant. The mathematical representation of it is

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{\varepsilon_2}{d_2} Z_G v_{sat} \Big|_{V_{DS}=constant} \quad (1)$$

where $v_{sat}$ is the electron velocity of the two dimensional electron gas (2DEG).[3]

The transonductance of a device is easily obtained by measurement. It is one of the most important indicators of device quality for microwave and millimeter wave applications. When all other characteristics are equal, a device with higher transconductance will provide greater gains and superior

high-frequency performance.

To measure $g_m$, initial gate voltage, gate voltage step, and drain voltage at which the measurement is done must be specified first. The source-drain current is a function of gate voltage and is nonlinear; therefore, $g_m$ generally becomes less as pinch-off bias is approached. That is to say, smaller voltage step will give higher transconductance. In addition, $g_m$ is closely related to the gate length and the channel material used.

### 2.3.2 Unit Current Gain Cutoff Frequency, $f_T$

The $f_T$ of a device is the frequency at which the short circuit current gain becomes unity. $f_T$ is defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2}$$

, and the $(C_{gs} + C_{gd})$ is the total capacitance related to the Schottky gate contact. From this relation, we could see that in order to achieve high $f_T$, large $g_m$ and small total gate capacitance must be achieved. Small total gate capacitance is accomplished by short gate length; for millimeter-wave applications the gate length is usually smaller than 0.15μm. In this equation

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat} \varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G} \tag{3}$$

the $L_G$ is the is the gate length; therefore, the shorter the gate length the higher the $f_T$ and higher the $g_m$.[3]

### 2.3.3 Maximum Frequency of Oscillation, $f_{max}$

Another important parameter is $f_{max}$, which is the frequency where the power gain falls to unity. $f_{max}$ is expressed as

$$f_{\max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right)^{\frac{1}{2}}} \tag{4}$$

This expression shows that to obtain useful power gain at high frequency, the $f_T$ of a device must be large; in addition, the resistances of gate, source and drain must be small.[3]

A typical HEMT device structure is consisted of a doped AlGaAs layer next to an undoped GaAs layer. One of the major elements that determine the mobility of electrons in GaAs is impurity. Impurity scattering will lower the mobility of electrons; therefore, it is preferred that electrons flow through the undoped GaAs layer. With a doped AlGaAs layer, the electrons are supplied from this AlGaAs layer, but the actual flow happens in the adjacent undoped GaAs layer. This phenomenon is possible because the band-gap discontinuity between the two layers allows the electrons to stay in GaAs layer, see Figure 2-2. Since the electrons are electrostatically constrained to stay close to the donor atoms, electrons tend to stay close to the boundary between GaAs and AlGaAs. This phenomenon is known as the two-dimensional electron gas or 2DEG.

# Chapter 3

## *Device Fabrication*

As shown in Figure 3-1, basically, the fabrication process flow can be break into six parts: mesa isolation; ohmic contact making; T-shaped gate making; gate recess; passivation and contact via hole; air bridge.

## 3.1 Wafer Cleaning

Before any fabrication step, every wafer must go through the cleaning procedure. Every wafer was immersed in ACE for 5 minutes, and then followed by 5 minutes in IPA to remove contamination from the wafer surface. After, the wafer was blown dry using nitrogen.

## 3.2 Mesa Isolation

As the name suggested, mesa isolation is to isolated devices from each other. A mesa isolation can force the current to flow under the gate metal from source to drain. This is very important because if the some of the current flow between source and drain without passing under the gate metal, the current will become a parasitic resistance, which can degrade the RF performance of the device.

The active region is defined by mesa isolation. In addition, parasitic capacitance, parasitic resistance, leakage current and back-gating effect can all be reduced with effective isolation. A successful isolation provides sufficient insulating area to form passive elements such as transmission lines, capacitors,

pads, etc.

Typically, etching, ion bombardment isolation and selective implantation are the three methods of achieving mesa isolation. Among these three methods, mesa etching is the simplest one. First, the mesa pattern was defined by photolithography. The mesa was etched using phosphoric solution; later, the depth was measured using α-step. For this study, the ideal depth is around 3000Å. In addition, the etched profile could be checked with SEM (scanning electron microscopy).

## 3.3 Ohmic Contact

The purpose of an ohmic contact on semiconductor is to allow the electrical current to flow in and out of the semiconductor. It is a low resistance junction formed between metal and semiconductor interface. An ohmic contact should obey the ohms law; in another word, it should have a linear I-V characteristic either under forward or reverse bias. Ohmic contact is very important because a successful one can lead to better device performance. With lower contact resistance, power consumption will decrease. In order to create a low resistance ohmic contact, the metal-semiconductor interface region should be heavily doped. In addition, an ohmic contact should be stable over time and temperature and should have as little resistance as possible.

The pattern of the ohmic contact with an undercut profile was defined using photolithography method. After, the sample was send to $O_2$ plasma descum to remove residual photoresist and dipped into HCl solution to remove

oxide. Finally, an e-gun evaporation system was used to deposit Au/Ge/Ni/Au onto the sample. After ohmic formation, the contact resistance was measured by TLM (transmission line method).

The purpose of the germanium in the ohmic metal is for GaAs doping during alloy. The nickel is like a wetting agent which prevents the AuGe metal from "balling up" during alloy. The Au/Ge alloy is commonly used because it forms low contact resistance ohmic and has good reliability.

## 3.4 T-Shaped Gate

Schottky barrier gate is one of the most important elements in a GaAs device. Both the dimension length and placement of the gate are very critical.

A gate opening was defined between the source and the drain using lithographic techniques. In this step, electron beam lithography system is commonly used because an e-beam system allows high resolution, excellent registration, and can automatically generate undercut resist profile for the ease of lift-off.

After the gate open had been defined on resist, recess was to be performed. Usually, wet etching was used for this task; although dry etching could also be used, it tends to cause ion bombardment damage that degrades the device performance. A recessed gate offers several advantages. First of all, when the gate is placed under the surface depletion of surrounding material,

the surface depletion will not be able to restrict the current flow during forward gate bias. Secondly, when the channel is thinner, the breakdown is increased. Finally, gate recess can increase the breakdown and reduce source-gate resistance.

Citric acid (C.A.) based solution was used during recess process to etch the cap layer. After, HCl solution was used to etch the schottky layer until the target current was reached.

Gate length is a crucial parameter of determining the performance of a device. Shorter gate can give higher gain and lower noise; in addition, high frequency devices depend greatly on short gates. However, there is one problem with short gate and that is the raise in gate resistance due to the reduction in cross-sectional area of the gate. A major solution for this problem is a T-shaped gate. This kind of gate will have a large cross-sectional area at top while maintaining a remaining a short gate length that is contacting the wafer.

To fabricate a T-shaped gate, a dual layers photoresist technique can be used. Traditionally, the bottom layer is poly methyl methacrylate (PMMA) and the top layer is copolymer (PMMA-MAA). Since the sensitivity of copolymer is higher than PMMA, the opening for copolymer will be greater than that of the PMMA; therefore, a T-shaped gate can be formed. This dual layer process will be discussed in more detail later on.

In this study, instead of the traditional PMMA and PMMA-MAA, chemical amplified resist was used as the e-beam resist. Conventionally,

chemical amplified resist is used for deep UV lithography due to its high sensitivity. High sensitivity is not the only advantage of a chemical amplified resist. The exposed and unexposed areas have solubility with great difference; therefore, resolution is high.

## 3.5 Passivation and Contact Via

An III-V device can easily be affected by surface conditions especially at the gate area. As the size of gate shrinks, particles and contaminations can easily damage a device. Passivation can protect the device from these damages during handling, processing and data measuring. The material used for passivation is usually $SiN_x$. In this research, the passivation layer was grown by PECVD and the precursors used are $SiH_4$/Ar, $NH_3$, and $N_2$.

After passivation, via holes was formed using photolithographic method and etched using RIE. The via holes were opened at source and drain areas for interconnects. The gases used for $SiN_x$ etching was $CF_4$ and $O_2$.

## 3.6 Air Bridge

In order for source, drain and gate to be on the same plane, there will be places where the gate will cross either drain or source since eventually all the gates must be connected. However, when gate and drain are in contact, parasitic capacitance will be formed and cause problems during operation. Therefore, usually, the gate only crosses with source. A bridge suspended in the air over the gate is used to connect the sources. There is nothing but air between the source and the gate; hence, it is called an air bridge, see Figure 3-2. Having air in between has several advantages. Air has a very low

dielectric constant, with air the parasitic capacitance can be low and can carry substantial current.

Photolithography and electro plating are the two major steps in air bridge formation. After the first layer pattern was defined using photolithography, Ti/Au/Ti was been deposited on the wafer. Then second layer pattern was formed using photolithography. Finally, the air bridge metal, gold in this case, was electro-platted. After gold had been electro-platted, the photoresist and Ti/Au/Ti layer were removed separately; the only remaining was the electro-platted air bridge.

Gold is usually the material used for air bridge. Gold has many advantages: high conductivity, inert to oxidation and acidic environment, ductile, good formability etc. Since the adhesion between gold and the wafer surface is poor, a thin layer of titanium is usually deposited. By doing so, the adhesion can be improved.

Air bridge is the last step for the front-side process. After finishing this last step, RF characteristics of the device can be measured.

# Chapter 4

## *Novel Gate Fabrication Methods*

Before introducing the new methods of gate fabrication, let us take a look at the traditional ones. In this section, two traditional methods of gate fabrication will be introduced first, and two novel methods proposed in this study will be presented.

## 4.1 Dual Layer Process

One of the most common traditional methods of gate fabrication is the dual layer process. Two resists, poly methyl mthacrylate (PMMA) and copolymer (PMMA-MAA), were used. Figure 4-1 is a schematic illustration of the dual layer process. Using a spin coater, two layers of resists would be spun on with PMMA-MAA on the top and PMMA on the bottom. Because the sensitivity of PMMA-MAA is higher than that of the PMMA, under the same exposure, the resulting feature size after development of PMMA-MAA will be larger compare to PMMA. Therefore, PMMA-MAA is used for fabricating the head of the T-shaped gate while PMMA is used for fabricating the foot of the T-shaped gate.

One advantage with the dual layer process is only one exposure is required for T-shaped gate fabrication. All the other methods that will be introduced later required at least two exposures to fabricate a T-shaped gate. However, there is one problem with the dual layer process. With this method, there may be no effective undercut profile; hence, after metal deposition, lift-off will be more difficult.

## 4.2 Modified Dual Layer Process

As mentioned in the previous section, the dual layer process may not produce an effective undercut profile to aid the metal lift-off. As a result, a modified dual layer process with improved undercut profile was introduced.

Figure 4-2 shows the flowchart of the modified dual layer process. First, a layer of nitride was grown using PECVD. PMMA was then coated on with a spin coater. After exposure with electron beam system and development, this footprint pattern was transferred to the nitride using ICP etcher. Later, PMMA and PMMA-MAA was coated on with a spin coater. However, this time, PMMA was on the top and PMMA-MAA was on the bottom. Like mentioned before, PMMA-MAA has higher sensitivity than PMMA; therefore, under same exposure, the feature size will be greater. As shown in Figure 4-2f), after the second exposure and development, an undercut profile was formed because the placement of PMMA-MAA and PMMA was reversed.

Using this method, an undercut profile was formed, which made metal lift-off easier. However, two exposures were required to make a T-shaped gate and a nitride layer needed to be grown beforehand.

## 4.3 Gate Fabrication Using I-line Stepper

In this study, we did a demonstration using Si wafer instead of GaAs wafer. Figure 4-3 is the flow chart of the gate fabrication with I-line Stepper. First, a layer of $SiN_x$ was grown on the wafer using PECVD. Later, after the coating of photoresist, I-line stepper was used to define the first pattern, which

was a series of single lines parallel to each other. After exposure and development, the nitride was etched using a transfer couple plasma etcher. The same mask was used to define the second pattern. The mask would first be aligned with the first pattern on the wafer but immediately after the alignment, the chuck along with the wafer would shift. Followed exposure and development, E-gun evaporator was used to fill the space with gate metal and then lift-off. The result was a γ-shaped gate. Though a γ-shaped gate is different from a T-shaped gate, it still offers a head with large cross-section area and a small foot in contact with substrate.

### 4.3.1 Alignment Mechanism

The alignment mechanism will now be discussed. Figure 4-4 is a typical alignment mark for a stepper. This kind of stepper alignment mark is called a grating. If one looked from the top, the grating is a series of lines lining up parallel to each other, which looks a bar code. On the other hand, viewing from the side, it looked like a series of islands lining up side by side with equal spacing.

During alignment, a beam of He-Ne laser would first scan over the grating. Since the height between the bar and the surface is different, the intensity of the reflected laser beam would be different as well. In addition, since the width of the bar and the space in between the bars are known, the stepper can analyze the reflected light and locate the center of the grating efficiently.

He-Ne laser is not the only light source for alignment; however, it is the most accurate one. Compare to other broad band light source, the output of

laser is more coherent and is consisted of a single wavelength. When scanning the grating, signals of reflected beams are sharper when the source used is laser. Therefore, more accurate result is achieved using He-Ne laser as the light source for alignment.

As shown in Figure 4-5, gratings are located both on the x- and y-axis. Imaging there are lines extending from the center of both grating as shown in Figure 4-5. The intersection of these two lines is a preset point. Assume that this preset point is at the center of the reticle. Using the grating system, the stepper can quickly align a mask with a wafer.

### 4.3.2 Shifting Mechanism

Having explained the I-line stepper alignment mechanism, we may go on and discuss the actual shifting mechanism used for gate fabrication. Seeing the first layer of pattern did not require alignment, we will start the discussion with definition of second pattern. Now, assume the first pattern was defined, nitride was etched and photoresist had been removed. The mask used for second pattern is exactly the same as the one used in the first pattern. As Figure 4-6 shows, when a sample entered the stepper, using the grating system, the stepper would first align the mask with the wafer. After alignment, the chuck would shift to a distance we chose. As indicated in Figure 4-7, x is the distance of the shift. In this study, the mask used is shown in Figure 4-8. The pattern on the mask is basically a series of lines lining parallel to each other. The widths of the line and space between the lines are both 0.4μm. In other words, this mask is a 1:1 mask. Therefore, in this study, since the gap between lines is 0.4μm, the resulting line width can be calculated using

$$l_w = 0.4 - x \tag{5}$$

$l_w$ = line width

x = distance shifted

This equation only works in this case. When other masks are used, this equation will not be useful. However, simply replace the 0.4 in the equation with y, an arbitrary number that is equal to the feature size of the mask itself.

## 4.4 Gate Fabrication Using Electron Beam Lithography System with Chemical Amplified Resist

CA photoresist is very sensitive; therefore the thickness, baking temperature, storing condition and exposure dosage must be carefully controlled. In this study, DSE 1010 CA photoresist was used. This resist can be used for the fabricating of both foot and head of the T-shaped gate.

### 4.4.1 Chemical Amplified Resist

The first chemical amplified (CA) resist was developed in 1980s by IBM to manufacture DRAMs using DUV lithography. CA resist is formulated to react at an accelerated rate based on an acid-catalyzed reaction. Increasing the sensitivity of the photoresist is possible with the help of a sensitizer known as the *photoacid generator* (PAG). During exposure, the PAG in the photoresist will produce an acid only in the exposed area.

Although many researches have been done on finding new CA resists, the basic principle is still the same. Every CA resist will have a chemical protecting group which makes the resist insoluble to aqueous solution. The acid created during exposure will undergo a catalyst reaction during

post-exposure bake step which removes the protecting group and makes the resist highly soluble in aqueous solution. This mechanism is called deprotection.

With traditional photoresist, one photon only causes one or less chemical reaction. For example, if 100 photons only create 30 chemical reactions, the quantum yield is said to be 0.3.

When a photon creates a PAG, this PAG will then undergo deprotection. After deprotection, a new PAG is released and this new PAG will again undergo deprotection. Hence, deprotection mechanism and formation of new PAG will keep on going until oxygen or other contaminations consume all the PAGs and eventually lead to termination, the seize of entire reaction. More than 800 reactions from just one photon can often be seen. This is why CA resist has high sensitivity.

Lithography systems such as the electron beam lithography system are very expensive. Thus, with the high sensitivity of CA resists, exposure time can be shortened, which means shorter operation time. With operation time shortened, lifetime of the equipment can be prolonged, less energy is required and production rate is higher

In this study, the chemical amplified resist used is DSE1010. DSE 1010 CA photoresist was developed by DONGJIN, a Korean company. The developer for DSE 1010 is called FHD-5 which was developed by Fujifilm.

### 4.4.2 Gate Fabrication Using Chemical Amplified Photoresist

Refer to Figure 4-9, after finished ohmic contact, a layer of nitride was grown on the sample using PECVD. Thereon, chemical amplified photoresist was coated on the wafer using a spin coater. For gate foot definition, the initial revolution was 1000 rpm for 10 seconds and the final revolution was at 7000 rpm for 30 seconds. After coating, soft baked the sample for 10 minutes at 95°C. Next, the sample was sent into the electron beam lithography system for footprint definition. Post baked for 2 minutes at 115°C and the sample was ready for development. The sample was then developed for 105 seconds, and finally, hard baked at 115°C for 1 minute.

Since, only one resist was used, before defining the gate head, nitride must be etched to form the pattern of the foot. After the gate foot was defined, the nitride below the resist was etched using ICP, inductive couple plasma. Head definition procedures were exactly the same as foot definition except for part of coating resist, the initial revolution was still 1000 rpm for 10 seconds but the final revolution was lowered to 4500 rpm for 30 seconds.

Recess etching immediately followed head definition. After recess, gate metal, Ti/Pt/Au, was deposited using e-gun evaporator system. Thereafter, lift-off was done to finish the T-shaped gate.

Typically, the dosage required for dual layer process with PMMA/PMMA-MAA was around 2100 $\mu C/cm^2$. On the other hand, with CA resist, only ~50 $\mu C/cm^2$ and ~300 $\mu C/cm^2$ was required for foot and head of a gate respectively. It is clear that CA resist required less energy and therefore, exposure time was shorter compared to that of the dual layer process. The total amount time of a sample spent in the electron beam system for gate

definition was less than 2 hours. Compared to the dual layer process which usually took 4 or more hours, this CA resist method was much faster.

# Chapter 5

## *Measurements*

Several measurements had been done in between and after the MHEMT device fabrication. Basically, only by these measurements can we know whether a device is functioning normally and performance according to our initial goal. Measurements can be divided into two portions, DC and RF measurements. DC measurements were performed to obtain I-V curves, break-down voltage, pinch-off voltage, transconductance and contact properties. On the other hand, RF measurements include scattering parameters (S-parameters).

## 5.1 DC Measurements

### 5.1.1 IV-Curve

HP4142B and Karl Suss semi-automatic probe system were used to measure the IV-curves of the MHEMT devices. Total of three probes contacting source, drain and gate were used. The source electrode was grounded, the gate electrode was applied with negative voltage and the drain electrode was applied with positive voltage.

In this study, voltage between 0 to 1.5V was applied to drain-to-source and the voltage applied to the gate was between 0 to -1V.

### 5.1.2 Pinch Off Voltage

Pinch off voltage were measured using HP4142B and Karl Suss semi-automatic probe system. In order to measure the pinch off voltage, the source-to-drain voltage must be kept constant; then, slowly increased the voltage applied to gate to decrease the source-to-drain current till pinch-off.

### 5.1.3 Breakdown Voltage

Breakdown voltage was also measured using HP4142B and Karl Suss semi-automatic probe system. In this study, the breakdown voltage is said to be the gate-to-drain voltage when gate-to-drain current is 1mA/mm. During measurement, the source pad was not in contact with any probe during breakdown voltage measurement. In addition, the gate was grounded and the drain was applied with a positive bias. The gate-to-drain bias was slowly applied and adjusted to find the breakdown voltage which occurred when gate-to-drain current reached 1mA/mm. It is important that the gate-to-drain current does not go over too high or the device will be burnt.

### 5.1.4 Extrinsic Transconductance ($g_m$)

HP4142B and Karl Suss semi-automatic probe system can also be used to measure $g_m$. Gate bias was varied till the peak $g_m$ was obtained while the source-to-drain bias was kept constant. In this study, the applied source-to-drain voltage was 1.5V and the applied gate voltage was between -1.2V and 1V. Finally, the $g_m$ was calculated by differentiating Id and $V_{gs}$.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{6}$$

## 5.2 RF Measurements

### 5.2.1 Scattering Parameters (S-Parameters)

Scattering parameter or S-parameter is one of the major properties of microwave measurement. Although Y and Z parameters can also be used to describe the microwave performance, in the study, only the S-parameter will be discussed. Usually, the S-parameter is measured by VNA. Using S-parameter, $f_T$ and $f_{max}$ can be calculated.[4]

Basically, the performance of a microwave device is determined by the S-parameters. The S-parameters are defined in Figure 5-1. In this figure,

a1 is the electic field of the microwave signal entering the component input.

b1 is the electric field of the microwave signal leaving the component input.

b2 is the electric field of the microwave signal leaving the component output.

a2 is the electric field of the microwave signal entering the component

output.

# Chapter 6

*Results and Discussions*

In this study, the main focus is on methods of gate fabrication using electron beam system and I-line stepper. This chapter will be divided into two parts showing the results from electron beam system and I-line stepper.

## 6.1 I-Line Stepper

One of the major issues with gate fabrication with an I-line stepper is scattering effect. As shown in Figure 6-1, during 2nd exposure, when light hits the edge of the nitride layer, light will be scattered in random directions. These scattered beams of light will hit the photoresist in all directions even sideways. The outcome is the amount of exposure at different places will be different, and the result is shown in Figure 6-2b where the side of the photoresist is not smooth. The surfaces of the walls are wave-like. Furthermore, when the light hit the plane surface of either nitride or substrate, it will be reflected. Due to the height difference between nitride and the wafer, the reflected light beams caused by the plane surfaces are different in intensity. With reflected light beams of different intensities, the amount of exposure experienced by the resist over the nitride and substrate are different. Since the behavior of light is very complex and is not the focus of this study, there will be no further discussion about it. However, because of the complex behavior of light, carefully tuned dosage becomes very crucial.

Figure 6-2a is a SEM picture of a successful 0.2μm shifted sample. The area circled by the red lines is the nitride and the area within the yellow lines is

the photoresist of the 2nd layer. Originally, the trench was 0.4 micron, but after the shifting technique, the trench shrunk to 0.2 micron, half the original size, see Figure 6-2b. As mentioned in the previous paragraph, in Figure 6-2b, the walls of the photoresist are not even. This is due to the scattering of the light beams. However, with the correct dosage from I-line stepper, this problem can be minimized. When the optimum dosage is used the result, will be like that shown in Figure 6-3. In Figure 6-3, there is almost no sign of the uneven walls caused by the scattering of light.

In this study, the required dosage for 1st layer pattern was around 1650 J/m$^2$ for all different shifts. For 0.2μm shift, the dosage for the second layer pattern was approximately 2500J/m$^2$. This condition was only suitable for samples with 0.2μm shift. For other shifts, the required dosage of the 2nd layer pattern would be different. Different shift would require different exposure dosage because, as mentioned before, the height difference between nitride and substrate would cause the amount of exposure experienced by the resist to be different. Therefore, every different shift requires an optimum dosage of its own.

As mentioned previously, the advantages of using I-line stepper for gate fabrication include high throughput, high accuracy, high reliability and lower cost than electron beam lithography. Another major advantage is that the amount of shifting can be changed to any value desired. In another word, any gate length within the machine's capability can be achieved. The result of 0.2 micron shift has already been shown previously. In Figure 6-4, a sample with 0.1 μm shift had been demonstrated.

After the desired trench had been made, Ti/Pt/Au was deposited. Immediately after metal deposit on was metal lift-off. Figure 6-5 is a SEM picture of a metal gate for a 0.2 micron shift sample after metal lift-off.

### 6.1.1 Statistic Analysis

To achieve high throughput, reliability is very important. To prove that this method is reliable and accurate, we used 18 dies all with 0.2 micron shift. Analyzing these dies by statistical analysis, we were able to calculate the amount of error and the accuracy of this study.

According to Canon, the FPA 3000 i5+ has a 3σ of 45nm. In statistics, this means that 95% of the errors are within 45nm. Refer to Figure 6-6, there are 18 bars each represents one reticle and its final gate length. The dash red line indicates the ideal gate length, 0.2μm. Table 6-1 shows the actual gate lengths and errors. The average feature size error is ±23nm. In the 18 dies we analyzed, 16 dies have errors smaller than 45nm. This means that 89% are within 45nm of error, which is not as Canon suggested, 95%. However, not all errors were caused by the stepper alone. The dry etcher and SEM measurement could also be other sources of error.

The final line width was determined by SEM. In the SEM computer there is a built-in virtual ruler, which is used for measuring distances between two points of a SEM image. User simply clicks on a computer mouse to control the ruler and measure the desired distance. Hence, human error is introduced using this method of measuring line width. In another word, if the distance between two points were measured 10 times, the results may not be

consistent.

Figure 6-7 is a simple schematic drawing of a SEM stage. As shown in the figure, when trying to take SEM cross-section picture of a sample, the sample is taped inside the slot. However, as shown in Figure 6-7b, if the sample was taped at an angle to the horizontal, the resulting dimension would be inaccurate. This is the reason why SEM could be a source of error.

Other than stepper and SEM, another source of error was the TCP plasma etcher. This etcher was used for nitride etching; in another word, pattern was transferred to the nitride film. After etching, throughout the wafer, the widths of the trenches were not consistent; instead, some would be wider while others would be narrower. This may be caused by two reasons. First of all, the plasma etcher itself might cause the uneven trench dimension. Secondly, the problem might be caused by uneven thickness of the nitride film. Because of the dimension difference between the trenches of the first pattern, when the second pattern was defined, the resulting foot-print dimensions would be inconsistent. The outcome of the statistical analysis was hence affected.

So far, we had explained that not all the errors were due to the I-line stepper. SEM and TCP plasma etcher were other two major sources of error. If we could limit the source of error to I-line stepper only, the outcome should be closer to the $3\sigma$ value suggested by Canon. In order to achieve this goal, we offer several solutions. For one thing, instead of PECVD, HDPCVD (High Density Plasma CVD) could be used for growing nitride to achieve higher uniformity of the film. Combine the more uniform film with a better plasma dry etcher could ensure higher consistency of the dimension of the

trenches. Furthermore, if a SEM with higher definition is used, the result should be more accurate.

### 6.1.2 Future Study of Gate Fabrication Using I-line Stepper

In this study, the new method of gate fabrication using an I-line stepper had been demonstrated on a Si wafer only. Later on, it will be demonstrated on a real III-V semiconductor high frequency device. At this point, the effect of a γ-shaped gate with uneven head on a real device is still unknown.

## 6.2 Electron Beam Lithography System

As mentioned before, chemical amplified resist can be used for fabricating both foot and head of a T-shaped gate by simply varying the dosage. Figure 6-8a is a SEM picture that shows the foot of the T-shaped gate using a lower dosage. Figure 6-8b is a SEM picture showing the head of the T-shaped gate using a higher dosage.

After the T-shaped gate was fabricated, DC characteristics of the devices were measured. In this section, I-V characteristics, breakdown voltage, transconductance, as well as relationship between footprint length vs. dosage, will be shown and discussed.

### 6.2.1 I-V Characteristics

Figure 6-9 is the I-V curve of the MHEMT device with In content of 0.55 in the channel layer fabricated with the chemical amplified photoresist and gate length of 0.25μm. The saturation drain current ($I_{DSS}$) is 450 mA/mm at $V_D$ = 1.5V and $V_{pinchoff}$ = 2V.

### 6.2.2 Breakdown Voltage

Reliability of a device greatly depends on the breakdown voltage. In this study, the breakdown voltage was defined as the drain-gate voltage when drain-current reaches 1mA/mm.

Figure 6-10 is a graph of $V_{DG}$ vs. $I_{DG}$. The graph indicates that the breakdown voltage is 5.1V.

### 6.2.3 Transconductance, $g_m$

As mentioned previously, $g_m$ is the ability of gate voltage on controlling the drain current. It is defined by this equation,

$$g_m = \frac{dI_D}{dV_G} = \frac{\varepsilon_2}{d_2} Z_G v_{sat} \tag{7}$$

which was mentioned previously. Refer to Figure 6-11, in this study, the applied darin-to-source bias was 1.5V and the resulting $g_m$ was 760 mS/mm. The gate length in this case was around 0.25μm. The results are comparable to the results reported in [11], in which a MHEMT device (In = 0.67 in InGaAs channel) with a 0.25μm gate , when applied with a 1.5V source-to-drain bias, $g_m$ is around 773 mS/mm.[11] It must be noted that the higher $g_m$ from the publication was due to its higher In content. Higher In content gives higher electron saturation velocity, and from the equation, $g_m$ is proportional to $v_{sat}$. However, the reason why this MHEMT device was chosen for comparison was the gate length and source-to-drain bias was exactly the same as that of this study. Therefore, it helps to prove that CA resist is indeed more than capable for fabricating T-shaped gate of III-V high frequency devices.

### 6.2.4 Dosage vs. Footprint Length for CA Resist

The relationship between dosage and footprint length is simply that the greater the dosage, the larger the footprint length. In this study, we had tested the CA resist with dosage range from 35 to 60μC/cm$^2$. Figure 6-12 shows the result we obtained. When the dosage was 35μC/cm$^2$, the footprint length was around 127nm, and when the dosage was 60μC/cm$^2$, the footprint was around 214nm. The result is linear.

### 6.2.5 Dosage vs. Tee-Top Length for CA Resist

Using the same CA resist, the head of a T-shaped gate can be made as well. Figure 6-13 shows the relationship between dosage and the feature size of the tee-top. As one can see, the result is linear. We tested three dosages between 230 and 320μC/cm$^2$. At 230μC/cm$^2$ the tee-top length was 530nm and at 320μC/cm$^2$ the tee-top length was around 990nm.

### 6.2.6 Dosage vs. Footprint Length for PMMA

For comparison purpose, we also tried to find the relationship between dosage and footprint length for PMMA/PMMA-MAA. Figure 6-14 shows this relationship. We tested with dosages from 1600 to 2000μC/cm$^2$. At 1600μC/cm$^2$, the footprint length was around 170nm and at 2000μC/cm$^2$, the footprint length was around 260nm. Please note that in this case, the process used was the modified dual layer process. The reason why we chose this process for comparison was because like the CA resist fabrication process, nitride layer was required and two exposures are required.

### 6.2.7 Comparison between CA Resist and PMMA/PMMA-MAA

Table 6-2 is a table comparing dosage/footprint between CA resist and PMMA/PMMA-MAA. Same footprint length can be achieved using these two different types of resists; however, the difference between dosages is significant.

Coulomb, C, is related to time and is defined by the following relation,

$$C = A \bullet s \tag{8}$$

where A (ampere) is the current, and s (second) is the time. Because the beam current of the electron beam system is fixed, higher dosage means longer exposure time. This proves that using CA resist for T-shaped gate fabrication is more efficient than using PMMA. Take footprint length 170nm for example, if PMMA were used, the required dosage was 1600 μC/cm$^2$. On the other hand, if CA resist were used, the required dosage was only 46μC/cm$^2$. In this case, it means that the required exposure time of PMMA was 35× longer than that of the CA resist.

# Chapter 7

## *Conclusions*

In this study, two novel methods for the submicron gate fabrication have been introduced. We had successfully demonstrated gate fabrication using an I-line stepper on a silicon substrate. Using the stage shifting mechanism, we were able to shrink the gate length to more than half the size of the original pattern. In this study, we had demonstrated γ-shaped gates with gate length equal to 0.2 and 0.3μm. In addition, we had shown that 89% of the errors are within 45nm and the average error is 23nm, which made this method of gate fabrication very reliable. Metal was also successfully deposited and lifted-off to form a T-gate.

Another method which had been introduced was to fabricate T-shaped gate with electron beam lithography system and the chemical amplified resist. We had demonstrated that using chemical amplified photoresist to fabricate gate was more efficient than using PMMA/PMMA-MAA. The required exposure time of PMMA/PMMA-MAA was 35× longer than that of the chemical amplified resist. A MHEMT device with 0.55 of In content in the channel was also used to demonstrate this method. The gate length for this device was around 0.25μm and the saturation drain current was 360mA/mm. Furthermore, the breakdown voltage was around 5.1V. Furthermore, the measured transconductance, $g_m$, was 760mS/mm which was comparable to other MHEMT devices with the same gate length

In conclusion, the two novel methods proposed in this study both showed better efficiency than the traditional methods. Both methods are reliable for

fabricating submicron T-shaped gate for III-V semiconductor high frequency devices for wireless applications.

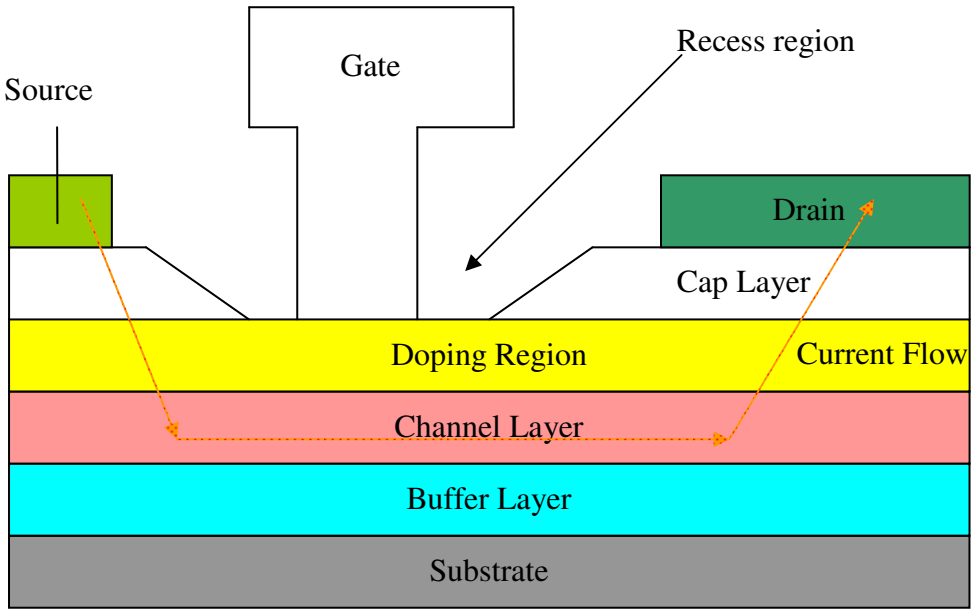



Figure 2-1 Typical HEMT Device strucuture

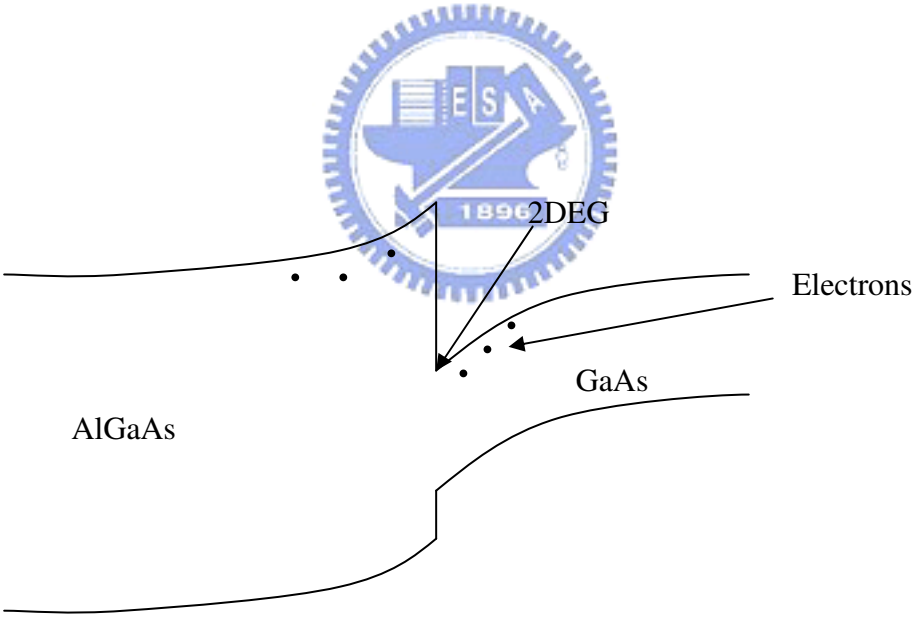



Figure 2-2 Two-dimensional electron gas (2DEG) at AlGaAs/GaAs heterinterface

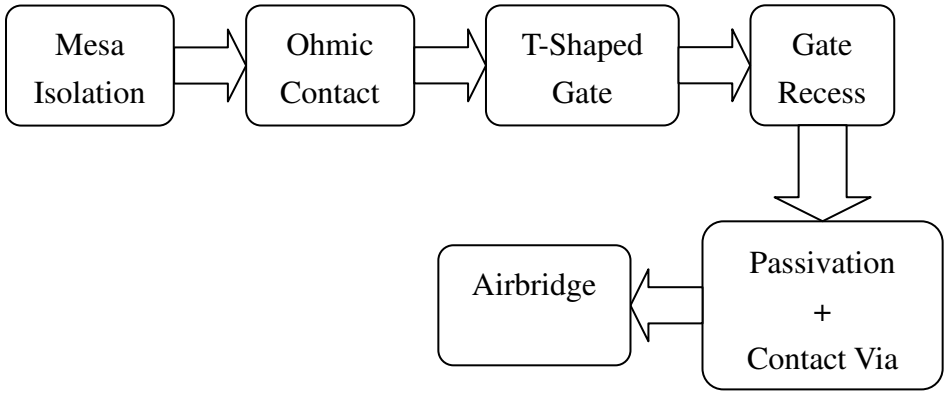
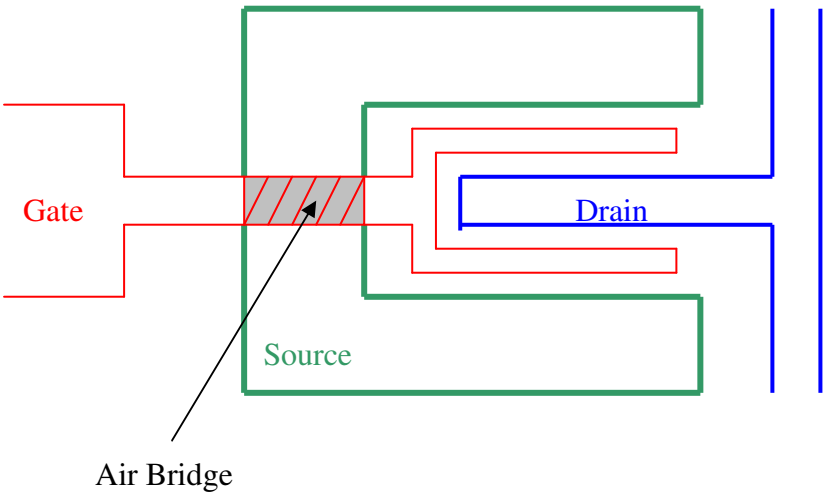
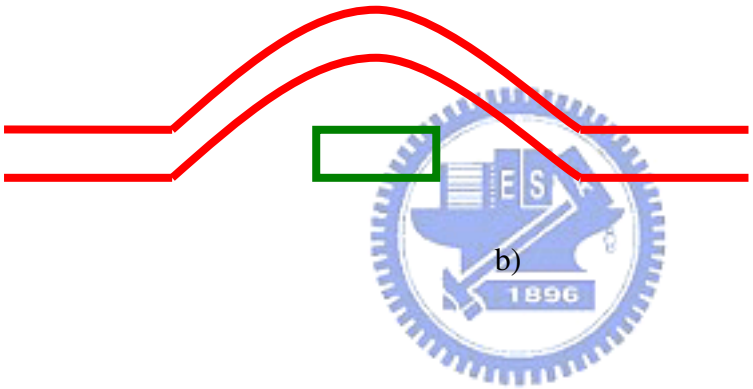



Figure 3-1 Basic Flow Chart of HEMT Fabrication




a)



b)

Figure 3-2 Typical Air Bridge a) Top-View; b) Side-View

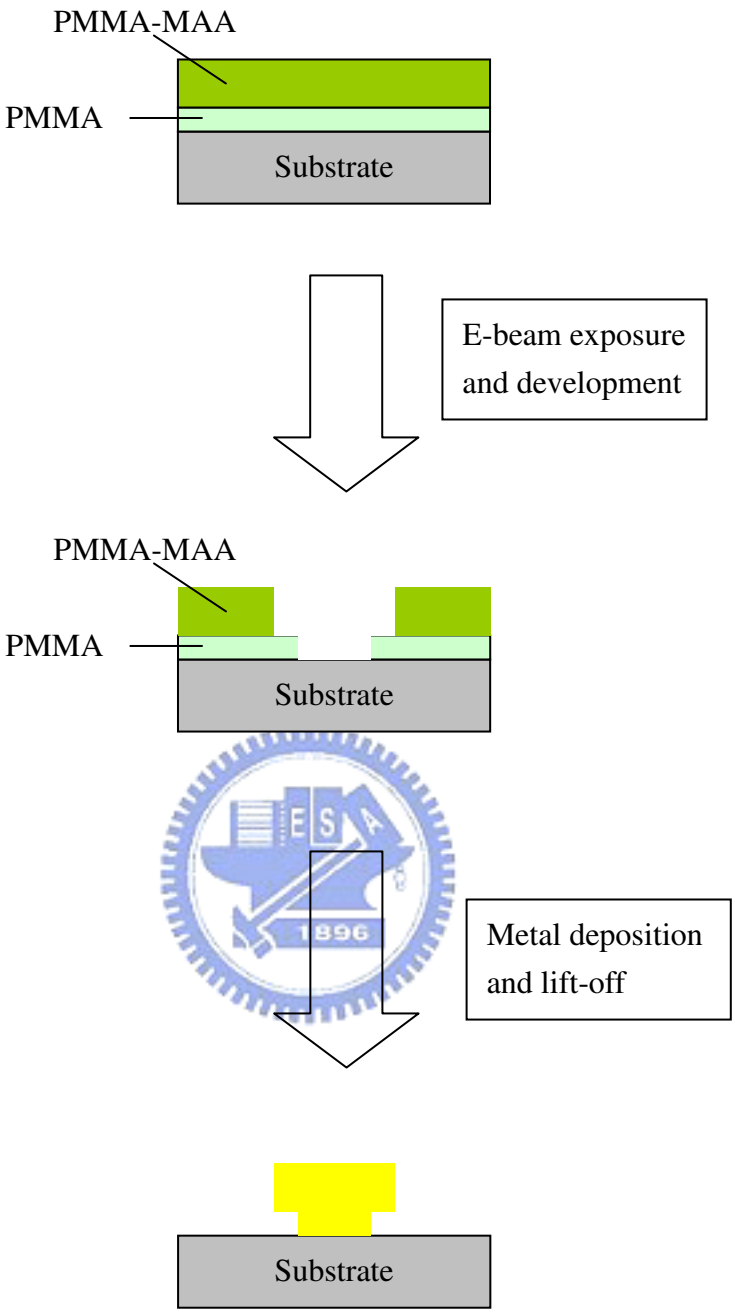



Figure 4-1 Dual layer gate fabrication process

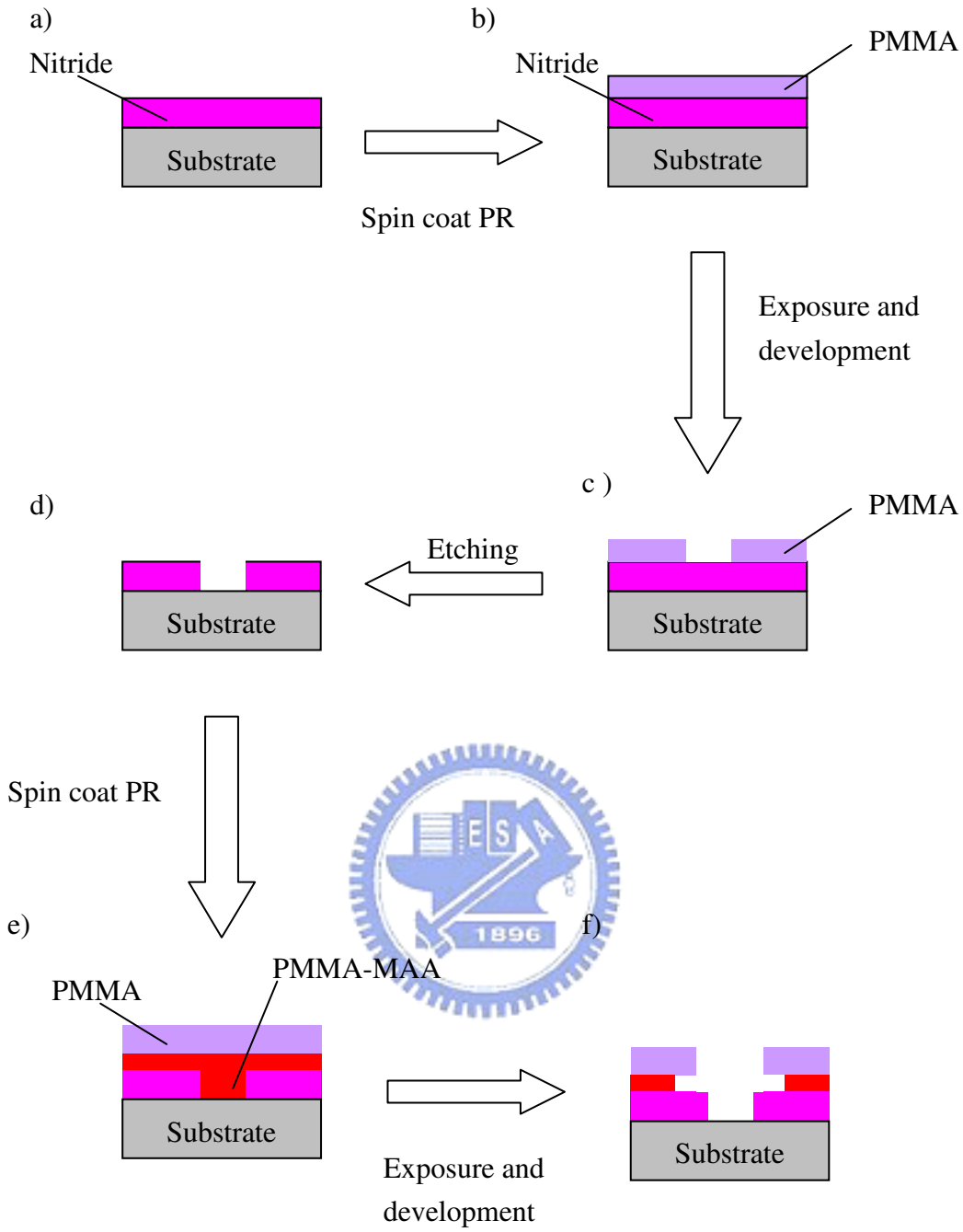



Figure 4-2 Modified Dual Layer Process

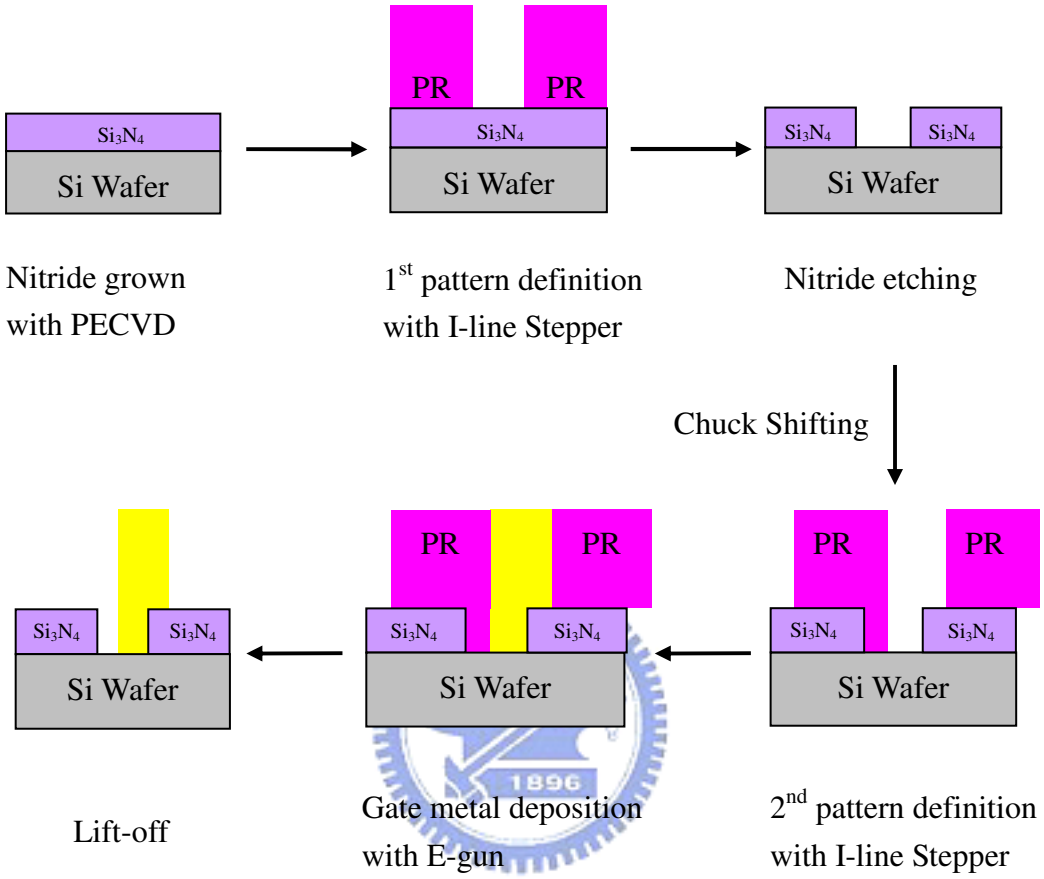



Figure 4-3 Flowchart of Gate Fabrication Using I-line Stepper

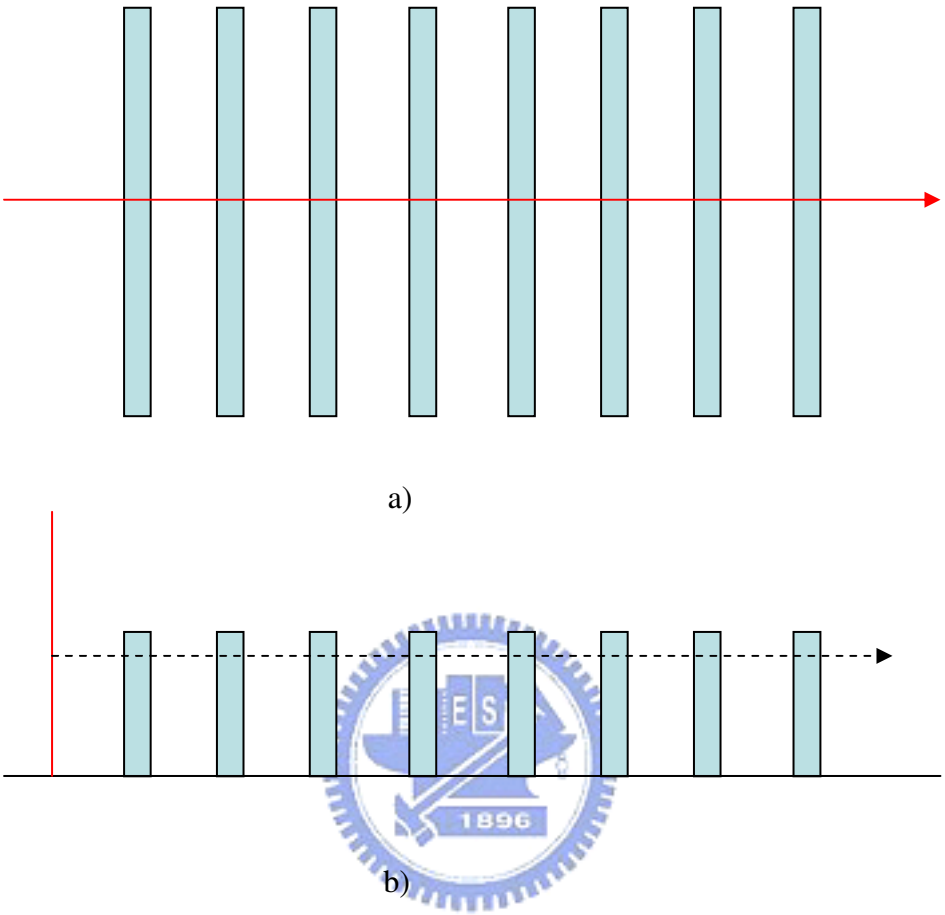



Figure 4-4 Stepper Alignment Mark: a) Top View; b) Side View

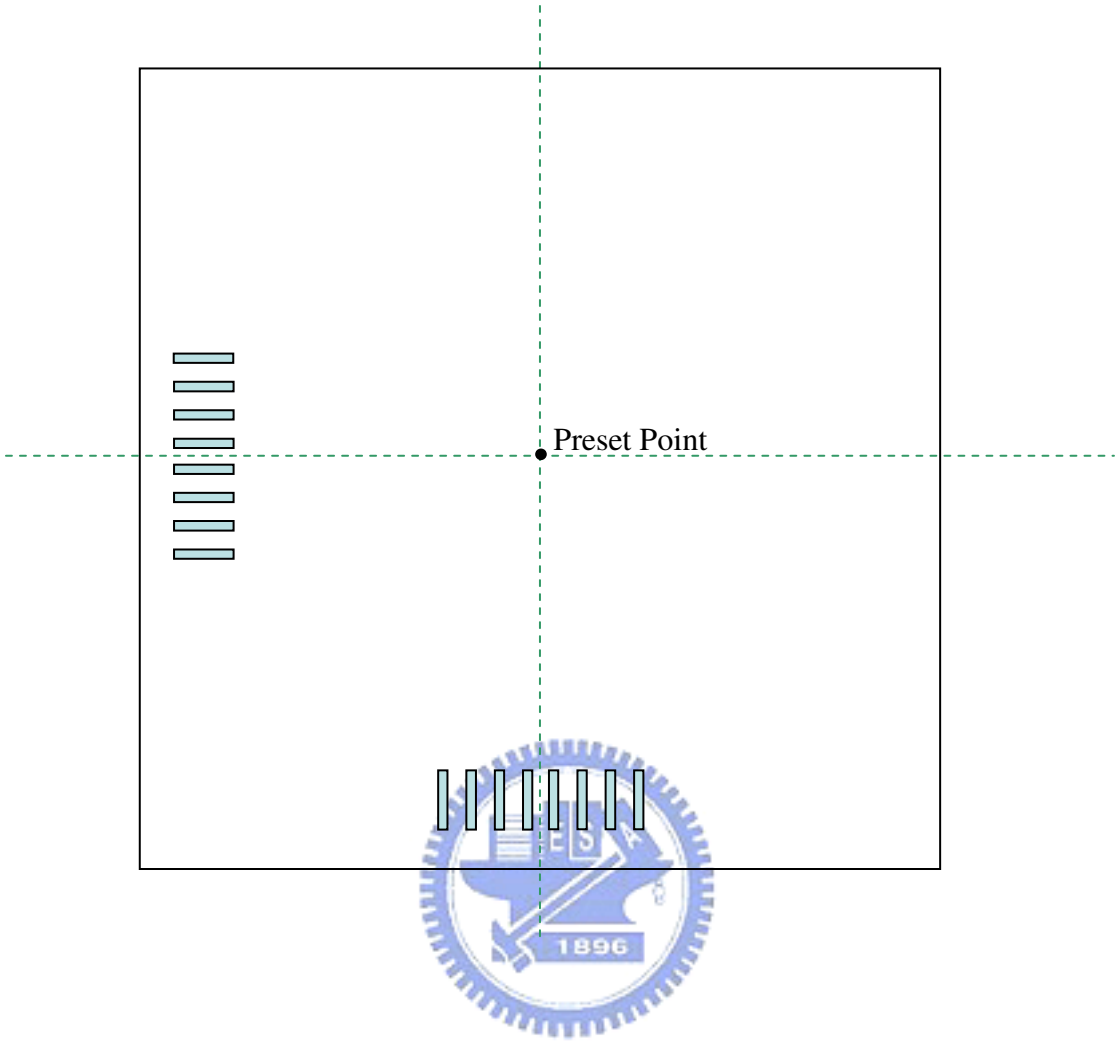



Figure 4-5 Location of Grating on a Stepper Mask

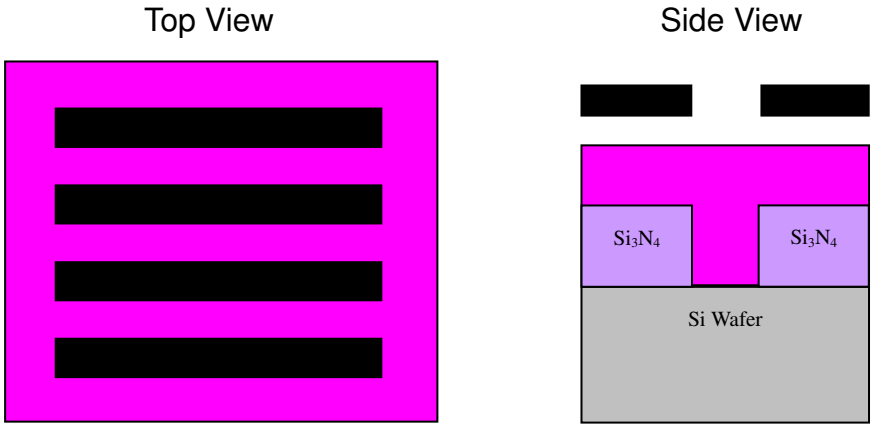



Figure 4-6 Mask aligned exactly over the first pattern

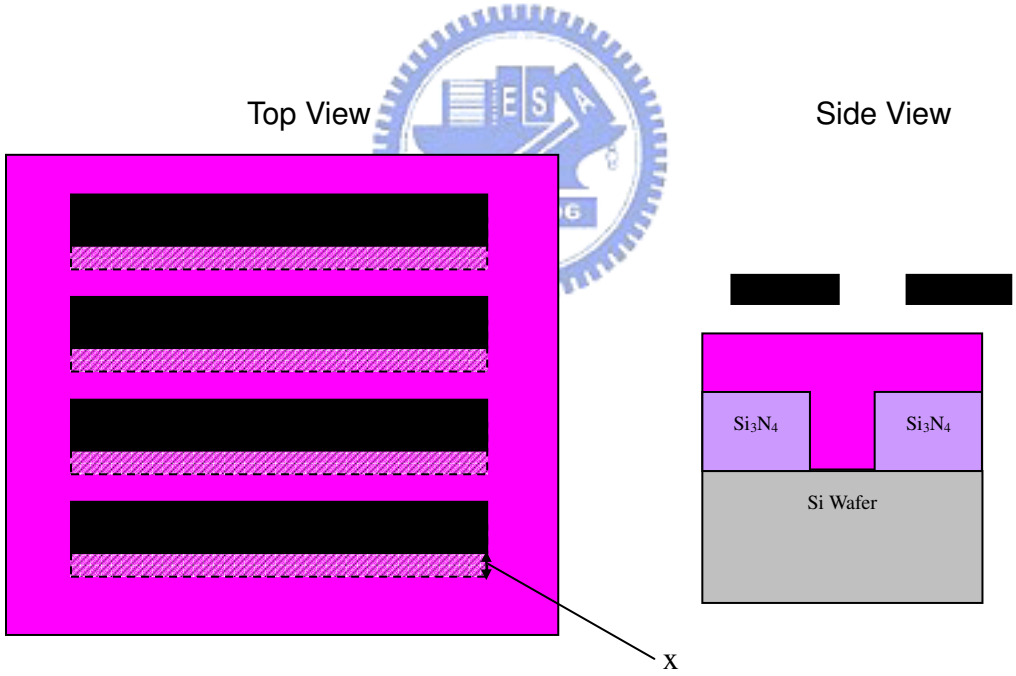



Figure 4-7 Stage shifted after alignment

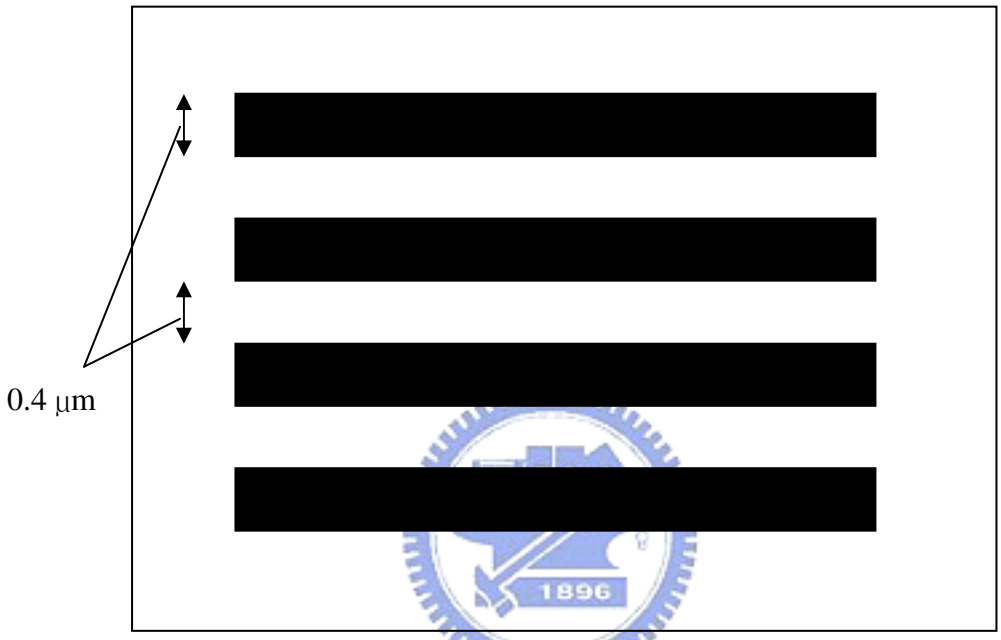



Figure 4-8 I-line stepper mask used for this study

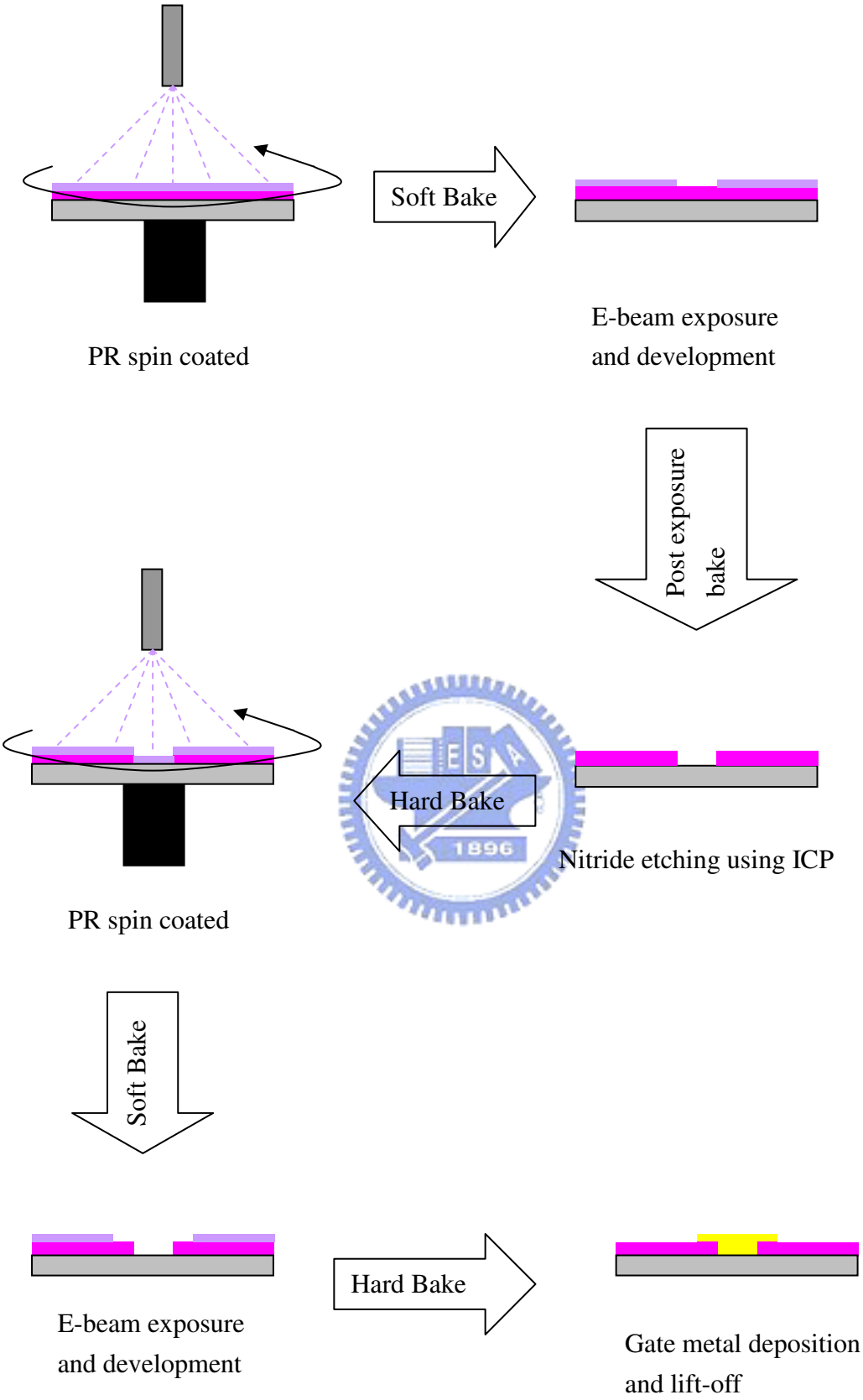



Figure 4-9 Flowchart of gate fabrication using chemical amplified resist

$a_1$ = in at input $b_2$ = out at output

$b_1$ = out at input $a_2$ = in at output

$S_{11} = b_1/a_1$ *Input reflection coefficient*
$S_{21} = b_2/a_1$ *Gain/Loss*
$S_{12} = b_1/a_2$ *Isolation*
$S_{22} = b_2/a_2$ *Output reflection coefficient*

Figure 5-1 Definition of S-parameters

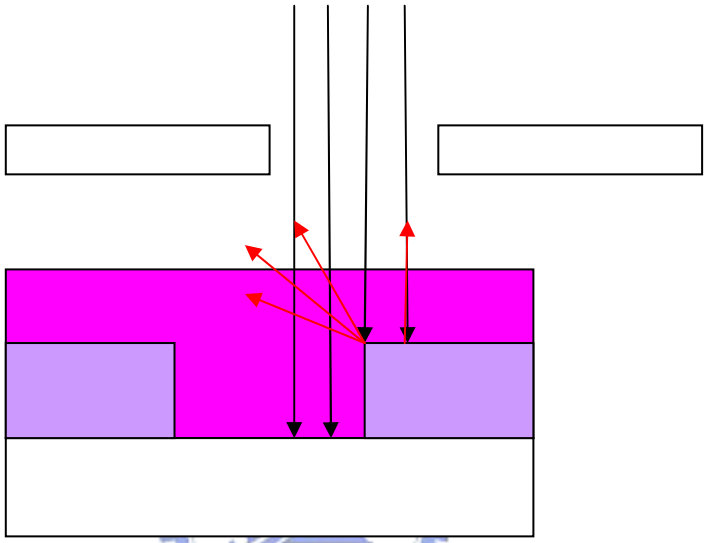


Figure 6-1 Scattering Effect

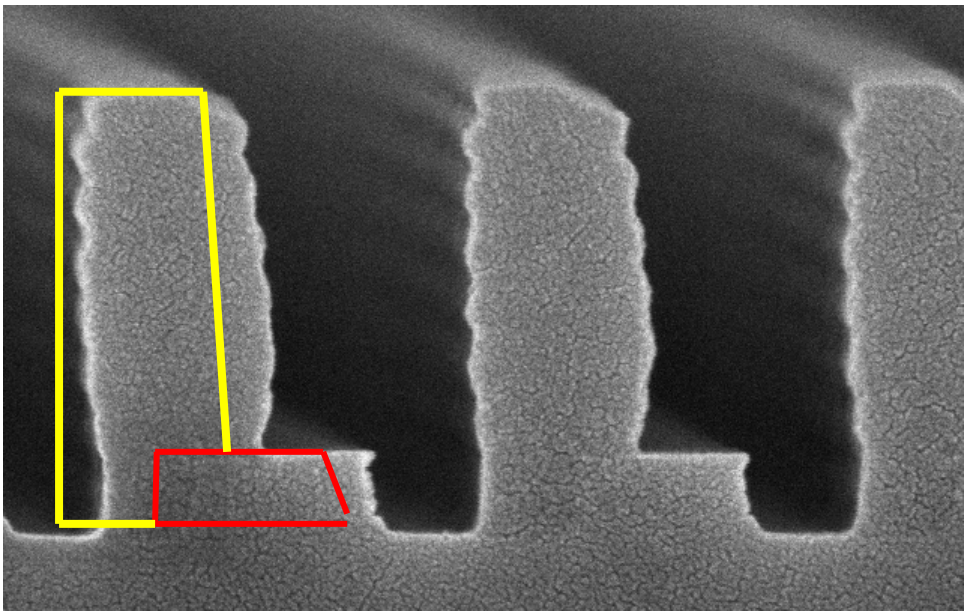


Figure 6-2a)  SEM picture after shifting mechanism

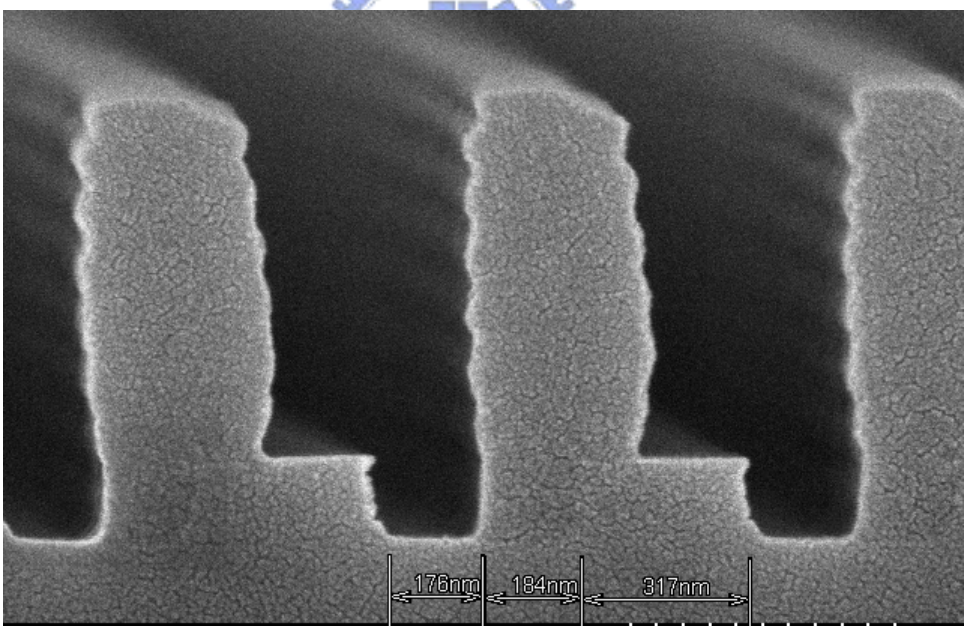



Figure 6-2b)  SEM picture of a 0.2μm shifted sample

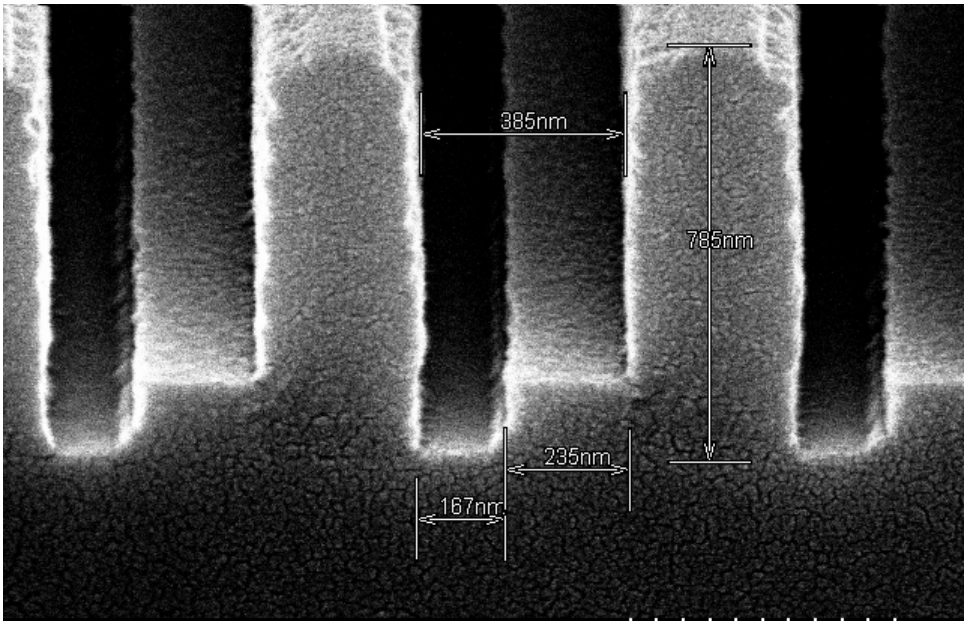



Figure 6-3 Optimum result of a 0.2µm shifted sample

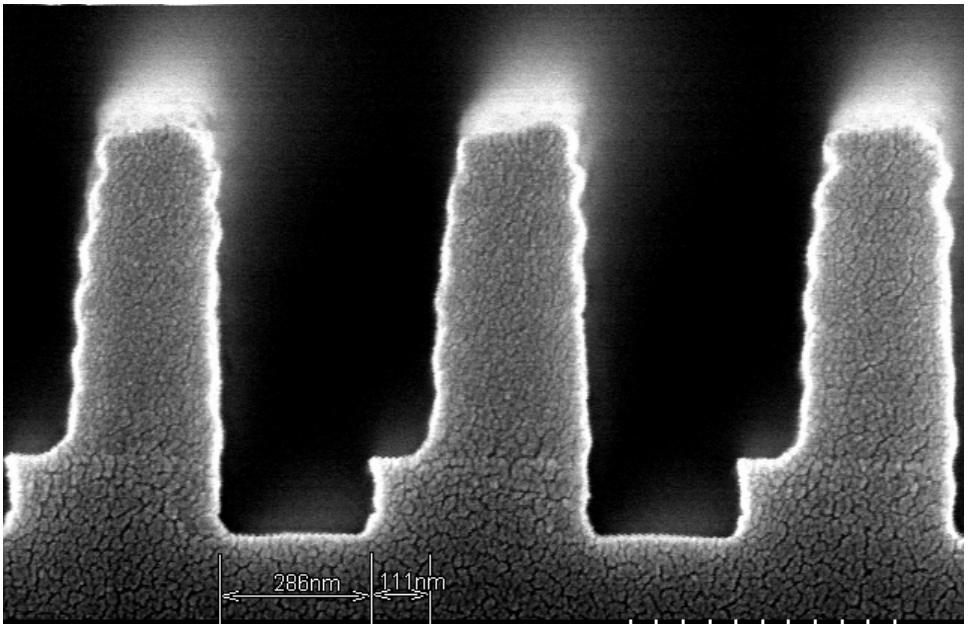



Figure 6-4 SEM picture of a 0.1µm shifted sample

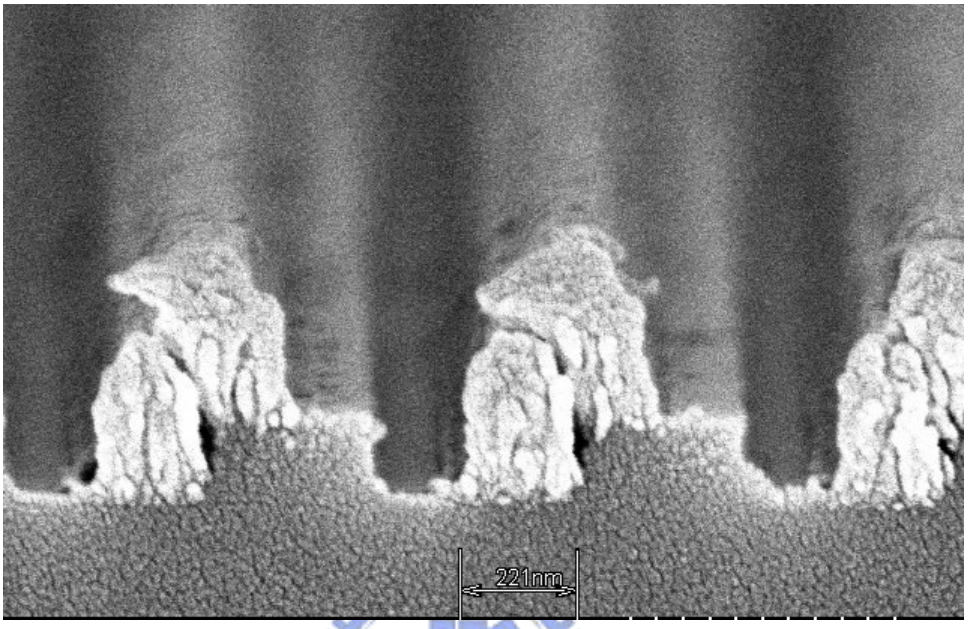



Figure 6-5 Metal gate after lift-off process

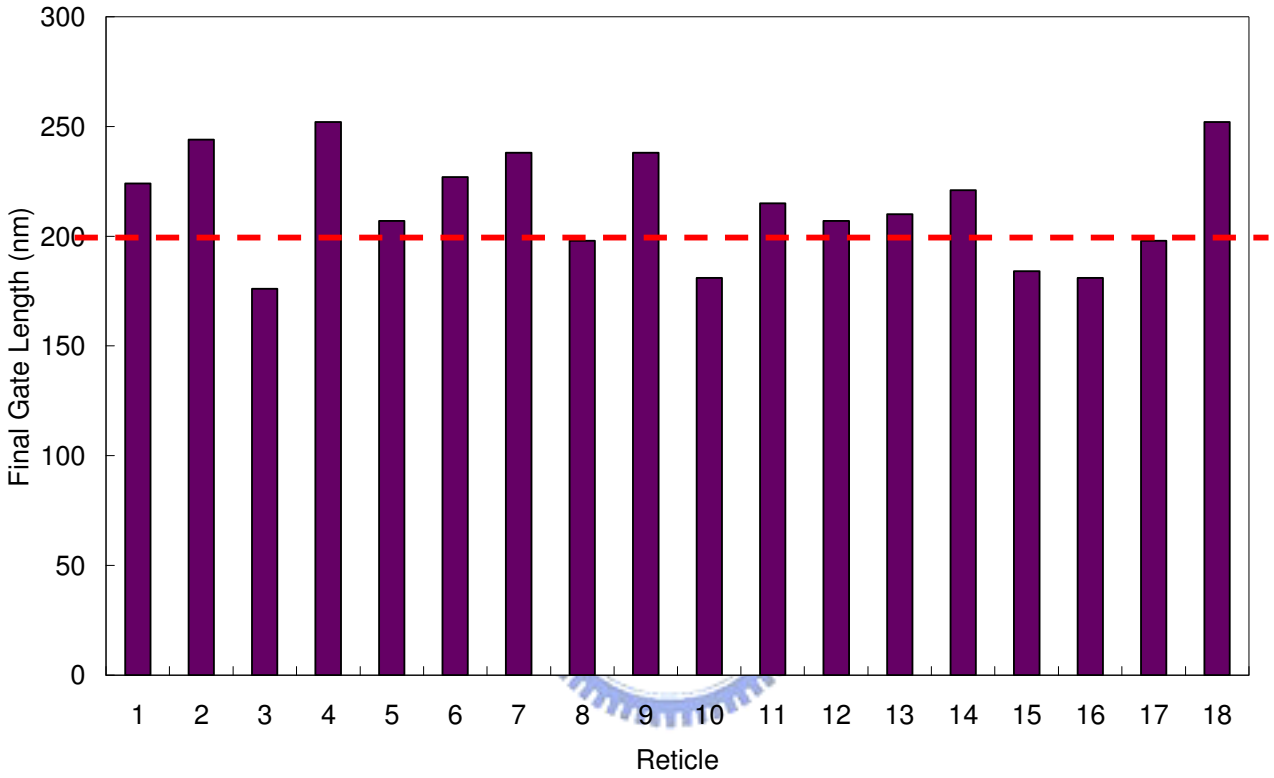
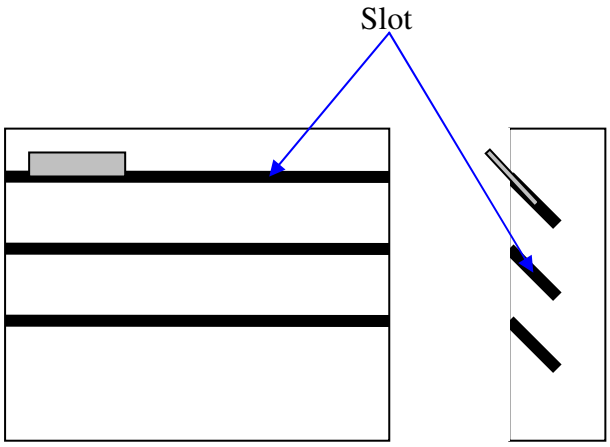
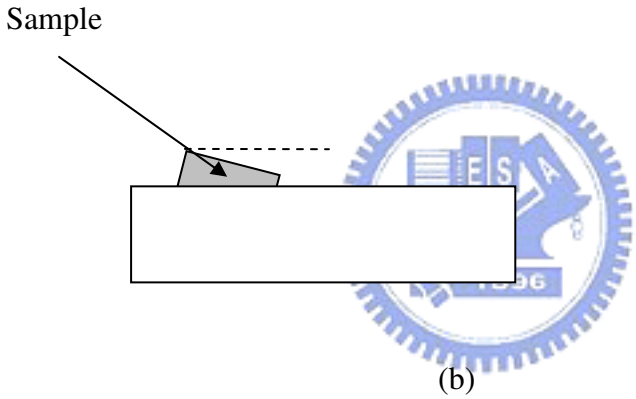



Figure 6-6 Bar graph of 18 reticles with 0.2μm shift




(a)




(b)

Figure 6-7 SEM Stage

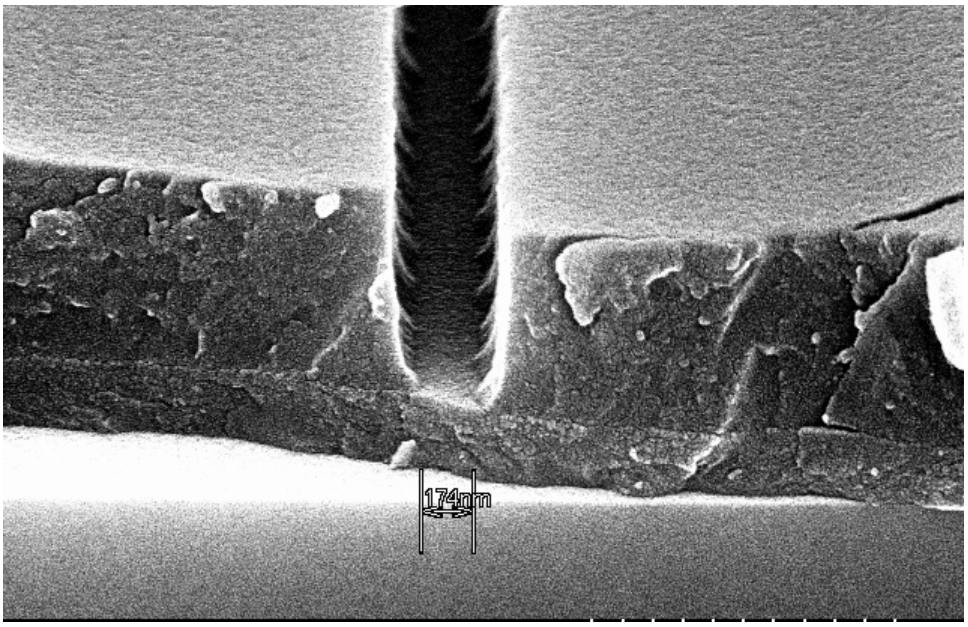



Figure 6-8a Foot for T-shaped Gate

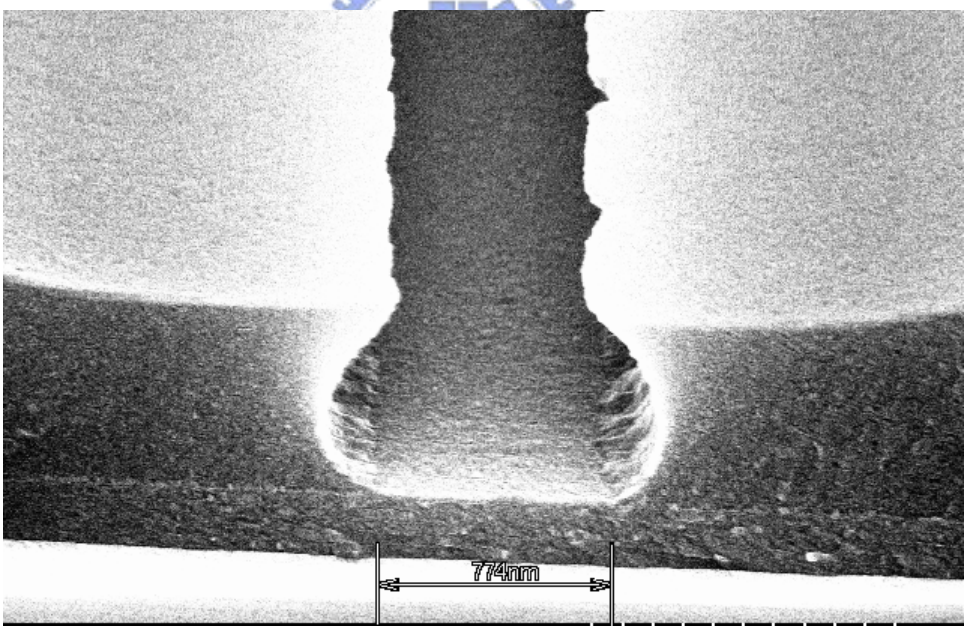



Figure 6-8b Head for T-shaped gate

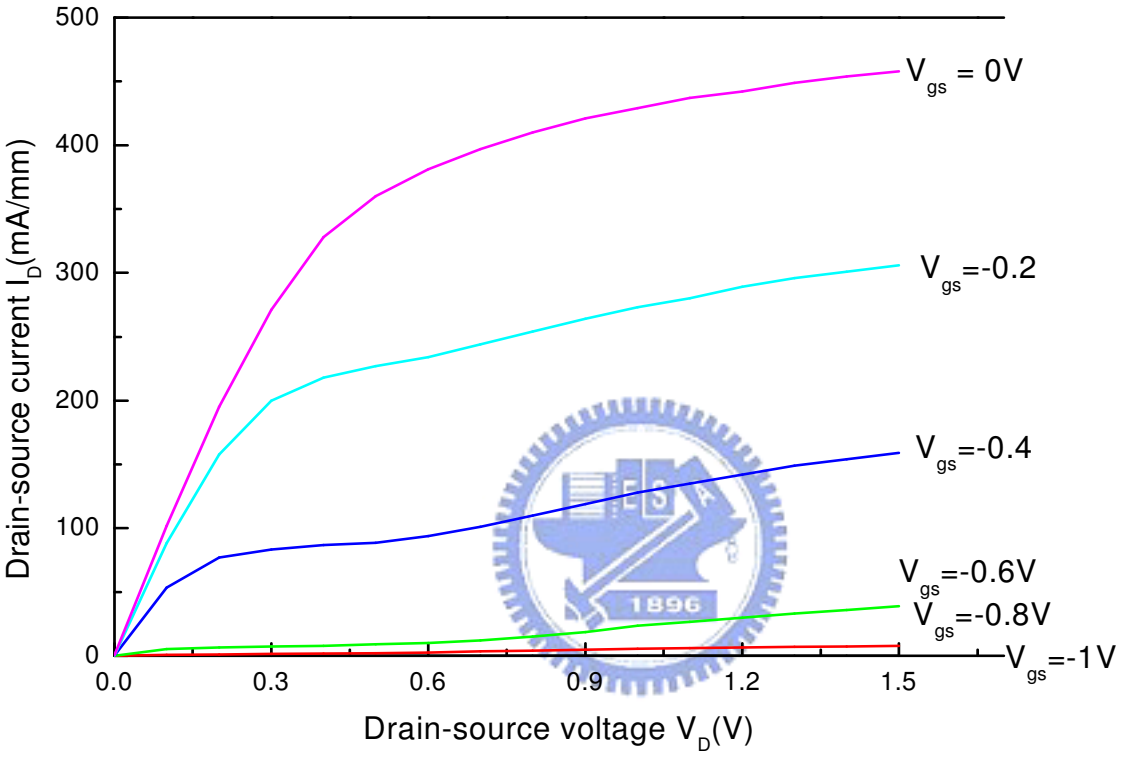



Figure 6-9 I-V curve

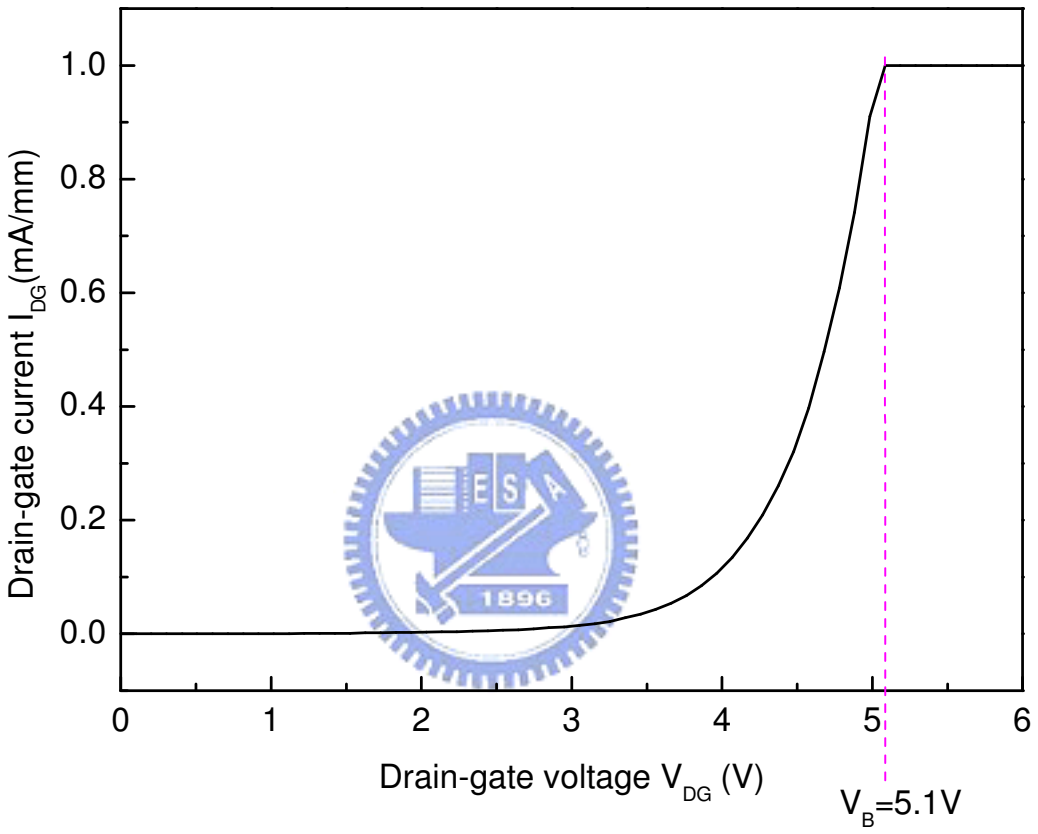



Figure 6-10 $V_{DG}$ vs. $I_{DG}$

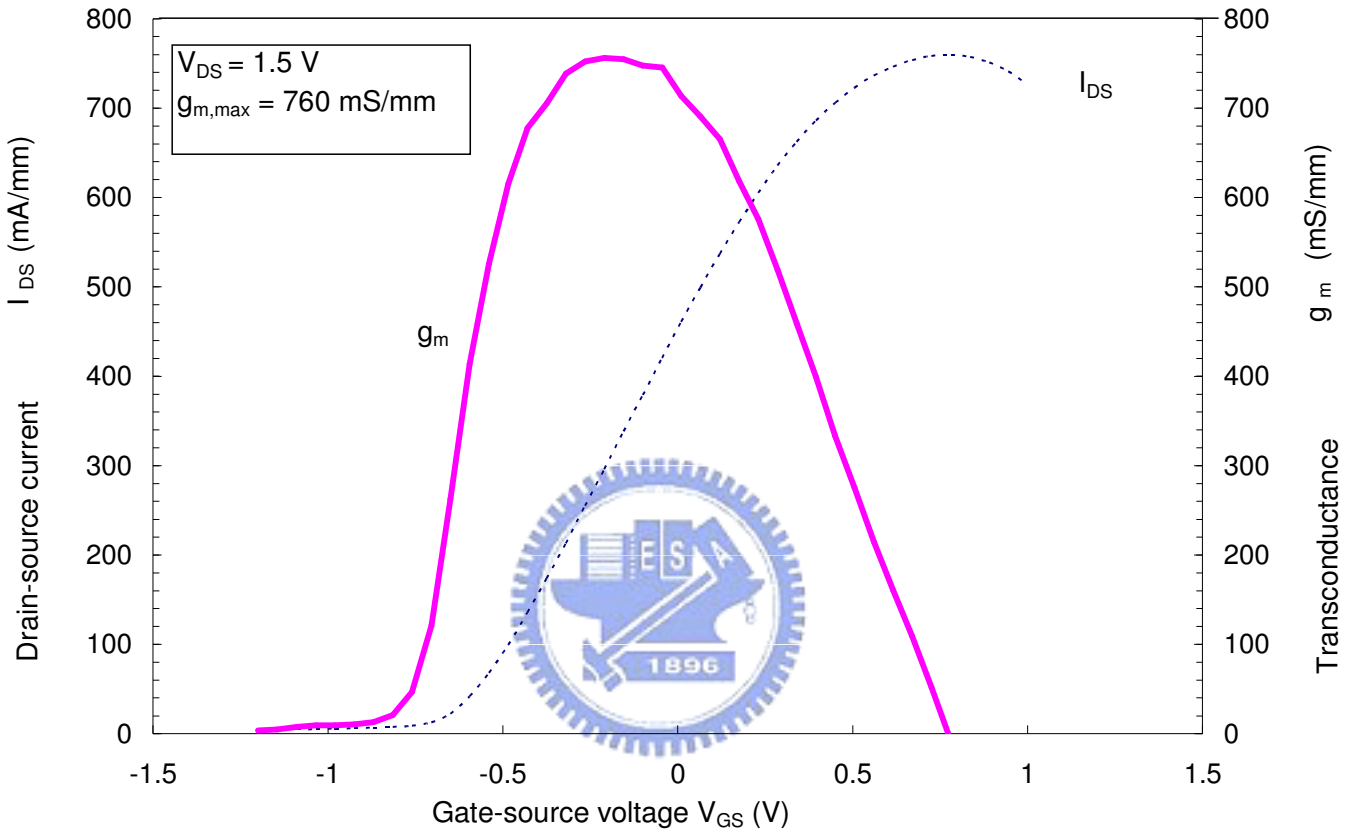



Figure 6-11 Transconductance, $g_m$

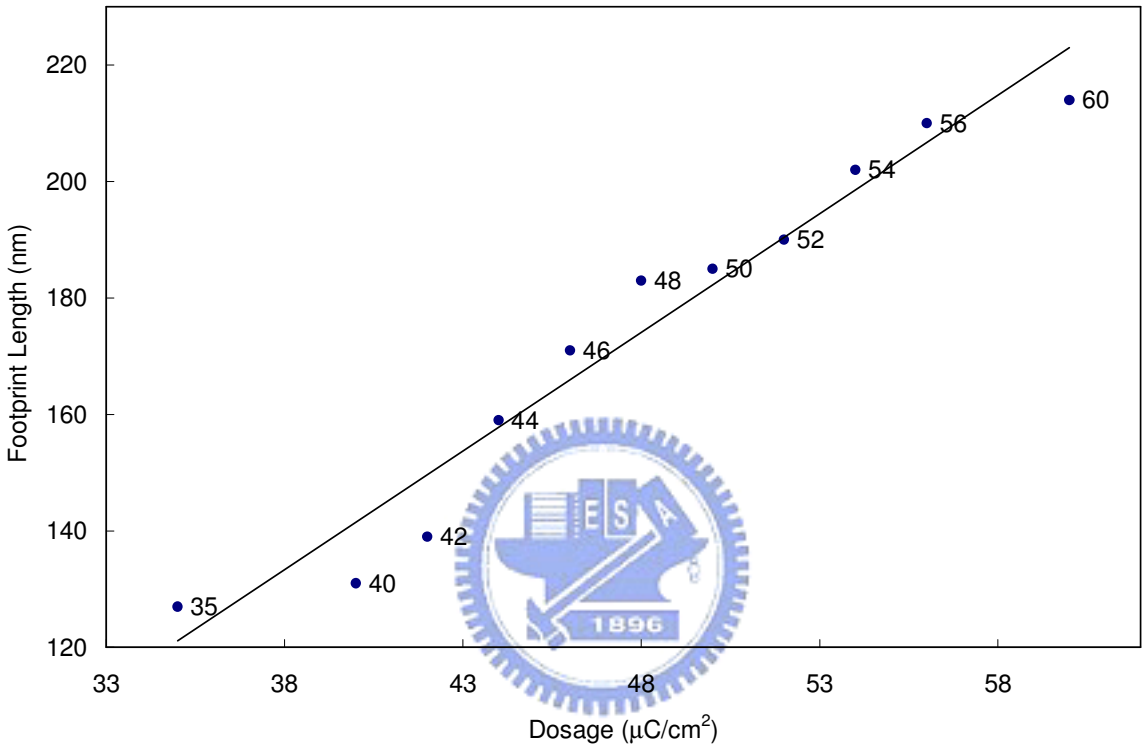



Figure 6-12 Dosage vs. Footprint Length for CA resist

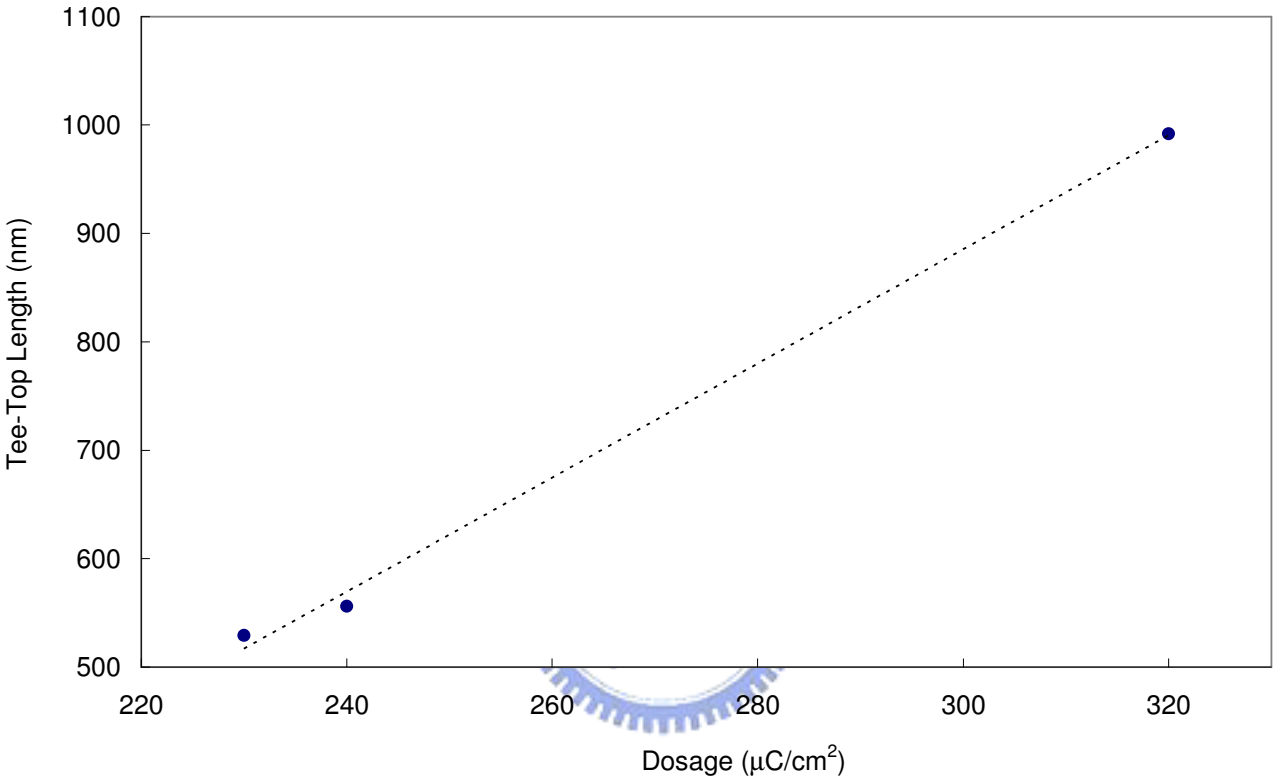



Figure 6-13 Dosage vs. Tee-Top Length for CA Resist

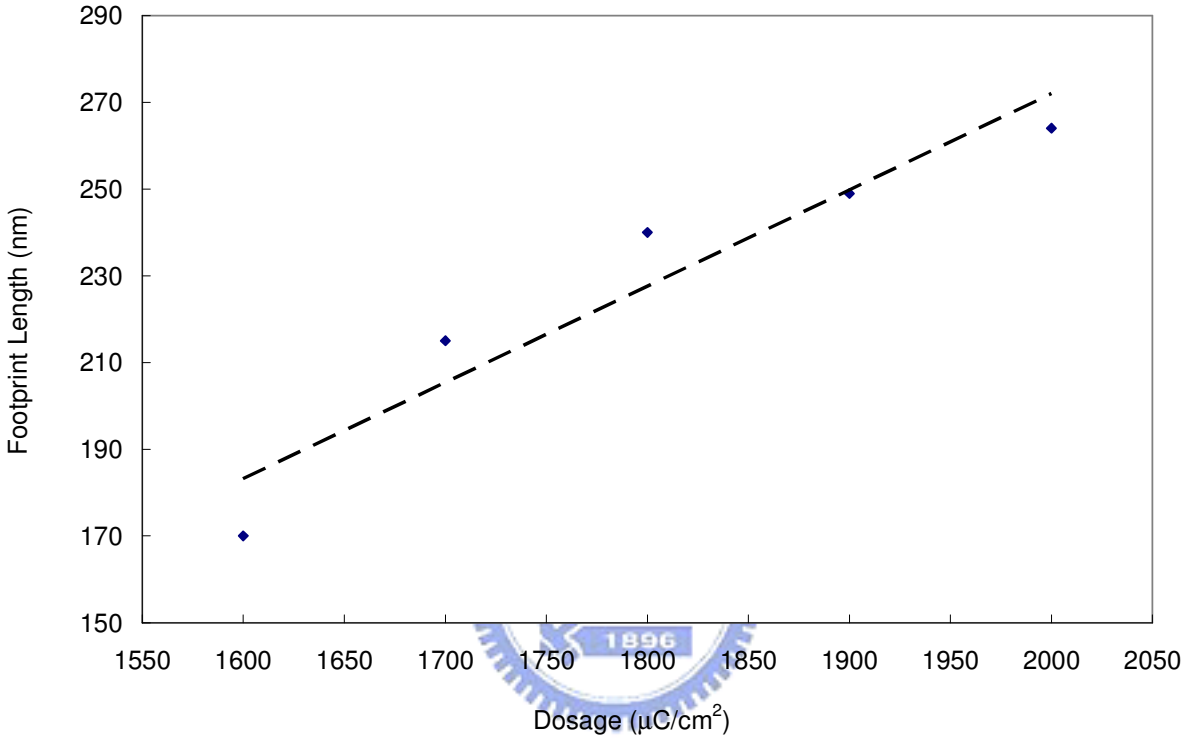



Figure 6-14 Dosage vs. Footprint Length for PMMA

| **Reticle** | **Final Gate Length (nm)**<br>Ideal: 200nm | **Error (nm)**<br>Real Length – Ideal Length |
|---|---|---|
| 1 | 224 | 24 |
| 2 | 244 | 44 |
| 3 | 176 | 24 |
| 4 | 252 | 52 |
| 5 | 207 | 7 |
| 6 | 227 | 27 |
| 7 | 238 | 38 |
| 8 | 198 | 2 |
| 9 | 238 | 38 |
| 10 | 181 | 19 |
| 11 | 215 | 15 |
| 12 | 207 | 7 |
| 13 | 210 | 10 |
| 14 | 221 | 21 |
| 15 | 184 | 16 |
| 16 | 181 | 19 |
| 17 | 198 | 2 |
| 18 | 252 | 52 |
| | Average = | 23 |

Table 6-1 Actual gate lengths and experimental errors

| | **Dosage (μC/cm$^2$)** | **Footprint Length (nm)** |
|---|---|---|
| CA resist (DSE1010) | 46 | 171 |
| *PMMA/PMMA* | *1600* | *170* |
| CA resist (DSE1010) | 56 | 210 |
| *PMMA/PMMA* | *1700* | *215* |

Table 6-2 Comparison between CA Resist and PMMA/PMMA-MAA

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