國立交通大學

電子工程學系電子研究所

博士論文

無摻雜 GaAs/AlGaAs 量子井之橫向 p-i-n 二極體

Lateral p-i-n Diode in an Undoped GaAs/AlGaAs Quantum Well

研究生 ： Dai Van Truong

指導教授 ： 李建平 博士

林聖迪 博士

中華民國　一〇三年 六月

無摻雜 GaAs/AlGaAs 量子井之橫向 p-i-n 二極體

Lateral p-i-n Diode in an Undoped GaAs/AlGaAs Quantum Well

研究生 ： 戴文長　　Student: Van-Truong Dai

指導教授 ： 李建平 博士　　Advisor: Dr. Chien-Ping Lee

林聖迪 博士　　Dr. Sheng-Di Lin

國立交通大學

電子工程學系電子研究所

博士論文

A thesis
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of Requirements
for the Degree of Doctor of Philosophy
in
Electronics Engineering

June 2014
Hsinchu, Taiwan, Republic of China

中華民國 一〇三年 六月

無摻雜 GaAs/AlGaAs 量子井之橫向 p-i-n 二極體

Lateral p-i-n Diode in an Undoped GaAs/AlGaAs Quantum Well

研究生：戴文長 (Dai Van Truong)　　指導教授：李建平 博士

林聖迪 博士

電子工程學系電子研究所

摘要

在表面聲波(SAW)驅動的單光子源元件中，高品質的二維 p-i-n 接面是個關鍵的因素。另外二維 p-n 橫向接面是另一個在光學方式探討二維系統中電子自旋有競爭力的選擇。在本論文中，我們發展了一個利用普通的金屬化與曝光製程，可靠且相對簡單的方式，在完全沒有摻雜的 GaAs/AlGaAs 量子井結構上來製作 p-i-n 橫向接面。

一個沒有摻雜的異質接面所誘發出的二維電子或電洞氣相較於有摻雜的系統表現出許多的優點，例如遷移率，特別是在低載子濃度下。為了得到這個優點，我們發展了一個可被誘發的橫向接面二維 p-i-n 二極體。兩種不同類型的通道透過金屬-絕緣質-半導體(MIS)閘極，其稱之為單一閘極元件誘發出。在 p 類型施加負電壓與 n 類型施加正電壓下，2DHG 與 2DEG 通道可以在 GaAs 量子井中被誘發出，所以一個橫向接面的二維 p-i-n 二極體因此產生。我們研究了這個元件在低溫的電性與光性。此 2DEG 與 2DHG 被誘發的臨界電壓分別為 3.5V 與 -1.25V。元件的電壓電流曲線在導通電壓 1.53V 電壓時呈現了清楚的整流特性。及符合理論的計算導通電壓值 V_{bi} = 1.535 V。電激發螢光的峰值在 1.529 eV (811 nm)而半高寬有 4.4 meV。這吻合理論計算中量子井基態的能量。

然而因為閘極與通道的距離使得閘極控制量子井的載子能力並不是非常有效率。導致兩個在絕緣層上的上層閘極不能彼此靠得太近。這直接影響到在 i 區域的載子複合。另外這個限制讓元件的發展上更加受限，例如表面聲波驅動的單光子源。因此我更發展了兩個通道同時有表面閘極與上層閘極的雙閘極結構。這個表面的蕭基閘極提供了一個通道中載子很好的控制能力下同時可以彼此靠近。跨越源極與汲極在絕緣層這上的上層閘極，可以在歐姆接觸與閘極間，沒有漏電路徑下控制著源極與汲極間的通道載子。雙閘極元件表現出較穩定的電性與清楚的光學頻譜。這些成果展示出這個元件非常適合在單光子元件的應用。

Lateral p-i-n Diode in an Undoped GaAs/AlGaAs Quantum Well

Student: Van-Truong Dai **Advisor: Dr. Chien-Ping Lee**

Dr. Sheng-Di Lin

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

Abstract

In SAW-driven single-photon source devices, the key component is a high-quality 2-D p-i-n junction. In addition, lateral 2-D p-n junctions are also potential candidates for investigating the properties of electron spins in low-dimensional systems by optical methods. In this thesis, we developed a reliable and relatively easy method to fabricate a lateral p–i–n junction in a completely undoped GaAs/AlGaAs quantum well structure by utilizing conventional metallization and lithography processes.

An induced gas (2DEG or 2DHG) in undoped heterostructure shows great advantages compared to a doped gas, such as high mobility, especially in low carrier density. To gain the advantage of induced gas, we developed an induced lateral 2D p-i-n diode. The two different types of channels are induced via metal-insulator-semiconductor (MIS) gates, which called single-gate devices. With a negative voltage applied on the p-gates and a positive voltage applied on the n-gates, both 2DHG and 2DEG channels can be induced in the GaAs quantum well, so a lateral 2-D p-i-n diode is formed. The electrical and optical of the devices at low temperature are studied. The 2DEG and 2DHG can be induced at threshold voltage of 3.5 V and -1.25 V, respectively. The current-voltage curve of the devices shows clearly the rectifying behavior with a turn-on voltage of 1.53 V. This is in agreement with the theoretical calculation of the built-in voltage V_{bi}

= 1.535 V. The main peak of electroluminescence is at 1.529 eV (811 nm) with the full-width at half-maximum of 4.4 meV. This is in good agreement with theoretical calculation of ground state energy of the quantum well.

However, the gate control of the carriers in the quantum well is not very efficient because of the distant gate from the channel. As a result, the two top gates on the insulator could not be put too close to each other. This directly affects the carrier recombination in the i region. In addition, this limits further development more complicated devices, such as SAW-driven single-photon source. Thus, we developed the twin-gate structure which has surface gate and top gate for each channel. The surface Schottky gates provide a very good control for the carriers in the channel and at the same time can be put very close to each other. The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts. The twin-gate devices show more stable electrical characteristics and clearer optical spectrum. These results demonstrate that the device is promising for applications in the single-photon devices.

Acknowledgements

I am indebted to many people who contributed in several ways to this thesis, and suppoted me with their cooperation and timely help.

In particular, I would like to acknowledge my adviser, Professor Chien Ping Lee, for providing me an opportunity to work in his research group. He has been a great mentor with his enthusiasm, understanding and willingness to help students professionally and personally. He also has been an exceptional role model of life.

I also would like to thank my co-adviser, Professor Sheng Di Lin, who gave me strong motivation in my research throughout his discussion. I have learnt a lot about methodology of research and life from him. I would like to thank Professor Gray Lin for the many discussions we had about my research, for the numerous suggestions and experiment equipment supports.

I am indebted to Mr. Wu Jau Yang and Ms. Lee Yi San for their help not only in research but also in life. I am extremely thankful to Mr. Hsu-Chieh Cheng, Mr. Shih-Wei Lin, Mr. Chang Chia Hao, Ms. Shu Pei Ying, Mr. Liu Nai Cheng, Mr. Zhang Yin Jie, and Mr. Chen Shu Wen for serving my experimental supports. I would like to thanks to all my lab members for their friendship and help. I also thank Dr. Li Liang Chen for helpful measurement suggestions.

I would like to thank Department of Electronics Engineering, Chiao Tung University, especially Ms. M. N. Lin, Ms. Patty Chen for their enthusiasm and help.

I wish to thank my parents, my brothers, my sisters. They have given me their love and support, and I am grateful to them. My daughter Minh Chau has been a source of joy and delight, and has made fatherhood a wonderful experience for me. I thank my dear wife Do Hien, who has been so patient and selfless during our seven years of marriage. I could not have done this work without her love and support.

I would like to thank everybody who was important to the successful realization of thesis, as well as expressing my apology that I could not mention personally one by one.

The financial support of my Ph. D research work by a grant from NCTU and the NSC, Taiwan, ROC is grateful acknowledged.

Table of Contents

摘要 I

Abstract III

Acknowledgement V

Table of Contents VI

Abbreviations and Symbols IX

Table Captions XI

Figure Captions XII

Chapter 1: Introduction and motivation 1

1.1. Motivation 1

1.1.1. Spin Hall Effect 1

1.1.2. SAW-driven Single photon Source 3

1.2. Preview of Fabrication of Lateral p-n junction 4

1.2.1. Employing the Amphoteric Nature of the Si Dopants on GaAs 4

1.2.2. n-type compensation doping of a p-doped heterostructure 6

1.2.3. Partially Etching a Modulation Doped AlGaAs/GaAs Heterostructures 7

1.2.4. Other Methods 8

1.3. Our Approach 10

1.3.1. Induced 2DEG on an Undoped Heterostructure. 10

1.3.2. Lateral 2D p-i-n junction on an undoped heterostructure. 11

1.4. Contents of Thesis 11

Chapter 2: Device Fabrication Techniques 12

2.1. Basic Principle of Formation an Induced 2DEG 12

2.2. Device design 15

2.2.1. Sample Structure 15

2.2.2. Device design 16
2.3. Process Flow 17
2.3.1. Mesa Isolation 18
2.3.2. Contact Metallization and Thermal Diffusion 18
2.3.3. Single-Gate Devices 19
2.3.4. Twin-Gate Devices 20
2.4. Fabrication Procedures 21
2.4.1. Sample Cleaning 21
2.4.2. Photolithography 22
2.4.3. Wet Etching and Dry Etching 25
2.4.4. Ohmic Contact Metallization 28
2.4.5. Lift-off and Thermal Annealing 30
2.4.6. Dielectric Layer Deposition 31
2.4.7. Gate Metallization 32
Chapter 3: Single-Gate Devices 34
3. 1. Mask Design 34
3. 2. Principle of Device Operation 35
3.3. Electrical Characteristics 37
3.3.1. Single Channel 37
3.3.2. Current – Voltage Characteristics of the Single-Gate Diode. 39
3.4. Optical Characteristics 41
3.5. The Yield of n-channel and p-channel 44
3.6. Disadvantages of Single-Gate Structure 45
Chapter 4: Twin-Gate Devices 47
4.1. Mask Design 47
4.2. Principle of Device Operation 48

4.3. Electrical Characteristics 50
4.3.1. Single Channel 50
4.3.2. Current-voltage Characteristics of the Twin-Gate Diode 54
4.4. Optical Characteristics 56
4.4.1. Electroluminescence Spectrum 56
4.4.2. External quantum efficiency 58
4.5. The Yield of n-channel and p-channel 59
Chapter 5: Summary and Future Work 60
5.1. Summary 60
5.2. Future Work 60
5.2.1. Single-Electron Pump Driven Single-Photon Source 61
References 63
Appendix -1 69

Abbreviations and Symbols

Symbol	Description	Symbol	Description
SAW	Surface Acoustic Wave	2DEG	Two-Dimension Electron Gas
SHE	Spin Hall Effect	2DHG	Two-Dimension Electron Gas
2D	Two Dimensional	MIS	Metal Insulator Semiconductor
n-gate	Insulated gate which overlaps n-type ohmic	p-gate	Insulated gate which overlaps p-type ohmic
n-TG	Top gate which overlaps n-type ohmic	p-TG	Top gate which overlaps p-type ohmic
n-SG	Surface gate which overlaps n-type ohmic	p-SG	Surface gate which overlaps p-type ohmic
V_{bi}	Built-in voltage of the lateral p-i-n junction	E_g	Bandgap energy of GaAs
E_{1n}	Ground state energies of the electrons in quantum well	E_{1p}	Ground state energies of the holes in quantum well
m_n	Effective electron mass	m_p	Effective hole mass
N_{sn}	Area densities of electrons in the 2DEG	N_{sp}	Area densities of electrons in the 2DEG
V_{ds}	Drain to source voltage	I_{ds}	Drain to source current
V_{gn}	Voltage applied to n-type ohmic side gate	V_{gp}	Voltage applied to p-type ohmic side gate
I_{gn}	Voltage applied to n-type ohmic side gate	I_{gp}	Leakage current of p-type ohmic side gate
V_{tg}^{n}	Voltage applied to n-type ohmic side top gate	V_{tg}^{p}	Voltage applied to p-type ohmic side top gate
I_{tg}^{n}	Leakage current of n-type ohmic side top gate	I_{tg}^{p}	Leakage current of p-type ohmic side top gate
V_{sg}^{n}	Voltage applied to n-type ohmic side surface gate	V_{sg}^{p}	Voltage applied to p-type ohmic side surface gate

Symbol	Description	Symbol	Description
I_{sg}^{n}	Leakage current of n-type ohmic side surface gate	I_{sg}^{p}	Leakage current of p-type ohmic side surface gate
V_{pn}	p-type ohmic to n-type ohmic voltage	I_{pn}	p-type ohmic to n-type ohmic current
η_{ext}	External quantum efficiency of the p-i-n diode	e	Electron charge
N_{ph}	Photon count measured by CCD	RF	Radio frequency

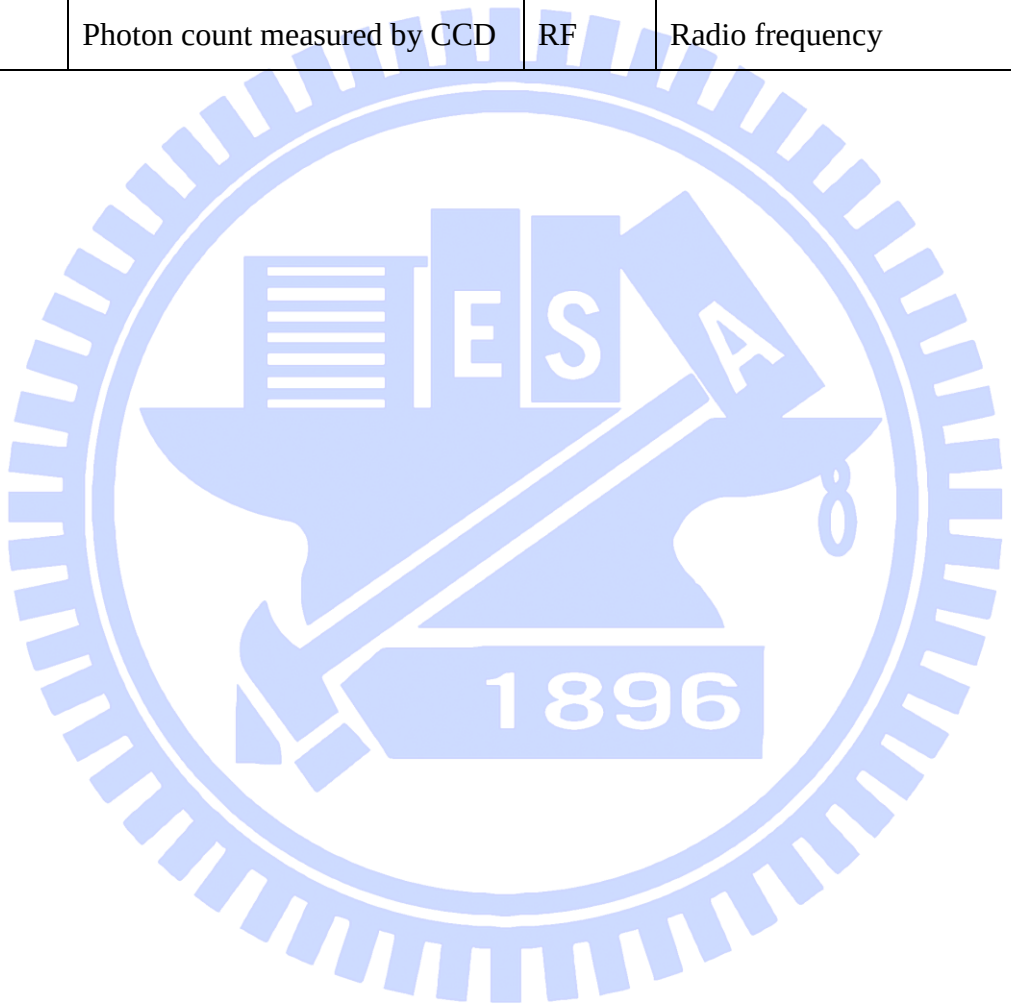


Table Captions

Table 2.1: *Comparison between wet and dry etching* ……..……25

Table 2.2: *Physical properties of polyimide* ……31

Figure captions

Chapter 1

Figure 1.1 *The Spin Hall Effect. An electrical current induces spin accumulation at the lateral boundaries of the sample. Spin-up electrons accumulate one side and spin-down electrons on the other side.....2*

Figure 1.2 *Wunderlich et al.* ***a****, Schematic of the lateral p–n junction with the channel current I_p and the diode current I_{LED} for detecting spin accumulation. b, Emitted light polarization of recombined light in the p–n junction for the channel and diode current flow indicated by arrows in (a). 3*

Figure 1.3 *Foden et al. a, Schematic of the single-photon source. b, The conduction (CB) and valence-band (VB) edge profiles across the n-i-p junction and recombination when SAW wave propagate through.....4*

Figure 1.4 *Fabrication of lateral p-n junction by employing the amphoteric nature of the Si dopants on GaAs. N-type doping on (100) surface and p-type doping on (n11) surface with n <= 3.....5*

Figure 1.5 *Gell et al. Schematic diagram of a device which integration of a SAW transducer with a lateral p-n junction.....6*

Figure 1.6 *Reuter et al. Schematic presentation of a compensation n-type doping on p-type modulation doped heterostructures. 7*

Figure 1.7 *Schematic cross-section of a quasi-lateral p-n junction formed by partially etching a modulation doped heterostructures. 8*

Figure 1.8 *Fabrication scheme of a planar p-n junction proposed by Cecchini et al. 9*

Figure 1.9 *Schematic cross-section of a Lateral p-n junction created by bevel etching...9*

Figure 1.10 *Harrell et al. (a) Schematic cross-section of a indeced 2DEG on undoped GaAs/AlGaAs heterostructure. (b) Comparison between the mobility versus carrier density relationship of an induced 2DEG and that of a doped 2DEG. 10*

Figure 1.11 *Schematic diagram of an induced lateral 2D p-i-n junction. 11*

Chapter 2

Figure 2.1 *Schematic diagram of an induced gas 13*

Figure 2.2 *Band structure of an induced gas with assuming no surface state and background doping. (a), unbiased condition; Fermi energy is at the midgap energy. (b), positive voltage applied; Fermi energy is above the conduction band, a 2DEG will form. (c), negative voltage applied; Fermi energy is below the valence band, a 2DHG will be induced. 14*

Figure 2.3 *The ohmic contact diffusion profile. (a), a standard diffusion profile is shown; since this does not reach underneath the gate a 2D gas cannot be form. (b), the channel is contacted under the gate and so a 2D gas should form.....15*

Figure 2.4 *Schematic diagram showing GaAs/AlGaAs quantum well structure that was used to fabricate lateral p-i-n junctions.....16*

Figure 2.5 *Schematic diagram of a lateral 2D p-i-n junction. (a), single-gate device. (b), twin-gate device.....17*

Figure 2.6 *Mesa isolation process 18*

Figure 2.7 *p-type and n-type contact metallization.....19*

Figure 2.8 *Fabrication steps of single-gate devices.....20*

Figure 2.9 *Fabrication steps of the twin-gate devices 21*

Figure 2. 10 *Development of positive and negative photoresist 23*

Figure 2. 11 *Comparison of dry etching with and without O_2 plasma treatment 28*

Figure 2. 12 *Thermal annealing ohmic contact program 30*

Figure 2. 13 *Polyimide curing program.....32*

Chapter 3

Figure 3. 1 *Mask design for single-gate devices* *34*

Figure 3.2 *(a) Optical microscopy image of the finished devices, (b) schematic cross-section of the devices* *36*

Figure 3. 3 *The schematic band diagram at equilibrium along the channel of the 2D p-i-n diode. E_{1n} (dark yellow dashed line) and E_{1p} (purple dashed line) are ground state of electron and hole, respectively.* *37*

Figure 3. 4 *Current – voltage characteristics of 2DEG at temperature of 77 K and bias of V_{ds} = 200 mV between n-drain and n-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DEG channel.* *38*

Figure 3. 5 *Current – voltage characteristics of 2DHG at temperature of 77 K and bias of V_{ds} = 200 mV between p-drain and p-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DHG channel.* *39*

Figure 3. 6 *Current – voltage characteristics of the lateral 2D p-i-n diode at temperature of 1.5 K with p-gate and n-gate biasing at V_{gp} = -3 V and V_{gn} = +5 V, respectively. Vpn is the operation voltage of the diode. The inset shows a schematic diagram of the measurement setup for the lateral 2D p-i-n junction.* *40*

Figure 3. 7 *Electroluminescence spectra of the lateral 2D p-i-n diode at temperature of 1.5 K with p-gate and n-gate biasing at V_{gp} = -7 V and V_{gn} = +7 V, respectively, and a forward current I_{pn} = 200 μA.* *42*

Figure 3. 8 *Configuration of Micro Photoluminescence system* *43*

Figure 3. 9 *Contour plot of integrated spectrum intensity at temperature T = 77 K, gate bias V_{gp} = -5 V, V_{gn} = +5 V and forward current I_{pn} = 100 μA.* *44*

Chapter 4

Figure 4. 1 *Mask design for twin-gate devices.....48*

Figure 4. 2 *(a) Schematic cross-section of the devices. (b) Optical microscopy image of the finished device. 49*

Figure 4. 3 *The schematic of the measurement setup for the 2DHG and 2DHG channel. V_{tg} (V^{p}_{tg} or V^{n}_{tg} in text) and V_{sg} (V^{p}_{sg} or V^{n}_{sg} in text) are top gate and surface biases, respectively.....50*

Figure 4. 4 *Current – voltage characteristics of 2DEG and 2DHG with bias between two Ohmic V_{ds} = 500 mV at temperature of 4 K. Current – TG voltage characteristics of 2DHG with different SG voltages, -0.4 V (dashed line) and -0.6 V (solid line). The inset shows current – TG voltage characteristics of 2DEG.....51*

Figure 4. 5 *Current – voltage characteristics of 2DEG and 2DHG with bias between two Ohmic V_{ds} = 500 mV at temperature of 4 K. Current – SG voltage characteristics of 2DHG with different TG voltages, -0.8 V (solid line), -1.0 V (dot line), and -1.2 V (dashed line). The inset shows current – SG voltage characteristics of 2DEG channel.* *.....52*

Figure 4. 6 *Gate leakage currents versus top gate voltage. (a)I^{n}_{tg} and I^{n}_{sg} are leakage currents of n-type ohmic side top gate and surface gate. (b) I^{n}_{tg} and I^{n}_{sg} are leakage currents of p-type ohmic side top gate and surface gate.....53*

Figure 4. 7 *Linear and logarithmic current – voltage characteristics of the lateral 2-D p-i-n diode at temperature of 4 K with p-TG and n-TG biased at V^{p}_{tg} = -3 V and V^{n}_{tg} = +6 V, respectively, and p-SG and n-SG biased at V^{p}_{sg} = -0.6 V and V^{n}_{sg} = +0.9 V, respectively. V_{pn} is the operation voltage of the diode. The inset shows measurement configuration. 55*

Figure 4. 8 *Gate leakage currents versus the diode bias V_{pn} at temperature of 4 K with p-TG and n-TG biased at V^{p}_{tg} = -3 V and V^{n}_{tg} = +6 V, respectively, and p-SG and n-SG biased at V^{p}_{sg} = -0.6 V and V^{n}_{sg} = +0.9 V, respectively. V_{pn} is the operation voltage of the diode.. .....56*

Figure 4. 9 *Electroluminescence spectra of the lateral 2D p-i-n diode at temperature of 4 K with with p-TG and n-TG biasing at V^{p}_{tg} = -3 V and V^{n}_{tg} = +6 V, respectively and p-SG and n-SG biasing at V^{p}_{sg} = -0.6 V and V^{n}_{sg} = +0.9 V, respectively and V_{pn} from 1.6 V to 2.0 V with step 0.05 V. Inset shows photoluminescence spectrum at 4 K. 57*

Figure 4. 10 *Light integrated intensity versus forward bias voltage of the lateral 2D p-i-n diode measured at the same condition. Inset shows the light integrated intensity (black curve with triangle symbol) and external efficiency (blue curve with round symbol) versus the diode current. 58*

Chapter 5

Figure 5. 1 *(a) Schematic electrical connections. Electrons are pumped from left to right. (c) Potential profile during the pumping cycle (offset vertically): (i) loading, (ii) back-tunneling, (iii) trapping, and (iv) ejection.....61*

Figure 5. 2 *Schematic of a single-photon source driven by a single-electron pump device.....62*

Chapter 1

Introduction and motivation

1.1 Motivation

Most of the III-V optoelectronic devices rely on junctions formed by stacks of epilayers, where the electrical current flows across the junction vertical to the sample surface. The lateral p-n junctions that are difficult to fabricate, however, are often desirable for many device applications. For example, because of their coplanar geometry, they are suitable for optoelectronic integration. Since the cross section of the lateral junction is determined by the thickness of the epilayer, the capacitance of the junction can also be much smaller than that of conventional vertical ones. Thus, the 2D lateral junctions could lead to a new family of high-frequency and optoelectronic devices [1-6]. Furthermore, lateral 2D p-n junctions are potential candidates for investigating the properties of electron spins in low-dimensional systems by optical methods [7]. On the other hand, the lateral p-i-n junction is key component in a SAW-driven single photon source devices, proposed by Foden *et al* [8].

1.1.1 Spin Hall Effect

The spin Hall Effect (SHE) was predicted 40 years ago [9, 10]. Theorists Dyakonov and Perel proposed that an unpolarized electrical current should lead to a transverse spin current in systems with the relativistic spin–orbit coupling. In their picture, spin–orbit coupling enters SHE via the Mott scattering of electrons on unpolarized impurities, which results in spatial separation of electrons with opposite spins directions. The effect has Hall symmetry, because the polarization axis of the spin is perpendicular to the plane of the transverse spin current and the driving longitudinal electrical current. We can simply as in figure 1.1. The SHE consists in spin accumulation at the lateral boundaries of a current-carrying conductor, the spin directions being opposite at the opposing boundaries.

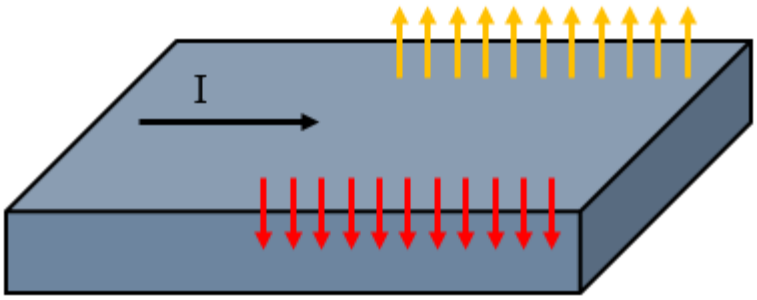


Figure 1.1. The Spin Hall Effect. An electrical current induces spin accumulation at the lateral boundaries of the sample. Spin-up electrons accumulate one side and spin-down electrons on the other side.

The term "Spin Hall Effect" was introduced by Hirsch in 1999 [11]. Indeed, it is somewhat similar to the conventional Hall Effect, where charges of opposite side accumulate at the different boundaries of the sample due to the Lorentz force, acting on moving charges in magnetic field. However, there are significant differences. First, no magnetic field is needed for spin accumulation. On the contrary, if a magnetic field perpendicular to the spin direction is applied, it will destroy the spin polarization. Second, the value of the spin polarization at the boundaries is limited by spin relaxation.

There are two distinct mechanisms of SHE, intrinsic [12, 13] and extrinsic [9-11, 14], which differ in the role played by external impurities. The extrinsic mechanism is caused by spin-orbit coupling between Bloch electrons and impurities, whereas the intrinsic mechanism is caused by spin-orbit coupling in the band structure of the semiconductor and survives in the limit of zero disorder. The intrinsic mechanism does not depend explicitly on impurities, but it would be a serious error to think that impurities can be ignored. The intrinsic SHE proposal focused on semiconductors and suggested that the optical activity of these materials be utilized for detecting SHE. In particular, the circularly polarized electroluminescence was suggested in reference [12] and the magneto-optical Kerr effect in references [12, 13]. These methods were used in the first measurements of the SHE phenomenon [7, 15].

Wunderlich *et al* in reference [7] used coplanar n – p - n diodes to detect circularly polarized electroluminescence at opposite edges of the spin Hall channel, see the figure 1.2 (a). When current (Up or Down direction) was injected into hole channel, spin accumulation occurred at the boundaries of hole channel. A p-n junction current was applied simultaneously. Electron will recombined with spin-polarized hole and emitted

polarized light. Dependence of Light polarization on current direction is shown in figure 1.2 (b). Wunderlich *et al*. ascribed the observed signal to the intrinsic SHE. However, impurities in their lateral diode were high, so the effect of impurities cannot be ignored. Therefore, it would be ideal to fabricate an impurity-free lateral p-i-n diode to investigate the intrinsic SHE.

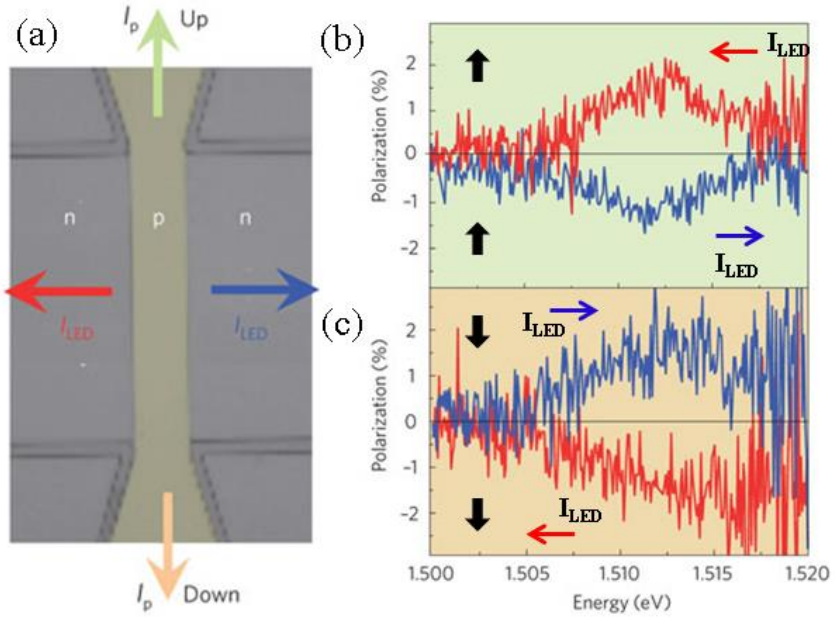


Figure 1.2. Wunderlich et al. a, Schematic of the lateral p–n junction with the channel current I_p and the diode current I_{LED} for detecting spin accumulation. b, Emitted light polarization of recombined light in the p–n junction for the channel and diode current flow indicated by arrows in (a).

1.1.2 SAW-driven Single photon Source

In recent years, explosive growth of the field of quantum-information science theory and metrology were the main driving forces behind the development of a novel technological tool [16, 17] - a controllable source of single photons on demand. Single photons on demand are an important resource in various areas of the emerging quantum technologies such as quantum key distribution [17-20] and all-optical quantum information processing [21]. They are the basic prerequisite for unconditional security in quantum key distribution protocols [20, 22-24] and a key ingredient for fault tolerant quantum computing schemes [18, 25, 26].

More recently, there has been an increasing interest in the surface acoustic wave (SAW)-driven single-photon sources owing to their potential applications in high-speed

quantum communications [8, 27, 28]. In [8], Foden *et al* proposed that when a SAW propagates through a two-dimensional (2D) p-i-n junction, see figure 1.3 (a), a series of traveling quantum dots are formed in the i-region of the junction. Consequently, a constant stream of electron packets, which can be manipulated by a controlled split gate voltage, flows from a two-dimensional electron gas (2DEG) channel into a two-dimensional hole gas (2DHG) channel, where electrons and holes are recombined to create bursts of optical pulses. By controlling the split gate voltage, one can obtain a stream of single electrons to generate single photons, see figure 1.3(b). In SAW-driven single-photon source devices, the key component is a high-quality 2D p-i-n junction.

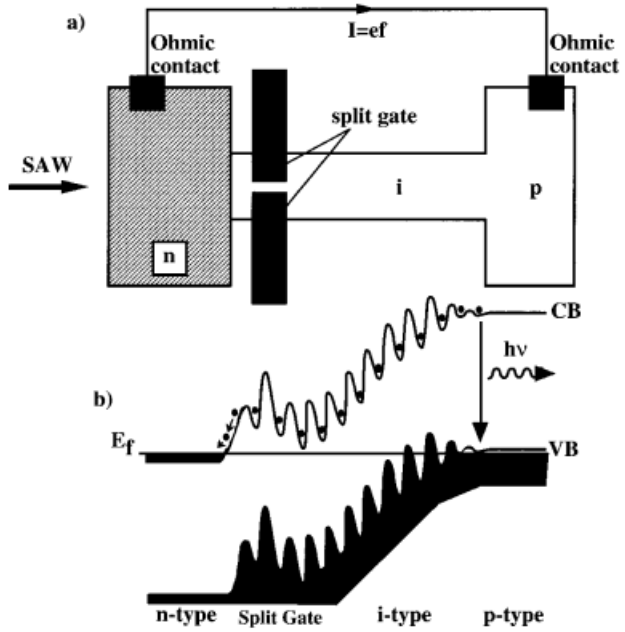


Figure 1.3 Foden et al. a, Schematic of the single-photon source. b, The conduction (CB) and valence-band (VB) edge profiles across the n-i-p junction and recombination when SAW wave propagate through.

1.2 Preview of Fabrication of Lateral p-n junction

1.2.1 Employing the Amphoteric Nature of the Si Dopants on GaAs

Silicon is widely used as an n-type dopant in GaAs growth by molecular beam epitaxy. However, silicon atoms can be incorporated as acceptors when the substrate is GaAs (nl1)A-oriented and n<=3 [29, 30] (The notation A or B is used to differentiate the atomic termination of the polar (N11) surfaces: A is Ga terminated and B is As terminated.).

Moreover, the conduction type can be controlled by adjusting substrate temperature and V/III flux ratio during the growth. Lateral p-n junctions formed at the intersection of different surface orientations can be obtained on the patterned substrates [27, 30-32]. The process to fabricate lateral p-n junction is as follows:

- A strips of photoresist was placed on (100) GaAs substrate surface along one of the <110> directions.
- The pattern was then etched with a crystallographic plane-selective etchant.
- A (100)-(n11)A-(100) step was created.
- Samples were cleaned and loaded into MBE system.
- Silicon-doped GaAs layer was regrown over the pattern substrate.
- A lateral p-n junction is created at the interface between the flat and etched planes see figure 1.4.

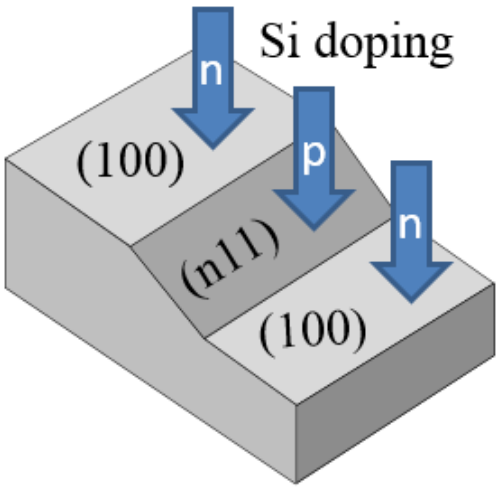


Figure 1.4 Fabrication of lateral p-n junction by employing the amphoteric nature of the Si dopants on GaAs. N-type doping on (100) surface and p-type doping on (n11) surface with n <= 3.

Base on this method, Gell *et al.* in references [27, 31] have fabricated a SAW-driven photoluminescence device. The authors have integrated a transducer into a lateral p-n junction, see figure 1.5. The transducer creates SAW wave. The SAW wave drives electrons through the junction. However, the device fabrication included regrowth process, many defects may occur. The electroluminescence is not very clear. Therefore, it is difficult to get further study toward single photon-devices.

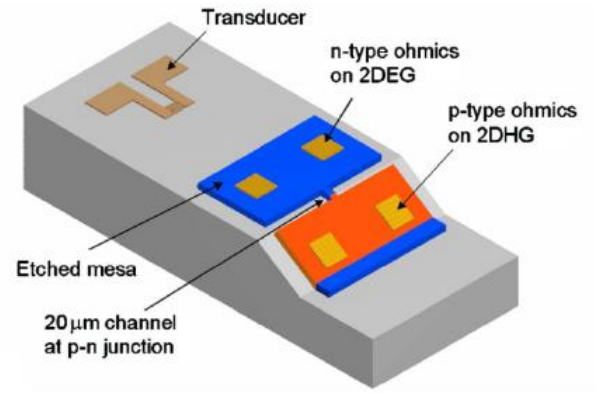


Figure 1.5 Gell et al. Schematic diagram of a device which integration of a SAW transducer with a lateral p-n junction.

1.2.2 n-type compensation doping of a p-doped heterostructure

In most cases many types of dopants will be present in the resultant doped semiconductor. If an equal number of donors and acceptors are present in the semiconductor, in this situation the dopants tend to cancel each other out and the semiconductor almost behaves intrinsically. This phenomenon is known as *compensation*, and occurs at the p-n junction in the vast majority of semiconductor devices. Reuter *et al.* in references [33, 34] have utilized n-type compensation doping of a p-doped heterostructure to realize two-dimensional p-n junctions. The base material for the junction fabrication was a p-modulation doped GaAs/$In_yGa_{1-y}As$/$Al_xGa_{1-x}As$ heterostructure which was fabricated by solid source molecular beam epitaxy. Compensation-doped silicon is carried out by using focused ion beam implantation. As a result, One side of AlGaAs layer is p-type doped and another side is n-type doped, as shown in figure 1.6. Therefore, 2DEG and 2DHG could be simultaneously formed in InGaAs quantum well. It means that two-dimension p-n junction was created. However, this method introduced high dopant in devices. In addition, implantation process also makes damage in the crystal. Therefore, non-radiative recombination is high. This is not suitable for application in single-photon source devices.

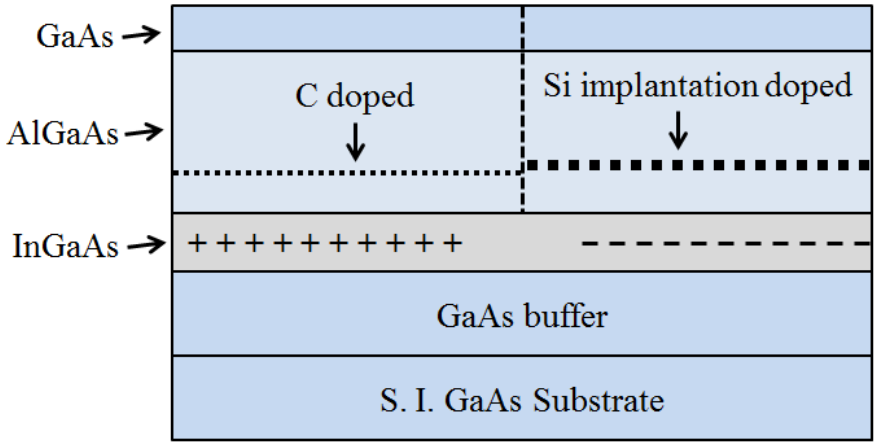


Figure1.6 Schematic presentation of a compensation n-type doping on p-type modulation doped heterostructures.

1.2.3 Partially Etching a Modulation Doped AlGaAs/GaAs Heterostructures

Kaestner *et al.* in ref. [35, 36] recently proposed a different design based on vertical p-i-n modulation-doping scheme in GaAs/AlGaAs heterostructures and showed very promising results. Figure 1.7 shows their schematic cross-section of junction design. In the as-grown state, the 2DEG is fully depleted such that the 2DHG is the only conducting layer. And part of the upper highly doped p-type material is removed by etching, the previously depleted 2DEG establishes at the lower interface. Thus, a junction between a 2DEG and a 2DHG can be created at the edge of an etched region. By removing doping impurities in the active layer their scheme is expected to lead to improved optical performance of the devices by drastically reducing the nonradiative recombination channels. Additionally the reduced dimensionality should lead to a further reduction in junction area.

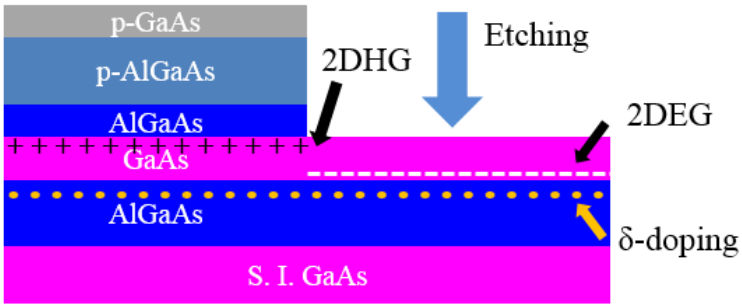


Figure1.7 Schematic cross-section of a quasi-lateral p-n junction formed by partially etching a modulation doped heterostructures.

However, because GaAs channel is very thin, surface depletion will strongly affect the density of carriers and luminescence efficiency in such a structure. In addition, since confinement and quantization are not good enough especially in forward bias, bulk signal still occurs in the electroluminescence spectrum. Although GaAs channel was undoped, but dopants still were very close to channel. Therefore, the electroluminescence was quite complicated.

1.2.4 Other Methods

Cecchini *et al.* [4] have proposed a fabrication scheme, which based on a p-type modulation-doped $Al_{0.5}Ga_{0.5}As$/GaAs heterostructure, see figure 1.8. First, p-type ohmic contact was deposition. And then the Be-doped $Al_{0.5}Ga_{0.5}As$ layer was completely removed from a portion of the mesa to obtain an intrinsic region within the QW. Following the etching procedure, n-type contact was deposited. The n-type contact introduces donors into the host semiconductor, creating an electron gas within the GaAs layer below the metal pad, adjacent to the 2DHG. This method is similar with one reported by Kaestner *et al.* [35, 36], except that the low bandgap channel was initially doped p-type via a doped high bandgap layer parallel to the surface. Both of these methods rely on accurate etching of the doped layers so that the channel itself is neither destroyed nor fully depleted after completion of the etching process.

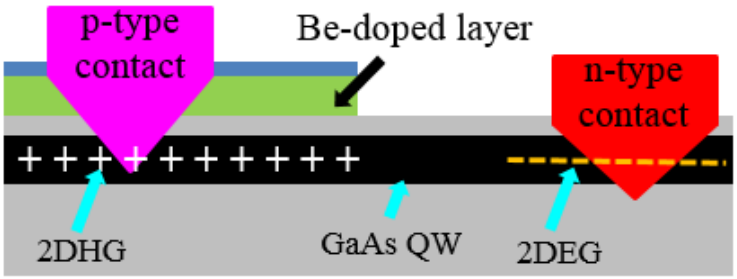


Figure 1.8 Fabrication scheme of a planar p-n junction proposed by Cecchini et al.

The authors in reference [37, 38] have utilized bevel etching technique to fabricating lateral p–i–n junctions, in similar structures to those described by Kaestner *et al.* [35, 36] and Cecchini *et al.* [4]. A schematic diagram of the InSb/$In_{0.85}Al_{0.15}Sb$ quantum well structure after etching is shown in figure 1.9. The levels of p and n doping and the layer thicknesses were chosen so that in the as-grown state the well is p-type everywhere. After bevel etching one end of the well remains p-type, as in the unetched structure, whereas around the point at which sufficient p-dopant is removed a region of the well becomes n-type, as shown schematically in figure 1.9. Current-voltage characteristics of the diode shows good rectify behavior. However, device's dimension is large and it is difficult to determine position of junction interface.

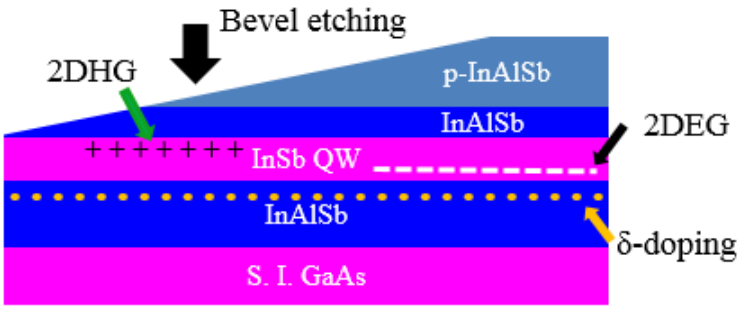


Figure 1.9 Schematic cross-section of a Lateral p-n junction created by bevel etching

In conclusion, a variety of different approaches for fabricating lateral junctions have been previously investigated by many groups. However, all these approaches used complicated techniques and/or required specialist equipment. In addition, highly doped structures were needed, so high non-radiative recombination is unavoidable. This is not suitable for application in single-photon source and intrinsic SHE study.

1.3 Our Approach

1.3.1 Induced 2DEG on an Undoped Heterostructure.

Modulation doping in MBE growth is an approved technique to reduce scattering from ionized dopants, by separating the two-dimensional electron gas (2DEG) from the (intentional) dopants by an undoped ‘‘spacer’’ layer. However, even with thick (80 nm) AlGaAs ‘‘spacer’’ layers, the Coulomb potential from the dopants still causes a randomly fluctuating background potential strong enough to cause significant scattering at low carrier densities (smaller than 10^{11} cm^{-2}). However, disorder due to this background potential can be dramatically reduced in undoped heterostructures where an external electric field electrostatically induces the 2DEG. Harrell et al. [39] have developed a technique for the fabrication of high-mobility electron gases formed in undoped GaAs/AlGaAs heterostructures, see figure 1.10 (a). Carrier density in the channel was manipulated by gate's bias. Figure 1.10 (b) reported the comparison between the mobility versus carrier density relationship of an induced 2DEG and that of a doped 2DEG with 80 nm-spacer layer. At high carrier densities, where the scattering is dominated by the unintentional background impurities and interface roughness, the mobility of the two devices is similar. However, as the carrier density is reduced the mobility of the doped device drops sharply, due to increased scattering from the rough background potential.

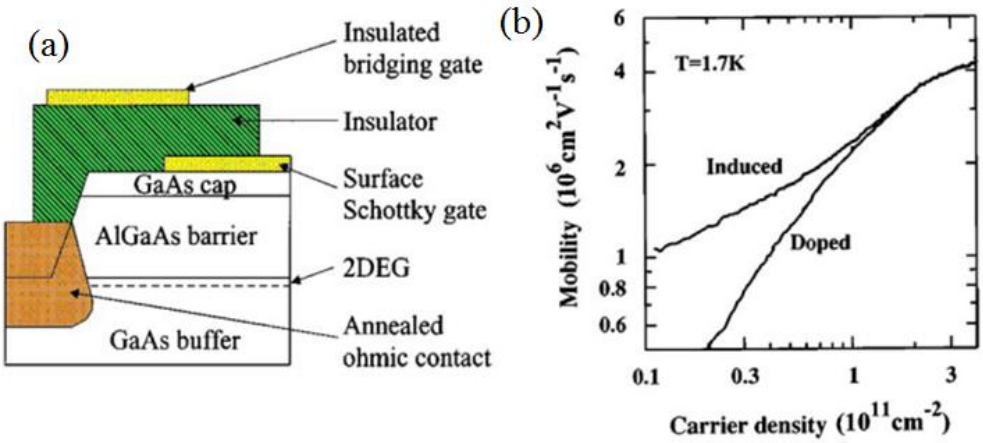


Figure 1.10 Harrell et al. (a) Schematic cross-section of a indeced 2DEG on undoped GaAs/AlGaAs heterostructure. (b) Comparison between the mobility versus carrier density relationship of an induced 2DEG and that of a doped 2DEG.

1.3.2 Lateral 2D p-i-n junction on an undoped heterostructure.

To employ the advantage of induced gas, we developed an induced lateral 2D p-i-n diode. The schematic cross-section of the device is shown in figure 1.11. The two different types of channels are induced via metal-insulator-semiconductor (MIS) gates. With a negative voltage applied on the p-gates and a positive voltage applied on the n-gates, both 2DHG and 2DEG channels can be induced in the GaAs quantum well, so a lateral 2-D p-i-n diode is created. 2DEG and 2DHG are induced in the left and the right side of the quantum well, respectively.

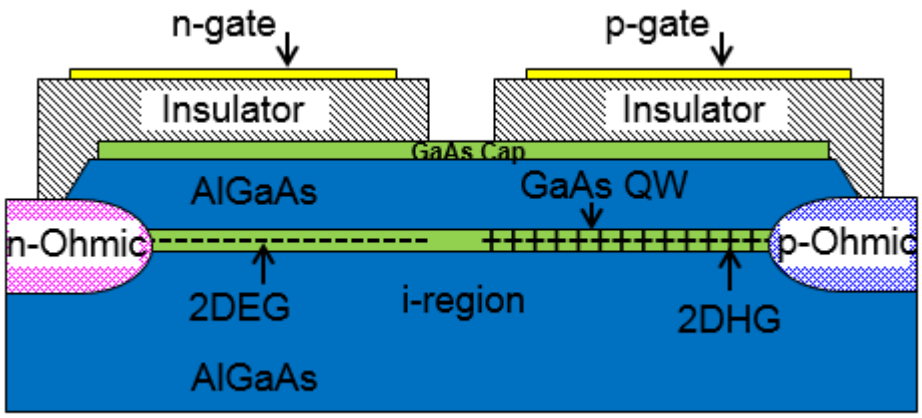


Figure 1.11 Schematic diagram of an induced lateral 2D p-i-n junction.

1.4 Contents of Thesis

In the previous sections, the motivations for developing a fabrication process to create a lateral 2D p-i-n junction in a totally undoped heterostructures have been detailed, and we also summary up-to-date, as we known, lateral p-n junction fabrication schemes. In chapter 2 fabrication process of a lateral 2D p-i-n junction will report in detail. Chapter 3 and chapter 4 contain mask design and experiment results from single-gate and twin-gate devices, respectively. Finally, conclusions from the work presented are given and the opportunities for further work are discussed.

Chapter 2

Device Fabrication Techniques

This chapter contains a description of fabrication techniques of an induced lateral p-i-n diode in a wholly undoped GaAs/AlGaAs quantum well. The device fabrication deals with the fabrication techniques used in processing the lateral p-i-n diode. These are cleaning, patterning, gate dielectric deposition, etching, and metallization. The fabrication process is summarized with illustrations to explain the sequence of fabrication. One set of devices deals with single top gate, whereas the second deals with twin gate (top and surface gates) design. A very brief overview of the fabrication is given to highlight the differences in design of the lateral 2D p-i-n diode. Further details of these differences are given in single and twin gate device chapters, respectively.

2.1 Basic Principle of Formation an Induced 2DEG

In general, the 2DEG (or 2DHG) can be electrostatically induced in GaAs/AlgaAs quantum well by an external electric field, which may be controlled via isolated gate or Schottky gate. The basic principles underlying the formation of an induced 2DEG (or 2DHG) are illustrated in figure 2.1. The device is analogous to a capacitor; one plate of the device is connected to ground and the other has a fixed voltage applied to it. In this device, see figure 2.1, a Schottky gate acts as one plate, the undoped AlGaAs as the dielectric and the quantum well as the other plate. Electron (hole) gas are induced in quantum well by the application of a positive (negative) voltage on the Schottky gate.

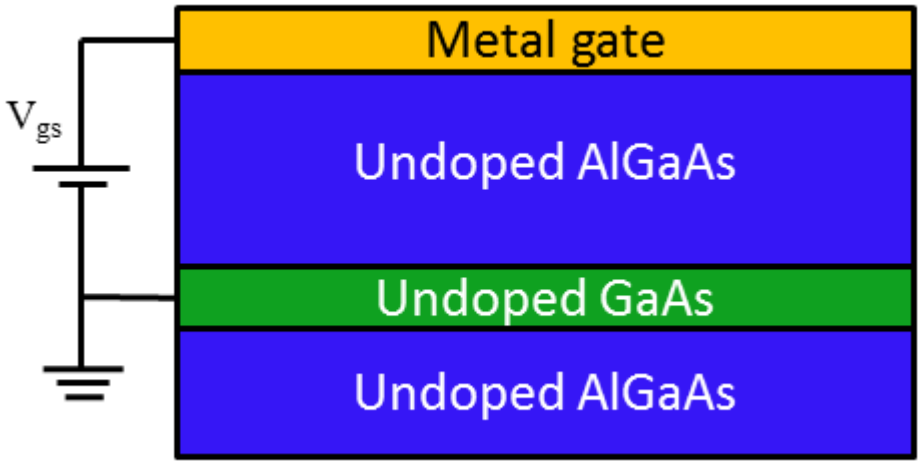


Figure 2.1 Schematic diagram of an induced gas

Figure 2.2 illustrates the formation of 2D gas in undoped GaAs/AlGaAs quantum well with assumed that there is no background doping or surface state. In unbiased condition, see figure 2.2 (a), Fermi energy is at the midgap energy. There is no extrinsic carrier in quantum well. The application of the external field causes an offset in the Fermi energy. When a sufficient positive voltage is applied to bring Fermi energy above the conduction band, and above the electron energy of ground state in quantum well, electrons are injected into quantum well from ohmic contact and a 2DEG will form, as shown in figure 2.2 (b). A 2DHG will create when an enough negative voltage is applied to take Fermi energy below the valence band, and below hole bound state energy in the quantum well, see figure 2.2 (c).

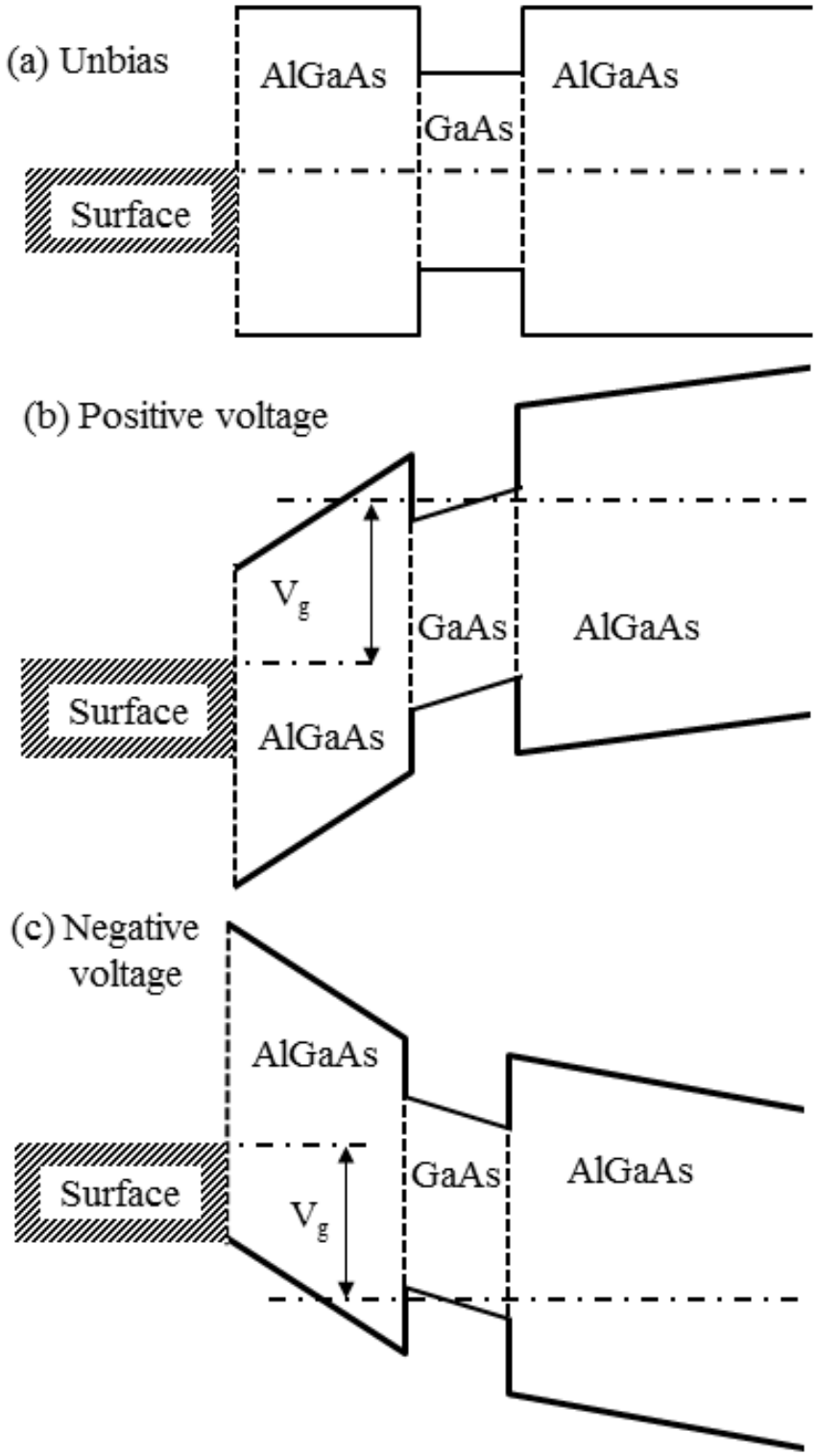


Figure 2.2 Band structure of an induced gas with assuming no surface state and background doping. (a), unbiased condition; Fermi energy is at the midgap energy. (b), positive voltage applied; Fermi energy is above the conduction band, a 2DEG will form. (c), negative voltage applied; Fermi energy is below the valence band, a 2DHG will be induced.

The ohmic contact and its relationship to the Schottky gate are decisive for fabrication of induced gas. Making contact to the gate is trivial but making contact to the channel while remaining isolation from the gate is very difficult. Figure 2.3 (a) demonstrates the typical "spike" profile of a diffused ohmic contact, as it is often assumed to be the case. In this case, there is separation between the ohmic contact and channel under the gate the potential cannot be defined and so the 2D gas will not form. However, if the diffusion profile can be developed as shown in the figure 2.2 (b) a 2D gas can be induced.

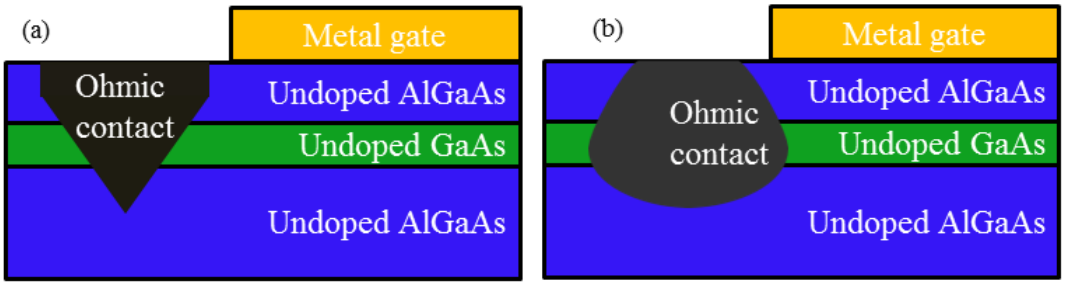


Figure 2.3 The ohmic contact diffusion profile. (a), a standard diffusion profile is shown; since this does not reach underneath the gate a 2D gas cannot be form. (b), the channel is contacted under the gate and so a 2D gas should create.

2.2 Device design

2.2.1 Sample Structure

The layer structure used for lateral junction fabrication is that of a GaAs/AlGaAs quantum well shown in figure 2.4. The sample was grown on a semi-insulating (100) GaAs substrate by using a solid-source MBE system. A 400 nm $Al_{0.33}Ga_{0.67}As$ was grown on top of a 100 nm GaAs buffer layer, followed by a 10-period GaAs/$Al_{0.33}Ga_{0.67}As$ (3 nm/3 nm) superlattice. A 20 nm GaAs quantum well between two $Al_{0.33}Ga_{0.67}As$ barriers was grown as the conductive channel of the device. Finally, the sample was capped with a 5 nm GaAs layer. All the layers were completely undoped. Here SL was grown in order to improve device quality of the active layer, such as internal quantum effiency, high carrier mobility [40-42]. These improvements have been attributed to the capture of impurities, which could originate from either the substrate or from the AlGaAs epilayers,

or to automatically smoothing effect by the growth of AlGaAs/GaAs superlattice [40, 43, 44].

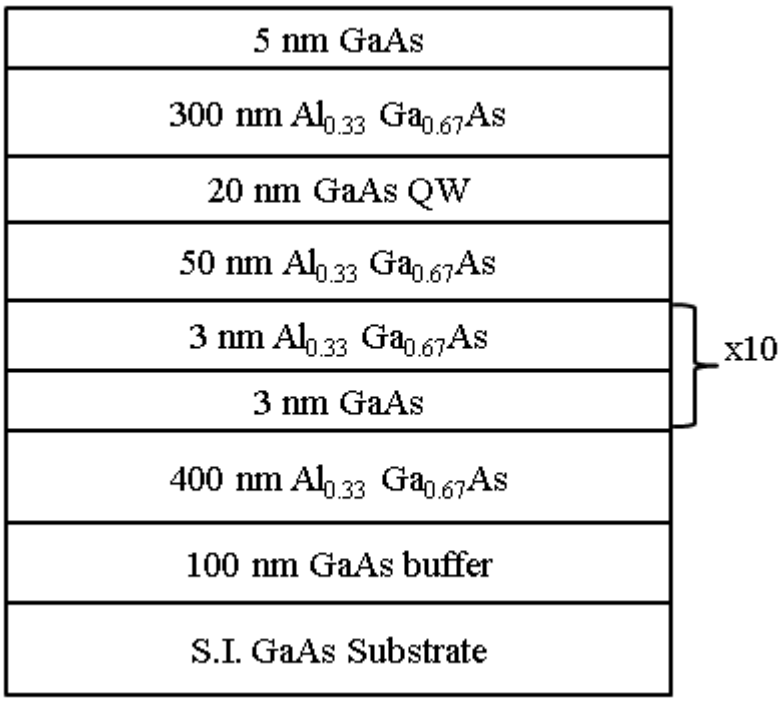


Figure 2.4 Schematic diagram showing GaAs/AlGaAs quantum well structure that was used to fabricate lateral p-i-n junctions.

2.2.2 Device design

The devices were fabricated in a completely undoped GaAs/AlGaAs quantum well which is described above. There are two designs for lateral 2D p-i-n junction, as shown in figure 2.5. In principle, two gates will induce 2DEG and 2DHG side by side in the quantum well under appropriate gate biases. Figure 2.5 (a) shows the schematic cross-section of the single-gate device design. There are two isolated gate, p-gate and n-gate, in this design. With a negative voltage applied on the p-gate and a positive voltage applied on the n-gate, both 2DEG and 2DHG channels can be induced in the GaAs quantum well, so a lateral 2D p-i-n diode is formed. 2DEG and 2DHG are induced in the left and the right side of the quantum well, respectively. The schematic cross-section of the twin-gate device design is displayed in figure 2.5 (b). In the twin-gate devices, each gas (2DEG or 2DHG)

is controlled by two gates, surface gate (SG) and top gate (TG). The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts. Surface gate, which is very close to the channel; provide a very good control for the carriers in the channel.

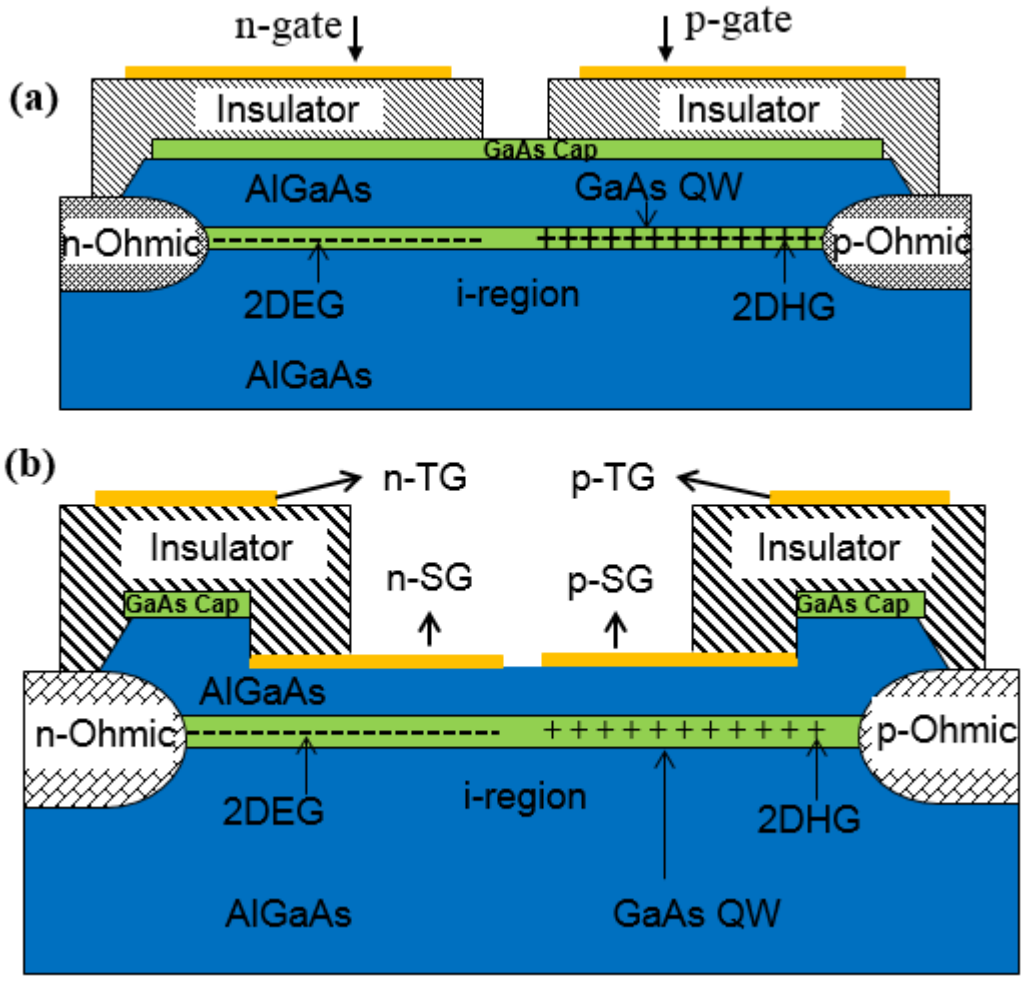


Figure 2.5 Schematic diagram of a lateral 2D p-i-n junction. (a), single-gate device. (b), twin-gate device.

2.3 Process Flow

The fabrication processing starts with sample cleaning, followed by wet etching to form the photolithography markers and device isolation patterns. And then the ohmic contact region was then defined and recessed down to the GaAs channel. Afterwards, the contact metal was deposited by E-gun evaporation and annealed in nitrogen gas. It further moves

on to explain the deposition of gate dielectric, formation of metal contacts and the subsequent lift off processes. Here similarities in fabrication process of all designs of the devices are highlighted. Finally, emphasis is given to explain the difference in design of single and twin gate devices.

2.3.1 Mesa Isolation

The process flow explains the sequence of device fabrication. Mesa isolation is carried out as the very first step after cleaning the substrate. In the Figure 2.6 (a) to (d) the processes are illustrated. Here cleaning of the sample and resist spinning are shown in (a), patterning of resist layer using mask aligner is presented in (b), wet etch of AlGaAs/GaAs using H_3PO_4:H_2O_2:H_2O = 3:1:50 solution shown in (c). Here red color has been used for positive photo-resist Az6112 and the white pattern represents developed resist layer as shown in (b). Green layer is 20 nm-GaAs layer and gray layer is AlGAsAs layer. Finally in (d) the resist layer is removed.

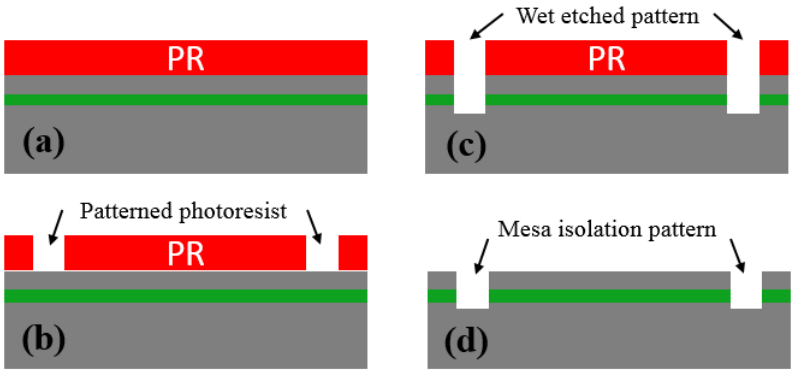


Figure 2.6 Mesa isolation process

2.3.2 Contact Metallization and Thermal Diffusion

Contact's metal deposition and diffusion are shown in figure 2.7. Here red color has been used for positive photo-resist Az6112. After mesa isolation, sample was pattern for selective p and n metal deposition in two separate steps. Each deposition processes (figure (a) to (e) refer to p-type deposition and (f) to (k) refer to n-type deposition) was followed by rapid thermal annealing in pure nitrogen gas to diffuse dopant into quantum well channel. Here in figure 2.7 (k) the cross-section of device isolation patterns, p-type and n-

type metals regions are shown. The solid fill blue and purple colors are corresponding for p- and n- metallization regions. These regions serve as p and n contacts of the diode.

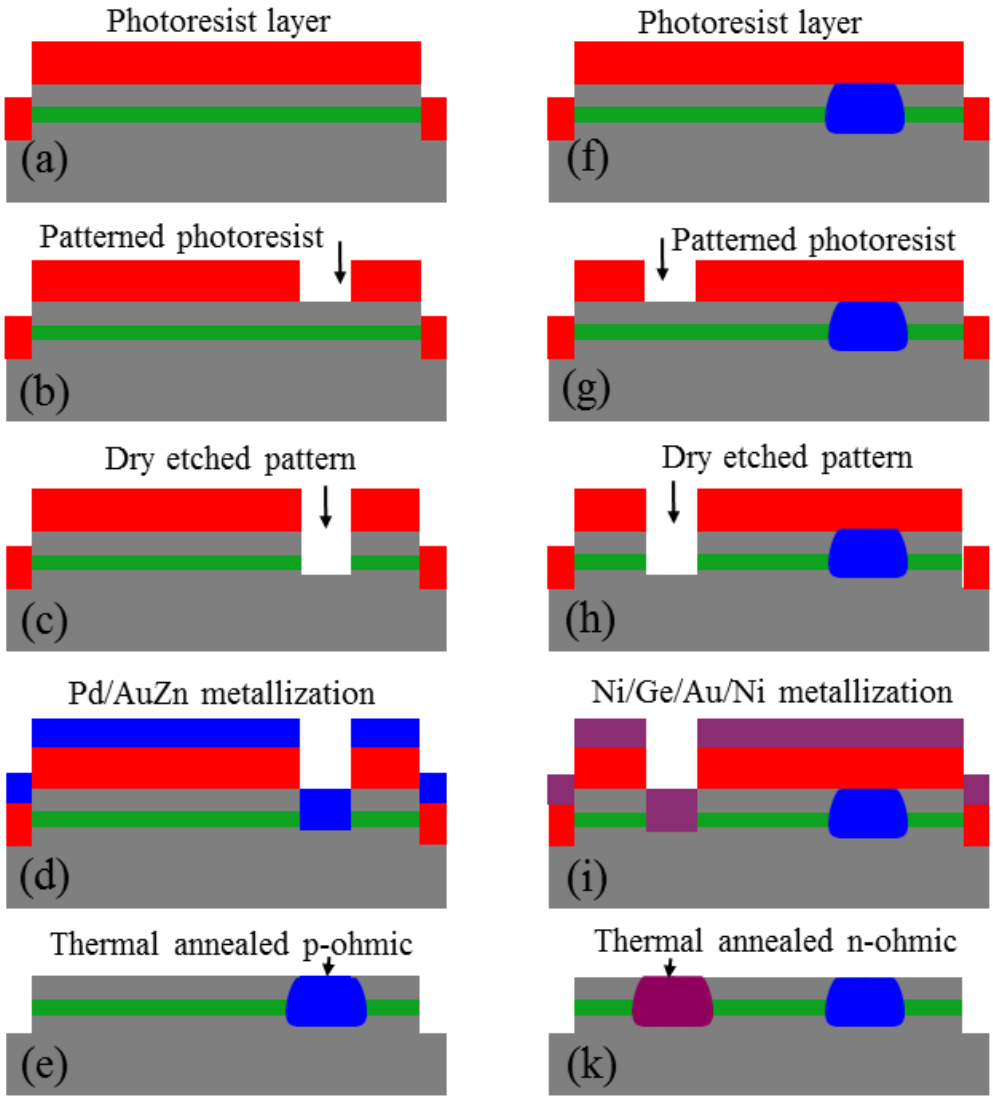


Figure 2.7 p-type and n-type contact metallization

2.3.3 Single-Gate Devices

Following the contact's metallization process, a photosensitive polyimide insulator (SU-8 2000.5, HD Microsystems) was then coated and patterned on the surface and cured for 30 mins at 200 ^{o}C in nitrogen, which gave a thickness of about 350 nm, as shown in figure 2.8 (a) – (b). And then, the metal Ti/Au (20 nm/100 nm) was deposited on top of the

polyimide layer to form the gate by E-gun evaporator, see figure 2.8 (c) – (g). Finally, the sample was processed for lift-off in acetone (figure 2.8(f)). Here diagonal line pattern area is illustrated for photosensitive polyimide. The dark yellow color has been used the insulated gate.

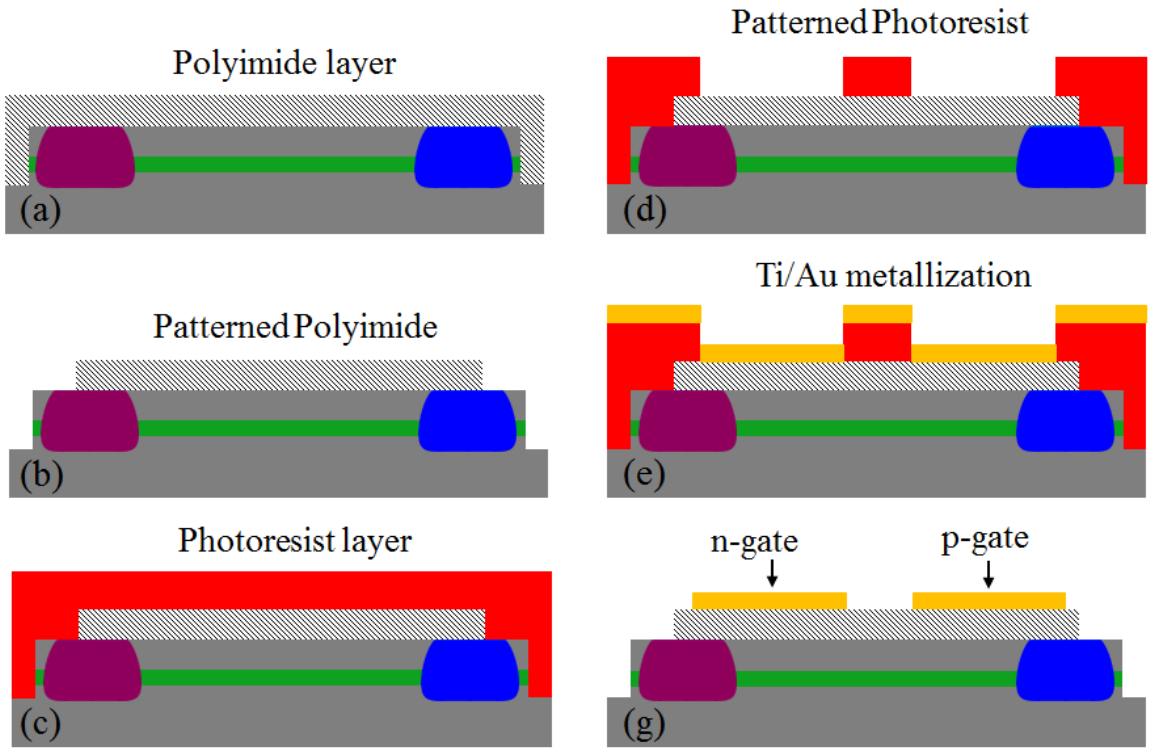


Figure 2.8 Fabrication steps of single-gate devices

2.3.4 Twin-Gate Devices

The initial fabrication process for the twin-gate devices follows the same steps as explained above up to the figure 2.7 (k). Recess surface gate processes are shown in figure 2.9 (a) to (d). The recess depth is 150 nm. Figure 2.9 (e) to (f) and (g) to (i) are illustrated fabrication process for polyimide insulator and top gate, respectively. These processes are the same as for single-gate devices. It is to be note that one part of top gate is overlap with ohmic contact and some other is overlap with surface gate, as shown in figure 2.9 (i). Here diagonal line pattern area is also illustrated for photosensitive polyimide. The top gates and surface gates both are presented by dark yellow color.

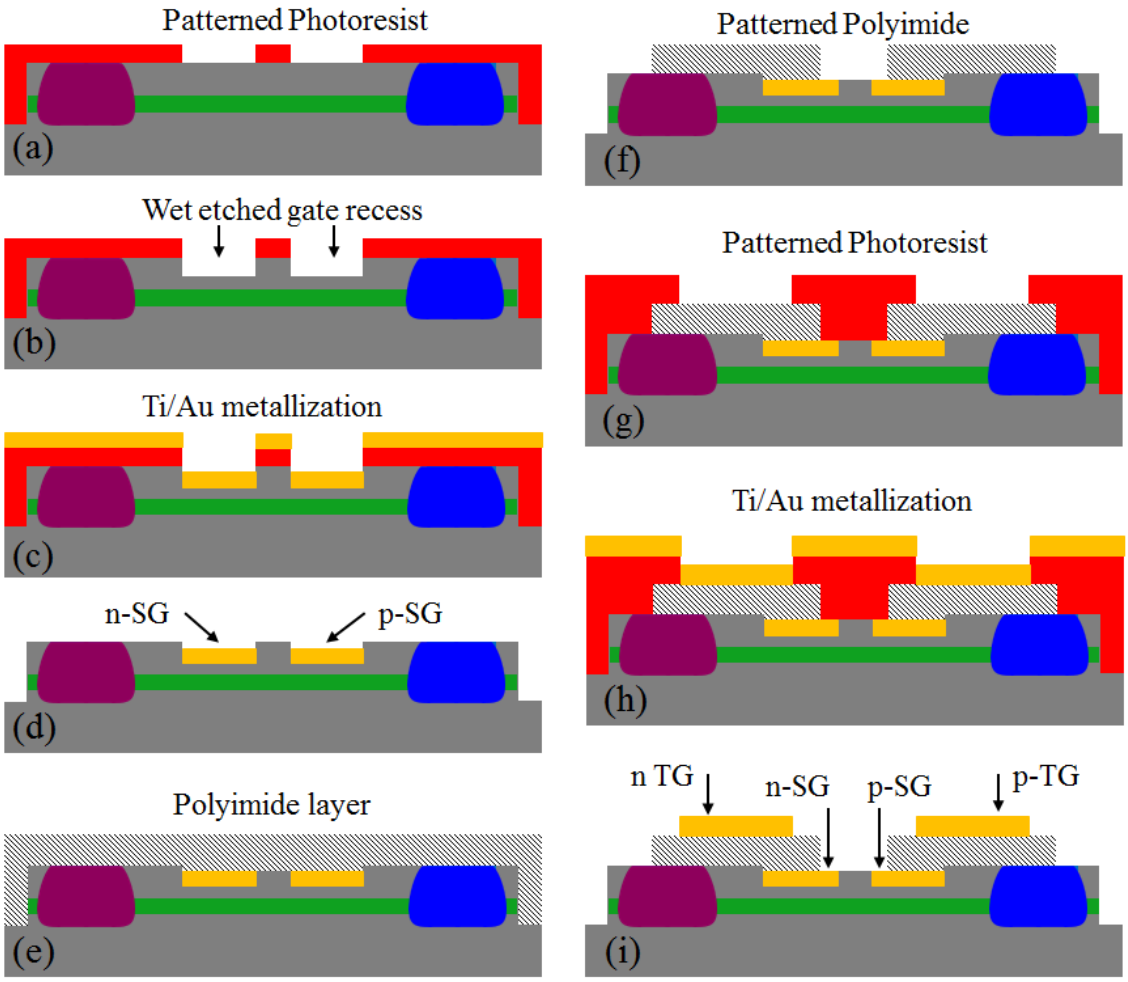


Figure 2.9 Fabrication steps of the twin-gate devices

2.4 Fabrication Procedures

In the earlier sections, fabrication steps are described, whereas in this section details of the processes and critical factors affecting the fabrication process are given.

2.4.1 Sample Cleaning

The surface cleaning of GaAs and other semiconductors involves two different aspects. The first is the removal of contaminants, such as organic compounds and metal ions. The

second is the removal of the native oxide to expose the bare semiconductor for subsequent processing such as metal contact deposition.

Device substrates require proper cleaning to remove contaminants and residues from prior process steps. Dust particles may also get on to substrates because of the sample cleaving process. There are always some organic vapors in the air of a clean room, and a wafer that has been exposed to them for even a moderate amount of time can become contaminated. Particulates can also arise as a result of certain fabrication processes, e.g. wet etching, dry etching, or metallization. Improper cleaning during fabrication processes may result in unwanted residue for the following fabrication step.

Substrate cleaning is performed using cleaning solutions i.e. acetone and isopropanol alcohol (IPA) in a proper order. Initially, the sample is soaked in acetone to remove oil and grease particles. As acetone has a very high evaporation rate, so the substrate might be left with a layer of contaminated acetone and therefore it requires a rinse in IPA, which is a powerful solvent for contaminated acetone. During each cleaning step, the sample is placed in a cleaning solvent such as acetone; in an ultrasonic bath for three minutes. Finally the substrate is rinsed in D.I water and is dried with a stream of nitrogen gas.

All the III–V semiconductors are readily oxidized by atmospheric oxygen, so the surface of GaAs and other compound semiconductors that have been exposed to air will be covered by a thin layer of native oxide. This is typically of the order of 1–2 nm after long-term air exposure. Immersion in either acidic or basic dilute solutions will dissolve the native oxide. In our some processes such as surface gate, ohmic contact fabrication, addition cleaning step is required to remove native oxide. The sample is dipped in an 1:10 HCl:H_2O solution in 30s to remove the oxide layer. The HCl/H_2O solution will also assist in the removal of organic and metallic impurities. So it also helps to improve the sample surface quality for subsequent processing.

2.4.2 Photolithography

Photolithography is the process of transferring geometric shapes on a mask to a light-sensitive chemical, called photoresist, on the surface of a wafer. The tone of the photo-resist may be either positive or negative. Use of the photo-resist mainly depends upon the

mask used to transfer the pattern and the limitation of the fabrication process. Furthermore, positive and negative photo-resists are used for dark field and light field masks, respectively. During the fabrication of these devices, we use Az 6112 and Az 5214E photoresist. Az 6112 is positive photoresist, so it is suitable for dry etch process. Az 5214E has image reversal capability, thus it is suitable for processes that require lift-off.

**** Positive photoresist***

In positive photoresist, exposure to the UV light changes the chemical structure of the photoresist so that it becomes more soluble in the developer. Therefore, exposed resist is washed away in developer solution and unexposed resist remains on the wafer.

**** Negative photoresist***

In contracts to positive photoresist, exposure to the UV light causes the negative resist to become polymerized, and more difficult to dissolve. As a result, exposed resist stays and the rest of the resist get dissolved in the developer solution. Figure 2.10 Shows development of positive and negative photoresists.

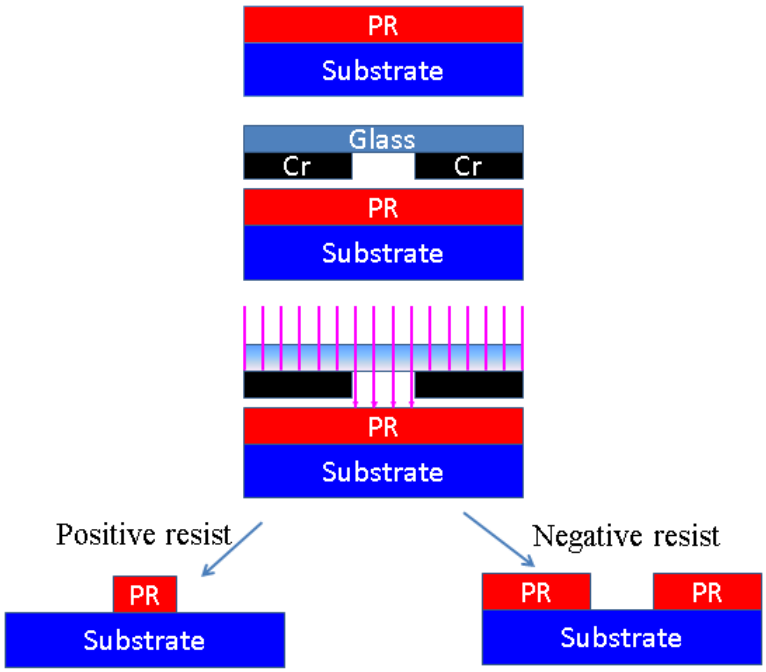


Figure 2.10 Development of positive and negative photoresist

**** Photolithography process***

A typical photolithography process consists of resist coating, mask alignment, exposure, and development.

- Resist coating: The wafer is covered with photoresist by spin coater. A viscous, liquid solution of photoresist is dispensed onto the wafer, and the wafer is spun rapidly to produce a uniformly thick layer. Thickness of the thin resist layer is a function of spin speed [ ].
- Mask alignment and exposure: Device fabrication involves multiple photolithography exposures. Therefore, alignment accuracy is important parameter for photolithography. Alignment markers are used to expose the mask pattern exactly over the substrate pattern. One the mask pattern is aligned to the substrate design, the photoresist is exposed to high intensity UV light for a specific time.
- Development: After exposure to UV light, sample was dipped in developer solution in a particular time.

In our processes, we used both negative (Az 5214E) and positive (AZ 6112) photoresist. The photolithography process of Az 5214E is as follows:

- Resist coating: a small amount of Az 5214E is applied on sample surface. Substrate is rotated at 1000 rpm in 10 s and then at 6000 rpm in 45 s.
- Hard bake: sample is baked at 90 ^{0}C in 90 s. Thickness of the photoresist layer after baking is about 1300 nm.
- Exposure: After mask alignment, sample is exposed for 2.8 s.
- Reversal bake: 120 seconds at 120 ^{0}C in nitrogen-flow oven. This is the most critical step.
- Flood exposure: 120 seconds
- Development: Sample is dipped in Az300 developer solution for 40 s, and then rinsed in D. I. water in 2 minutes.
- Post bake: sample is baked at 120 ^{0}C in 120 seconds. This step is optional. The post bake solidifies the remaining photoresist, to make a more durable protecting layer in future processes such as, wet etch, dry etch. It also improves adhesion of the photoresist to the wafer surface, this will reduce undercut in wet etching.

The photolithography process of Az 6112 is as follows:

- Resist coating: Substrate is rotated at 1000 rpm in 10 s and then at 6000 rpm in 45 s.

- Hard bake: sample is baked at 90 ^{0}C in 90 seconds. Thickness of the photoresist layer after baking is about 1200 nm.
- Exposure: After mask alignment, sample is exposed for 2.4 s.
- Post exposure bake: 90 ^{0}C in 60 seconds.
- Development: Sample is dipped in Az300 developer solution for 40 s, and then rinsed in D. I. water in 2 minutes.
- Post bake: sample is baked at 90 ^{0}C in 90s. This step is also optional, as the case of Az5214E photoresist.
-

2.4.3 Wet Etching and Dry Etching

Since most of III-V devices require the exposure of buried layers for metal contact formation and/or the formation of mesa isolation, etching will always be a critical part of their fabrication. There are two etching methods: wet etch and dry etch.

Wet etching is a material removal process that uses liquid chemicals or etchants to remove materials from a wafer. The specific patterns are defined by masks on the wafer. Materials that are not protected by the masks are etched away by liquid chemicals. The mechanism for most of wet etching of GaAs is the oxidation of surface to form Ga and As oxides, and then these oxides are dissolved by liquid chemicals with bases or acids [45].

In dry etching, plasmas or etchant gasses remove the substrate material. The reaction that takes place can be done utilizing high kinetic energy of particle beams, chemical reaction or a combination of both [45]. Both approaches have their own advantages and disadvantages. Table 2 shows the comparison of wet and dry etching.

Table 2.1 Comparison between wet and dry etching

	Wet etching	**Dry etching**
Method	Chemical solutions	Ion Bombardment or Chemical reactive
Environment and Equipment	Atmosphere, bath	Vacuum Chamber

Advantages	- Low cost, easy to implement - No surface electric damage - Many chemistry choices - Good selectivity for most materials	- Good dimensional control - Excellent profile control: vertical to controlled angle
Disadvantages	- Limited dimensional control - Potential of chemical handling hazards - Wafer contaminations issues - Vertical profile hard to get	- Ion-induced surface damage - Limit number of chemistries - Resist erosion can limit depth - Hazardous reactant gases - Expensive hardware
Directionality	- Isotropic (Except for etching Crystalline materials)	anisotropic

In mesa isolation process and surface gate recess etching, wet etching was used. To shadow etch AlGaAs and GaAs, the phosphoric acid family of etchants are prefer because they product smooth surfaces and can provide control of etch depths at level of tens of angstroms [46]. In addition, a good non-selective etch for AlGaAs is H_3PO_4:H_2O_2:H_2O with a 3:1:50 ratio. This chemistry etchs AlGaAs and GaAs at nearly equal rates of approximately 1.8 nm/s. It is important to note that etching solution can change composition with passage of time, with a resulting change in their associated etch rates. In general, etching rate reduces with time. In H_3PO_4:H_2O_2:H_2O system, etching rate varies if the solution is used too soon after it is mixed. After thermal equilibrium (around one hour), no change in etch rate is observed in next one week [45]. To reproducible process, it needs to note the age of the solution.

Fabrication of the ohmic contact is the critical step in our processes. Our device structure is totally undoped, so ohmic dopant need to lateral diffuse into channel to form self-align structure, as have explained above. Therefore controlling etching profile of the ohmic contact is important. To get vertical sidewall profile, dry etching was used. Dry etch processes can provide excellent profile control. The energetic ion bombardment increases the etch rate on the exposed surface relative to those regions protected by the

mask, so vertical sidewalls with negligible undercutting are readily achieved. But in dry etching, the ion bombardment so essential to achieve this advantage simultaneously damages the near-surface region of wafer. To reduce degradation of electronic properties, we use an inductively coupled plasma (ICP) RIE system. This system uses two separate power supplies with one (ICP power) generating the plasma and the second one providing the RF power that controls the ion bombardment energy.

The ICP-RIE system provides semi-independent control of the plasma chemical species, both ions and neutrals, and the energy with which the ions hit the wafer surface. Control over damage can be achieved by low ion energy (i.e., low RF power). Our dry etch process was done as follow:

- Sample with pattern photoresist on the surface was dipped in 1:10 HCl:H_2O solution in 30 s to remove oxide layer on sample's surface.
- Sample was loaded into reaction chamber via a load locker chamber.
- Sample surface was treated by Oxygen plasma in 5 s at 20 mTorr background chamber pressure and RF power of 60 W to remove residual photoresist.
- GaAs/AlGaAs etching process was performed in chamber with $SiCl_4$:Ar gas mixture in the ratio of 24:4 standard cm^3 per minute (sccm), RF power of 30 W, ICP power of 350 W. The entire process was carried out at 1.5 mTorr background chamber pressure. Standard etching rate for this receipt is 6.6 nm per second.

It is worth to note that remove of surface oxide layer will improve repeatable factor for dry etching, especially in shadow etch such as our case. And oxygen plasma treatment will make etched surface smoother, particularly in the edge of photoresist pattern. Figure 2.11 shows comparison between dry etch with and without oxygen plasma treatment. Scanning electron micrograph of samples before and after dry etch without oxygen plasma treatment are shown in figure 2.11 (a) and (b). We can clearly see in the figure 2.11 (a) that residual photoresist still remain between photoresist mask and exposure region. These photoresist cause surface roughness on sample after dry etch, as shown in figure 2.11 (b). This may further produces spikes in ohmic metal and then leakage between ohmic contact and top gate occurs. In the contract, with oxygen plasma treatment sample surface become clean and smooth, as shown in figure 2.11 (c) and (d).

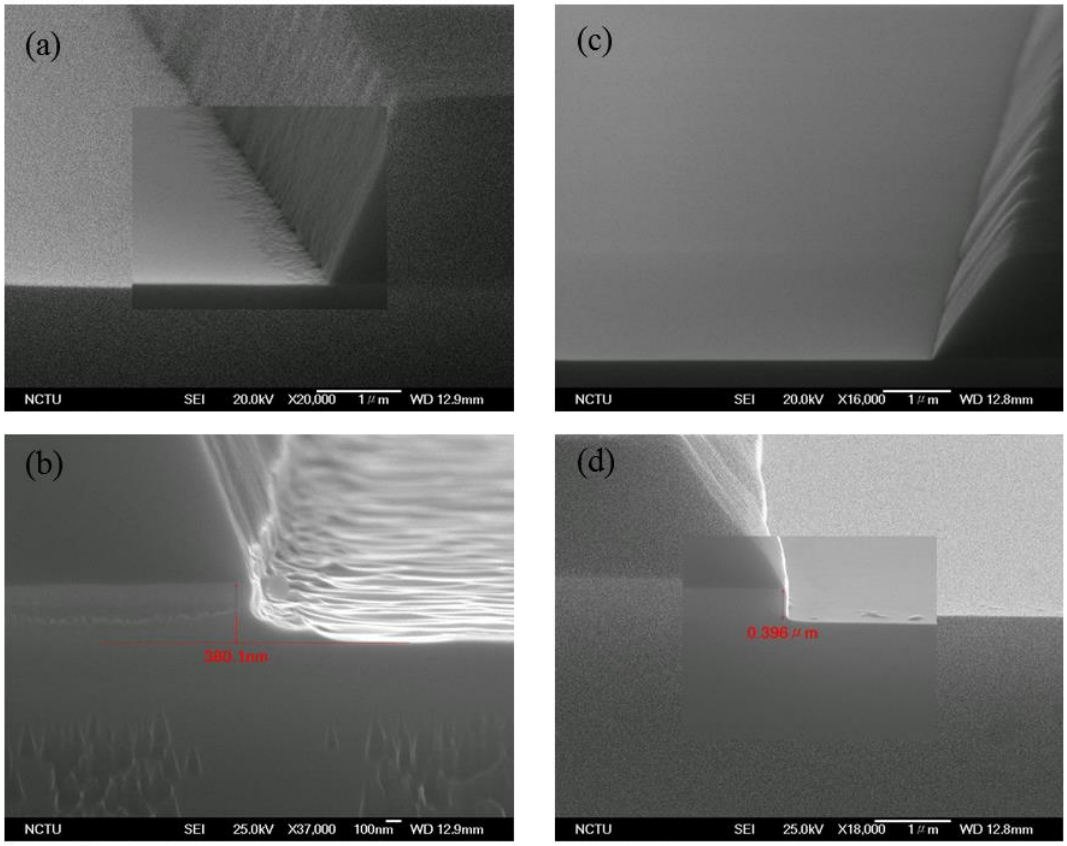


Figure 2.11 Comparison of dry etching with and without O_2 plasma treatment

2.4.4 Ohmic Contact Metallization

Metals and semiconductors come into close contact, and physical or chemical bonds are formed at an interface between them. Such contacts are of two generic types, Schottky and ohmic. Ohmic contacts are those that follow Ohm's law that current increases linearly with applied voltage. Therefore, in ohmic contacts a low barrier to current conduction exists at the metal/semiconductor interface. Almost metal/semiconductor interfaces have barriers to mobile carrier. The key to making an ohmic contact is to design these barriers to be low enough that current can cross the interface by thermionic emission or to be narrow enough that current can cross the interface by field emission.

Most of the n-ohmic contact to GaAs seems to follow the broad outlines of general mechanism. The metallurgy of n-ohmic contact formation to GaAs will include some or all following steps [45]:

- An element of the contact reacts with the GaAs native oxide.

- An element of the contact reacts with GaAs at low temperature to form a X-GaAs complex.
- An element of contact diffuses into GaAs mediated by defects creates in step 2 and dopes GaAs.
- An element of the contact diffuses into GaAs and forms a low bandgap semiconductor phase.
- Ga outdiffuses from the contact and reacts, usually with Au.
- Elements of the contact react and form their thermodynamically preferred compounds.
- As diffuses from the GaAs to the contact surface where it vaporizes or resides.

GaAs/Ge/Au/Ni is the most common used contact and is n-type ohmic contact. As describe above, first the Ni reacts with the native oxide. Because the native oxide may vary unrepeatably due to variation in processing, therefore contact with the Ni will improve contact morphology. And the Ni also forms intermediate complexes with GaAs. The important role of intermediate complexes is to disturb the crystal lattice to make way for diffusion of other atoms and further reactions. The Ge is diffused into GaAs and acts as dopant. Normally, diffusion of dopants such as Ge into the GaAs requires a subtitutional-interstitial mechanism where the Ge can diffuse along interstitial sites until it finds a vacancy in the GaAs lattice. This type of mechanism has high activation energy and normally occurs at temperatures of 600^0C and above. In a GaAs ohmic contact, the diffusion process is thought to take place at much lower temperatures because of the driving forces of the Ni-GaAs complex formation and the driving force of the next reaction which further disturbs the crystal lattice. The diffusion of Ge into GaAs can occur at temperature between 100^0C and 400^0C.

The metallurgical reactions shown above are mostly applicable to p-type contacts and mainly need to be modified by the choice of elements needed for doping the GaAs. GaAs/AuZn [47] is one of the most commonly utilized p-type contacts. In this contact, the Au provides the role of a lattice disrupting element. No surface oxide reacting element is present, so the methods of surface preparation are critical. The Zn takes a role as p-type dopant in GaAs.

In fabricating device, ohmic metal is deposited by E-gun evaporator at vacuum pressure $2*10^{-6}$ mTorr. This machine works with electron beam sources, to vaporize the metal. After dry etching, sample was dipped in 1:10 HCL:H_2O solution to clean sample's surface and remove oxide layer. And then samples were loaded into E-gun evaporator

immediately. The metallization receipt for p-type contact was Pd (40 nm) / AuZn (120 nm). The Pd not only increases adhesion of contact on GaAs surface but also improve contact's morphology. The metallization receipt for n-type contact was Ni (5 nm) / Ge (70 nm) / Au (70 nm) / Ni (35 nm). The thin Ni layer is deposited first to improve surface smoothness [45, 48]. It is worth to note that deposition rate should keep stable at reasonable rate. If the rate is too high, surface morphology of contact metal will become bad. This will lead to high leakage current between the contact and gate. If the rate is too low, photoresist will expose in metal vapor too long. It will be difficult to properly lift-off.

2.4.5 Lift-off and Thermal Annealing

Lift-off is a process to remove unwanted metal after metal deposition. Lift-off is normally done by placing the sample in acetone for 20-30 minutes, the pattern photoresist is dissolved, and then unwanted metal is wept away. In our ohmic contact process, it is required no undercut in photoresist. Positive photoresist was used. It is possible that some unwanted metal still remain in the edge photoresist, so spikes may occur at the edge of metal contact after normal lift-off process. Therefore, the sample is placed in acetone in an ultrasonic bath for 1 minute after lift-off process to remove any possible spikes.

Samples were annealed afterward in Nitrogen gas. Figure 2.12 shows annealing profile for the ohmic. Temperature rising time is 20 seconds. p-type and n-type ohmic contacts were annealed at 420 ^{0}C and 450 ^{0}C for 2 minutes, respectively. Heater is turned off afterward. Temperature of sample slowly decreases to the room temperature.

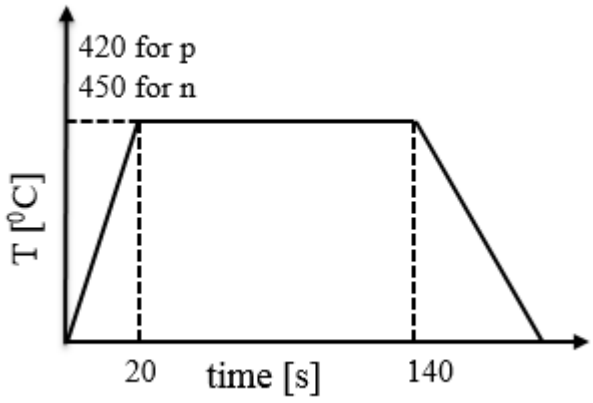


Figure 2.12 Thermal annealing ohmic contact program

Here, p-type ohmic was annealed before any further processes. This will improve yield of p-type ohmic contact. It also worth to note that sample were annealed immediately after n-type metal lift-off since any delay can lead to oxidization of the exposed Ni layer which form a rough, black deposit around the edge of the ohmic and lead to leakage.

2.4.6 Dielectric Layer Deposition

Photosensitive polyimide, Su-8 2000.5 [49], were used as an insulator layer in our devices. Su-8 2000.5 is a high contrast, epoxy based photoresist. And it is negative photoresist. Physical properties of the polyimide [49] is shown in the below table.

Table 2.2 Physical properties of polyimide

Adhesion Strength (mPa) Silicon/Glass/Glass & HMDS	38/35/35
Glass Transition Temperature (Tg °C), tan δ peak	210
Thermal Stability (°C @ 5% wt. loss)	315
Thermal Conductivity (W/mK)	0.3
Coefficient of Thermal Expansion (CTE ppm)	52
Tensile Strength (Mpa)	60
Elongation at break (εb %)	6.5
Young's Modulus (Gpa)	2.0
Dielectric Constant @ 10MHz	3.2
Water Absorption (% 85^0C/85 RH)	0.65

The polyimide process is very sensitive to humidity. Therefore, the process should be done at low humidity (below 50%). If not, polyimide does not properly form continuous film. This will result in leakage current between gates and ohmic contacts. Polyimide deposition and pattern processes were done as follows:

- Resist coating: Substrate is rotated at 500 rpm in 10 s and then at 3000 rpm in 40 s.
- Hard bake: sample is baked at 90^0C in 60 s. Thickness of the photoresist layer after baking is about 500 nm.
- Exposure: After mask alignment, sample is exposed for 5 s.

- Post exposure bake: 90^0C in 90 s.
- Development: Sample is dipped in SU-8 developer solution for 45 s, and then dipped in isopropyl alcohol (IPA) in 10 s.

Su-8 2000.5 has good mechanical properties. However, our devices need to be cooled down to low temperature. Therefore, after polyimide patterning curing process (hard bake) was done. The hard bake step is also useful for annealing any surface cracks that may be evident after development. Sample was loaded into a furnace where Nitrogen gas continuously flows. Figure 2.13 shows polyimide curing program. To reduce possibility of bubble in polyimide and crack in metal/polyimide interface, temperature of the furnace increased with low rate of 1 ^{0}C/min. And then the furnace temperature remained at 200 ^{0}C in 30 mins. Afterward temperature will decrease with rate of 1 ^{0}C/min. Final thickness of polyimide layer is approximately 350 nm.

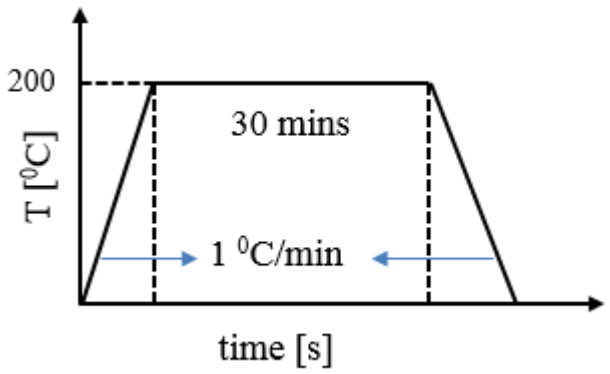


Figure 2.13 Polyimide curing program

2.4.7 Gate Metallization

**** Surface gate (Schottky contact)***

Schottky contact is the term used to describe metal/semiconductor interfaces that display rectifying or diode-like behaviour. In our twin-gate devices, we use recessed-gate structure. Fabrication of the recessed-gate was processed as follows:

- AZ 5214E was deposited and patterned on wafer surface.
- Prior to the recess etch, a surface treatment was done: sample is placed in oxygen plasma for 5 s to remove monolayers or less of organic material that remains after the

resist development process. And then sample was dipped into 1:10 HCl:H_2O for 30 s to remove oxide layer. The surface treatment will make the GaAs surface to wet with chemical etchant promptly, to start the etching without any time delay and to etch at the rate expected without roughening. Therefore, etched surface will be smooth; this is good for subsequent processes.

- Sample was etched down 150 nm by 1:3:50 H_2O_2:H_3PO_4:H_2O solution. As a result, the channel is 150 nm below the surface.
- Sample is immediately loaded into E-gun evaporator chamber. 20 nm/80 nm Ti/Au was afterward deposited.
- Lift-off process.

**** Top gate***

Top gate metal of 20 nm/100 nm Ti/Au was also deposited by E-gun evaporator. It should be noted that oxygen plasma treatment to remove residual resist cannot be done, because oxygen plasma will etch polyimide. Therefore, development time of resist was added 10s to make the surface cleaner.

Chapter 3

Single-Gate Devices

In this chapter two-dimensional lateral p-i-n junction devices with single-gate design are described. These devices were based on MIS-architecture. Mask design is described, followed by a description of the device's electrical and optoelectronic properties including current-voltage (I-V) characteristics, optical characteristics. In the end of this chapter, we will discuss about yield and failure reasons of fabrication of the devices.

3. 1 Mask Design

Mask design for single-gate device is shown in figure 3.1. The figure 3.1(b) is an enlarge center region of the device. Mesa isolation etching is in white color. Purple and green colors present for n-type and p-type ohmic pads, respectively. Gate pads are in dark yellow color. The distance between two gates is 5.0 μm. The length of both gates is 120 μm, and the width is 7.5 μm. Part of the gate overlaps with ohmic contact with polyimide in-between.

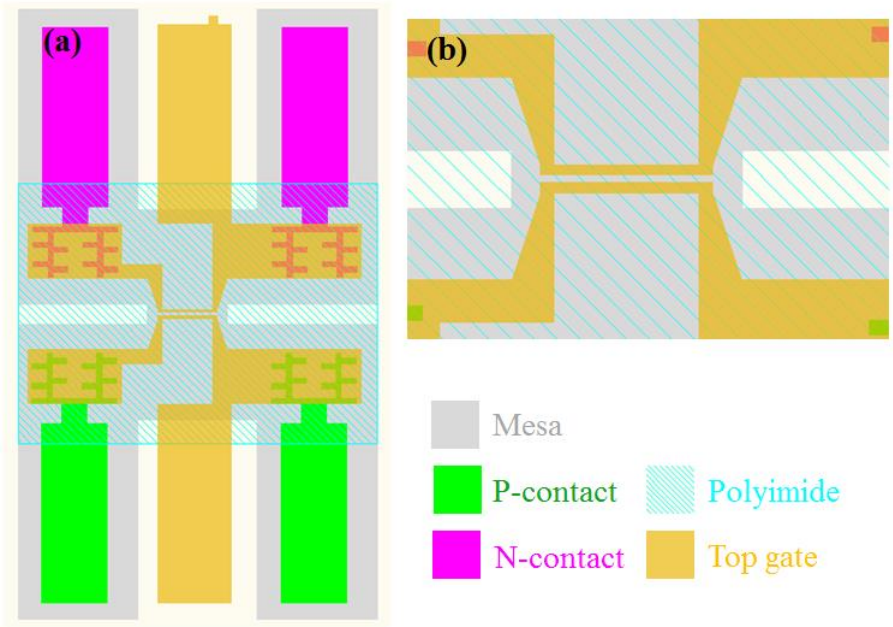


Figure 3.1 Mask design for single-gate devices

3. 2 Principle of Device Operation

The top view of a finished device is shown in figure 3.2 (a). The upper half is the p-channel device and the lower half is the n-channel device. The fabricated device has a length of 120 μm and a width of 7.5 μm for both 2DEG and 2DHG channels. The spacing between the n-gate and the p-gate, that is the length of i region, is 5 μm. Unlike in δ-doped structures, in induced devices the 2D gas only forms when a threshold inducing voltage in reached electrons/holes are pulled from the n/p type ohmic contacts by a biased gate in a principle analogous to that of enhancement mode MOSFETs. With a negative (positive) voltage applied on the p-gate (n-gate) of the p-channel (n-channel) device, the 2D hole (electron) gases in the p-channel (n-channel) can be electrically induced. By measuring the conductance between the two p-ohmic (n-ohmic) contacts, we can determine the threshold voltage of the p-channel (n-channel) devices. Figure 3.2 (b) shows the schematic cross-section of device. 2DEG and 2DHG are induced in the left and the right side of the quantum well, respectively.

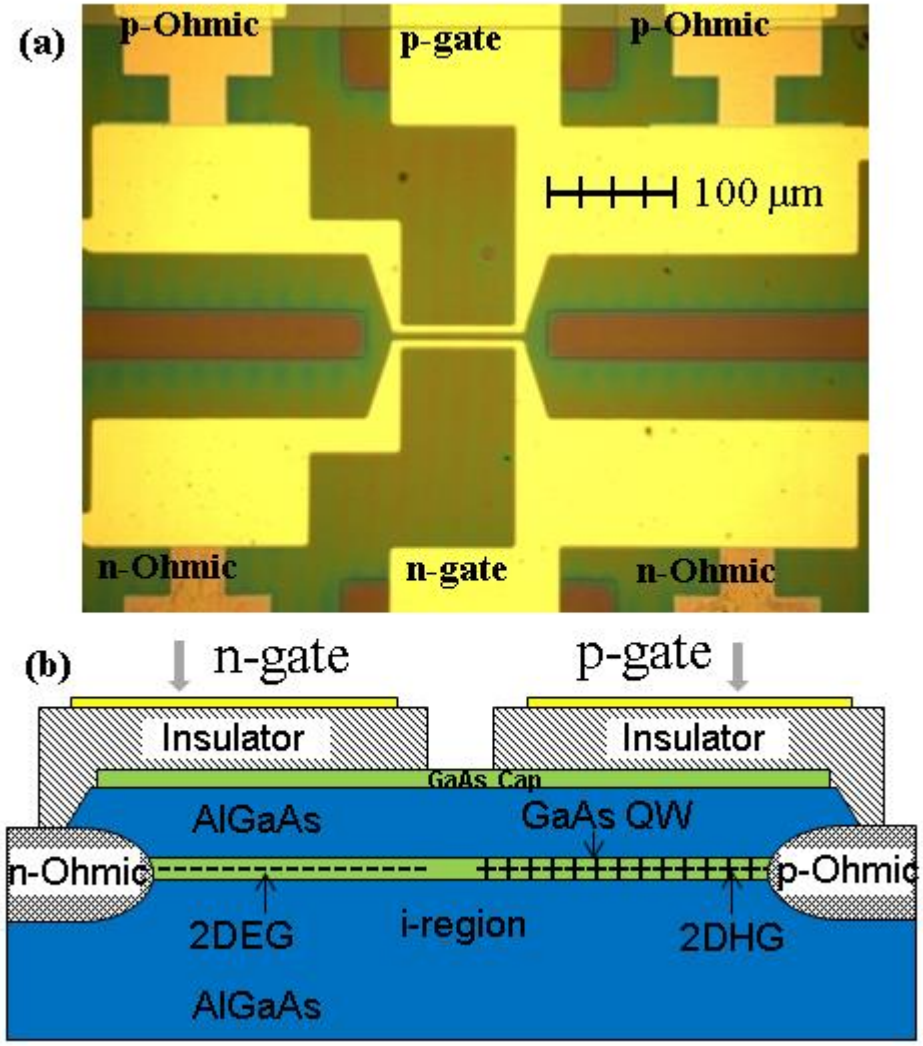


Figure 3.2 (a) Optical microscopy image of the finished devices, (b) schematic cross-section of the devices

The schematic energy band diagram at equilibrium along the channel of the 2D p-i-n diode is shown in figure 3.3. E_{1n} (dark yellow dashed line) and E_{1p} (purple dashed line) are the ground state energies for the electrons and holes, respectively, E_F is the Fermi level in the quantum well, and E_g is the GaAs band gap. Using an infinitely deep quantum well approximation, the built-in voltage V_{bi} of the lateral p-n junction is given by [50].

$$eV_{bi} = E_g + \frac{\pi\hbar^2 N_{sp}}{m_p} + \frac{\pi\hbar^2 N_{sn}}{m_n} + \frac{\pi^2\hbar^2}{2d^2}\frac{m_n+m_p}{m_n m_{np}}, \tag{3.1}$$

where N_{sp} and N_{sn} are the area densities of electrons and holes in the 2DEG and 2DHG, respectively, d is the width of the quantum well, and m_n and m_p are the effective electron and hole masses, respectively. N_{sp} and N_{sn} are functions of gate voltage. In a GaAs/AlGaAs quantum well (m_n = 0.067 m_0, m_p = 0.48 m_0, and E_g = 1.515 eV at 1.5 K),

we can approximate $N_{sp} = N_{sn} = 10^{11}$ cm^{-2}. With the quantum well width d = 20 nm, the built-in voltage is estimated to be V_{bi} = 1.535 V at 77 K. The built-in potential eV_{bi} of the lateral 2D junction is larger than the band gap E_g.

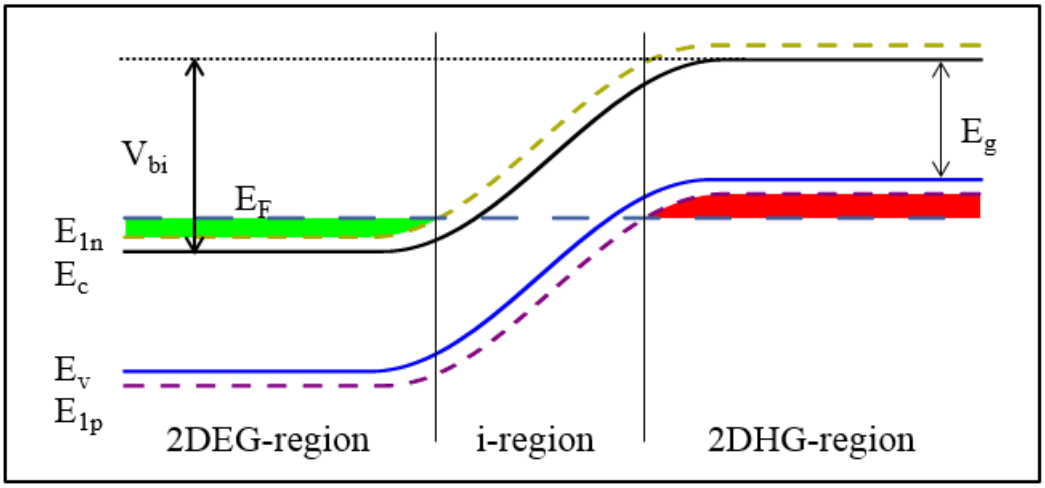


Figure 3.3 Schematic energy band diagram at equilibrium along the channel of the 2D p-i-n diode. E_{1n} (dark yellow dashed line) and E_{1p} (purple dashed line) are ground state of electron and hole, respectively.

3.3 Electrical Characteristics

3.3.1 Single Channel

To create a lateral 2D p-i-n junction, 2DEG and 2DHG have to be induced in the same device. Therefore, firstly we have to investigate the induced condition for one channel. Single channel is a MIS-structure. But the sample is totally undoped, so normally no carrier in the channel. By increasing gate bias (more positive for n-channel and more negative for p-channel), Fermi level of channel will shift into conduction band (for n-channel) or valence band for p-channel.

The device was mounted on a ceramic holder and wire-bonded, and then placed in a low-temperature tank for electrical measurement. The device was cooling in the dark. The schematic of the measurement setup for the 2DEG channel is shows in the inset of figure 3.4. Current-voltage (I-V) characteristics of devices were measured with a Keithley 2602A Dual-channel System SourceMeter Instrument. In figure 3.4, we show the drain current versus gate voltage curve for the n-channel device measured at 77 K and the drain-source voltage V_{ds} of 200 mV. The n-channel device turned on at a threshold

voltage of +3.5 V. To ensure that the insulator layer is working well, the gate current I_{gn} was monitored at the same time. The leakage current I_{gn} is less than 1.5 nA up to 4.0 V, see the figure 3.4.

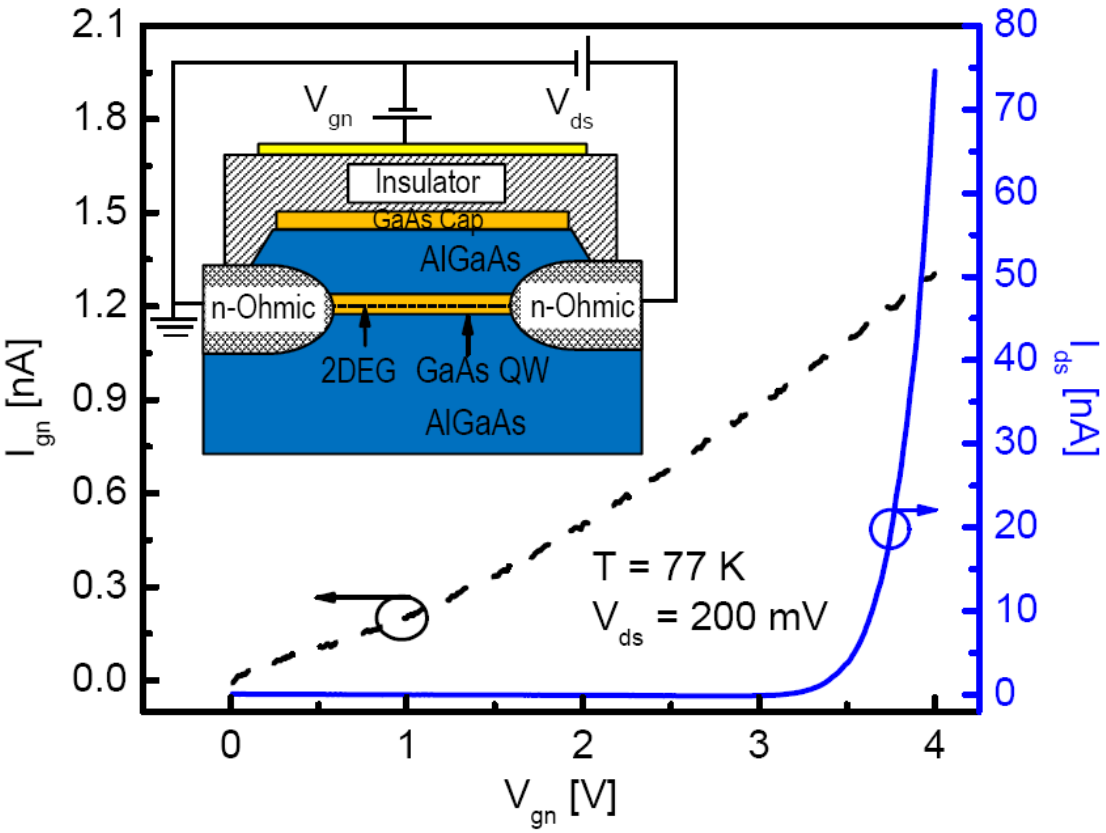


Figure 3.4 Current – voltage characteristics of 2DEG at temperature of 77 K and bias of V_{ds} = 200 mV between n-drain and n-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DEG channel.

Similarly, the electrical characteristics of the p-channel device were measured with a negative gate bias. The schematic of the measurement setup for the 2DHG channel is shows in the inset of figure 3.5. The drain versus gate voltage of the p-channel is shown in figure 3.5. The threshold voltage of the p-channel device is about -1.25 V. The gate leakage current I_{gp} was less than 1.5 nA with the bias up to -2 V. Because of the presence of negative charges on the GaAs/polyimide interface [51, 52], the threshold voltage of the n-channel and p-channel shifts towards more positive values. Therefore, the threshold of the p-channel is smaller than that of the n-channel. In fact, the threshold voltages of the p- and n-device depend on the measurement condition, because the interface charges change over long periods and when the device is illuminated.

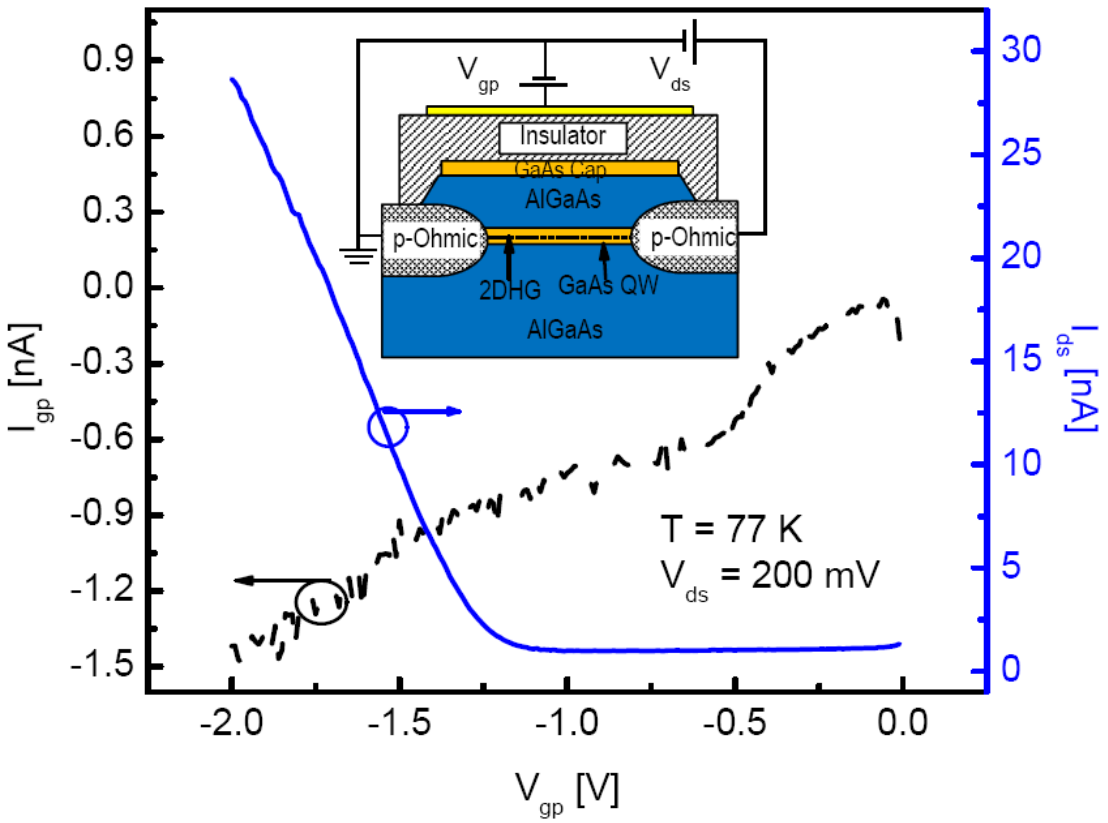


Figure 3.5 Current – voltage characteristics of 2DHG at temperature of 77 K and bias of V_{ds} = 200 mV between p-drain and p-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DHG channel.

3.3.2 Current – Voltage Characteristics of the Single-Gate Diode

By biasing the n- and p-channel devices above their threshold voltages, the electrical characteristics of the p-i-n device were then measured with the setup schematically shown in the inset of the figure 3.6. The measurement was carried out at 1.5 K in a helium continuous-flow cryostat. The gate voltage of the p-channel device V_{gp} was set at -3 V and that of the n-channel device V_{gn} at +5 V. The current flows between the p-channel and the n-channel I_{pn} was measured as a function of the voltage applied between the p and n ohmic contacts V_{pn}. In the measurement setup, the gate voltages for the N channel were measured relative to the source (the ohmic contact on the left), and the voltage of the P gates were measured relative to the drain (the ohmic contact on the right). So with this setup, the channel condition for both the N channel and the P channel remains the same when V_{pn} is changed. Note that the current I_{pn} in figure 3.6 was plotted both in the linear

and logarithmic scales for clarity. One can see clearly the rectifying behavior with a turn-on voltage of 1.53 V. This is in agreement with the theoretical calculation of the built-in voltage V_{bi} = 1.535 V [50]. The turn-on voltage of the p-i-n diode, however, slightly depends on the gate voltage applied to the n-gate and the p-gate. From the band energy diagram in figure 3.3 and the built-in voltage V_{bi} (shown above), we can see that the turn-on voltage is approximately at the band gap energy and depends on the carrier densities in 2DEG and 2DHG. The higher the gate bias (positive for the n gate and negative for the p gate) is, the higher the built-in potential is and, therefore, the higher the turn-on voltage is. The current of the diode can go up to hundreds of μA. In the reverse bias, the leakage current is below 1 nA up to – 2 V.

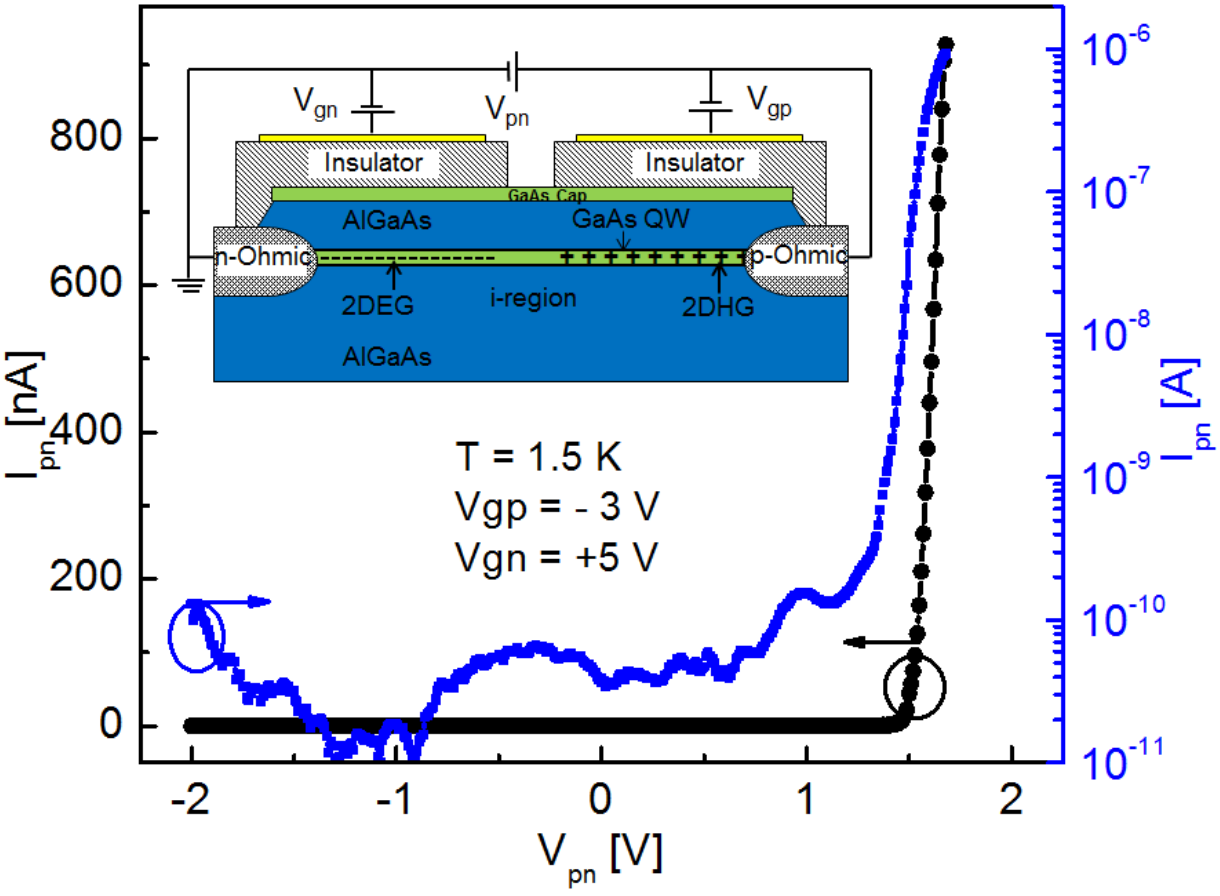


Figure 3.6 Current – voltage characteristics of the lateral 2D p-i-n diode at temperature of 1.5 K with p-gate and n-gate biasing at V_{gp} = -3 V and V_{gn} = +5 V, respectively. Vpn is the operation voltage of the diode. The inset shows a schematic diagram of the measurement setup for the lateral 2D p-i-n junction.

3.4 Optical Characteristics

The electroluminescence (EL) emission of the p-i-n diode measured at 1.5 K is shown in figure 3.7. The device was measured under gate voltages of V_{gn} = 7 V and V_{gp} = -7 V, and a forward current I_{pn} = 200 μA. There are two peaks in the EL spectra. The peak at 1.529 eV (811 nm) with the full-width at half-maximum of 4.4 meV is, we believe, from the ground state emission of the 20 nm GaAs/AlGaAs quantum well. The results are in good agreement with the theoretical calculation. Using the infinite-well approximation, the ground state of electrons in the quantum well E_{1n} = 0.014 eV and the ground state of holes in the quantum well E_{1p} = 0.002 eV. Otherwise, the band gap energy of GaAs at 1.5 K is 1.517 eV. Therefore, the energy of ground state excitons of the quantum well can be estimated to be approximately 1.533 eV (809 nm). The small peak at 831 nm is probably from the acceptor level in the quantum well. The positions of the peaks are independent of the diode current. The electroluminescence emission spectra of our devices are stable and much cleaner than those of previously reported lateral 2D junctions [4, 7, 27, 53] which is important for using the device for further studies and applications.

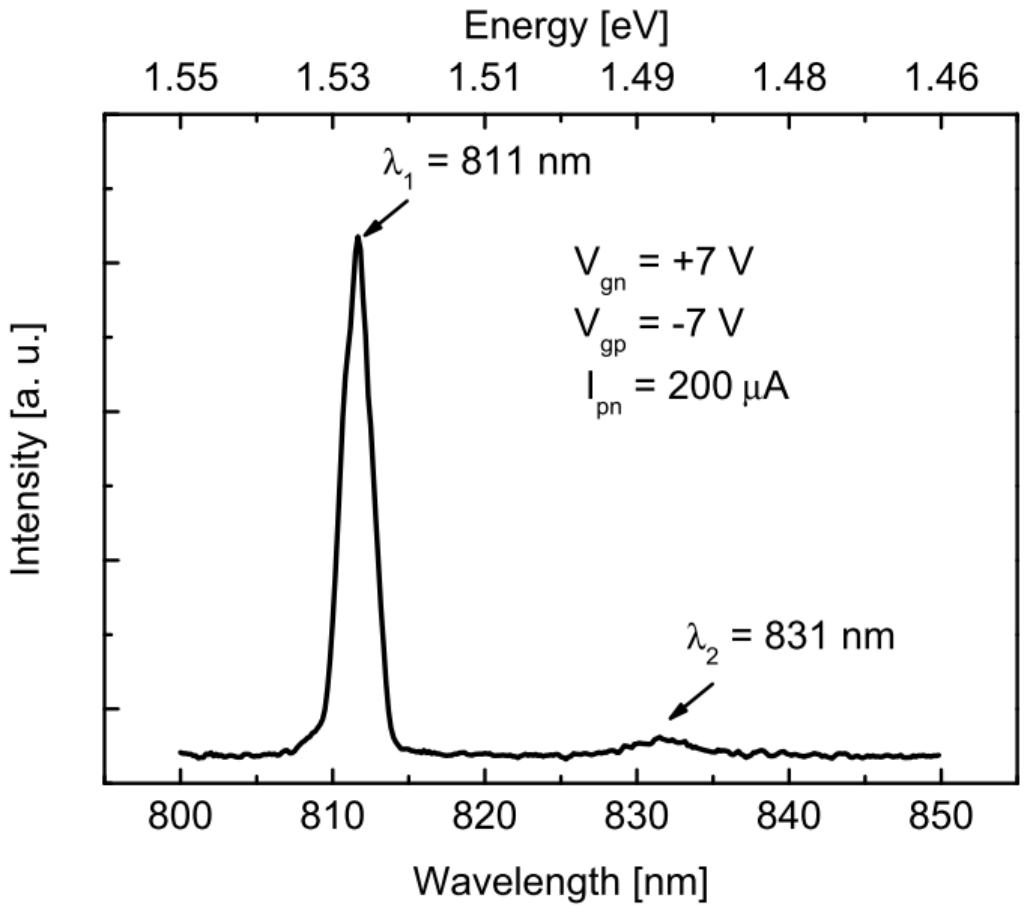


Figure3.7 Electroluminescence spectra of the lateral 2D p-i-n diode at temperature of 1.5 K with p-gate and n-gate biasing at V_{gp} = -7 V and V_{gn} = +7 V, respectively, and a forward current I_{pn} = 200 μA.

Furthermore, to confirm that the light was indeed emitted from the 2D p-i-n junction, EL intensities were measured as a function of position with a spatial resolution of 10 μm. The device was inserted into the micro-photoluminescence (μ-PL) system, which is shown in figure 3.8. The stage can be controlled by using a Newport Universal Motion Controller ESP 300 with a step resolution of 0.5 μm. Thus, a spectrum of the diode is captured by Princeton camera ST-133 for each position of the device. All system was controlled automatically by labview program.

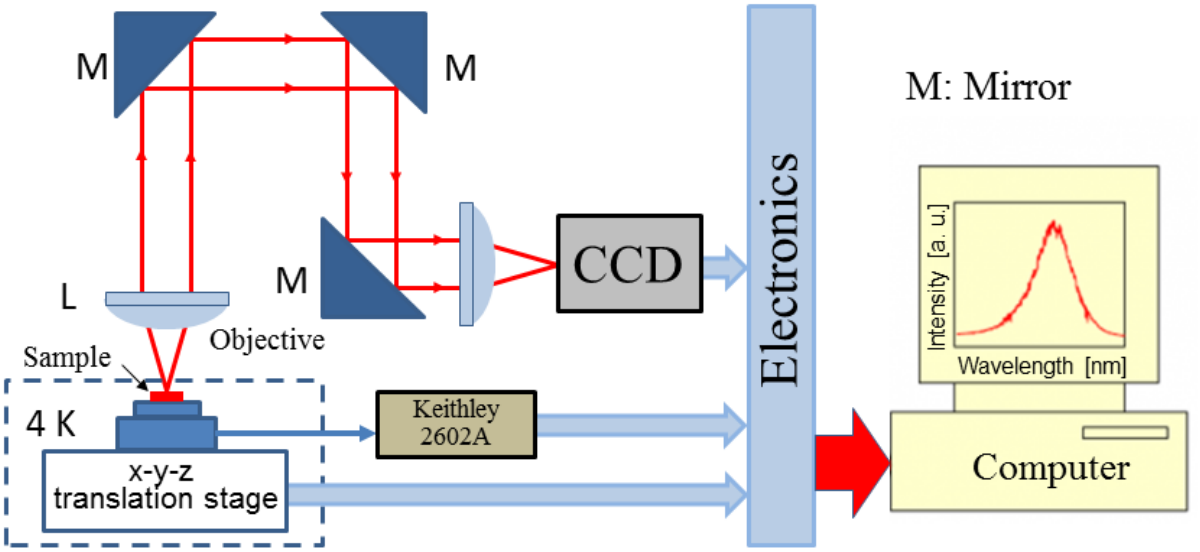


Figure 3.8 Configuration of Micro Photoluminescence system

Figure 3.9 shows the contour plot of the integrated spectral intensity versus position. The scanned area is 225 x 30 μm^2. The device was measured with I_{pn} = 100 μA, V_{gp} = -5 V, and V_{gn} = +5 V at 77 K. From the result, one can clearly see that the emitted light is indeed from the junction area (in the middle between the dashed guide lines), but close to the two sides of the device. The reason for such distribution is because the lowest resistive path is near the two sides. Additionally, the emitted light coming from the right corner is much stronger than that coming from the left corner. This is possibly attributed to the asymmetric gate geometry [see figure 3.2 (a)] and the resistance difference of the ohmic contacts.

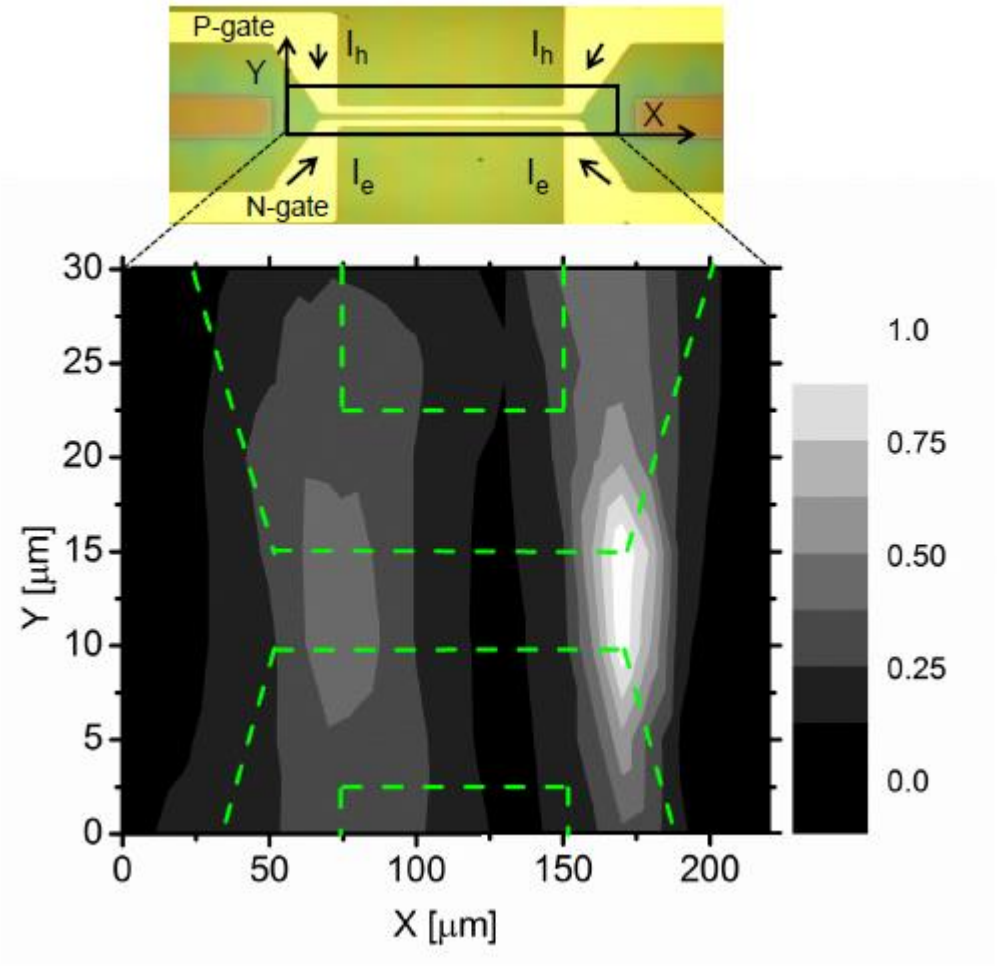


Figure 3.9 Contour plot of integrated spectrum intensity at temperature T = 77 K, gate bias V_{gp} = -5 V, V_{gn} = +5 V and forward current I_{pn} = 100 μA.

3.5 The Yield of n-channel and p-channel

The yield of the induced 2DEG and the induced 2DHG are approximately 60% and 80%, respectively. The yield of the induced 2DHG is higher than that of the induced 2DEG. This is possibly due to p-type ohmic contacts are smoother than n-type ohmic contacts. In addition, AuZn/GaAs contact lacks the low-temperature lattice disrupting constituents common to n-type GaAs contacts [45]. There are several main causes of failure. One of these is leakage. The most common leakage is between the gate metal and the ohmic contact. This leakage occurs as soon as any voltage is applied. There is a main reason that lead to this leakage: spikes in the ohmic contact surface. To reduce possibility of spikes, ohmic metal deposition should keep stable at a reasonable rate, and lift-off and thermal

annealing processes should immediately done after sample was unloaded from the chamber.

Another reason for failure of the device can occur during processing of polyimide layer. This process is sensitive to humidity. The first and most obvious of these is that under high humidity conditions the polyimide does not form a continuous film on the sample. This problem has been improved somewhat by the addition of several steps to reduce the humidity locally. Between each processing step the samples are kept in a vacuum box with silica gel. Another problem, possibly occurred in curing of polyimide, is crack on the polyimide surface. Therefore, we should keep temperature increasing and decreasing rate during curing low.

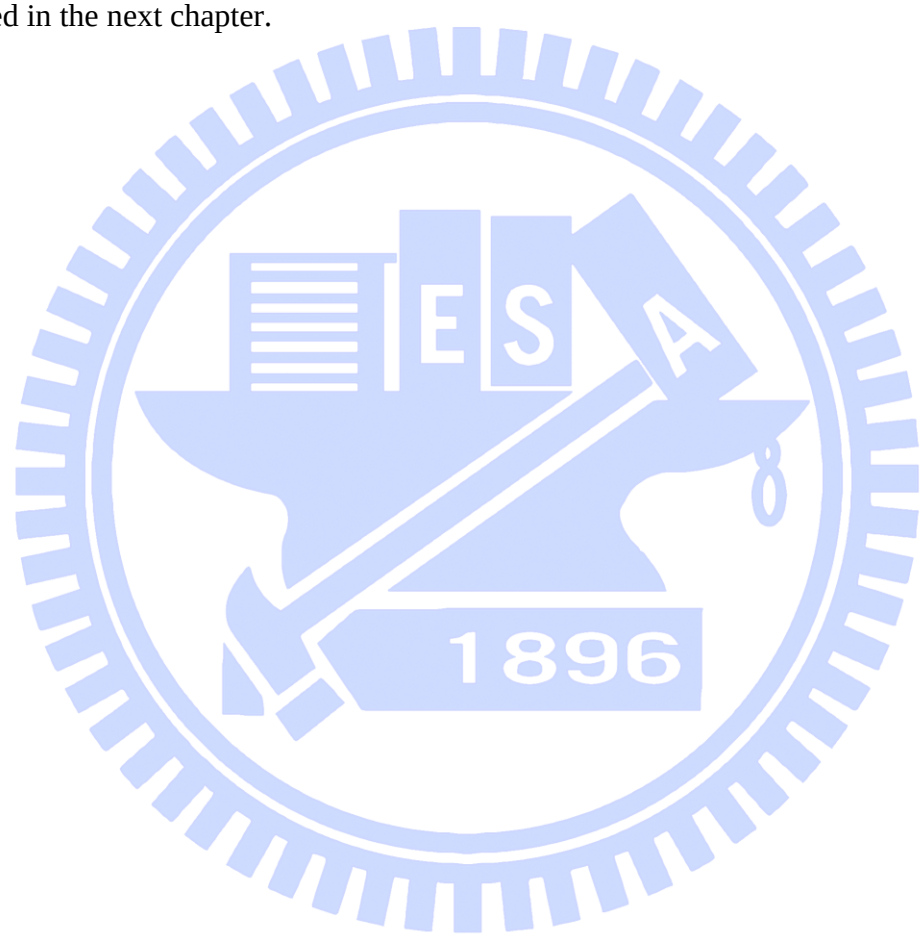
A third reason for failure is ohmic contact recess. As has been explained above, the diffusion profile for the ohmic contact is critical. To induced 2DEG or 2DHG, diffusion profile has to well extend into quantum well. Therefore, recess etched depth should be down to quantum well. In Our sample (quantum well is 305 nm below the surface), if etching depth is above or 40 nm below the quantum well, 2D gas cannot form.

A fourth reason for failure, involved with the measurement of these devices, should be mentioned. It should be appreciated that the measurement of these devices is different from that of doped samples in several ways. The first is that a gate voltage will always have to be applied to induce a 2D gas. Also the voltage required to form a 2D gas are far in excess of voltages typically used on doped gas. Therefore it has been found that the devices appear to have leakage problems when in fact it is the electrical contacts to the devices, via the probe, that are at fault. The devices should also be cooled in the dark. This prevents the devices from turning on, possibly due to charging effects.

3.6 Disadvantages of Single-Gate Structure

We have developed a relatively simple method to fabricate high-quality lateral 2D p-i-n junctions. By using the MIS structure, 2DEG and 2DHG can be induced side by side in a completely undoped GaAs/AlGaAs quantum well. Our results show that the device is promising for applications in SAW-driven single-photon sources and probing the intrinsic spin Hall effect in low-dimensional systems by optical means. However, the gate control of the carriers in the quantum well is not very efficient because of the distant gate from

the channel. As a result, the two top gates on the insulator could not be put too close to each other. This directly affects the carrier recombination in the i region. To solve this problem, we developed the present twin-gate structure, whose cross-section was shown in figure 2.5 (b) of the previous chapter. The surface gates provide a very good control for the carriers in the channel and at the same time can be put very close to each other. The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts. The characteristics of the devices will be reported in the next chapter.



Chapter 4

Twin-Gate Devices

In this chapter two-dimensional lateral p-i-n junction devices with twin-gate design are described. These devices were based on MIS-architecture hybrid with Schottky-gate structure. Mask design is described, followed by a description of the device's electrical and optoelectronic properties including current-voltage (*I*-*V*) characteristics, optical characteristics.

4.1 Mask Design

Figure 4.1 shows the mask design for twin-gate devices. The figure 4.1 (b) is an enlarged center region of the device. Mesa isolation etching is in white color. Purple and green colors present for n-type and p-type ohmic pads, respectively. Top gate metal is in dark yellow color. Two n-type ohmic contacts are in purple color and two p-type ohmic contacts are in green color. Surface gate metal is in blue color. The polyimide layer has two rectangular holes at two sides of polyimide layer to make pad contact to surface gate. The distance between two surface gates is 2.0 μm. The length of the surface gate is 10 μm, and the width is 7.5 μm. Top gate (TG) overlaps part of the surface gate (SG) and part of ohmic contacts with polyimide in-between.

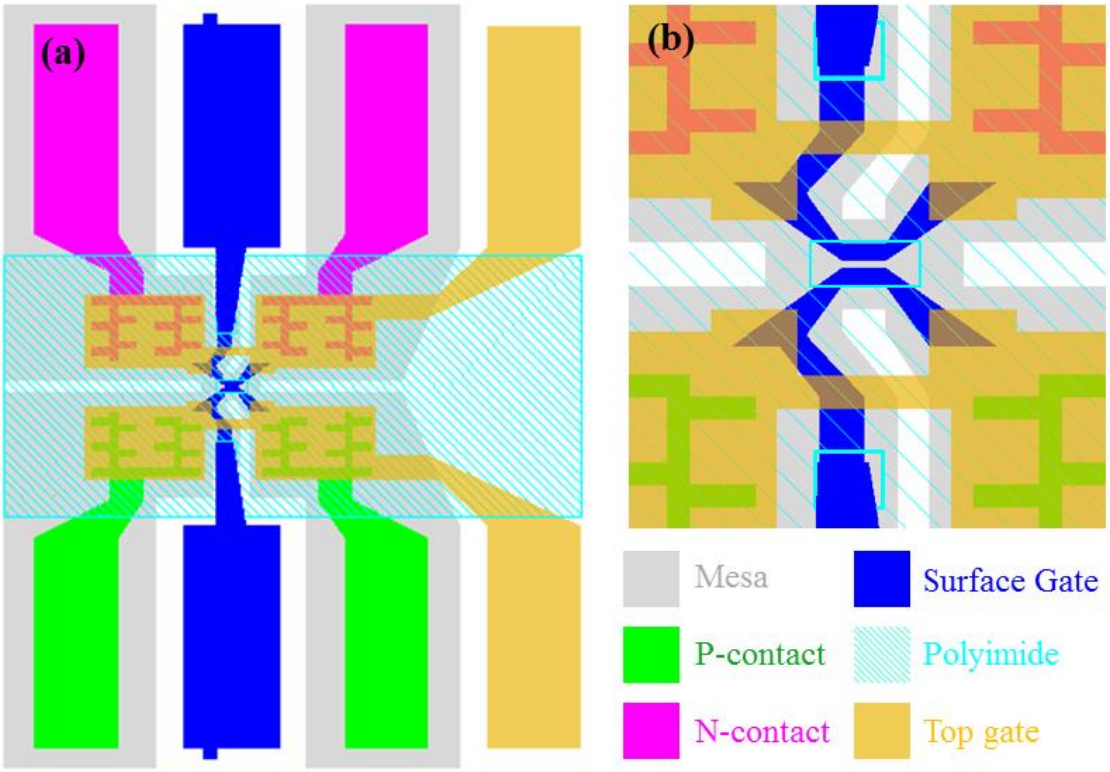


Figure 4.1 Mask design for twin-gate devices

In the previous chapter, we have discussed a lateral p-i-n diode using a single-gated MIS structure. But the gate control of the carriers in the quantum well is not very efficient because of the distant gate from the channel. As a result, the two top gates on the insulator could not be put too close to each other. This directly affects the carrier recombination in the i region. To solve this problem, we developed the present twin gate structure, which was first introduced by Harrell *et al*. [39]. The surface gates provide a very good control for the carriers in the channel and at the same time can be put very close to each other. The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts.

4.2 Principle of Device Operation

Figure 4.2 (a) shows the schematic cross-section of device. Recessed surface gates are fabricated on AlGaAs and at the distance 150 nm from GaAs quantum well channel. 2DEG and 2DHG are induced in the left and the right side of the quantum well under appropriate gate biases, respectively. The top view of a finished device is shown in figure

4.2 (b). The upper half is the p-channel device and the lower half is the n-channel device. The fabricated device has a length of 10 μm and a width of 7.5 μm for both 2DEG and 2DHG channels. The distance between the n-SG and the p-SG, that is the length of i region, is 2 μm. Dark blue is polyimide. The devices are normally off because the epitaxy layers are totally undoped.

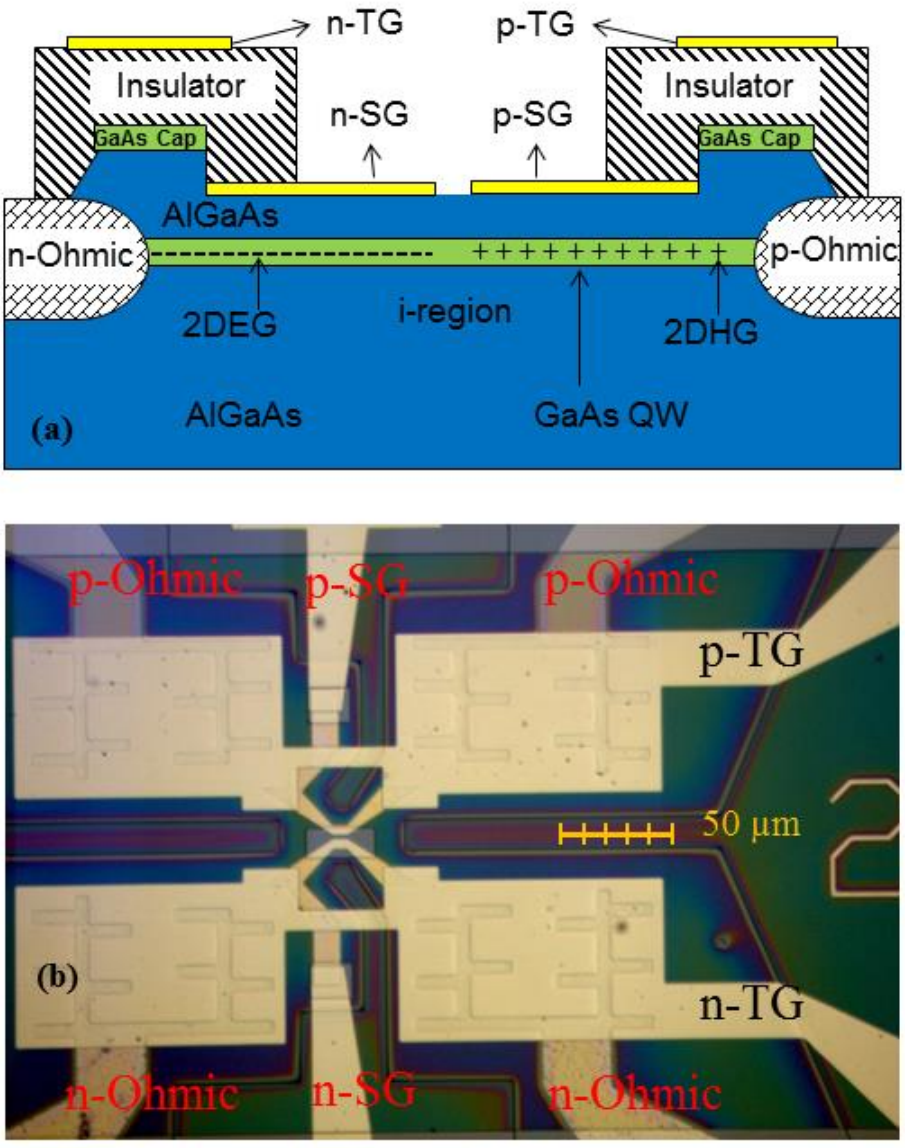


Figure 4.2 (a) Schematic cross-section of the devices. (b) Optical microscopy image of the finished device.

In our device layout, the n-SG and the p-SG are placed side by side with 2 μm spacing; see figure 4.1(b). With a negative voltage applied on the p-gates (SG and TG) and a positive voltage applied on the n-gates (SG and TG), both 2DHG and 2DEG

channels can be induced in the GaAs quantum well, so a lateral 2-D p-i-n diode is created. The operation of the devices is almost the same as the operation of the single-gate devices.

4.3 Electrical Characteristics

4.3.1 Single Channel

The device was mounted on a ceramic holder and wire-bonded, and then placed in a helium continuous-flow cryostat for electrical measurement. The device was cooled down to 4 K in the dark. The schematic of the measurement setup for the 2DHG and 2DHG channel is shows in figure 4.3. This setup is similar to that used for the single-gate devices with addition of a voltage source for surface gate. Current-voltage (I-V) characteristics of devices were measured with a Keithley 2602A Dual-channel System SourceMeter Instrument.

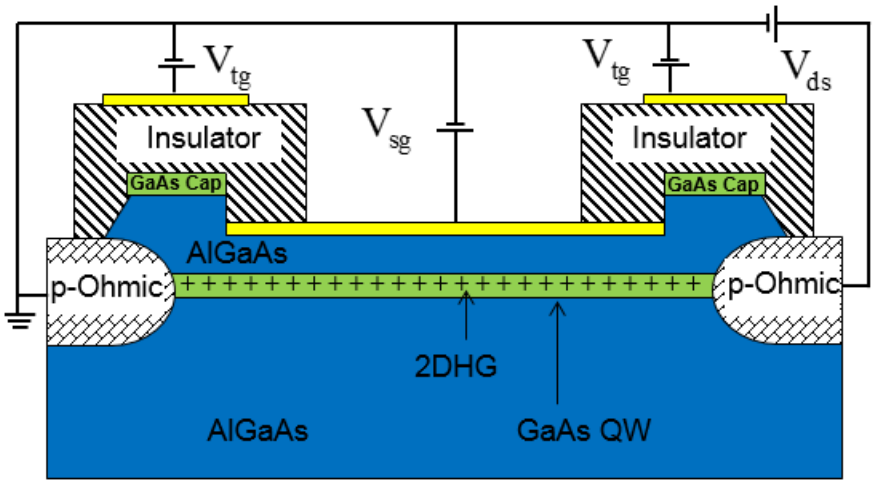


Figure 4.3 The schematic of the measurement setup for the 2DHG and 2DHG channel. V_{tg} (V^{p}_{tg} or V^{n}_{tg} in text) and V_{sg} (V^{p}_{sg} or V^{n}_{sg} in text) are top gate and surface biases, respectively.

Figure 4.4 shows the drain current versus p-TG voltage (denoted as V^{p}_{tg}) curve for the p-channel with the drain-source (two p-type Ohmic contacts) voltage, V_{ds}, set at 500 mV. The two different curves correspond to two different p-SG voltages of -0.4 V and -0.6 V. The p-TG threshold voltage is -0.8 V, which stays constant for the two p-SG voltages. The transconductance is higher for V^{p}_{sg} = -0.6V as expected because more carriers are induced in the channel. The same measurements were performed for n-channel of the devices. The inset of figure 4.4 shows the drain current versus n-TG

voltage curve of the n-channel with n-SG voltage V^{n}_{sg} = 0.9 V and the drain-source (two n-type Ohmic contacts) voltage V_{ds} of 500 mV. The threshold voltage of the n-TG is 3.2 V. The higher threshold voltage of the n-channel is probably due to the surface state pinning at the insulator/semiconductor interface [18].

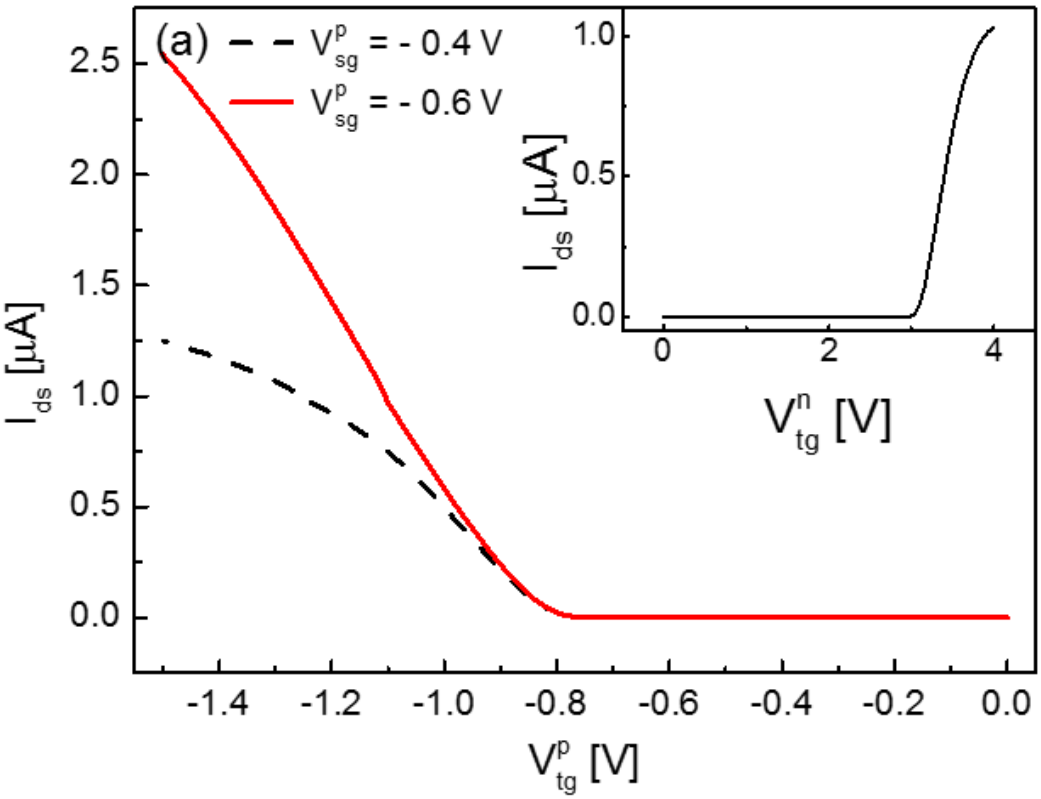


Figure 4.5 Current – voltage characteristics of 2DEG and 2DHG with bias between two Ohmic V_{ds} = 500 mV at temperature of 4 K. Current – TG voltage characteristics of 2DHG with different SG voltages, -0.4 V (dashed line) and -0.6 V (solid line). The inset shows current – TG voltage characteristics of 2DEG.

Figure 4.5 shows the drain current versus p-SG voltage V^{p}_{sg} for the p-channel at V_{ds} = 500 mV. Different curves correspond to different p-TG voltages. The p-SG threshold voltage is -0.2 V. The saturation current is higher for higher V^{p}_{tg}, because the series resistance between the channel and the source Ohmic contact is reduced when V^{p}_{tg} increases. The I_{ds}- V^{n}_{sg} curve for the n-channel with V^{n}_{tg} = 6 V and V_{ds} = 500 mV is shown in the inset of figure 4.5. The threshold voltage of the n-SG is 0.5 V.

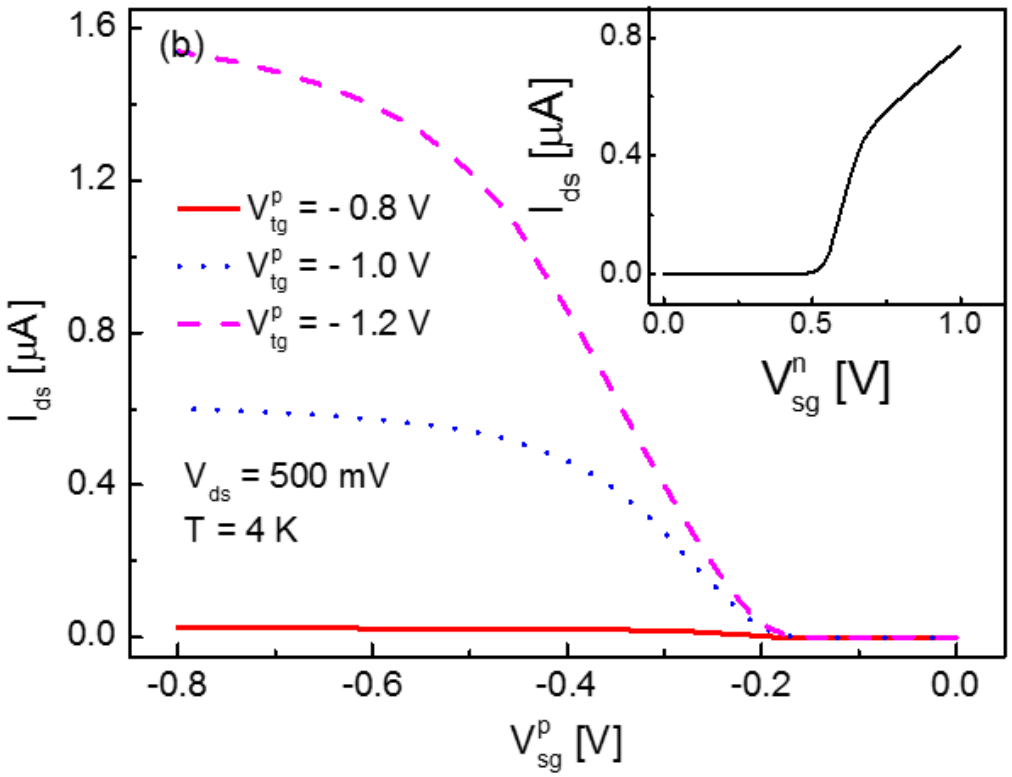


Figure 4.5 Current – voltage characteristics of 2DEG and 2DHG with bias between two Ohmic V_{ds} = 500 mV at temperature of 4 K. Current – SG voltage characteristics of 2DHG with different TG voltages, -0.8 V (solid line), -1.0 V (dot line), and -1.2 V (dashed line). The inset shows current – SG voltage characteristics of 2DEG channel.

The gate leakage currents versus top gate voltage are presented in figure 4.6. Leakage currents to gates were in scale of the system limit, about 100 pA. Therefore, the stability of the induced carriers is pretty good. The leakage of n-channel is more stable than that p-channel, this possibly due to lower threshold voltage of p-channel.

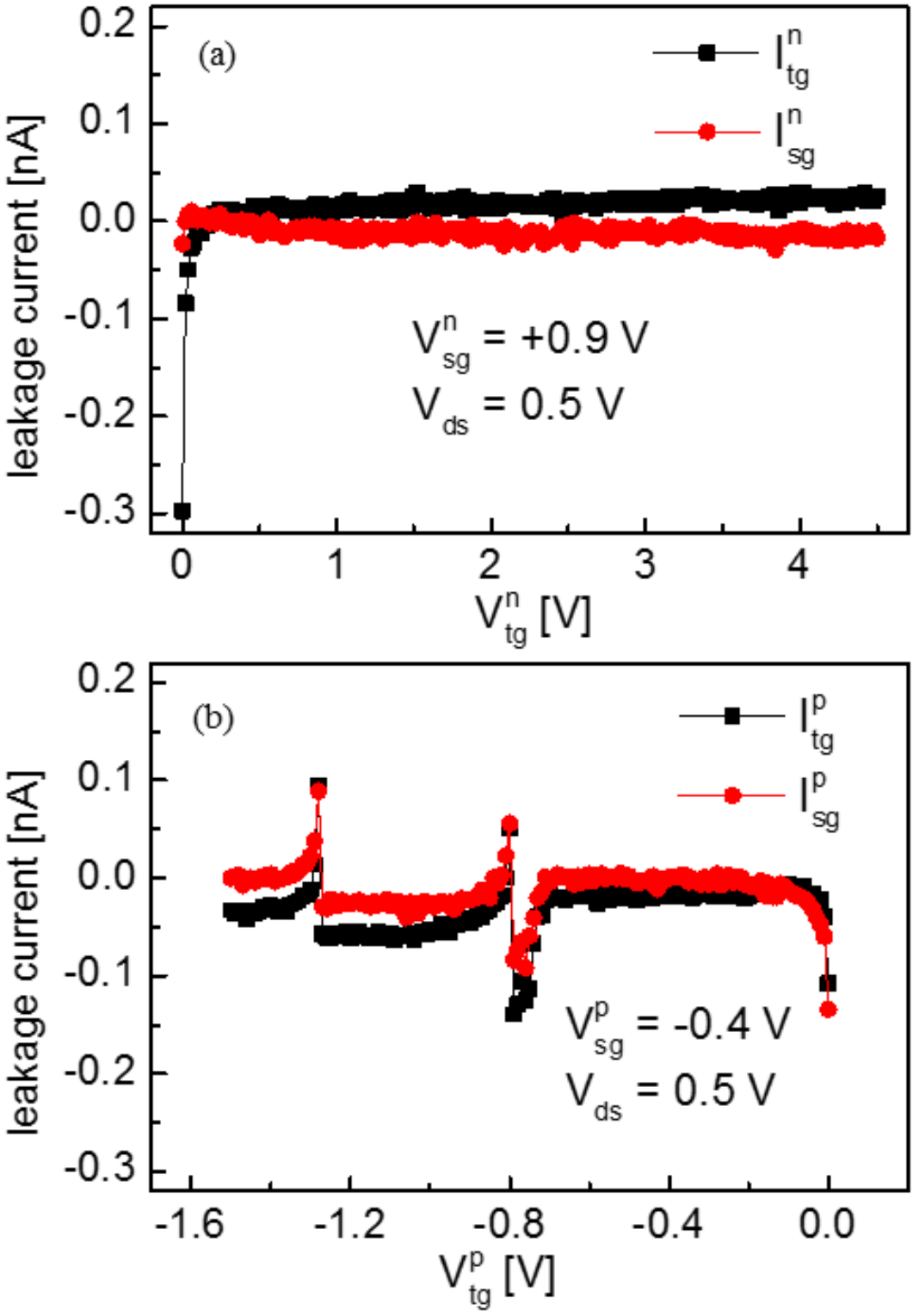


Figure 4.6 Gate leakage currents versus top gate voltage. (a)I^n_{tg} and I^n_{sg} are leakage currents of n-type ohmic side top gate and surface gate. (b) I^n_{tg} and I^n_{sg} are leakage currents of p-type ohmic side top gate and surface gate.

4.3.2 Current-voltage Characteristics of the Twin-Gate Diode

Measurement electrical characteristics of the twin-gate devices are similarity to that of the single-gate devices. By biasing the n- and p-channel devices above their threshold voltages, the electrical characteristics of the p-i-n device were then measured. The measurement configuration is shown in the inset of figure 4.7. The p-TG bias V^{p}_{tg} and p-SG bias V^{p}_{sg} of the p-channel device were set at -3 V and -0.6 V respectively and those of the n-channel device were V^{n}_{tg} = +6 V and V^{n}_{sg} = +0.9 V. The current flow between the p-channel and the n-channel, denoted as I_{pn} , was measured as a function of the voltage applied between the p and n ohmic contacts V_{pn}; see inset of figure 4.7. In the measurement setup, the gate voltages for the N channel were measured relative to the source (the ohmic contact on the left), and the voltage of the P gates were measured relative to the drain (the ohmic contact on the right). So with this setup, the channel condition for both the N channel and the P channel remains the same when V_{pn} is changed. The current I_{pn} in figure 4.7 is plotted both in the linear and logarithmic scales for clarity. One can see clearly the rectifying behavior with turn-on voltages of 1.73 V. Very good exponential behaviour was observed all the way down to the measurement limit. The current of the diode can go up to hundreds of microamperes. Two kinks occur in the I-V curve at V_{pn} = 1.48 and 1.70 V. The kink position slightly changes with the surface gate bias. Thus, they could be attributed to the potential barriers for hole at p-i junction and for electron at the n-i junction. However, further investigations are needed to address this issue.

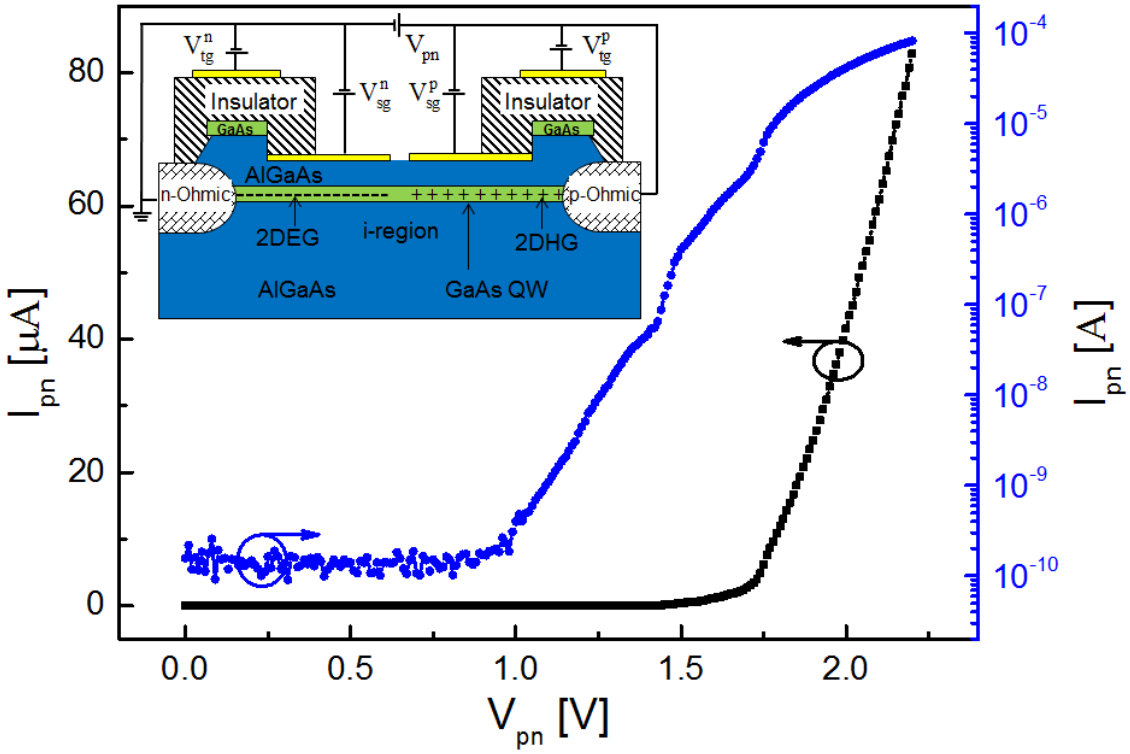


Figure 4.7 Linear and logarithmic current – voltage characteristics of the lateral 2-D p-i-n diode at temperature of 4 K with p-TG and n-TG biased at V^p_{tg} = -3 V and V^n_{tg} = +6 V, respectively, and p-SG and n-SG biased at V^p_{sg} = -0.6 V and V^n_{sg} = +0.9 V, respectively. V_{pn} is the operation voltage of the diode. The inset shows measurement configuration.

Figure 4.8 shows the gate leakage currents versus the diode bias V_{pn}. We can see clearly that the gate leakage currents are very small. The leakage currents slightly increase when the diode bias is near threshold voltage. In fact, the gate leakage currents versus the diode voltage V_{pn} curves, however, change from device to device. But, the leakage currents remain very small in comparison with the diode current.

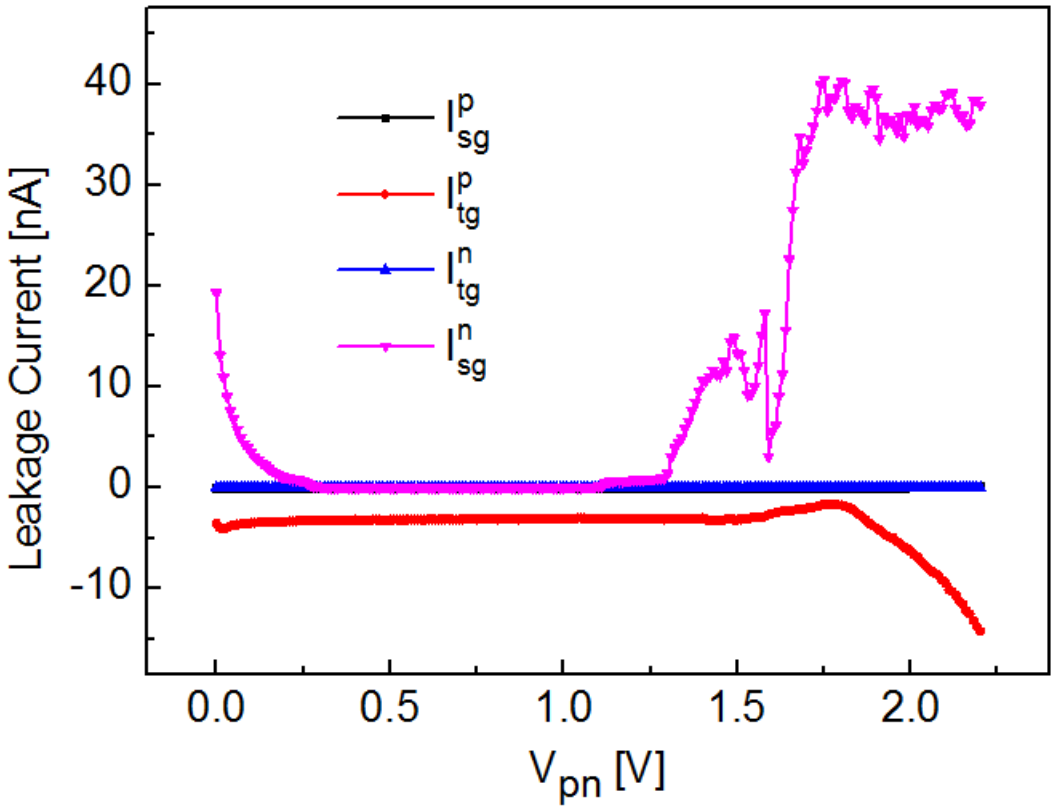


Figure 4.8 Gate leakage currents versus the diode bias V_{pn} at temperature of 4 K with p-TG and n-TG biased at V^p_{tg} = -3 V and V^n_{tg} = +6 V, respectively, and p-SG and n-SG biased at V^p_{sg} = -0.6 V and V^n_{sg} = +0.9 V, respectively. V_{pn} is the operation voltage of the diode.

4.4 Optical Characteristics

4.4.1 Electroluminescence Spectrum

Electroluminescence of the devices was measured in micro-photoluminescence system (micro-PL), as shown in figure 3.8 of the previous chapter. The electroluminescence (EL) emission of the p-i-n diode measured at 4 K is shown in figure. 4.8. The device was measured under the surface gate voltages of V^n_{sg} = +0.9 V and V^p_{sg} = -0.6 V, and the top gate voltages of V^n_{tg} = 6 V and V^p_{tg} = -3 V, and the junction voltage from V_{pn} = 1.6 V to 2.0 V with step of 0.05 V. The inset of figure 4.8 shows the measure photoluminescence (PL) of the sample. We clearly observe two peaks in the PL spectra at 1.5205 eV (815.5 nm) and 1.5239 eV (813.7 nm). The intensity ratio of the two PL peaks remains constant when the excitation power changes. Thus, the two peaks observed here are most likely due to the roughness of the quantum well interfaces [54]. There are also two peaks at

1.5174 eV (817.5 nm) and 1.5207 eV (815.4 nm) in the EL spectra. The peaks have a 0.4 meV redshift when the junction bias V_{pn} increases from 1.6 V to 2.0 V. Full width at half maximum of the 1.5205 eV peak changes from 1.2 to 2.2 meV, and that of the other peak from 1.2 to 3 meV when V_{pn} increases from 1.6 V to 2.0 V. The narrow linewidths of the peaks demonstrate that the 2-D channel is of high-quality, which is essential for further applications such as electrically-driven single photon sources.

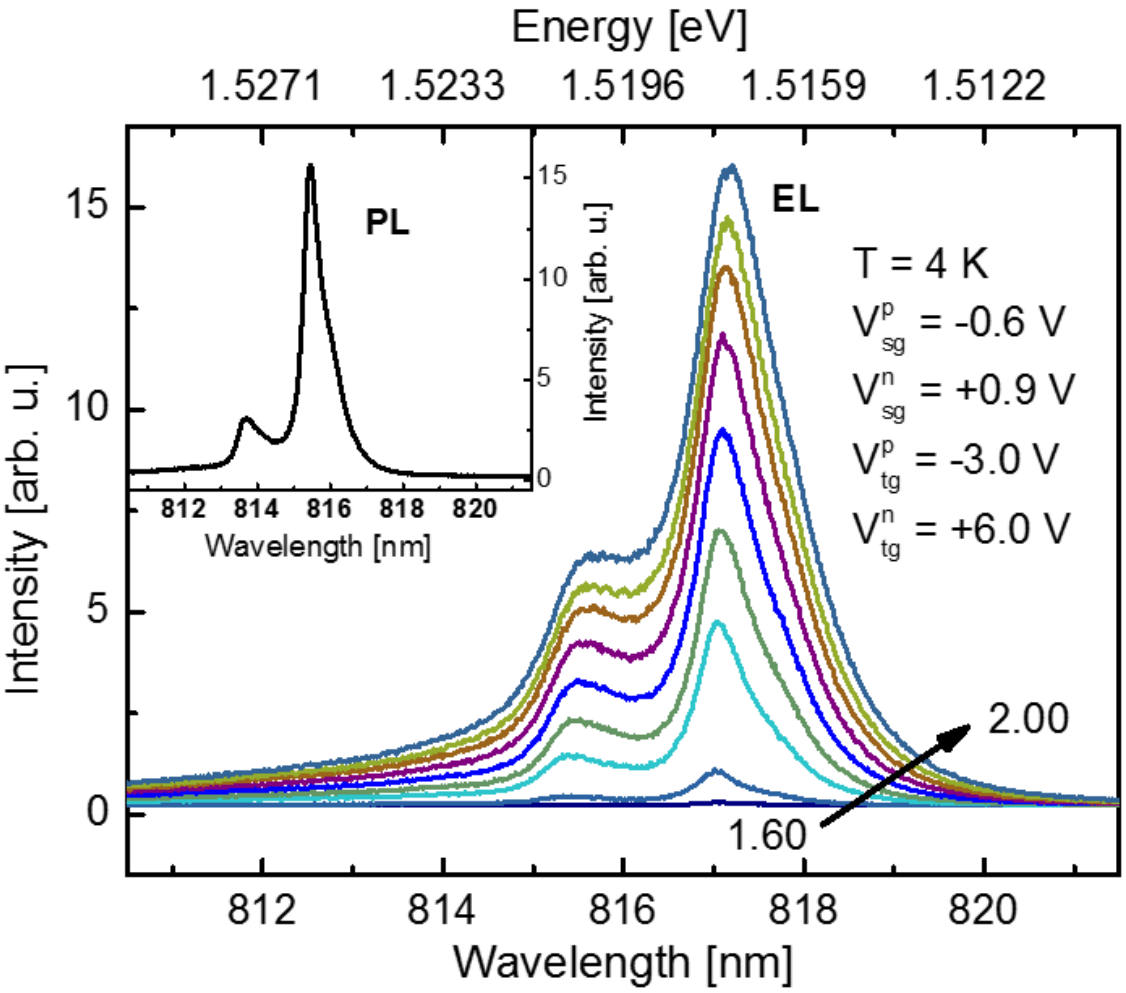


Figure 4.9 Electroluminescence spectra of the lateral 2D p-i-n diode at temperature of 4 K with with p-TG and n-TG biasing at V^p_{tg} = -3 V and V^n_{tg} = +6 V, respectively and p-SG and n-SG biasing at V^p_{sg} = -0.6 V and V^n_{sg} = +0.9 V, respectively and V_{pn} from 1.6 V to 2.0 V with step 0.05 V. Inset shows photoluminescence spectrum at 4 K.

4.4.2 External quantum efficiency

Figure 4.9 shows the integrated intensity of the EL spectra (black curve with square symbol) against the junction bias V_{pn}. Light intensity increases linearly with diode voltage V_{pn}.

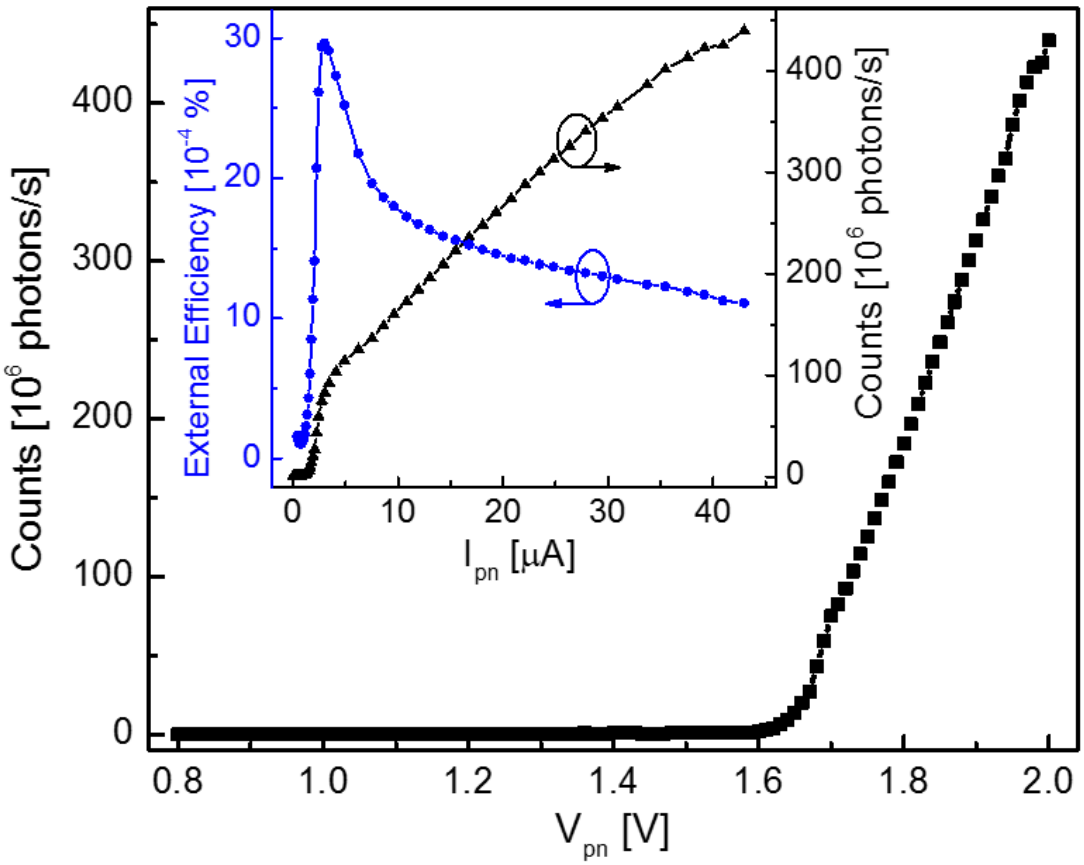


Figure 4.10 Light integrated intensity versus forward bias voltage of the lateral 2D p-i-n diode measured at the same condition. Inset shows the light integrated intensity (black curve with triangle symbol) and external efficiency (blue curve with round symbol) versus the diode current.

We can estimate the external quantum efficiency of the diode by assuming that internal quantum efficiency is 100%. The Transmission and reflection parameters for micro-PL system are as follows:

- CCD quantum efficiency at wavelength 817 nm: $\eta_1 = 93\%$
- Reflectivity of mirror: 95%, we use three mirrors, so $\eta_2 = 0.95*0.95*0.95$
- Reflectivity of grating at wavelength 817 nm: $\eta_3 = 85\%$
- Transmissivity of the windows: $\eta_4 = 90\%$

- Transmissivity of the objective and the lens at wavelength 817 nm: η_5 = 75%
- NA of the objective: 0.5 so the collection efficiency of the objective is η_6 = 33%

Therefore, external efficiency of the device is:

$$\eta_{ext} = \frac{N_{ph}}{\eta_1\eta_2\eta_3\eta_4\eta_5\eta_5\eta_6} / \frac{I_{pn}}{e}, \quad (4.1)$$

Where N_{ph} is the photon count measured by the CCD.

Inset of figure 4.9 shows the integrated intensity of the EL spectra (black curve with triangle symbol) and external efficiency (blue curve with round symbol) versus the diode current I_{pn}. At low currents, I_{pn} < 5.0 μA, after an initial set back, the light intensity rises sharply with current. At higher currents, I_{pn} > 5.0 μA (after the diode turns on, V_{pn} > 1.73 V), the light intensity increases with current at a constant rate. However, the slope of L-I curve is much smaller in comparison to low injection currents. The result can be explained as follows. At low currents, radiative recombination mostly happens in the i-region. But at high currents, electrons are injected into the p-region under p-SG and holes are injected into the n-region under n-SG. So, as a result, part of the radiation is blocked by the gate metal. Consequently, light collection efficiency decreases. This can be seen in the external efficiency curve in inset of figure 4.10. With the increasing forward current I_{pn} from 0.0 μA to 5.0 μA, the external quantum efficiency increases to a maximum of 0.003 %, then it drops dramatically for I_{pn} > 5.0 μA (after the diode turn on, V_{pn} > 1.73 V). This problem could be avoided by using semi-transparent metal gate.

4.5 The Yield of n-channel and p-channel

The yield of the induced 2DEG and the induced 2DHG are approximately 50% and 70%, respectively. So the yield of the lateral p-i-n junction is about 35%. The yield of the twin-gate devices is lower than that of the single-gate devices, because there is extra leakage path (between the surface gate and top gate, ohmic contacts) in the twin-gate devices. In addition, the more processes twin-gate devices needed, higher probability of process related failure occurs.

Chapter 5

Summary and Future Work

5.1 Summary

The main results of this thesis are summarized as follows:

- We have developed a relatively simple method to fabricate high-quality lateral 2D p-i-n junction. Our devices show better optical characteristics in comparison with the previous reports. We used standard processing technology to fabricate the devices, so it could be employ to fabricate the devices on other material.
- By using MIS-structure, 2DEG and 2DHG can be induced side by side to form a p-i-n junction. Single-channel 2DEG or 2DHG were induced at threshold bias of 3.5 V and -1.25 V, respectively. This illustrates the reliability and simplicity of the ohmic contact fabrication method that only utilized conventional dry etch and E-gun vapor deposition. The current – voltage of the diode shows clear rectifying behavior with turn-on voltages of 1.53 V. Main peak of EL spectrum is in good agreement with the theoretical estimate of ground state energy of 20-nm GaAs/AlGaAs quantum well.
- By using twin-gate structure (surface gate and top gate), the lateral p-i-n junction has also successfully fabrication. The surface gates provide a very good control for the carriers in the channel and at the same time can be put very close to each other. The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts. Therefore, the devices show better characteristics. Full width at haft maximum of EL peak is about 1.2 meV to 3 meV. The narrow linewidths of the peaks demonstrate that the 2-D channel is of high-quality, which is essential for further applications such as electrically-driven single photon sources.
-

5.2 Future Work

We have demonstrated that 2DEG and 2DHG can be induced simultaneously in a same structure and can place closed together to limitation of lithography process (nanometer scale with ebeam lithography). In addition, the devices were fabricated in undoped

structure; so the 2D channel is of high-quality. Therefore, the devices can integrate with other devices to create new devices for different applications such as realization of electrical driven single-photon source device, intrinsic Spin Hall Effect study… Some ideas are given here for future work to look into further possibilities available with the lateral p-i-n junction architecture.

5.2.1 Single-Electron Pump Driven Single-Photon Source

Recently, Kaestner et al. [55] and Fletcher et al. [56] have successfully fabricated a stable single-electron pump on a 2DEG GaAs/AlGaAs heterostructure. Figure 5.1 (a) shows the principle operation of a single electron pump proposed by Fletcher et al. [56]

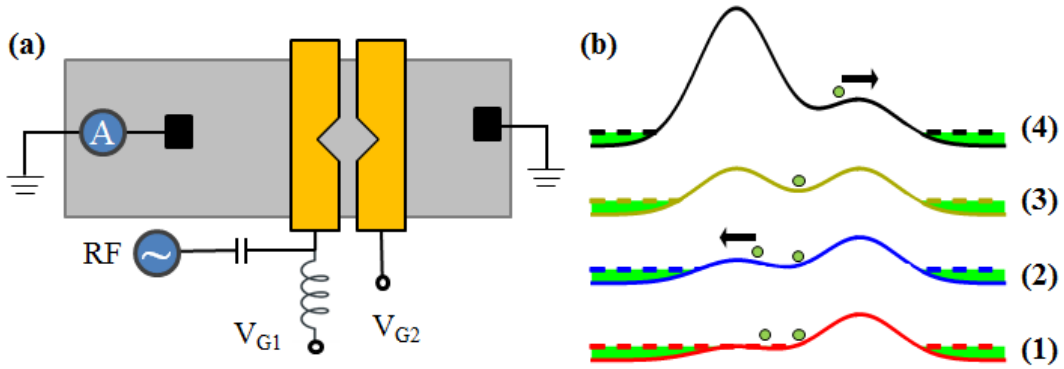


Figure 5.1 (a) Schematic electrical connections. Electrons are pumped from left to right. (c) Potential profile during the pumping cycle (offset vertically): (i) loading, (ii) back-tunneling, (iii) trapping, and (iv) ejection.

Their pumps use a dynamically formed quantum dot defined in a two-dimensional electron gas (2DEG) AlGaAs/GaAs heterostructure by two surface gates (yellow color in the figure 5.1 (a) above). Electron will be pumped from left to right. The gates cross an etch-defined wire terminated with Ohmic electrical contacts. The bias applied to the entrance gate (left) is a ac voltage added to constant voltage V_{G1} while the exit gate (right) is held at constant voltage V_{G2}. Pump operation is illustrated in figure 5.1 (b): (i) When the entrance barrier is in the lowest position, Electrons from the source reservoir (left) are loaded into a quantum dot formed in the space between the gates. (ii) As the entrance barrier rising, some initially trapped electrons tunnel back to the source. (iii) The number of electrons being trapped in every cycle is the same and depends on V_{G1} and V_{G2}. (iv) When the entrance barrier is high enough, trapped Electrons are forced over the exit

barrier into the drain lead, producing a quantized current in an external circuit. By adjusting the values of V_{G1} and V_{G2}, single-electron pump per cycle can be achieved.

We propose a single-electron pump driven single-photon source device, as shown in figure 5.2. The single-electron pump is fabricated on the i-region of the lateral p-i-n junction. Thus, single hot electron can be pumped into 2DHG region and then single photon emitted as electron-hole recombination occurs. In this aspect, high repetition-rate and electrically-driven single photon source could be realized in coming years.

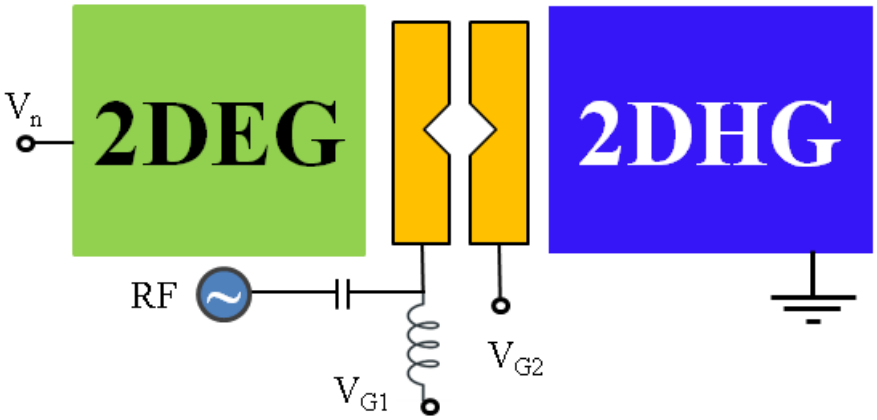


Figure 5.2 Schematic of a single-photon source driven by single-electron pump device.

References

[1] N. Tsutsui, V. Ryzhii, I. Khmyrova, P.O. Vaccaro, H. Taniyama, T. Aida, High-frequency performance of lateral p-n junction photodiodes, Ieee J Quantum Elect, 37 (2001) 830-836.

[2] B. Kaestner, D.A. Williams, D.G. Hasko, Nanoscale lateral light emitting p-n junctions in AlGaAs/GaAs, Microelectron Eng, 67-8 (2003) 797-802.

[3] B. Kaestner, J. Wunderlich, J. Sinova, T. Jungwirth, Co-planar spin-polarized light-emitting diodes, Appl Phys Lett, 88 (2006) 091106.

[4] M. Cecchini, V. Piazza, F. Beltram, M. Lazzarino, M.B. Ward, A.J. Shields, H.E. Beere, D.A. Ritchie, High-performance planar light-emitting diodes, Appl Phys Lett, 82 (2003) 636-638.

[5] G. De Simoni, L. Mahler, V. Piazza, A. Tredicucci, C.A. Nicoll, H.E. Beere, D.A. Ritchie, F. Beltram, Lasing in planar semiconductor diodes, Appl Phys Lett, 99 (2011) 261110.

[6] V. Ryzhii, M. Ryzhii, V. Mitin, T. Otsuji, Terahertz and infrared photodetection using p-i-n multiple-graphene-layer structures, J Appl Phys, 107 (2010) 054512.

[7] J. Wunderlich, B. Kaestner, J. Sinova, T. Jungwirth, Experimental observation of the spin-Hall effect in a two-dimensional spin-orbit coupled semiconductor system, Phys Rev Lett, 94 (2005) 047204.

[8] C.L. Foden, V.I. Talyanskii, G.J. Milburn, M.L. Leadbeater, M. Pepper, High-frequency acousto-electric single-photon source, Phys Rev A, 62 (2000) 011803.

[9] M.I. Dyakonov, V.I. Perel, Possibility of orienting electron spins with current, JETP Lett, 13 (1971) 467-470

[10] M.I. Dyakonov, V.I. Perel, Current-induced spin orientation of electrons in semiconductors, Phys Lett A, 35 (1971) 459-460.

[11] J.E. Hirsch, Spin Hall effect, Phys Rev Lett, 83 (1999) 1834-1837.

[12] S. Murakami, N. Nagaosa, S.C. Zhang, Dissipationless quantum spin current at room temperature, Science, 301 (2003) 1348-1351.

[13] J. Sinova, D. Culcer, Q. Niu, N.A. Sinitsyn, T. Jungwirth, A.H. MacDonald, Universal intrinsic spin Hall effect, Phys Rev Lett, 92 (2004) 126603.

[14] S.F. Zhang, Spin Hall effect in the presence of spin diffusion, Phys Rev Lett, 85 (2000) 393-396.

[15] Y.K. Kato, R.C. Myers, A.C. Gossard, D.D. Awschalom, Observation of the spin hall effect in semiconductors, Science, 306 (2004) 1910-1913.

[16] Technical Report on Quantum Cryptography Technology Experts Panel,

Advanced Research and Development Activity (ARDA), see http://qist.lanl.gov.

[17] A. Ekert, N. Gisin, B. Huttner, H. Inamori, H. Weinfurter, The Physics of Quantum Information, Springer, Berlin-Germany, 2000.

[18] N. Gisin, G.G. Ribordy, W. Tittel, H. Zbinden, Quantum cryptography, Rev Mod Phys, 74 (2002) 145-195.

[19] C.H. Bennett, F. Bessette, G. Brassard, L. Salvail, J. Smolin, Experimental Quantum Cryptography, Lect Notes Comput Sc, 473 (1991) 253-265.

[20] C.H. Bennett, G. Brassard, In Quantum Cryptography: Public Key Distribution and Coin Tossing, in: IEEE International Conference of Computer Systems and

Signal Processing, IEEE, Bangalore, India,, 1984, pp. 175–179.

[21] E. Knill, R. Laflamme, G.J. Milburn, A scheme for efficient quantum computation with linear optics, Nature, 409 (2001) 46-52.

[22] H. Inamori, N. Lutkenhaus, D. Mayers, Unconditional security of practical quantum key distribution, Eur Phys J D, 41 (2007) 599-627.

[23] C.H. Bennett, Quantum Cryptography Using Any 2 Nonorthogonal States, Phys Rev Lett, 68 (1992) 3121-3124.

[24] A.K. Ekert, Quantum Cryptography Based on Bell Theorem, Phys Rev Lett, 67 (1991) 661-663.

[25] A. Stefanov, N. Gisin, O. Guinnard, L. Guinnard, H. Zbinden, Optical quantum random number generator, J Mod Optic, 47 (2000) 595-598.

[26] J.G. Rarity, P.C.M. Owens, P.R. Tapster, Quantum Random-Number Generation and Key Sharing, J Mod Optic, 41 (1994) 2435-2444.

[27] J.R. Gell, P. Atkinson, S.P. Bremner, F. Sfigakis, M. Kataoka, D. Anderson, G.A.C. Jones, C.H.W. Barnes, D.A. Ritchie, M.B. Ward, C.E. Norman, A.J. Shields, Surface-acoustic-wave-driven luminescence from a lateral p-n junction, Appl Phys Lett, 89 (2006) 243505.

[28] G. De Simoni, V. Piazza, L. Sorba, G. Biasiol, F. Beltram, Acoustoelectric luminescence from a field-effect n-i-p lateral junction, Appl Phys Lett, 94 (2009) 121103.

[29] J.M. Ballingall, C.E.C. Wood, Crystal Orientation Dependence of Silicon Autocompensation in Molecular-Beam Epitaxial Gallium-Arsenide, Appl Phys Lett, 41 (1982) 947-949.

[30] D.L. Miller, Lateral P-N-Junction Formation in Gaas Molecular-Beam Epitaxy by Crystal Plane Dependent Doping, Appl Phys Lett, 47 (1985) 1309-1311.

[31] J.R. Gell, M.B. Ward, A.J. Shields, P. Atkinson, S.P. Bremner, D. Anderson, M. Kataoka, C.H.W. Barnes, G.A.C. Jones, D.A. Ritchie, Temporal characteristics of surface-acoustic-wave-driven luminescence from a lateral p-n junction, Appl Phys Lett, 91 (2007) 013506.

[32] A. North, J. Burroughes, T. Burke, A. Shields, C.E. Norman, M. Pepper, The two-dimensional lateral injection in-plane laser, Ieee J Quantum Elect, 35 (1999) 352-357.

[33] D. Reuter, C. Werner, C. Riedesel, A.D. Wieck, D. Schuster, W. Hansen, Fabrication of two-dimensional p-n junctions formed by compensation doping of p-modulation doped GaAs/ln(y)Ga(1-y)As/AlxGa1-x As hetero structures, Physica E, 22 (2004) 725-728.

[34] D. Reuter, C. Werner, A.D. Wieck, S. Petrosyan, Depletion characteristics of two-dimensional lateral p-n-junctions, Appl Phys Lett, 86 (2005) 162110

[35] B. Kaestner, D.G. Hasko, D.A. Williams, Lateral p-n junction in modulation doped AlGaAs/GaAs, Jpn J Appl Phys 1, 41 (2002) 2513-2515.

[36] B. Kaestner, J. Wunderlich, D.G. Hasko, D.A. Williams, Quasi-lateral 2DEG-2DHG junction in AlGaAs/GaAs, Microelectr J, 34 (2003) 423-425.

[37] G.R. Nash, K.J. Nash, S.J. Smith, C.J. Bartlett, J.H. Jefferson, L. Buckle, M.T. Emeny, P.D. Buckle, T. Ashley, Lateral n-i-p junctions formed in an InSb quantum well by bevel etching, Semicond Sci Tech, 20 (2005) 144-148.

[38] S.J. Smith, G.R. Nash, C.J. Bartlett, L. Buckle, M.T. Emeny, T. Ashley, Lateral light emitting n-i-p diodes in InSb/AlxIn1-xSb quantum wells, Appl Phys Lett, 89 (2006) 111118.

[39] R.H. Harrell, K.S. Pyshkin, M.Y. Simmons, D.A. Ritchie, C.J.B. Ford, G.A.C. Jones, M. Pepper, Fabrication of high-quality one- and two-dimensional electron gases in undoped GaAs/AlGaAs heterostructures, Appl Phys Lett, 74 (1999) 2328-2330.

[40] T. Fujii, S. Hiyamizu, S. Yamakoshi, T. Ishikawa, Mbe Growth of Extremely High-Quality Gaas-Algaas Grin-Sch Lasers with a Superlattice Buffer Layer, J Vac Sci Technol B, 3 (1985) 776-778.

[41] O. Wada, T. Sanada, M. Kuno, T. Fujii, Very Low Threshold Current Ridge-Waveguide Algaas Gaas Single-Quantum-Well Lasers, Electron Lett, 21 (1985) 1025-1026.

[42] X.G. Xu, B.B. Huang, H.W. Ren, M.H. Jiang, Smoothing Effect of Gaas Alxga1-Xas Superlattices Grown by Metalorganic Vapor-Phase Epitaxy, Appl Phys Lett, 64 (1994) 2949-2951.

[43] W.T. Masselink, M.V. Klein, Y.L. Sun, Y.C. Chang, R. Fischer, T.J. Drummond, H. Morkoc, Improved Gaas/Aigaas Single Quantum Wells through the Use of Thin Superlattice Buffers, Appl Phys Lett, 44 (1984) 435-437.

[44] P.M. Petroff, R.C. Miller, A.C. Gossard, W. Wiegmann, Impurity Trapping, Interface Structure, and Luminescence of Gaas Quantum Wells Grown by Molecular-Beam Epitaxy, Appl Phys Lett, 44 (1984) 217-219.

[45] Albert G. Baca, C.I.H. Ashby, Fabrication of GaAs devices, The Institution of Engineering and Technology, USA, 2005.

[46] Y. Mori, N. Watanabe, New Etching Solution System, H3po4-H2o2-H2o, for Gaas and Its Kinetics, J Electrochem Soc, 125 (1978) 1510-1514.

[47] Y. Lu, T.S. Kalkur, C.A. Paz de Araujo, Rapid Thermal Alloyed Ohmic Contacts to p-Type GaAs, J Electrochem Soc, 136 (1989) 3123-3129.

[48] Y.C. Shih, M. Murakami, E.L. Wilkie, A.C. Callegari, Effects of Interfacial Microstructure on Uniformity and Thermal-Stability of Aunige Ohmic Contact to N-Type Gaas, J Appl Phys, 62 (1987) 582-590.

[49] www.microchem.com, in.

[50] A. Achoyan, A. Yesayan, É. Kazaryan, S. Petrosyan, Two-dimensional <i>p-n junction under equilibrium conditions, Semiconductors+, 36 (2002) 903-907.

[51] O.A. Tkachenko, V.A. Tkachenko, D.G. Baksheyev, K.S. Pyshkin, R.H. Harrell, E.H. Linfield, D.A. Ritchie, C.J.B. Ford, Electrostatic potential and quantum transport in a one-dimensional channel of an induced two-dimensional electron gas, J Appl Phys, 89 (2001) 4993-5000.

[52] S.E. Laux, D.J. Frank, F. Stern, Quasi-one-dimensional electron states in a split-gate GaAs/AlGaAs heterostructure, Surface Science, 196 (1988) 101-106.

[53] T. Hosey, V. Talyanskii, S. Vijendran, G.A.C. Jones, M.B. Ward, D.C. Unitt, C.E. Norman, A.J. Shields, Lateral n-p junction for acoustoelectric nanocircuits, Appl Phys Lett, 85 (2004) 491-493.

[54] M.A. Herman, D. Bimberg, J. Christen, Heterointerfaces in quantum wells and epitaxial growth processes: Evaluation by luminescence techniques, J Appl Phys, 70 (1991) R1-R52.

[55] B. Kaestner, V. Kashcheyevs, S. Amakawa, M.D. Blumenthal, L. Li, T.J.B.M. Janssen, G. Hein, K. Pierz, T. Weimann, U. Siegner, H.W. Schumacher, Single-parameter nonadiabatic quantized charge pumping, Phys Rev B, 77 (2008).

[56] J.D. Fletcher, M. Kataoka, S.P. Giblin, S. Park, H.S. Sim, P. See, D.A. Ritchie, J.P. Griffiths, G.A.C. Jones, H.E. Beere, T.J.B.M. Janssen, Stabilization of single-electron pumps by high magnetic fields, Phys Rev B, 86 (2012) 155311.

Appendix -1

No	Process	Details	Conditions
Mesa Insolation			
1	Clean the substrate	Acetone, IPA and DI water	3 minutes each in ultrasonic tub
2	Spin resist	Az6112 positive PR	6000 RPM for 45 seconds
3	Hard bake	Hot plate	90 seconds at 90^0C
4	Photolithography exposure	Photolithography makers & Device isolation patterns	2.4 seconds
5	Post exposure bake	Hot plate	60 seconds 90^0C
6	Development	Az300 developer	40 seconds in the developer and 90 seconds in DI water
7	Blow dry	with nitrogen gun	
8	Hard bake	Hot plate	2 minutes at 120 ^{0}C to harden the photoresist and improve adhesion of the photoresist to the wafer surface
9	Wet etch	1:3:50 H_2O_2:H_3PO_4:H_2O solution. 1.8 nm per second rate	220 seconds, etching depth about 400 nm.
10	Remove PR	Acetone	
11	Clean the substrate & blow dry	Acetone, IPA and DI water	2 minutes each in ultrasonic tub
p-type ohmic contacts			
12	Spin resist	Az6112 positive PR	6000 RPM for 45 seconds
13	Hard bake	Hot plate	90 seconds at 90^0C
14	Photolithography exposure	Photolithography makers & p-type ohmic patterns	2.4 seconds
15	Post exposure bake	Hot plate	60 seconds 90^0C

No	Process	Details	Conditions
16	Development	Az300 developer	40 seconds in the developer and 90 seconds in DI water
17	Blow dry	with nitrogen gun	
18	Surface oxide remove	1:10 HCl:H_2O solution	30 seconds
19	Blow dry	with nitrogen gun	
20	Remove residual PR	Oxygen plasma	5 seconds at 20 mTorr pressure and RF power of 60 W
21	Dry etch	$SiCl_4$:Ar with ratio of 24:4 sccm, background pressure 1.5 mTorr	55 seconds with RF power of 30 W, ICP power of 350 W. Etching rate about 6.6 nm/s
22	Surface oxide remove (immediately loaded into chamber afterward)	1:10 HCl:H_2O solution	30 seconds
23	Metal deposition	Pd (40 nm), AuZn (120 nm)	E-gun evaporator at pressure of $2*10^{-6}$ mTorr
24	Lift-off	Acetone	Approximately from 20 to 30 minutes for good lift-off.
25	Clean the substrate (post lift-off) & blow dry	Acetone & DI water	1 minute each in ultrasonic tub
26	Thermal annealing	RTA	2 minutes at 420^0C in nitrogen gas flow
27	Clean the substrate (post lift-off) & blow dry	Acetone & DI water	1 minute each in ultrasonic tub
n-type ohmic contacts			
28	Spin resist	Az6112 positive PR	6000 RPM for 45 seconds

No	Process	Details	Conditions
29	Hard bake	Hot plate	90 seconds at 90^0C
30	Photolithography exposure	Photolithography makers & n-type ohmic patterns	2.4 seconds
31	Post exposure bake	Hot plate	60 seconds at 90^0C
32	Development	Az300 developer	40 seconds in the developer and 90 seconds in DI water
33	Blow dry	with nitrogen gun	
34	Surface oxide remove	1:10 HCl:H_2O solution	30 seconds
35	Blow dry	with nitrogen gun	
36	Remove residual PR	Oxygen plasma	5 seconds at 20 mTorr pressure and RF power of 60 W
37	Dry etch	$SiCl_4$:Ar with ratio of 24:4 sccm, background pressure 1.5 mTorr	55 seconds with RF power of 30 W, ICP power of 350 W. Etching rate about 6.6 nm/s
38	Surface oxide remove (immediately loaded into chamber afterward)	1:10 HCl:H_2O solution	30 seconds
39	Metal deposition	Ni (5 nm), Ge (70 nm), Au (70 nm) & Ni (35 nm)	E-gun evaporator at pressure of $2*10^{-6}$ mTorr
40	Lift-off (immediately after unload from the chamber)	Acetone	Approximately from 20 to 30 minutes for good lift-off.
41	Clean the substrate (post lift-off) & blow dry	Acetone & DI water	1 minute each in ultrasonic tub
42	Thermal annealing	RTA	2 minutes at 450^0C in nitrogen gas flow

No	Process	Details	Conditions
43	Clean the substrate (post lift-off) & blow dry	Acetone & DI water	1 minute each in ultrasonic tub
Surface gate Process			
44	Spin resist	Az5214E negative PR	6000 RPM for 45 seconds
45	Hard bake	Hot plate	90 seconds at 90 ^{0}C
46	Photolithography exposure	Photolithography makers & Surface-gate patterns	2.8 seconds
47	Image reversal bake	Nitrogen gas oven	120 seconds at 120 ^{0}C
48	Flood exposure		13.8 seconds
49	Development	Az300 developer	40 seconds in the developer and 90 seconds in DI water
50	Blow dry	with nitrogen gun	
51	Hard bake	Hot plate	2 minutes at 120 ^{0}C to harden the photoresist and improve adhesion of the photoresist to the wafer surface
52	Gate recess	1:3:50 H_2O_2:H_3PO_4:H_2O solution. 1.8 nm per second rate	90 seconds. Etching depth about 150 nm.
53	Blow dry (immediately loaded into chamber afterward)	with nitrogen gun	
54	Surface gate metallization	Ti (20 nm) & Au (80 nm)	E-gun evaporator at pressure of 2*10^{-6} mTorr
55	Lift-off	Acetone	Approximately from 20 to 30 minutes for good lift-off.
56	Clean the substrate (post lift-off) & blow dry	Acetone & DI water	30 seconds each in ultrasonic tub

No	Process	Details	Conditions
Insulator layer process			
57	Dehydration bake	Nitrogen gas oven	2 minutes at 120 ^{0}C if humidity is above 50%
58	Spin resist	Polyimide Su8-2000.5	3000 RPM for 40 seconds
59	Hard bake	Hot plate	60 seconds at 90 ^{0}C
60	Photolithography exposure	Photolithography makers & isolation layer patterns	5 seconds
61	Post exposure bake	Hot plate	90 seconds at 90 ^{0}C
62	Development	Az300 developer	45 seconds in the developer and 10 seconds in IPA
63	Blow dry	with nitrogen gun	
64	Curing	Furnace with nitrogen flow	30 minutes at 200 ^{0}C with temperature increasing and decreasing rate of 1 ^{0}C/min
Top gate process			
65	Spin resist	Az5214E negative PR	6000 RPM for 45 seconds
66	Hard bake	Hot plate	90 seconds at 90 ^{0}C
67	Photolithography exposure	Photolithography makers & Top-gate patterns	2.8 seconds
68	Image reversal bake	Nitrogen gas oven	120 seconds at 120 ^{0}C
69	Flood exposure		13.8 seconds
70	Development	Az300 developer	40 + 10 seconds in the developer and 90 seconds in DI water
71	Blow dry	with nitrogen gun	
72	Top-gate metallization	Ti (20 nm) & Au (100 nm)	E-gun evaporator at pressure of 2*10^{-6} mTorr
73	Lift-off	Acetone	Approximately from 20 to 30 minutes for good lift-off.
74	Clean the substrate & blow dry	Acetone & DI water	30 seconds each in ultrasonic tub

Vita

Name: Dai Van Truong (戴文長)

Date of birth: 19-11-1981

Place of birth: Vinh Phuc – Viet Nam

Education:

- Vinh Phuc high school, Vinh Phuc – Viet Nam, 1996-1999.
- Department of Physics, Ha Noi National University of Education, Ha Noi - Viet Nam, 1999-2003.
- Institute of Physics, Vietnam Academy of Science and Technology, Ha Noi - Viet Nam, 2004-2006.
- Department of Electronics Engineering, National Chiao Tung University, Hsinchu – Taiwan, 2007 - 2014.

  Ph. D dissertation topic:

  "**Lateral p-i-n diode in an Undoped GaAs/AlGaAs Quantum Well**"

  "無摻雜 GaAs/AlGaAs 量子井之橫向 p-i-n 二極體"

Publication List

[1] **Van-Truong Dai**, Sheng-Di Lin, Shih-Wei Lin, Jau-Yang Wu, Liang-Chen Li and Chien-Ping Lee, *"Lateral Two-Dimensional p–i–n Diode in a Completely Undoped GaAs/AlGaAs Quantum Well"*, Japanese Journal of Applied Physics, pp. 014001-014004, Vol. 52 (2013).

[2] **Van-Truong Dai**, Sheng-Di Lin, Shih-Wei Lin, Yi-Shan Lee, Yin-Jie Zhang, Liang-Chen Li, and Chien-Ping Lee, *"High-quality planar light emitting diode formed by induced two-dimensional electron and hole gases"*, Optics Express, pp. 3811-3817, Vol. 22 (2014).

[3] **Van-Truong Dai**, Sheng-Di Lin, Shih-Wei Lin, Jau-Yang Wu, Liang-Chen Li and Chien-Ping Lee, *"Lateral Two-Dimensional p–i–n Diode in a Completely Undoped GaAs/AlGaAs Quantum Well"*, in The 3rd International Workshop on Nanotechnology and Application, Nov, 2011.

[4]Hien Do, Yue-Han Wu, **Van-Truong Dai**, Chun-Yen Peng, Tzu-Chun Yen, Li Chang, *"Structure and property of epitaxial titanium oxynitride grown on MgO(001) substrate by pulsed laser deposition"*, Surface and Coatings Technology, pp. 91-96, Vol. 214, 2013.

[5] Hien Do, **Van-Truong Dai**, Jr-Sheng Tian, Tzu-Chun Yen, Li Chang, *"Structural and nanoindentation studies of epitaxial titanium oxynitride (001) films grown on MgO(001) substrate"*, Surface and Coatings Technology, pp. 1-6, Vol. 251, 2014.

[6] Gray Lin, **Van-Truong Dai**, and Chien-Ping Lee, *"Modeling the simultaneous two ground-state lasing emissions in chirped quantum dot lasers"*, LEOS Annual Meeting Conference Proceedings, 2009. LEOS '09. IEEE , vol., no., pp.672,674, Oct. 2009

[7] Gray Lin, **Van-Truong Dai**, and Chien-Ping Lee, *"Simulation Analysis of Simultaneous Two Ground-State Lasing Emissions in Chirped Quantum Dot Lasers"*, International Electron Devices and Materials Symposia (IEDMS 2009), Nov. 2009.