國 立 交 通 大 學

材料科學與工程學系

博士論文

銅內連線及低介電常數材料製程整合於高介電常數薄膜電容

Integration of High-*k* MIM Capacitors with Copper Interconnect and Low-*k* Dielectric

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摘要

本研究探討及研發具有高效能及穩定性的銅金屬內連線於先進高介電常數金屬-絕緣層-金屬(MIM)薄膜電容元件應用。以金屬鋁/鉭/金屬銅/鉭 (Al/Ta/Cu/Ta)作為 Ta_2O_5 薄膜電容的底電極，可降低漏電流密度至 $1x10^{-9}$ A/cm^2 並提升崩潰電壓至 5.2 MV/cm。因金屬鋁自身形成緻密且均勻氧化鋁，所以超薄金屬鋁成功地阻絕 Ta_2O_5 中的氧熱擴散至金屬銅層形成氧化銅。此外以低溫短時間的高密度 N_2O 電漿處理 Ta_2O_5 薄膜能有效提升電容效能及元件熱穩定性，降低漏電流密度至 $4x10^{-10}$ A/cm^2。

本研究並研究高介電常數材料鈦酸鍶鋇薄膜(BST)於先進 MIM 薄膜電容的應用。以銅鎂合金[Cu(Mg)]取代金屬銅成為金屬電極，因退火後會生成超薄 MgO 薄膜，能阻絕氧擴散，所以大幅降低漏電流密度。以氮化鉭/銅/氮化鉭(TaN/Cu/TaN)為電極應用於先進高介電常數 BST MIM 電容，結果顯示電容元件具有超高電容密度(11.5 fF/μm^2)。此外，高介電常數材料 BST 薄膜蝕刻及圖型定義亦是研究重

點。以氯為反應氣體雖能有效蝕刻 BST 薄膜，但會殘留含鋇及鍶的化合物，降低元件電容特性。本實驗以氧電漿做蝕刻後處理能修補因蝕刻所造成的薄膜缺陷，降低漏電流密度至 3.0×10^{-8} A/cm^2 及提升崩潰電場強度至 2 MV/cm。

本實驗亦研究銅導線系統中，擴散阻障層與低介電常數材料 SiOC:H 薄膜間的交互作用及穩定性分析，藉銅離子漂移程度探討擴散阻障層效能及元件穩定性。因為在以金屬銅為電極的金屬層-絕緣層-半導體(MIS)結構中，施加正電場於金屬銅會使其分解為銅離子加速擴散至元件中。因此，高穩定性的 MIS 的結構是以金屬銅/氮化鉭/金屬鉭(Cu/TaN/Ta)多層薄膜為電極。此外，研究 N_2O 電漿後處理對擴散阻障層氮化鎢及金屬鎢薄膜的阻障效能影響。結果顯示經電漿後處理的擴散阻障層具有奈米結構表面，能增加元件熱穩定性及阻障效能。本研究並以 Whipple 及 Fick's 第二定律深入分析銅擴散在擴散阻障層的晶粒及晶界擴散因子。

Integration of High-*k* MIM Capacitors with Copper Interconnect and Low-*k* Dielectric

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Advisor: Dr. Chuen-Guang Chao

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A Dissertation

Department of Materials Science and Engineering

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Abstract

We have investigated the characteristics and reliability of high dielectric constant metal-insulator-metal capacitors with copper interconnects. The properties of tantalum oxide (Ta_2O_5) metal-insulator-metal (MIM) capacitors with Al/Ta/Cu/Ta bottom electrodes were investigated. An ultra thin Al film successfully suppresses oxygen diffusion in the Ta_2O_5 MIM capacitor with the Cu-based electrode. The decrease in leakage current is attributed to formation of a dense and uniform Al_2O_3 layer, which has self-protection property and stops further oxygen diffusion into the tantalum contact. Moreover, the electrical characteristics of $Ta/Ta_2O_5/Ta$ capacitors are improved by the treatments with inductively coupled N_2O plasma.

To integrate the high dielectric constant $(Ba,Sr)TiO_3$ (BST) film in the advanced MIM capacitor, Cu(Mg) alloy films have replaced pure Cu films as bottom electrodes for BST capacitors used in high-frequency devices. High-quality characteristics probably follow the formation of a self-aligned MgO layer following the deposition of

a Cu(Mg) alloy by annealing in an oxygen ambient, yielding an electrode with an excellent diffusion barrier and electrical characteristics, which is therefore effective in a BST thin-film capacitor. MIM capacitors made from a BST high-k dielectric film with Cu-based electrodes were also fabricated and demonstrated. The MIM capacitor has a high capacitance density of 11.5 fF/μm^2, a low dissipation factor below 0.03 and small frequency dependence. Furthermore, BST thin films were patterned for fabricating BST capacitors in a helicon-wave plasma system. Some etching residues consisting of Ba and Sr were found after the BST films were etched and increased leakage current density. Oxygen surface plasma treatment can effectively repair surface damage caused by etching, and reduce the leakage current density and increase the breakdown field of the BST capacitor.

To study the high performance Cu metallization in ULSI technology, the interactions between low-*k* material SiOC:H and barrier layers have been investigated. The drift mobility of the Cu^+ ions in the Cu/TaN/Ta-gated capacitor was lower than that in a Cu-gated capacitor. The electric field in the Cu-gated MIS capacitor in the cathode region is believed to be increased by the accumulation of positive Cu^+ ions, which determines the breakdown acceleration. Good Cu^+ ions drift barrier layers are required as reliable interconnects using thin TaN and Ta layers. Thermal stabilities of Cu-contacted n^+-p junctions with tungsten nitride (WN_x) diffusion barriers deposited at various nitrogen flow ratios are investigated. N_2O plasma treatment is applied to improve thermal stability and barrier performance of WN_x film. Meanwhile, N_2O plasma-treated W barrier has a nanostructured surface layer and shows high thermal stability and best barrier properties. Also investigated herein are the lattice and grain boundary diffusivities extracted from the Cu penetration depth profiles using the Whipple analysis of grain boundary diffusion and Fick's second law of diffusion.

Contents

Chapter 3 High Performance and Reliability of High Dielectric Constant (Ba,Sr)TiO_3 Thin-Film Capacitor with Cu-based Electrodes

Table Captions

Chapter 2

Chapter 3

Chapter 5

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Organization of the Thesis

The relentless drive toward high-speed and high-density silicon-based integrated circuits (ICs) has necessitated significant advances in processing technology. The entrance of copper interconnects in IC manufacturing has led to new challenges in metal-insulator-metal (MIM) capacitor fabrication. The requirement to reduce passive chip space has resulted in active researches for MIM with high dielectric constant film. This thesis provides the integration of MIM capacitor with the Cu-based backend of line (BEOL). In Chapter 2 and 3, the integration of MIM capacitors with Cu-based interconnect was investigated, such as high-*k* dielectrics, as shown on mark 1 in **Fig. 1.1**. In Chapter 4 and 5, the integration of Cu-based interconnect was investigated, such as diffusion barriers and low-*k* dielectric materials, as shown on mark 2 in **Fig. 1.1**.

In Chapter 2, the properties of tantalum oxide (Ta_2O_5) MIM capacitors with Al/Ta/Cu/Ta bottom electrodes were investigated. An ultra thin Al film successfully suppresses oxygen diffusion in the Ta_2O_5 MIM capacitor with the Cu-based electrode. The electrical characteristics and reliability of Ta_2O_5 MIM capacitors are improved by addition of ultra thin Al films. Furthermore, the electrical characteristics of $Ta/Ta_2O_5/Ta$ capacitors are improved by the treatments with inductively coupled N_2O plasma. A low-temperature and short process was used to reduce the leakage current and improve the reliability.

In Chapter 3, $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) film has replaced Ta_2O_5 as an insulator for MIM capacitors used in high-frequency devices. The characteristics of high dielectric constant BST with Cu(Mg)/Cu-based gate electrodes have been investigated. The TaN

layer in the MIM capacitor with a Cu-based electrode constitutes a physical layer against the diffusion of oxygen into the bottom electrode. These characteristics make it very suitable for use in silicon integrated circuit applications. Additionally, Cu(Mg) alloy films have replaced pure Cu as bottom electrodes for BST capacitors used in high-frequency devices. Furthermore, BST thin films were patterned for fabricating BST capacitors in a helicon-wave plasma system. Oxygen surface plasma treatment can effectively repair surface damage caused by etching, and reduce the leakage current density of the BST capacitor.

In Chapter 4, the interactions between low dielectric constant material hydrogenated silicon oxycarbide (SiOC:H) and barrier layers have been investigated in Cu metallization. By studying flat band voltage shift in *C-V* and *I-V* tests, it is demonstrated that Cu^+ ions drift into SiOC:H under electric field at elevated temperature. A thin layer of TaN is proven to be good Cu drift barrier layer with SiOC:H dielectrics. Moreover, experiments on bias-temperature stressing, capacitance-voltage measurements, current-voltage characteristics and time-dependent dielectric breakdown were performed to evaluate the reliability of Cu and low-*k* SiOC:H integration.

In Chapter 5, the thermal stabilities of Cu-contacted n^+-p junctions with W-based diffusion barriers are investigated. N_2O plasma-treated W barrier has a nanostructured surface layer and shows high thermal stability and best barrier properties. Also investigated herein are the lattice and grain boundary diffusivities extracted from the Cu penetration depth profiles using the Whipple analysis of grain boundary diffusion and Fick's second law of diffusion. Analysis results indicate that the diffusion models correlate well with experimental results.

In Chapter 6, we conclude our results and summarize the main conclusions.

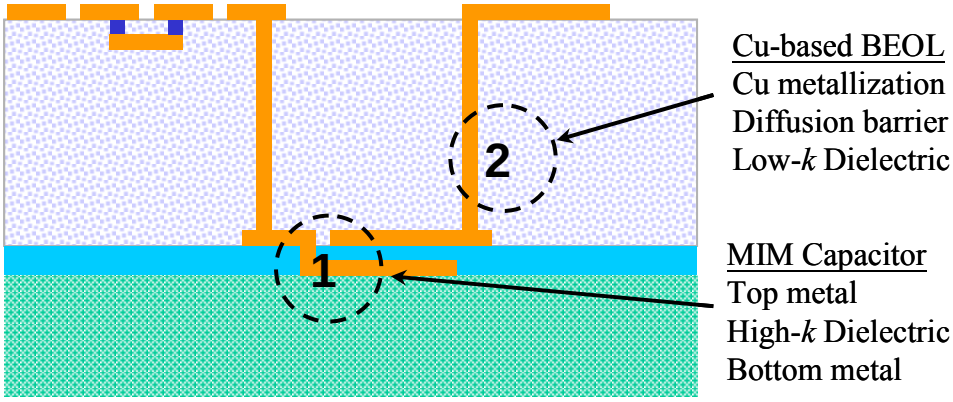


Figure 1.1 Schematic of MIM capacitor in the Cu-based BEOL.

Chapter 2

High Reliability and Performance Ta_2O_5 MIM Capacitor with Cu-based Electrodes

2.1 Introduction

Metal-insulator-metal (MIM) capacitors are used as radio frequency (RF) capacitors in high frequency circuits and analog capacitors in mixed-signal integrated circuit (IC) applications due to their high conductive electrodes and low parasitic capacitance [1-5]. The demand for high-performance capacitors has increased for use as components of system on chip (SoC), which are essential in realizing RF and mixed-signal IC applications, and greater densities of the capacitors allow chips to be shrunk. As the circuit density increases, materials with a dielectric constant (ε) much higher than SiO_2 (~3.9) are desired [6-7]. Among various high-ε dielectric candidates, tantalum pentoxide (Ta_2O_5) has been studied as a promising material for a gate dielectric of MOSFETs because of its high dielectric constant, and excellent thermal and chemical stability [8-15].

2.1.1 Enhancement on the Cu-based Electrode

Current semiconductor technology demands the use of low-resistivity metals as electrode materials for ultra large scale integrated (ULSI) conduction lines and contact structures. In order to minimize the cost of ownership aspect in the electrode processes, several metallization technologies have been proposed in IC applications.

Platinum (Pt) and ruthenium (Ru) have been used as the electrodes of capacitors with high dielectric materials [16-20]. Pt and Ru, however, have limitations for application due to their high resistivity (Pt: ~10.6 μΩ cm, Ru: ~7.7 μΩ cm), cost and leakage current [21]. Cu based metallization technology could be incorporated into devices owing to ease of processing and reduction in production cost of silicon RF capacitors and mixed-signal IC. In addition, Cu has low resistivity (1.67 μΩ cm) and high electro- and stress-migration resistance. However, Cu oxidizes during the initial stage of Ta_2O_5 reactive sputtering, and hillocks or particles are observed after annealing in oxygen ambient [22,23]. Significant efforts have been made to identify an appropriate diffusion barrier layer for Cu-based electrodes. Among these diffusion barrier materials, tantalum (Ta) is selected for Cu-based electrodes, since it not only has low resistivity, but it also is thermodynamically stable with Cu [24-29].

Unfortunately, the grain boundaries of a sputtered Ta layer generally provide paths for oxygen and copper diffusion when formation of Ta_2O_5 dielectrics requires processing under high temperature and oxygen ambient. Protection against oxidation and copper penetration is essential when growing Ta_2O_5 dielectric films on Cu-based electrodes. A capacitor structure using an ultra thin Al layer inserted between Ta_2O_5 dielectric and Ta diffusion barrier is proposed in this study. The improved characteristics of Ta_2O_5 MIM capacitors are investigated.

2.1.2 Improvement on the Ta_2O_5 Film

Tantalum pentoxide (Ta_2O_5) has a higher dielectric constant (20-25), a lower leakage current, greater breakdown strength and a lower loss tangent than other dielectrics [10,12,30-33]. However, the as-deposited Ta_2O_5 films have a large leakage current and poor dielectric breakdown. Several post-annealing treatments have been

suggested to improve the leakage currents of Ta_2O_5 films [9,34-36]. Therefore, annealing is required to improve the electrical characteristics of Ta_2O_5. Conventional furnace annealing usually maintains samples at high temperatures for a long time, and so it is inappropriate for integrated circuit (IC) technology.

Tantalum (Ta) is cheaper than precious metals such as platinum (Pt), palladium (Pd) and their alloys that are responsible for a large part of the production cost of the capacitors, and it is used in an etching process developed for the IC industry. It is therefore a strong candidate to replace precious metal electrodes for ferroelectric and complex oxide thin film-based devices. Additionally, it acts as an effective diffusion barrier at the connection between metals [24-27,37]. In this paper, Ta was used as the electrode material for reactively sputtered Ta_2O_5 metal/insulator/metal (MIM) capacitors, and effects of the Ta electrode on the electrical and dielectric properties of Ta_2O_5 MIM capacitors were investigated.

One important mechanism of current leaks is related to grain boundaries for Ta_2O_5 MIM capacitors. Although high-temperature annealing causes the as-deposited amorphous Ta_2O_5 film to crystallize into a polycrystalline film, it nevertheless generates leakage currents because of the grain boundaries. Previous studies have established that a polycrystalline Ta_2O_5 film that has been annealed at high temperature has a larger leakage current than the amorphous Ta_2O_5 film [9,38-40]. However, problems associated with post-deposition annealing at a low annealing temperature for a short duration is unfavorable for the suppression in the leakage current [41], as the oxidizing gases cannot be easily decomposed into oxygen atoms at low temperatures. This investigation introduces the advantages of post-treatment using an inductively coupled plasma (ICP) system. Previous studies have revealed the use of an ICP system to deposit a dense dielectric film at low temperature, typically as low as room temperature, with a very low chamber pressure in the 1-10 mtorr range

[42-44]. ICP treatment was expected to improve the electrical characteristics of Ta_2O_5 and ensure the reliability of the devices.

2.2 Device Fabrication and Characteristics Measurement

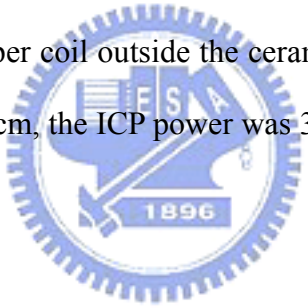
2.2.1 MIM Capacitor with Cu-based Electrode

Thermally grown SiO_2 films were formed on p-type Si (100) substrates for isolation. Three types of Cu-based bottom electrode layers were deposited by sputtering, (a) Cu (300 nm)/Ta (50 nm), (b) Ta (50 nm)/Cu (300 nm)/Ta (50 nm), and (c) Al (20 nm)/Ta (30 nm)/Cu (300 nm)/Ta (50 nm). The Ta film was deposited first and the Al film was the top layer for Al/Ta/Cu/Ta electrode layers. The Al/Ta/Cu/Ta electrode multilayers were formed by sequential sputtering of metal targets without breaking vacuum. Ta_2O_5 films of 40 nm thickness were deposited on Cu-based electrodes by reactive sputtering using a Ta target. During Ta_2O_5 deposition, Ar and O_2 mixture gases were introduced into the chamber to produce a total pressure of 3.5 mTorr. After Ta_2O_5 films were deposited, some wafers were post-annealed at 500-600°C in oxygen ambient for 30 min. Then 50 nm Ta and 100 nm Cu films were deposited sequentially as top electrodes. **Table 2.1** lists the MIM structures with multilayered bottom electrodes in the study.

2.2.2 MIM Capacitor using Low-temperature ICP-N_2O Plasma

To study the effect on the Ta_2O_5 film after plasma treatment, test capacitors with a MIM structure were fabricated on SiO_2 (200 nm)/Si substrates. The Ta bottom electrodes with a thickness of 200 nm were deposited onto SiO_2/Si substrates by dc-magnetron sputtering using a highly pure tantalum target. After electrode deposition, 50 nm-thick Ta_2O_5 thin films were deposited by relative sputtering. The sputtering chamber was evacuated to a base pressure of 1×10^{-7} torr. The films were

prepared at a power of 100 W and a constant pressure of 3.5 mtorr. As-deposited Ta_2O_5 films were subjected to various post treatments to evaluate their effects. These were a) N_2O plasma annealing at 250°C for 5 min in a plasma-enhanced chemical vapor deposition system (PE-N_2O); b) inductively coupled N_2O plasma at 250°C for 5 min in a high-density plasma chemical vapor deposition system (ICP-N_2O); c) annealing in a quartz tube furnace in O_2 ambient at 400°C for 30 min (F-O_2); d) no annealing treatment (reference). **Table 2.2** lists the MIM structures after various plasma treatment in the study Conventional plasma was generated using a radio-frequency (rf, 13.56 MHz) power supply connected to a showerhead plate with a power of 300 W and a N_2O flow rate of 200 sccm in a plasma-enhanced chemical vapor deposition (PECVD) system. In the ICP system, an rf power source (13.56 MHz) is connected to the copper coil outside the ceramic plate of the upper chamber. The N_2O flow rate was 200 sccm, the ICP power was 300 W, and the process pressure was 5 mtorr.



2.2.3 Characteristics Measurement

The film thickness and refractive index were measured by field emission scanning electron microscopy (FESEM, JEOL JSM-6500F) and spectroreflectometry, respectively The samples were investigated by cross-sectional transmission electron microscopy (XTEM) using a field emission microscope (JEOL JEM-2010F) and an acceleration voltage of 200 kV. The samples were prepared by mechanical grinding and polishing followed by ion milling under an acceleration voltage of 3-5 kV in a Gatan Duomill. The surface roughness was elucidated by atomic force microscopy (AFM, Digital Instruments Nano-Scope Ⅲ).Chemical reaction and oxygen penetration profile were characterized by secondary ion mass spectrometry (SIMS,

CAMECA IMS-5F) and X-ray photoelectron spectrometry (XPS). The electrical characteristics of the Ta_2O_5 MIM capacitors versus electric field and time were determined. During the electrical measurements, the top electrode was biased while the bottom electrode was grounded. Current-voltage (*I-V*) characteristics were used to investigate the leakage current and breakdown field. The breakdown field (E_{bd}) was defined as the electrical field when the current density through the dielectric exceeds 10^{-6} A/cm^2. To evaluate the reliability of the Ta_2O_5 film, time dependent dielectric breakdown (TDDB) measurements using constant voltage stress under constant voltage stress using a Hewlett-Packard (HP) 4156B semiconductor parameter analyzer. Capacitors with an area of 3.14×10^{-4} cm^2 were employed.

2.3 Results and Discussion

2.3.1 Ta_2O_5 MIM Capacitor with Cu-based Electrode

2.3.1-1 Physical Characteristic

Figure 2.1 illustrates SEM micrographs of the Ta_2O_5/Ta/Cu/Ta and Ta_2O_5/Al/Ta/Cu/Ta samples after annealing at 600°C in oxygen for 30 min. As displayed in **Fig. 2.1(a)**, the Ta_2O_5/Ta/Cu/Ta sample becomes rugged and forms particles and hillocks on the surface. Normally, oxygen easily penetrates the Ta layer via active diffusion paths and oxidizes the underlying layer. As shown in **Fig. 2.1(b)**, however, no hillocks are observed on the Ta_2O_5/Al/Ta/Cu/Ta sample surface. It indicates that Al/Ta barrier is impermeable to oxygen diffusion and protects the Cu layer underneath from oxidation.

Figure 2.2(a) illustrates the SIMS depth profiles of the O elements in the Ta_2O_5/Ta/Cu/Ta sample following annealing at 500 and 600°C in oxygen ambient. The annealing was performed after the Ta_2O_5 film was deposited. Oxygen diffusion is found after annealing. The oxygen contents in Ta and Cu films increase with increasing annealing temperature. Oxygen atoms will diffuse along the grain boundaries of the Ta crystal and react with the Ta layer during annealing. The high-resolution TEM image in **Fig. 2.2(b)** clearly shows that an interlayer of thickness 4-5 nm is formed between Cu and Ta layers after annealing at 600°C in oxygen. **Figure 2.3(a)** displays the SIMS depth profiles of the O elements in the Ta_2O_5/Al/Ta/Cu/Ta sample after annealing at 500 and 600°C. Almost no indication exist that oxygen atoms diffuse into the Ta and Cu layer. The SIMS observation shown is consistent with the high-resolution TEM micrograph of Ta_2O_5/Al/Ta/Cu/Ta

structures (**Fig. 2.3(b)**) after annealing at 600°C in oxygen. No oxygen defection or reaction is observed between the Ta and Cu layers in the Ta_2O_5/Al/Ta/Cu/Ta samples. Significant improvement in thermal stability is obtained, compared with the samples without thin Al film, apparently owing to the barrier effectiveness of Al/Ta layers. However, the effective dielectric constant is about 18 instead of the value of 25 for pure Ta_2O_5. **Figure 2.4** shows the TEM micrograph of the Cu/Ta/Ta_2O_5/Al/Ta/Cu device after thermal annealing at 600°C and reveals that the ultra thin film with an amorphous structure is formed between Ta_2O_5 and Al layers.

To identify this amorphous layer, the O 1s XPS spectra of Ta_2O_5 films deposited on Ta/Cu/Ta and Al/Ta/Cu/Ta electrodes were analyzed and are depicted in **Fig. 2.5**. Ta_2O_5 films were sputtered onto the electrodes for 5 min to form a layer of Ta_2O_5 of thickness ≤ 10 nm and then both samples were ion etched in order to expose the interfaces of the Ta_2O_5-Ta and Ta_2O_5-Al. The O 1s spectra presented in **Fig. 2.5(a)** show that the oxygen photoelectrons are in the Ta-O state. The standard O 1s peak position is located at ~531 eV. The O 1s spectra presented in **Fig. 2.5(b)** show that the oxygen photoelectrons are in the Ta-O and Al-O states, indicating formation of an Al_2O_3 layer [45]. In fact, formation of a dense monolayer of Al_2O_3 layer results in self-protection to oxidation and stops further oxygen diffusion. The layer behaves as an effective diffusion barrier to protect the underlying Cu and Ta layers [46,47]. The formation of Al_2O_3 is thermodynamically favorable compared to Cu oxide, due to the large difference in oxide formation energy between Al (-226 kcal/g mol O_2) and Cu (-53 kcal/g mol O_2). Therefore, the Al_2O_3 layer will behave as an effective diffusion barrier to protect the underlying Cu and Ta layers.

2.3.1-2 Electrical Characteristics

Figure 2.6 displays leakage current densities of Ta_2O_5 films deposited on Al/Ta/Cu/Ta bottom electrodes after annealing at various temperatures in O_2 ambient. The thickness of the dielectric layer is the total thickness of the Ta_2O_5 and Al_2O_3 films. The leakage current density of the as-deposited Ta_2O_5 film is ~100 nA/cm^2 and decreases to ~1 nA/cm^2 at 1 MV/cm after annealing at 600°C due to elimination of oxygen vacancies and bond defects. Atanassova et al. have reported that oxygen annealing may affect the concentration of the oxygen vacancies and non perfect bonds in the initial layers and consequently leads to leakage current reduction [48]. Several post-deposition treatments were investigated and successfully applied to reduce the oxygen vacancies and improve the electrical properties of Ta_2O_5 thin film [7]. Electrical properties of Ta_2O_5 MIM capacitors with various bottom electrodes, including Cu/Ta, Ta/Cu/Ta, and Al/Ta/Cu/Ta, were further compared and investigated. **Figure 2.7** displays the leakage current densities as a function of electrical field up to 6 MV/cm following annealing at 600°C for 30 min. The leakage current densities are ~250 and 1.2-1.5 nA/cm^2 at 1 MV/cm for Cu/Ta and Ta/Cu/Ta bottom electrodes. The lowest leakage current density of 1 nA/cm^2 is measured for the Al/Ta/Cu/Ta bottom electrode. Also, the leakage current densities of Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes are much lower than those reported by Ezhivalavan and Tseng [22,49]. The breakdown field (E_{bd}) for the Al/Ta/Cu/Ta bottom electrode is approximately 5.2 MV/cm (at 10^{-6} A/cm^2) and higher than those for the Cu/Ta and Ta/Cu/Ta bottom electrodes of around 1.4 and 3.7 MV/cm.

2.3.1-3 Electrical Mechanism

Leakage current is a key parameter for ultra large scale integrated circuit applications. The leakage current in the Ta_2O_5 MIM capacitor may be due to several

mechanisms, including Schottky emission, Poole-Frenkel effect, electronic hopping conduction and tunneling [7,48,50-54]. The leakage current density versus electric field (*J-E*) characteristics of MIM capacitor using bottom and top electrodes of different work function will be highly asymmetric with the voltage polarity for the Schottky emission and symmetric for the Poole-Frenkel emission [55]. In this study, symmetric *J-E* characteristics were observed for Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes and Ta/Cu top electrodes. This behavior indicates that Poole-Frenkel emission is the possible dominant conduction mechanism for leakage currents. The Poole-Frenkel effect predicts a field-dependent behavior of the form

$$J = CE\exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta_{PF}}{kT}E^{1/2}\right) \tag{2.1}$$

where J denotes current density, T denotes the absolute temperature, q is the electronic charge, ϕ_0 is the barrier height, k represents the Boltzmann constant, E represents electric field, C is a constant and β is defined by

$$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2} \tag{2.2}$$

where ε_0 is the permittivity of free space and ε denotes the high-frequency dielectric constant. Poole-Frenkel conduction is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band. **Figure 2.8(a)** shows the logarithmic current density divided by the electric field as a function of the square root of the electric field [ln(*J/E*) vs. $E^{1/2}$]. A good linearity is observed for the field E > 1.5 MV/cm for the plots. Furthermore, the dielectric constant deduced from the slope of the linear region of the Poole-Frenkel emission graph yields an ε value 9.21 almost equal to the measured. The results indicate that the conduction mechanism is dominated by Poole-Frenkel effect for the field E > 1.5 MV/cm. In the case of the Al/Ta/Cu/Ta bottom electrode, the temperature dependence of *J-E*

characteristics of the Ta_2O_5 capacitors was further studied. The leakage current increases exponentially with the temperature, as shown in **Figs. 2.8(b)** and **(c)**. These results reveal that it is affected by trap charge density and the behavior shown in these plots indicates the Poole-Frenkel mechanism.

Figures 2.9(a) and **(b)** illustrate conduction mechanisms of Ta_2O_5 MIM capacitors with Ta/Cu/Ta and Al/Ta/Cu/Ta bottom electrodes. Some activated oxygen in the Ta_2O_5 film could diffuse into the Ta/Cu/Ta bottom electrode and react with the Ta layer during annealing. The oxygen vacancy acts as an electron trap with certain trap level in the energy band diagram. The traps act as stepping sites for electrons and facilitate their transport through the oxide. Moreover, the barrier height becomes low when the oxygen vacancies accumulate at the interface of the Ta_2O_5-metal electrode [56]. Ta/Cu/Ta bottom electrodes could result in more oxygen vacancies at the Ta_2O_5-Ta interface compared to Al/Ta/Cu/Ta bottom electrodes. When the top electrode is positively biased, electrons are relatively easily injected from the Ta/Cu/Ta bottom electrode into the tantalum oxide layer and further conductivity is governed by Poole-Frenkel effect (**Fig. 2.9(a)**). An interfacial Al_2O_3 layer is formed at the Ta_2O_5-Al interface for the Al/Ta/Cu/Ta bottom electrode. The formation of this layer can lead to modification of the conduction mechanism due to the difference in the band gaps of Ta_2O_5 and Al_2O_3. Ta_2O_5 and Al_2O_3 have band gaps of 4.4 and 8.8 eV, respectively [57]. It is found that the dominant conduction mechanism is also Poole-Frenkel effect for the Al/Ta/Cu/Ta bottom electrode from analyses of *J-E* characteristics. However, the interfacial Al_2O_3 layer will result in self-protection to oxidation and stop further oxygen diffusion. Reduction of oxygen vacancies leads to decreasing trap site, and leakage currents of Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes could be reduced.

2.3.1-4 Device Lifetime

Nowadays, the time-dependent dielectric breakdown (TDDB) is an important reliability indicator of the MIM capacitor. **Figure 2.10** illustrates cumulative probabilities of breakdown fields for Ta_2O_5 MIM capacitors with various bottom electrodes. Breakdown is defined as occurring when the leakage current density increases to 10^{-6} A/cm^2. Obviously, the Cu/Ta/Ta_2O_5/Al/Ta/Cu/Ta MIM capacitors exhibit better breakdown behaviors than Cu/Ta/Ta_2O_5/Ta/Cu/Ta and Cu/Ta/Ta_2O_5/Cu/Ta MIM capacitors. **Figure 2.11** shows the TDDB lifetime as a function of electric field for Ta_2O_5 MIM capacitors with various bottom electrodes. The Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes have a longer lifetime than the others. The extrapolated long-term lifetime indicates that the Ta_2O_5 MIM capacitors with the Al/Ta/Cu/Ta bottom electrodes can survive ten years at a stress field of 1.2 MV/cm. Moreover, the plotted points follow straight lines and random failure modes are not observed, indicating the Ta_2O_5 MIM capacitors with the Cu-based bottom electrodes are of high quality and good uniformity.

2.3.2 Ta_2O_5 MIM Capacitor using Low-temperature ICP-N_2O Plasma

2.3.2-1 Electrical Characteristic

Figure 2.12 presents the leakage current densities of the reference, F-O_2, PE-N_2O and ICP-N_2O samples as a function of electric field up to ±4.5 MV/cm. Asymmetric current density vs. electric field (*J-E*) curves are observed. After post treatments, the leakage current is more decreased at a negative bias than at a positive bias. The leakage current at negative bias is influenced primarily by the interface of the Ta_2O_5 and Ta top electrode. The lowest leakage current densities were measured on the ICP-N_2O sample, yielding a value of 4.0×10^{-10} A/cm^2 at an electric field of -1 MV/cm, which is less than 3.8×10^{-9} A/cm^2 for the PE-N_2O sample, 3.8×10^{-7} A/cm^2 for the reference, and 5.7×10^{-8} A/cm^2 for the F-O_2 sample. Also, the leakage current density of the ICP-N_2O sample was lower than that in ref. [49] at an electric field of 1 MV/cm. After the Ta_2O_5 films were deposited, the oxygen escaped and oxygen vacancies were formed, according to,

$$O_o \longleftrightarrow V_o^{"} + 2e^{-} + \frac{1}{2}O_2 \qquad (2.3)$$

where O_o, $V_o^{"}$ and e^{-} represent the oxygen ion in its normal state, an oxygen vacancy and an electron, respectively. A high concentration of oxygen vacancies caused electrons to be generated and a large leakage current to flow. Treatment with oxygen-containing plasma yielded active oxygen atoms and reduced oxygen vacancies, and ultimately improved the quality of Ta_2O_5 films.

Figure 2.12 indicates that ICP-N_2O and PE-N_2O samples have better electrical characteristics than the F-O_2 sample. Many studies presented similar results, and have established that the nitridation and oxidation are controlled by the mobility of

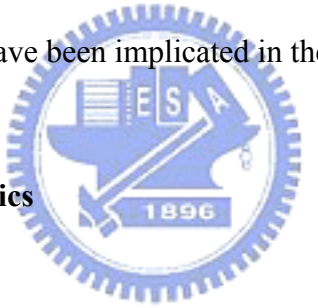
nitrogen- and oxygen-based adatoms during the N_2O plasma treatment [58-62]. N_2O is a stronger oxidizing agent than O_2 because free O atoms are more easily produced according to the reaction [63,64],

$$O_2 \rightarrow 2O \quad (2.4)$$

$$e^- + N_2O \rightarrow NO + N + e^- \quad (2.5)$$

$$N + NO \rightarrow N_2 + O \quad (2.6)$$

The activation energy in Eq. (2) is 5.12 eV, whereas that in Eqs. (3) and (4) is 2.51 eV. This result can be easily explained by the fact that less energy is required to break the N-O bond in a N_2O molecule than the O=O bond in an O_2 molecule. The excited oxygen atoms diffused rapidly into the Ta_2O_5 films and reduced the degree of imperfection and the concentration of oxygen vacancy. In addition, atomic N and surface-generated ions (NO) have been implicated in the nitridation process.



2.3.2-2 Physical Characteristics

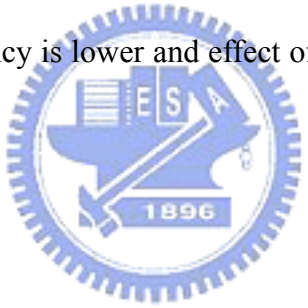
Figure 2.13 illustrates the SIMS depth profiles of the O elements in the F-O_2 and ICP-N_2O samples. The apparent oxygen diffusion is found in F-O_2 sample due to the oxygen atoms diffuse along the grain boundaries of the Ta crystal and react with the Ta layer during annealing. Nevertheless, almost no indication exists that oxygen atoms diffuse into the Ta layer in ICP-N_2O sample due to low-temperature plasma treatment.

The leakage current density in the ICP-N_2O sample is much lower than that in the PE-N_2O sample at a negative bias, as displayed in **Fig. 2.12**. The influence of N_2O plasma on Ta_2O_5 layer increases the concentration of oxygen atoms (or reduces the number of oxygen vacancies) in the Ta_2O_5 film. A PECVD system cannot generate high-density plasma. In fact, generating plasma even in a magnetic field at a chamber

pressure of only a few mtorr is very difficult [65]. In an ICP system, a flowing RF current in the coils easily generates a changing magnetic field, which in turn induces a changing electric field through inductive coupling. Therefore, the inductively coupled electric field accelerates electrons at low pressure. The electronic mean free path may be shorter than the gap between the electrodes, so enough ionizing collisions occur. Hence, inductively coupled plasma reactors produce a high electron temperature that efficiently dissociates the N_2O gas under pressure and causes more O radicals and ions to be present. Previous studies demonstrated that the oxidant produced under high-density plasma discharge is more reactive than the primary reactant used in plasma O_2 annealing [66]. Accordingly, the high concentration of oxidants may explain why the leakage current density in the ICP-N_2O sample is lower than that in the PE-N_2O sample. Another reason may be the resulting roughness of the Ta_2O_5 layer. The Ta_2O_5 surfaces of the F-O_2 and PE-N_2O samples are clearly rougher than that of the ICP-N_2O sample, as displayed in **Fig. 2.14**. It is believed the reactions or bombardments of energetic radicals and ions would occur during plasma treatment. They could sputter the films and make them smooth. The roughness effect can be interpreted as an image force that reduces the barrier height [11,67]. **Table 2.3** summaries the electrical properties of Ta/Ta_2O_5/Ta capacitors with various post treatments. The breakdown field is defined as the electric field when leakage current density exceeds 10^{-6} A/cm^2 under a positive bias. The breakdown fields of the reference and the F-O_2 samples are approximately 1.2-1.9 MV/cm and that of the PE-N_2O sample is 2.7 MV/cm. The excellent breakdown field of the ICP-N_2O sample is 4.2 MV/cm. The improvement in breakdown field is attributed to the reduced surface roughness after treatments. A smooth surface can suppress the local accumulation of electrons and is responsible for the uniform electric field, and hence the ICP-N_2O sample has a high breakdown field.

2.3.2-3 Plasma Treatment Mechanism

Figure 2.15 depicts the proposed schematic diagram of N_2O plasma treatment on the Ta_2O_5 film based on the above results. Plasma treatment modifies the surface and causes ion bombardment effects. The principal dissociation products (N, O, and NO) of N_2O would modify the surface of Ta_2O_5 films. The O atoms were accelerated toward the Ta_2O_5 film, where they were adsorbed and incorporated in oxygen vacancies. The dissociation of gas importantly affects the results of plasma treatment. The leakage current density of the ICP-N_2O sample is one order of magnitude lower than that of the PE-N_2O sample at an electric field of -1 MV/cm, because the concentration of oxygen vacancy is lower and effect of nitridation is higher following ICP than PE treatment.



2.3.2-4 Device Lifetime

Figure 2.16 shows the leakage current density versus time characteristics at high stress electric fields. At the beginning of the stress test, the leakage current fell rapidly. The decrease in the leakage current was believed to be caused by electron trapping [68-70]. The drop was gradual during the middle stage of the stress test. However, the leakage current rapidly increased and fatal breakdown occurred after the stress was applied for a longer period. Fatal breakdown is defined as leakage current density increases to 10^{-3} A/cm^2 or ten times higher than the value at the previous one second time step. The data indicates that lower leakage films have longer breakdown lifetime. The ICP-N_2O sample has a lower leakage current and longer breakdown lifetime under the stress at a constant electric field of 1.8 MV/cm. The leakage

currents in F-O_2 and PE-N_2O samples are higher and associated with a shorter time to breakdown at constant fields of 1.2 and 1.6 MV/cm, respectively. Breakdown is manifested by the formation of a conductive path through the oxide initiated by the presence of weak spots [48]. Local field enhancements at the weak spots cause vacancy-related breakdowns. The high-density local vacancies, including traps, are responsible for vacancy-related breakdown. Furthermore, TDDB lifetime was studied under various equivalent electric fields. The ICP-N_2O sample exhibits a longer-term reliability than the PE-N_2O, F-O_2, and reference samples and the samples in ref. [49]. The extrapolated long-term lifetime demonstrates that the ICP-N_2O sample can survive 10 years at a stress field of 1.61 MV/cm, as listed in **Table 2.3**.

2.3.2-5 Electrical Mechanism

The leakage current in the $Ta/Ta_2O_5/Ta$ capacitor may be due to several mechanisms, including Schottky emission, Poole-Frenkel effect, electronic hopping conduction and tunneling [9,48,50-53]. The leakage current density versus electric field (*J-E*) characteristics of MIM capacitor will be highly asymmetric with the voltage polarity for the Schottky emission. In this study, asymmetric *J-E* characteristics were observed, as shown in **Fig. 2.12**. The Schottky current is due to electrons which transit above the potential barrier at the surface of a metal or semiconductor, and is typical of the electrode-limited current. A current density-electric field relation for Schottky emission is given by the following equation [9,50].

$$J = AT^2 \exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta}{kT}E^{1/2}\right) \qquad (2.7)$$

Where J is the current density; A is a constant; T denotes the absolute temperature;

q is the electronic charge; ϕ_0 is the barrier height; k represents the Boltzmann constant; E represents the electric field, and β is defined as

$$\beta = \left(\frac{q^3}{4\pi\varepsilon_0 \varepsilon} \right)^{1/2} \tag{2.8}$$

Where ε_0 is the permittivity of free space and ε represents the high-frequency dielectric constant. **Figure 2.17** shows the logarithmic current density as a function of the square root of the electric field [log(J) vs. $E^{1/2}$]. A good linearity is observed for the plots, indicating that the Schottky emission is the possible dominant conduction mechanism for leakage currents, whereby electrons from the cathode overcome the Ta/Ta_2O_5 energy barrier before being emitted into the Ta_2O_5. The Schottky emission can be explained when an electron enters the dielectric, it produces an image field that adds and lowers the barrier field, resulting in a reduced barrier height and an enhanced current given.

Figures 2.18(a) and **(b)** illustrate conduction mechanisms of Ta/Cu/Ta capacitors with O_2 furnace annealing and inductively coupled N_2O plasma post-treatments, respectively. The Schottky emission is the possible dominant conduction mechanism for leakage currents. Surface roughness and oxygen vacancy are attributed to resulting conduction mechanism in the study. The F-O_2 sample has a rougher surface than the ICP-N_2O sample, as shown in **Fig. 2.14**. It was reported that surface roughness yields on the image potential were as high as high as even 10%-60% compared to that of a flat interface [11]. Some activated oxygen in the Ta_2O_5 film could diffuse into and react with the Ta bottom electrode layer during annealing. The oxygen vacancy acts as an electron trap with certain trap level in the energy band diagram. The traps act as stepping sites for electrons and facilitate their transport through the oxide. A thin highly oxygen-deficient layer remains in the tantalum oxide film adjacent to the Ta electrode for the F-O_2 sample, as shown in

SIMS analyses of **Fig. 2.13**. The barrier height becomes low when the oxygen vacancies accumulate at the interface of the Ta_2O_5-metal electrode [37,56]. The F-O_2 sample has a higher interfacial barrier compared to the ICP-N_2O sample due to higher surface roughness and oxygen vacancy concentration, as shown in **Fig. 2.18**. When the top electrode is negatively biased, electrons are relatively easily injected from the Ta top electrode into the tantalum oxide layer and further conductivity is governed via trap sites.

2.4 Summary

Multilayered Al/Ta/Cu/Ta electrodes enhance the properties of the Ta_2O_5 MIM capacitors with Cu-based electrodes. This work found that the capacitors demonstrated a significant improving capability against oxygen diffusion after inserting an Al film. This improvement is attributed to a dense Al_2O_3 film formed on the surface of the Al/Ta/Cu/Ta bottom electrode after thermal annealing in oxygen ambient. Ultra-low leakage current density (1 nA/cm^2 at 1 MV/cm) and high breakdown field (5.2 MV/cm at 10^{-6} A/cm^2) are obtained for Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta electrodes because of reducing oxygen vacancy in tantalum oxide films. Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta electrodes also show less charge trapping and better TDDB properties. Al/Ta/Cu/Ta electrodes enable the integration of Cu electrodes with high-dielectric constant tantalum oxide thin films for high-frequency devices at interconnect levels.

The electrical properties of Ta_2O_5 thin films with MIM structures following the inductively coupled N_2O plasma (ICP-N_2O) post treatments were examined. The resulting Ta/Ta_2O_5/Ta capacitors have low leakage current densities (4.0×10^{-10} A/cm^2 under 1 MV/cm), high breakdown fields (4.2 MV/cm at 10^{-6} A/cm^2), and lifetimes of over 10 years at 1.61 MV/cm due to effectively dissociated N_2O gas and reduced bombardment. The leakage current of the Ta/Ta_2O_5/Ta capacitor is dominated by Schottky emission. Oxygen vacancy and surface roughness are attributed to resulting conduction mechanism in the study. The low-temperature ICP system reduces the diffusion of oxygen atoms into the Ta bottom electrode, and lessens to the oxygen vacancies, while, the reactions of energetic radicals and ions reduce surface roughness. Consequently, the electrical characteristics and reliability of Ta/Ta_2O_5/Ta capacitors are enhanced after the low-temperature ICP treatments.

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Table 2.1 MIM capacitors with various multilayered bottom electrodes used in the study.

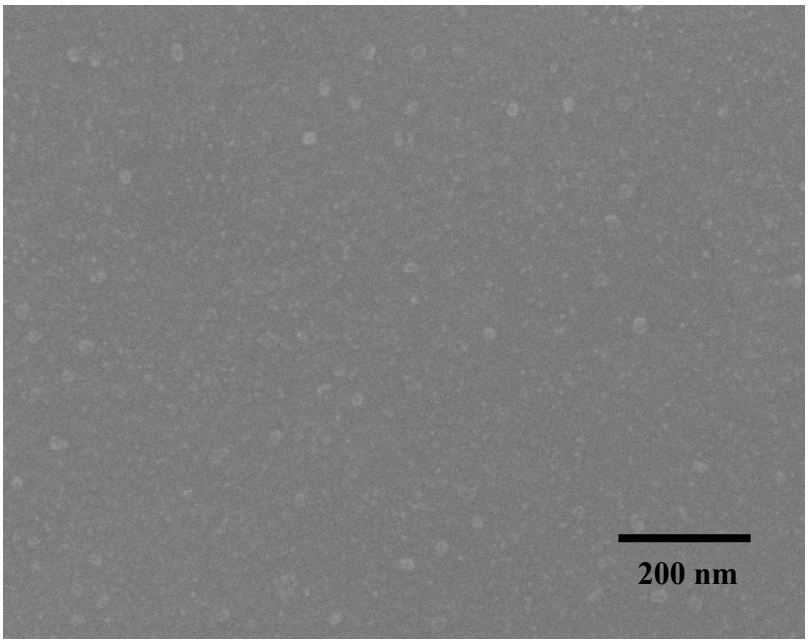
Sample	Top electrode (nm)	Insulator (nm)	Bottom electrode (nm)
(a)	Cu (100) / Ta (50)	Ta_2O_5 (40)	Cu (300) /Ta (50)
(b)	Cu (100) /Ta (50)	Ta_2O_5 (40)	Ta (50) /Cu (300) /Ta (50)
(c)	Cu (100) /Ta (50)	Ta_2O_5 (40)	Al (20) /Ta (30) /Cu (300) /Ta (50)

Table 2.2 MIM capacitors with various plasma treatments in the study.

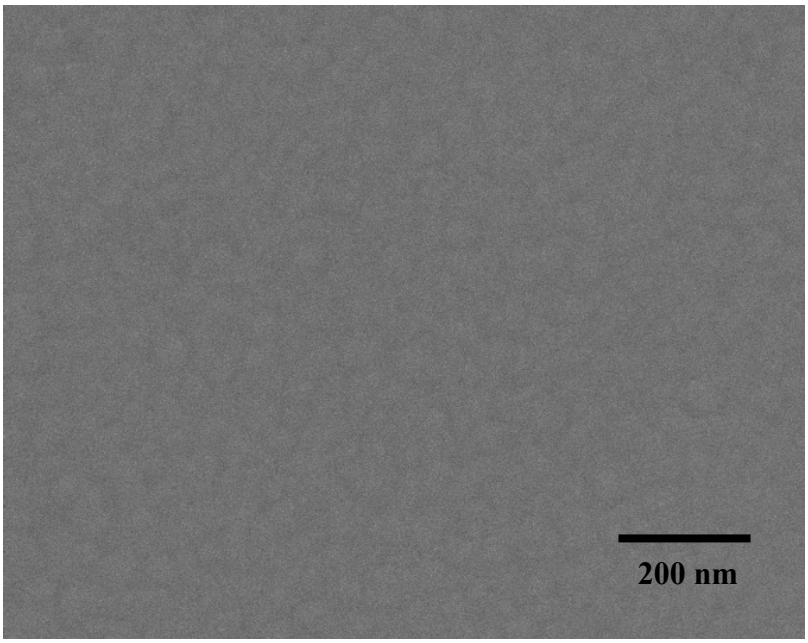
Sample	MIM	equipment	condition
(a)	PE-N_2O	plasma-enhanced chemical vapor deposition	N_2O, 250°C, 5 min
(b)	ICP-N_2O	high-density plasma chemical vapor deposition system	N_2O, 250°C, 5 min
(c)	F-O_2	quartz tube furnace	O_2, 400°C, 30 min
(d)	Reference	No	No

Table 2.3 Properties of $Ta/Ta_2O_5/Ta$ capacitors with various post treatments.

	Reference	F-O_2	PE-N_2O	ICP-N_2O
Roughness (nm)	1.53	1.35	0.75	0.45
Leakage current (A/cm^2) at E = 1 MV/cm	4.5×10^{-7}	2.4×10^{-7}	2.7×10^{-8}	2.1×10^{-8}
Leakage current (A/cm^2) at E = -1 MV/cm	3.8×10^{-7}	5.7×10^{-8}	3.8×10^{-9}	4.0×10^{-10}
Breakdown field (MV/cm) at 10^{-6} A/cm^2 under a negative bias	1.2	1.9	2.7	4.2
Breakdown field (MV/cm) at 10^{-6} A/cm^2 under a positive bias	1.2	1.9	3	3.4
Dielectric constant	~19	20-23	19-21	19-21
Electric field of 10-year lifetime (MV/cm)		0.87	1.23	1.61

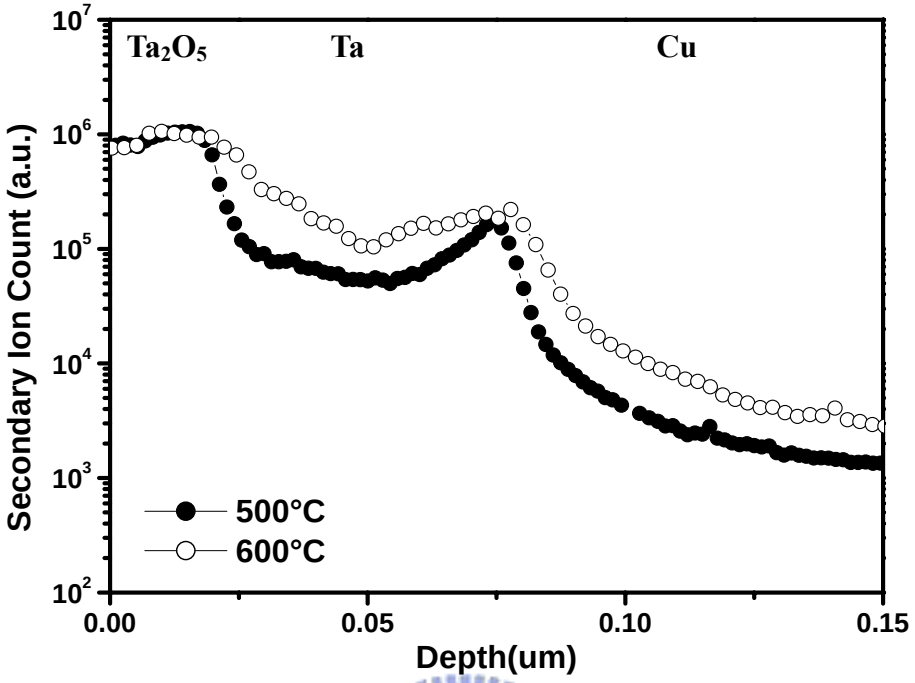


(a)

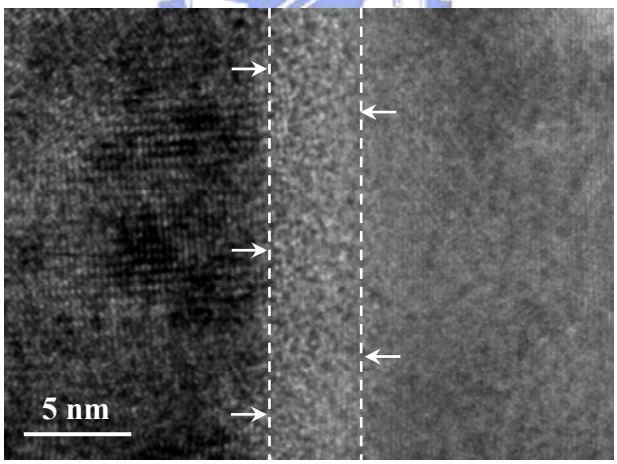


(b)

Figure 2.1 SEM images of the Ta_2O_5 films on (a) Ta/Cu/Ta and (b) Al/Ta/Cu/Ta bottom electrodes after annealing at 600^{o}C for 30 min in oxygen ambient.

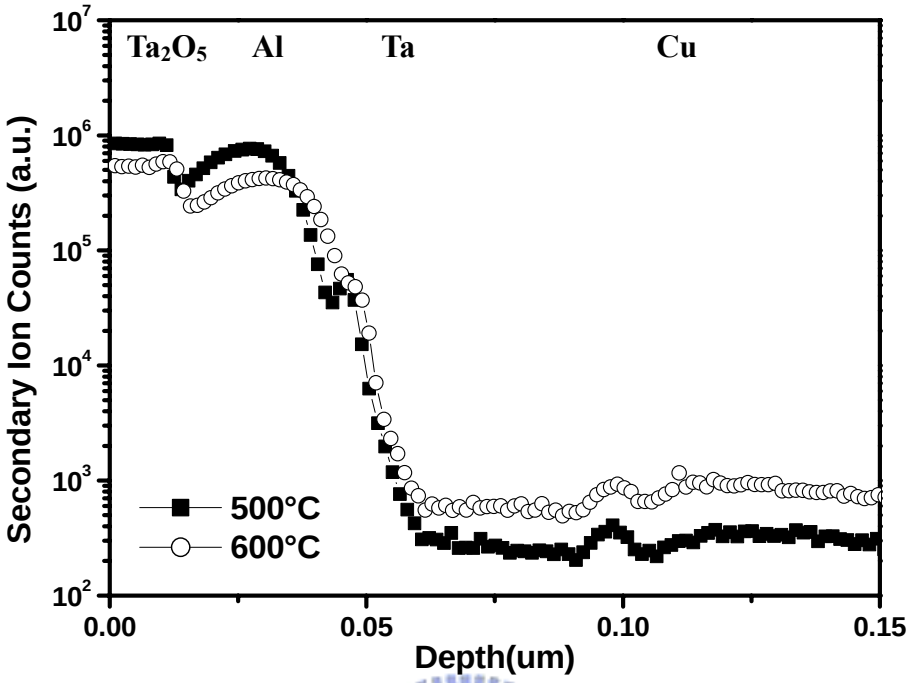


(a)

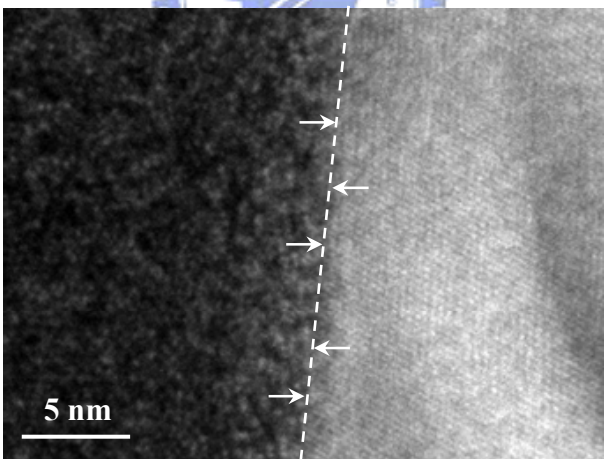


(b)

Figure 2.2 (a) SIMS depth profiles of O elements in the Ta_2O_5/Ta/Cu/Ta samples after furnace annealing at 500 and 600°C for 30 min in oxygen ambient. (b) High-resolution TEM image of the interlayer between Ta and Cu layers in the Ta_2O_5/Ta/Cu/Ta sample.



(a)



(b)

Figure 2.3 (a) SIMS depth profiles of O elements in Ta_2O_5/Al/Ta/Cu samples after furnace annealing at 500 and 600°C for 30 min in oxygen ambient. (b) High-resolution TEM image of the region between Ta and Cu layers in the Ta_2O_5/Al/Ta/Cu/Ta sample.

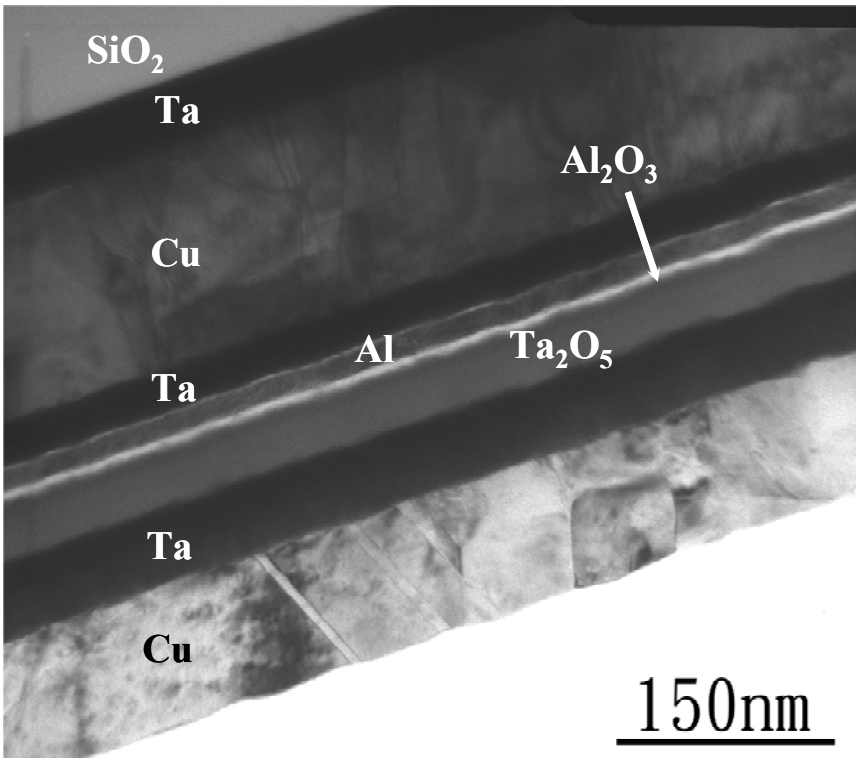
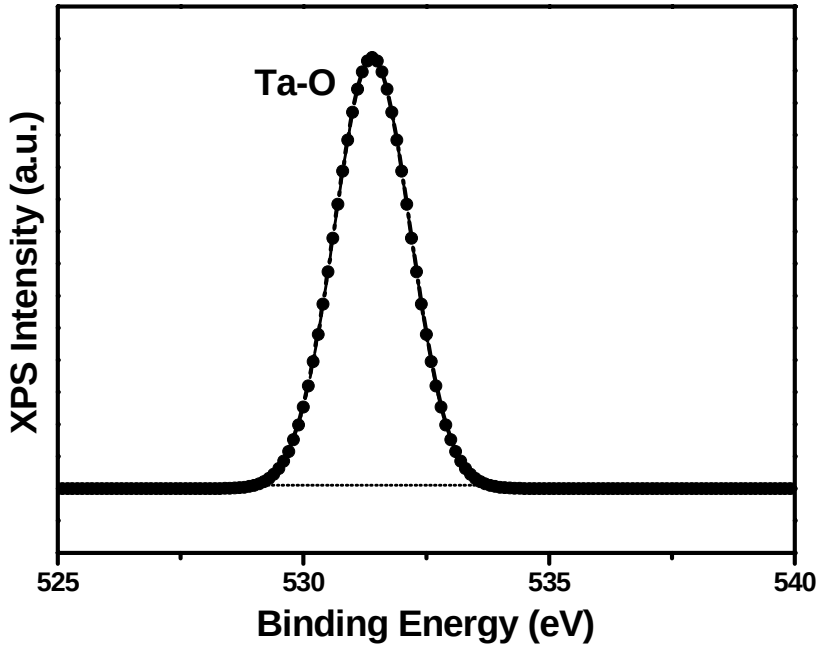
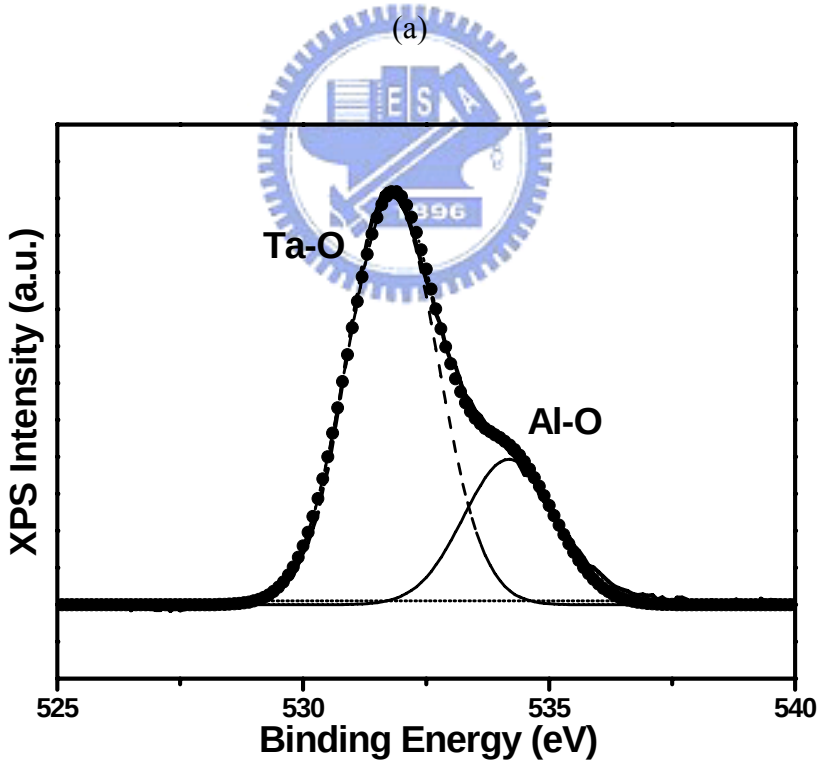


Figure 2.4 TEM image of the Cu/Ta/Ta_2O_5/Al/Ta/Cu/Ta MIM capacitor. The annealing was conducted at 600°C for 30 min in oxygen ambient after Ta_2O_5 film was deposited.



(a)



(b)

Figure 2.5 O 1s XPS spectra obtained from (a) Ta_2O_5-Ta interface for the Ta_2O_5/Ta/Cu/Ta sample and (b) Ta_2O_5-Al interface for the Ta_2O_5/Al/Ta/Cu/Ta sample.

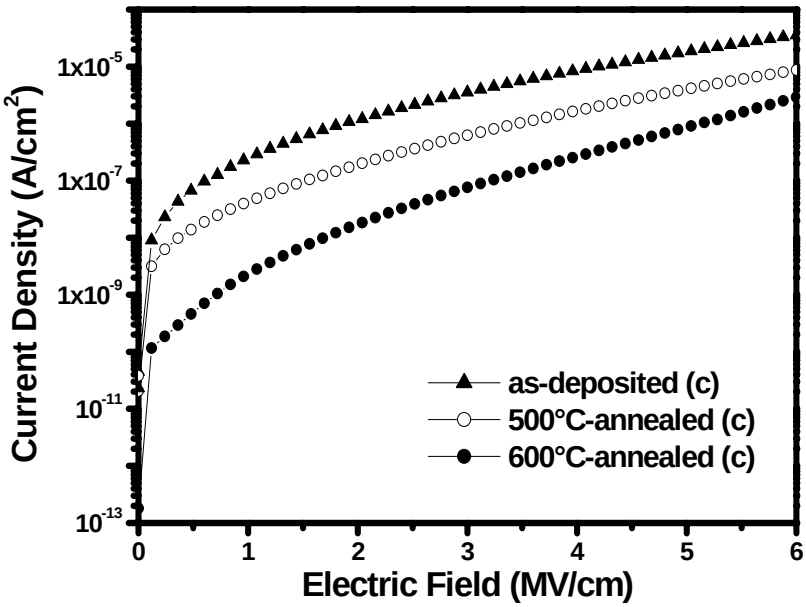


Figure 2.6 Current density-electric field (*J-E*) characteristics of the Cu/Ta/Ta_2O_5/Al/Ta/Cu/Ta MIM capacitors after annealing at various temperatures in oxygen ambient for 30 min.

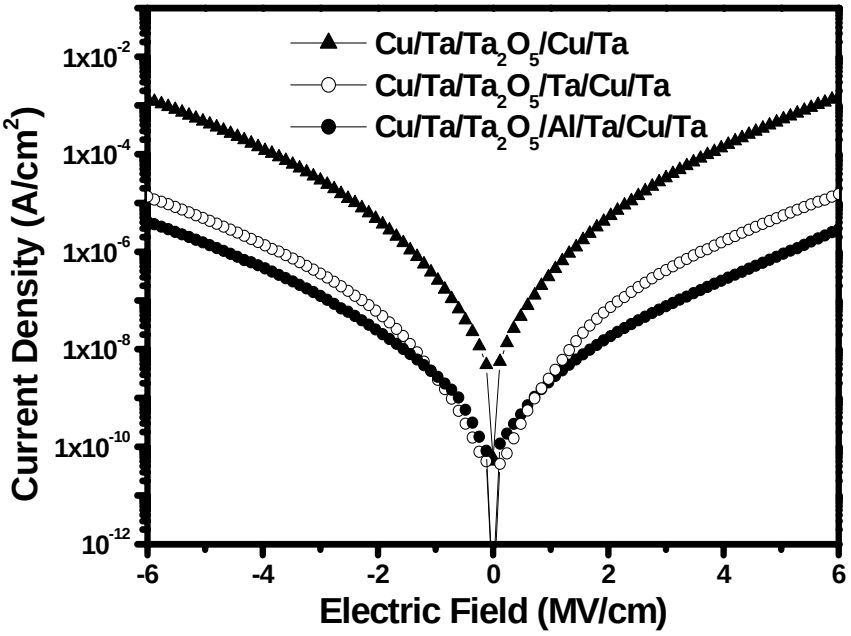
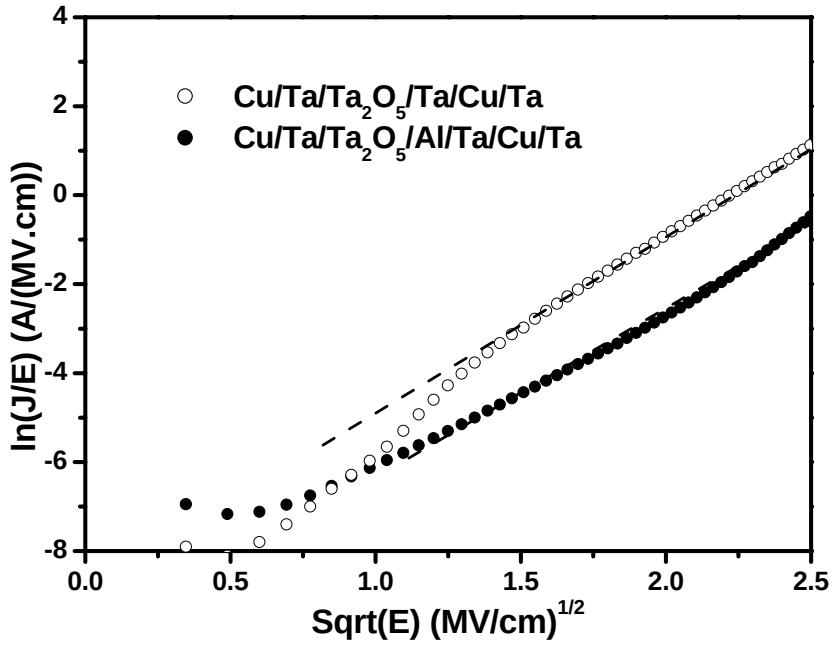
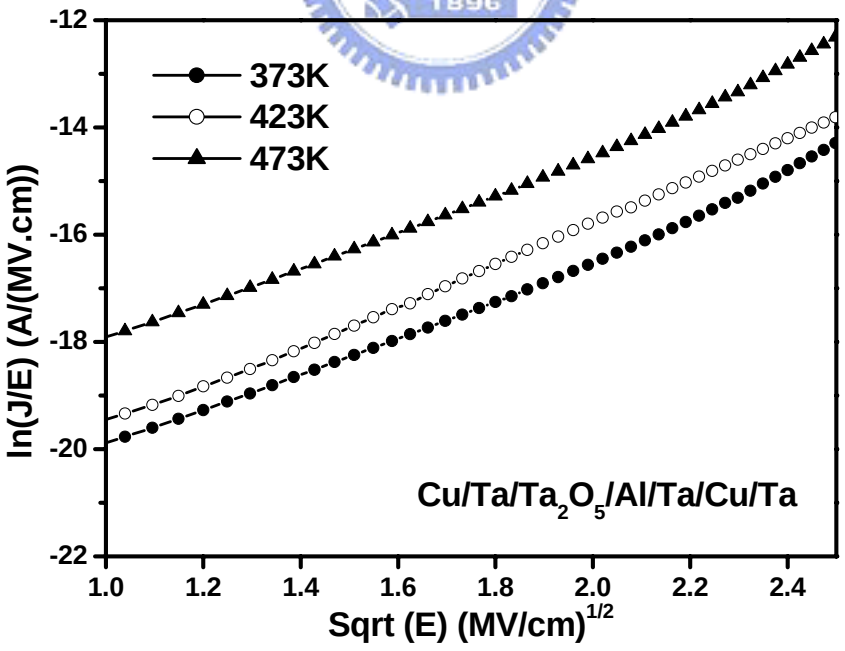


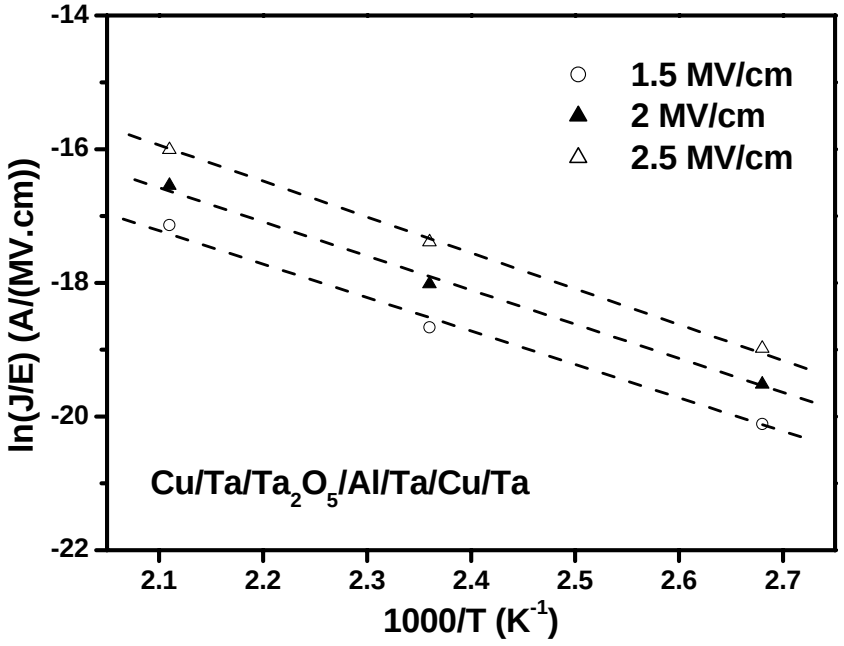
Figure 2.7 Current density-electric field (*J-E*) characteristics of the Ta_2O_5 MIM capacitors with various bottom electrodes after annealing at 600°C in oxygen ambient for 30 min.


Cu/Ta/Ta2O5/Ta/Cu/Ta
Cu/Ta/Ta2O5/Al/Ta/Cu/Ta
ln(J/E) (A/(MV.cm))
Sqrt(E) (MV/cm)1/2
4
2
0
-2
-4
-6
-8
0.0
0.5
1.0
1.5
2.0
2.5

(a)

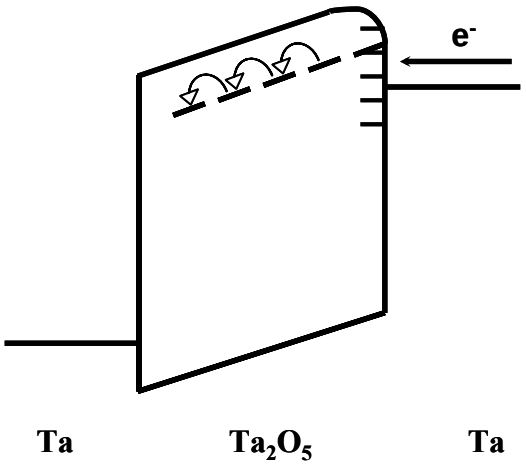

373K
423K
473K
Cu/Ta/Ta2O5/Al/Ta/Cu/Ta
ln(J/E) (A/(MV.cm))
Sqrt (E) (MV/cm)1/2
-12
-14
-16
-18
-20
-22
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4

(b)

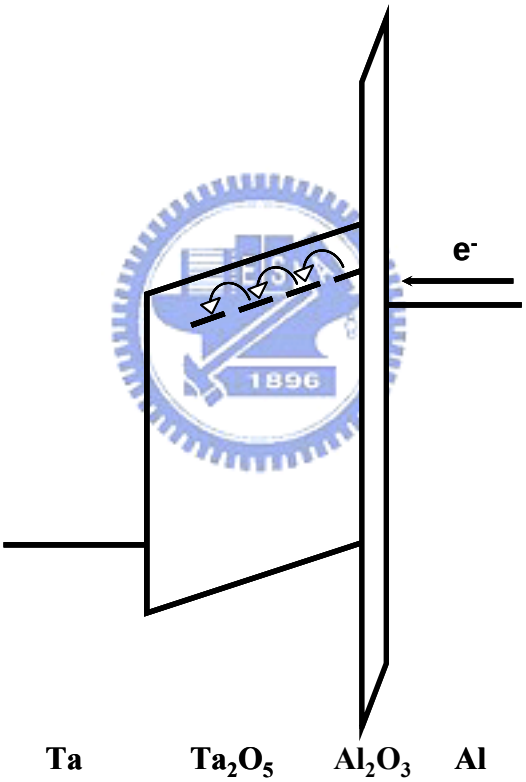


(c)

Figure 2.8 (a) The ln(*J*/*E*) versus $E^{1/2}$ plots for the Ta_2O_5 MIM capacitors. (b) The ln(*J*/*E*) versus $E^{1/2}$ plots for the Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes at various measurement temperatures. (c) The ln(*J*/*E*) vs 1000/*T* plots for the Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta bottom electrodes.



(a)



(b)

Figure 2.9 Schematic illustration of conduction mechanisms in Ta_2O_5 MIM capacitors with (a) Ta/Cu/Ta and (b) Al/Ta/Cu/Ta bottom electrodes biased at a positive voltage.

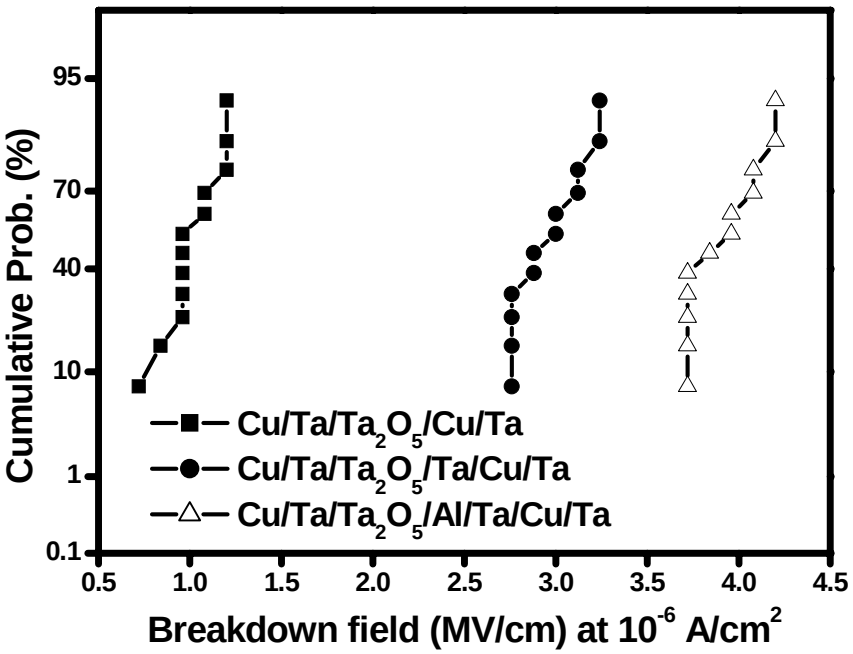


Figure 2.10 Cumulative probabilities of breakdown fields for Ta_2O_5 MIM capacitors with various bottom electrodes.

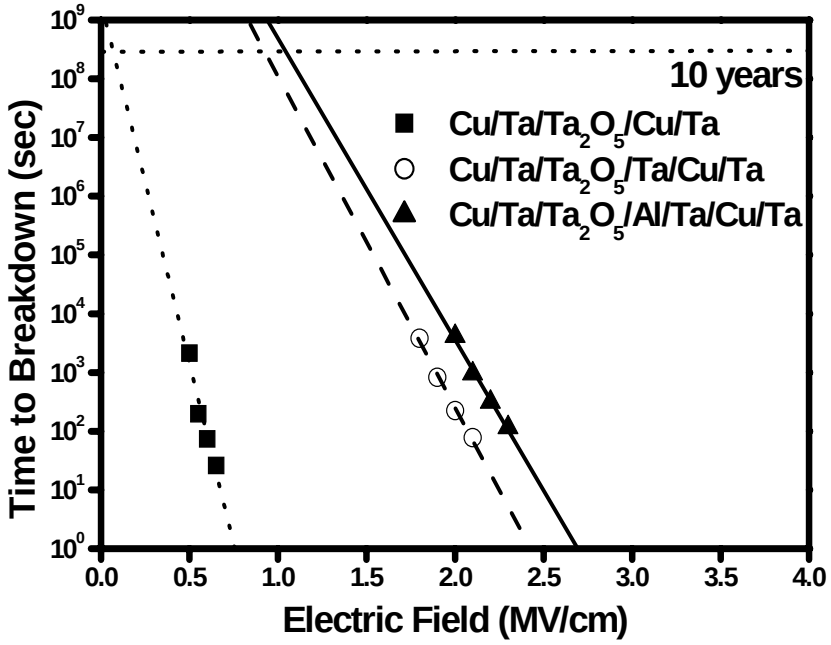


Figure 2.11 TDDB lifetime as a function of electric field for Ta_2O_5 MIM capacitors with various bottom electrodes.

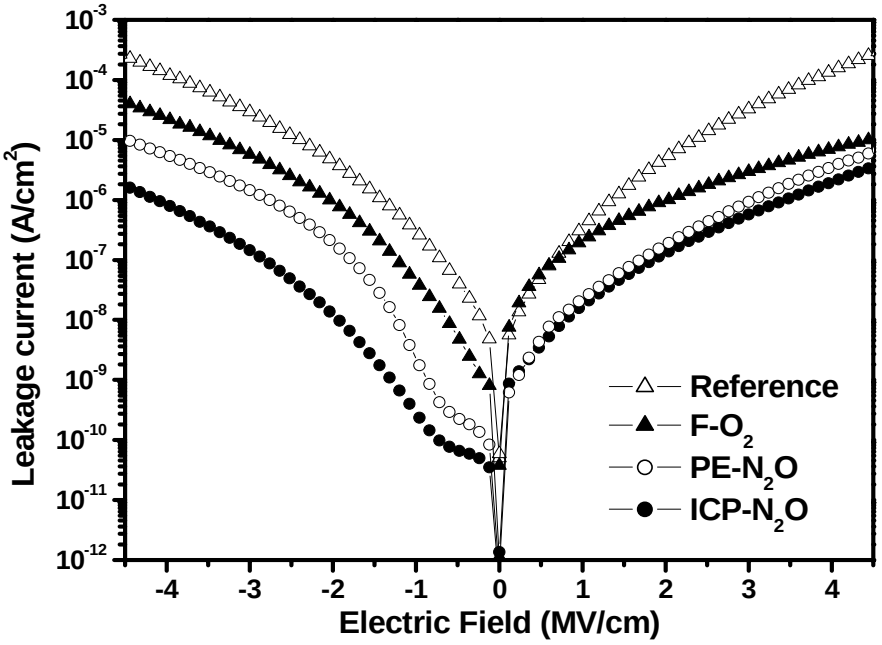


Figure 2.12 Leakage current densities of the $Ta/Ta_2O_5/Ta$ capacitors before and after various post treatments.

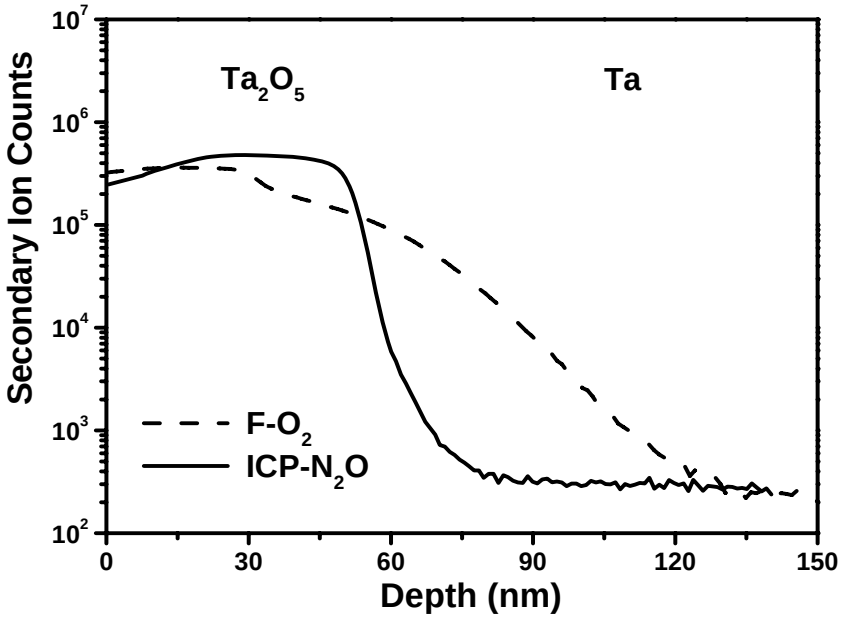
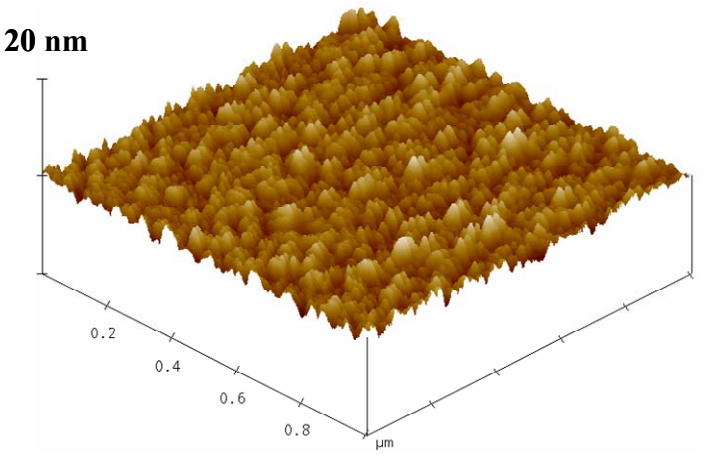
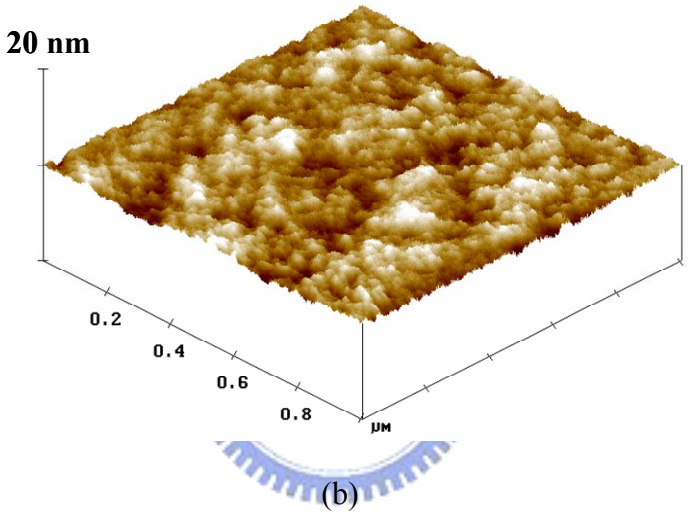


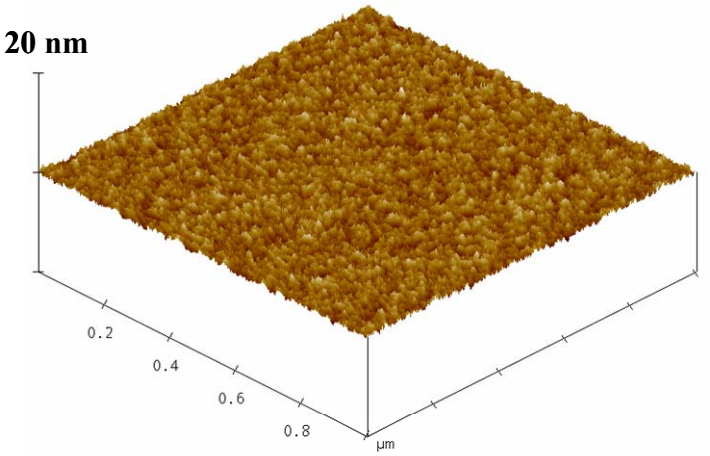
Figure 2.13 SIMS depth profiles of oxygen elements in Ta/Ta_2O_5/Ta capacitors after furnace annealing at 400°C for 30 min and ICP treatment at 250°C for 5 min.



(a)



(b)



(c)

Figure 2.14 AFM images of Ta_2O_5 surfaces after (a) furnace annealing at 400°C for 30 min, (b) PE treatment at 250°C for 5 min, and (c) ICP treatment at 250°C for 5 min.

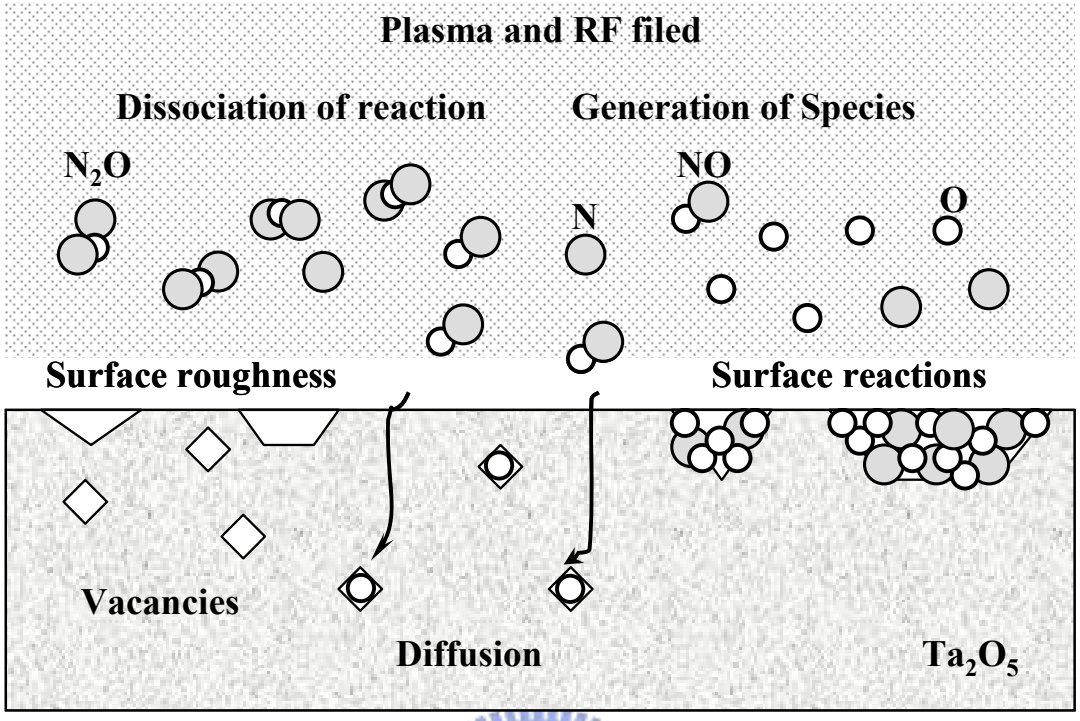


Figure 2.15 Schematic illustration for N_2O plasma treatment on the Ta_2O_5 film.

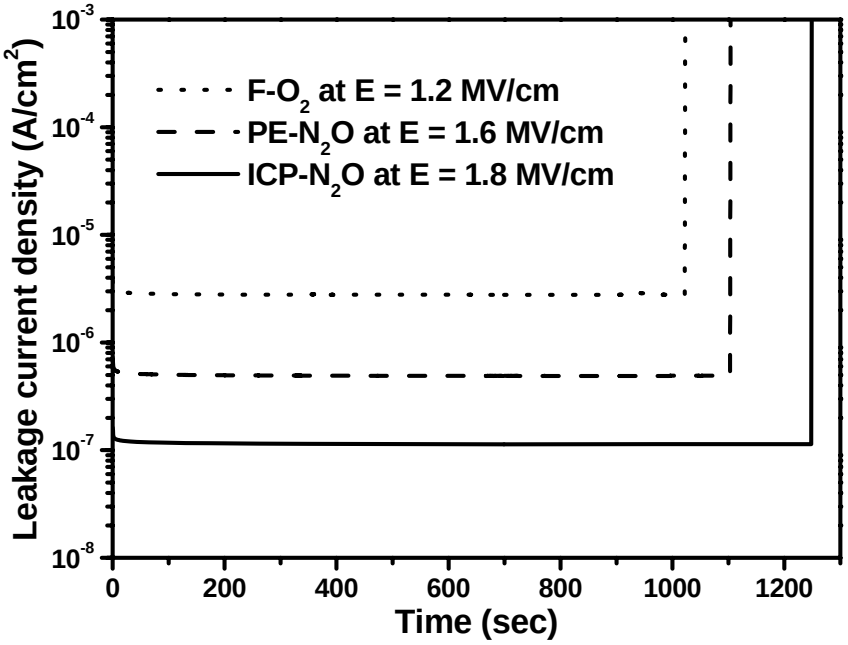


Figure 2.16 Leakage current density vs. time properties for F-O_2 sample under 1.2 MV/cm, PE-N_2O sample under 1.6 MV/cm, and ICP-N_2O sample under 1.8 MV/cm.

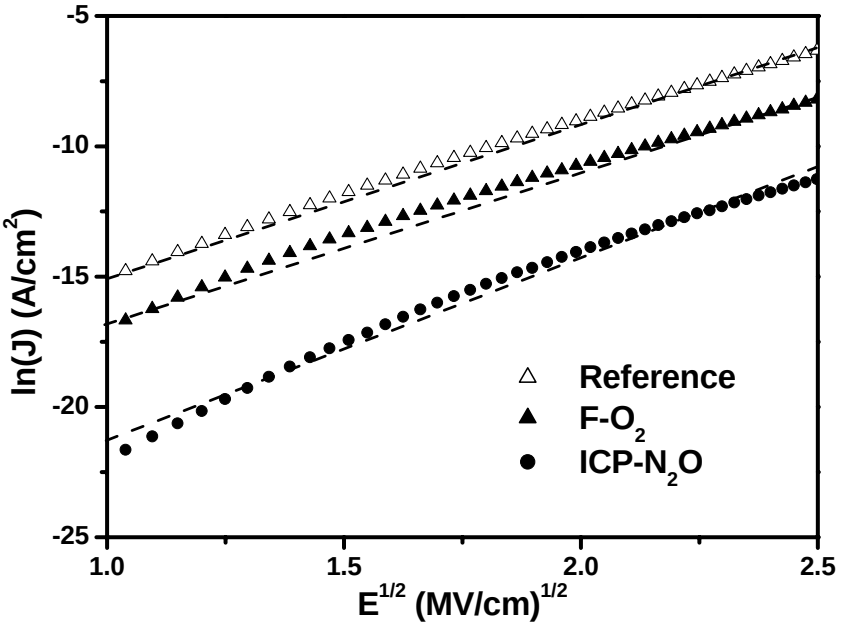
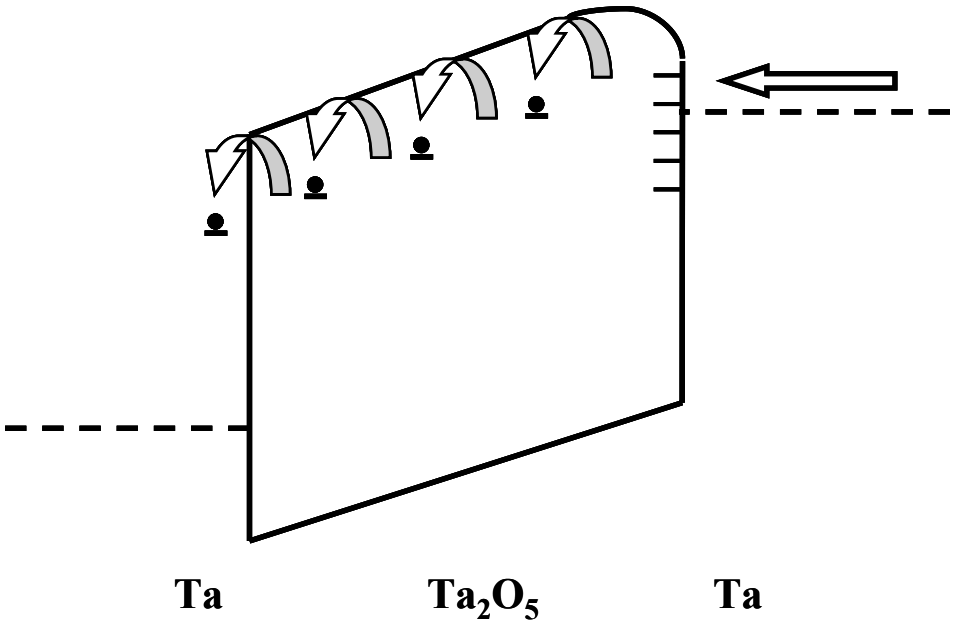
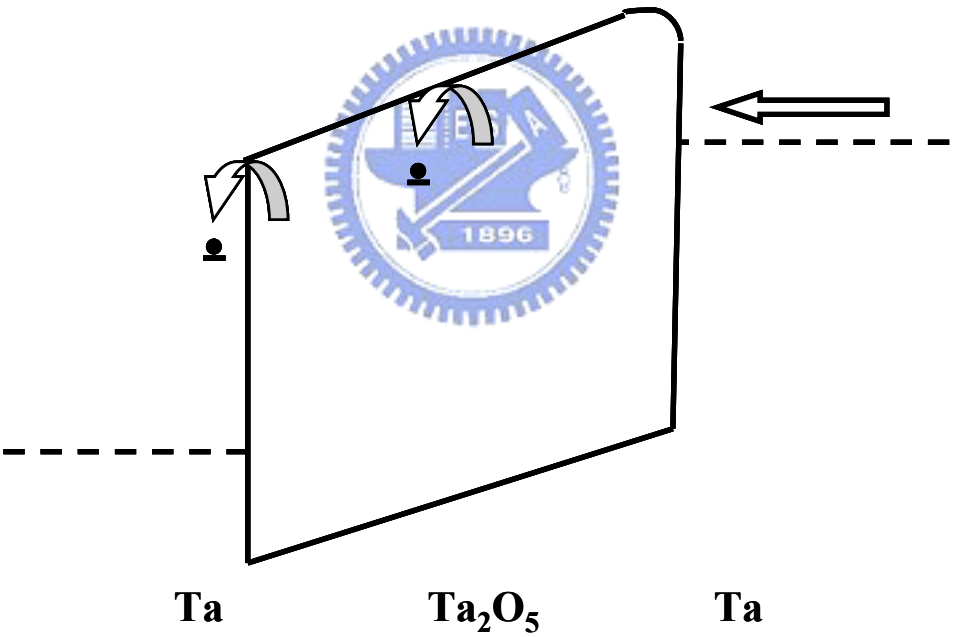


Figure 2.17 The ln(J) versus $E^{1/2}$ plots for various Ta/Ta_2O_5/Ta capacitors.



(a)



(b)

Figure 2.18 Schematic illustrations of conduction mechanisms in $Ta/Ta_2O_5/Ta$ capacitors. (a) F-O_2 and (b) ICP-N_2O samples.

Chapter 3

High Performance and Reliability of High Dielectric Constant $(Ba,Sr)TiO_3$ Thin-Film Capacitor with Cu-based Electrodes

3.1 Introduction

The metal-insulator-metal (MIM) capacitors in silicon radio frequency (RF) and mixed-signal IC applications have recently attracted considerable attention, because they comprise highly conductive electrodes and have low parasitic capacitance [1-3]. Although SiO_2 and Si_3N_4 have highly linear voltage properties and low temperature coefficients, their capacitance density is limited by low dielectric constants. Therefore, high-*k* materials seem to be an alternative material that satisfies the requirements for MIM capacitors in silicon RF and mixed signal IC applications.

Recently, the high-k dielectric material $(Ba_{0.5},Sr_{0.5})TiO_3$ (BST) has been intensively investigated for its possible applications in dynamic random access memory circuits (DRAM) [4-8], since it has a high dielectric constant, a low leakage current density and a high dielectric breakdown strength; also, its composition can be easily controlled because it contains volatile lead oxide [9,10]. The electrical characteristics of BST thin films depend strongly on the deposition conditions [11-13], the post-deposition annealing conditions [14], and the bottom electrode materials [15-18]. Moreover, the electrodes are most important parts of such capacitors. Current semiconductor technology depends on the use of low-resistivity metals as electrode materials for ultra-large-scale integrated (ULSI) conduction lines and contact structures. Several metallization technologies have been developed for use in IC

applications to minimize the cost of ownership in electrode processes [11,19,20]. Platinum (Pt) and ruthenium (Ru) have been adopted as electrodes in capacitors made of high-*k* materials. Pt and Ru, however, have a limited range of applications owing to their high resistivity (Pt: ~10.6 μΩ cm, Ru: ~7.7 μΩ cm), cost and leakage current [21-25]. Copper (Cu) has attracted much interest as a potential interconnection metal in advanced metallization technology, because it exhibits greater electromigration resistance and lower resistivity than conventional Al metal [26-29]. Cu-based metallization technology can be incorporated into devices because of their ease of processing and the reduced production cost of silicon RF capacitors and mixed-signal IC [30]. Furthermore, Cu has a low resistivity (1.67 μΩ cm) and high electrical and stress-migration resistance, compared to Pt and Ru. However, practically no work has been conducted on Cu metallization to be applied to thin-film oxide–based devices, because Cu diffusion in dielectrics is generally known to be severe, and Cu oxidizes strongly when exposed in an oxygen environment [31]. Copper oxidizes at relatively low temperatures at a high rate, greatly degrading the electrical properties that govern its performance as interconnect or electrode material.

3.1.1 Impact of a Cu(Mg) Bottom Electrode

Previous research introduced the self-aligned passivation method, which involves the co-deposition of Cu and Mg to yield an oxidation-resistance layer, such as MgO, upon annealing in ambient oxygen [32,33]. This study systematically designed to improve the thermal stability of bottom electrodes using Cu(Mg) alloy film by investigating the self-aligned MgO layer which forms at elevated temperatures. Furthermore, the BST/Cu(Mg)/TaN/SiO_2/Si multilayered structure was also investigated in metal-insulator-metal (MIM) capacitor devices in terms of its electrical

characteristics such as breakdown voltage, leakage current density, bias temperature stressing (BTS) and time-dependent dielectric breakdown (TDDB) tests.

3.1.2 Impact of Cu-based Electrodes

Effective diffusion barriers are required to prevent the diffusion and intermixing of Cu into silicon. Various diffusion barriers for Cu metallization have been investigated, including TiN, WN, and TaN [28,34,35]. Among these, Ta-based barriers have attracted the most attention owing to their high thermal stability and resistance to forming compounds with copper [35]. In this study, the use of BST as the dielectric in the MIM capacitor with Cu-based electrodes was demonstrated. The maximum temperature of 400ºC can fulfill the requirements of recently developed Cu and low-*k* interconnects technology [36,37]. The fabrication of the devices is described and their characteristics are discussed as well.

3.1.3 BST Etching Issue

$Ba_{0.5}Sr_{0.5}TiO_3$ (BST) thin films have attracted considerable interest as a new dielectric material for use in capacitors in the next generation of ultra large-scale integrated dynamic random access memories (DRAM). The etching process had been intensively developed to realize highly integrated DRAMs that include BST thin films. However, previous studies have established that conventional reactive ion etching may not be effective in etching BST because of some shortcomings, including slow etching rates of less than 25 nm/min [38,39]. *Kim et al.* reported that enhancement of etching rate of BST thin films using inductively coupled Cl_2/Ar plasma with additive CF_4 gas [40].

Helicon-wave plasma (HWP) etching is an attractive dry etching technique because HWP reactors have the benefits including the relatively low electron temperature and the ease of control of ion flux. At low pressures of below 5 mTorr, HWP is expected to yield low damage, while achieving a high etching rate, because the plasma drifts from the generation region to the substrate at relatively low energy [41]. In this investigation, the electric properties of BST thin films capacitors during the HWP etching of BST thin films is studied using Ar/Cl_2 mixing gas. This work characterizes the etching response as a function of HWP power, substrate bias rf power and flow ratios.

The effect of etching on device performance is an important issue [1,40,42,43]. These effects are typically referred to as etching (or plasma)-induced damage, which is unfavorable to device operation. The literature has established that activated oxygen annealing could reduce the higher leakage current of as-etched BST films [7,8,44,45]. However, these post-annealing processes require high temperature (~600ºC). In this study, oxygen surface plasma treatment was performed on the as-etched BST films at a low substrate temperature (<150ºC) to eliminate etching-induced damage.

3.2 Device Fabrication and Characteristics Measurement

3.2.1 MIM using a Cu(Mg) Electrode

A 500 nm-thick SiO_2 film was produced on a (100) Si wafer by thermal oxidation. Stacked layers of Cu(1.5wt% Mg)/TaN were produced to develop materials integration strategies for forming a reliable Cu(Mg) electrode for high-k capacitors. BST thin films were deposited on Cu(Mg) electrodes by radio-frequency (rf) magnetron sputter deposition. BST film growth was conducted using a stoichiometric $(Ba_{0.5}Sr_{0.5})TiO_3$ target in an atmosphere of argon gas at a pressure of 25 mTorr. All of the BST films had the same thickness of approximately 50 nm. The substrate temperature of the sputtered BST films was room temperature (RT). Some of the BST films were annealed after deposition at temperatures from 400 to 500°C in an atmosphere of oxygen for 30 min in a quartz glass tube furnace. Then, the 300 nm-thick Cu(Mg) and Cu layer was formed as a top electrode by sputtering; it then patterned using the shadow mask process, respectively. In this investigation, the Cu/BST/Cu/TaN/SiO_2/Si system is used as the reference sample.

3.2.2 MIM using Cu-based Electrodes

Test capacitors with an MIM structure were fabricated on SiO_2 (550 nm)/Si substrates. Sputtered Ta/TaN layers were used to reduce the parasitic resistance of the electrode and served as barrier layers. Two Cu-based bottom electrode layers were deposited by sputtering Cu (300 nm) and TaN (25 nm)/Cu (300 nm) layers, respectively. The BST thin films were deposited by sputtering a $Ba_{0.5}Sr_{0.5}TiO_3$ target (99.95% purity) in Ar gas to a thickness of 70 nm. The pressure of the Ar during the

deposition was 10 mTorr and the gas flow rate was 20 sccm. The rf power density was 160 W/cm^2; the deposition rate was 0.67 nm/min and the target to substrate distance was 10 cm. The substrate temperature during deposition was 400ºC. Then, the 25nm TaN and 300nm Cu layers were sputtered as top electrodes. **Table 3.1** lists the BST MIM capacitors utilized herein. BST-3 and BST-4 samples were annealed at 400ºC for 30 min in O_2 after BST films were deposited, to reduce the leakage current. Finally, a photolithography step and dry etching were applied to define the MIM capacitors. **Figure 3.1** depicts the structure of the BST MIM capacitor with Cu-based electrodes. The maximum temperature used to fabricate the device was 400ºC, to ensure compatibility with the CMOS back-end of line process.

3.3.3 BST Etching Method

(Ba,Sr)TiO_3 thin films were deposited at room temperature to a thickness of 200 nm on Ta (300 nm)/SiO_2 (500 nm)/Si by radio-frequency (rf) magnetron sputtering using a $Ba_{0.5}Sr_{0.5}TiO_3$ ceramic single target. The deposition was performed at a pressure of 6 mTorr using pure Ar gas. The substrate was maintained at room temperature during the deposition of the BST films; the rf source power was 700W, and the base pressure was 3.8×10^{-7} Torr. Post oxygen surface plasma treatment for 3 min at 100-300ºC reduced the number of oxygen vacancies. The final thickness of the BST thin films was ~300 nm and the leakage current was approximately 3.0×10^{-8} A/cm^2 at 1 MV/cm. The plasma etching of BST films was studied using the HWP system. A one-turn copper coil, which was connected to a 13.56 MHz rf power supply, was wound around the center of the ceramic chamber to generate high-density plasma. A bias voltage induced by an rf power of 13.56 MHz was capacitively coupled to the substrate susceptor, with a capacitor to control the ion energy. The wafer was placed

on the bottom electrode. During the BST, the total gas flow rate was maintained at 50 sccm and the process pressure was 5 mTorr. The BST film was etched at Ar(80%)/Cl_2(20%) and the etched sample was treated in oxygen surface plasma for 3min.

3.3.4 Characteristics Measurement

The thickness of the film and the characteristics of its surface were measured by thermal-field emission scanning electron microscopy (TFSEM, JEOL JSM-6500F). The samples were examined by cross-sectional transmission electron microscopy (TEM, JEM-2010F) at an acceleration voltage of 200 kV. The samples were prepared by mechanical grinding and polishing, followed by ion milling at an acceleration voltage of 3-5 kV in a Gatan Duomill. Auger electron spectroscopy (AES) was undertaken to determine the depth profile of the element in the films. X-ray photoemission spectroscopy (XPS) was used to measure the etched surface of bonding structures and chemical binding energies, to elucidate the etching mechanism further. Surface roughness was analyzed by atomic force microscopy (AFM). Capacitances from 1 kHz to 1 MHz were measured using a Hewlett-Packard (HP4284A) precision *LCR* meter. The temperature coefficient of capacitance (*TCC*) was determined at temperatures from 25 to 100ºC. Current density-electric field (*J–E*) and current density-time (*J–t*) characteristics were obtained using an HP4156B semiconductor parameter analyzer. During the electrical measurements, the top electrode was biased and the bottom electrode was grounded. The breakdown field (E_{bd}) was defined as the average applied field at which the current density through the dielectric exceeded $1x10^{-6}A/cm^2$. The breakdown field of approximately 20 capacitors was measured on each sample. Measurements of the bias-temperature-stressing (BTS)

and time-dependence of dielectric breakdown (*TDDB*) were made at constant current stress in ambient nitrogen (N_2) in an electric field of 2 V at a temperature from 100 to 200°C to obtain about the traps and Cu^+ ions drift in the BST.

3.3 Results and Discussion

3.3.1 Improving the Electrical Properties and Thermal Stability of $(Ba,Sr)TiO_3$ Thin Films on Cu(Mg) Bottom Electrodes

3.3.1-1 Physical Characteristic

The thermal stability of BST on Cu and Cu(Mg) bottom electrodes were studied. **Figure 3.2** presents XRD patterns of BST thin films on (a) Cu/TaN/SiO_2/Si and (b) Cu(Mg)/TaN/SiO_2/Si structures before and after annealing at 400°C for 30 min in an atmosphere of oxygen. The Cu (111) peak intensities from both samples are almost the same before annealing. In the BST/Cu system, the intensity of the CuO (111) was 38.4 degree and Cu_2O (111) was 36.3 degree, when the temperature was increased to 400°C. Several researchers have reported that the surface of Cu is oxidized when exposed to oxygen in the atmosphere at high temperature [46]. However, almost no clear peak of CuO arose from the BST/Cu(Mg) system. In particular, the resistance to oxidation of the Cu(Mg) bottom electrode exceeds that in the Cu bottom electrode at 400°C.

SEM analysis was conducted and the resultant images are displayed in **Figs. 3.3**, to study the surface morphology of the BST films deposited on Cu and Cu(Mg) bottom electrodes. Before annealing, the surface morphology of the BST films deposited on Cu and Cu(Mg) bottom electrodes are almost the same. After the BST/Cu/TaN/SiO_2/Si sample was annealed at 400°C for 30 min in an atmosphere of oxygen, as displayed in **Fig. 3.3(b)**, the surface of the BST film is rough because it exhibits pinholes and hillocks, mostly of CuO, formed by oxidation growth at the BST/Cu electrode interface. **Figure 3.4** depicts the mechanism of oxidation of Cu on

the BST/Cu/TaN/SiO_2/Si structure following annealing at 400°C for 30 min in an atmosphere of oxygen. The oxygen atoms from the environment easily penetrate the BST layer through diffusion paths and begin oxidizing the Cu layer. Cu oxide will grow along the oxygen diffusion path toward the BST surface at a considerable rate. Accordingly, the increase in the volume of the Cu oxide widens the path and allows more oxygen to pass through, accelerating oxidation. Recent reports support this finding [31]: as the oxide keeps growing outward and Cu ions are transported from the metal layer, a hillock of substantial size is formed on the surface. Nevertheless, the surface of the BST/Cu(Mg)/TaN/SiO_2/Si sample, as shown in **Fig. 3.3(d)**, has almost no hillock or pinhole. This investigation demonstrated that the BST layer on the Cu(Mg) bottom electrode is impermeable to diffusing oxygen and, therefore, protects the underlying Cu layer from oxidation.

Auger depth profiling of BST/Cu and BST/Cu(Mg) systems was conducted to examine the diffusion of oxygen atoms. **Figure 3.5** depicts the resultant profiles. In the BST/Cu system, oxygen atoms diffuse into the Cu layer after annealing at 400°C for 30 min in ambient oxygen, as shown in **Fig. 3.5(a)**. However, in the BST/Cu(Mg) system, oxygen that participated in annealing remained at the surface of the Cu layer. The diffusion behavior of oxygen does not differ from that of other molecules or ions, as presented in **Fig. 3.5(b)**, because the diffusivity of oxygen depends strongly on the thermal stability and barrier property of the bottom electrode at a particular annealing temperature. In addition, upon annealing at 500°C, Mg atoms diffuses to the Cu surface, where it is converted into an MgO thin film. The tendency of Mg to segregate near the free surface was stronger than that in the BST film. The low surface energy of Mg and its high reactivity with ambient oxygen favor preferential oxidation of Mg to MgO. The formation of MgO can be caused by the reaction of Mg with adsorbed oxygen following annealing in ambient oxygen and oxygen that is present in the BST

film. The formation of BST interfacial MgO was thus the main cause of the enhancement on the resistance of oxygen diffusion in the BST/Cu(Mg)/TaN/SiO_2/Si multilayer.

Figure 3.6 shows the cross-sectional TEM image of the BST/Cu and BST/Cu(Mg) systems after annealing at 400 and 500°C for 30 min in an atmosphere of oxygen. The results reveal that the BST film participate in the effective resistance of oxygen when a self-aligned 3.75nm-thick MgO layer is introduced using Cu(Mg) film, whereas the BST/Cu interface loses its stability at 500°C. The formation of interfacial MgO was thus the main cause of the improvement in the diffusion barrier properties of the bottom electrode in the BST/Cu(Mg) interface. When the MgO barrier is formed, the capacitance value will be reduced. However, the effective dielectric constant is about 76 instead of the value of 80 for pure BST in this study. The difference in effective dielectric constant can be ignored since the thickness of an MgO film is thinner than total thickness of the BST film.

3.3.1-2 Electrical Characteristic

The electrical characteristics of combined Cu/BST/Cu and Cu(Mg)/BST/Cu(Mg) multiplayer structures were thus studied, as shown in **Fig. 3.7**. During the electrical measurements, the top electrode was biased while the bottom electrode was grounded. The breakdown field was defined as the electrical field when the current density through the dielectric exceeds 10^{-6} A/cm^2. All leakage current densities of as-deposited BST on both electrodes were approximately 2×10^{-8} A/cm^2 at 1 MV/cm, but the breakdown field of 2.3 MV/cm in the Cu(Mg)/BST/Cu(Mg) structure exceeded that of 1.6 MV/cm in the Cu/BST/Cu structure. The electrical characteristics of both multilayer systems after annealing at 400°C for 30 min in oxygen were also

evaluated. The results demonstrate a large leakage current density of 3×10^{-5} A/cm^2 at 0.5 MV/cm and a low breakdown field of 0.35 MV/cm for the 400°C-annealed BST/Cu system. However, the leakage current density of the MIM structure with Cu(Mg) electrodes after annealing at 400°C, was reduced to 3×10^{-8} A/cm^2 at 1 MV/cm with a breakdown field of over 2.4 MV/cm. Moreover, the samples were annealed at 500°C, and the results indicated that the Cu/BST/Cu structure has a very high leakage current density but the combined Cu(Mg)/BST/Cu(Mg) structure has a breakdown field of over 2.2 MV/cm and a leakage current density of 3×10^{-8} A/cm^2 at 1 MV/cm. The rough surface morphology of the bottom electrode of a capacitor with an MIM structure has been reported to be responsible for a high leakage current density [46,47]. The high leakage current density of the BST thin film on the Cu electrode was attributable to the rough surface morphology due to Cu oxide formation, as presented in **Figs. 3.3(b)** and **3.6(a),(b)**. The leakage current density of the BST film on the Cu(Mg) electrode was the lowest, because the surface morphology of the bottom electrode was smooth and the BST/Cu(Mg) layer was stable, as presented in **Figs. 3.3(d)** and **3.6(c),(b)**. The combined Cu(Mg) system structure thus supports the excellent properties of the electrodes of a capacitor with the MIM structure, promoting resistance to oxygen diffusion.

3.3.1-3 Device Thermal Stability

The drift of Cu^+ ions into BST thin film was also studied using BTS tests. **Figure 3.8** plots the dependence of the leakage current density in the BST/Cu (Cu/TaN/BST/Cu/TaN/SiO_2/Si) and BST/Cu(Mg) (Cu/TaN/BST/Cu(Mg)/TaN/SiO_2/Si) systems on temperature. During the BTS tests, the bottom electrode was biased while the upper electrode was grounded. In both samples, the leakage current densities

increase with temperatures, suggesting thermally assisted conduction. The BST/Cu sample had a consistently higher leakage current density than the BST/Cu(Mg) sample at the same temperature. The higher leakage current density of a BST/Cu system is probably associated with the ionization and injection of Cu^+ ions at the interface of Cu electrode under positive gate bias, and the subsequent injection of these Cu^+ ions into the BST films as the temperature rises. The leakage current difference between various temperatures in the BST/Cu(Mg) system is less than that in the BST/Cu system, indicating that the former has a higher Cu^+ ions drift resistance than the BST/Cu sample. *Murarka et al.* reported that Cu(Mg)-gated could cause an inhibition of the diffusion or drifting of copper into the SiO_2 [48]. **Figure 3.9** plots the stress-induced changes in the *J-E* characteristics of the BST sample with the Cu(Mg) electrode. The *J-E* curves of the fresh device were first measured. A bias (2V) was applied to the accumulation region of the device for 30 and 60 sec, and the *J-E* characteristics were again measured. This procedure was repeated after 30s. Stressing at a bottom electrode caused a lateral shift in the *J-E* curve. Subsequent stressing for 30s did not result in further significant lowering of the current, revealing that first 30s of stressing at 2V sufficed to fill most of the traps, further stressing did not cause any further significant generation of traps.

Several references reported that a positive electric field ionizes Cu atoms and then injects the resulting Cu^+ ions into the dielectrics, generating leakage currents [49-53]. Additional insights into Cu^+ ions drift into BST films were gained by performing TDDB tests with a constant voltage of 2 V applied to the bottom electrodes of the samples, which were at room temperature (RT) and heated to 200°C, respectively. At the beginning of the stress test, the leakage current declined. The decrease in the current in the first stage is believed to be caused by electron trapping in the dielectric films [54,55]. Breakdown, which is accompanied by a sudden increase in current, can

happen after a certain period, when the accumulated charge density at the interface reaches a critical value. **Figures 3.10(a)** and **(b)** show the TDDB test results for BST/Cu (Cu/TaN/BST/Cu/TaN) and BST/Cu(Mg) (Cu/TaN/BST/Cu(Mg)/TaN) systems, respectively, with 2 V bias applied with bottom electrode at different temperatures. The BST/Cu system broke down rapidly and time to fail significantly as the temperature increased to 200°C, which effect is believed to be caused by the much faster accumulation of Cu^+ ions at 200°C because of the higher Cu^+ ions drift rate. However, the BST/Cu(Mg) system did not break down after it was stressed for 500 s at 2V at 200°C, as plotted in **Fig. 3.10(b)**. These results demonstrate that the BST/Cu(Mg) system successfully inhibits the drift of Cu^+ ions into the BST thin film.

3.3.2 Impact of Cu-based Electrodes on the Reliability of Metal Insulator Metal (Ba,Sr)TiO_3 Thin-film Capacitors

3.3.2-1 Physical Characteristic

Figures 3.11 display SEM micrographs of the surface morphology of BST films deposited on Cu (BST-3) and TaN/Cu bottom electrodes (BST-4). As presented in **Fig. 3.11(a)**, the surface of the BST film in BST-3 sample is rough because it exhibits pinholes and hillocks, mostly of CuO, formed by oxidation growth at the BST/Cu electrode interface. The oxygen atoms from the environment easily penetrate the BST layer via diffusion paths and begin oxidizing the Cu layer. Recent reports support this finding:[31,56] as the oxide continues to grow outward and the Cu ions are transported from the metal layer, a hillock of considerable size is formed on the surface. Nevertheless, the surface of the BST-4 sample, as shown in **Fig. 3.11(b)**, has almost no hillocks or pinholes. This study established that the BST layer on the TaN/Cu bottom electrode is impermeable to diffusing oxygen and so protects the underlying Cu layer against oxidation. The SEM observation is consistent with the cross-sectional TEM micrograph of the BST-4 sample, as shown in **Fig. 3.12**. The interface between the TaN and Cu layers is smoother and no reaction is observed between them.

3.3.2-2 Electrical Characteristic

Figure 3.13 plots the leakage current density as a function of electrical field up to 4.0 MV/cm. Before annealing, the leakage current density of BST-2 sample is observed to be much better than that of the BST-1 sample without a thin TaN film as a

diffusion barrier. The leakage current density of the BST-2 sample is $4.0\text{x}10^{-8}$ A/cm^2 at 1 MV/cm lower than that for the BST-1 sample ($8.0\text{x}10^{-5}$ A/cm^2). After annealing at 400°C for 30 min in O_2, the leakage current density of BST-3, not shown here, is caused by serious device failure due to Cu oxidation. However, the leakage current density of the BST-4 sample is $2.0\text{x}10^{-8}$ A/cm^2 at 1 MV/cm, significantly lower than that before annealing at 400°C. Also, the breakdown field (E_{bd}) of the BST-4 sample is around 3.2 MV/cm (at 10^{-6} A/cm^2), higher than those of the BST-1 and BST-2 samples, which are approximately 0.4 and 1.8 MV/cm. Numerous references have reported that post-annealing treatment in an oxygen-containing atmosphere yielded oxygen atoms and reduced the number of oxygen vacancies, ultimately enhancing the quality of BST films [11,19,20].

The mechanisms that govern the conduction of leakage current in the MIM capacitor may include Schottky emission, the Poole-Frenkel effect, electronic hopping conduction and tunneling [57-59]. Schottky emission is modeled as,

$$J = AT^2 \exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta_s}{kT}E^{1/2}\right) \tag{3.1}$$

where A is a constant; T represents the absolute temperature; q is the electronic charge; ϕ_0 is the barrier height; k is the Boltzmann constant, and β_s is given by

$$\beta_s = \left(\frac{q^3}{4\pi\varepsilon_0\varepsilon}\right)^{1/2} \tag{3.2}$$

where ε_0 is the permittivity of free space and ε is the high-frequency dielectric constant. **Figure 3.14** plots ln(J) as a function of $E^{1/2}$ in the Cu/TaN/BST/TaN/Cu structure (BST-4). The figure demonstrates that different conduction mechanisms dominate in different electric field regimes. Two linear regions are observed, and the gradient yields the corresponding effective dielectric constant in the electric field E<1.0 MV/cm. The figure reveals that the dominant conduction mechanism in the

BST-4 capacitor is Schottky emission in a low electric field, in which electrons from the cathode overcome the TaN/BST energy barrier before they are emitted. The leakage current density increases with the electric field, because when an electron enters the BST, it creates an image field that adds to or is subtracted from the barrier field, reducing the barrier height and increasing the current.

When electric field E>1.25 MV/cm, electrical conduction is governed by Poole-Frenkel emission, which is described by,

$$J = CE\exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta_{PF}}{kT}E^{1/2}\right) \tag{3.3}$$

where C is a constant and β_{PF} is defined by

$$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2} \tag{3.4}$$

Figure 3.15 plots ln(J/E) versus $E^{1/2}$ in the BST-4 capacitor. The gradient in the linear region yields the corresponding effective dielectric constants in electric field E>1.25 MV/cm, which value is close to that obtained from C-V measurement. Hence, Poole-Frenkel emission is determined to dominate in a high electric field. Poole-Frenkel emission is caused by the field-enhanced excitation of trapped electrons into the conduction band of the dielectric and its existence in capacitors establishes the presence of electron traps [60]. In electric fields of over 1.25 MV/cm, electrons in BST film traps absorb sufficient energy to be excited to the conduction band and Poole-Frenkel emission then dominates conduction.

The time to breakdown (t_{BD}) of BST capacitors is measured by applying a voltage from 10.5 to 12.25 V, which corresponds to an electric field of 1.5 to 1.75 MV/cm in the BST-4 sample. **Figure 3.16(a)** plots the J –t curves of TDDB measurement. These data demonstrate the t_{BD} is a function of the total number of carriers that pass though the films [61]. At the beginning of the stress test, the leakage current declined. The

decrease in the current in the first stage is believed to be caused by electron trapping in the dielectric films. After the majority of the electron traps were filled, the leakage current densities fell in the middle stage. However, the leakage current rapidly increased and fatal breakdown occurred after stress was applied for a longer period. **Figure 3.16(b)** plots log(t_{BD}) as a function of applied field for the BST-4 capacitor. The sample has a longer lifetime than 10 year at 1.1 MV/cm. This result indicates the long-term intrinsic reliability of the BST capacitor in Gbit-scale DRAM applications.

3.3.2-3 Frequency Effect

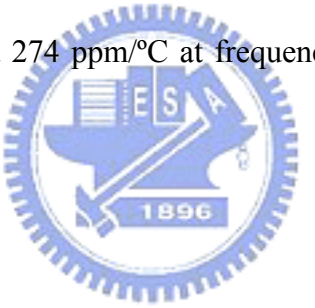
Figure 3.17 plots the capacitance density and dissipation factor of the BST-2 and BTS-4 capacitors versus frequency. The results indicate that the capacitance density is maintained about 11.5 fF/μm^2 at frequency from 1 kHz to 1 MHz and a high dielectric constant of 91 is obtained, which is higher than that of the Al_2O_3 and HfO_2 MIM capacitors [62-64]. The large capacitance density at a low frequency of 1 kHz, in combination with the decline in capacitance density at a high frequency of 1 MHz, reveals that the mechanism may be defect-related because the slow traps may not have sufficient speed to follow the high-frequency signals [65]. Furthermore, a low dissipation factor under 0.03 is observed.

The linearity of capacitance against voltage is a significant parameter that depends on the material properties of the BTS film. The dependence of capacitance on voltage can compared with the voltage coefficients of capacitance (VCCs), which are given by

$$\frac{dC}{C_0} = \frac{C(V) - C_0}{C_0} = \alpha V^2 + \beta V \qquad (3.5)$$

where C_0 is the zero-biased capacitance at each frequency, and α and β are the

quadratic and linear voltage coefficients, respectively. The capacitances are measured at 1 kHz, 10 kHz, 100 kHz and 1 MHz. **Figures 3.18(a)** and **(b)** plot the obtained α and β values. For BST-4 capacitor, α falls from 357 ppm/V^2 to 101 ppm/V^2 for and β declines from 3637 ppm/V to 1347 ppm/V. Both α and β decrease as frequency increases, and relationship can be explained by the low time constant of traps within the BST layer. A comparison between the results for the BST MIM capacitor and those reported recently for the Ta_2O_5 capacitor shows overall superior VCCs that suggest that the MIM capacitor is very useful in Si RF applications [66,67]. **Figure 3.19** plots the normalized capacitance of the BST-4 capacitor versus temperature at frequencies from 1 kHz to 1 MHz. The results demonstrate that the capacitance increases with the temperature. The temperature coefficients of capacitance (TCC) are 633 ppm/ºC, 433 ppm/ºC, and 274 ppm/ºC at frequencies of 1 kHz, 100 kHz and 1 MHz, respectively.



3.3.3 Repairing of Etching-induced Damage of High-*k* $Ba_{0.5}Sr_{0.5}TiO_3$ Thin Films by Oxygen Surface Plasma Treatment

Figure 3.20(a) plots the effect of HWP power on the etch rates of BST under an Ar/Cl_2 gas mixture with 20% Cl_2. As the HWP power increases from 1500 to 2500 W, the etch rates of BST films increase from 45 to 70 nm/min. The selectivity of BST toward Ta seems to be constant at about 0.95, and the selectivity of BST toward PR seems to be constant at about 0.92. This effect may by explained by the fact that the increase of HWP power promotes the formation of reactive free radicals (Cl) and ions (Ar^+) by increasing the efficiency of both physical and chemical etching mechanisms by increasing the volume densities and fluxes of ions and chlorine atoms. *Kim et al.* reported a similar data [40]. **Figure 3.20(b)** plots the etching rates of BST, Ta and photoresist (PR) as functions of substrate bias rf power. The ion bombardment energy increases with the substrate bias rf power, increasing the selectivity of BST toward PR. However, the selectivity of BST toward Ta is almost constant, because the ion bombardment effect is similar to those associated with BST and Ta etching.

The reactive free radicals and ions in the plasma may change the electrical characteristics of the BST films, which will degrade the device performance. The etching-induced damage in the Ta/BST/Ta capacitors was analyzed in terms of the change in the leakage current density. **Figure 3.21(a)** plots the current-voltage curves of the etched BST samples with various HWP power levels. The leakage current of the as-deposited BST thin film was 3.0×10^{-8} A/cm^2 at 1 MV/cm and the breakdown field was ~ 2 MV/cm at 1.0×10^{-6} A/cm^2. The leakage current densities in the etched BST samples significantly increase with HWP power. Therefore, the capacitor is damaged during BST etching. The oxygen vacancies or space charge at the BST/Ta interface are considered to increase as the plasma ions accumulate on the surface of

the BST films. *Wuu et al.* reported a similar ions effect [44]. **Figure 3.21(b)** presents the effects of substrate bias rf power on the leakage current density of as-etched capacitors. The leakage current density was observed increased at an rf power of 150 W. The effect of the substrate bias rf power on the BST film may be explained by the increase in ion bombardment energy and the increase in sputtering yields of both main materials and reaction products. As the substrate bias rf power rises, the positive ions are accelerate to the substrate and then penetrated into the BST films, increasing the polarization loss and yield, and reducing the dielectric constant [68].

Figure 3.22 shows the etch rate of BST thin films as a function of % Cl_2 flow ratios in the Ar/Cl_2 system. During etching, the pressure of the chamber, the HWP power and the substrate bias rf power were fixed at 5 mTorr, 1500 W and 90 W, respectively. The etch rate of the BST films is maximal when the proportion of Cl_2 in the gas mixture was 20%. The etch rate of the sample at 20% of Cl_2 was approximately 48 nm/min, which twice as fast as that of the film etched in pure Cl_2 and pure Ar ambient. *Kim et al.* obtained similar results [69]. Two parallel etching mechanisms operate chemical and physical conditions. They are monotonic but exhibit opposite tendencies as the Ar mixing ratio is increased in the Ar/Cl_2 mixture. The point of the etching rate varied from 0% to 20% Cl_2 (100% to 80% Ar). Chemically enhanced physical sputtering occurs when Cl-atoms etching produce vulnerable surface moieties that are easily sputtered by ion impact. The dominant ion-assisted etching mechanism is ion bombardment and ion-stimulated desorption of low-volatily reaction products. The ion-assisted etching mechanisms are those predicted by *Humbird* [70].

Nevertheless, the etch rate declines as the flow ratio of Cl_2 gas increases above 20%. This results is expected because the chemical etching products Ba-Cl and Ti-Cl are very low-volatility compounds with the same melting points as $BaCl_x$ and $TiCl_x$ [71]. This result is consistent with the observations of *Stafford* who reported that the

desorption of these compounds caused by ion impact is less efficient than that caused by the direct impact of ions on BST, resulting in the accumulation of reaction products on the etched surface, which obstruct access by chlorine atoms and reduce the etch rate [38]. Additionally, *Efremov et al.* reported that increasing the Ar mixing ratio increases the electron temperature and reduces the electron density [72]. The surface of BST thin films was studied using XPS to confirm this assumption.

The elements of BST (Ba, Sr and Ti) were investigated using XPS narrow scan spectroscopy. The samples used were bare BST films that did not undergo any photoresist treatment. **Figure 3.23(a)** displays the Ba 3*d* spectra resolved in Ba-O and Ba-Cl. As revealed in **Fig. 3.23(a)**, the as-deposited film has two peaks, corresponding to Ba ($3d_{5/2}$) and Ba ($5d_{3/2}$), at 779 and 794.5 eV binding energies, which were identified as being associated with Ba-O bonds [40,73]. Spectra (2)-(5) in **Fig. 3.23(a)** exhibit a small shift to high binding energy, in comparison with the as-deposited film. This chemical shift demonstrates a chemical reaction between Ba and Cl. The relative atomic proportion of the Ba of BST films etched with high Ar content (spectra (2), (3)) is less than that of etched BST films at high Cl_2 content (spectra (4), (5)). Hence, the Ba-O bond is broken by Ar ion bombardment. Furthermore, spectra (4) and (5) indicate that the intensities of the BaO and $BaCl_x$ peaks are higher than the those of spectra (2)-(3), because Ar ion bombardment, rather than by the chemical reaction, effectively removes Ba compounds such as $BaCl_x$. Ba-Cl compounds remain on the surface as a residue because the boiling point is high (1560ºC). **Figure 3.23(b)** shows the Sr 3*d* narrow scan spectra which may be resolved in two peaks, corresponding to Sr $3d_{5/2}$-O (135.2 eV) and Sr $5d_{3/2}$-O (137 eV) [40,74,75]. A chemical reaction between Sr and Cl is not easily observed because of the lack of a chemical shift; the appearance of the new peaks in **Fig. 3.23(b)**. The intensities of the Sr 3*d* peaks decline as the Ar content increases. The removal of Sr

by the Cl radical is assumed to be difficult, but Ar bombardment can remove all of the Sr. The intensity of the Sr-O peaks in spectrum (6) seems not to be change clearly following oxygen surface plasma treatment. **Figure 3.23(c)** displays the Ti 2*p* spectra. The spectrum (1) of the as-deposited film has two peaks, corresponding to Ti $2p_{3/2}$ and Ti $2p_{1/2}$ at binding energies of 458 and 464 eV, respectively [40,73,75]. Etching in Ar/Cl_2 plasma shifted the Ti-O peaks towards high binding energy. Peaks correspond to Ti $2p_{1/2}$-Cl and Ti $2p_{3/2}$-Cl in spectrum. The intensities of the TiO_x and $TiCl_x$ peaks drop as the amount of Cl_2 increases, because chemically reactive etching is effective in removing Ti from BST films because the $TiCl_x$ has a low boiling point (136.5°C). Oxygen surface plasma treatment shifts spectrum (6) to the Ti-O binding energy, unlike that associated with as-etched films. This shift verifies that the oxygen atoms were absorbed during plasma treatment.

Figure 3.24 presents that the leakage current density of etched BST in various Ar/Cl_2 gases and shows the etched samples following oxygen surface plasma treatment at room temperature. The as-etched BST films exhibit a higher leakage current level than the as-deposited films, and lower onset voltages associated with the abrupt increase in leakage current. Accordingly, the capacitor suffers damage during BST etching. This result is considered to be the combined effect of surface charge accumulation and ionic penetration. Therefore, additional modification, including the annealing treatment of etched BST films, was required [44,45]. However, a post-annealing treatment temperature of 600ºC is too high for the Cu backend process. The leakage current can be reduced by oxygen plasma treatment at room temperature. Following oxygen surface plasma treatment, the leakage current of the etched BST films slightly improved. In such cases, the extent of recovery is around or exceeds 50%. Chemical damage, such as that with non-volatile products can be undone by setting the plasma-electron temperature, but the physical damage such as that caused

by ion bombardment can not be completely undone.

Figure 3.25 shows scanning electron microscopy (SEM) photographs of the BST surface. The as-deposited BST surface was very smooth, as presented in **Fig. 3.25(a)**. In contrast, **Fig. 3.25(b)** indicates that post-etched residues were present on the surface of the as-etched BST film. The XPS findings of the etched BST surface, plotted in **Fig. 3.23** imply that these residues comprise Ti and Ba compounds. **Figure 3.25(c)** mirrors the fact almost no Cl-based residue was present on the surface of the BST after oxygen surface plasma treatment. **Figure 3.26** depicts the typical atomic force microscopic (AFM) scans of as-deposited and as-etched BST thin film surfaces before and after oxygen surface plasma treatment. The root-mean-square (rms) roughness of the as-deposited BST thin film is about 1.21 nm. During pure Ar plasma etching, the surface became slightly rougher, as indicated by the change in rms roughness, perhaps because the rates of removal of the lattice constituents of Ba, Sr, Ti and O atoms are unequal because the sputter yields vary. Moreover, the rms roughness of BST thin film in pure Ar plasma is lower than that in Ar(80%)/Cl_2(20%) plasma. The increased roughness of the as-etched BST thin films with the Ar/Cl_2 gas mixing ratio may be caused by the redeposition of nonvolatile etch products. Oxygen surface plasma treatment reduced the rms roughness of the BST etched at a mixing ratio Ar/Cl_2 declined from 7.85 to 2.15 nm. However, pure Ar plasma caused almost no improvement, suggesting that the physical damage to the BST film in Ar/Cl_2 plasma is lower than that in pure Ar plasma. Oxygen surface plasma treatment can repair chlorine-induced damage. Oxygen surface plasma treatment cannot reverse the physical damage caused by energetic ions.

3.4 Summary

In conclusion, the bottom electrodes strongly influenced the electrical characteristics of BST thin films. The surface morphology of an electrode and the variation of this morphology with temperature caused significant interfacial problems in BST thin films. The presence of Mg in Cu dramatically reduces the oxidation rate of the metal. Thin self-aligned MgO layers were formed by annealing in ambient oxygen. The resulting barriers had high thermal stability of up to 400 or 500°C in a Cu(Mg)/BST/Cu(Mg)/TaN/SiO_2/Si multilayer system. The Cu(Mg) layer as an electrode material in the MIM structure had a higher breakdown field, 2.4 MV/cm, and lower leakage current density, 3×10^{-8} A/cm^2, than the Cu electrodes. Furthermore, when Cu(Mg) electrodes were used, Cu^+ ions drift was lower, and the BST capacitor more reliable.

The BST MIM capacitor with Cu-based electrodes has a high capacitance density of 11.5 fF/μm^2 and a low dissipation factor below 0.03, which can be adapted to satisfy the requirements of the ITRS roadmap. It has a low leakage current density of $2.0\text{x}10^{-8}$ A/cm^2 and a high breakdown field of 3.2 MV/cm, small linear VCCs of 101 ppm/V^2, 1347 ppm/V and TCC of 274 ppm/ºC, and a TDDB of over 10 years at 1.1 MV/cm. The leakage current of the Cu-based BST capacitor at a low electric field of 1.0 MV/cm was governed by Schottky emission, and at a high electric field of the BST capacitor, the leakage current mechanism was Pool-Frenkel emission. All these findings demonstrate that the BST MIM capacitor with Cu-based electrodes is very reliable in Gbit-scale DRAM applications, and is effective in silicon RF technology.

The results of this investigation indicated the etching characteristics of BST thin films fabricated by HWP system. During the etching of BST thin films in Ar/Cl_2 plasma, ion bombardment and chemical contamination cause physical damage by the

formation of nonvolatile etching products, including serious chlorine-based residues, which severely degrade the leakage characteristics of the BST films. Applying oxygen surface plasma treatment to as-etched BST films can effectively reduce the chlorine-based residues at low substrate temperatures with short process duration. Excellent electrical properties, including a low leakage current density of ~ 3.0×10^{-8} A/cm^2 at 1 MV/cm and a high breakdown field of ~ 2 MV/cm at 1.0×10^{-6} A/cm^2 can be achieved. The recovery behavior of the as-etched BST film can be explained by the fact that metal-chlorine compounds can be removed from the surface and increase the number of metal-oxide bonds.

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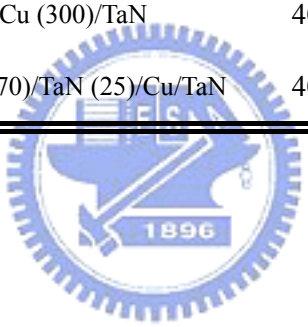
Table 3.1. Structures and thickness (nm) of BST MIM capacitors used in this study.

MIM type	Structures and thickness (nm)	Annealed after BST deposition
BST-1	Cu (300)/BST (70)/Cu (300)/TaN (50)	None
BST-2	Cu/TaN (25)/BST (70)/TaN (25)/Cu/TaN	None
BST-3	Cu (300)/BST (70)/Cu (300)/TaN	400^0C, 30 min, O_2 atmosphere
BST-4	Cu/TaN (25)/BST (70)/TaN (25)/Cu/TaN	400^0C, 30 min, O_2 atmosphere



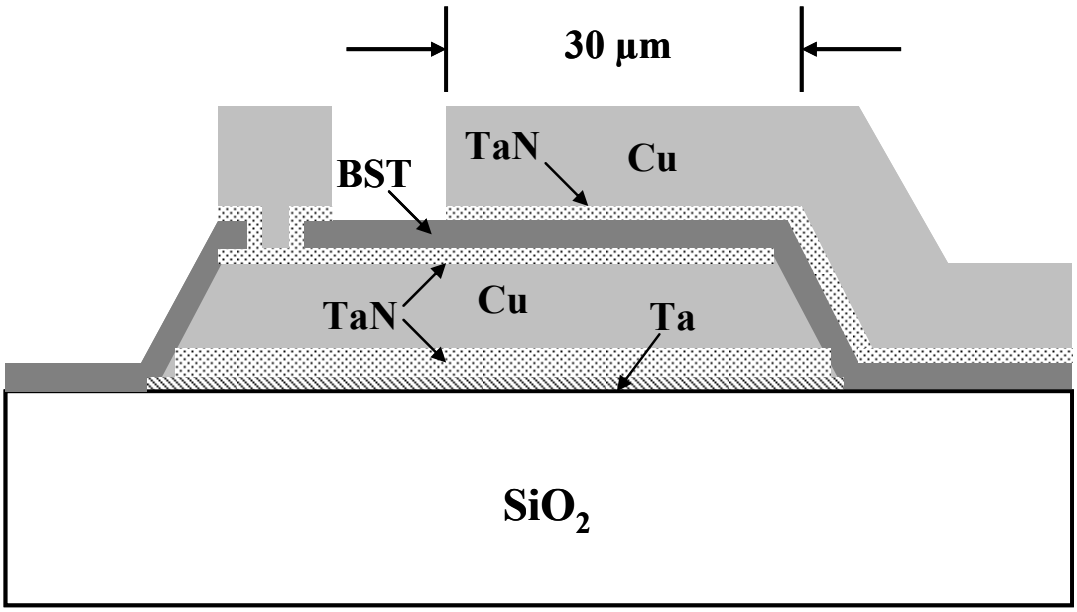


Figure 3.1 Schematic diagram of BST MIM capacitor with Cu/TaN electrodes.

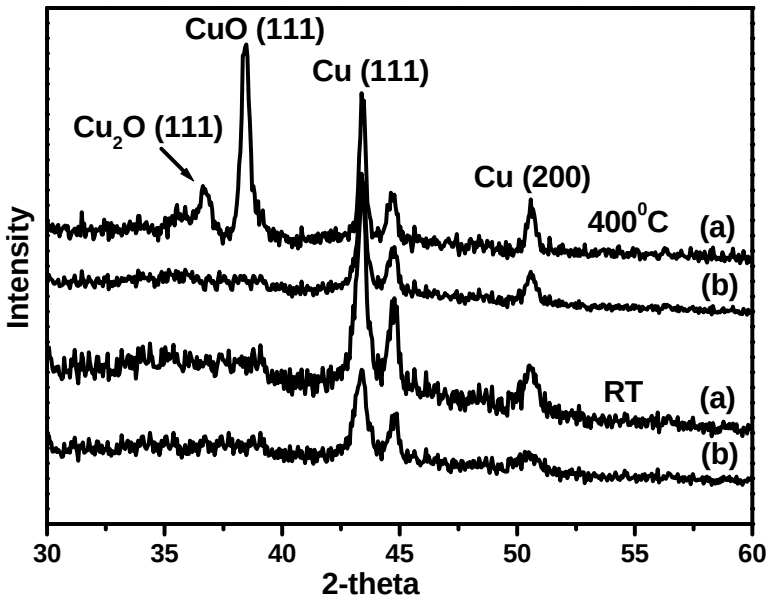


Figure 3.2 XRD patterns of BST thin film deposited on (a) Cu, and (b) Cu(Mg) bottom electrodes before and after annealing at 400°C for 30 min in an oxygen atmosphere in a furnace.

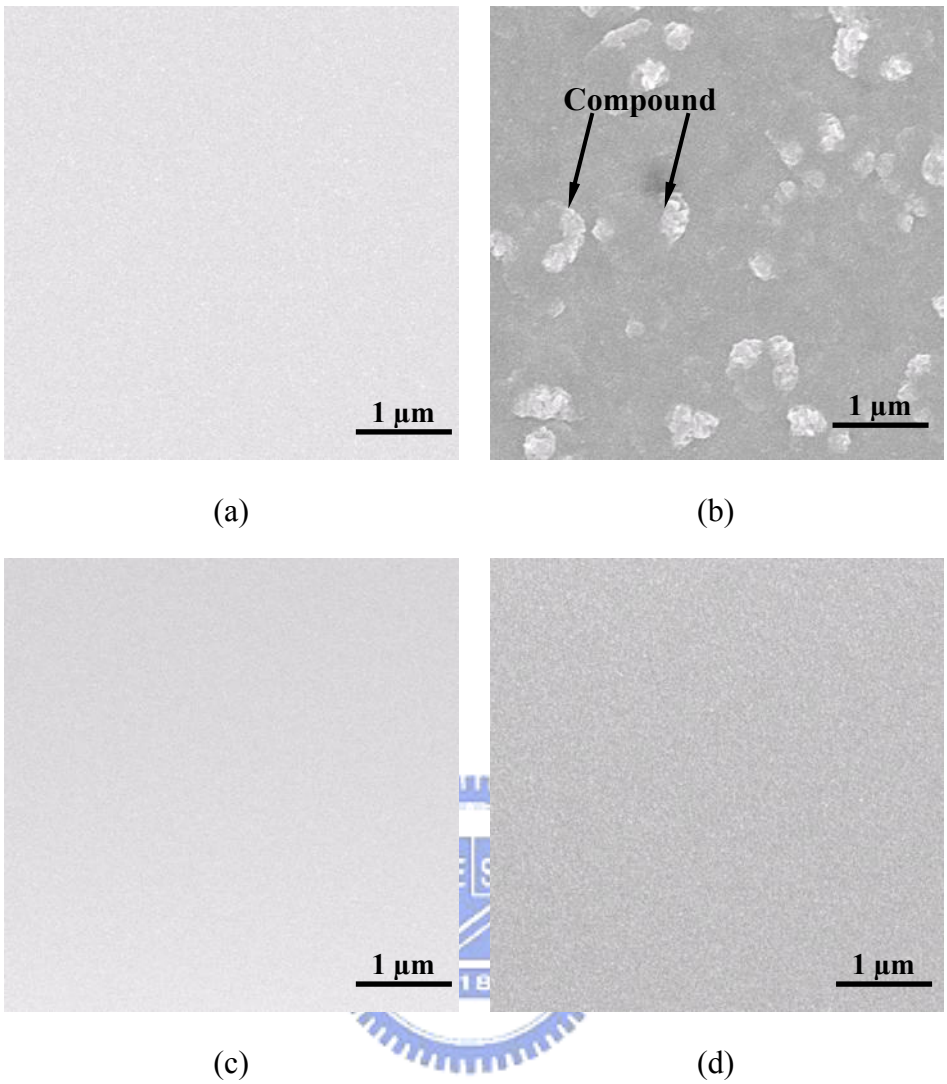


Figure 3.3 SEMs of BST thin film deposited on the Cu bottom electrode (a) before and (b) after annealing at 400°C for 30 min in oxygen atmosphere, and deposited on the Cu(Mg) electrode (c) before and (d) after annealing at 400°C for 30 min in oxygen atmosphere.

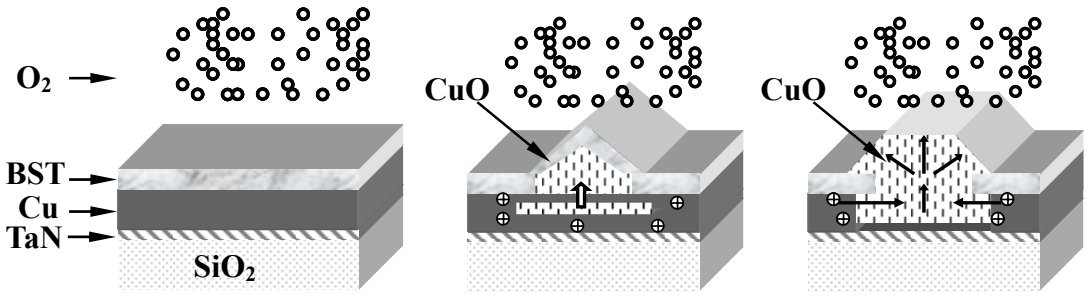
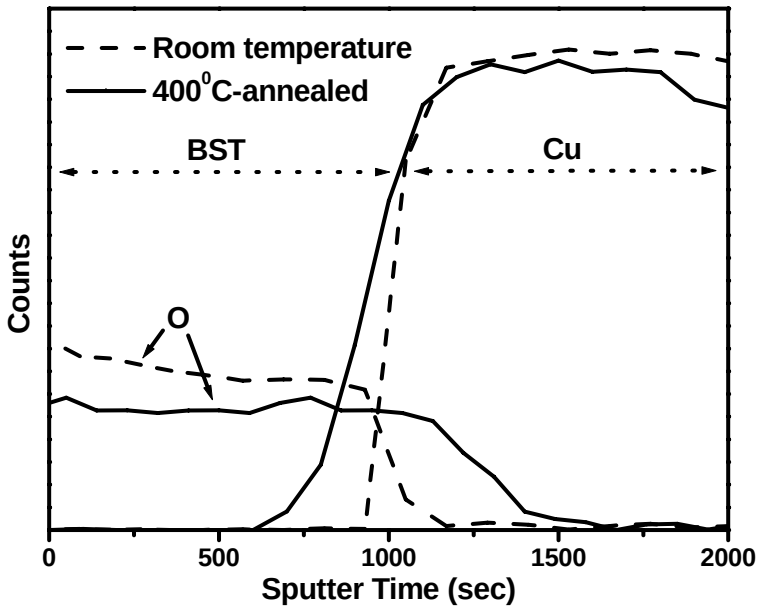
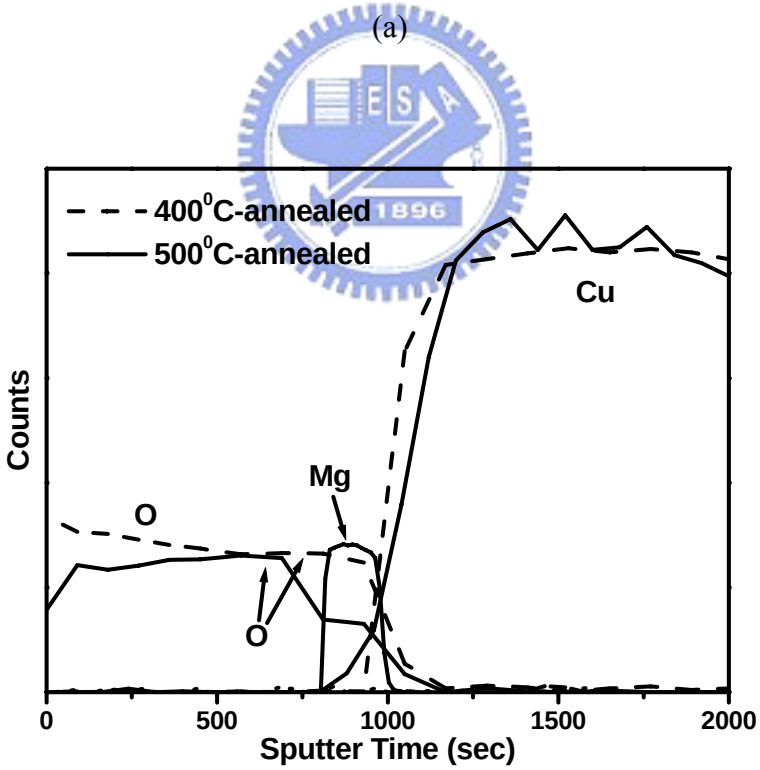


Figure 3.4 Schematic drawing presents Cu oxidation mechanism where the oxidation barrier fails.



(a)



(b)

Figure 3.5 Auger depth profiles of (a) BST/Cu and (b) BST/Cu(Mg) systems before and after furnace annealing at 400°C for 30 min in oxygen ambient.

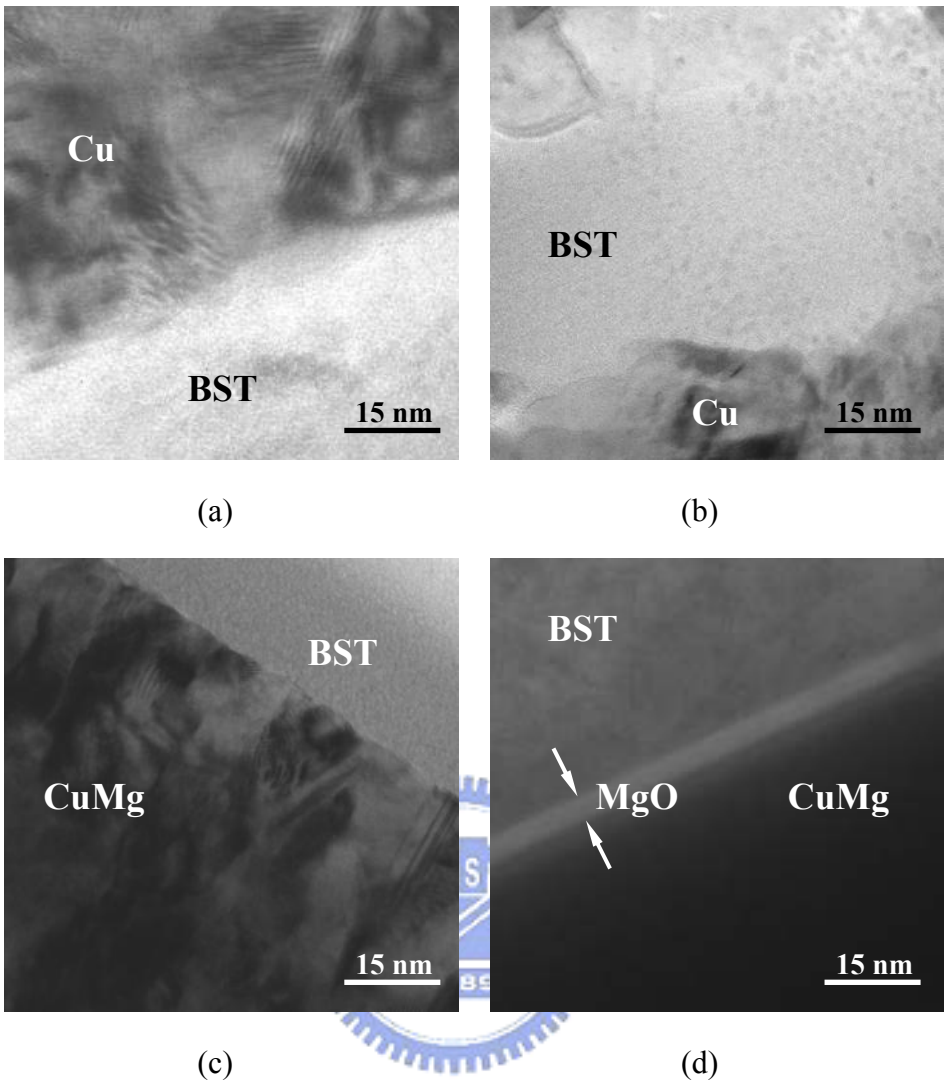


Figure 3.6 Cross-sectional TEM images of interface of the BST/Cu system after furnace annealing at (a) 400 and (b) 500°C for 30 min in oxygen ambient, and which of the BST/Cu(Mg) system after furnace annealing at (c) 400 and (d) 500°C for 30 min in oxygen ambient.

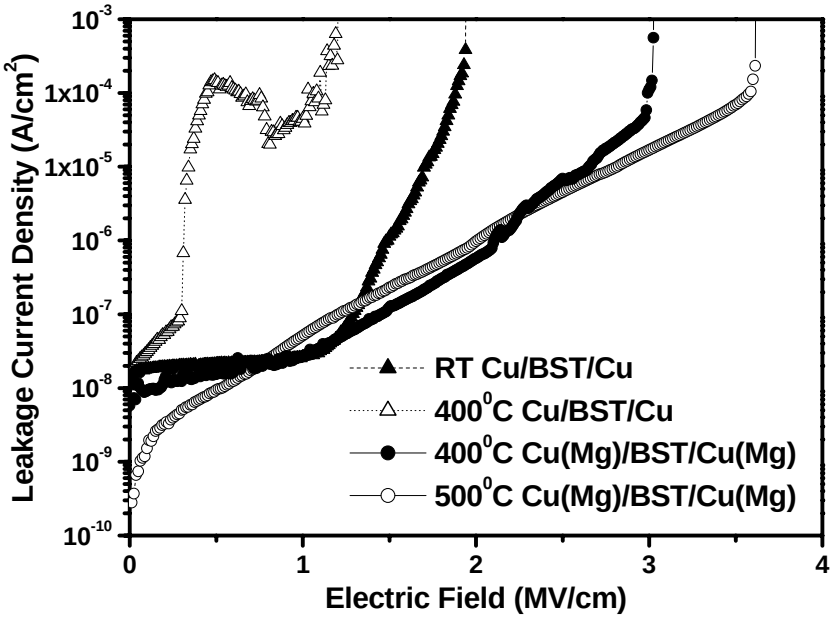
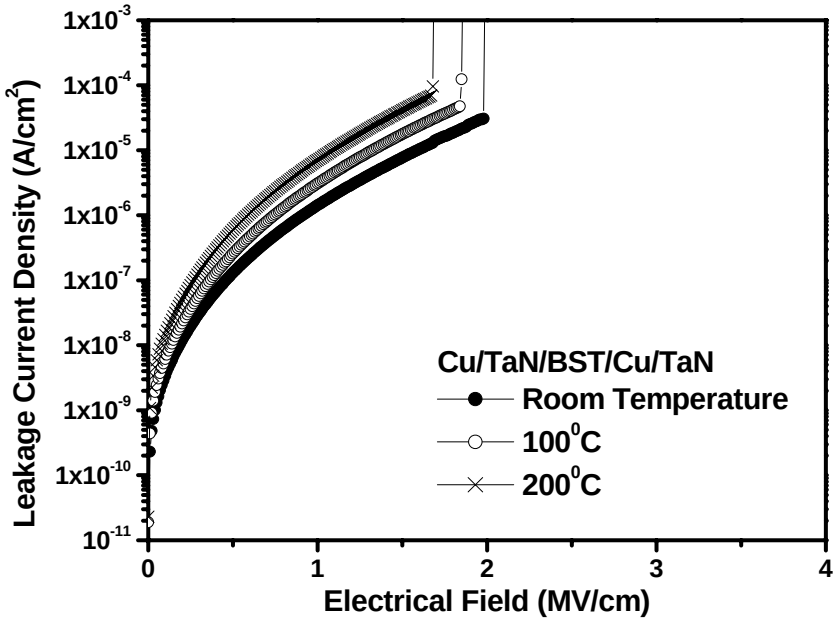
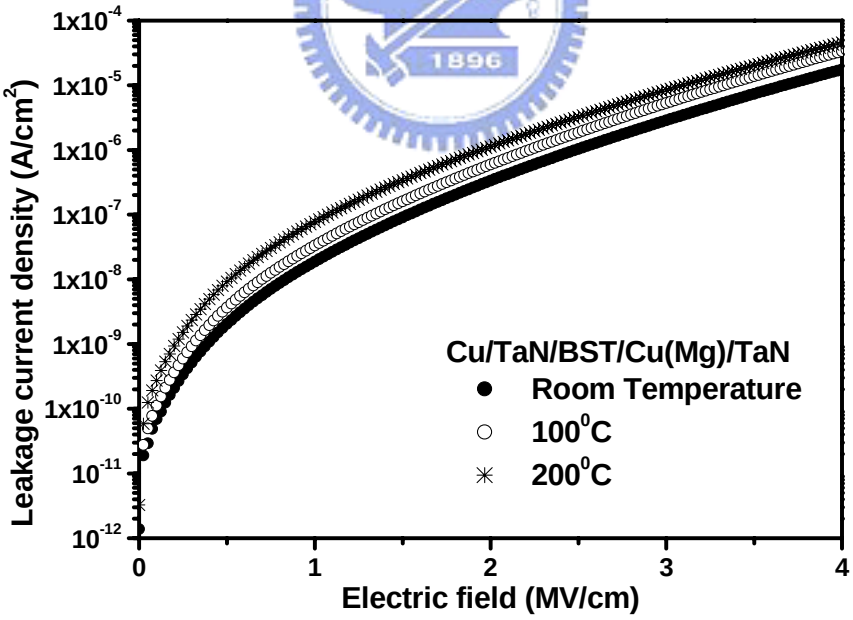


Figure 3.7 *J-E* characteristics of the BST with Cu and Cu(Mg) electrodes before and after furnace annealing at 400 and 500°C for 30 min in oxygen ambient.



(a)



(b)

Figure 3.8 *J-E* relations of the (a) BST/Cu and (b) BST/Cu(Mg) interface in the temperature range 100 to 200°C and an electrical field of up to 4 MV/cm.

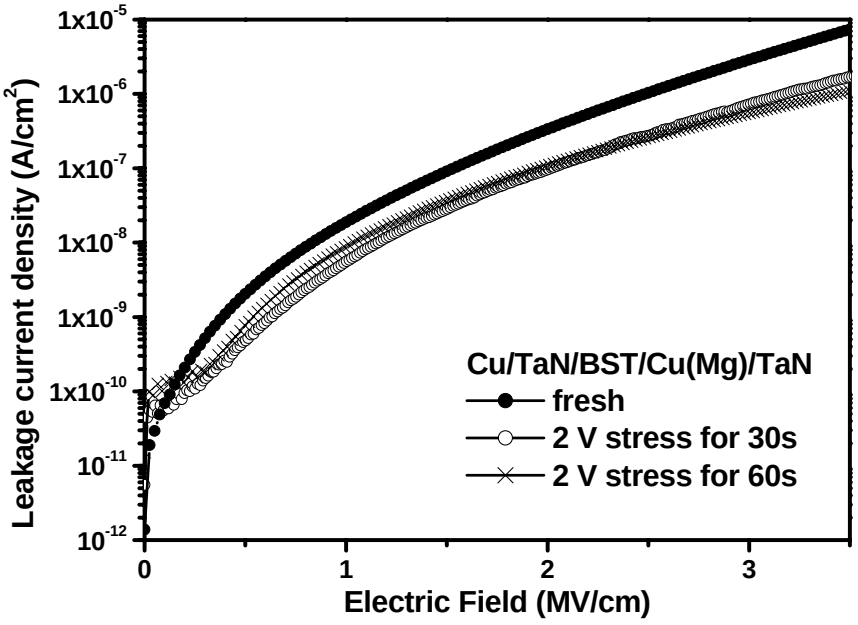
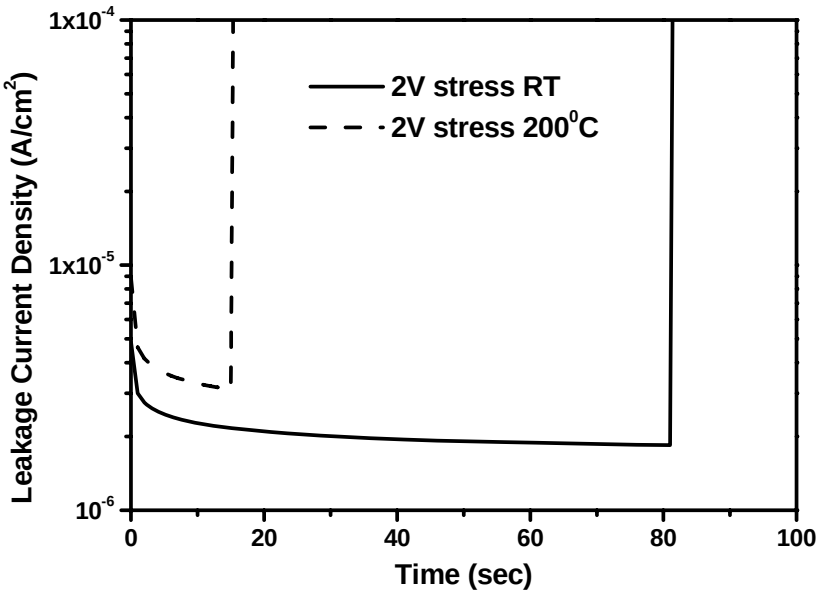
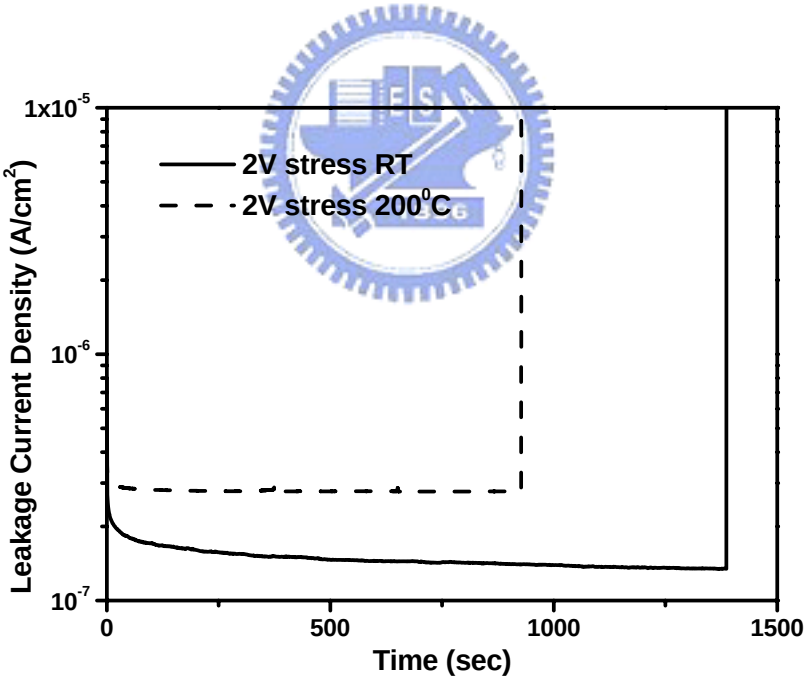


Figure 3.9 *J-E* relations of BST/Cu(Mg) system before and after a constant 2V stress has been applied for 30 and 60 sec.

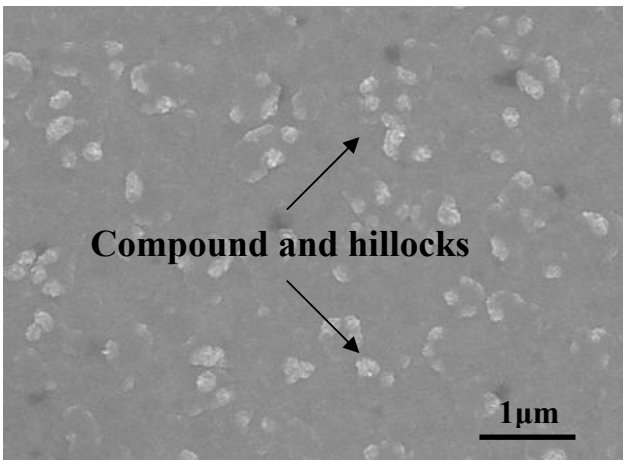


(a)

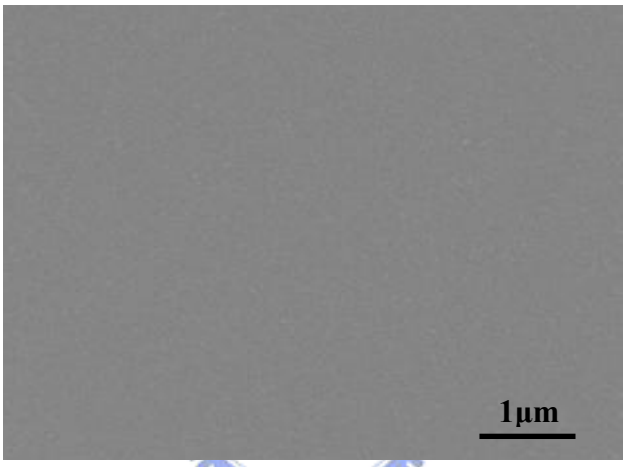


(b)

Figure 3.10 Time-dependent dielectric breakdown (TDDB) characteristics of BST capacitors with (a) Cu and (b) Cu(Mg) electrodes with an applied bias of 2V at room temperature (RT) and at 200°C.



(a)



(b)

Figure 3.11 SEM micrographs of BST film when deposited directly on the (a) Cu and (b) TaN/Cu bottom electrodes after annealing at 400^0C for 30 min in O_2.

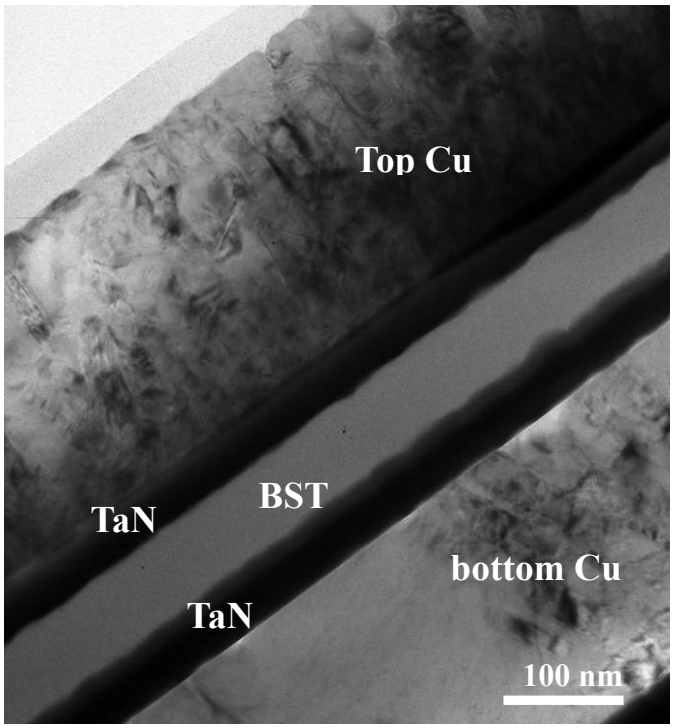


Figure 3.12 Cross-sectional TEM image of BST MIM capacitors with Cu/TaN electrodes.

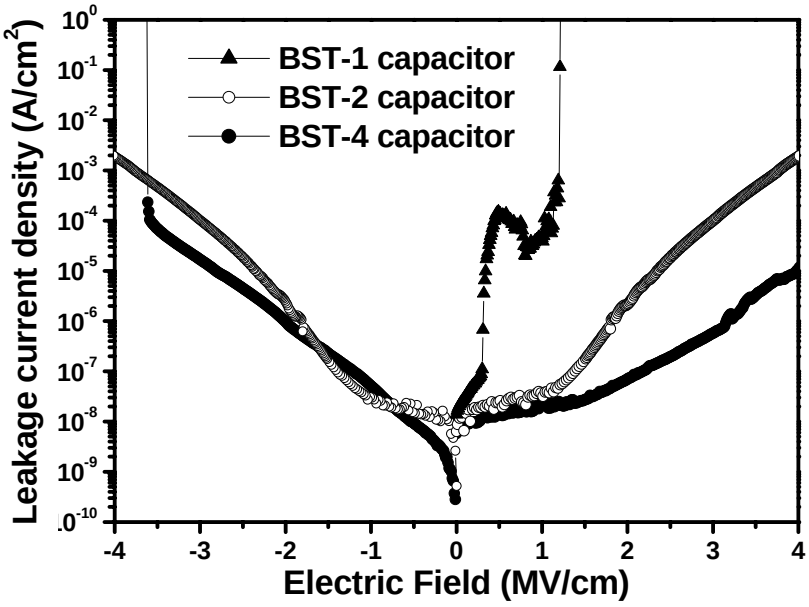


Figure 3.13 Leakage current density-electric field (*J-E*) characteristics of BST MIM capacitors with Cu-based electrodes at various annealing temperatures.

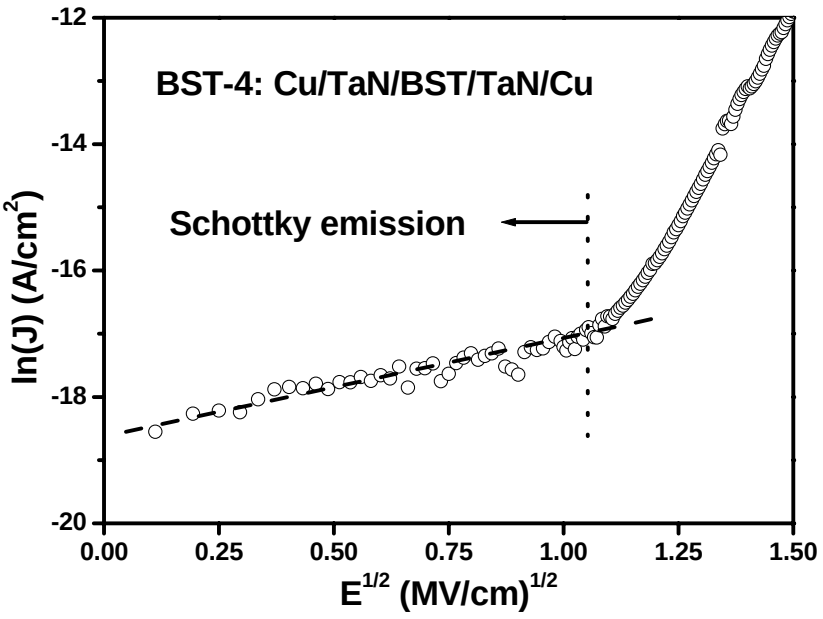


Figure 3.14 ln(J) versus $E^{1/2}$ for conduction mechanism of BST-4 capacitor, representing Schottky emission at low electric field.

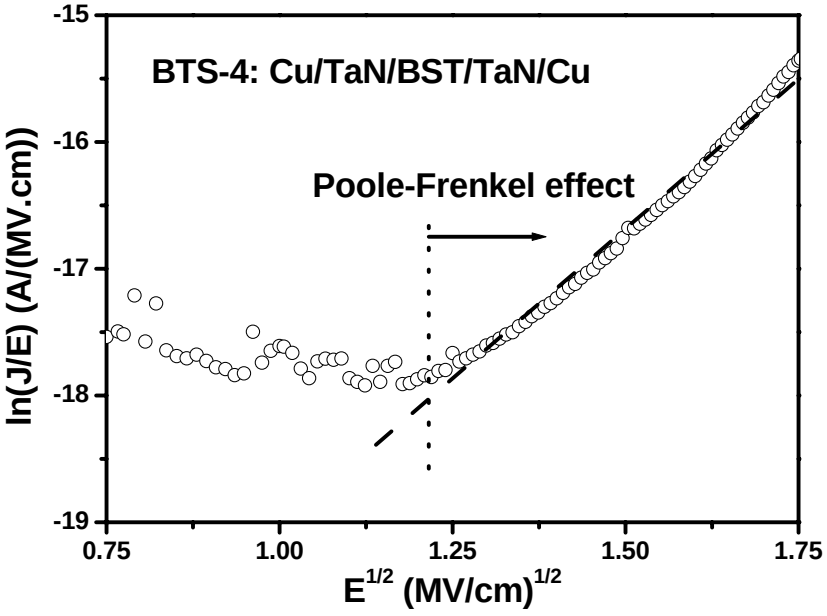
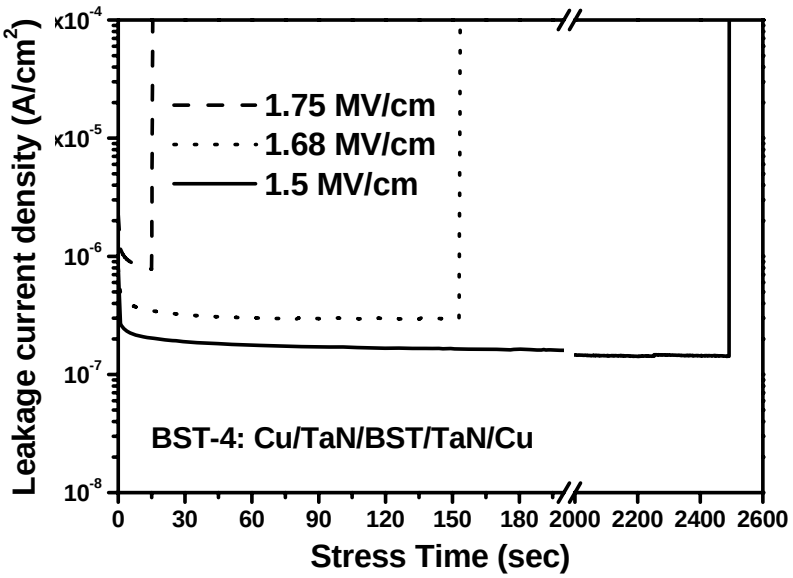
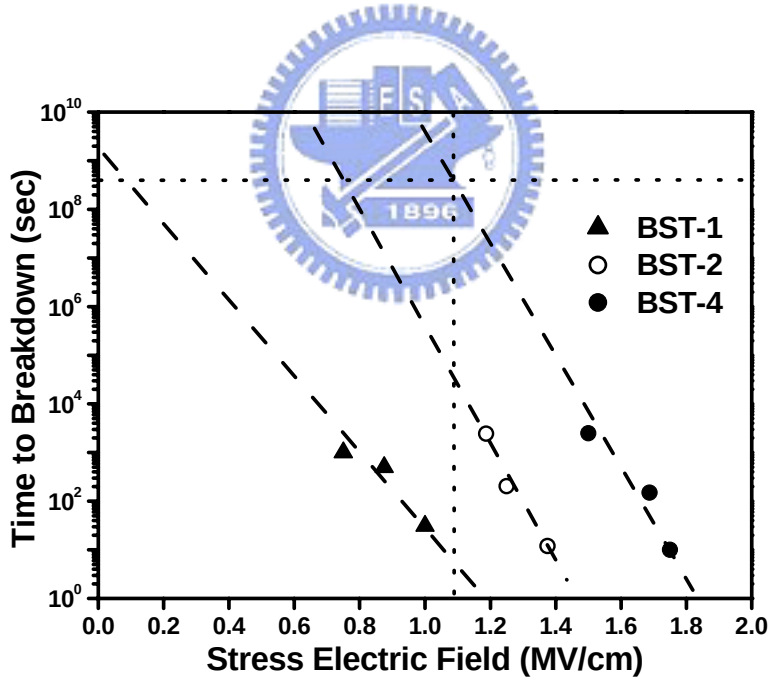


Figure 3.15 ln(*J*/*E*) versus $E^{1/2}$ for conduction mechanism of BST-4 capacitor, representing Poole-Frenkel effect at high electric field.



(a)



(b)

Figure 3.16 (a) Characteristics of leakage current density against period of stress in constant electric field from 1.5 to 1.75 MV/cm for the BST-4 capacitor. (b) Projected life-time of BST capacitors with Cu-based electrodes.

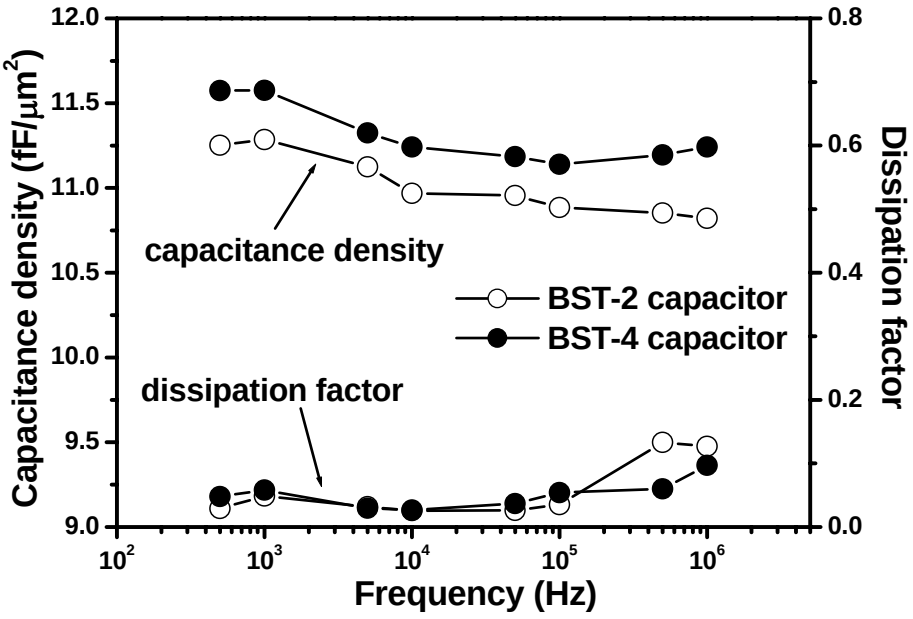
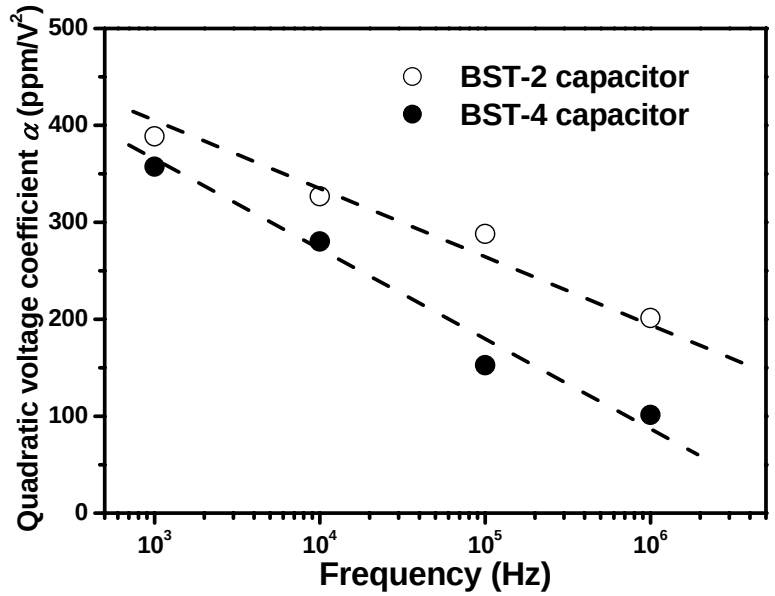
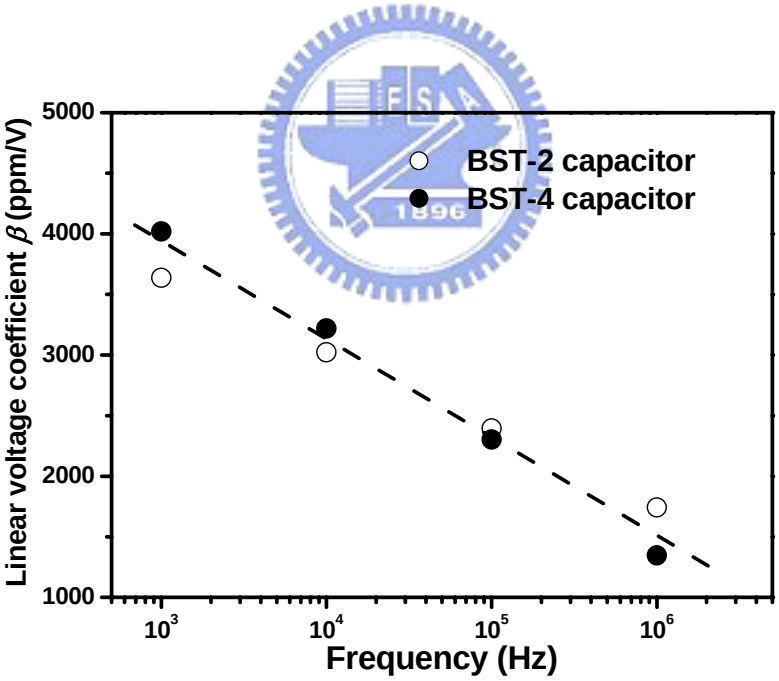


Figure 3.17 Capacitance densities and dissipation factors of BST-4 capacitor with Cu/TaN electrodes as functions of frequency.



(a)



(b)

Figure 3.18 (a) Quadratic voltage coefficients α and (b) linear voltage coefficients β of capacitances of BST-4 capacitor with Cu/TaN electrodes as functions of frequency.

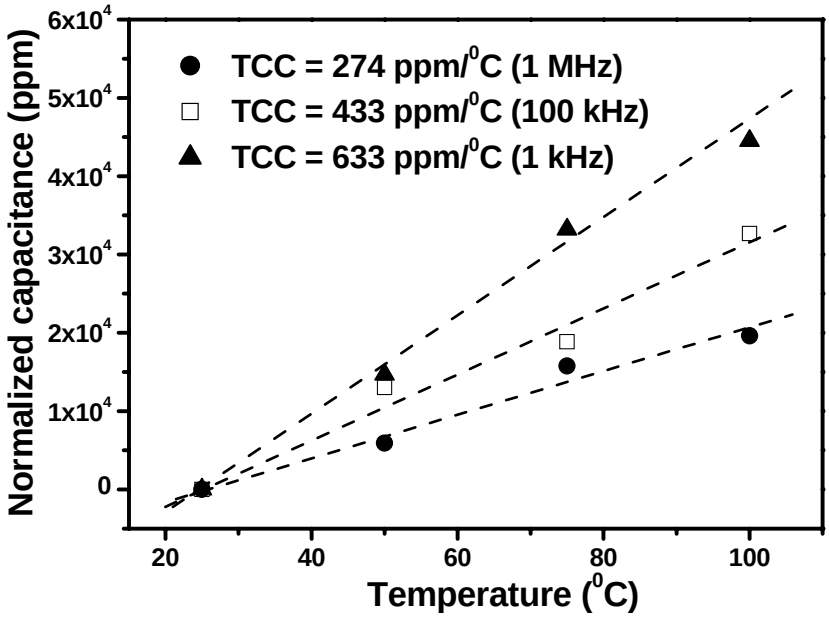
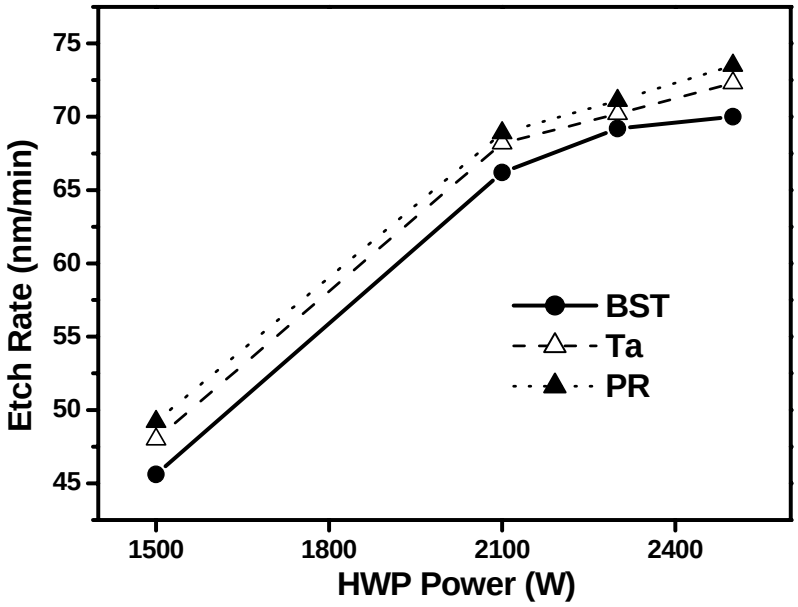
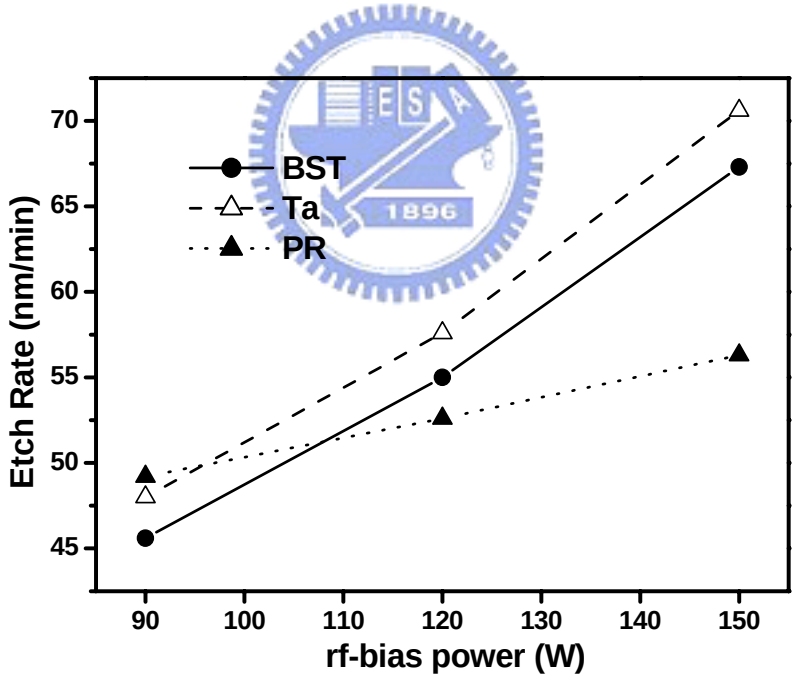


Figure 3.19 Normalized capacitances of BST-4 capacitor with Cu/TaN electrodes as a function of temperatures.

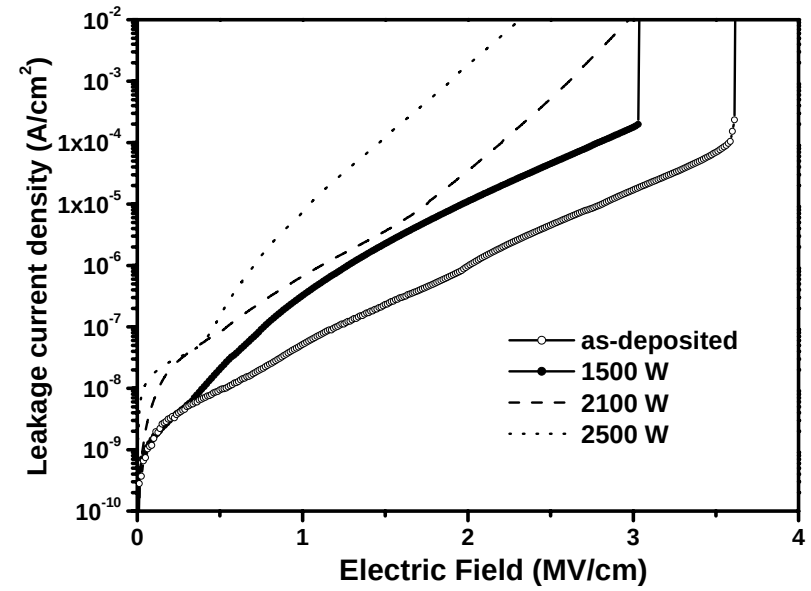


(a)

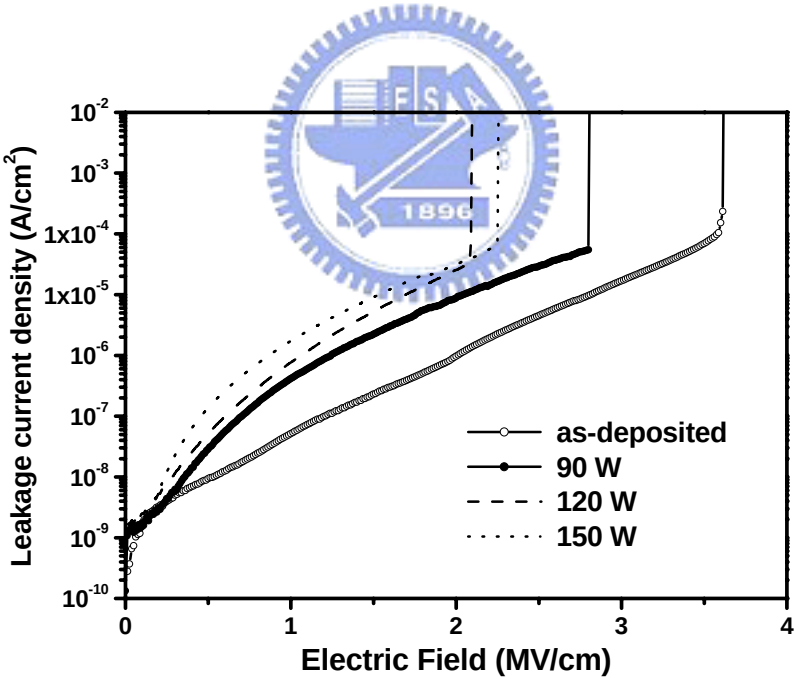


(b)

Figure 3.20 Etch rate of BST thin film as a function of (a) HWP power, and (b) substrate bias rf power.



(a)



(b)

Figure 3.21 Leakage current characteristics of the etched BST thin films with various (a) HWP power, and (b) substrate bias rf power.

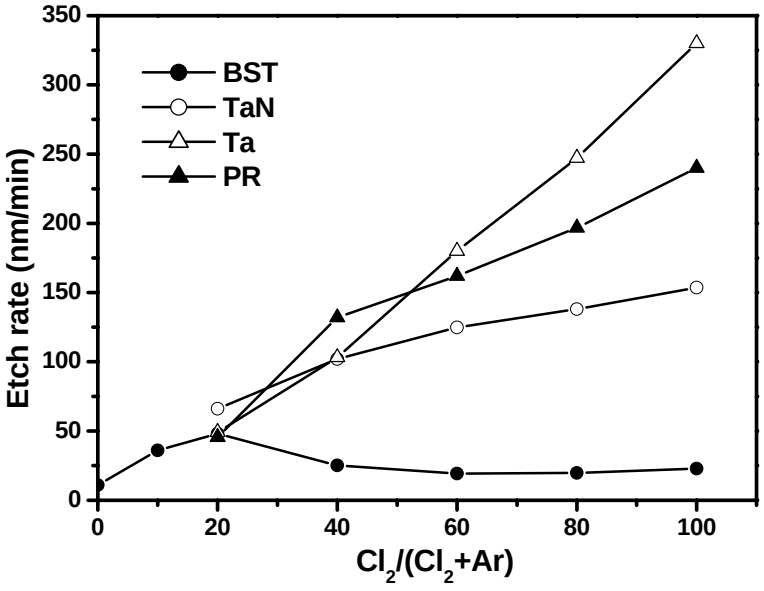
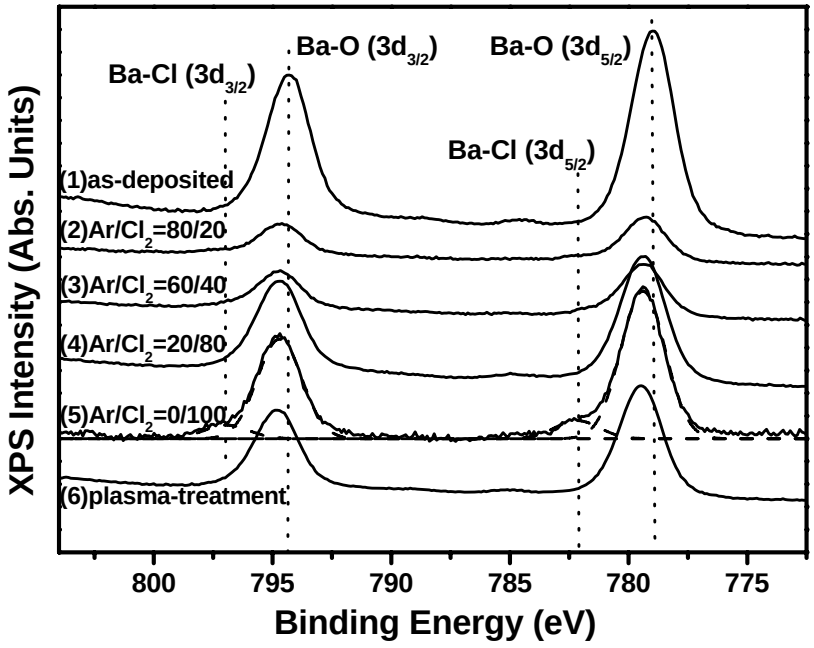
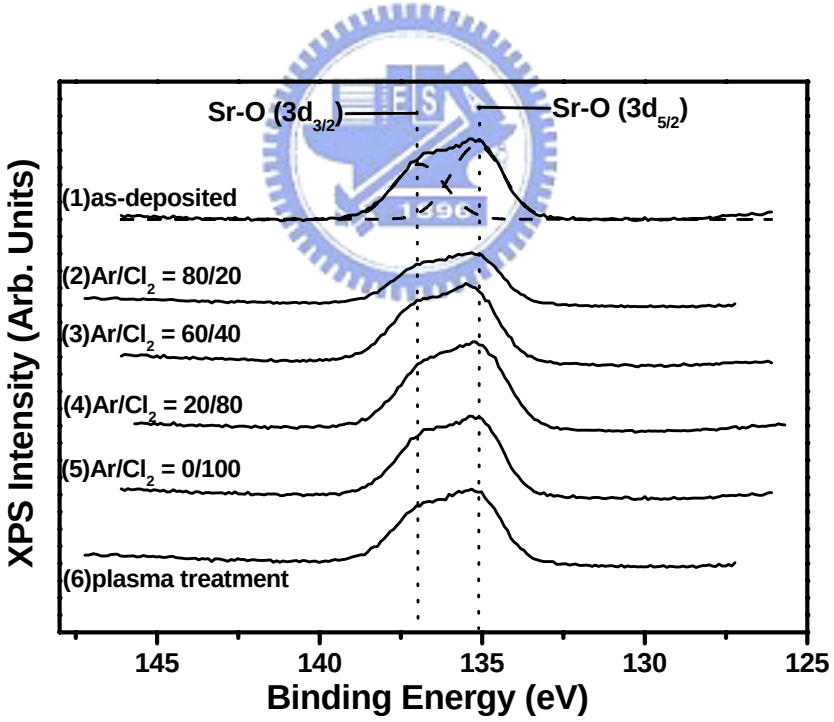


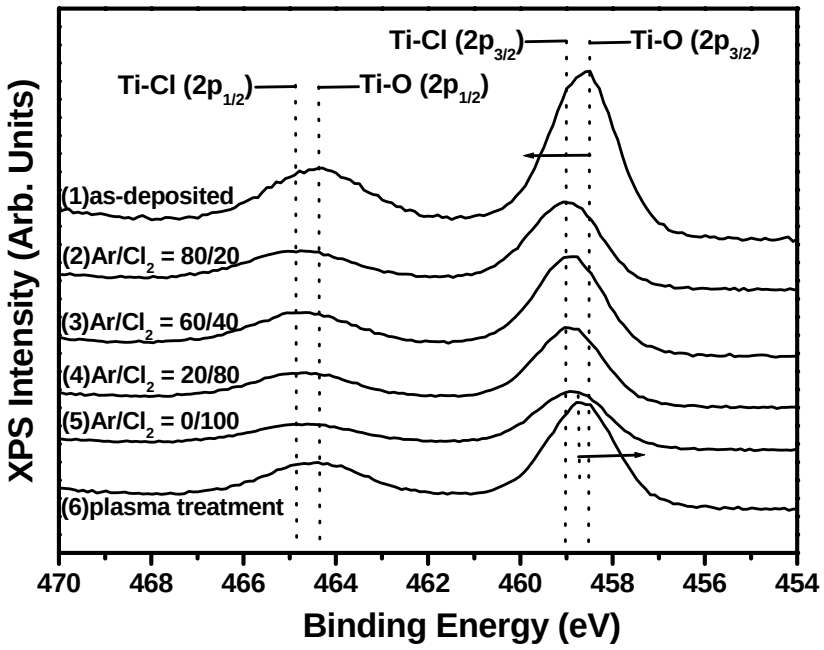
Figure 3.22 Etch rate of BST thin films as a function of gas mixture.


Ba-Cl (3d3/2)
Ba-O (3d3/2)
Ba-O (3d5/2)
Ba-Cl (3d5/2)
(1)as-deposited
(2)Ar/Cl2=80/20
(3)Ar/Cl2=60/40
(4)Ar/Cl2=20/80
(5)Ar/Cl2=0/100
(6)plasma-treatment
XPS Intensity (Abs. Units)
800
795
790
785
780
775
Binding Energy (eV)

(a)


Sr-O (3d3/2)
Sr-O (3d5/2)
(1)as-deposited
(2)Ar/Cl2 = 80/20
(3)Ar/Cl2 = 60/40
(4)Ar/Cl2 = 20/80
(5)Ar/Cl2 = 0/100
(6)plasma treatment
XPS Intensity (Arb. Units)
145
140
135
130
125
Binding Energy (eV)

(b)



(c)

Figure 3.23 (a) Ba 3*d*, (b) Sr 3*d*, and (c) Ti 2*p* XPS narrow scan spectra of the as-etched BST thin films with various Ar/Cl_2 gas mixing ratio, and oxygen surface plasma treatment.

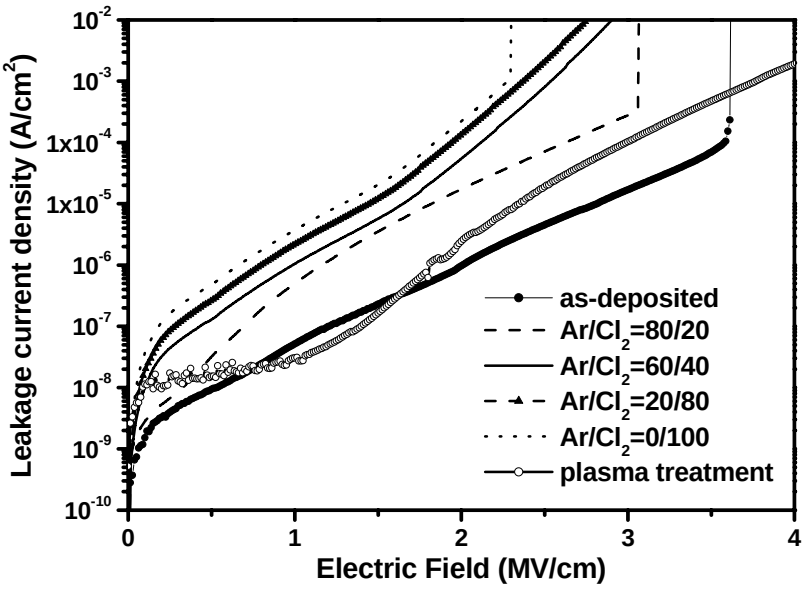
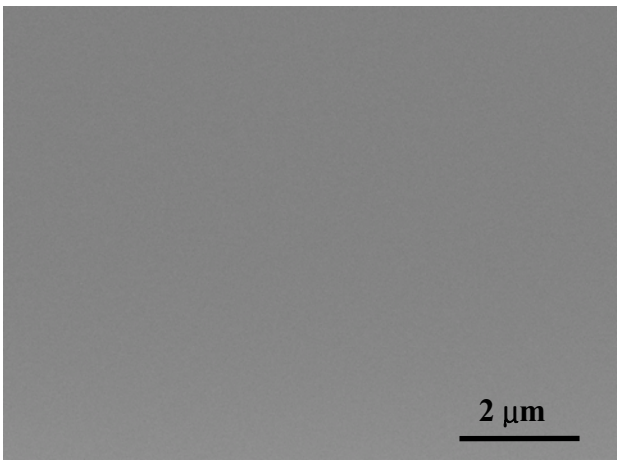
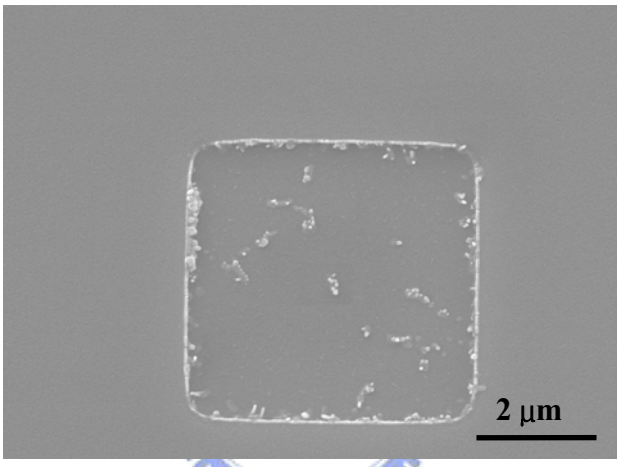


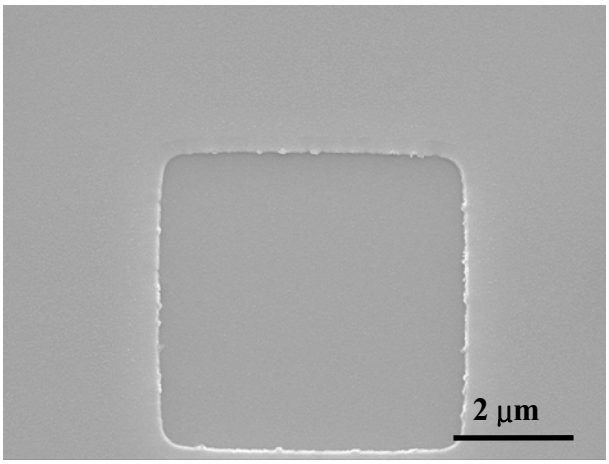
Figure 3.24 Leakage current characteristics of the as-etched and oxygen surface plasma treatment BST thin films.



(a)



(b)



(c)

Figure 3.25 SEM photographs of (a) the as-deposited BST thin film; as-etched BST thin films (b) before and (c) after oxygen surface plasma treatment.

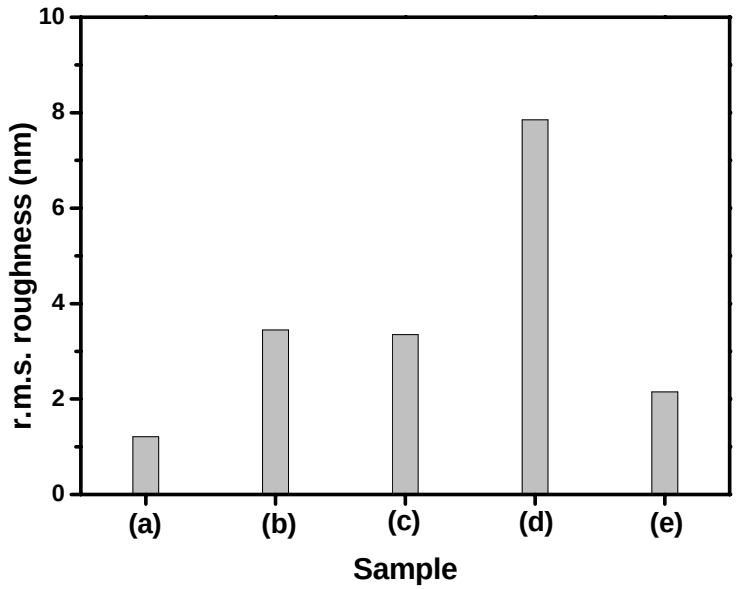


Figure 3.26 Rms roughness value of as-etched BST thin films as a function of Ar/Cl_2 gas mixing ratio and oxygen surface plasma treatment sample: (a) as-deposited BST thin film, (b) pure Ar etched BST thin film, (c) (sample (b)) after oxygen surface plasma treatment, (d) $Ar(80\%)/Cl_2(20\%)$ etched BST thin film, and (e) (sample (d)) after oxygen surface plasma treatment.

Chapter 4

Impact of Diffusion Barrier Layers on Integration of Low-*k* SiOC:H and Copper

4.1 Introduction

As devices in integrated circuits continue to be reduced in size, the resistance-capacitance (*RC*) delay of the interconnection increases [1,2]. In practice, aluminum or aluminum alloys are employed as interconnect metals and the plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 has been used to form the intermetal dielectric material in integrated circuits (*ICs*). Yet, the resistivity (ρ) of aluminum (ρ~2.7 μΩ-cm) and the dielectric constant of PECVD SiO_2 (k~3.9) are unsuitable for next-generation interconnections. A low-k (k<3.9) intermetal dielectric and a metal with a low resistivity, such as copper (ρ~1.7μΩ-cm), are required in the next-generation of ICs, to ensure that the interconnection system performs well with small RC delay [3,4]. Hydrogenated silicon oxycarbide (SiOC:H), formed by high density plasma chemical vapor deposition (HPDCVD), has become the leading candidate for replacing SiO_2, because of its low dielectric constant (~2.9) and excellent interlayer features when used in damascene interconnects [5]. Its properties were studied in detail and are present elsewhere [5]. HDPCVD dielectrics with excellent electric properties outperform those formed by other methods; our recent work described the formation of dielectrics [6,7].

Meanwhile, Cu interconnections have several disadvantages when used in device process technology. For instance, the Cu film is easily oxidized, and Cu atoms or ions

easily diffuse into the low-*k* interlayer dielectric film by thermal annealing or under the influence of an electric field, causing the interconnection to fail [8]. Hence, a diffusion barrier and an adhesion promoter in the copper interconnect is required. This barrier must be deposited good step coverage to offer a high aspect-ratio and subsequently grow Cu on it. The barrier layer must also be as thin as possible, so as not to degrade the electrical performance of the Cu wiring. Diffusion barriers of refractory metals and their nitrides in copper metallization have been extensively investigated, because of their superior thermal stability and high conductivity, such as those of Ti, Ta, Ti–N, Ta–N and W–N [9-11]. Although several investigations of Ti and Ta barriers on SiO_2 and dielectrics have been published [12-14], interactions with low-*k* SiOC:H have been less well studied. The adsorption of atoms in the SiOC:H layers adjacent to the diffusion barriers during annealing may influence the integrity of the films. This study thus aims to examine interactions with the SiOC:H and evaluate the effectiveness of such barriers between the SiOC:H and the diffusion barrier. Although Cu diffusion and drift in various dielectric materials have been extensively examined [15-18], a few studies have addressed electrical behavior and reliability of SiOC:H with a diffusion barrier. In this study, very thin TaN/Ta films and low-*k* SiOC:H films in metal-insulator-semiconductor (MIS) capacitors are investigated and leakage current conduction mechanisms proposed. The reliability is examined in terms of bias-temperature-stress (BTS) and time-dependent dielectrics breakdown (TDDB). Furthermore, the barrier effectiveness of Ta and TaN films is studied using the capacitance voltage method.

4.2 Device Fabrication and Characteristics Measurement

4.2.1 Experimental Methods

Test capacitors with a MIS structure were fabricated on p^+-Si substrates with a 20 nm thick Ti, TiN, Ta or TaN barrier layer sandwiched between Cu and SiOC:H layer. **Figure 4.1** shows the schematic cross section of the MIS capacitor. A 20nm-thick thermal SiO_2 layer was initially grown on Si to produce a high-quality dielectric–semiconductor interface. The SiOC:H film, 300 nm thick, was fabricated using a HDPCVD system, with trimethysilane [$Si(CH_3)_3H$,3MS] and nitrous oxide (N_2O) as precursors at 10 and 90 sccm, respectively. Radio-frequency (rf) power and substrate temperature were 500 W and 300°C, respectively. The Ta barrier was sputtered from a Ta target in Ar ambient at a pressure of 2 mTorr, while the TaN barrier was reactively sputtered using the same Ta target with Ar/N_2 flow rates of 20/5 sccm at the same pressure of 2 mTorr. The PVD-Ti or TiN barrier layer was sputter deposited on the SiOC:H layer using a sputtering system with a base pressure of $5x10^{-7}$ Torr and no intentional substrate heating. A CVD-Ti or TiN film was deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 550^0C, using a mixture of $TiCl_4$, NH_3, H_2 and Ar. The process chamber pressure was at 5 Torr and the rf power was 350 W. The Cu overlay (200 nm) was deposited by sputtering onto the barrier layer at room temperature to form a Cu/barrier/SiOC:H/Si MIS structure. The prepared samples were then annealed in a vacuum at 10^{-7} torr for 30 min at various temperatures up to 700°C, to determine the thermal stability of the samples. A 200nm-thick Al backside sputtering produces an electrical contact during the measurement.

To study the electrical behaviors and reliability of Ta/TaN films between SiOC:H

and Cu. The SiOC:H film, 200 nm thick, was fabricated using an inductively coupled plasma (ICP) HDPCVD system, with trimethysilane [$Si(CH_3)_3H$,3MS] and nitrous oxide (N_2O) as precursors at 10 and 90 sccm, respectively. Radio-frequency (rf) power and substrate temperature were 500 W and 300°C, respectively. Electrodes were sputtered on top of the SiOC:H dielectrics using a shadowmask, which was used to yield a circular metal gate with an area of about $3.14x10^{-2}$ mm^2. Ta and TaN layers, 20 nm thick, were deposited by sputtering from a Ta metal (99.95% purity) target at a dc power of 500 W, respectively. The atmospheres in which were sputtered Ta and TaN were 20 sccm pure Ar and a 20/5 sccm Ar/N_2 mixture, respectively. Finally, a 300nm-thick copper film was prepared by sputtering a pure Cu metal target, at a dc power of 1500 W, and then reactively sputter-depositing a 50nm-thick TaN layer on the Cu surface to prevent the oxidation of the Cu electrode during the subsequent thermal process. **Figure 4.2** presents the structures of Cu-gated and Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics. A 200nm-thick Al backside sputtering produces an electrical contact during the measurement.

4.2.2 Characteristics Measurement

The sheet resistance (*Rs*) measurement using the four-point probe method was employed to characterize the obtained barrier films. The surface roughness and morphology of the films were determined using the atomic force microscope (AFM, Digital Instruments Nano-Scope Ⅲ) with a 0.5 Hz scanning frequency in an air ambient. A thermal desorption spectrometer (TDS, Hitachi Tokyo Electronics) was utilized to monitor the amount of moisture desorbed by the SiOC:H film. The diffusion and reaction that took place at the interfaces or surface of the barrier/SiOC:H caused by annealing were estimated by comparison with a surface

micrographs obtained by a thermal emission scanning electron microscope (TFSEM, JEOL JSM-6500F). Auger electron spectroscopy (AES, VG Microlab 310F) was used to determine the composition of the diffusion barrier films.

The probe station with a 6 in. water-cooled chuck was situated in a hot chuck system, which was a hermetically sealed aluminum enclosure designed specifically for Cu drift studies. The room temperature capacitance-voltage (*C–V*) characteristics at 1 MHz were obtained using a Keithley package 82 system at a voltage sweep rate of 0.25 V/s. Current density-electric field (*J–E*) and current-time (*I–t*) characteristics were measured using a Hewlett-Packard (HP4156A) semiconductor parameter analyzer, and a Keithley package 82 system to supply bias during the BTS experiments. After the test samples were loaded, the hot chuck was purged with N_2 for at least 1 h before high-temperature test was conducted. These precautions minimize the oxidation of Cu electrodes during high-temperature testing and prevent the dielectrics from absorbing ambient moisture during testing. BTS tests were performed at 175-250°C in electric fields of up to 1.5 MV/cm. In high-temperature testing, samples were initially heated to the target temperatures, and then the bias was applied for particular periods, ranging from a few minutes to several hours. After the period of stress or the samples had broken down, the hot chuck was cooled to room temperature. The voltage sweeping direction was set such that a MIS capacitor starts from the inversion region and ends in the accumulation region to prevent the deep depletion of capacitors.

4.3 Results and Discussion

4.3.1 Influence of Ti, TiN, Ta and TaN Layers on Integration of Low-*k* SiOC:H and Cu

4.3.1-1 Physical Property

Figure 4.3 presents the TDS spectra of the SiOC:H/Si sample from 25° to 800°C. In the TDS spectra, the primary peaks observed are H_2O with a major mass peak at 18 and CH_4 with a major mass peak at 16, physically and chemically absorbed in the SiOC:H film. TFSEM analysis was used to analyze the microstructure and identify possible surface reactions. **Figures 4.4** present the top-views of the as-deposited Ti on SiOC:H using CVD and PVD system. **Figure 4.4(a)** indicates that some fine compounds and cracks are present on the surface of the CVD-Ti/SiOC:H sample, but almost no compound is found on the surface of the PVD-Ti/SiOC:H sample, as depicted in **Fig. 4.4(b)**. The formation of the compounds was caused by the reaction between the inorganic precursor ($TiCl_4$) with SiOC:H in CVD-Ti deposition at 550°C. A considerable amount of O atoms desorbed from SiOC:H, which is confirmed using TDS analysis, and reacted with Ti atoms to form a Ti(O) compound, raising the resistivity of Ti significantly. Moreover, Ti atoms begin to react and form silicide at ~550°C [19].

The variation of sheet resistance as a function of the annealing temperature is commonly used to examine the capability of reaction between diffusion barriers and SiOC:H film. The difference of sheet resistance between the annealed and as-deposited samples, divided by the sheet resistance of as-deposited samples, is called the variation percentage of sheet resistance and is defined as follows [20]:

$$\frac{\Delta R_s}{R_s}\% = \frac{R_{s,annealed} - R_{s,as-deposited}}{R_{s,as-deposited}} \times 100\% \quad (4.1)$$

Figure 4.5 plots the percentage variation in sheet resistance of the barriers/SiOC:H samples following furnace annealing for 30 min at various temperatures. The results indirectly reveal the interactions between the diffusion barriers and SiOC:H. Except for that of CVD-Ti sample, the sheet resistance initially declines gradually as the annealing temperature increases because the number of crystal defects reduce and the grains of the diffusion barrier films grow. However, at certain temperature, failure of the diffusion layers result from the reaction between the diffusion barriers and the SiOC:H, and the formation of compounds. The increase in sheet resistance of the Ti sample is higher than those in TiN and TaN samples. Low increasing rate for TaN is believed to alleviate the interdiffusion and formation of compound.

Figures 4.6(a) and **(b)** show the experimental content percentage of C and O results from the interaction of the barriers with SiOC:H, based on the AES. The analyses show that the as-deposited and annealed CVD and PVD Ti, TiN, Ta and TaN films on SiOC:H films upon 600°C. As shown in **Fig. 4.6**, it is obvious that the as-deposited CVD barrier films, especially the CVD-Ti film, have a much higher C and O contents than the PVD barriers. Reaction occurs in CVD-Ti/SiOC:H system due to the decomposition of SiOC:H into Ti during deposition at 550°C. Upon 400°C annealing, a significant amount of C and O atoms incorporate into the Ti film. The high content of C and O are due to the formation of the Ti(C) and Ti(O) compounds. For the PVD-Ti film, the AES results are in agreement with sheet resistance analysis, showing the formation of compounds above 500°C annealing. Moreover, the CVD-TiN film has higher C and O contents than other nitride films. However, there is the evidence of the low reaction between TaN and underlying SiOC:H film.

Figures 4.7 display the AFM images of the PVD-Ti, PVD-TiN and CVD-TiN

layers on SiOC:H films. **Figures 4.7(a)** and **(b)** reveal that the PVD-barriers have a great roughness and a significantly columnar microstructure, which can enhance the rapid out-diffusion (at the grain boundaries) of H atoms [16]. As shown in **Fig. 4.7(c)**, the CVD-TiN film has a low roughness and fine-grained microstructure so the out-diffusion path of H atoms from the SiOC:H film reduces. Hence, the CVD-TiN barrier is expected to be more resistant to the out-diffusion of H atoms than PVD-TiN barrier. Accordingly, the C and O impurities are speculated posited to stuff the grain boundaries of the finely grained CVD-TiN barrier and to block atomic diffusion - at least the initial out diffusion of H atoms from SiOC:H. Moreover, O impurities can stuff the grain boundaries of TiN, enhancing the property of TiN barrier layers [22]. Atoms normally diffuse much more quickly through grain boundaries than through the crystal lattice. However, the diffusion of H atoms through the lattice is also fast because these atoms are small and have extremely high mobility. The Ti film has a hexagonal close-packed (hcp) structure with two types of interstitial sites - octahedral and tetrahedral [23]. The atomic radius of H (r_H=0.2r_{Ti}) is less than the minimum radius of the interstitial sites, so such interstices can provide the lattice diffusion paths for H atoms. However, the TiN film has a NaCl-type face-centered-cubic (fcc) structure, with Ti atoms' occupying normal fcc lattice sites and N atoms' filling the octahedral interstitial sites [24]. N atoms block the lattice diffusion paths for H atoms, so the lattice diffusion coefficient of H diffusion in the Ti barrier layer exceeds that the TiN film.

4.3.1-2 Electrical Property

Figures 4.8 illustrate the distribution of breakdown field for the as-deposited Cu/barrier/SiOC:H MIS capacitors having a CVD-TiN, PVD-TiN as well as TaN

diffusion barrier after annealing at 400 and 500ºC for 30 min. Compared to the samples with CVD and PVD TiN diffusion barrier, significant improvement in thermal stability was obtained, apparently due to the barrier effectiveness of a TaN layer. In fact, the sheet resistance measurement was reported that the TaN barrier in MIS capacitor can sustain a 30 min thermal annealing up to 600ºC, without causing degradation to the devices' electrical characteristics. Thus, the TaN diffusion barrier layer is believed to be enhanced the thermal stability of the Cu and SiOC:H in back-end process.

Figures 4.9 show the *C–V* results of MIS capacitors subjected to BTS at 250ºC for different stressing time. In BST/*C-V* analysis, capacitors were stressed under 60 V (2 MV/cm). The Cu^+ ions drift rate will change when stressing time increase. This can happen because Cu^+ ions can pile up at a dielectrics-Si interface creating increasing electric field opposing the external electric field. Continuous flatband voltage shift (ΔV_{FB}) in negative direction under 2 MV/cm is likely caused by Cu^+ ions drift through SiOC:H and reached SiO_2-Si interface or even gone into Si substrate. For the Cu/PVD-TiN/SiOC:H MIS capacitor, ΔV_{FB} is much larger than that of other capacitors, thus, some of these Cu^+ ions might become neutralized and generate electrically effective trap centers near the Si interface and in bulk Si substrate. These deep-level states generated by Cu near the SiO_2-Si interface reduce the device lifetime. As shown in **Fig. 4.9(c)**, the constant inversion capacitance of Cu/TaN/SiOC:H MIS capacitor after BTS suggests that low Cu^+ ions drift through SiOC:H and reach SiO_2-Si interface, as expected.

4.3.2 Influence of Bias-Temperature Stressing on the Electrical Characteristics of SiOC:H Film with Cu/TaN/Ta-gated Capacitor

4.3.2-1 Electrical characteristic

The drift diffusion of Cu^+ ions is studied by determining the shift in the flatband voltage (V_{FB}) in the *C-V* curve for processed Cu gate capacitors before and after BTS. V_{FB} is determined by the number of charges in the dielectric and at the dielectric/Si interface [25]. The contribution of the flatband voltage shift of Cu^+ ions ($\Delta V_{FB[Cu^+]}$) after positive bias BTS is applied can be extracted by subtracting the flat band voltage shift of a Cu/TaN/Ta-gated capacitor ($\Delta V_{FB[Cu/TaN/Ta]}$) from that of a Cu-gated capacitor ($\Delta V_{FB[Cu]}$), using Eq. (4.2), to demonstrate the effectiveness of the barrier layers and the Cu injection mechanism.

$$\Delta V_{FB[Cu^+]} = \Delta V_{FB[Cu]} - \Delta V_{FB[Cu/TaN/Ta]} \tag{4.2}$$

Therefore, a positive flatband voltage shift reveals an increase in the positive charge (Cu^+) in the SiOC:H film. **Figure 4.10** shows the flatband voltage shift of the Cu^+ ions ($\Delta V_{FB[Cu^+]}$) versus stressing time at various temperatures in the electric field of 1.5 MV/cm, using Eq. (4.2). Every data point is a mean of results from ten tested capacitors. MIS gate capacitors stressed at 175 and 200°C exhibit minor changes of $\Delta V_{FB[Cu^+]}$ as the stressing time changes, while capacitors stressed at 225 and 250°C have a higher $\Delta V_{FB[Cu^+]}$ of Cu^+ ions. The general trend clearly suggests the continuous injection of Cu^+ ions and the rapid injection of Cu^+ ions at high temperature.

The drift rate of Cu^+ ions is determined from the gradients of the lines fitted using Eq. (4.3), to quantify the diffusion [26].

$$\frac{d[Cu^+]}{dt} = -\frac{C_{ox}}{q}\frac{d(\Delta V_{FB[Cu^+]})}{dt} \tag{4.3}$$

where [Cu^+] is the Cu^+ ion concentration per unit area; C_{ox} is the dielectric stack capacitor per unit area, and q is the magnitude of the charge on an electron ($1.6x10^{-19}$ C). This equation assumes that the Cu^+ ions drifted to the SiO_2/Si interface. The initial drift rate is determined by the change in the electric field in the dielectric with time, due to the accumulation of Cu^+ ions. **Figure 4.11** displays Arrhenius plots of the drift rates in the different MIS capacitors. Increasing the temperature increases the drift rate of Cu^+ ions in the material. Moreover, the drift rates of Cu^+ ions in HDPCVD SiOC:H layers are markedly lower than those in PECVD SiOC:H layers [27]. These characteristics - the low hydrogen (low defect sites) and the high oxygen concentration (enhanced porous densities) - of SiOC:H films deposited on the HDPCVD system, reduce the number of carrier-trapping sites, and therefore, slightly reduce the drift rate of Cu^+ ions [5].

The drift of Cu^+ ions into the SiOC:H film was examined using *J–E* analysis. The *J–E* characteristics of Cu-gated and Cu/TaN/Ta-gated MIS capacitors were measured at 175, 200, 225 and 250°C and are plotted in **Figs. 4.12(a)** and **(b)**, respectively. The Cu-gated MIS capacitor exhibits consistently higher leakage current ($8x10^{-10}$~$2x10^{-8}$ A/cm^2 at 1 MV/cm) than a Cu/TaN/Ta-gated MIS capacitor ($2x10^{-10}$~$5x10^{-10}$A/cm^2 at 1 MV/cm) at the same temperature. The higher leakage current of a Cu-gated MIS capacitor is probably related to the ionization and injection of Cu^+ ions into dielectrics. According to a physical model introduced elsewhere [27,28], Cu atoms are ionized into Cu^+ ions at gate interface under positive gate bias, and these Cu^+ ions are then injected into the dielectrics, leaving behind electrons collected using an external instrument. In an external electric field, the flux of Cu^+ ions from gate to the SiO_2/Si interface, and the electrons collected by an external instrument tend to increase the leakage current. The difference between the leakage current densities of the Cu-gated and Cu/TaN/Ta-gated MIS capacitors (J_{diff}) were measured and given in **Fig. 4.13**.

J_{diff} increases with electric field and temperature, indicating that Cu^+ ions drift into the HDPCVD SiOC:H is the probable cause of larger J_{diff}. Based on the assumption that the drifting of Cu^+ ions into SiOC:H determines $\Delta V_{FB[Cu^+]}$ in BTS/*C–V* analysis and J_{diff} in *J–E* analysis, $\Delta V_{FB[Cu^+]}$ should be linearly correlated with J_{diff} according to,

$$\Delta V_{FB[Cu^+]}(t) = \frac{Q_{Cu}(t)}{C_{ox}} \propto \frac{1}{C_{ox}} \int_0^t J_{diff}(\tau) dt \tag{4.4}$$

where C_{ox} is the capacitance per unit area, and $Q_{Cu}(t)$ is the accumulated Cu^+ ions charge density. **Figure 4.14** compares J_{diff} at 1.5 MV/cm (30V), which is the voltage used in the BTS/*C–V* test, to $\Delta V_{FB[Cu^+]}$ after 40 min BTS. A good linear correlation is found between $\Delta V_{FB[Cu^+]}$ and J_{diff}, revealing that J_{diff} is related to the number of injected Cu^+ ions.

4.3.2-2 Electrical Mechanism

Several mechanisms may govern the conduction of the leakage current in the Cu/TaN/Ta-gated MIS capacitor, including Schottky emission, the Poole-Frenkel effect, electronic hopping conduction and tunneling [18,29-31]. Schottky emission is modeled as [31],

$$J = AT^2 \exp\left(-\frac{q\phi_0}{kT}\right) \exp\left(\frac{\beta}{kT} E^{1/2}\right) \tag{4.5}$$

where A is a constant; T represents the absolute temperature, q is the electronic charge, ϕ_0 is the barrier height, k is the Boltzmann constant, and β is given by

$$\beta = \left(\frac{q^3}{4\pi\varepsilon_0\varepsilon}\right)^{1/2} \tag{4.6}$$

where ε_0 is the permittivity of free space and ε is the high-frequency dielectric constant. **Figure 4.15(a)** plots ln(J) as a function of $E^{1/2}$. The figure demonstrates that

different conduction mechanisms dominate in different electric field regimes. Two linear regions are observed, and the slope yields the corresponding effective dielectric constant in the electric field E<1.25 MV/cm. The figure demonstrates that the dominant conduction mechanism in the Cu/TaN/Ta-gated MIS capacitor is Schottky emission in the electric field E<1.25 MV/cm, at which electrons from the cathode overcome the Ta/SiOC:H energy barrier before they are emitted. **Figure 4.15(b)** presents Richardson plots of $\ln(J/T^2)$ vs. ($1000/T$) associated with a close examination of Schottky emission transport, for electric fields between 0.5 and 1.25 MV/cm. The straight lines fitted to the data points are quite consistent with Schottky emission. The leakage current density increases with the measured temperature and the electric field, because when an electron enters the SiOC:H, it generates an image field that adds to and subtracts from the barrier field, reducing barrier height and increasing current.

When electric field E>1.5 MV/cm, electrical conduction is governed by Poole-Frenkel emission, which is described by [31],

$$J = CE\exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta_{PF}}{kT}E^{1/2}\right) \tag{4.7}$$

where C is a constant and β_{PF} is defined by

$$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2} \tag{4.8}$$

Figure 4.16(a) plots $\ln(J/E)$ as a function of $E^{1/2}$. The gradient in the linear region yields the corresponding effective dielectric constants in electric field E>1.5 MV/cm, which value is close to that obtained from the C-V measurement. Therefore, Poole-Frenkel emission is deduced to dominate in electric field E>1.5 MV/cm. The leakage current increases with the temperature, as shown in **Fig. 4.16(b)**. Poole-Frenkel emission results from the field-enhanced excitation of trapped electrons into the conduction band of the dielectric and its existence in Cu/TaN/Ta-gated MIS

capacitor indicates the presence of electron traps. In fields of over 1.5 MV/cm, electrons in SiOC:H bulk traps absorb sufficient energy to be excited to the conduction band and Poole-Frenkel emission then dominates conduction.

4.3.2-3 Device Lifetime

The impact of Cu^+ ions on breakdown has been examined by comparing the TDDB test results of Cu-gated and Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics. **Figure 4.17** plots the *I-t* characteristics of the SiOC:H MIS capacitors at 200-250°C and 2.5 MV/cm. At the beginning of the stress test, the leakage current declined. The decrease in the current in the first stage is believed to be caused by electron trapping in the dielectric films [32,33]. After the majority of the electron traps have been filled, the leakage currents decrease during the middle stage. However, the leakage current rapidly increased and fatal breakdown occurred after stress was applied for a longer period. The Cu-gated capacitor has a higher leakage current than the Cu/TaN/Ta-gated capacitor under the same test conditions. The Cu/TaN/Ta-gated MIS capacitor was found to exhibit a time-to-breakdown value (t_{BD}) of over 75 min at 250^0C, longer than of the Cu-gated MIS capacitor, which broke down after 25 min at 200^0C. In the Cu-gated capacitor, the data reveals that the leakage curve during TDDB increases a lot just before breakdown due to the degradation of the SiOC:H film. *Li et al.* reported that the leakage curve may not increase before the breakdown even if there are Cu^+ ions [34]. Therefore, the higher leakage current of the Cu-gated capacitor is believed to be caused by defects (like moisture) in the samples due to process and absence of a passivation layer protecting the SiOC:H film.

4.3.2-4 Mechanism of Injection of Cu^+ ions

Physical models previously presented by other researchers suggest that Cu atoms are thermally ionized at the Cu-dielectric interface, leaving behind free electrons, while the Cu^+ ions drift towards the substrate under the influence of the applied positive bias [15,35]. **Figures 4.18(a)** and **(b)** show the injection of Cu^+ ions in Cu-gated and Cu/TaN/Ta-gated MIS capacitors, respectively. The physical model displayed in **Fig. 4.18(a)** describes the drift kinetics of Cu^+ ions. A positive electric field ionizes Cu atoms and then injects the resulting Cu^+ ions into the SiOC:H dielectrics, generating leakage currents. They accumulate at the interface, setting up an uncompensated positive space charge near the Si substrate, as indicated by the shift in *C-V* analyses. Hence, the dielectric conduction and valence band edges are distorted such that the magnitude of electric field is increased while Cu^+ ions accumulate in the dielectrics. In the absence of Cu^+ ions, however, the electric field of a Cu/TaN/Ta-gated MIS capacitor is distributed uniformly, as presented in **Fig. 4.18(b)**. A lower Cu ionization rate at the Cu-dielectric interface and a lower Cu^+ ions drift rate in the dielectric are desired to slow the rate of accumulation of Cu^+ ions in the dielectric and thus increase t_{BD}.

4.4 Summary

The interaction between low-*k* dielectric SiOC:H and diffusion barrier layers varied with the annealing temperature. Deposition of CVD-Ti layer at 550^0C, O and C atoms were dissolved into the Ti film to form Ti(O) and Ti(C) compounds, increasing the sheet resistance. The Ti did not improve the loss of H from SiOC:H caused by the thermal decomposition, however, the TiN block the lattice diffusion path for H atoms. The drift of Cu^+ ions was used to investigate the effectiveness of diffusion barrier layers using BST/*C*-*V* analysis. Under a 2 MV/cm electric field, higher Cu^+ ions drift resistance for TaN layer was compared to CVD and PVD TiN layers.

The drift of copper Cu^+ ions into a SiOC:H film, which is a promising low-*k* material for use in inter-layer dielectrics in ultra-large scale integrated circuit interconnects, was examined using BTS/*C*–*V* and *J*–*E* plots at elevated temperatures and in TDDB tests. The physical model demonstrates that Cu^+ ions significantly accelerate the breakdown of SiOC:H films, and the buildup of positively charged Cu^+ ions in the dielectric cathode region is believed to enhance the local electric field and accelerate thermochemical breakdown process, distorting the dielectric conduction and valence band edges, and increasing the magnitude of the electric field. Integrating Cu in low-*k* SiOC:H with poor Cu resistance involves thin TaN and Ta diffusion barrier layers, which effectively provide a low leakage current density of around $2x10^{-10}$ A/cm^2 at 1 MV/cm, a high breakdown field at E>4 MV/cm of over $1.0x10^{-6}$ A/cm^2, and a low Cu^+ ion drift rate at various temperatures in the Cu/TaN/Ta-gated MIS capacitor.

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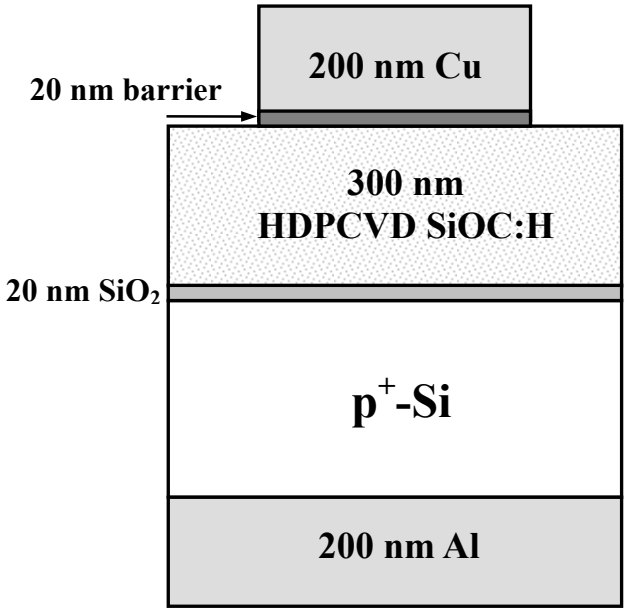
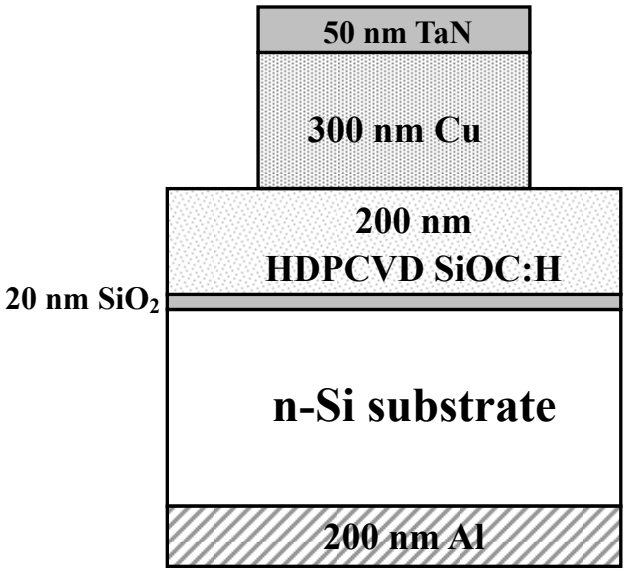
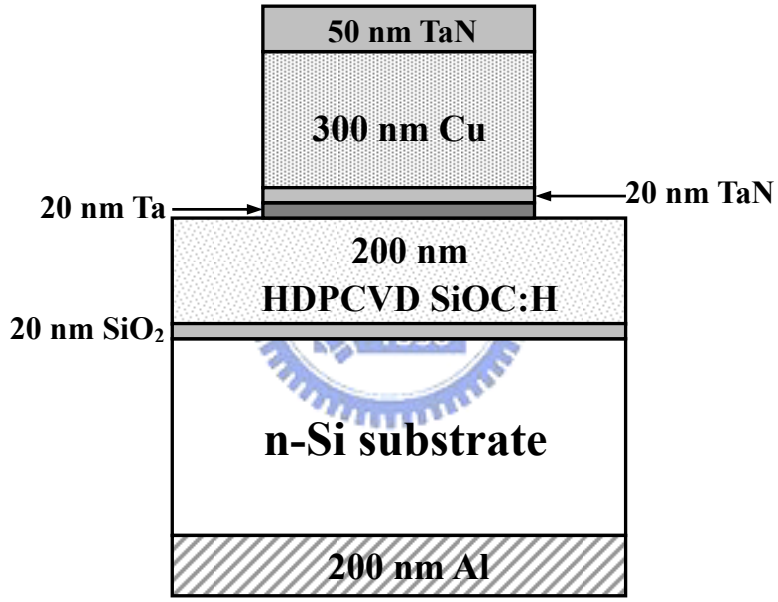


Figure 4.1 The structures of Cu/barrier/SiOC:H MIS capacitor.



(a)



(b)

Figure 4.2 Structures of (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics.

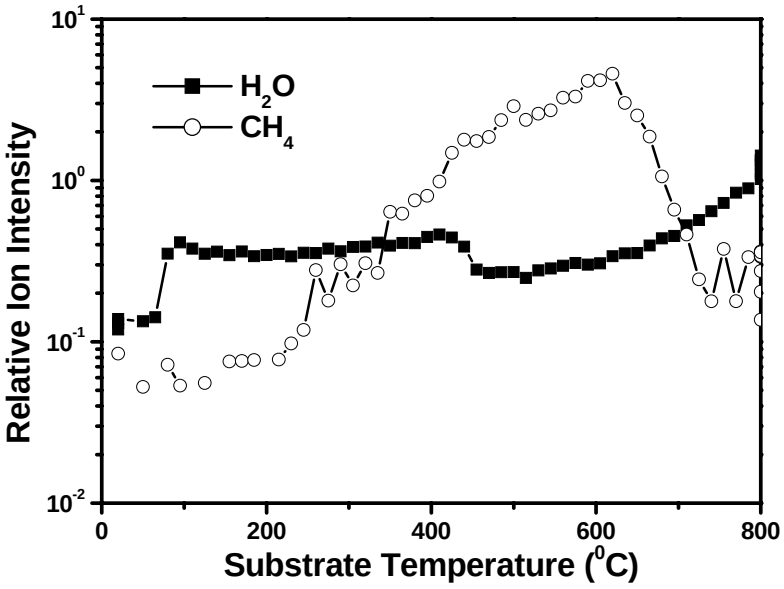
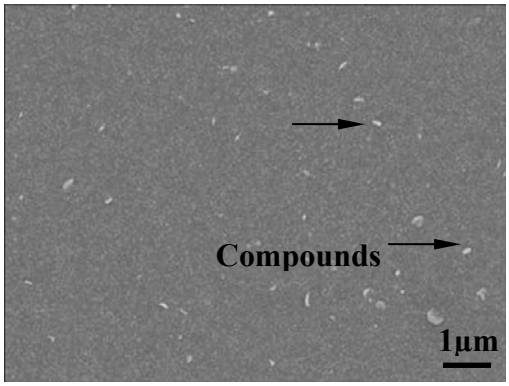
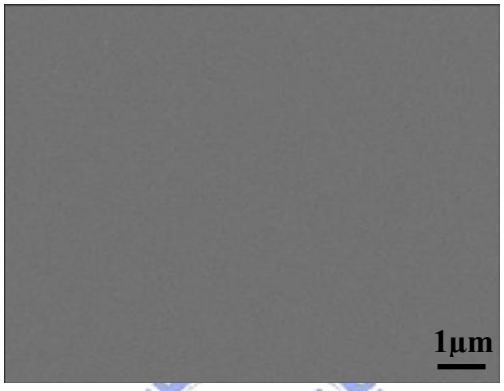


Figure 4.3 TDS spectra of H_2O and CH_4 desorption as functions of temperature for the SiOC:H film.



(a)



(b)

Figure 4.4 Top-view SEM micrographs showing the surface morphology of the (a) CVD-Ti and (b) PVD-Ti capacitors.

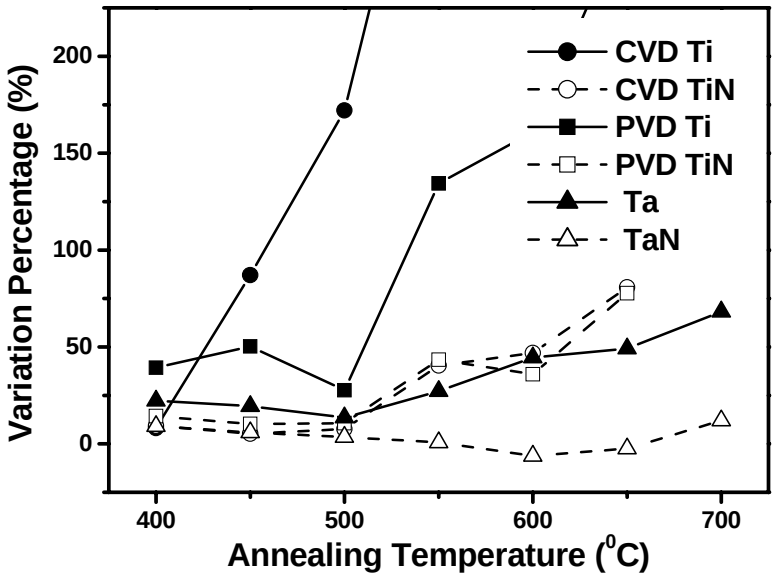
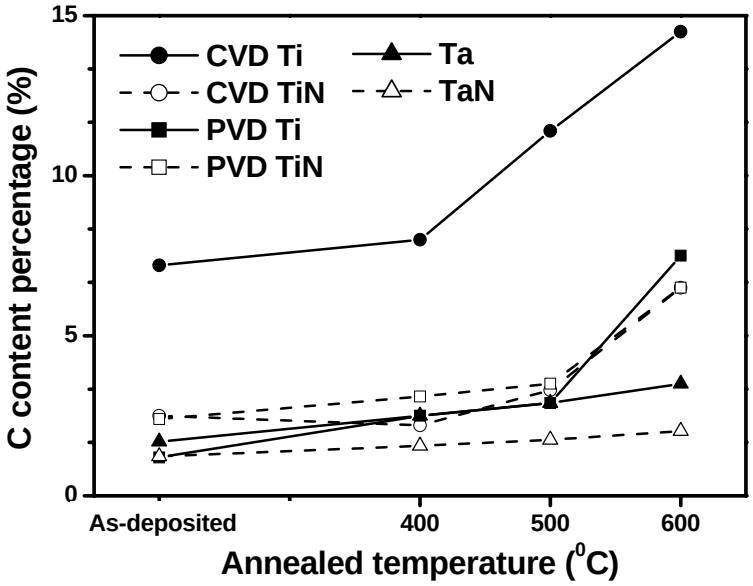
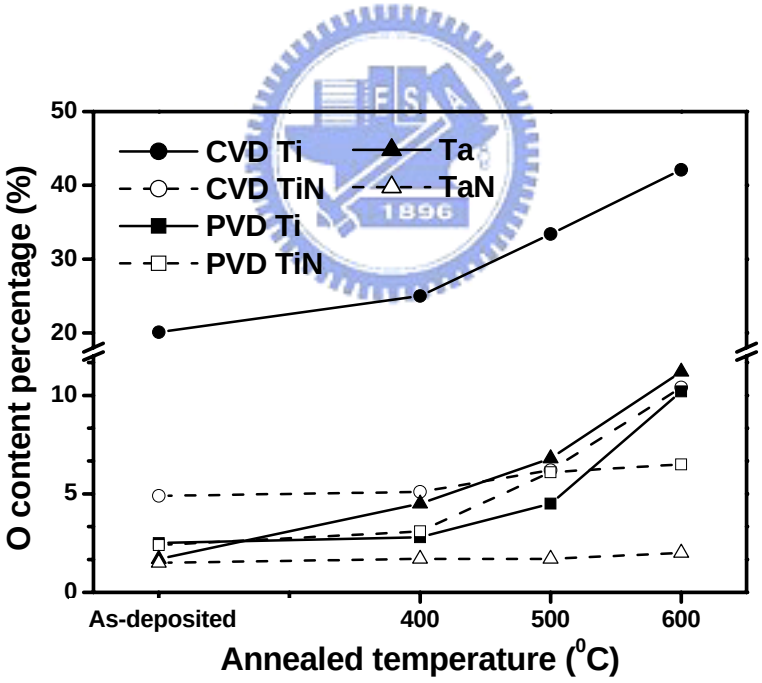


Figure 4.5 Percentage variation in sheet resistance of diffusion barrier layers on SiOC:H/Si structures as a function of annealing temperatures range from 400 to 700ºC.

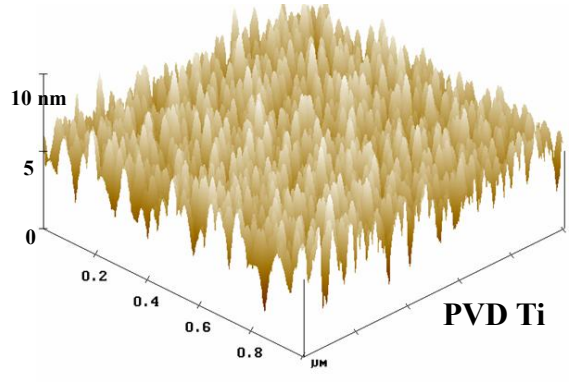


(a)



(b)

Figure 4.6 Experimental content percentage of (a) C and (b) O results from the interaction of the barriers with SiOC:H before and after annealing at 400-600ºC, based on the AES.



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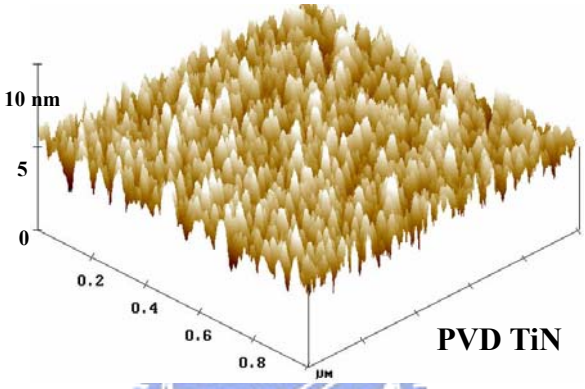

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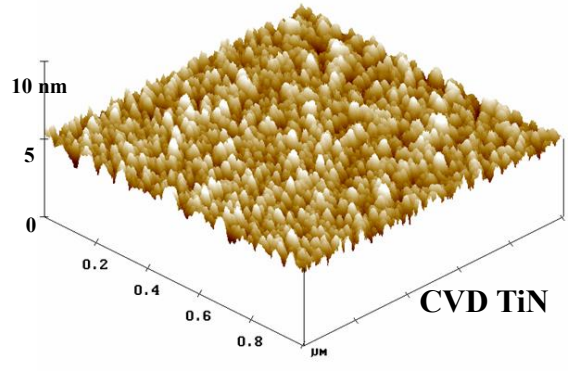
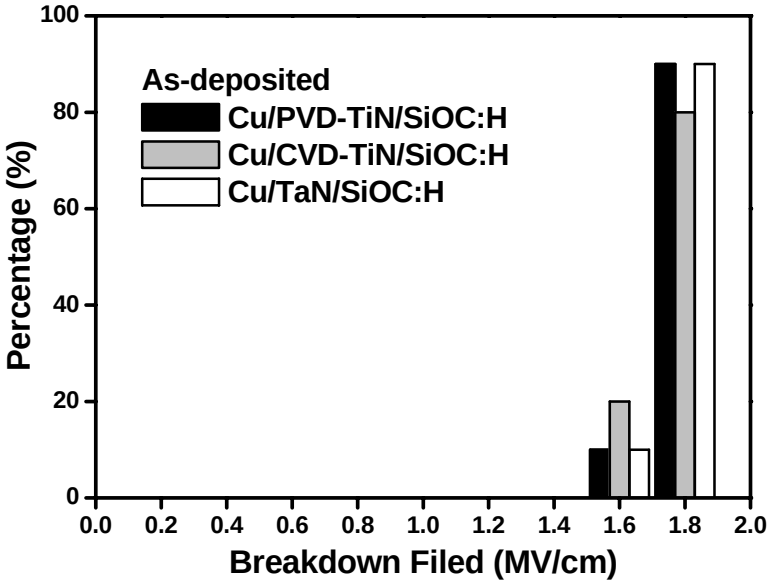
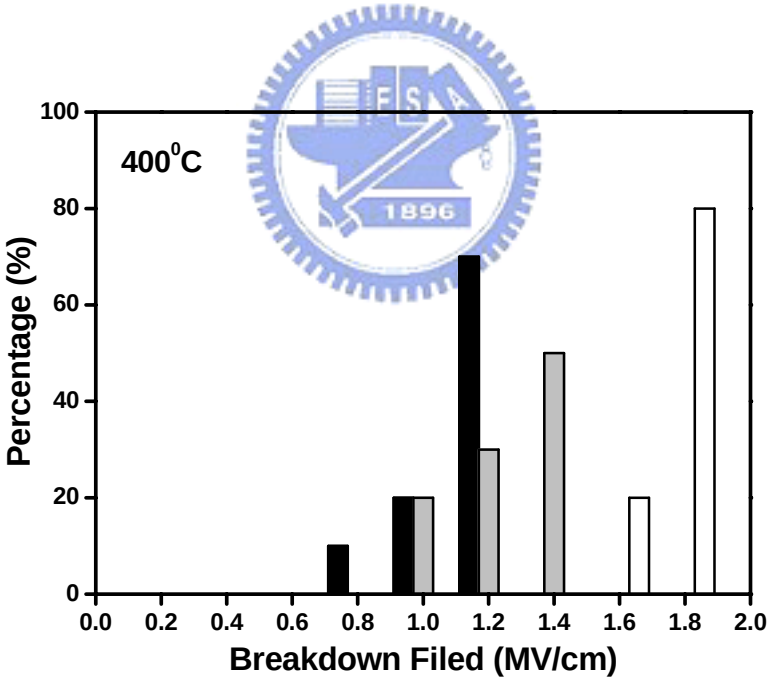


(c)

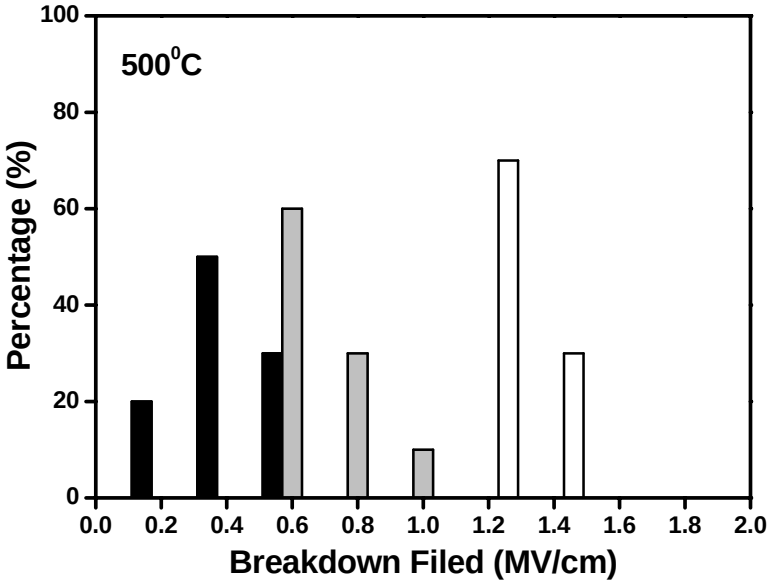
Figure 4.7 AFM images of the (a) PVD-Ti, (b) PVD-TiN and (c) CVD-TiN MIS capacitors.


As-deposited
Cu/PVD-TiN/SiOC:H
Cu/CVD-TiN/SiOC:H
Cu/TaN/SiOC:H
Percentage (%)
Breakdown Filed (MV/cm)
0
20
40
60
80
100
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

(a)

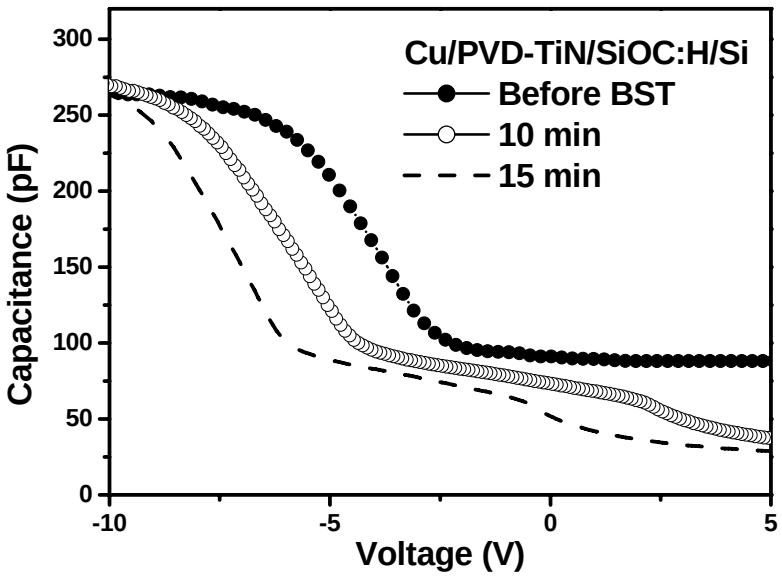

400°C
Percentage (%)
Breakdown Filed (MV/cm)
0
20
40
60
80
100
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

(b)

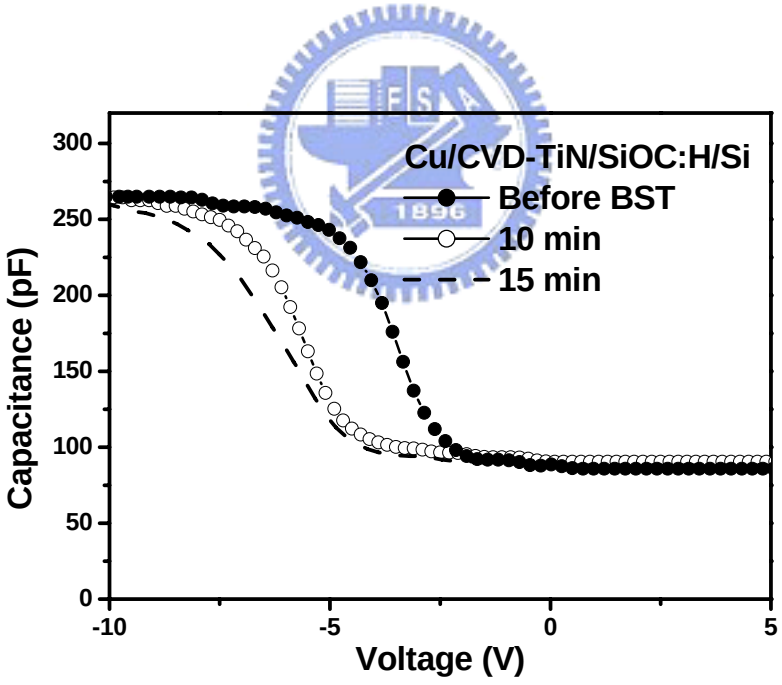


(c)

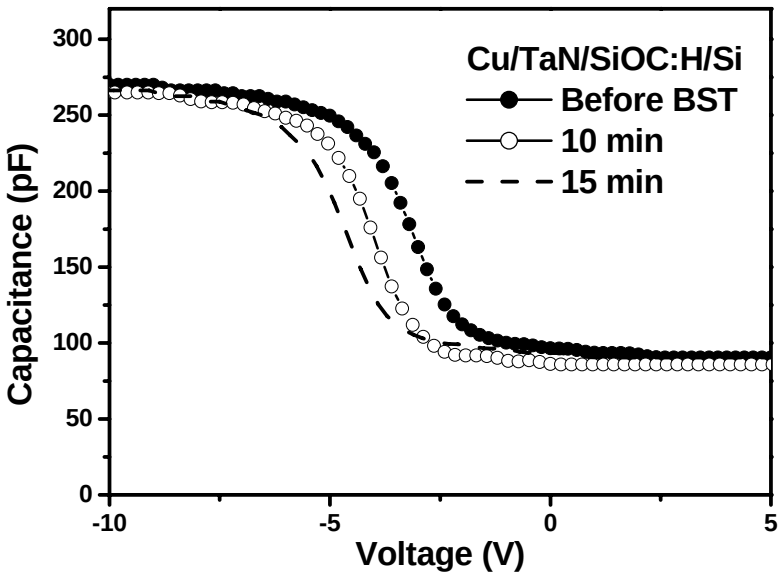
Figure 4.8 Breakdown field distributions of (a) as-deposited Cu/barrier/SiOC:H MIS capacitors and after annealing at (b) 400ºC and (c) 500ºC for 30 min.


Cu/PVD-TiN/SiOC:H/Si
Before BST
10 min
15 min
Capacitance (pF)
Voltage (V)
300
250
200
150
100
50
0
-10
-5
0
5

(a)


Cu/CVD-TiN/SiOC:H/Si
Before BST
10 min
15 min
Capacitance (pF)
Voltage (V)
300
250
200
150
100
50
0
-10
-5
0
5

(b)



(c)

Figure 4.9 *C-V* characteristics with Cu/barrier/SiOC:H MIS capacitor after BTS at 2 MV/cm and 250ºC for the (a) PVD-TiN, (b) CVD-TiN and (c) TaN layer.

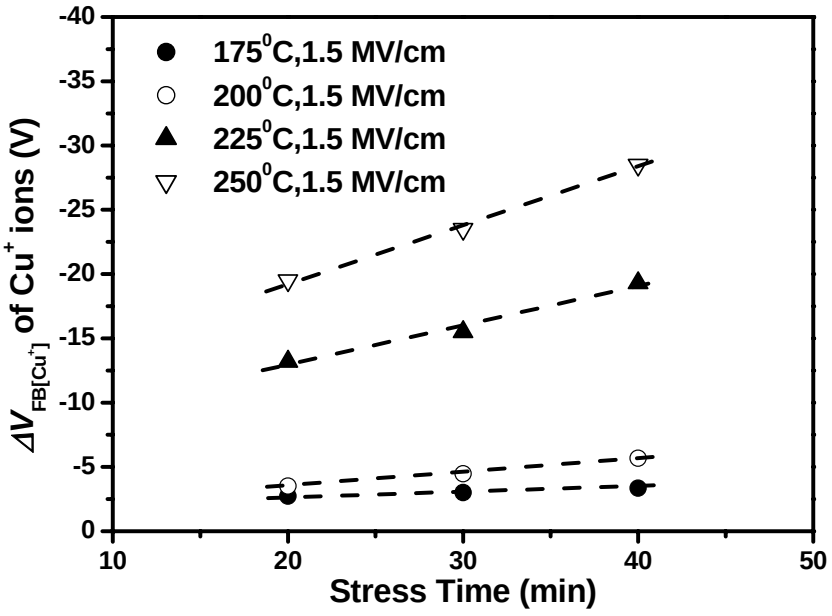


Figure 4.10 Flatband voltage shift $\Delta V_{FB[Cu^+]}$ of Cu^+ ions versus BTS temperature under various stress time at 1.5 MV/cm.

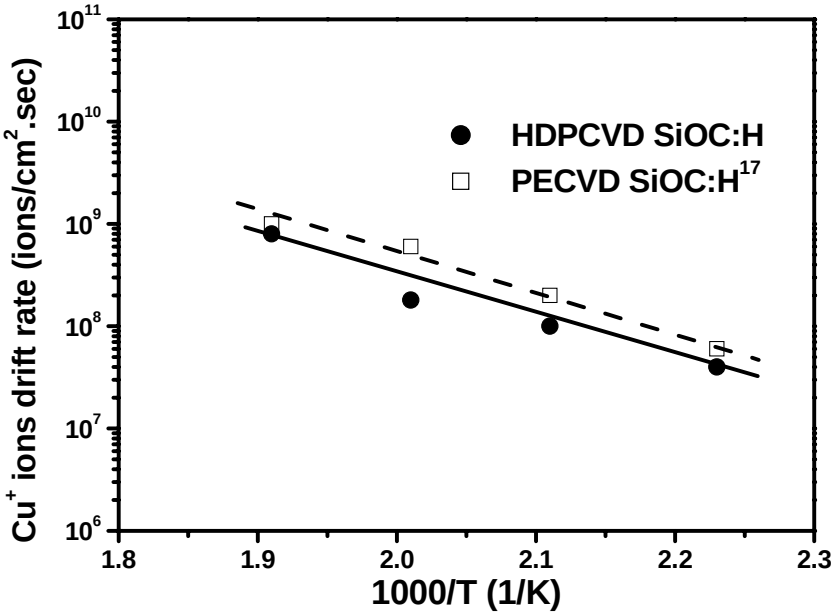
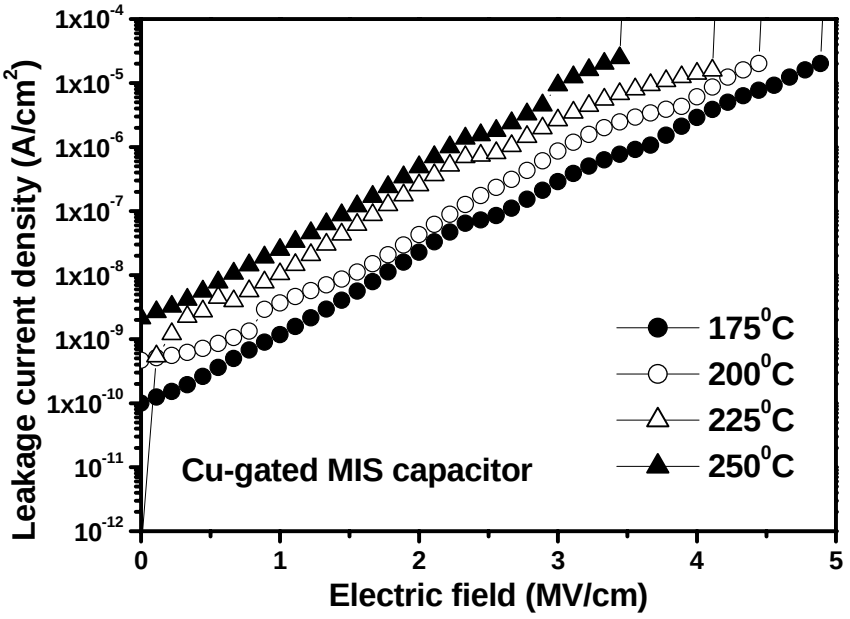
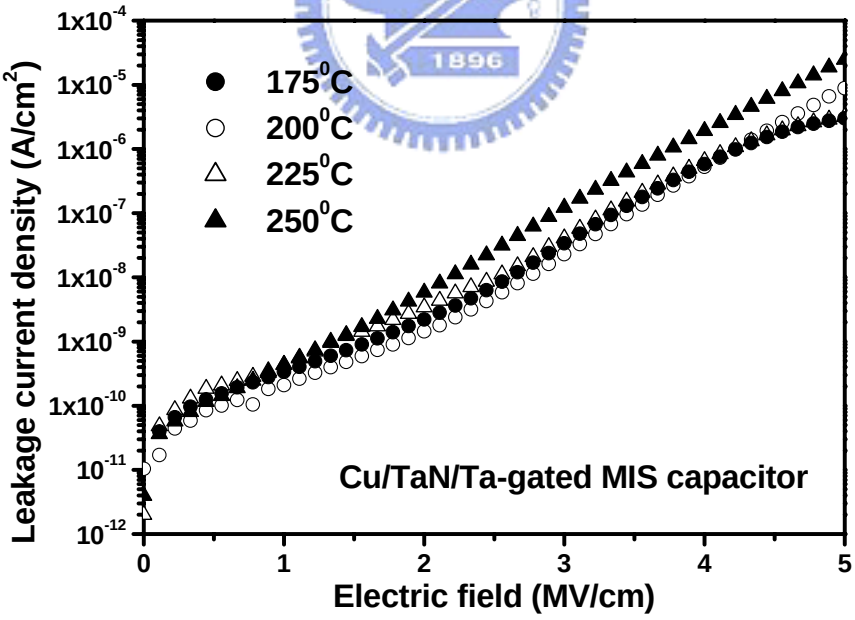


Figure 4.11 Arrhenius plot of estimated drift mobility of Cu^+ ions in the SiOC:H dielectrics versus *1000/T*.



(a)



(b)

Figure 4.12 Leakage current density-electric filed characteristics of (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors at various temperatures.

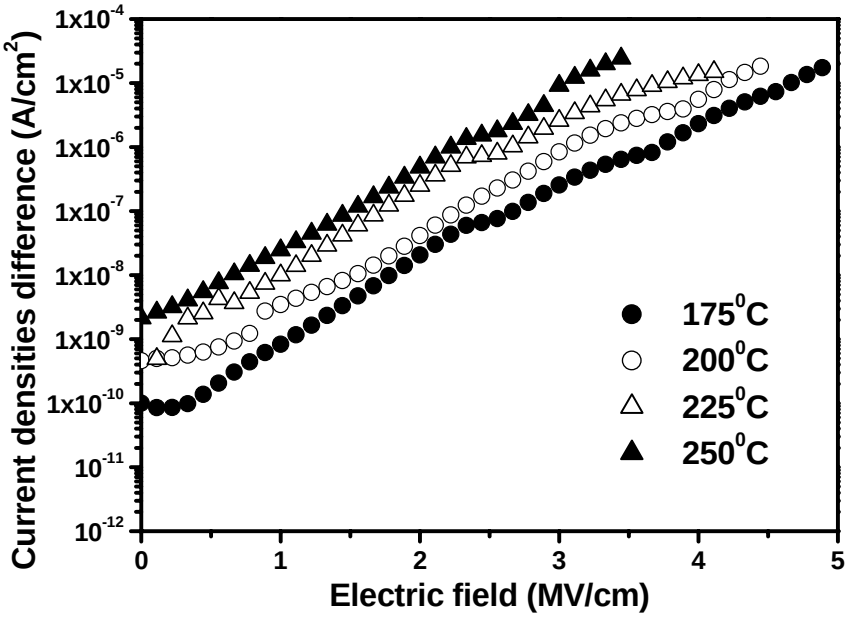


Figure 4.13 Leakage current densities difference J_{diff} of Cu-gated and Cu/TaN/Ta-gated MIS capacitors at various temperatures.

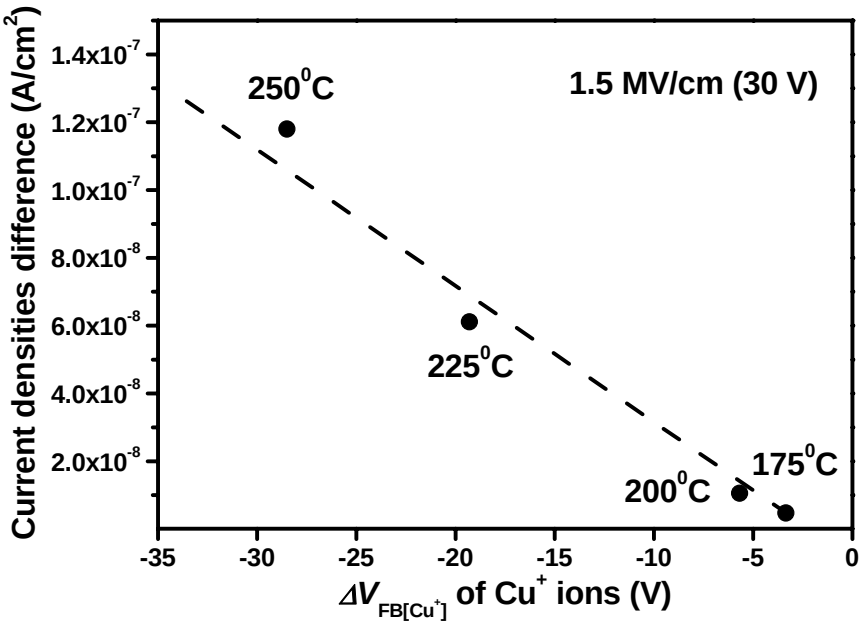
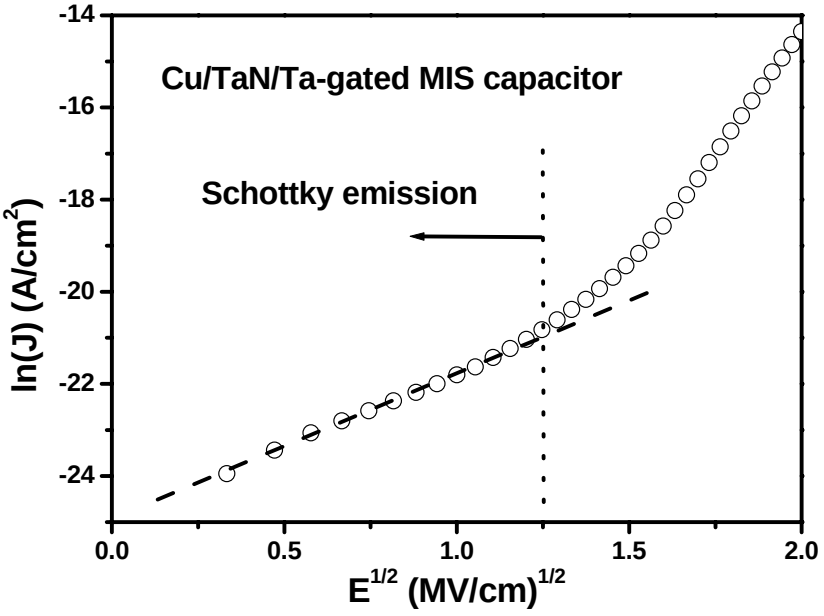
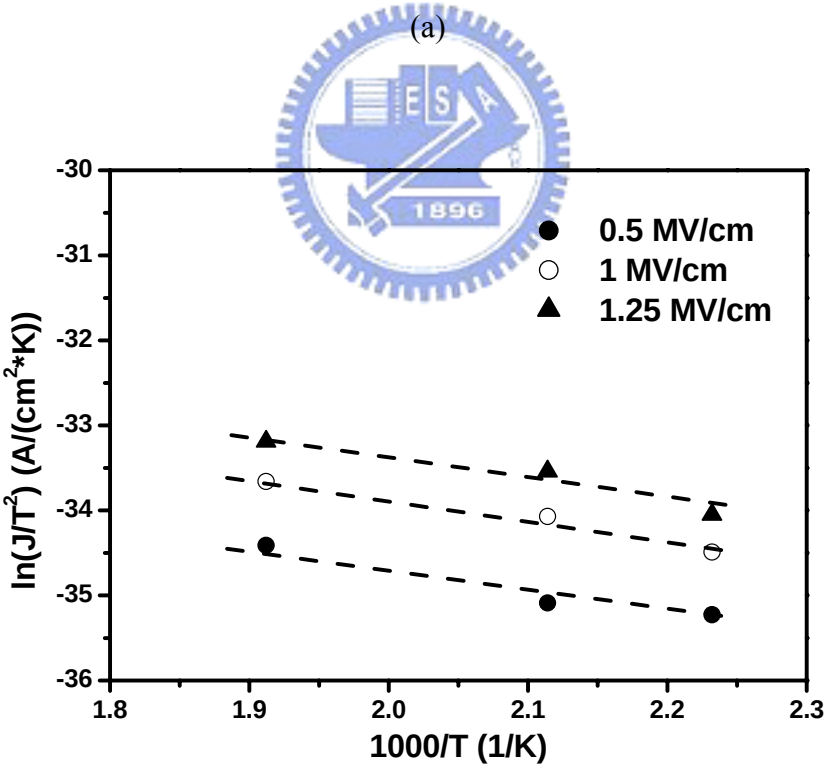


Figure 4.14 Leakage current densities difference J_{diff} of Cu-gated and Cu/TaN/Ta-gated MIS capacitors at 1.5 MV/cm (30V) versus $\Delta V_{FB[Cu^+]}$ of Cu^+ ions after 40 min at 30V BTS at various temperatures.

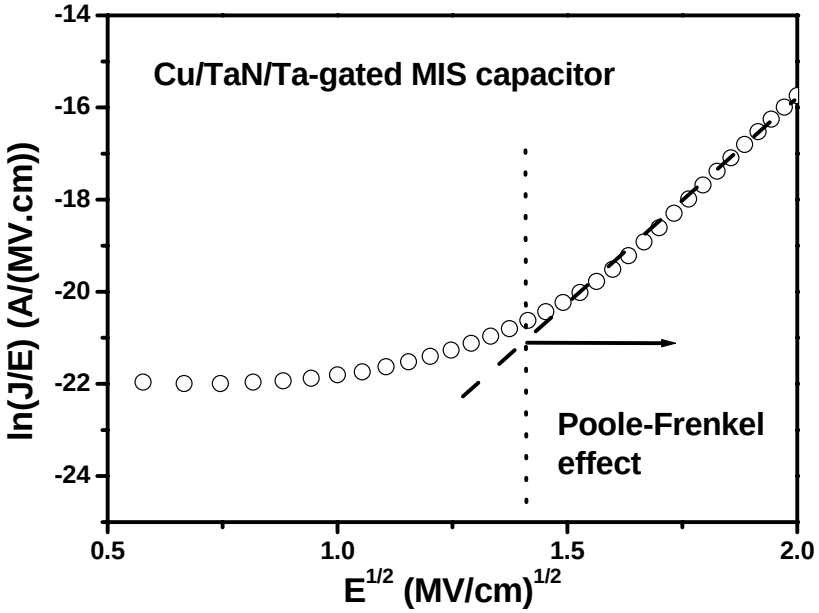


(a)

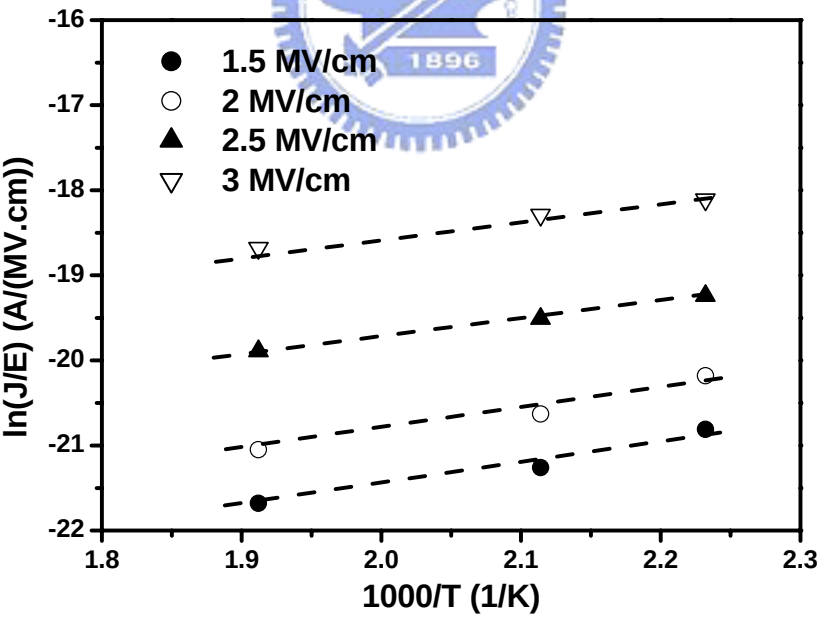


(b)

Figure 4.15 (a) ln(J) versus $E^{1/2}$, and (b) ln(J/T^2) versus 1000/T for Cu/TaN/Ta-gated MIS capacitors at various measured temperatures in electrical field E<1.25 MV/cm.



(a)



(b)

Figure 4.16 (a) ln(*J*/*E*) versus $E^{1/2}$, and (b) ln(*J*/*E*) versus 1000/*T* for Cu/TaN/Ta-gated MIS capacitors at various measurement temperatures in electrical field *E*>1.5 MV/cm.

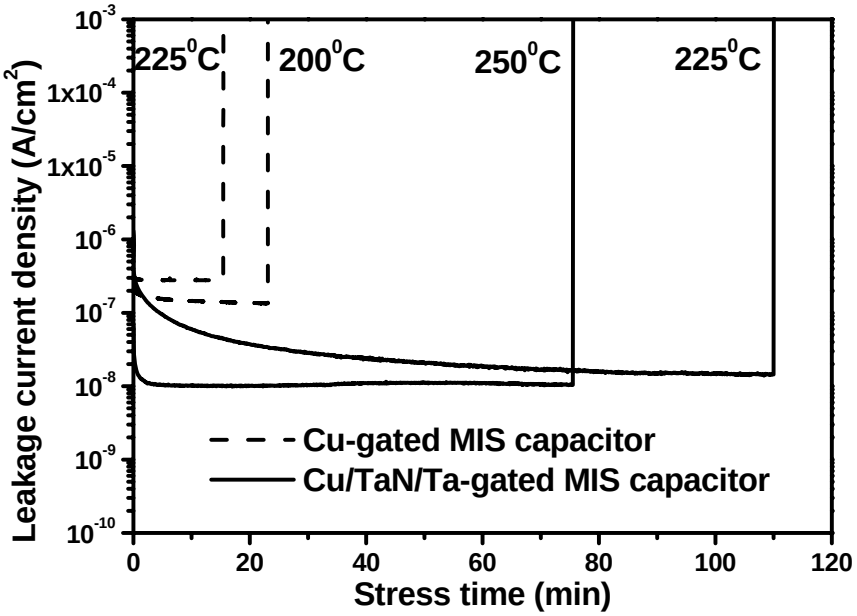
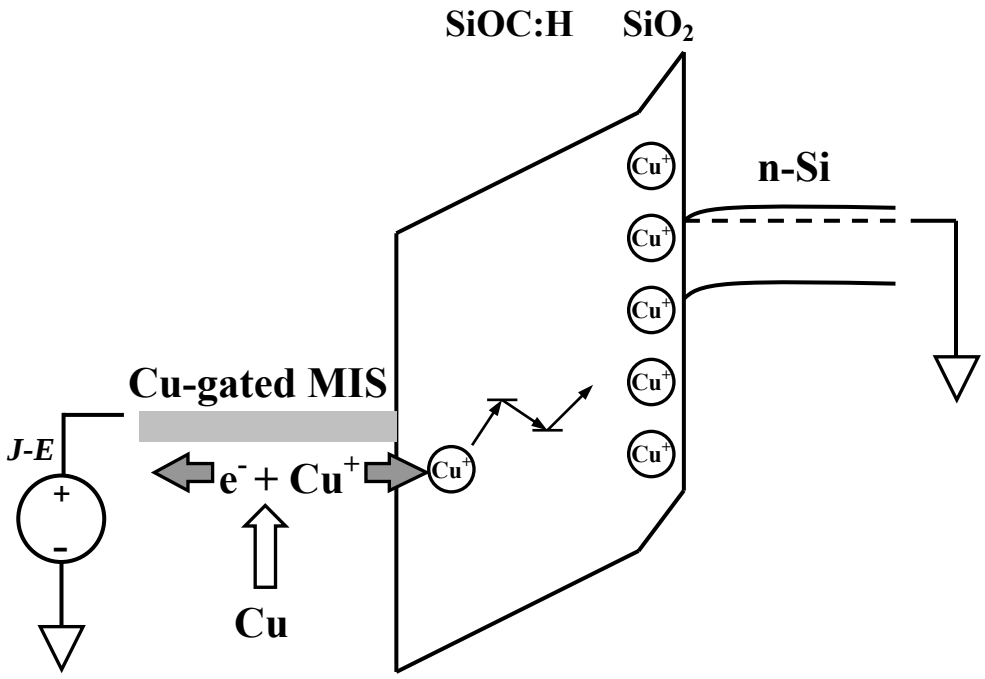
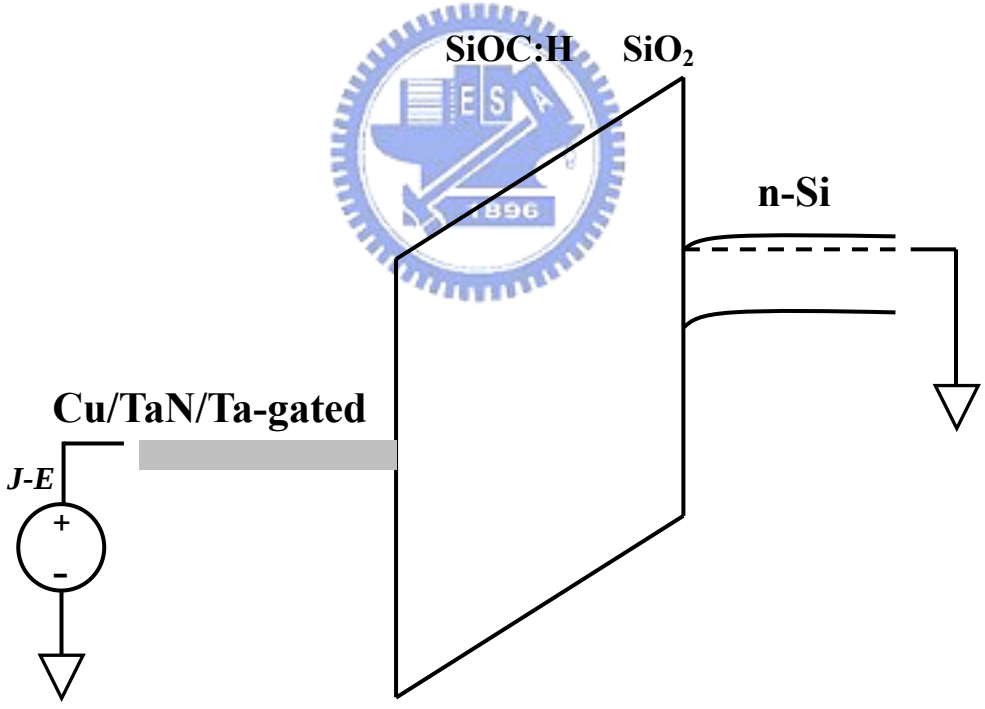


Figure 4.17 Current-time characteristics of the Cu-gated and Cu/TaN/Ta-gate MIS capacitors in the electric field of 2.5 MV/cm at various temperatures.



(a)



(b)

Figure 4.18 Schematic band diagram of injection of Cu^+ ions in (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors under positive gate bias.

Chapter 5

Effects of Plasma Treatment on the Performance of W-based Diffusion Barrier Layers for Cu Interconnection

5.1 Introduction

In microelectronic devices, the critical feature sizes of integrated circuits have been greatly reduced to improve packing density. Cu has been used as an on-chip interconnection in microelectronic devices recently due to its lower electrical resistivity and better electromigration resistance compared to aluminum [1,2]. However, for the application of Cu metallization, the interaction between Si and Cu is very severe and will degrade electrical performance of the device even at temperatures as low as 200°C [3,4]. A barrier layer is needed to prevent the copper diffusion. Refractory metals and their nitrides had been investigated for such application. Among several metal nitrides, tungsten nitride (WN_x) is a commonly used material in integrated-circuit (IC) technologies because of its refractory nature and high thermal stability [5,6]. Furthermore, tungsten nitride is promising compared to tantalum or other barriers due to excellent chemical mechanical polishing (CMP) process compatibility [7]. However, the dominant failure of the sputtered WN_x barrier is attributed to diffusion via fast diffusion paths in grain boundaries [8,9]. Copper and silicon interdiffuse through the grain boundaries of the WN_x barrier during annealing at elevated temperature, resulting in degraded electrical characteristics, and ultimately, in device failure.

5.1.1 Influence of N_2O Plasma Treatment on WN_x Barriers

One method used to retard Cu penetration involves intentionally contaminating the barrier with either nitrogen or oxygen. Theoretically, these impurities would physically block the fast diffusion paths, or chemically react with Cu to enhance the barrier properties. Another method to avoid fast diffusion paths along grain boundaries is to change the microstructure of the barrier from a crystalline to an amorphous structure [10-13]. In this research, reactively sputtered WN_x barriers were used as the diffusion barriers for Cu metallization. The effects of nitrogen flow ratio during sputtering were investigated. Barrier performance of the WN_x layer can be improved by changing microstructure and stuffing grain boundaries with N_2O plasma treatment. We found that N_2O plasma treatment exhibits nitridation and oxidation of the WN_x barrier and results in an amorphous surface layer. But this treatment also stuffs nitrogen and oxygen atoms into grain boundaries of WN_x barriers.

5.1.2 Analysis of Cu Diffusion in Plasma-treated Tungsten Barrier

tungsten nitride (WN) has received the most attention owing to its high thermal stability and excellent chemical mechanical polishing (CMP) process compatibility [7]. However, resistivity of tungsten nitride film is higher than that of tungsten film. As the technology node moves to 130 nm and below, a barrier layer with low resistivity is necessary to lower the resistance of the total line interconnect and/or via.

Most of refractory metal films used as diffusion barriers in Cu metallization are polycrystalline rather than monocrystalline. Moreover, columnar grain structure is frequently found in sputtered refractory metal and metal nitride films [14-16]. In general, atomic diffusion along grain boundaries is much faster than in the bulk of

grains. Grain boundaries may presumably serve as fast diffusion paths for copper. Coupled lattice and grain boundary diffusion is different from lattice diffusion. Whipple had given formulae for the concentration in a semi-infinite region of low diffusion coefficient bisected by a thin well-diffusing slab [17,18]. This is of interest in grain boundary diffusion.

In this study, a method of forming nitrogen and oxygen incorporated W films with low resistivity was investigated. N_2O plasma was used to post-treat the W diffusion barrier. The effectiveness of as-deposited and N_2O plasma treated W films as diffusion barriers between Cu and Si was evaluated. A composite diffusion barrier was formed after N_2O plasma treatment. Cu diffusion in the N_2O plasma treated W barrier was further analyzed by numerical calculation using Whipple's and Fick's models.

5.2 Device Fabrication and Characteristics Measurement

5.2.1 Plasma-treatment on WN_x Barrier Layer

Single-crystal, (100)-orientated silicon wafers were used in this study. WN_x films were deposited onto Si substrates by reactive sputtering of the W target after the substrates were cleaned in a dilute HF solution. The sputtering chamber was evacuated to a pressure less than 6×10^{-7} torr, and sputtering pressure was 6×10^{-3} torr during deposition. Deposition was carried out at room temperature without intentional heating. WN_x films of 50-nm thickness were sputtered at D.C. power of 1000 W under nitrogen flow ratio $N_2/(Ar+N_2)$ of 10, 15, 20, or 30%. Some WN_x films received N_2O plasma post-treatments in a plasma-enhanced chemical vapor deposition (PECVD) system. The power and pressure were 200 W and 100 mtorr, respectively, for N_2O plasma post-treatment. For easy identification, the WN_x film sputtered at a nitrogen flow ratio of a% and N_2O plasma-treated WN_x film were denoted as WN_x(a%) and $WN_x(N_2O)$, respectively, in the work. Subsequently, the Cu film with thickness of 300 nm was sputtered onto the WN_x barrier. The $Cu/WN_x/Si$ samples were annealed at 550° to 750°C in N_2 ambient for 30 min to investigate thermal stability.

5.2.2 Plasma-treatment on W Barrier Layer

Single crystal, (100) orientated silicon wafers were used in this study. Tungsten films of 50 nm were deposited at a power of 1000 W by sputtering. Films were sputtered at room temperature without intentional heating and base pressure was less than 6×10^{-7} Torr. The wafers further received N_2O plasma treatment in a plasma enhanced

chemical vapor deposition (PECVD) system after W films were deposited. The power and pressure of N_2O plasma treatment were 200 W and 100 mTorr respectively. Some wafers were treated by N_2 or NH_3 plasma for comparison. For easy identification, the untreated, N_2O, N_2, and NH_3 plasma-treated W films were denoted as W, W(N_2O), W(N_2), and W(NH_3) barriers in the work. Copper films, 300 nm thick, were deposited on top of the barrier layers by sputtering.

5.2.3 Characteristics Measurement

Film thickness was measured by a stylus surface profiler and scanning electron microscopy (SEM). Transmission electron microscopy (TEM) and X-ray diffraction (XRD) were used to determine microstructure and crystalline orientation of the film. Rutherford backscattering spectroscopy (RBS) was used to determine the composition and density of the WN_x film. X-ray photoemission spectroscopy (XPS) was used to study the bonding structures and chemical binding energies. A four-point probe system was employed to measure sheet resistance. Compositional depth profiles after annealing were analyzed by Auger electron microscopy (AES).

The failure of the WN_x barrier between Cu and Si was determined by leakage current of the n^+-p junction diode. The local oxidation of silicon (LOCOS) process was applied to the wafer to define active regions after cleaning. The n^+-p junctions were formed by As^+ implantation at 60 keV with a dose of $5x10^{15}$ cm^{-2}, followed by rapid thermal annealing (RTA) at 1050°C for 30 s in N_2 ambient. The WN_x film was etched using $CF_4/CHF_3/O_2$ plasma after copper patterns were etched by a diluted HNO_3 solution. Leakage currents of the diodes were measured at a reverse bias of 5 V by a HP4145B semiconductor parameter analyzer after annealing at various temperatures for 30 min.

5.3 Results and Discussion

5.3.1 Influence of N_2O Plasma Treatment on Microstructure and Thermal Stability of WN_x Barriers for Cu Interconnection

Table 5.1 is the summary of properties of WN_x barriers sputtered at various nitrogen flow ratios. The nitrogen concentration of WN_x film increases as the nitrogen flow ratio increases from 10% to 30%. The corresponding nitrogen content of WN_x films increases from 25 to 38 at. % from RBS analyses. The deposition rate of WN_x film decreases with increasing nitrogen flow ratio. The decreasing deposition rate at high nitrogen flow ratio is attributed to the sputtering yield of nitrogen being lower than that of argon. The effective sputtering yield decreases with decreasing argon flow ratio, and hence, the deposition rate decreases, as listed in **Table 5.1**. **Figure 5.1** displays a cross-sectional TEM image of a reactively sputtered WN_x(20%) film. Columnar grains are observed, as shown in **Fig. 5.1**. The columns may develop via a surface diffusion process influenced by both geometrical shadowing effects and limited atomic mobility [19,20]. The grain size of sputtered WN_x film decreases with increasing nitrogen content, as indicated in **Table 5.1**. The decreasing grain size can be explained in terms of nitrogen enrichment at the grain surface, which prevents further growth, and hence, contributes to finer grains and the decrease of surface roughness, as shown in **Table 5.1**. Moreover, as the nitrogen flow ratio increases, the resistivity increases because numerous of disorder regions and vacancies occur among the WN_x grains and grain boundaries. Furthermore, it is reported that impurities (nitrogen or oxygen) in the films are responsible for the intrinsic compressive stress [21]. In the study, a decrease of tensile stress is observed as the nitrogen concentration of WN_x film increases.

Figure 5.2(a) displays the variation percentage in sheet resistance of the Cu/WN_x/Si sample after furnace annealing at various temperatures. The variation percentage in sheet resistance is defined as the ratio of ($R-R_0$) to R_0, in which R_0 and R denote the sheet resistance of as-deposited and annealed samples, respectively. The results reflect the interactions between Cu and Si indirectly. The sheet resistance initially decreases gradually with increasing annealing temperature due to the reduction of crystal defects and grain growth of the Cu film. But sheet resistance increases at a certain temperature because of failure of the diffusion layer, which results in the reaction of Cu or WN_x barrier with the silicon substrate and formation of compounds. **Figure 5.2(b)** shows XRD patterns of the samples with the WN_x barriers deposited at various nitrogen flow ratios after annealing at 675°C for 30 min. From XRD analyses, no compound is found for the Cu/WN_x(30%)/Si system after annealing at 675°C. In contrast, an inferior barrier performance is observed for the WN_x barrier deposited at a lower nitrogen flow ratio because sheet resistance starts to increase and W_5Si_3 compounds are found. In addition, the nanostructured W_2N (111) and b.c.c. W (100) grains are observed in nitrogen-rich WN_x(20%-30%) barriers. It is reported that WN_x films transferred into a two-phase mixture of W and W_2N between 600° and 700°C, and the mixture of W and W_2N plays an important role in preventing Cu diffusion even after crystallization [22]. **Figure 5.2(b)** also shows that the peak of the b.c.c. W (100) reflection line in WN_x(10%) film is very sharp compared to that in WN_x(30%) film, and the peak of W_2N (111) is not observed. The partially incorporated nitrogen will release from the WN_x(10%) barrier during annealing at high temperature, and hence, the nitrogen-stuffing effects in the WN_x grain are eliminated, and coarse b.c.c. W grains develop in the nitrogen-deficient WN_x(10%) barrier.

Figures 5.3(a) and **(b)** illustrate the statistical distributions of leakage current

densities measured at a reverse bias of 5 V for the Cu/WN_x/n^+-p junction diodes annealed at 500° and 600°C, and at least 30 diodes are measured in each case. The leakage current densities of all the samples are below 1.0×10^{-8} A/cm^2 before annealing. Almost all Cu/WN_x(30%)/n^+-p junction diodes retain low leakage current densities after annealing at 500°C for 30 min. Furthermore, the leakage current densities are less than 10^{-7} A/cm^2 for most junction diodes with the WN_x(30%) barriers after annealing at 600°C for 30 min. In contrast, high leakage current densities above 10^{-7} A/cm^2 are found for diodes with low-nitrogen-incorporated WN_x barriers after annealing at 600°C. Although WN_x and Cu do not form compounds, the diffusion of a small amount of copper through the grain boundaries or defects in the WN_x barriers into the Si junction region may cause the severe failure of the shallow junction. As shown in XRD results of **Fig. 5.2(b)**, coarse b.c.c. W grains are formed in the WN_x(10%) barrier at 675°C, and opened grain boundaries can significantly degrade the barrier due to formation of fast diffusion paths. On the other hand, the increasing nitrogen incorporation leads to microstructural change, which can reduce the fast diffusion paths of the barrier.

To improve the barrier effectiveness of the WN_x layer, N_2O plasma treatment is applied to treat the WN_x(15%) barrier in this work. XPS analysis was carried out to identify the chemical bonding states of barriers. **Figures 5.4**, **5.5**, and **5.6** show W 4f, O 1s, and N 1s XPS spectra, respectively, of WN_x(15%) and $WN_x(N_2O)$ barriers. The W 4f peaks can be well resolved into many peaks by curve fitting, as shown in **Fig. 5.4**. Curves 1, 2, and 3 are the separated curves of the XPS superimposition spectrum. The main binding energies of the W $4f_{7/2}$ and W $4f_{5/2}$ electrons of WN_x and $WN_x(N_2O)$ barriers, resolved as curve 1 in the W 4f spectra, are 31.8 and 34.2 eV, respectively. These values are consistent with the peaks of metal tungsten [23]. The W $4f_{7/2}$ and W $4f_{5/2}$ peaks of curve 2 are 33.7 and 35.9 eV. These peaks are associated with the peaks

of WN_x [23]. Two other peaks at high binding energies of 35.5 and 37.5 eV, resolved as curve 3 in **Fig. 5.4(b)**, are found for the $WN_x(N_2O)$ barrier. The peaks correspond to binding energies of tungsten oxide and are attributed to oxidation during N_2O plasma treatment. There is almost no peak in the O 1s spectrum of the WN_x(15%) barrier, as shown in **Fig. 5.5(a)**. However, two peaks at around 530.9 and 532.9 eV are found in the O 1s spectrum of the $WN_x(N_2O)$ barrier, as shown in **Fig. 5.5(b)**. The low-energy peak at 530.9 eV corresponds to the O^{2-} ion of WO_3, and the major peak at 532.9 eV is identical to the O 1s peak of the O^{2-} ion of other combination states of WO_x [24]. This means that the oxidation occurs during N_2O plasma treatment. The major peak centered at 397 eV, as shown in the N 1s spectra of **Fig. 5.6**, is consistent with the N 1s binding energy of a nitride compound. Another peak at a higher binding energy of ~400 eV is attributed to the N atoms or molecules present in grain boundaries of WN_x [13,25,26]. The relative intensity of the peak at ~400 eV in the $WN_x(N_2O)$ barrier is much higher than that in the WN_x(15%) barrier, as shown in **Fig. 5.6**. It could be explained that most of the introduced nitrogen atoms are likely present at the grain boundaries during N_2O plasma treatment. Hence, N_2O plasma treatment enhances nitrogen atoms to stuff into the grain boundaries to block diffusion paths.

To further clarify the structure and identify possible surface reactions of the WN_x and $WN_x(N_2O)$ barriers, plan-view TEM analysis was used to analyze the microstructure. Both the bright-field plan-view images and the selected-area diffraction (SAD) patterns of the WN_x and $WN_x(N_2O)$ barriers are shown in **Fig. 5.7**. The $WN_x(N_2O)$ barrier is composed of finer grains compared to the WN_x barrier. The SAD shows that the $WN_x(N_2O)$ barrier has clear board halos, instead of diffusion spots, indicating that the N_2O plasma treatment causes the formation of an amorphous layer on the WN_x barrier.

Figure 5.8(a) shows the variation percentage in sheet resistance of the

Cu/barrier/Si sample after furnace annealing at various temperatures. Sheet resistance of the Cu/$WN_x(N_2O)$/Si system only increases around 20%, even after annealing at 750°C. However, after annealing at temperatures of 600°~700°C, the sheet resistances of Cu-contacted systems with other barriers (WN_x, WC_x [27], TiC_x [28], PVD TaN [29], and CVD TaN [29]) sharply increase (≥100%), indicating that a considerable amount of Cu has already diffused through the barrier layers and reacted with Si substrates, thus resulting in Cu_3Si or barrier-Si compounds and the deterioration of the conductivity of the contact systems. Further evidence is given by XRD results, as shown in **Fig. 5.8(b)**: formation of Cu_3Si compounds is observed in the Cu/WN_x/Si system after annealing at 700°C for 30 min. Cu_3Si compounds are not found in the system with the $WN_x(N_2O)$ barrier. According to XPS and TEM results, the nitridation and oxidation of the WN_x barrier is controlled by the mobility of the nitrogen- and oxygen-based adatoms on the WN_x surface during the N_2O plasma treatment. This can be understood by the fact that nitrogen- and oxygen-based adatoms can act as a roadblock to the WN_x or serve as nucleation sites for defects. Therefore, the WN_x grains may not have sufficient mobility to migrate to the preferred sites for crystallization growth during thermal annealing. Compared to previous research, the failure temperature (variation percentage > 50%) of the $WN_x(N_2O)$ barrier is greater than 750°C and is superior to WC_x(~650°C) [27], TiC_x(~625°C) [28], and TaN(~650°C) [29]. **Figure 5.9** displays the AES depth profiles of the Cu/WN_x/Si and Cu/$WN_x(N_2O)$/Si systems after annealing at 675°C. Some copper diffuses through the WN_x layer into the Si substrate for the Cu/WN_x/Si system. Copper diffusion is limited, and a copper signal is not found for the Cu/$WN_x(N_2O)$/Si system.

Figures 5.10(a) and **(b)** indicate statistical distributions of reverse-biased leakage current densities measured at 5 V for Cu/barrier/Si junction diodes after

annealing at 500° and 600°C. The leakage current densities are less than 10^{-8} A/cm^2 before annealing. Leakage current densities of diodes with 50-nm $WN_x(N_2O)$ barriers are significantly lower than those with WN_x(50 nm), WC_x(50 nm) [27], TiC_x(50 nm) [28], or TaN(60 nm) [29] barriers after annealing at 500°C. After 600°C annealing, the leakage current densities of almost all diodes with WN_x, WC_x, TiC_x, or TaN barriers are higher than 10^{-7} A/cm^2. In contrast, diodes with $WN_x(N_2O)$ barriers retain low leakage current densities, and leakage current densities are less than 10^{-8} A/cm^2. It is obvious that N_2O plasma treatment will improve barrier performance effectively because it could impede Cu to diffuse into Si substrate. Effects of N_2O plasma treatment on WN_x barrier are summarized as following. The nitrogen- and oxygen-based radicals and ions are produced in the PECVD system, and they result in nitridation and oxidation on the surface of WN_x barriers. The nitrogen atoms form covalent or ionic bonds with the tungsten to be tungsten nitrides. But excessive nitrogen atoms also stuff WN_x grain boundaries and block the rapid diffusion paths for Cu and Si atoms. On the other hand, the oxygen-based radicals or ions will react with tungsten nitride to form compounds of tungsten oxides (WO_3 and WO_x). These effects contribute to improve the effectiveness of the tungsten nitride diffusion barrier.

5.3.2 Numerical and Experimental Analysis of Cu Diffusion in Plasma-treated Tungsten Barrier

To investigate the effects of N_2O plasma treatment on W barrier, chemical bonding states of barrier were analyzed by XPS. **Figures 5.11(a)**, **(b)**, and **(c)** show the W 4f, O 1s, and N 1s spectra of as-deposited and N_2O plasma-treated W barriers. The W $4f_{7/2}$ and W $4f_{5/2}$ peaks are situated at the same position (31.2, 33.4 eV) for two barriers, and the two peaks are characteristics of the W itself [23]. However, two another peaks at binding energies 36.16 and 38.43 eV are observed for the W(N_2O) barrier. The peaks correspond to binding energies of tungsten oxide and are attributed to oxidation during N_2O plasma treatment. The O 1s spectrum of the W(N_2O) barrier exhibits a strong and broad peak centered at around 531.2 eV, as shown in **Fig. 5.11(b)**. There is almost no peak in untreated W barrier. W-O phases are believed to form on the surface of W(N_2O) barrier. The N 1s peak of the W(N_2O) barrier can be well resolved into two peaks by curve fitting compared to no peak in the N 1s spectrum of the W barrier, as shown in **Fig. 5.11(c)**. These two peaks are centered at 397.5 and 399.25 eV. The weak peak centered at 397.5 eV is consistent with the N 1s binding energy of nitride compound and is also reported by previous research [25]. Another strong peak at ~399.25 eV is observed in N 1s spectrum and attributed to the N atoms or molecules present in grain boundaries of W [13,14,30]. It indicates that some N atoms do not form strong covalent or ionic bonds with W during N_2O plasma treatment.

Figure 5.12(a) displays cross-sectional bright field TEM micrograph of as-sputtered W film. Columnar grain structure is observed. Cu diffusion in columnar grains is believed to be relatively easy because columnar grains will provide fast diffusion paths for Cu diffusion. **Figures 5.12(b)** and **(c)** display plane-view TEM

images and selected area diffraction (SAD) patterns of W and W(N_2O) barriers. Several sharp ring is observed for untreated W film. It indicates that the as-deposited W film is a polycrystalline structure. The grain size of as-deposited W film is 20-40 nm, as shown in **Fig. 5.12(b)**. The W(N_2O) barrier has a diffused ring pattern instead of diffraction spots, indicating that the N_2O plasma treatment causes an amorphous surface layer upon W film. Grain size of the W(N_2O) barrier is only 2-5 nm. It indicates that a surface layer with finer grains is formed due to the reactions and bombardments of energetic radicals and ions during plasma treatment. It is reported that the nanostructured amorphous diffusion barrier, defined as a very short-range order single crystal, is highly attractive due to its relatively thermal stability and its relatively higher resistance against Cu diffusion [33].

Figure 5.13 displays resistivity and root-mean-square (RMS) surface roughness of plasma treated W film as a function of plasma treatment time. Surface roughness reduces apparently after plasma treatment, as shown in **Fig. 5.13**. Plasma treatment could sputter the barriers and make them smooth. Sputtering and stuffing effects are believed to occur due to the reactions or bombardments of energetic radicals and ions during plasma treatment. Resistivity increases with increasing plasma treatment time. It is expected that resistivity of W with plasma treatment would increase because a high-resistivity surface layer is formed and thus the effective thickness of the W film with low resistivity reduces. Resistivity of W(N_2O) barrier is higher than those of the W(N_2) and W(NH_3) barriers. High resistivity may be due to the formation of high-resistance W-O compounds in W(N_2O) barrier, as indicated in XPS analyses. However, the resistivity of W(N_2O) (~24 μΩ cm) barrier is still much lower than that of the reactively sputtered WN film (150~200 μΩ cm) [14].

Table 5.2 summarizes the properties of W, WN and W(N_2O) barriers. **Table 5.2** also lists properties of sputtered Ta and Ti films in literatures [13,31,32,34] for

comparison. The resistivities of sputtered W and W(N_2O) barriers are about 20 and 24 μΩ cm, respectively. The resistivities are very close and much lower than that of the reactively sputtered WN (150-200 μΩ cm) [14], Ta (~160 μΩ cm) [13,31], and Ti (~70 μΩ cm) [34]. Moreover, it is reported that electroplating of Cu layer is difficult on seed layers with rough surface [35]. Surface roughness could be reduced from 2.5 to 0.5 nm by N_2O plasma treatment, as listed in **Table 5.2**. Grain size is calculated from plane-view TEM. The as-deposited W film is columnar grain structure with a grain size of 20-40 nm and grain size of the W(N_2O) barrier is only 2-5 nm. It indicates that nanocrystallization effect would occur due to the reactions and bombardments of energetic radicals and ions during N_2O plasma treatment. Furthermore, it is reported that the impurities (nitrogen or oxygen) in the films are responsible for the intrinsic compressive stress [21]. In this research, the tensile stress decreases from 1.9×10^{10} to 1.4×10^{9} dynes/cm^2 as N_2O plasma treatment is applied to W film, as listed in **Table 5.2**. N_2O plasma treatment also enhances the adhesion between Cu and W(N_2O) barrier. The adhesion strength of Cu on W(N_2O) barrier (50-58 Mdynes/cm^2) is better than untreated W (30-35 Mdynes/cm^2) and other barriers such as Ta and Ti [32]. It is suggested that O or N species on the barrier surface can react with Cu to form more stable interface and thus promote adhesion after N_2O plasma treatment.

Figure 5.14(a) shows the variation percentage of the Cu/barrier/Si system after furnace annealing at various temperatures. The variation in sheet resistance is defined as the ratio of ($R-R_0$) to R_0, in which R_0 and R denote the sheet resistance of as-deposited and annealed samples. The results reflect the interactions between Cu and Si indirectly. Resistance increases rapidly at certain temperature because of failure of the diffusion layer and formation of compounds. Sheet resistance of Cu/W(N_2O)/Si increases slightly even after annealing at 750°C. However, sheet

resistances of samples with other barriers (W, WN [14], WC_x [27], TiC_x [28], and TaN [29]) sharply increase after annealing at 600-700°C, indicating that a considerable amount of Cu has already diffused through the barrier layers and resulted in Cu_3Si compounds, and thus strongly deteriorated the conductivity of the contact system. X-ray diffraction technique is further used to detect the structural change in the annealed samples. **Figure 5.14(b)** shows XRD patterns of Cu/W/Si and Cu/W(N_2O)/Si systems after annealing at 700°C for 30 min. Peaks of Cu_3Si compounds are observed for W barrier and the resulting XRD pattern is consistent with variation in sheet resistance. There is no Cu_3Si peak in W(N_2O) barrier system, indicating that W(N_2O) has an excellent barrier performance. It is noted that there is no Cu-W compound in the XRD spectra, and similar results are found for WN barriers [14]. The failure of W and WN barriers is attributed that Cu atoms diffuse through defects and grain boundaries of the barrier without reacting with the WN and W film. Failure temperature (variation percentage > 50%) of W(N_2O) barrier is higher than 750°C and superiors to sputtered WC_x(~650°C) [27], TiC_x(~625°C) [28], and TaN(~650°C) [29] barriers.

Barrier performance is also evaluated by the leakage current density of the junction diode. **Figure 5.15** illustrates the statistical distributions of leakage current densities of Cu/barrier/n^+-p junction diodes measured at reverse bias of 5 V after annealing at 500 and 600°C. The leakage current densities of all diodes are below 10^{-8} A/cm^2 before annealing. Most diodes with sputtered W, WN [14], WC_x [27] and TiC_x [28] barriers have leakage current densities higher than 1×10^{-7} A/cm^2 after annealing at 500°C for 30 min. Diodes with W(N_2O) barriers retain leakage current densities less than 10^{-8} A/cm^2 after annealing at 500°C. Moreover, most diodes with W(N_2O) barriers retain leakage current densities less than 10^{-8} A/cm^2 even after annealing at 600°C. W(N_2O) show an excellent barrier capability against Cu diffusion compared to

W, WN [14], WC_x [27], TiC_x [28] and TaN [29], as shown in **Fig 5.15**.

Although barrier performance of the W film is significantly improved by N_2O plasma treatment, similar plasma treatments, e.g., N_2 plasma treatment, had been proposed to enhance barrier performance in previous researches [13,30]. W barriers are also treated by N_2 or NH_3 plasma for comparison in the work. **Figure 5.16** exhibits statistical distributions of leakage current densities of Cu/W(N_2O)/n^+-p, Cu/W(N_2)/n^+-p and Cu/W(NH_3)/n^+-p diodes after annealing at 500 and 600°C. All W(N_2O), W(N_2), and W(NH_3) show an enhanced barrier performance compared to untreated W. Moreover, N_2O plasma treatment has a better barrier improvement than N_2 plasma treatment and N_2 plasma is more effective than NH_3 plasma. It is found that some diodes have leakage current densities higher than 1×10^{-7} A/cm^2 for W(NH_3) barriers after annealing at 500°C. Most diodes with W(N_2O) barriers retain leakage current densities less than 1×10^{-8} A/cm^2 and large leakage current densities in range of 10^{-7} to 10^{-4} are found for Cu/W(N_2)/n^+-p and Cu/W(NH_3)/n^+-p diodes after annealing at 600°C. Enhancing performance of the W(N_2O) barrier is attributed to combined effects of nitridation and oxidation during N_2O plasma treatment. N_2O is a strong oxidizing agent and energetic oxygen radicals and atoms are more easily produced by dissociation of N_2O. In contrast, it is less effective to dissociate triple bonds of nitrogen as nitrogen plasma is used to post-treat W barrier. The bond strengths of N-O and N-N are 630.57 and 945.33 kJ/mol. Energetic oxygen radicals and atoms are helpful in formation of an oxygen stuffed layer on the columnar-grained W barrier. It will act as a more efficient barrier against the Cu diffusion. N_2 plasma treatment doesn't induce oxygen stuffed layer on surface of the W barrier and nitrogen radicals and atoms are limited for nitridation and stuffing compared to N_2O plasma treatment. Bond strength of N-H is 339 kJ/mol for NH_3 plasma treatment. Although nitridation is expected to occur greatly, no plasma oxidation on W surface occurs and lots of atomic

hydrogen will diffuse into the grain boundaries of W due to effective dissociation of NH_3. Hydrogen will out-diffuse from grain boundaries of plasma-treated W after annealing at a certain temperature, lead to defect sites or carrier trapping sites, and hence, decrease its resistance to copper penetration.

Barrier capabilities are further investigated by evaluating Cu diffusion in W and W(N_2O) barriers. The diffusion of Cu in the temperature range of 600-700°C is evaluated by SIMS and the penetration depth profiles of specimens are indicated in **Fig. 5.17**. Relatively low Cu penetration into the W(N_2O) barrier is detected compared to sputtered W barrier. Since the mixing enthalpy of Cu solute in W is large (8.0×10^4 j/mol), Cu atoms do not intermix with W at high temperature [36,37]. As far as we know, it is relatively difficult for Cu penetration into W barrier by lattice diffusion. However, the diffusion coefficients of Cu in grain boundaries of W barrier are still unknown, though the rough estimation has been discussed [38], and the results are still needed to be further discussed.

Whipple had given formulae for the concentration in a semi-infinite region of low diffusion coefficient bisected by a thin well-diffusing slab. Since our source condition is close to infinite one, the Whipple's solution is used for profile analysis [17]. The key result of Whipple's solution is

$$D_B\delta = 0.661\left(-\frac{\partial \ln(\overline{C})}{\partial y^{\frac{6}{5}}}\right)^{-\frac{5}{3}}\left(\frac{4D_L}{t}\right)^{\frac{1}{2}}, \qquad (5.1)$$

where $\overline{C} = C/C_s$ in a section at a depth y μm from the original surface, C_s is the surface concentration, t is the annealing time, and δ is the grain boundary width. D_L and D_B present the diffusion coefficients in the lattice and the grain boundary. **Figure 5.18** displays the concentration profiles obtained from diffusion of Cu in W barriers at

various temperatures in the standard coordinates $\ln\overline{C}$ vs. $y^{\frac{6}{5}}$. Based on Eq. 5.1 and provided that D_L is known, δD_B can be determined by measuring the slope from the linear region in the $\ln\overline{C}$ vs. $y^{\frac{6}{5}}$ plots. The value of D_L can be found from the initial part of the concentration profile. Under the assumptions of a semi-infinite system and constant source at the surface, the boundary conditions applied to solve Fick's diffusion equation are

$C = C_s, \quad y < 0, \quad t = 0$ (5.2a)

$C = 0, \quad y > 0, \quad t = 0$ (5.2b)

An error function solution can be expressed by the equation

$$C(y,t) = C_s \,\mathrm{erfc}\left(\frac{y}{2\sqrt{D_L t}}\right) \tag{5.3}$$

where the error function was fitted to the initial part of the concentration profiles and extrapolated to zero thickness $y = 0$ in the case of subtracting the grain boundary contribution. The results are shown in **Table 5.3**, and the derived value of D_L was used to calculate δD_B. To obtain a value D_B, a grain boundary width must be assumed, it is reasonable to assume a width of about two atom layers, $\delta = 5\times10^{-8}$ cm [39,40].

Based on the numerical calculation, a satisfactory fitting to the experimental depth profile can be obtained [16]. The solid curves shown in **Fig. 5.18** are the fitted curves according to the derived parameters. The temperature dependence of the grain boundary diffusivity in W barrier can be expressed by the Arrhenius relation of $D_B = D_{B0} \exp(-Q_B/kT)$, as plotted in **Fig. 5.19**, where D_{B0} is the pre-exponential factor, Q_B is the activation energy for grain boundary diffusion, k is the Boltzmann constant, and T is annealing temperature. Also, the temperature dependence of the lattice diffusivity in W barrier can be expressed by the Arrhenius relation of $D_L = D_{L0} \exp(-Q_L/kT)$, where D_{L0} is the pre-exponential factor and Q_L is the activation energy for lattice diffusion.

The dependency is plotted in **Fig. 5.20**. The values of diffusivities, pre-exponential factors, and activation energies are summarized in **Table 5.3**. The *D* values of Cu in sputtered W films are smaller than those in CVD-W films, but the magnitudes are in the same order. In addition, the activation energy of Cu diffusion in sputtered W films is somewhat larger than that in CVD-W films [38,41].

Similar numerical analysis can be applied to evaluate the effects of Cu diffusion in W(N_2O) barriers. As mentioned previously, N_2O plasma treatment causes an amorphous surface layer upon the W film. This is the case of a semi-infinite medium which has a skin or surface layer W$(N_2O)_1$ having diffusion properties different from those of the rest of the medium W$(N_2O)_2$. The subscripts 1 and 2 denote the amorphous surface layer and the rest in the W(N_2O) barrier. Thus, suppose in the semi-infinite region $-h < y' < \infty$, the diffusion coefficient is D_{L1} in the region $-h < y' < 0$, and the concentration is denoted by C_1 there, while the corresponding quantities in $y' > 0$ are D_{L2} and C_2. Assume the conditions at the interface to be

$$C_1 = C_2, \ y' = 0$$

$$D_{L1}\frac{\partial C_1}{\partial y'} = D_{L2}\frac{\partial C_2}{\partial y'}, \ y' = 0$$

the solution to the problem of zero initial concentration and the surface $y' = -h$ maintained at constant concentration C_0 is given as following [18]

$$C_1 = C_0 \sum_{n=0}^{\infty} \alpha^n \left\{ \operatorname{erfc}\frac{(2n+1)h + y'}{2\sqrt{D_{L1}t}} - \alpha \operatorname{erfc}\frac{(2n+1)h - y'}{2\sqrt{D_{L1}t}} \right\} \tag{5.4}$$

$$C_2 = \frac{2kC_0}{k+1} \sum_{n=0}^{\infty} \alpha^n \operatorname{erfc}\frac{(2n+1)h + ky'}{2\sqrt{D_{L1}t}} \tag{5.5}$$

where

$$k = \sqrt{\frac{D_{L1}}{D_{L2}}} \quad , \quad \alpha = \frac{1-k}{1+k}$$

The thickness h of the surface layer $W(N_2O)_1$ is about 3 nm from high-resolution TEM micrograph. Both diffusion coefficients can be obtained by numerical calculation. The values of D_{L1} and D_{L2} can be roughly estimated from fitting of experimental concentration profiles using an error function solution such as that in Eq. 5.3. The estimated values are used as the initial guess of D_{L1} and D_{L2} and further substituted into the Eqs. 5.4 and 5.5 to obtain concentrations C_1 and C_2, respectively. To quickly obtain the numerical convergence, the high order terms are neglected in the Eqs. 5.4 and 5.5 during the calculation. It is found that the calculated error is smaller than 10^{-4} as n = 4. The relatively exact lattice diffusion coefficients can be found by fitting of the experimental concentration profile. **Figure 5.21** shows experimental and calculated concentration profiles. The derived values of D_{L1} and D_{L2} are listed in **Table 5.4**.

Similarly, grain boundary diffusion coefficients D_{B2} in $W(N_2O)_2$ region can be determined from the derived lattice diffusion coefficient D_{L2} and the slope in $\ln\overline{C}$ vs. $y'^{\frac{6}{5}}$ plots. **Figure 5.22** displays experimental and calculated concentration profiles for Cu diffusion in $W(N_2O)$ barriers at various annealing temperatures in the standard coordinates $\ln\overline{C}$ vs. $y'^{\frac{6}{5}}$. The derived grain boundary diffusion coefficients D_{B2} are listed in **Table 5.4**. **Table 5.4** summaries the values of diffusion coefficients and pre-exponential factors for Cu diffusion in $W(N_2O)$ barriers. Other barrier materials in literatures also list for comparison [38,41,42]. The $W(N_2O)$ barrier shows small lattice diffusion coefficients compared to W_2N, W, and TiB_2 barriers. The variation of D_{L2} with temperature is slight for the $W(N_2O)$ barrier, indicating that the $W(N_2O)$ barrier has better thermal stability.

One significant finding in the present study is that some atomic nitrogen and oxygen will react with W, segregate at grain boundaries of W film as impurities, and

act as a stuffing agent to block fast diffusion path during N_2O plasma treatment. Nitrogen addition will stuff the grain boundaries of W and nitrify tungsten to form tungsten nitride, as shown in XPS analyses of **Fig. 5.11(c)**. The same effect has been reported after forming of TiN barrier layer at the surface of Ti layer [43]. **Figure 5.23** shows cross sections of the interfacial structures of Cu/W/Si and Cu/W(N_2O)/Si samples before and after annealing,. The as-deposited W barrier has a columnar grain structure as shown in **Fig. 5.23(a)**. The failure of W barrier is attributed to the Cu diffusion through the columnar W to form Cu_3Si after annealing at 700°C for 30 min. Grain boundary diffusion coefficients are $2.3\sim4.7\times10^{-16}$ cm^2/s using Whipple analysis of grain boundary diffusion. The barrier capability of the W film against Cu diffusion can be improved by N_2O plasma treatment. An oxidized and nitrided layer with nanostructured grains is formed on the surface of the stuffed W barrier, as shown in **Fig. 5.23(b)**. Relatively low diffusion coefficients are found. No Cu silicide compound is observed for Cu/W(N_2O)/Si sample after annealing at 700°C for 30 min because nanostructured and stuffed barrier can effectively impede Cu diffusion.

5.4 Summary

Effects of N_2O plasma treatment on the thermal stability of the Cu/WN_x/n^+-p junction system were systematically investigated. With N_2O plasma treatments on WN_x barriers, the Cu/WN_x(N_2O)/Si systems sustained thermal annealing up to 750°C without electrical degradation. N_2O plasma treatment resulted in nitridation and oxidation of the WN_x barrier and formation of a resulting amorphous layer on the surface. Furthermore, N_2O plasma treatment introduces excessive nitrogen atoms to stuff grain boundaries of the WN_x barrier, and hence, effectively suppresses the formation of Cu-Si compound and improves barrier performance.

The effectiveness of W(N_2O) films as diffusion barriers between Cu and Si has been investigated. W(N_2O) films, which have amorphous and nano-grained surface layers, show high thermal stability, low resistivity, low surface roughness, low tensile stress, and better adhesion with Cu. W(N_2O) barriers show excellent barrier capabilities against Cu diffusion. Cu/W(N_2O)/n^+-p junction diodes retain leakage current densities less than 10^{-8} A/cm^2 even after annealing at 600°C. Copper diffusion in W and W(N_2O) barriers is further analyzed using the Whipple analysis of grain boundary diffusion and Fick's diffusion law. Both lattice and grain boundary diffusivities of Cu diffusion in W and W(N_2O) barriers are extracted from the Cu concentration profiles after annealing the samples at 600-700°C. Grain boundary diffusion coefficients of Cu in sputtered W films are 2.3~4.7×10^{-16} cm^2/s. Relatively low diffusion coefficients are found in W(N_2O) barriers because oxidized and nitrided layers with nano grains are formed on the surface of the stuffed W barriers after N_2O plasma treatments.

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Table 5.1 Properties of tungsten nitride barriers deposited at various nitrogen flow ratios used in the study.

	$N_2/(Ar+N_2)$ = 10%	15%	20%	30%
Deposition Rate (Å/min)	177.6	163.5	160.8	153.2
Resistivity (μΩ cm)	148.5	168.2	172.5	200.1
Stress (dyne/cm^2)	1.55×10^{-10}	1.45×10^{-10}	1.43×10^{-10}	1.40×10^{-10}
RMS Roughness (nm)	2.05	0.56	0.31	0.28
Grain Size (nm) measured from TEM	10 ~ 20	8 ~ 15	5 ~ 13	< 10
Atomic Ratio (W/N) measured from RBS	0.75/0.25	0.67/0.33	0.64/0.36	0.62/0.38
Density (g/cm^3) measured from RBS	17.39	17.07	16.9	16.33

Table 5.2 Properties of W, WN and W(N_2O) diffusion barriers. Properties of sputtered Ta, Ti films are also listed for comparison. Leakage current densities of diodes were measured at a reverse bias of 5V after annealing at 600°C for 30 min.

	W	W(N_2O)	WN[14]	Ta [13,31]	Ti [32,34]
Resistivity (μΩ cm)	~20	~24	150-200	~160	~ 70
RMS roughness (nm)	2.5	~0.5	1-2	4	3.2-4.2
Grain Size (nm)	20-40	2-5	5-15	20	10-30
Stress (dynes/cm^2)	1.9×10^{10}	1.4×10^{9}	1.5×10^{10}	2.0×10^{10}	3.9×10^{9}
Adhesion	poor	good	poor	poor	fair
Leakage current density (A/cm^2)	$\sim9.0\times10^{-4}$	$\sim3.0\times10^{-9}$	$\sim8.5\times10^{-6}$	2.5×10^{-5}	5.5×10^{-4}

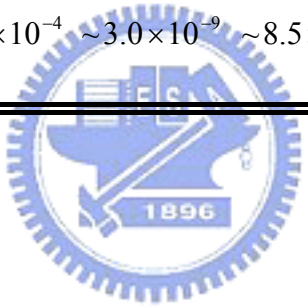


Table 5.3 Summary of the values of diffusivities, pre-exponential factors, and activation energies for Cu diffusion in W films at various annealing temperatures.

Sample	T(°C)	D_L (cm^2/s)	D_B (cm^2/s)	D_{L0} (cm^2/s)	Q_L (eV)	D_{B0} (cm^2/s)
W	600	2.28×10^{-16}	6.47×10^{-14}	1.83×10^{-13}	0.508	1.28×10^{-4}
	650	2.60×10^{-16}	1.24×10^{-13}			
	700	4.70×10^{-16}	6.05×10^{-13}			

Table 5.4 Summary of the values of diffusivities, and pre-exponential factors for Cu diffusion in $W(N_2O)$ films and at various annealing temperatures. Other barrier materials are also listed for comparison.

Sample	T (°C)	D_L (cm^2/s)		D_B (cm^2/s)	D_{L0} (cm^2/s)		D_{B0} (cm^2/s)
		D_{L1}	D_{L2}	D_{B2}	$D_{L0,1}$	$D_{L0,2}$	
$W(N_2O)$	600	1.17×10^{-16}	1.58×10^{-16}	4.07×10^{-14}	6.12×10^{-15}	6.43×10^{-15}	9.28×10^{-13}
	650	1.45×10^{-16}	2.04×10^{-16}	5.37×10^{-14}			
	700	1.76×10^{-16}	2.31×10^{-16}	5.57×10^{-14}			
W_2N [38]	600	1.15×10^{-16}			7.00×10^{-11}		
	700	4.52×10^{-16}					
W [41]	600	2.4×10^{-16}			1.11×10^{-13}		
	700	4.5×10^{-16}					
TiB_2 [42]	500	1.4×10^{-15}					
	600	2.0×10^{-15}					
	700	5.3×10^{-15}					
	800	5.0×10^{-14}					

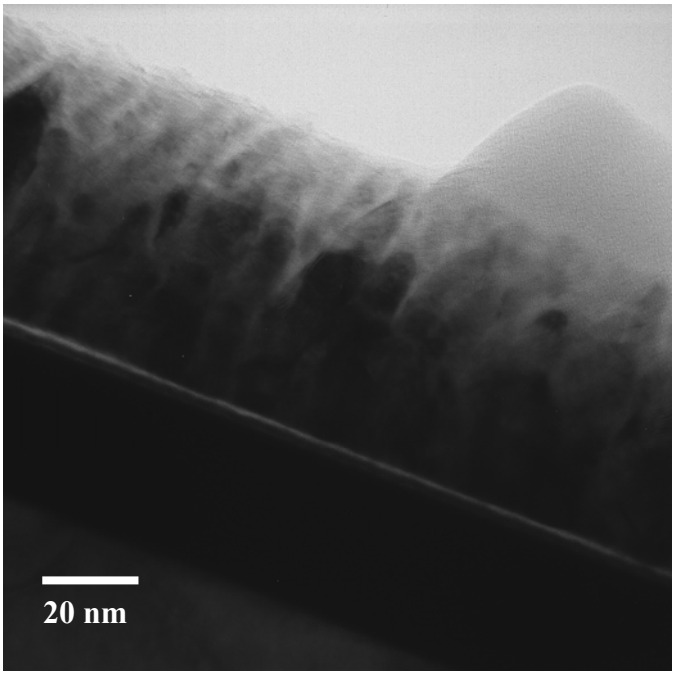
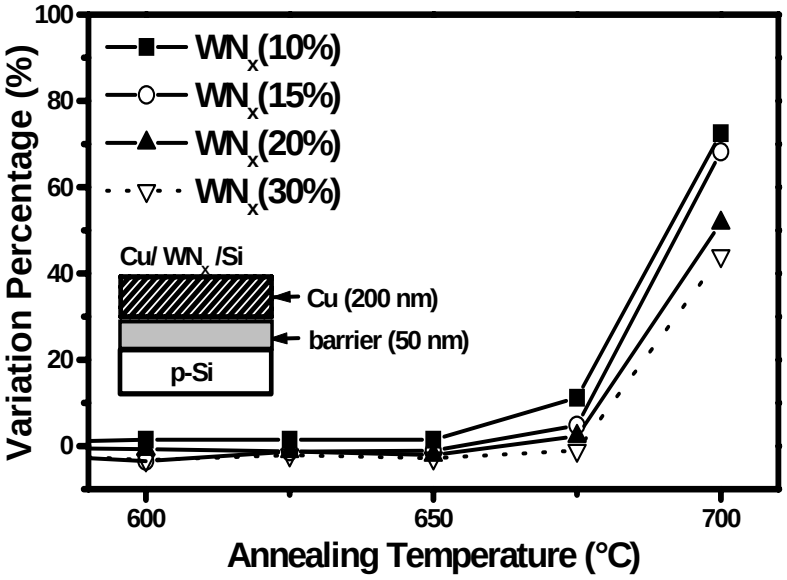
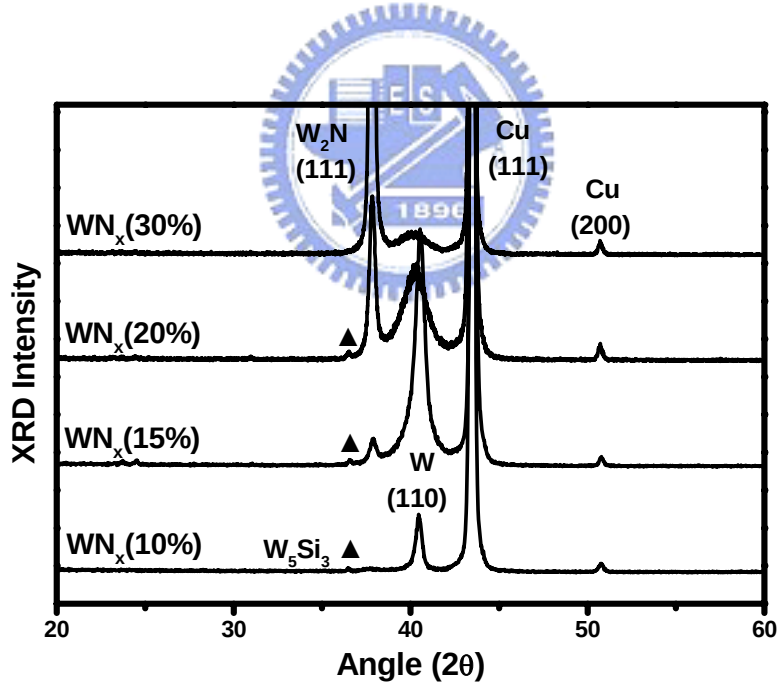


Figure 5.1 Cross-sectional TEM image of the WN_x(20%) film on the Si substrate.

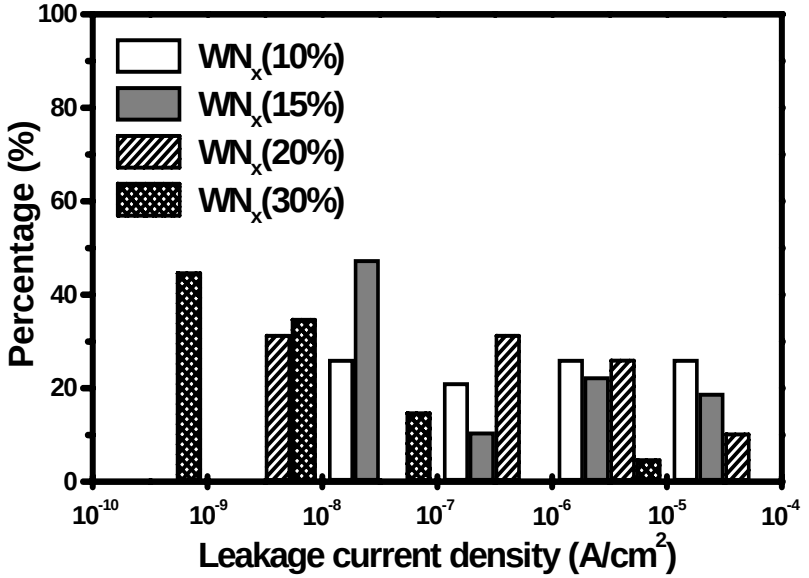


(a)

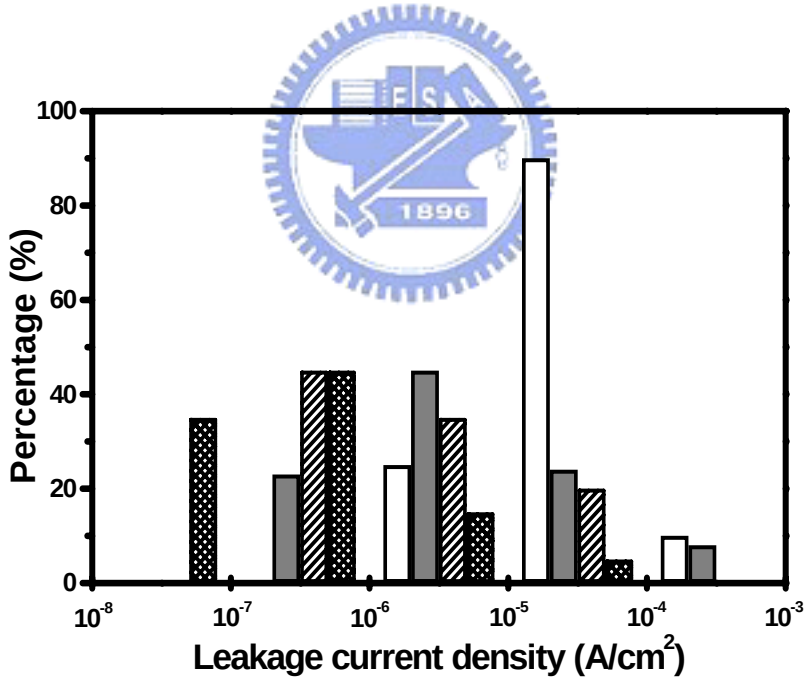


(b)

Figure 5.2 (a) Variation percentages in sheet resistance of $Cu/WN_x/Si$ contact system as a function of annealing temperature. (b) XRD spectra of $Cu/WN_x/Si$ contact systems after annealing at 675°C for 30 min.

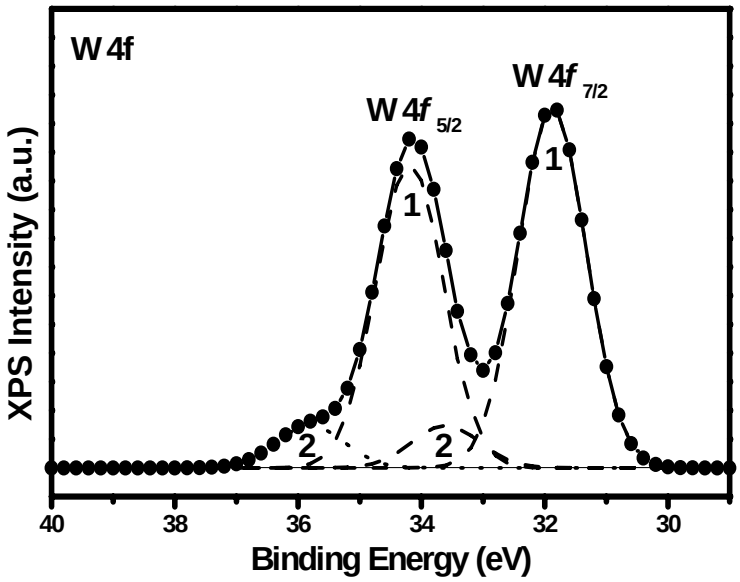


(a)

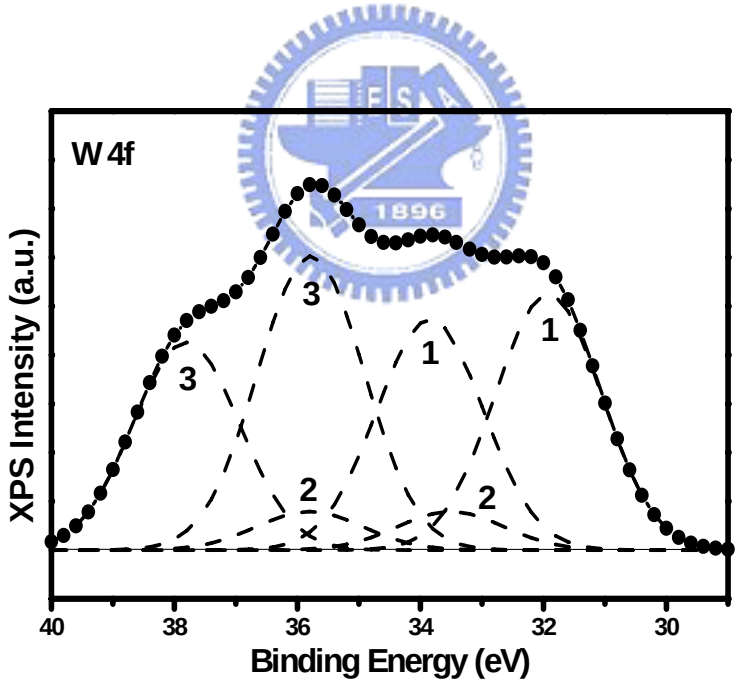


(b)

Figure 5.3 Statistical distributions of leakage current densities of Cu/WN_x/n^+-p junction diodes after annealing at (a) 500°C and (b) 600°C for 30 min.

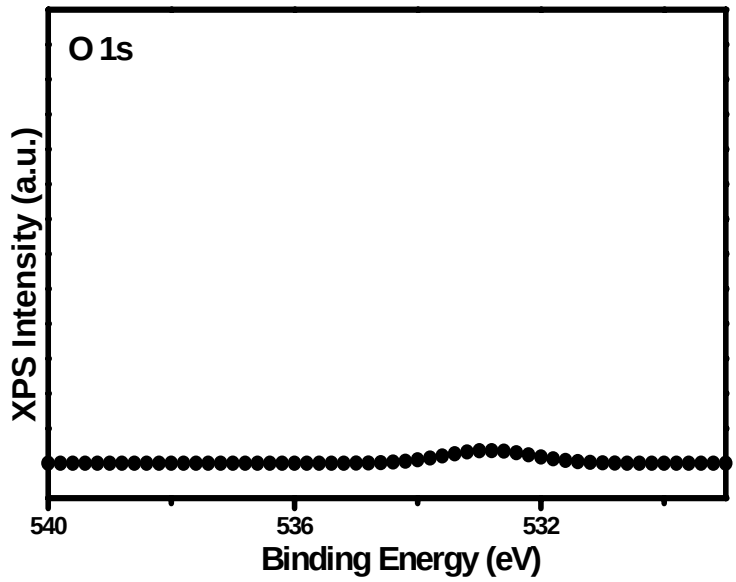


(a)

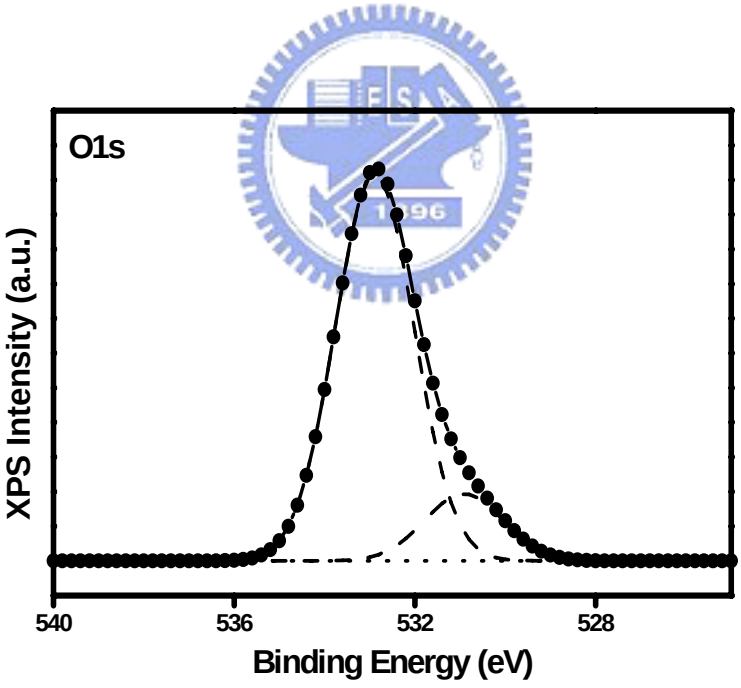


(b)

Figure 5.4 XPS W 4f spectra of WN_x(15%) and WN_x(N_2O) barriers.

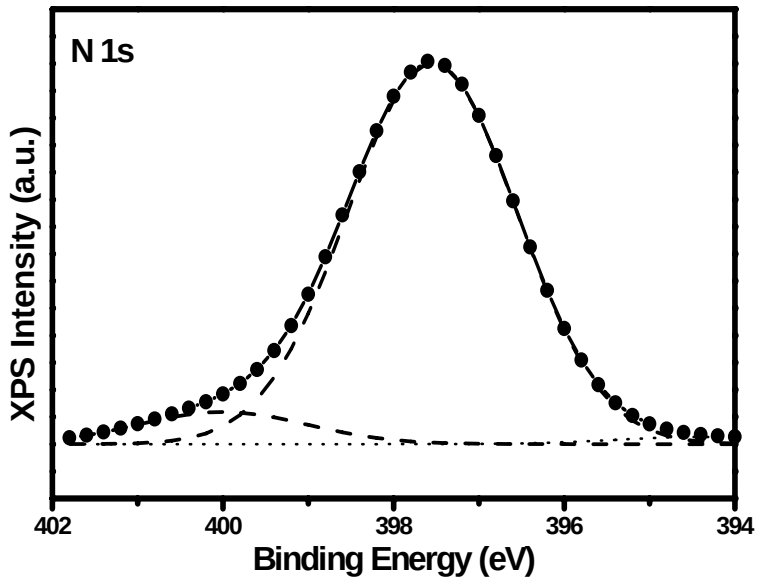


(a)

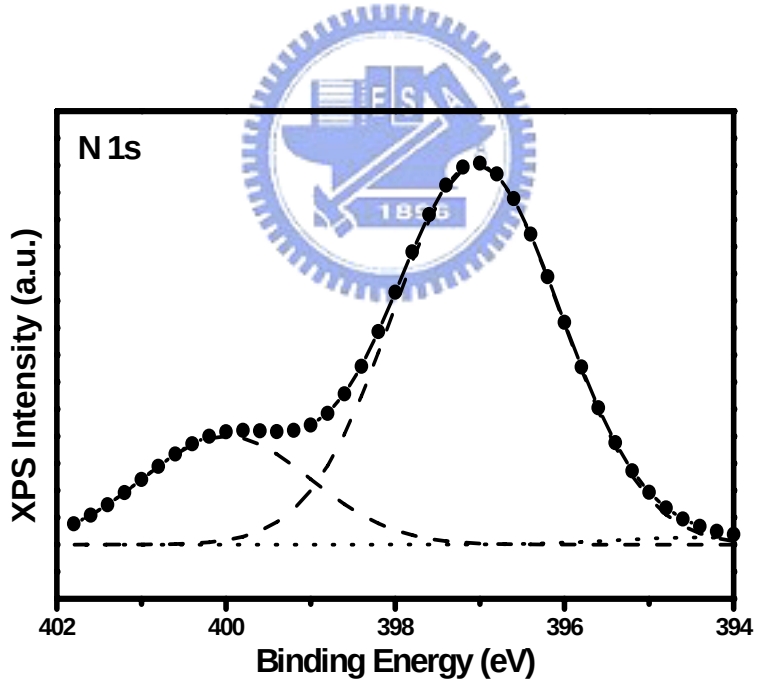


(b)

Figure 5.5 XPS O 1s spectra of WN_x(15%) and WN_x(N_2O) barriers.

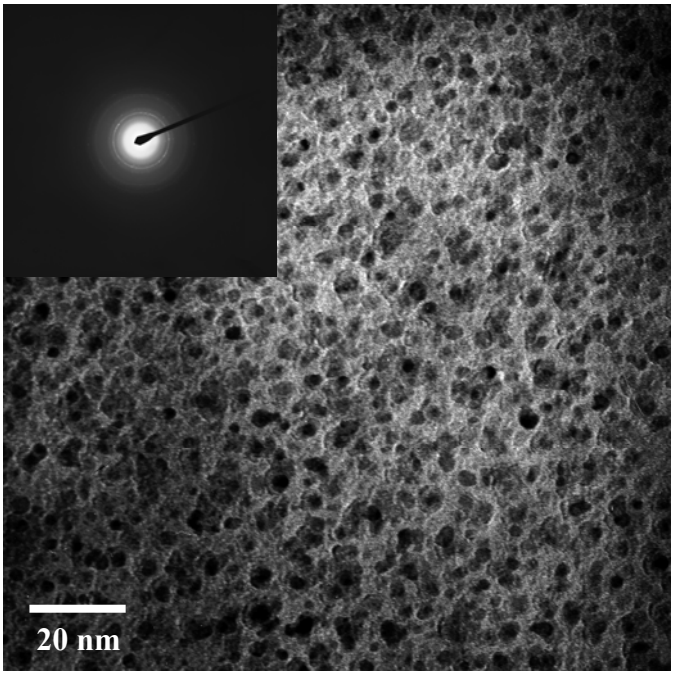


(a)

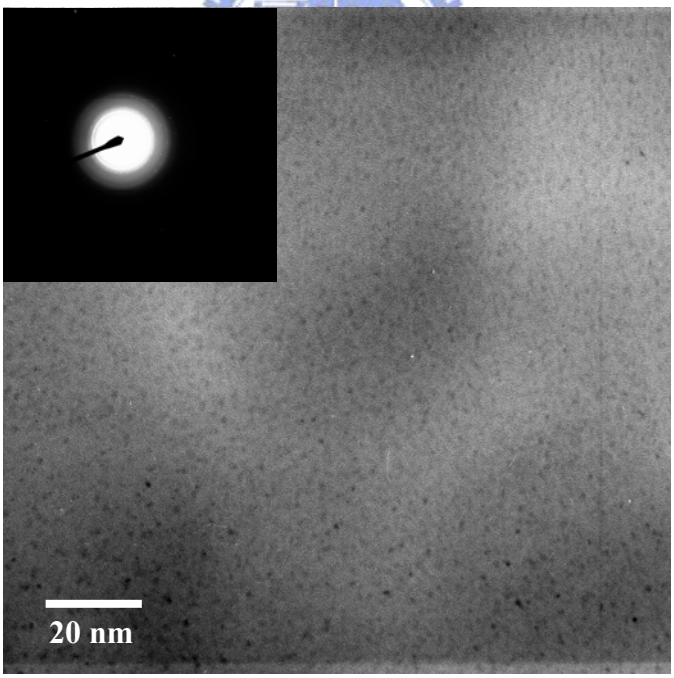


(b)

Figure 5.6 XPS N 1s spectra of WN_x(15%) and WN_x(N_2O) barriers.

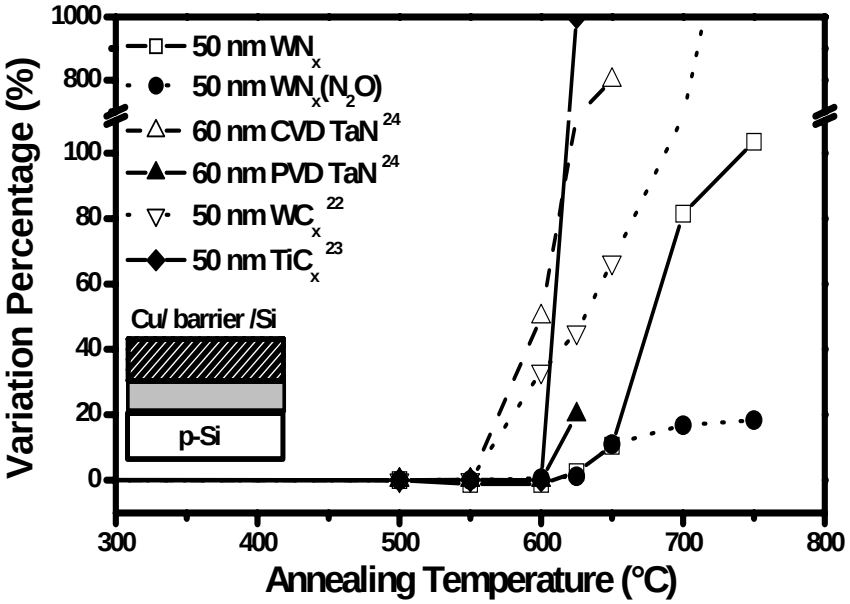


(a)

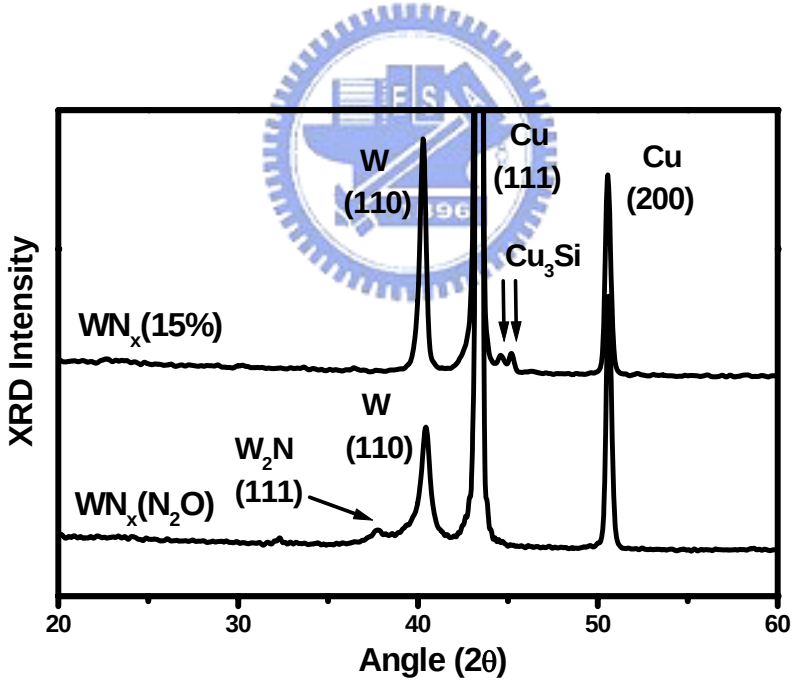


(b)

Figure 5.7 Bright-field TEM images and SAD patterns of the (a) WN_x(15%) and (b) $WN_x(N_2O)$ barriers.

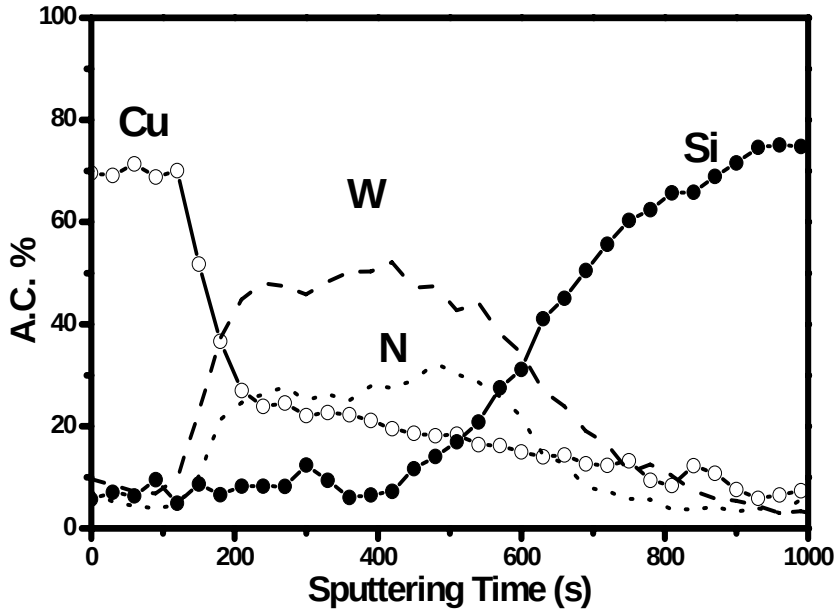


(a)

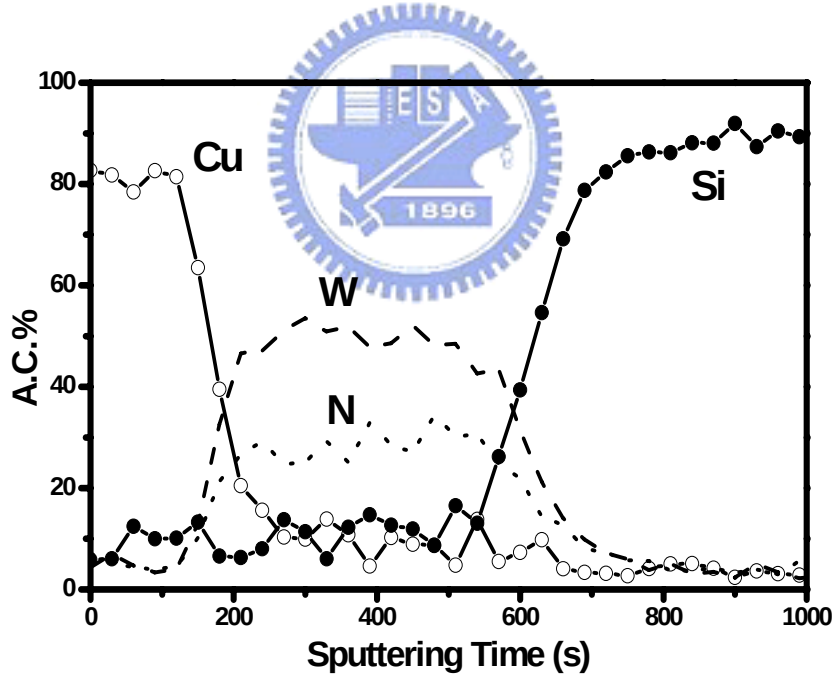


(b)

Figure 5.8 (a) Variation percentage in sheet resistance of Cu/barrier/Si contact system as a function of annealing temperature. (b) XRD spectra of Cu/WN_x(15%)/Si and Cu/WN_x(N_2O)/Si contact systems after annealing at 700°C for 30 min.

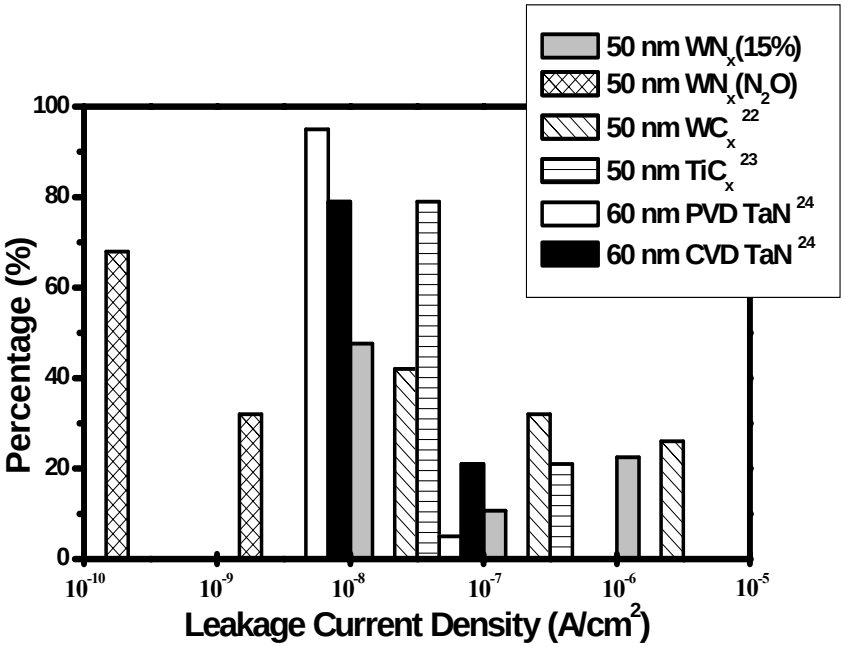


(a)

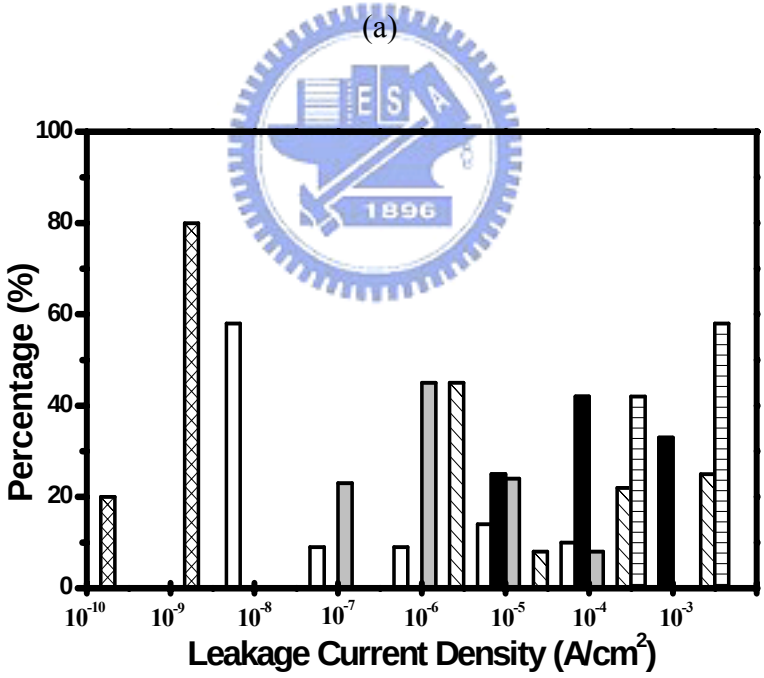


(b)

Figure 5.9 AES depth profiles of Cu/WN_x(15%)/Si and Cu/WN_x(N_2O)/Si contact systems after annealing at 675°C for 30 min.

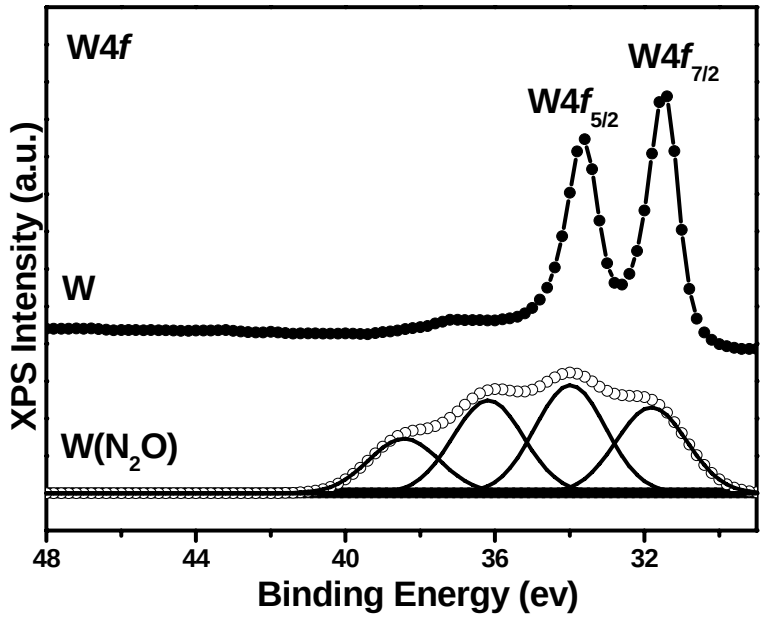


(a)

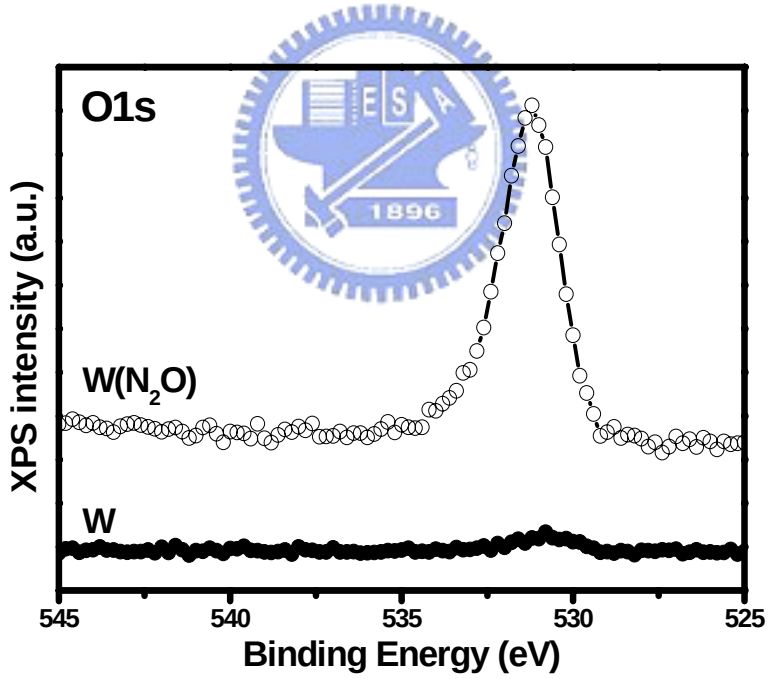


(b)

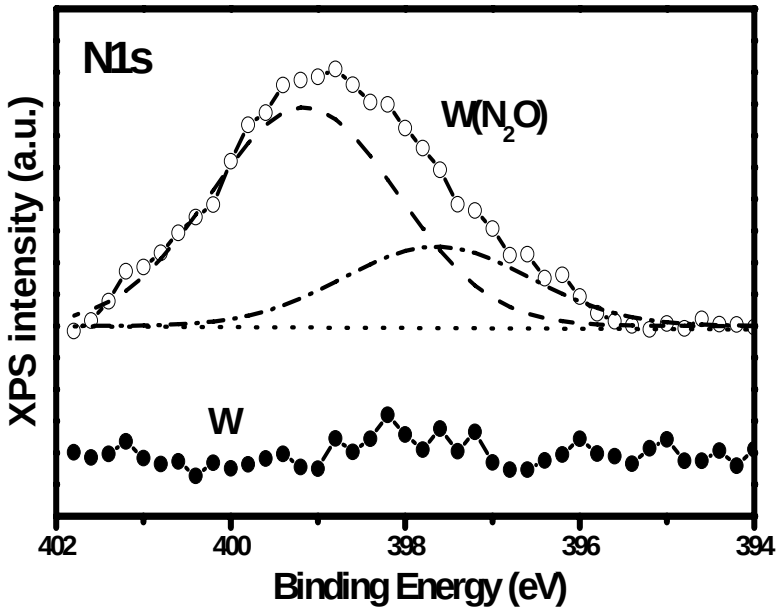
Figure 5.10 Statistical distributions of leakage current densities of Cu-contacted junction diodes with various diffusion barriers after annealing at (a) 500°C and (b) 600°C for 30 min.


W4f
W4f7/2
W4f5/2
XPS Intensity (a.u.)
W
W(N2O)
48
44
40
36
32
Binding Energy (ev)

(a)

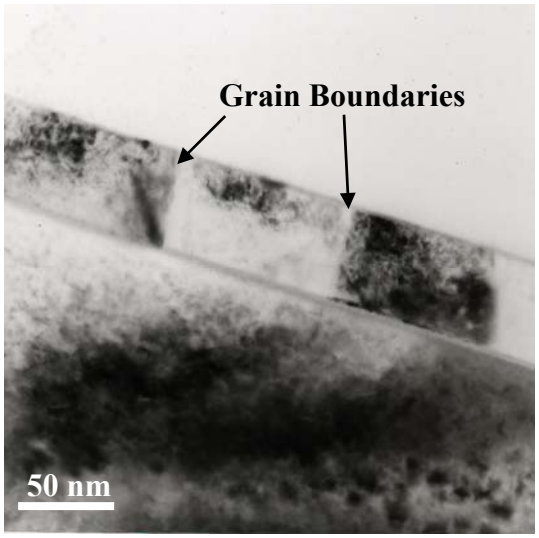

O1s
XPS intensity (a.u.)
W(N2O)
W
545
540
535
530
525
Binding Energy (eV)

(b)

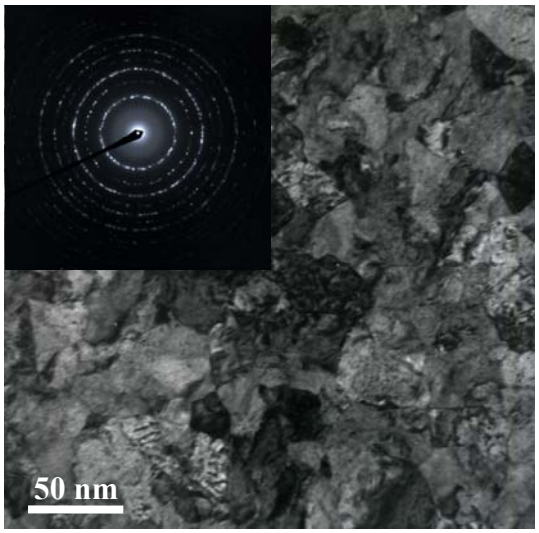


(c)

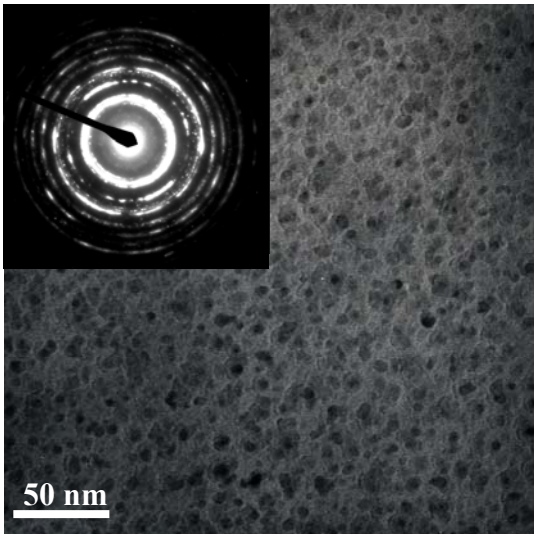
Figure 5.11 (a) W 4f, (b) O 1s, and (c) N 1s XPS spectra of W and W(N_2O) barriers.



(a)



(b)



(c)

Figure 5.12 (a) Cross-sectional bight field TEM image and SAD pattern of W barrier. Plan-view TEM images and SAD patterns of the (b) W and (c) W(N_2O) barriers.

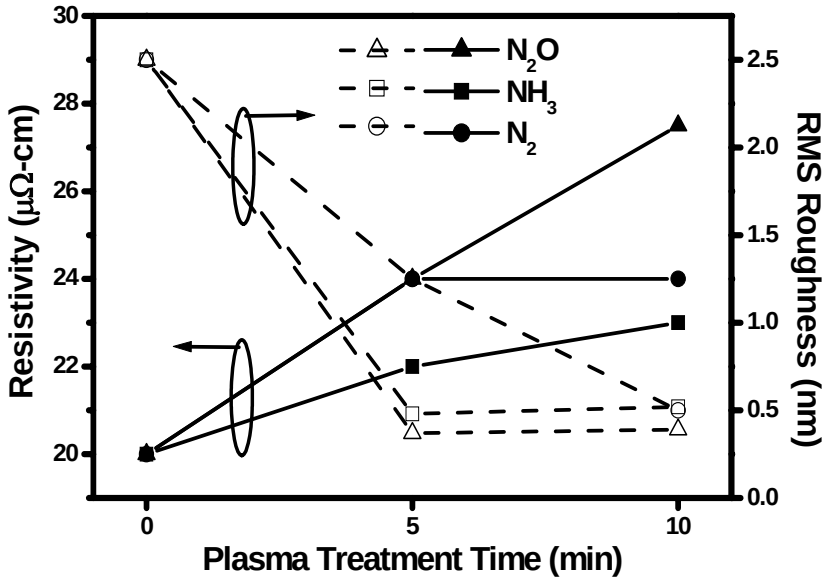
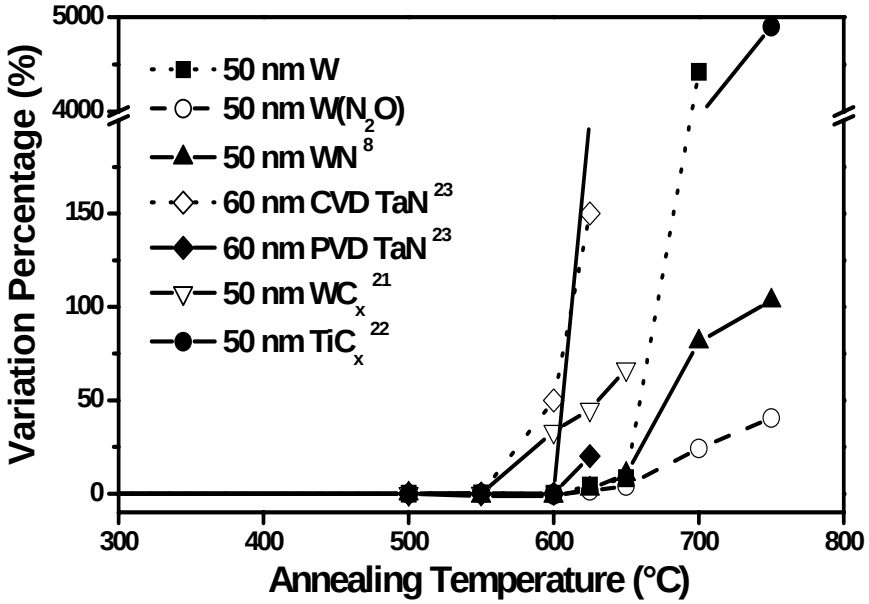
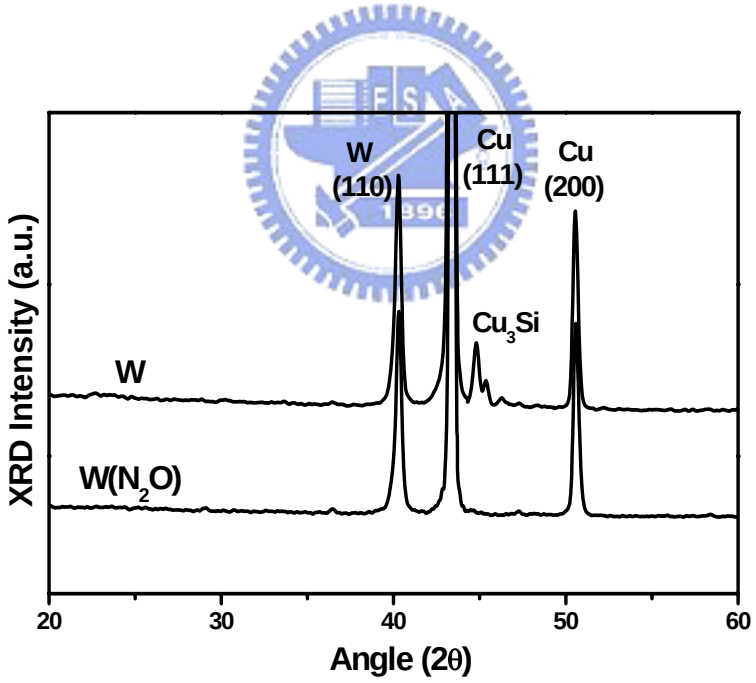


Figure 5.13 Resistivity and RMS surface roughness of $W(N_2)$, $W(NH_3)$, and $W(N_2O)$ films as a function of plasma treatment time.

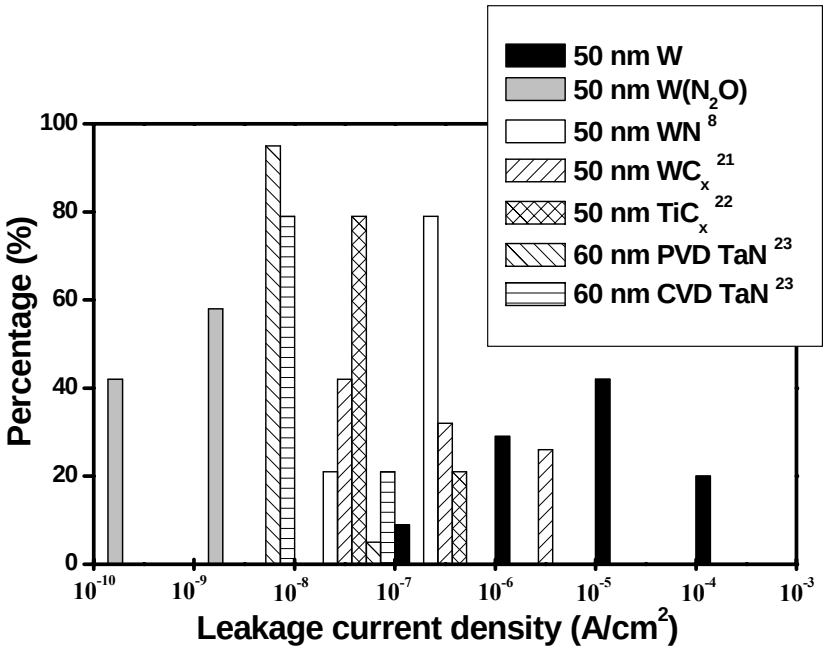


(a)

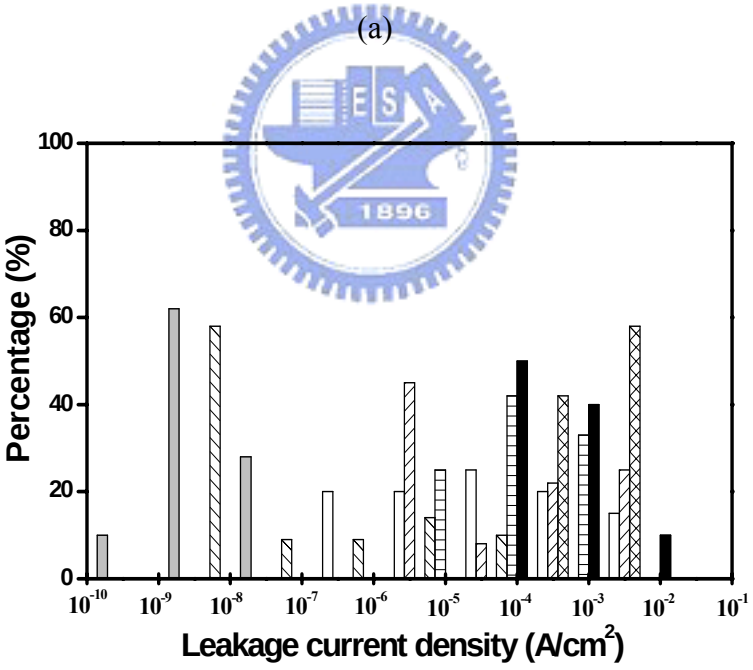


(b)

Figure 5.14 (a) Variation percentage in sheet resistance of Cu/barrier/Si as a function of annealing temperature. (b) XRD spectra of Cu/W/Si and Cu/W(N_2O)/Si contact systems after annealing at 700°C for 30 min.

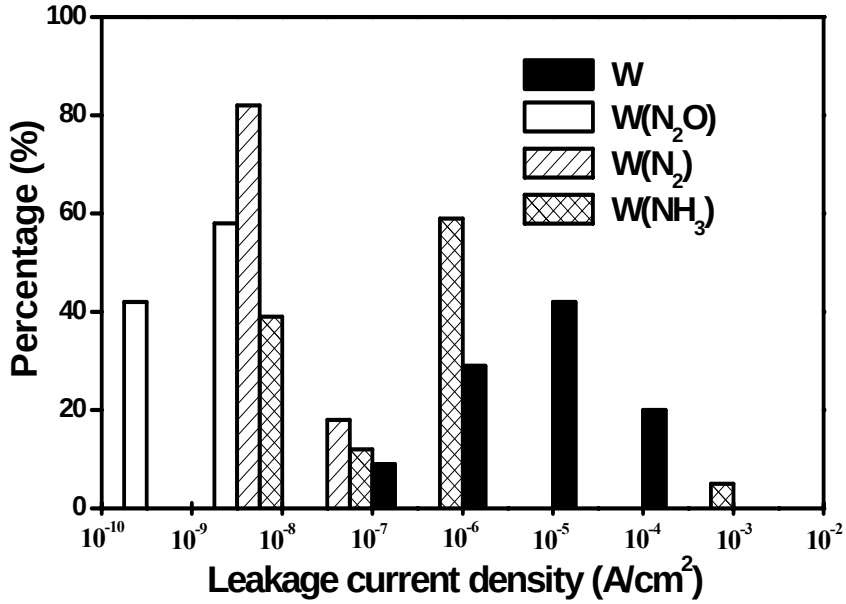


(a)

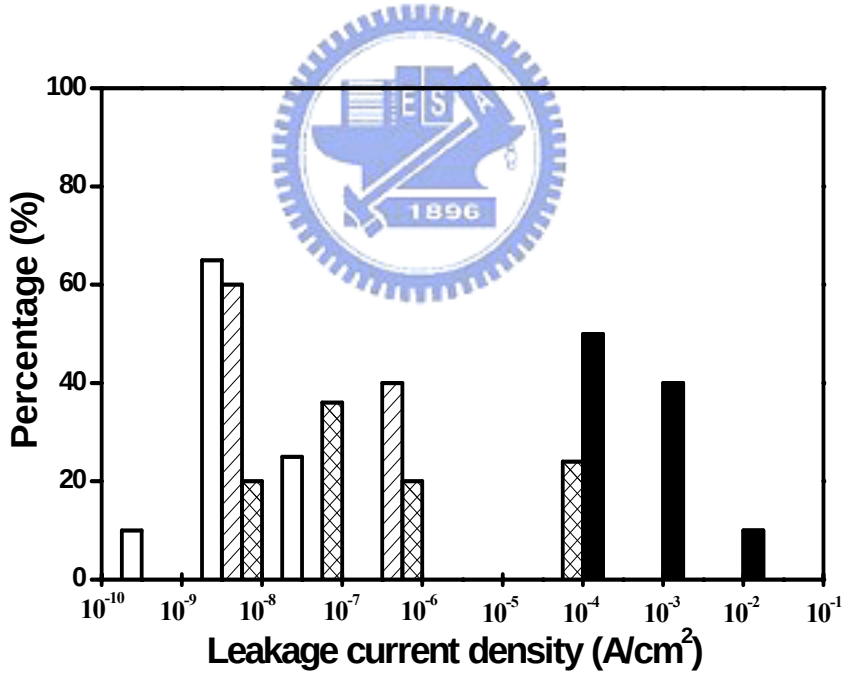


(b)

Figure 5.15 Statistical distributions of leakage current densities of copper contacted n^+-p junction diodes with various diffusion barriers after annealing at (a) 500°C and (b) 600°C for 30 min.

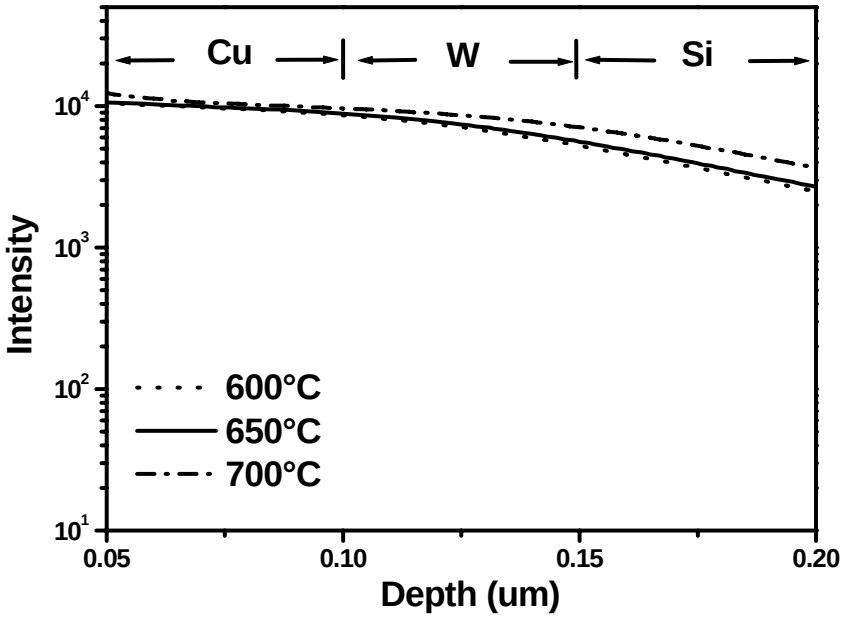


(a)

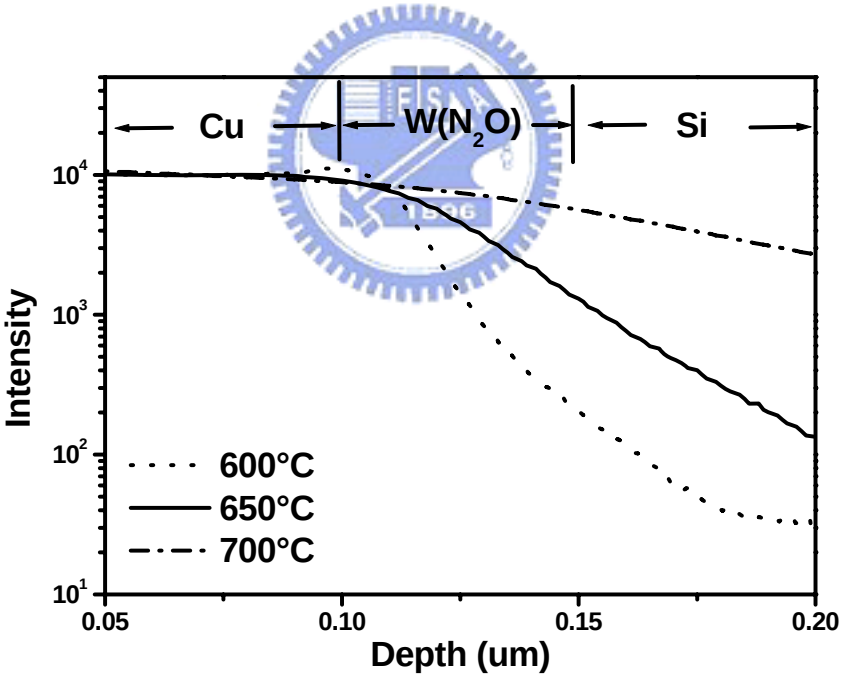


(b)

Figure 5.16 Statistical distributions of leakage current densities of copper contacted n^+-p junction diodes with various plasma-treated diffusion barriers after annealing at (a) 500°C and (b) 600°C for 30 min.

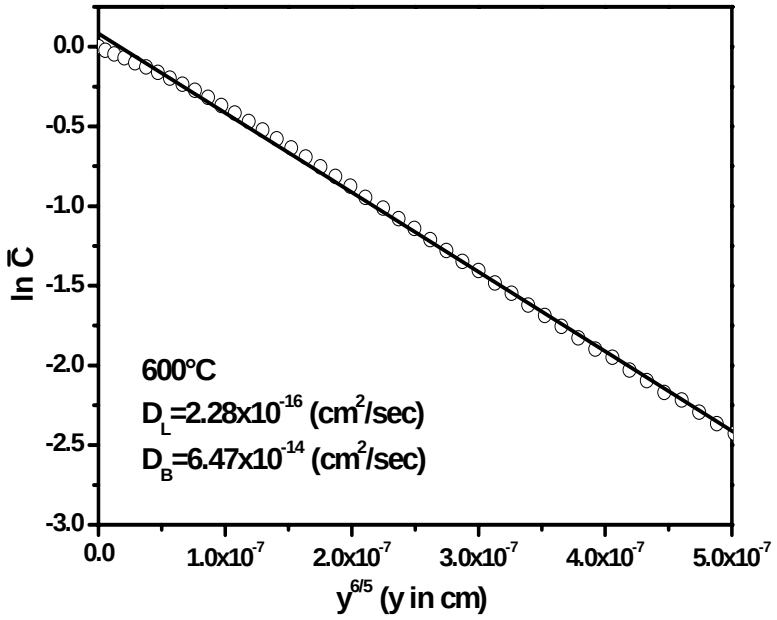


(a)

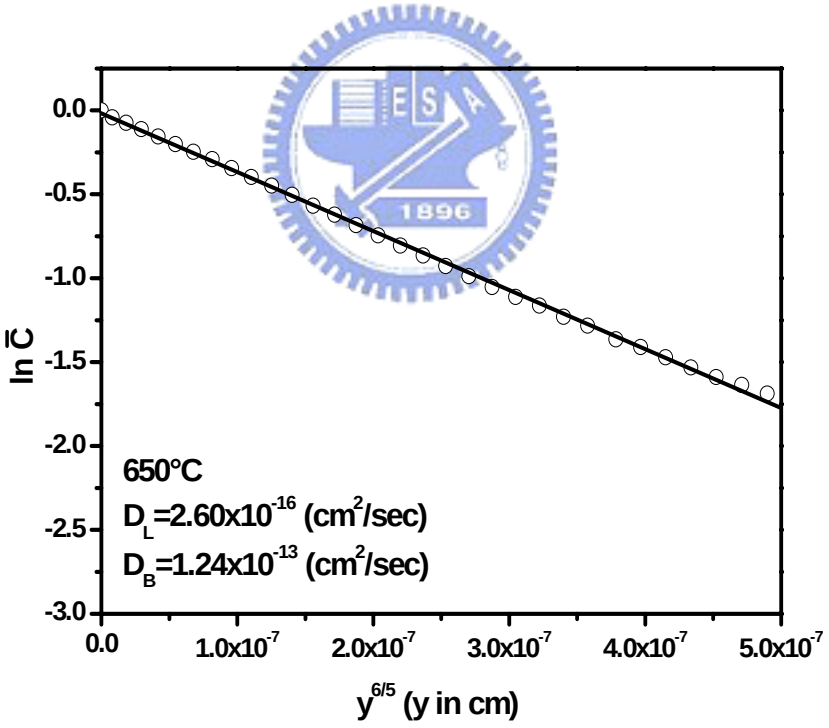


(b)

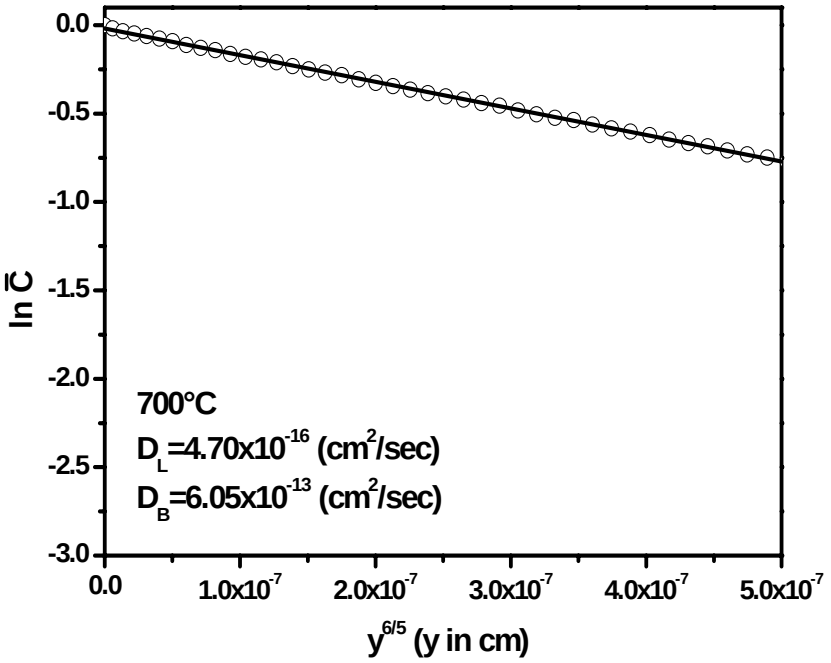
Figure 5.17 SIMS distribution profiles of the copper elements in (a) Cu/W/Si and (b) Cu/W(N_2O)/Si after annealing at 600, 650, and 700°C in N_2 ambient for 30 min.


0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
ln C̄
600°C
D_L=2.28x10^-16 (cm^2/sec)
D_B=6.47x10^-14 (cm^2/sec)
0.0
1.0x10^-7
2.0x10^-7
3.0x10^-7
4.0x10^-7
5.0x10^-7
y^6/5 (y in cm)

(a)


0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
ln C̄
650°C
D_L=2.60x10^-16 (cm^2/sec)
D_B=1.24x10^-13 (cm^2/sec)
0.0
1.0x10^-7
2.0x10^-7
3.0x10^-7
4.0x10^-7
5.0x10^-7
y^6/5 (y in cm)

(b)



(c)

Figure 5.18 Penetration plots for Cu diffusion into W films at various temperatures of (a) 600, (b) 650, and (c) 700°C. The solid curve is the profile calculated from Eq. (5.1).

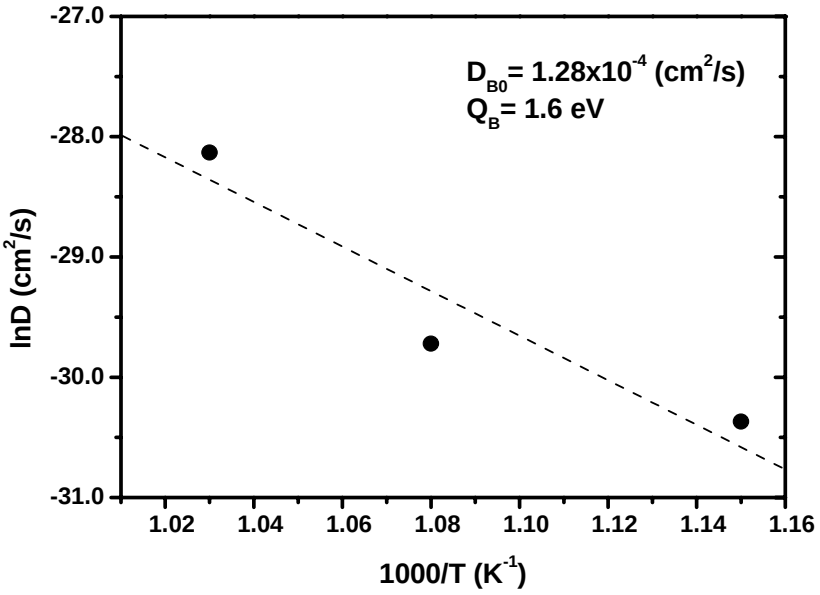


Figure 5.19 The Arrhenius plot of the grain boundary diffusivity D_B for Cu diffusion in W films.

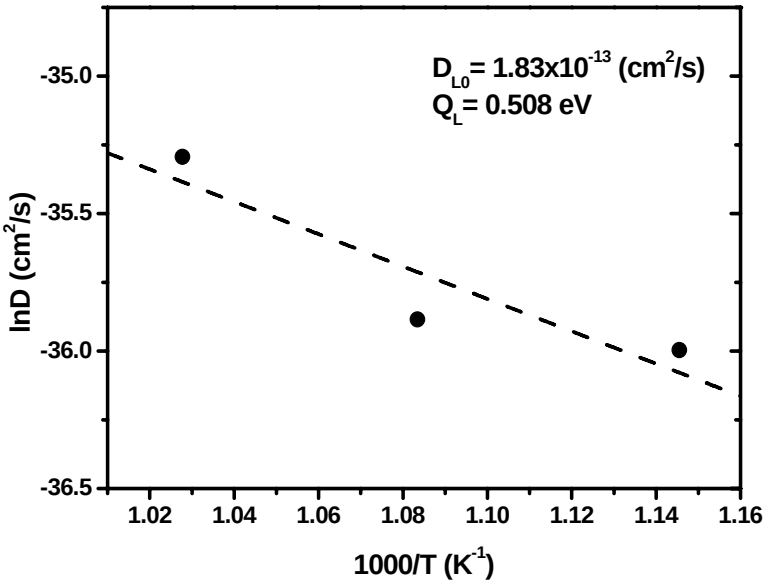
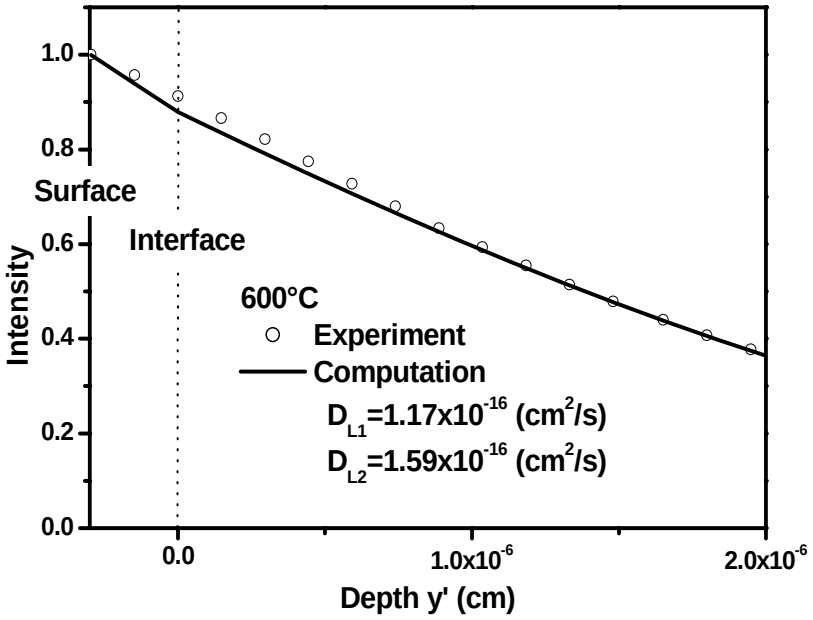
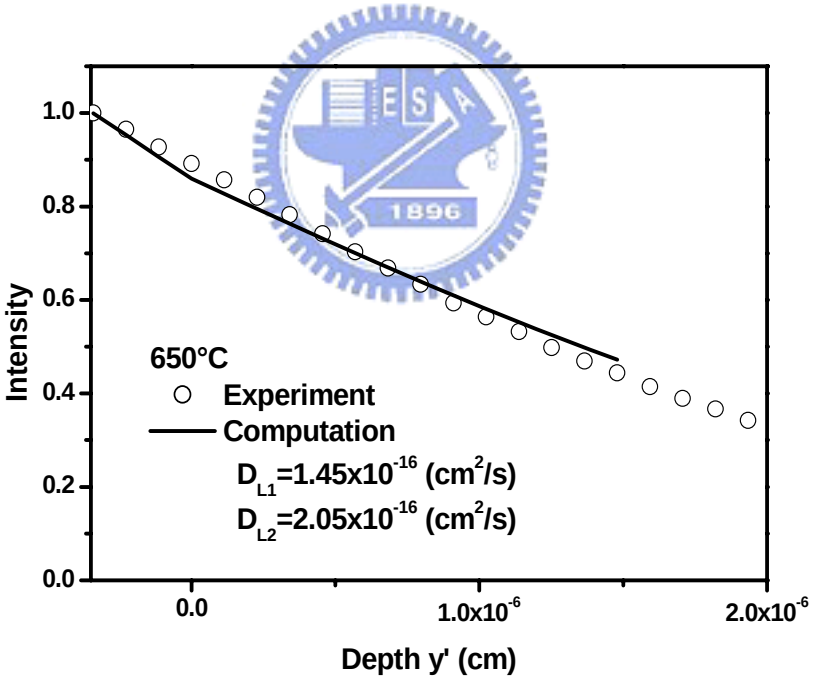


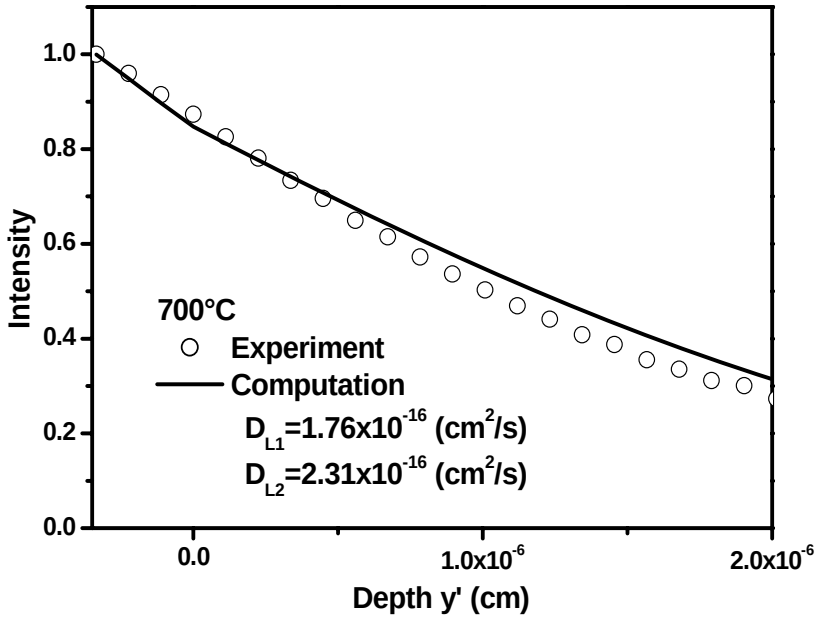
Figure 5.20 The Arrhenius plot of the lattice diffusivity D_L for Cu diffusion in W films.


1.0
0.8
0.6
0.4
0.2
0.0
Intensity
Surface
Interface
600°C
Experiment
Computation
D_{L1}=1.17x10^{-16} (cm^2/s)
D_{L2}=1.59x10^{-16} (cm^2/s)
0.0
1.0x10^{-6}
2.0x10^{-6}
Depth y' (cm)

(a)

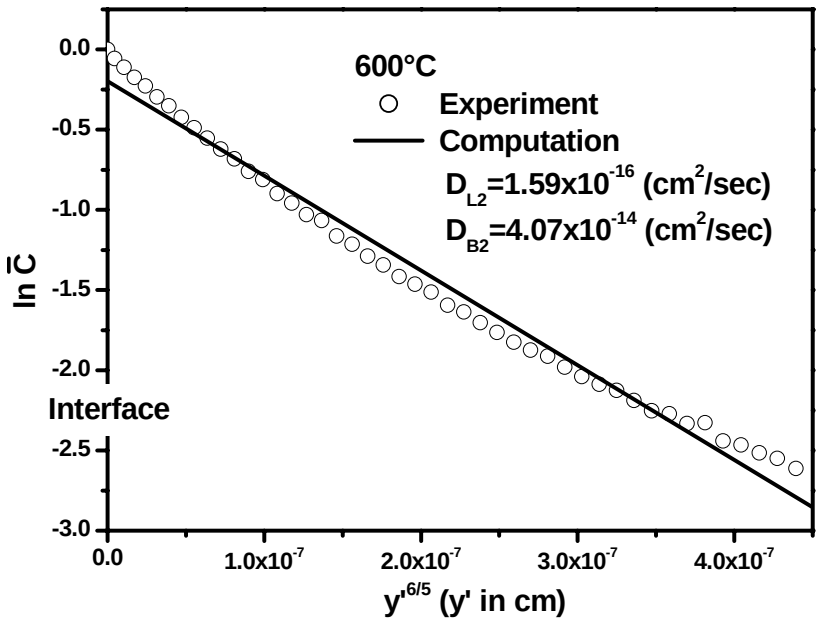

1.0
0.8
0.6
0.4
0.2
0.0
Intensity
650°C
Experiment
Computation
D_{L1}=1.45x10^{-16} (cm^2/s)
D_{L2}=2.05x10^{-16} (cm^2/s)
0.0
1.0x10^{-6}
2.0x10^{-6}
Depth y' (cm)

(b)

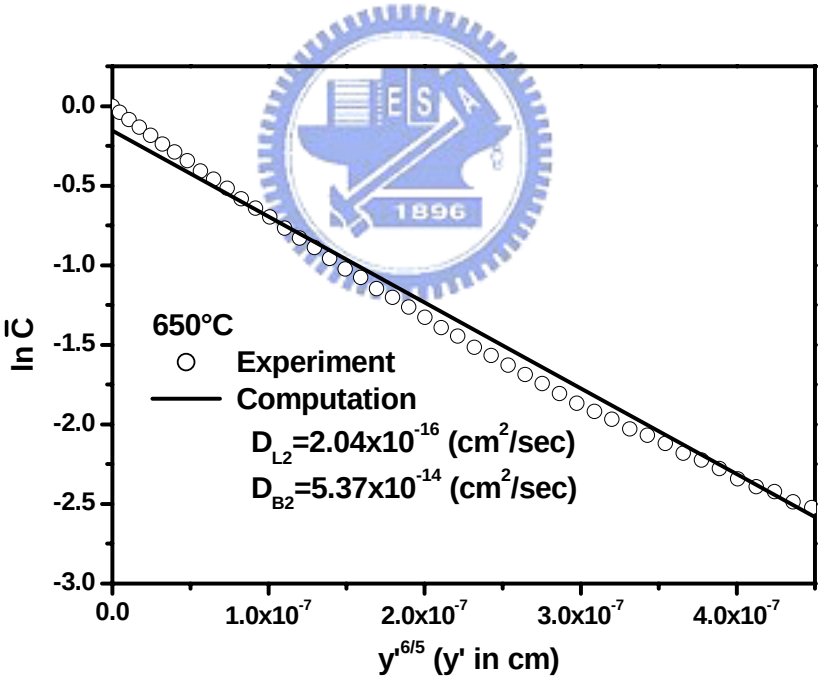


(c)

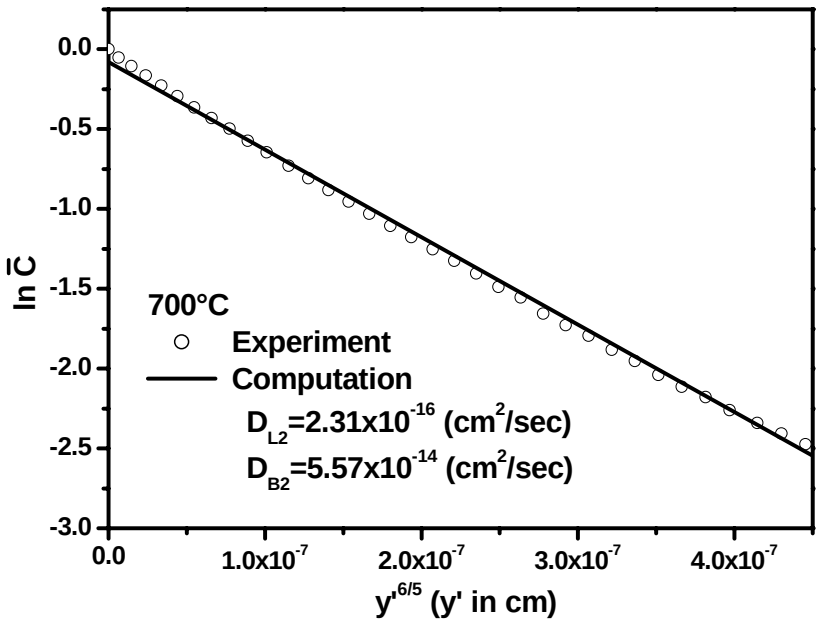
Figure 5.21 Penetration plots for Cu diffusion into W(N_2O) films at various temperatures of (a) 600, (b) 650, and (c) 700°C. The solid curve is the profile calculated from Eqs. (5.4) and (5.5).


600°C
Experiment
Computation
D_{L2}=1.59x10^{-16} (cm^2/sec)
D_{B2}=4.07x10^{-14} (cm^2/sec)
Interface
ln C̄
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
0.0
1.0x10^{-7}
2.0x10^{-7}
3.0x10^{-7}
4.0x10^{-7}
y'$^{6/5}$ (y' in cm)

(a)


650°C
Experiment
Computation
D_{L2}=2.04x10^{-16} (cm^2/sec)
D_{B2}=5.37x10^{-14} (cm^2/sec)
ln C̄
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
0.0
1.0x10^{-7}
2.0x10^{-7}
3.0x10^{-7}
4.0x10^{-7}
y'$^{6/5}$ (y' in cm)

(b)



(c)

Figure 5.22 Penetration plots for Cu diffusion into W(N_2O) films at various temperatures of (a) 600, (b) 650, and (c) 700°C. The solid curve is the profile calculated from Eq. (5.3).

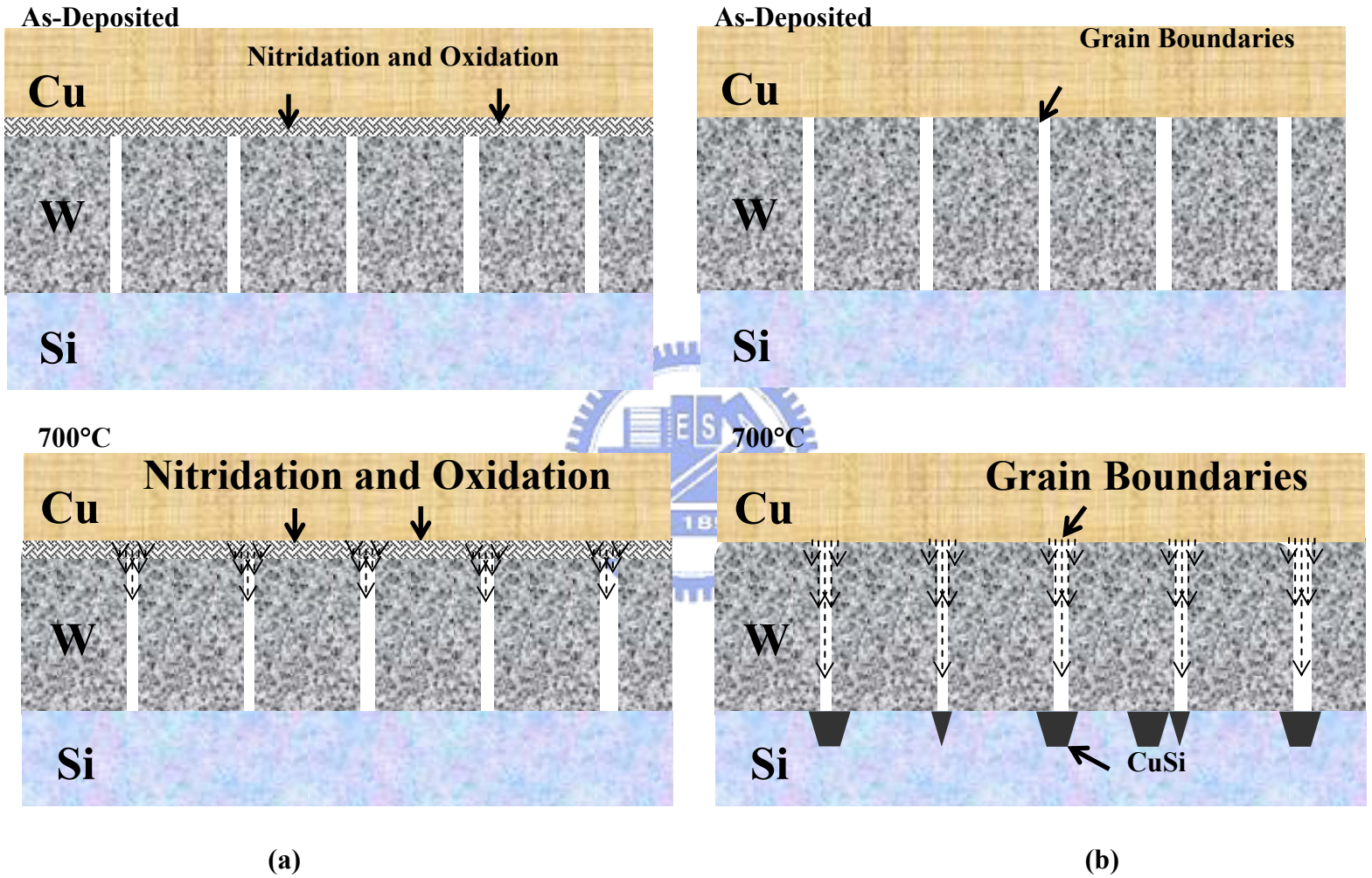


Figure 5.23 Schematic illustrations of the microstructures of (a) Cu/W/Si, and (b) Cu/W(N_2O)/Si samples before and after annealing.

Chapter 6

Conclusions

For the high reliability and performance Ta_2O_5 capacitor with Cu-based electrodes:

1. The capacitors demonstrated a significant improving capability against oxygen diffusion after inserting an Al film. This improvement is attributed to a dense Al_2O_3 film formed after thermal annealing in oxygen ambient.
2. Low leakage current density and high breakdown field are obtained for Ta_2O_5 MIM capacitors with Al/Ta/Cu/Ta electrodes because of reducing oxygen vacancy in tantalum oxide films.
3. The electrical properties of Ta_2O_5 thin films following the inductively coupled N_2O plasma post treatments had low leakage current densities, high breakdown fields, and lifetimes of over 10 years at 1.61 MV/cm due to effectively dissociated N_2O gas and reduced bombardment.

For the high reliability and performance BST capacitor with Cu-based electrodes:

1. The presence of Mg in Cu dramatically reduces the oxidation rate of the metal. Thin self-aligned MgO layers were formed by annealing in ambient oxygen. The resulting barriers had high thermal stability of up to 400 or 500°C.
2. The BST MIM capacitor with Cu-based electrodes has a high capacitance density and a low dissipation factor, which can be adapted to satisfy the requirements of the ITRS roadmap. It has a low leakage current density of $2.0x10^{-8}$ A/cm^2 and a high breakdown field of 3.2 MV/cm, small linear VCCs of 101 ppm/V^2, 1347 ppm/V and TCC of 274 ppm/ºC, and a TDDB of over 10

years at 1.1 MV/cm.

3. Applying oxygen surface plasma treatment to as-etched BST films can effectively reduce the chlorine-based residues at low substrate temperatures with short process duration. The recovery behavior of the as-etched BST film can be explained by the fact that metal-chlorine compounds can be removed from the surface and increase the number of metal-oxide bonds.

For the diffusion barrier layers on integration of Cu and SiOC:H films:

1. The Ti did not improve the loss of H from SiOC:H caused by the thermal decomposition, however, the TiN block the lattice diffusion path for H atoms.
2. Integrating Cu in low-*k* SiOC:H with poor Cu resistance involves thin TaN and Ta diffusion barrier layers, which effectively provide a low leakage current density of around 2×10^{-10} A/cm^2 at 1 MV/cm, a high breakdown field at E>4 MV/cm of over 1.0×10^{-6} A/cm^2, and a low Cu^+ ion drift rate at various temperatures in the Cu/TaN/Ta-gated MIS capacitor.

For the performance of W-based diffusion barrier layers for Cu interconnection:

1. With N_2O plasma treatments on WN_x barriers, the Cu/WN_x(N_2O)/Si systems sustained thermal annealing up to 750°C without electrical degradation. N_2O plasma treatment resulted in nitridation and oxidation of the WN_x barrier and formation of a resulting amorphous layer on the surface.
2. With N_2O plasma treatments on W barriers, which have amorphous and nano-grained surface layers, show high thermal stability, low resistivity, low surface roughness, low tensile stress, and better adhesion with Cu.
3. Copper diffusion in W and W(N_2O) barriers is further analyzed using the Whipple analysis of grain boundary diffusion and Fick's diffusion law. Grain

boundary diffusion coefficients of Cu in sputtered W films are $2.3\sim4.7\times10^{-16}$ cm^2/s.

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(民國 86 年 9 月 至 民國 88 年 6 月)
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(民國 87 年 9 月 至 民國 88 年 6 月)

專長

1. 積體被動元件材料與製程
2. ULSI 金屬化製程
3. 積體電路後段銅製程
4. 高介電常數介電質電容元件
5. 低介電常數介電質薄膜製程
6. 高介電常數介電質薄膜製程
7. 材料電性與物性分析

Publication List

International Journal

1. **Kou-Chiang Tsai**, Wen-Fa Wu, Jen-Chung Chen, Chuen-Guang Chao and Te-Jen Pan, "Influence of N_2O plasma treatment on microstructure and thermal stability of WN_x barriers for Cu interconnection," *J. Vac. Sci. Tech. B* **22**(3) 993 (2004).
2. **Kou-Chiang Tsai**, Wen-Fa Wu, Jen-Chung Chen, Chuen-Guang Chao and Te-Jen Pan, "Numerical and Experimental Analysis of Cu Diffusion in Plasma-treated Tungsten Barrier," *J. Electrochem. Soc.* **152**(1), G83-G91 (2005).
3. Wen-Fa Wu, **Kou-Chiang Tsai**, Chuen-Guang Chao, Jen-Chung Chen and Keng-Liang Ou "A Novel Multilayered Ti/TiN Diffusion Barrier for VLSI Technology," *J. Electron. Mater.* **34**(8), 1150 (2005).
4. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao and Cheng-Ping Kuan, "High Reliability Ta_2O_5 MIM Capacitors with Cu-based Electrodes", *J. Electrochem. Soc*. **153**, G492 (2006).
5. **Kou-Chiang Tsai**, Wen-Fa Wu and Chuen-Guang Chao, "Influence of bias-temperature stressing on the electrical characteristics of SiOC:H film with Cu/TaN/Ta-gated capacitor" to be published on *J. Electron. Mater*. (2006).
6. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain Tsai Lee and Jwo-Lun Hsu, "Improvement of etching-induced damage of high-*k* $Ba_{0.5}Sr_{0.5}TiO_3$ thin films by oxygen surface plasma treatment" to be published on *Jpn. J. Appl. Phys*. **45**, 6B (2006).
7. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain Tsai Lee and Shih-Wen Shen, "Thermal stability enhancement and electrical properties of $(Ba,Sr)TiO_3$ thin films on Cu(Mg) bottom electrodes" to be published on *Jpn. J. Appl. Phys* **45**, 6B (2006).
8. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao and Chi-Chang Wu, "Improving the electrical characteristics of $Ta/Ta_2O_5/Ta$ capacitors using low-temperature inductively coupled N_2O plasma annealing" has submitted to *J. Electrochem. Soc*.
9. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain-Tsai Lee, Wei-Che Chang and Guo-Shen Jheng, " Impact of Cu-based electrodes on the reliability of metal insulator metal $(Ba,Sr)TiO_3$ thin-film capacitors" has submitted to *J. Electron. Mater*.
10. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jwo-Lun Hsu and Chiu-Fen Chiang, " Influence of Ti, TiN, Ta and TaN layers on integration of low-*k* SiOC:H and Cu" has submitted to *Mater. Chem. Phys*.

International Conference

1. **K. C. Tsai**, W. F. Wu, C. P. Kuan, C. C. Wu, and C. G. Chao, "Improving Characteristics of Tantalum Oxide Thin Film Devices with Copper Electrodes", 2004 International Conference on Solid State Devices and Materials, p. 460, (SSDM 2004, Japan).
2. **K. C. Tsai**, W. F. Wu, C. G. Chao, J. L. Hsu, C. W. Yen and C. F. Chiang, "Influence of diffusion barrier layer on integration of low-*k* dielectric silicon oxycarbide and copper", 2004 Advanced Metallization Conference (ADMETA 2004, Japan).
3. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain Tsai Lee, and Jwo-Lun Hsu, "Improvement of etching-induced damage of high-*k* $Ba_{0.5}Sr_{0.5}TiO_3$ thin films by oxygen surface plasma treatment", 2005 International Microprocesses and Nanotechnology Conference, p. 122 (MNC 2005, Japan)
4. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain Tsai Lee, and Shih-Wen Shen, "Thermal stability enhancement and electrical properties of (Ba,Sr)TiO_3 thin films on Cu(Mg) bottom electrodes", 2005 International Microprocesses and Nanotechnology Conference, p. 124 (MNC 2005, Japan)

Conference

1. **K. C. Tsai**, J. L. Hsu, W. F. Wu, and C. G. Chao, "The study of integration of diffusion barrier layers and low-k dielectrics", Proc. of The 2003 Annual Conference of The Chinese Society For Material Science, CSMS, p-246 (2003).
2. **K. C. Tsai**, J. L. Hsu, W. F. Wu, C. W. Yen, and C. G. Chao, "Characteristics of tantalum based diffusion barrier in silicon oxycarbide and copper damascene structure", Proc. of 2003 Electrics Devices and Materials Symposium, EDMS p. 25 (2003).
3. **K. C. Tsai**, J. L. Hsu, W. F. Wu, S. W. Shen, and C. G. Chao, "Metal diffusion barriers for the integration of silicon oxycarbide", Proc. of 2003 Electrics Devices and Materials Symposium, EDMS, p. 30 (2003).
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6. **K. C. Tsai**, W. F. Wu, J. C. Chen, T. J. Pan, and C. G. Chao, "Highly thermally stable W-based barriers formed by plasma treatment for Cu interconnection", The 3rd Asian Conference on Chemical Vapor Deposition (ACVD 2004).
7. **K. C. Tsai**, W. F. Wu, J. L. Hsu, S. W. Shen, and C. G. Chao, "Influence of thermal reactions and interdiffusion in Cu/TiN/Ti/SiOCH/n^+-p multilayer structure", The 3rd Asian Conference on Chemical Vapor Deposition (ACVD 2004).
8. J. C. Chen, **K. C. Tsai**, C. G. Chao, "Development of a Novel Process for Metal Coated on a Carbon Fiber Tow by PVD and Electroless Deposition", The 3rd Asian Conference on Chemical Vapor Deposition. 82-83 (ACVD 2004).
9. Jen-Chung Chen, **Kou-Chiang Tsai**, Chi-Yuan Lin and Chuen-Guang Chao. A study of Flow Field in the Fiber Pneumatic Spreader by Numerical Simulation and Experimet; The 11th National CFD Conference, August, 2004.
10. **K. C. Tsai**, W. F. Wu, J. C. Chen, T. J. Pan, and C. G. Chao, "Simulation of Copper/Tungsten Interdiffusion following Plasma Treatment", Proc. of The 2004 Annual Conference of The Chinese Society For Material Science, CSMS, p-84 (2004).
11. Jen-Chung Chen, **Kou-Chiang Tsai**, Chi-Yuan Lin, Chuen-Guang Chao, "An investigation on the mechanism of electroless nickel plating in a carbon fiber tow for EMI shielding", Proc. of The 2004 Annual Conference of The Chinese Society For Material Science, CSMS, p-51 (2004).
12. **K. C. Tsai**, J. T. Lee, J. L. Hsu, J. L. Hsu, W. F. Wu, and C. G. Chao, "Etching characteristics of high-k $Ba_{0.5}Sr_{0.5}TiO_3$ thin films using helicon-wave plasma system", Symposium on Nano Device Technology 2005, p.274, SNDT (2005).
13. Jain-Tsai Lee, **Kou-Chiang Tsai**, Wen-Fa Wu, and Chuen-Guang Chao, "Electrical properties of high-k $(Ba,Sr)TiO_3$ thin films deposited on Ta", Symposium on Nano Device Technology 2005, p.273, SNDT (2005).
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15. Jen-Chung Chen, **Kou-Chiang Tsai**, Wen-Fa Wu and Chuen-Guang Chao, "Modeling of Grain Boundary Diffusion of Cu in Plasma-treated Tungsten Thin Films", Electronics Devices and Materials Symposia, p87, EDMS 2005.
16. Jen-Chung Chen, **Kou-Chiang Tsai**, C. G. Kou and Chuen-Guang Chao, "Fabrication of Carbon nanotube/Carbon Fiber Hybrid Multiscale Composites for Development of a High Performance Dielectric Materials," Electronics

Devices and Materials Symposia, p113, EDMS 2005.

17. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain-Tsai Lee, Wei-Che Chang, Guo-Shen Jheng, and Jian-Yang Lin, "A High Reliability Metal Insulator Metal (Ba,Sr)TiO_3 Thin-Film Capacitor for Copper Technology," to be published on Symposium on Nano Device Technology 2006, p. , SNDT (2006).
18. **Kou-Chiang Tsai**, Wen-Fa Wu, Chuen-Guang Chao, Jain Tsai Lee, Jwo-Lun Hsu, and Chiu-Fen Chiang, "Investigation of damage reduction of etched $Ba_{0.5}Sr_{0.5}TiO_3$ thin films by oxygen plasma," to be published on Symposium on Nano Device Technology 2006, p. , SNDT (2006).
19. G. S. Jheng, J. Y. Lin, W. F. Wu, and **K. C. Tsai**, "Fabrication Study on the (Ba,Sr)TiO3 Metal-Insulator-Metal Capacitor with Cu-based electrode", to be published on Symposium on Nano Device Technology 2006, SNDT (2006).
20. W. C. Chang, T. K. Kang, W. F. Wu, **K. C. Tsai**, C. T. Chang, and K. T. Tsao "Study of the Interface Quality Improvement on High-κ Capacitors by Plasma and Annealing Process", to be published on Symposium on Nano Device Technology 2006, SNDT (2006).