PAPER

Impedance-Isolation Technique for ESD Protection Design in RF Integrated Circuits*

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SUMMARY An impedance-isolation technique is proposed for on-chip ESD protection design for radio-frequency (RF) integrated circuits (ICs), which has been successfully verified in a 0.25-μm CMOS process with thick top-layer metal. With the resonance of LC-tank at the operating frequency of the RF circuit, the impedance (especially, the parasitic capacitance) of the ESD protection devices can be isolated from the RF input node of low-noise amplifier (LNA). Therefore, the LNA can be co-designed with the proposed impedance-isolation technique to simultaneously achieve excellent RF performance and high ESD robustness. The power gain (S_{21}-parameter) and noise figure of the ESD protection circuits with the proposed impedance-isolation technique have been experimentally measured and compared to those with the conventional double-diodes ESD protection scheme. The proposed impedance-isolation technique had been demonstrated to be suitable for on-chip ESD protection design for RF ICs.
key words: *electrostatic discharge (ESD), impedance-isolation technique, LC-tank, noise figure power gain*

1. Introduction

With the advantages of high integration and low cost for mass production, integrated circuits (ICs) operating in giga-Hz (GHz) frequency bands have been designed and fabricated in complementary metal-oxide-silicon (CMOS) technology. Electrostatic discharge (ESD), which can cause serious damage to IC products, must be taken into consideration during the design phase of ICs, including radio-frequency (RF) ICs [1], [2]. However, the parasitic effects of on-chip ESD protection devices at the I/O pad often cause degradation of the performance of RF ICs. There are several requirements for ESD protection devices for RF ICs: low parasitic capacitance, constant input capacitance, insensitive to substrate-coupling noise, and high ESD robustness [3], [4]. The traditional input ESD protection device is the gate-grounded NMOS (GGNMOS), which is often implemented with large device dimensions and wide drain-contact-to-poly-gate spacing to sustain an acceptable ESD level. To further improve the ESD robustness of NMOS, the gate-coupled technique and the substrate-triggered technique had been reported to uniformly trigger the multiple fingers of the ESD protection NMOS [5]–[7]. However, the GGNMOS with a larger device size and a wide drain diffusion area contributes large parasitic capacitance to the input pad. Moreover, the overlapped gate-to-drain capacitance also contributes to the input pad. Thus, GGNMOS is not suitable for ESD protection for RF applications.

Silicon-controlled rectifier (SCR) had been demonstrated to be suitable for ESD protection design for RF ICs, because it has both high ESD robustness and low parasitic capacitance under a small layout area [8], [9]. However, the issue of high trigger-on voltage and slow turn-on speed must be overcome to effectively protect the thin gate oxide of input devices in RF ICs [10].

A typical specification on the maximum loading capacitance of the ESD protection device for a 2-GHz low-noise amplifier (LNA) was specified as ~200 fF [11]. In order to fulfill such a tight specification, diodes had been commonly used for ESD protection in LNA, as illustrated in Fig. 1 [12]–[14]. Moreover, by adding a turn-on efficient ESD clamp circuit between the power rails, the overall ESD level of the RF input pin had been significantly improved [12], [13]. To reduce the parasitic capacitance of the ESD protection devices contributed to the input pad, two or more diodes were stacked in the ESD protection circuits, as shown in Fig. 2 [3], [4]. Besides, the parasitic capacitance of the ESD protection devices can be tuned out by inductance [15], [16].

In this paper, a new ESD protection concept with LC-tank to isolate the parasitic capacitances of the ESD protec-

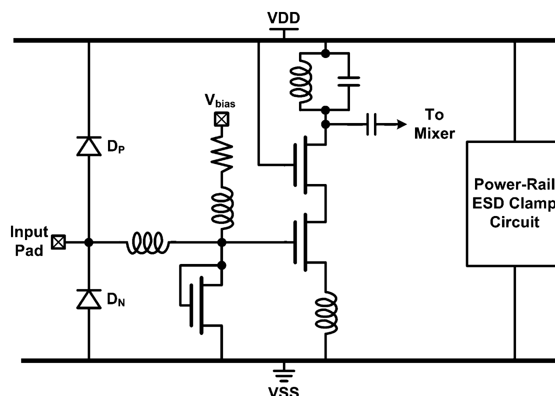

Fig. 1 Conventional ESD protection design with double diodes and the power-rail ESD clamp circuit for the input pin of the low-noise amplifier (LNA) [12].

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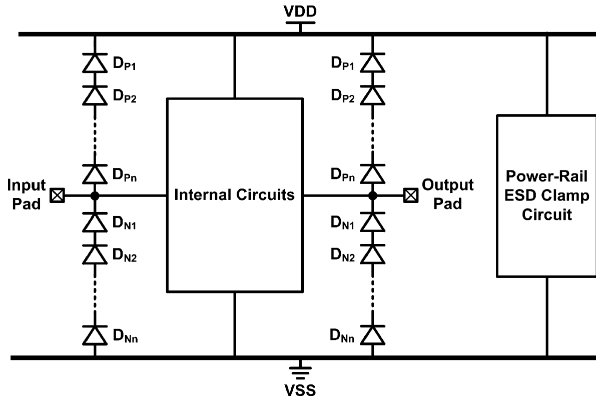


Fig. 2 ESD protection design with stacked diodes to reduce the equivalent parasitic capacitance of ESD protection devices for an RF input pin [4].

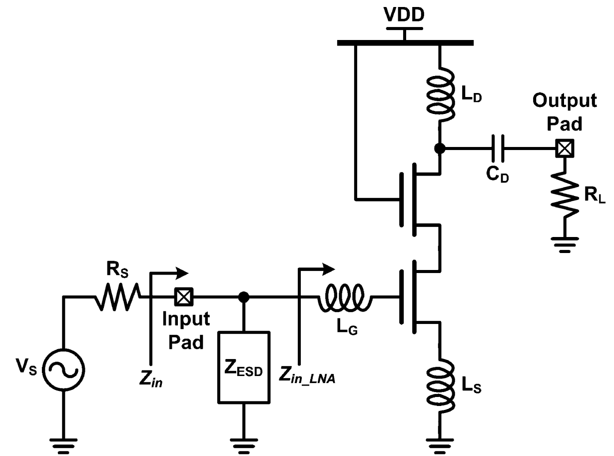


Fig. 3 Schematic circuit diagram of an LNA with on-chip ESD protection device for calculating the overall power gain.

tion devices for giga-Hz RF applications is proposed [17], [18]. The LC-tank is designed to resonate for "open circuit" at the operating frequency of the RF circuit. Thus, the RF input port will ideally see very huge impedance from the ESD protection devices with LC-tank. The proposed LC-tank ESD protection circuits with different combinations of inductances and capacitances have been designed and verified in a 0.25-μm CMOS process. The RF performance, including the power gain and noise figure, of the fabricated LC-tank ESD protection circuits have been experimentally investigated by two-port S-parameter and noise figure measurement. Besides, the human-body-model (HBM) and machine-model (MM) ESD robustness of the fabricated LC-tank ESD protection circuits have been verified by the ESD tester.

2. Impact of ESD Devices on RF Performance

To find the negative impacts caused by ESD protection devices on the RF performance of an LNA, the power gain of an RF LNA with on-chip ESD protection device has been calculated from its schematic circuit diagram, as shown in Fig. 3. A simple expression for the input impedance (Z_{in_LNA}) of the inductively degenerated LNA at resonance is [19]

$$Z_{in_LNA} = s(L_s+L_g)+\frac{1}{sC_{gs}}+\left(\frac{gm}{C_{gs}}\right)L_s \approx \omega_T L_s = R_s. \quad (1)$$

The overall input impedance of the RF LNA with ESD protection devices (Z_{in}) is

$$Z_{in} = Z_{ESD}//Z_{in_LNA} \approx Z_{ESD}//R_s \quad (2)$$

where Z_{ESD} is the parasitic impedance of the ESD protection devices at the input node. Therefore, the overall transconductance (G_m) of the LNA is

$$\begin{aligned} G_m &= \frac{Z_{ESD}}{Z_{ESD}+R_s}\frac{\omega_T}{s(R_s+Z_{in})} \\ &= \frac{\omega_T}{sR_s}\frac{Z_{ESD}}{R_s+2Z_{ESD}} = \frac{\omega_T}{sR_s}\frac{1}{2+\dfrac{R_s}{Z_{ESD}}}. \end{aligned} \quad (3)$$

To analyze the overall power gain of the LNA, the feedback capacitor C_{gd} of the MOS transistor was neglected first, and the input and output were assumed to be conjugately matched to get a simpler expression for the power gain. The transducer power gain (G_T) is

$$\begin{aligned} G_T &= \frac{P_L}{P_{avs}} = \frac{\frac{1}{8}|V_sG_m|^2(R_o//R_s)}{\frac{1}{8}|V_s|^2/R_s} = |G_m|^2 R_s(R_o//R_s) \\ &= \left(\frac{\omega_T}{\omega_0}\right)^2\frac{(R_o//R_s)}{R_s}\left|\frac{1}{2+\dfrac{R_s}{Z_{ESD}}}\right|^2. \end{aligned} \quad (4)$$

In (4), P_L is the average power delivered to the load, P_{avs} is the average power available from the source, and R_o is the output impedance of the cascoded NMOS transistors. ω_T and ω_0 are the unity-gain frequency of the MOS transistor and the frequency of input RF signal, respectively.

Ideally, if the impedance of the ESD protection device (Z_{ESD}) can approach to infinite, the power gain and noise figure of the RF LNA with ESD protection devices can be converged to those of a pure RF LNA without ESD protection devices. However, even though the ESD diodes are operated in the forward-biased condition to discharge ESD current with the help of the active power-rail ESD clamp circuit, such ESD diodes still have to be realized with some finite device dimensions to sustain the desired ESD level. The parasitic capacitance and resistance of the ESD diodes, even with limited device sizes, still generate the Z_{ESD} into above equations.

To practically investigate the negative impacts caused by the ESD diode on RF performance, three shallow-trench-isolation (STI) diodes with different device dimensions had been fabricated in a 0.25-μm CMOS process [20]. The layout top view of a unit cell of the STI diode is shown in Fig. 4(a), where it is an N+/P-well diode. The N+ diffusion (cathode) and P+ diffusion (anode) are separated by the STI. In Fig. 4(a), X is the length of the N+ diffusion, S is the spacing between N+ diffusion and P+ diffusion, and W is the width of the N+ diffusion. The device parameters of X =

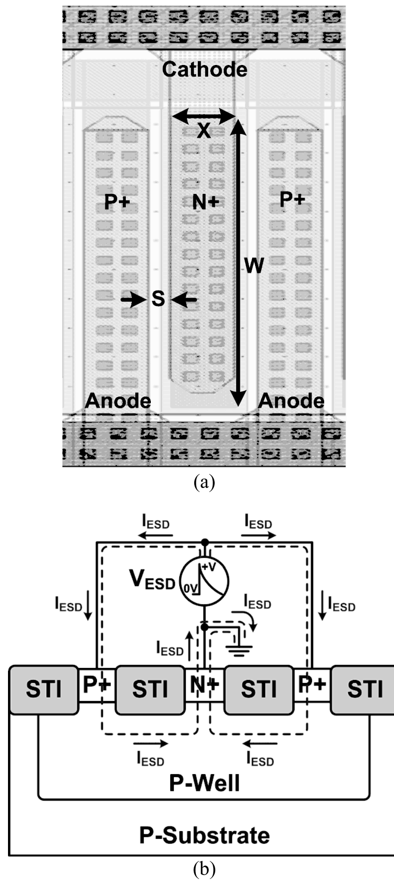


Fig. 4 (a) Layout top view and (b) cross-sectional view of the N+/P-well shallow-trench-isolation (STI) diode.

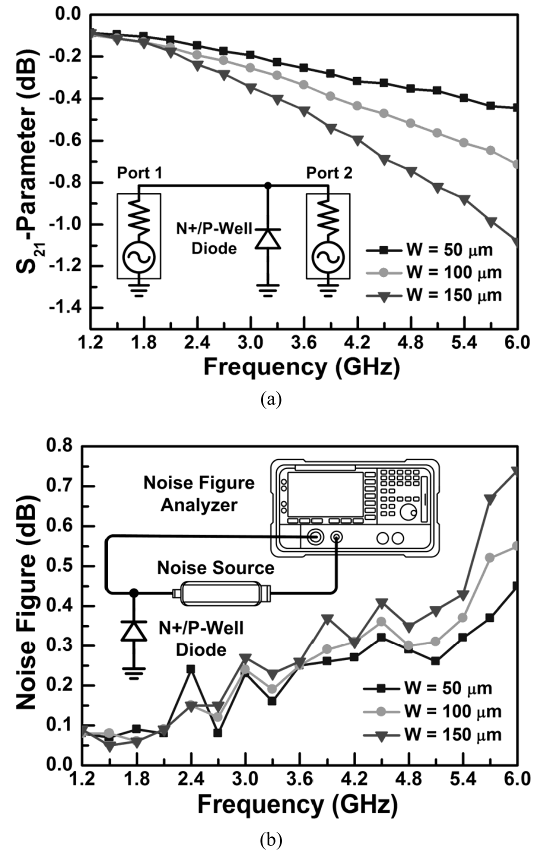


Fig. 5 Measured (a) power gains (S_{21}-parameters) and (b) noise figures of STI diodes with different device dimensions.

1.5 μm, S = 0.52 μm, and W = 50 μm, 100 μm, and 150 μm were used in this experiment. The N+/P-well diodes with different N+ diffusion widths were fabricated in the test chip to investigate their impacts on power gain and noise figure. The cross-sectional view of a unit cell of the STI diode is shown in Fig. 4(b). With the help of power-rail ESD clamp circuit, ESD current in the diodes under forward-biased condition is shown by the dashed line in Fig. 4(b), where the ESD current flows from P+ diffusion to N+ diffusion.

The S-parameter and noise figure measurement system have been used to measure the power gain (S_{21}-parameter) and noise figure. The measured power gains and noise figures of the STI diodes with different device dimensions in the frequency band of 1.2–6 GHz are compared in Fig. 5(a) and (b), respectively. The measurement setups of S-parameter and noise figure measurements are also illustrated in Figs. 5(a) and (b), respectively. The power gain of the STI diode with the same device dimension is decreased when the operating frequency increases. The power gain is decreased drastically by the STI diodes with larger device dimensions in higher frequency bands. The differences of the power gain loss of the STI diodes between different device dimensions become larger in higher frequency bands. This demonstrated that the parasitic capacitance of the ESD protection device (C_{ESD}) losses RF signal to ground and degrades power gain. This has confirmed the negative impacts caused by the ESD diodes on RF performance.

As the operating frequency of RF circuits increases, the impedance of the ESD protection device seen from the RF input port to ground ($Z_{ESD} = 1/j\omega C_{ESD}$) will be decreased. As Z_{ESD} decreases, the transducer power gain in (4) will decrease and the noise figure will increase. Since Z_{ESD} can not approach to infinity in actual RF LNAs with any ESD protection circuit, on-chip ESD protection circuits will degrade the performance of RF LNAs, especially in higher frequency bands. Therefore, how to design an effective on-chip ESD protection circuit for RF circuits operating in higher frequency bands with minimum RF performance degradation is a challenge, which must be solved for safe mass production of RF ICs.

3. ESD Protection Design with Impedance-Isolation Technique

The power gain loss and noise figure contributed by ESD protection devices are strongly dependent on the parasitic effects of the ESD protection devices at the input port. If the parasitic effects of the input ESD devices can be blocked from the RF circuit, the power gain would ideally not be degraded. To provide nearly infinite impedance between the on-chip ESD protection device and RF input port un-

der normal circuit operating conditions, a novel impedance-isolation ESD protection design with LC-tank to block the parasitic effects of the ESD protection devices for RF applications is shown in Fig. 6. The LC-tank is inserted between the RF input pad and the ESD diodes, which is called as the **LCD** structure.

To avoid the ESD diodes operating in the breakdown condition during PS-mode (positive-to-VSS) and ND-mode (negative-to-VDD) ESD stresses, which leads to much lower ESD robustness, a turn-on efficient ESD clamp circuit is added between the power rails (VDD and VSS) in the ESD protection circuit [12]. Since the ESD current is discharged through the forward-biased P+/N-well diode D_{P1} (N+/P-well diode D_{N1}), thick metal inductor, and the power-rail ESD clamp circuit under the PS-mode (ND-mode) ESD stresses, the ESD robustness can be high enough to protect the internal RF circuits.

The LC-tank is designed to resonate at the operating frequency of the RF circuit. Therefore, the RF input port will ideally see infinite impedance from the ESD protection devices with the LC-tank, which resonates at the operating frequency of the RF circuit. The inductance and capacitance in the LC-tank can be determined from the resonant frequency of

$$\omega_0 = \sqrt{\frac{1}{LC}}. \tag{5}$$

Once the operating frequency of the core RF circuit is determined, the resonant frequency of the LC-tank is determined, namely, the product of inductance and capacitance in the LC-tank is determined to be a constant. Moreover, as the operating frequency of the core RF circuit increases, the resonant frequency of the LC-tank increases correspondingly. Therefore, the inductance and the capacitance in the LC-tank decrease as the operating frequency of the RF circuit increases. With consideration of the parasitic effects of the inductor and capacitor realized in the silicon chip, the values of inductance and capacitance in the LC-tank with the same resonant frequency (demonstrated at 2.7 GHz in this work) have been implemented with several pairs which were realized with different device dimensions to investigate the overall performance. The LC-tanks with the same resonant frequency of 2.7 GHz, but realized with different inductances and capacitances are listed in Table 1, which have been designed and fabricated in a 0.25-μm CMOS process with thick top-layer metal to realize the on-chip inductors.

Since the ESD protection device and the LC-tank are in series connection from the input pad to the AC ground node in the LCD structure, the configuration of ESD protection circuit with LC-tank can be altered. The second design is the DLC structure which is shown in Fig. 7, where the LC-tank is inserted between the ESD diodes and the VDD or VSS power rail. In order to stack the LC-tank and the N+/P-well diode D_{N1}, a deep N-well is used to isolate the P-well of D_{N1} from the common P-type substrate.

The test chips to realize the proposed impedance-isolation technique for RF ESD protection have been designed and fabricated with different diode dimensions (for D_{N1} and D_{P1}) and different inductances and capacitances

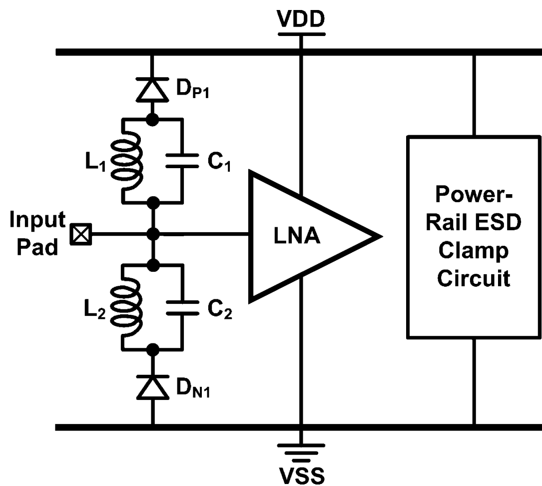


Fig. 6 Proposed impedance-isolation ESD protection design with LC-tank (called as the LCD structure).

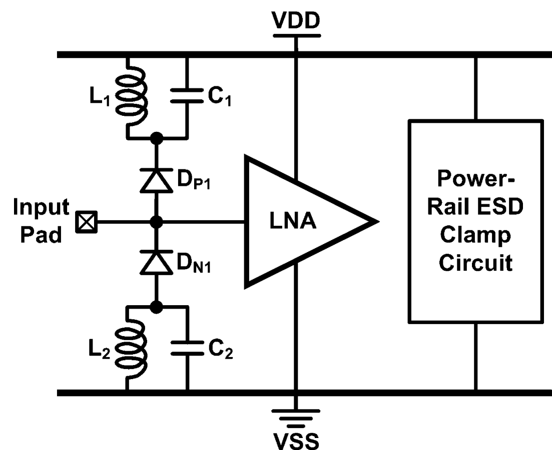


Fig. 7 Proposed impedance-isolation ESD protection design with LC-tank (called as the DLC structure).

Table 1 Dimensions of inductors and capacitors used in LC-Tanks.

	1	2	3	4	5
Inductor	12.12 nH (6.5 Turns)	8.64 nH (5.5 Turns)	5.88 nH (4.5 Turns)	3.74 nH (3.5 Turns)	2.17 nH (2.5 Turns)
Capacitor	219 fF (14.8 μm × 14.9 μm)	361 fF (19 μm × 19 μm)	596 fF (24.4 μm × 24.4 μm)	999 fF (31.6 μm × 31.6 μm)	1731 fF (41.6 μm × 41.6 μm)

Table 2 Layout dimensions of ESD diodes with different parasitic capacitances.

Total Capacitance	200 fF			600 fF			1200 fF		
Dimension	W (μm)	X (μm)	Finger Number	W (μm)	X (μm)	Finger Number	W (μm)	X (μm)	Finger Number
D_{N1}	21.38	3.2	1	21.38	3.2	3	21.38	3.2	6
D_{P1}	22	3.2	1	22	3.2	3	22	3.2	6

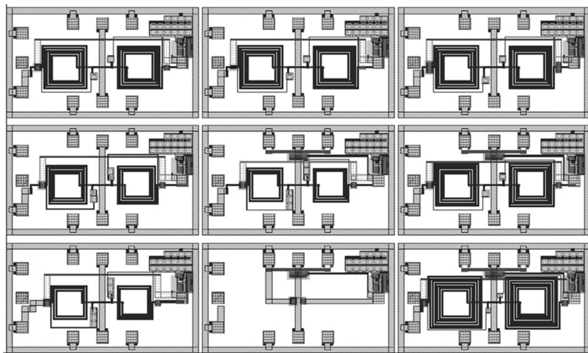


Fig. 8 Part of the layout top view of the ESD protection circuits with and without LC-tank.

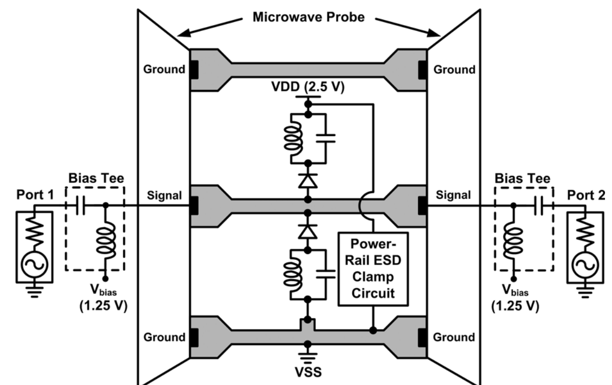


Fig. 9 Experimental setup to measure the power gain and noise figure of the fabricated ESD protection circuit with LC-tank.

(but with the same resonant frequency of 2.7 GHz). The measured results will be shown and discussed in the next section.

4. Experimental Results

The proposed impedance-isolation ESD protection circuits with different combinations of LC-tanks have been designed and fabricated in a 0.25-μm CMOS process with thick top-layer metal for both LCD and DLC structures. The power-rail ESD clamp circuit has been applied to achieve comprehensive whole-chip ESD protection. The ESD diodes (D_{N1} and D_{P1}) have been implemented in different device dimensions with the parasitic capacitances of 100 fF, 300 fF, and 600 fF for each diode. The layout dimensions of the diodes D_{P1} and D_{N1} with different parasitic capacitances, calculated from the SPICE parameters, are shown in Table 2. The conventional ESD protection circuit without LC-tank was also fabricated in the same process for comparison. Part of the layout top view is shown in Fig. 8. The area penalty of the proposed ESD protection circuit with LC-tank is dominated by the on-chip spiral inductor.

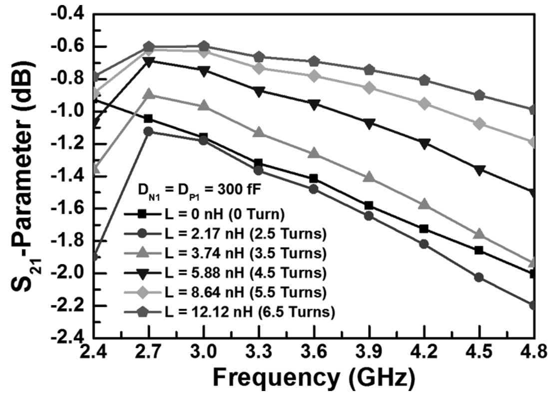
The experimental setup to measure power gain and noise figure is shown in Fig. 9. Ground-signal-ground (G-S-G) pads were adopted to facilitate on-wafer measurement. The dummy pads in G-S-G layout pattern were also fabricated in the test chip to de-embed the parasitic effects of the pads. The RF performances of power gain and noise figure of the fabricated LC-tank ESD protection circuits have been investigated by two-port on-wafer measurement. The ESD robustness of the fabricated LC-tank ESD protection circuits have been verified in both human-body-model (HBM) and machine-model (MM) ESD tests.

4.1 Power Gain

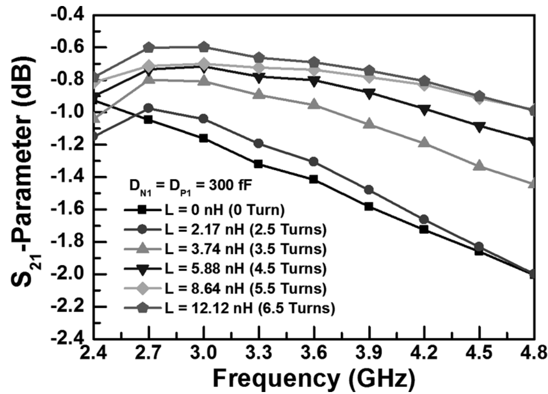
The measured power gains (S_{21}-parameters) of the LC-tank ESD protection circuits under LCD and DLC structures with different inductances in the frequency band of 2.4–4.8 GHz are shown in Figs. 10(a) and (b), respectively. The lines of L = 0 nH (0 turn) in Fig. 10 denote that the ESD diodes were not blocked by the LC-tank, which is the conventional ESD protection design shown in Fig. 1 as a reference. Each diode (D_{N1} or D_{P1}) in Fig. 10 has the parasitic capacitance of 300 fF. The measured results have shown that the power gain loss becomes smaller when the inductance in the LC-tank is larger. At 2.7 GHz, the power gain is improved from −1.05 dB (without LC-tank) to −0.6 dB (with LCD structure, L = 12.12 nH).

When the ESD diodes were implemented with different parasitic capacitances, the comparison among the power gain losses (at 2.7 GHz) of the proposed ESD protection designs with LC-tanks and the conventional structure (without LC-tank, as shown in Fig. 1) are shown in Fig. 11. When the total parasitic capacitance of the ESD diodes is increased, the power gain is seriously degraded. However, the degradation of the power gain can be mitigated by adding the LC-tanks into the ESD protection circuits. When larger ESD diodes were used, the power gain can be significantly improved by using the proposed ESD protection circuit with the LCD structure. This has demonstrated that the impedance-isolation technique can successfully block most parasitic effects of the ESD diodes.

In an LC-tank, different inductor and capacitor can be designed to achieve the same resonant frequency as long as



(a)



(b)

Fig. 10 Measured power gains of the impedance-isolation ESD protection circuits with different inductances using the (a) LCD structure and (b) DLC structure.

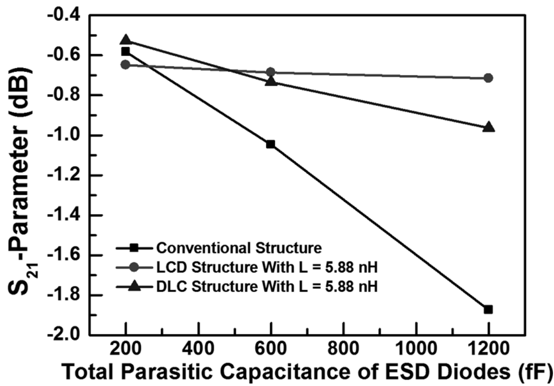


Fig. 11 Comparison among the power gains of the impedance-isolation ESD protection circuits with LCD structure, DLC structure and the conventional structure without LC-tank at 2.7 GHz.

the product of inductance and capacitance is identical. In CMOS processes, the quality factor of the on-chip spiral inductor is significantly less than that of the capacitor. Therefore, the parasitic series resistance of the inductor should be taken into consideration during the analysis of LC-tank. An LC-tank composed of inductor with parasitic series resistance is illustrated in Fig. 12(a). C is the capacitance, L_s is

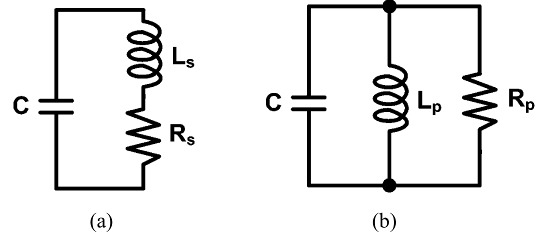


Fig. 12 (a) LC-tank composed of inductor with parasitic series resistance. (b) Equivalent parallel RLC network of LC-tank near the resonant frequency.

the inductance of the inductor and R_s is the parasitic series resistance of the inductor. To facilitate the analysis, the LC-tank can be transformed into a purely parallel RLC network near the resonant frequency, as shown in Fig. 12(b). The parallel inductance L_p and resistance R_p can be expressed by L_s, R_s, and the quality factor (Q) of the inductor, respectively:

$$Q = \frac{\omega L_s}{R_s} \tag{6}$$

$$L_p = L_s\left(\frac{Q^2+1}{Q^2}\right) \tag{7}$$

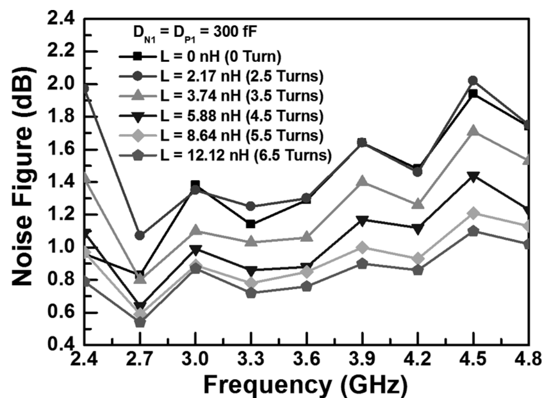
$$R_p = R_s\left(Q^2+1\right) \approx \frac{\omega^2 L_s^2}{R_s}. \tag{8}$$

Near the resonant frequency, the total impedance of C and L_p becomes very large and can be neglected. The remaining impedance of the LC-tank is only R_p. The power gain loss is reduced with larger R_p because of the larger impedance to the AC ground node. The inductor with larger inductance has larger R_p due to the square relationship between R_p and L_s. Thus, the power gain loss becomes smaller when the inductance in the LC-tank with the same resonant frequency is larger.

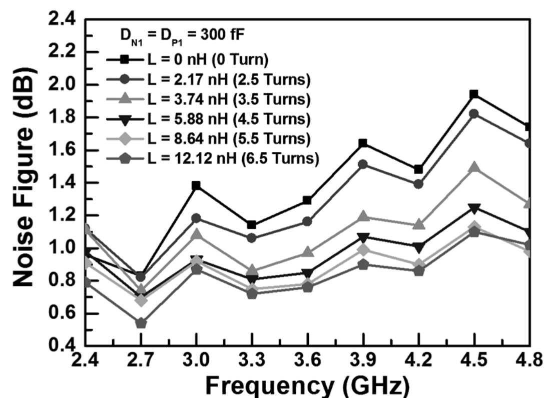
4.2 Noise Figure

The measured noise figures among the fabricated ESD protection circuits with different inductances in the LC-tank are compared in Figs. 13(a) and (b) under the LCD and DLC structures, respectively. The line of L = 0 nH (0 turn) is the conventional ESD protection design shown in Fig. 1 as a reference. The noise figures of the proposed ESD protection circuits with LC-tanks are smaller than those of the conventional ESD protection circuits without LC-tanks. All ESD diodes (D_{N1} and D_{P1}) were implemented with the parasitic capacitance of 300 fF in the ESD protection circuits. At 2.7 GHz, the noise figure of the ESD protection circuit is decreased from 0.83 dB (without LC-tank) to 0.54 dB (with LCD structure, L = 12.12 nH).

The comparison among the noise figures (at 2.7 GHz) of the proposed RF ESD protection designs with LC-tanks and the conventional structure without LC-tank under different total parasitic capacitances of ESD diodes are shown in Fig. 14. According to Fig. 14, the noise figure increases



(a)



(b)

Fig. 13 Measured noise figures of the impedance-isolation ESD protection circuits with different inductances using the (a) LCD structure and (b) DLC structure.

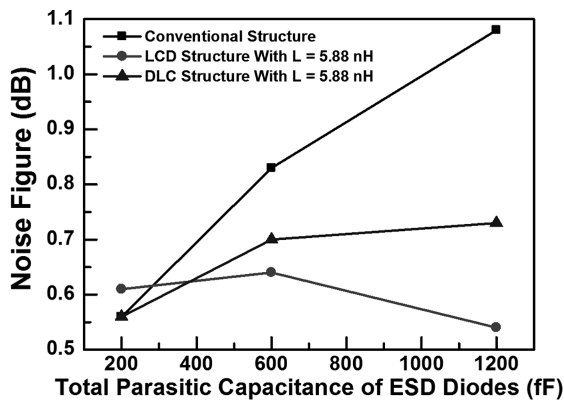
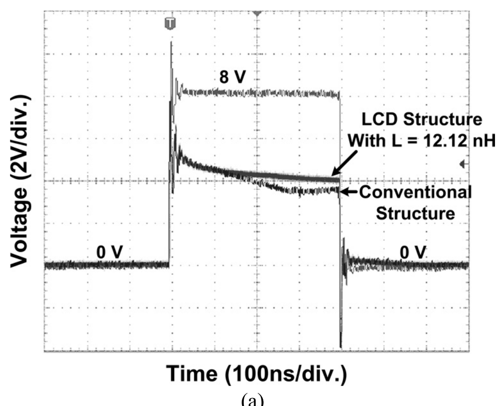
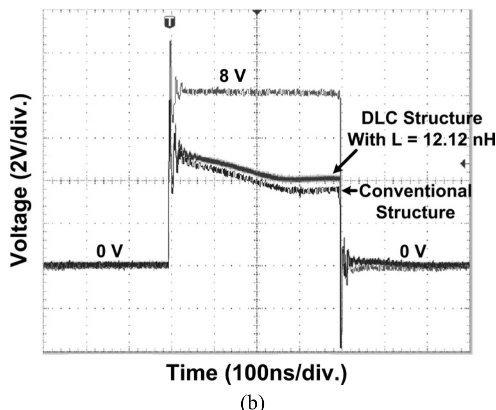


Fig. 14 Comparison among the noise figures of the impedance-isolation ESD protection circuits with LCD structure, DLC structure and the conventional structure without LC-tank at 2.7 GHz.

when the total parasitic capacitance of the ESD diodes is increased. Although the ESD robustness of the RF input pin can be improved with larger ESD diodes, the noise figure is degraded. The increase in the noise figure can be mitigated by adding the LC-tanks into the ESD protection circuits. The LCD structure has a lower noise figure than that of the DLC structure because the DLC structure has



(a)



(b)

Fig. 15 Turn-on verification of the impedance-isolation ESD protection circuit under PS-mode ESD test. (a) The voltage waveform on the input pad clamped by the LCD structure. (b) The voltage waveform on the input pad clamped by the DLC structure.

the diodes directly connected to the RF input pad. The extra parasitic capacitances from the deep N-well/P-substrate junction in D_{N1} and from the N-well/P-substrate junction in D_{P1} slightly increase the noise figure of the DLC structure.

The ESD protection circuit in this work can be viewed as a two-port network. For a passive two-port network, the noise figure is closely correlated to the power gain loss. The ESD protection circuits have smaller power gain loss have lower noise figure. As expected, measured results showed that the proposed ESD protection circuit has larger inductance in the LC-tank has smaller power gain loss and lower noise figure. The improvement on noise figure is attributed to the parasitic series resistance of the on-chip spiral inductor. The inductor with larger inductance has larger parasitic series resistance, which leads to larger impedance from the RF input pad to the AC ground nodes. Therefore, the power gain loss and the noise figure are improved with larger inductance in the LC-tank. Since the noise figure of the conventional ESD protection with 600-fF parasitic capacitance is only 0.83 dB, the improvement on noise figure is not significant (noise figure is 0.54 dB with LCD structure and 12.12 nH inductance). The improvement on noise figure will become more significant if ESD protection devices with larger parasitic capacitances are used.

Table 3 ESD levels of the conventional ESD protection circuits without LC-tank.

	PD-Mode		NS-Mode		PS-Mode		ND-Mode	
C_{diodes} (fF)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)
600	> 8000	625	> 8000	850	6700	550	> 8000	800
1200	> 8000	750	> 8000	1325	> 8000	650	> 8000	1150

Table 4 ESD levels of the proposed ESD protection circuits with LCD structure.

LCD ESD Protection Circuit			PD-Mode		NS-Mode		PS-Mode		ND-Mode	
C_{diodes} (fF)	L (Turns)	C (fF)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)
600	3.5	999	4000	400	6800	700	2500	225	6000	350
600	4.5	596	3400	375	6600	650	2000	200	5200	275
600	5.5	361	3200	300	6400	650	1600	175	4600	225
600	6.5	219	2800	300	6000	625	1400	150	3900	200
200	4.5	596	3000	300	4300	500	1600	125	3000	200
1200	4.5	596	3800	325	8000	775	2700	200	6300	325

4.3 Turn-On Verification

To verify the turn-on efficiency of the proposed LC-tank ESD protection circuit in PS-mode ESD tests, a voltage pulse was applied to the RF input pin, whereas the VSS pin was relatively grounded and the VDD pin was floating. With an 8-V voltage pulse with a rise time of 2 ns applied to the RF input pin, the turn-on efficiency of the LC-tank ESD protection circuit can be clearly verified. While such a positive voltage pulse was applied to the RF input pin, the overstress voltage at the RF input pin was clamped by the proposed LC-tank ESD protection circuits with LCD and DLC structures, as shown in Figs. 15(a) and (b), respectively. The inductor in the LC-tank did not increase the turn-on time. Only the clamping voltage was slightly increased in the LC-tank ESD protection circuits.

According to the experimental results, the voltage pulses were clamped by the proposed ESD protection circuits with LCD and DLC structures. During ESD stresses, diodes D_{N1} and D_{P1} were in the forward-biased condition rather than the reverse-biased breakdown condition, which leads to much higher ESD robustness.

4.4 ESD Robustness

When the proposed ESD protection circuit with the LCD structure was under ESD-stress conditions, Fig. 6 can be used to illustrate the mechanism. In the positive-to-VDD mode (PD-mode) ESD test, the input pad was zapped with a positive voltage pulse while the VDD pin was relatively grounded. During PD-mode ESD stresses, ESD current flows from the input pad through L_1 and D_{P1} to the VDD pin. For the same reason, in the negative-to-VSS mode (NS-mode) ESD test, the input pad was zapped with a negative voltage pulse while the VSS pin was relatively grounded. During NS-mode ESD stresses, ESD current (in the viewpoint of positive charge) flows from the VSS pin through D_{N1} and L_2 to the input pad.

In the positive-to-VSS mode (PS-mode) ESD test, the input pad was zapped with a positive voltage pulse while the VSS pin was relatively grounded. During PS-mode ESD stresses, ESD current flows from the input pad through L_1 and D_{P1} to the VDD power rail, and finally through the power-rail ESD clamp circuit to the grounded VSS pin. For the same reason, in the negative-to-VDD mode (ND-mode) ESD test, the input pad was zapped with a negative voltage pulse while the VDD pin was relatively grounded. During ND-mode ESD stresses, ESD current (in the viewpoint of positive charge) flows from the VDD pin through the power-rail ESD clamp circuit to the VSS power rail, and finally through D_{N1} and L_2 to the input pad.

Obviously, the ESD current paths in PS-mode and ND-mode ESD tests are longer than those in PD-mode and NS-mode ESD tests. Thus the PS-mode and ND-mode ESD tests are the critical modes for applying positive and negative voltage pulses to the input pad, respectively.

The PD-, NS-, PS-, and ND-mode HBM and MM ESD levels on the conventional ESD protection circuits without LC-tank, as well as the proposed ESD protection circuits with LCD and DLC structures under different diode capacitances and inductor turns are summarized in Tables 3, 4, and 5, respectively. The failure criterion for ESD robustness of the ESD protection circuit was defined as the corresponding voltage at 1 μA current to the grounded VDD and VSS pins shifting 30% from its original value. All the LC-tanks were designed with the same resonant frequency of 2.7 GHz. The total parasitic capacitances (C_{diodes}) of the ESD diodes (D_{N1} and D_{P1}) were 200 fF, 600 fF, and 1200 fF to verify their corresponding ESD robustness. The dimensions for such diodes in a 0.25-μm CMOS process are shown in Table 2. The I-V curves of the RF input pin with the LCD structure before and after three positive-to-VSS ESD stresses are compared in Fig. 16, where the currents were measured with both VDD and VSS pins grounded.

Table 5 ESD levels of the proposed ESD protection circuits with DLC structure.

DLC ESD Protection Circuit			PD-Mode		NS-Mode		PS-Mode		ND-Mode	
C_{diodes} (fF)	L (Turns)	C (fF)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)	HBM (V)	MM (V)
600	3.5	999	4200	400	7500	475	2200	225	3700	350
600	4.5	596	3400	325	6300	375	2000	200	3000	300
600	5.5	361	2900	300	5100	325	1900	175	2500	200
600	6.5	219	2400	225	4500	300	1600	150	2100	200
200	4.5	596	3000	250	2900	350	1700	125	2700	200
1200	4.5	596	3300	375	7500	475	2400	200	3500	300

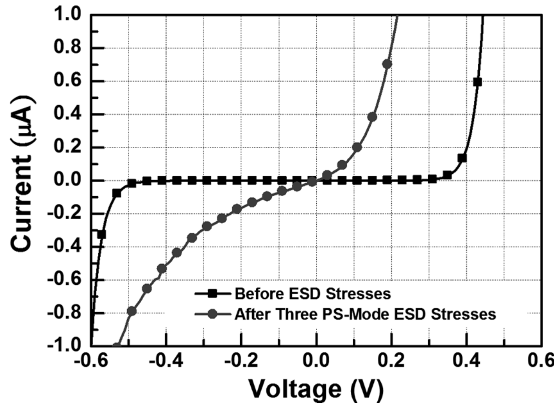


Fig. 16 I-V curves of the RF input pin with LCD ESD protection circuit before and after positive-to-VSS (PS-mode) ESD stresses. The currents were measured with both VDD and VSS pins grounded.

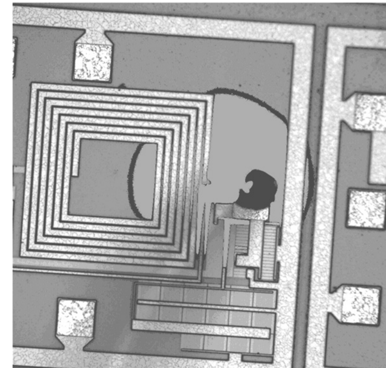


Fig. 18 EMMI photograph to show the failure location in the ESD protection circuit with LCD structure after positive-to-VSS (PS-mode) ESD stresses. The ESD damage is located on the DP1 diode.

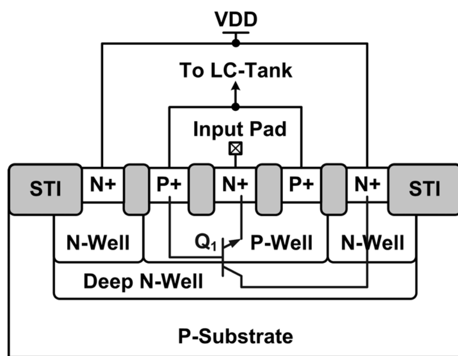


Fig. 17 Cross-sectional view of diode D_{N1} in DLC structure.

From the measured results in Tables 4 and 5, using more turns to realize the inductor in LC-tanks leads to lower HBM and MM ESD levels under the same parasitic capacitance (600 fF) of the ESD diodes. When the inductor in LC-tank is kept as 4.5 turns in layout, the HBM and MM ESD levels of the proposed ESD protection circuit can be increased by increasing the dimensions of the ESD diodes, which are indicated as C_{diodes} in Tables 4 and 5.

In the NS-mode (ND-mode) ESD test, the input pad is stressed by a negative ESD pulse, whereas the VSS (VDD) pad is grounded. The expected ESD current path in the LCD (DLC) structure under NS-mode ESD test is through L_2 and D_{N1} (D_{N1} and L_2). The expected ESD current path in the LCD (DLC) structure under ND-mode ESD test is through L_2, D_{N1}, and the power-rail ESD clamp circuit (D_{N1}, L_2, and the power-rail ESD clamp circuit). The P-well of the N+/P-well diode D_{N1} in the LCD structure is connected to VSS, so the ESD current flow through the expected paths under NS-mode and NS-mode ESD tests. Since the anode of D_{N1} is not connected to VSS in the DLC structure, the deep N-well is necessary to isolate the P-well of D_{N1} from the common P-substrate. As shown in Fig. 17, a parasitic NPN BJT Q_1 exists in D_{N1}, which is formed by N+ diffusion, P-well, and deep N-well. In the expected ESD current, the series resistance of the inductor increases the holding voltage. Therefore, Q_1 is turned on instead of the expected ESD current path due to the lower holding voltage under ND-mode ESD test. The size of Q_1 is not very large, so the ND-mode ESD level of DLC structure is lower than that of the LCD structure. During the NS-mode ESD test, the ESD current path is through the parasitic PN-junction from VSS to VDD and Q_1. Because the ESD current does not flow through the expected path, the NS-mode ESD level of the DLC structure is less than that of the LCD structure.

To find the failure location, the PS-mode ESD-zapped RF input pin was observed under the VDD bias of 2.5 V and the input bias of 0 V. A photon emission microscope (EMMI) was used to find the location of hot spots. The observed EMMI picture on the ESD protection circuit with the LCD structure after PS-mode ESD stresses is shown in Fig. 18, where the hot spot is located on the D_{P1} diode, not on the D_{N1} diode. The failure is due to the contact spiking from the P+ diffusion of the D_{P1} diode to the N-well.

This implies that under PS-mode ESD stresses, ESD current is conducted from the RF input pin to VDD through the LC-tank and D_{P1}, and then discharged from VDD to VSS through the active power-rail ESD clamp circuit. To reduce the parasitic capacitances of D_{P1} and D_{N1}, the layout clearance from the contact of P+ diffusion in N-well for D_{P1} (N+ diffusion in P-well for D_{N1}) to the PN junction edge was kept small. The small clearance in D_{P1} causes contact spiking during ESD stresses, as shown in Fig. 18.

5. Conclusion

The on-chip ESD protection design with impedance-isolation technique to block the parasitic effects of the ESD protection devices for giga-Hz RF applications has been proposed and successfully verified in a 0.25-μm CMOS process. The impedance-isolation concept realized by the LC-tank was designed to resonate at the operating frequency of the RF circuit and used to generate (ideally) infinite impedance of open circuit to isolate the parasitic capacitance of the ESD device. To meet the requirement of 2-kV HBM and 200-V MM ESD robustness, ESD diodes with 600 fF parasitic capacitance and the LC-tank with 5.88 nH inductance in the proposed impedance-isolation RF ESD protection circuit is preferred. For the RF performance, the preferred design has the power gain loss of only 0.69 dB and noise figure of only 0.63 dB at the resonant frequency of 2.7 GHz. The proposed ESD protection design with impedance-isolation technique has been successfully verified to achieve both good RF performance and high ESD robustness.

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