連續波固態綠光雷射退火之面板型類磊晶矽電晶體

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摘要

本論文主要探討與展示用連續波綠光雷射退火於非矽基基材上製作類磊晶電晶體之電特性與可靠度增益特性，這對於主動式開關電路、非揮發性記憶體、影像感測器與光偵測放大器等各式面板及與光積體線路具非常大之貢獻。本論文主要探討以下四個研究部分。

首先，研究發現連續波綠光雷射退火所製作類單晶之薄膜電晶體電性特徵與缺陷密度非常相關。隨雷射能量的提高其通道結晶性也隨之增加，結果發現通道缺陷密度隨著雷射退火能量提高而降低至 3×10^{19} $eV^{-1}cm^{-3}$，這符合通道缺陷密度降低而提高場效電子遷移率至 $284cm^2/Vs$，然而，提高雷射能最初降低深態位密度(deep-state density)，但隨後升至 $3\times10^{16}eV^{-1}cm^{-3}$。深態位密度的反轉是受雷射結晶增加其表面粗糙度而產生額外表面態缺陷所導致，其亦造成次臨界斜率提高與臨界電壓具飽和狀的降低趨勢。

下一步，我們利用連續波固態綠光雷射退火製作類單晶之高電洞載子遷移率之薄膜電晶體並探討其熱載子效應行為。當通道層變厚，雷射退火導致通道結晶性增加，然而也增加其表面粗糙度。由於此類磊晶之複晶矽薄膜有較厚通道時，雖然具較少通道缺陷密度，然而增及其表面粗糙度。在這樣類磊晶複晶矽基材，厚通道雖具較低之通道缺陷但也有差的表面品質，在熱載子效應作用下，造成較多之電荷陷阱(charge trapping)進而產生更多之深態位之通道缺陷密度(deep-state density of grain traps)，因此，薄通道 (50

nm) 之薄膜電晶體，因具有平整之表面，使得熱載子難以劣化元件特性。

第三，利用背向連續波固態雷射活化源極汲極區來獲得高電洞載子遷移率與可靠度之類磊晶之電晶體與於玻璃基板上。綠光雷射能量是均勻的跨過源、汲極與通道之介面，並不受閘極層之影響，並企圖達到超可見光側向活化。電特性效能的提升在於側向活化可以連續修補汲/源極與通道之介面，雷射活化能量亦可以降低通道缺陷密度且幾乎不增加表面缺陷密度，因此本研究也獲得超高之 P 型電晶體遷移率達 403cm^2/Vs，為傳統快速熱退火活化之兩倍大。

第四，探討正向連續波固態綠光雷射活化並製作面板電晶體。對於在自對準複晶矽閘極之薄膜電晶體結構，由於綠光雷射在複晶矽中具有長的穿透深度因此雷射能量將能有效的穿透複晶矽閘極。綠光雷射能量能不易受閘極所影響而均勻，且於次毫秒時間內，側向活化通道與源、汲極區，反之亦然。在綠光雷射活化的薄膜電晶體中，這樣快速的綠光雷射退火可獲得低外部阻抗與近乎連續的改善複晶矽結構來降低通道中之缺陷。利用連續波固態雷射正向退火活化技術可於相同雷射退火結晶之 100nm 之高結晶通道上製造出一個具有非常可觀的電子遷移率為 530cm^2/Vs 與陡峭的次臨界斜率為 120mV/dev 之電晶體。正向連續波雷射活化方式也可成功製作具氮化鈦金屬閘極結構之電晶體，其電子遷移率為 230cm^2/Vs。在金屬閘極面板電晶體中，正向連續波綠光雷射活化，由於雷射光受金屬反射，因而可選擇性的活化源汲極區，使金屬閘極下之材料僅受微小之熱損傷，因此能確保先進面板及光積體線路中之電晶體元件內嵌入複合物、奈米結構化、功能性介電層或複晶矽材料之發展。

未來可將這些連續波綠光雷射退火製造電晶體引入至面板光感應器、記憶體與奈米光積體線路元件上。

Continuous-wave solid-state green laser annealing in panel epi-like silicon transistors

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Abstract

This dissertation explores and demonstrates enhanced electrical characteristics and reliability of continuous-wave green laser fabricated epi-like silicon transistors on non-silicon substrates, which greatly impacts on active-matrix no/off circuits, nonvolatile memories, linear image sensors, and photo-detector amplifiers for various panels and photonic circuits. The main focus of this dissertation can be divided into four parts.

First, electrical characteristics of continuous-wave (CW) green laser-annealed single-grainlike silicon thin-film transistors in relation to trap-state densities were characterized. As laser power increases, highly crystalline channels form, reducing tail-state densities to as low as $3x10^{19}$ $eV^{-1}cm^{-3}$. This occurrence is responsible for high field-effect electron mobility of 284 cm^2/Vs. In contrast, increasing laser power initially reduces the deep-state density and then increases it to $3x10^{16}$ $eV^{-1}cm^{-3}$. This reversal in deep-state density, and thus in the subthreshold slope, as well as a saturating reduction in threshold voltage are associated with the formation of extra interface defects caused by laser-crystallization-enhanced surface roughness.

Next, stability of high hole-mobility thin-film transistors (TFTs) on single-grainlike silicon channels formed by CW laser-crystallization (CLC) during hot-carrier stressing (***HCS***) was studied. As channel layers become thicker, laser-mediated channel crystallinity

increases, increasing channel roughness. On such epi-like polycrystalline silicon (poly-Si) substrates, the poorer interface quality for thicker channels, even those with lower tail-state densities of grain traps, is responsible for the extensive charge trapping and creation of deep-state densities in the fabricated TFTs due to ***HCS***. Hence, on a thin channel with a thickness of 50 nm and ultra-smooth surfaces, ***HCS*** hardly degrades the electrical parameters of the devices.

Third, the hole-mobility and reliability of green CW laser-crystallized epi-like Si transistors on glass panel substrates were enhanced by source/drain activation by back-side green laser-irradiation. Green laser-energy was scanned uniformly across junctions, since the gate structures included no interrupt, in an attempt to conduct super visible-laser lateral-activation. The enhancement was thus explained by the formation of continuous improved epi-like Si microstructures with reduced grain defects and with a barely increased number of interface defects over the entire channel/junction. The hole-mobility in such laser-activated devices was as high as 403 $cm^2/V.s$ – doubles that of thermally activated devices.

Fourth, panel transistors were activated by front-side CW green laser irradiation. In self-aligned poly-Si TFTs, significant laser-energy penetrates through poly-Si gates owing to the considerably long penetration depth of green light in poly-Si. Green laser-energy was thus uniformly scanned laterally from channels to source/drain regions and, vice versa, in under a millisecond, hardly affected by gate structures. Such spike green-laser annealing yields low parasitic source/drain resistance and quasi-continuous improved poly-Si microstructures in green laser-activated TFTs, with reduced grain defects over the entire channel/junction. Electron-mobility and sub-threshold slope for such transistors that were fabricated on CLC channels of 100 nm, were remarkable values of 530 $cm^2/V.s$ and 120 mV/dec, respectively. In gate structures of TiN/SiO_2, laser-activated panel transistors that were fabricated on CLC channels of 100 nm, also revealed electron-mobility as high as 230 $cm^2/V.s$. In metal gated panel transistors, front-side CW green laser irradiation intrinsically

activates source/drain regions selectively, because of light reflection by metal gates, causes little thermal damage on materials underneath metal gates, which endorses advanced panel or photonic transistors with compound, nanostructured, and functionalized gate dielectrics or polycrystalline materials.

In future, those CW green laser-fabricated transistors will be routines for the development of panel photo-sensors and memories, as well as nano-photonic circuits.

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四年多，赤裸裸的博士班研究生活，終於在無盡的血淚中渡過。在碩士班從高溫腐蝕的研究轉行來到半導體相關製程，“隔行如隔山”這句話果真沒錯，但卻因如此也讓我在交大這幾年的博士班研究生活更多采多姿。記得老闆 陳智 教授曾說過，博士就是從不懂到懂，再從懂變成專家，雖是短短的幾句話，但裡面的涵意與過程卻是要克服許許多多的困難與靠大家的努力幫忙才有辦法完成。首先，感謝的包含陳智 教授給我了這一個薄膜電晶體相關研究的學習機會，這對我在製程技術的成長與了解幫助非常大；也感謝國家奈米研究院 謝嘉民 博士在雷射退火與電性上提供寶貴的意見與建議；吳耀銓 教授在去日本開會的時候非常照顧；口試委員中交大光電所潘犀靈 教授在光學系統上的指導；交大顯示所蔡娟娟 教授與葉長青 博士對材料、系統與整合上的寶貴建議；明新科技大學電子所王木俊 教授在電性上的討論等，使得研究的內容與論文能更加的完整。

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Chapter 1

Introduction

1.1 Development trends of Polycrystalline silicon thin film transistors

Liquid crystal displays (LCD) are key components for information and video products. An active matrix LCD (AMLCD) as large as 57 inches in diagonal size has been developed using the technology of hydrogenated amorphous Si (a-Si) thin film transistor (TFT) in 2006 [1.1]. Compared with a-Si TFTs, polycrystalline silicon (poly-Si) TFTs demonstrated the feasibility of low-temperature fabrication, extreme high mobility of 10~400 cm^2/Vs [1.2]-[1.5] and device scaling, which essentially ensures poly-Si TFTs-based electric circuits and switchers on large-area and flexible substrates. Hence, poly-Si thin film transistors not only pay a role of active-matrix no/off circuit, but also widely apply in Nonvolatile memories, linear image sensor, and photo-dector amplifier with increment TFTs performance [1.6]-[1.12]. The traditional excimer laser crystallization (ELC) are performed in the air ambient environment at room temperature, however, the grain size is limited size below sub-micrometer. Therefore, there have reliability problems including of non-uniform grain size and transistor characteristics. For this reason, it will be more focused on crystallization technique like single grains. Table 1- I shows the forecast of advanced low-temperature poly-Si (LTPS) TFT technology. The current technology is the first stage, which integrates

both X and Y-drivers by using TFTs with mobility of 100 cm^2/Vs. The next-generation TFT will demonstrate mobility more than 300 cm^2/Vs by the technology of Grain Boundary-Less Channel (GBLC). The GBLC-TFT will realize "System Displays" that are embedded with integrated signal processor, graphic I/F and small scale memory [1.13].

1.2 Poly-Si films by excimer laser crystallization methods

In 1975, Shtyrkov et al. initiated pulsed laser annealing and reported the lattice damage due to implantation into crystalline silicon could be repaired as well as activated by laser annealing without extra thermal process [1.14]. Many researches on the use of pulsed laser annealing were conducted in the 1980s. Sussmann et al. first applied pulsed lasers to crystallize the a-Si-H films in 1980 [1.15]. Immediately, Sameshima et al. successively employed excimer laser to crystallize a-Si films on glass substrate [1.16]. Note that high-power XeCl excimer lasers, developed by the European masker SOPRA, have also been applied on poly-Si annealing [1.17]. In excimer laser annealing, pulse-to-pulse repeatability (PPR), which was sensitive to discharge frequency, output laser-energy and laser pulse duration, affects productivity and film quality critically. PPR in state-of-the-art laser equipments for Si-based annealing applications is in the range of 6-9% (3σ). The value is expected to decline further to ~4% within 3 years.

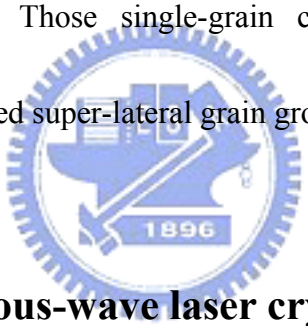
1.2.1 Crystallization mechanisms of ELA poly-Si

The lower laser fluence regime describes a condition where the incident laser fluence is

sufficient to induce melting of the a-Si film, but it is low enough that a continuous layer of Si remains at the maximum extent of melting. This regime is also referred to as "partial-melting regime" and obtains microcrystallities in the laser-crystallized Si film [1.18]. The high laser fluence regime corresponds to the situation when the laser fluence is sufficiently high to completely melt the Si film. The regime is also referred to as complete-melting regime. The mechanism of transformation in this regime related to the nucleation of solids within the liquid for the formation of a stable solid-liquid interface that can be accommodated the liquid-to solid conversion. The nucleation in the regime occurs as a result of undercooling in the molten-Si film. As a result of the copious nucleation that occurs within the undercooled molten-Si, the grain size obtained in the regime is about ten nanometers in diameter. A third regime has been found within a narrow process window between another two regimes. It is called super lateral grain growth (SLG). In general, the grain size in this regime is several hundred nanometers in diameter. The transformation process associated with this regime has been modeled by Im and others, in terms of near-complete-melting of Si films [1.19][1.20]. The practical implication of this model is that the unmelted islands provide solidification seeds, from which lateral growth can ensue, thus propagating the solid-liquid interface within the surrounding undercooled molted Si. In figure 1-1, SLG grain growth initiates from seeds, this survived the melting process, at the Si-SiO_2 interface [1.21].

1.2.2 Advanced ELA poly-Si technology

The drawbacks of conventional ELA process were related to difficulty in maintaining a proper balance between performance and process uniformity. PPR is hardly controlled [1.22], in response to worsened uniformity of ELA poly-Si TFTs. Another disadvantage in conventional poly-Si TFTs was what numerous grain boundaries in channels associated with small grains hinder carrier transportation and deteriorate TFT performance [1.23][1.24]. Recently, a few efforts attempt to demonstrate single-grain TFTs technologies by location-controlled crystal grains formed by excimer-laser-based sequential lateral solidification (SLS) [1.25], high-frequency pulse solid-state laser, and thin-beam directional X'tallization (TDX) [1.26]. Those single-grain crystallization technologies normally initialize efficiently laser-induced super-lateral grain growth.



1.3 Poly-Si by continuous-wave laser crystallization methods

Hara et al. in 2001 announced highly crystalline poly-Si films on large-area glass substrates by continuous-wave (CW) green laser crystallization (CLC) [1.27]. In CLC, power instability of diode pumped solid state (DPSS) CW laser (532nm (second harmonics (2ω) of Nd:YVO_4)) is less than 1%, which value is superior to that of XeCl excimer lasers and Ar lasers. Moreover, CLC processes were conduced at room temperature and in ambient environment. TFTs on such CLC poly-Si layers on glass substrates were fabricated at process temperature below 450℃; field-effect mobilities for n-channels and p-channels were as high as 566 cm^2/Vs and 200 cm^2/Vs, respectively.

CLC easily forms ~20 μm large grains and low roughness in crystallized layers, in a quite wide energy range as shown in Figure 1-3, because of continuous laser-energy supply, directional solidification caused by laser scanning, and slow cooling rate of molten Si due to the dwell time of laser beam is about 100μs during scanning.

In 2007, Ogawa et al. [1.28] introduced CLC technologies to perform a low power (~ 50mW) and high resolution (332ppi) VGA LCD with integrated 6-bit digital data drivers. Excellent uniformity in threshold voltage, as compared to that of conventional ELA-TFTs, is shown in Figure 1-4 and 1-5.

1.4 Laser-activated poly-Si TFTs

Future system-integrated-on-panel applications require a significant improvement in the performance of current poly-Si TFTs. The biggest leverage in circuit performance can be achieved by reducing channel length from the typical, 4-6μm to 1μm [1.29][1.30]. Rapid thermal annealing (RTA) and Spike RTA are conventional techniques which usually follow ion implantation to activate dopants in silicon layer. However, the ultra-shallow source/drain extensions (down to 10 nm), high doping (up to 10^{21} at/cm^3), and low sheet resistance (100Ω /sq), are very difficultly achieved by conventional techniques [1.31][1.32]. Moreover, for display panels on glass or even plastic substrates, the activation-fabrication temperature should be far below 600℃ [1.33]. Hence, ELA had been proposed as direct activation of dopants without heating the substrate [1.34]. However, laser activation suffers

from discontinuities and/ or residual damage in microstructure across junctions because of variations in laser energy that is scanned over the device bodies, which are caused by gate structure [1.35][1.36].

Consequently, a new and useful laser activation technology for high performance poly-Si TFTs was a concern in future.

1.5 Reliability issues in poly-Si TFTs

The continuous development of poly-Si TFTs was considered to construct high-speed circuits such as processors, memories, and drivers, etc. on non-silicon substrates, such that reliability of poly-Si TFTs, like transistors in integrated circuits on Si substrates, was also a concern. Poly-Si films consist of a high density of in-grain, grain boundary defects, and broken Si-H bonding so that stressed devices on poly-Si layers normally show significant degradation in electrical characteristics [1.37]-[1.40]. In addition, appropriate circuit and device design, the injection of energetic carriers into the gate insulator and subsequent parameter shift through carrier trapping and trap state generation poses one of the most significant long-term reliability concerns in the poly-Si TFTs. It has been known that the application of high drain voltage and a relatively high gate voltage (hot-carrier stressing, HCS) in poly-Si TFTs, decreases the maximum transconductance and causes the shift of turn-on voltage. Therefore, a systematical study of the poly-Si TFTs aging with stress time is required.

1.6 Motivation

As mentioned in the above sections, low temperature poly-Si TFTs have been considered for use in various three-dimensional circuits. However, for realization of a system on panels, the electrical characteristics of conventional excimer crystallized poly-Si TFTs is not insufficient due to hinder the carrier transport or large leakage current caused by trap-assisted carrier generation in defects. This problem can be solved only by fabricating the devices on silicon-on-insulator (SOI) substrates with separation-by-implantation-of-oxygen (SIMOX) technique. However, the major concerns of this technique are high temperatures (> 1300ºC) for annealing and high cost. Since poly-Si TFTs can offer less energy consumption and less fabrication cost than those of bulk-Si MOSFET and SOI-MOSFET circuits. Single-grain TFTs technique is desirable development for future. To realize single grains, several modulated ELA methods have been proposed, such as sequential super lateral solidification (SLS), and phase-modulated ELA (PMELA). However SLS requires a rather sophisticated beam scan process and PMELA needs complicated laser annealing system.

Since high duration time, pulse frequency and stability are very meaningful to derive larger and uniform poly-Si grain. CW green laser is provided with long melting time and lower solidification rate as well as formed single-grainlike poly-Si grain as addressed in this technology. CLC could enhance lateral grain growth in laser-crystallized silicon thin films as large as 20 μm, so that CLC highly crystalline poly-Si layers can be employed to fabricate high-performance TFTs. CW green laser was a reliable laser and generates long-wavelength

laser energy, which can penetrate through glass or even plastic substrates causing negligible damage. This method can also process at room temperature for plastic panel transistors. Compared with ELC, CLC in more reliable, durable, low cost, and less maintain consumption as next crystallization key technology in the future. For high efficiency devices, not only high carrier mobility and drive current but also how efficiently devices can be turn ON/OFF as addressed steeper subthreshold swing permitted of lower operation voltage. Since presence of channel state defects and interface states lead to a subthreshold swing enhancement, the reduction of defect density turn into a key process. This study focuses on continuous-wave green laser crystallization technique involving with polysilicon films quality and analysis of the defects in the channel. Density of state (DOS) distributions of grain defects and interface states in CLC crystallized channels related to device performance were studied.

Accordingly, a high-speed and reliable transistor must have a thin channel. In ELC, thin silicon layer receives the influence of solidification rate to cause small poly-Si grain size. In CLC, single-grainlike poly-Si thin films can be ease of attainment. However surface roughness with different thickness of silicon film leads to the difference of deteriorated mechanism in the hot-carrier stressing. To explore these degradation mechanisms, more practical experiments are performed to compare the divergence with reasonable material analysis related to electrical characteristics in this study.

In future, laser activation application provide for ultra-shallow source/drain extensions, high doping, and low sheet resistance. Activation of ion implant damage and improved

microstructure are involved in this study with CW green laser irradiation. Because of the high transparency on the glass substrate with the wavelength of 532 nm also lets us to build the new application on panel from back-side activation. A 532 nm solid-state laser is provided with stable output to reduce the fluctuation of laser energy. Continuous laser annealing can also uniformly stride across the device body on large panel size. For these, front-side irradiation can be attained simultaneously dopant activation and microstructure quality modification by laser annealing. Hence these works need to be investigated urgently.

1.7 Organization of the thesis

In this dissertation, six chapters are organized to the anterior works of CW green lasers annealing processes. In Chapter 1, the development trends of poly-Si TFTs is introduced, and conventional excimer and CW green lasers annealing technology are summarized. The importance of laser activation application is also described in Chapter 1. In addition, the reliability effect on the poly-Si TFTs and motivation are also include in this chapter.

In Chapter 2, the crystallization mechanism of CW green lasers is detail interpreted what is the different with excimer laser crystallization. Experimental equipments on beam size design and laser scanning system are shown in Section 2.3. Sample preparation and material analysis including in Scanning electron microscopy (SEM), Atomic force microscopy (AFM), Micro-Raman Scattering Spectrometer, X-ray diffraction in section 2.4 and device fabrication are ascribed in Section 2.5.

In Chapter 3, density of states extraction is exercised by FEC method to examine the channel quality of fabricated devices in Section 3.2. On resistance, channel resistance, and parasitic resistance method to explore the feasibility study in Section 3.3.

In Chapter 4, the characteristics of CW green laser-crystallized epi-like silicon transistors are discussed from electrical properties and density of state of proposed CLC poly-Si TFTs in Section 4.4. The influence of the gate-stressing and HCS in epi-like silicon transistors is measured in Section 4.4-3. With various laser powers, the changes of poly-Si film structure and surface roughness are clearly depicted. The material structure, electrical characteristics, and stability on fabricated TFTs are affected by variation of silicon thickness in Section 4.5.

In Chapter 5, novel approach with CW green laser activation is applied from backside and front-side irradiation. These novel devices from Section 5.3 and 5.5 are stressed to be identified by HCS. It is very important tests to combine the crystallization and activation technique.

Finally, the result of these experiments and analysis are concluded in Chapter 6. Some recommends are also given for future prospects.

Table 1- Ⅰ Forecast of advanced LTPS TFT technology [1.13]

	Current	Next Generation	Future
Structure	p-Si TFT	Next	Single-grainlike TFT
Mobility (cm^2/Vs)	100	300	500
Design Rule (μm)	4	1	0.5
Clock Freq. (MHz)	2	15	100
Circuits DRAM	64K	1M	16M
System	X, Y driver	Memory	Sensor

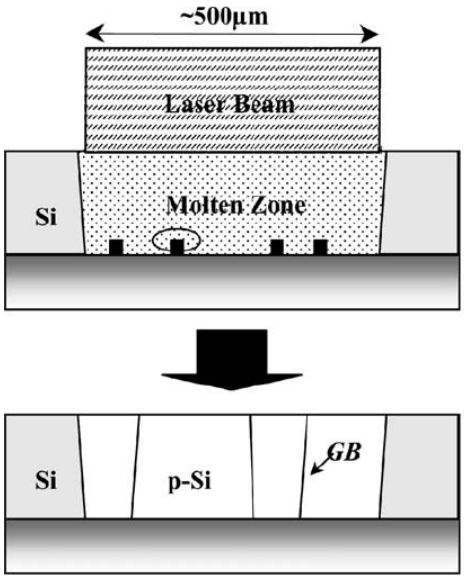


Figure 1-1 SLG process with excimer laser annealing [1.21].

Figure 1-2 shows the average grain size and related poly-Si TFT performance, associated with each of these three laser crystallization regimes.

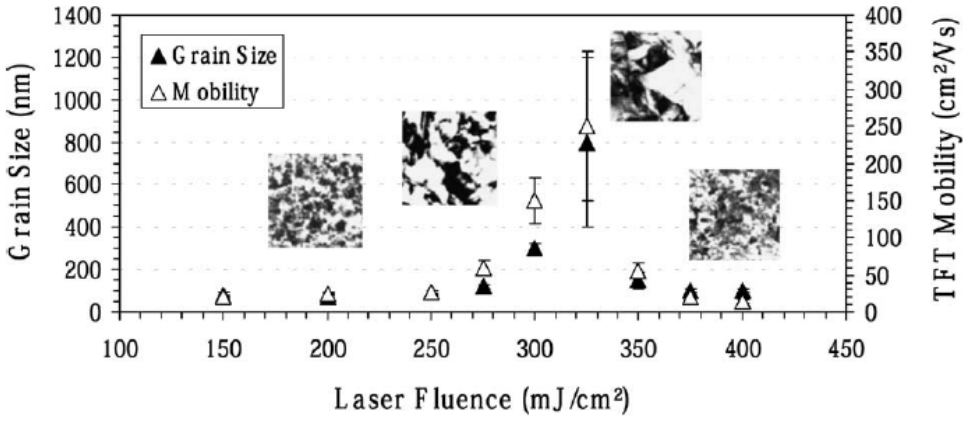


Figure 1-2 Grain size and corresponding poly-Si TFT mobility vs. laser fluence for ELA process [1.21].

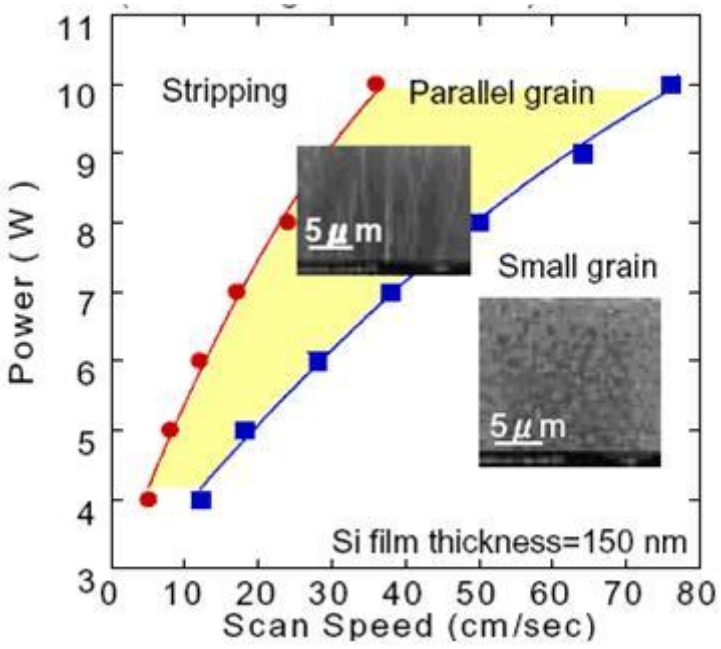


Figure 1-3 High scan speed and wide energy range of CLC [1.27].

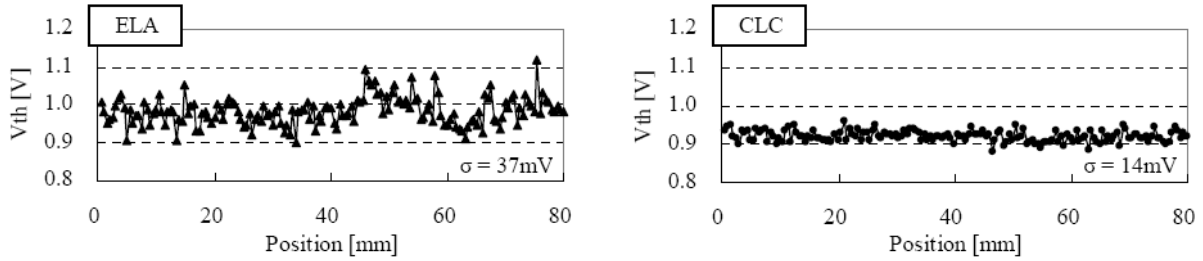


Figure 1-4 Global variation in NMOS threshold voltage: ELA (left), CLC (right). (L/W = 5.4μm/20μm, Tox = 30nm, TFT distance = 0.5mm) [1.28].

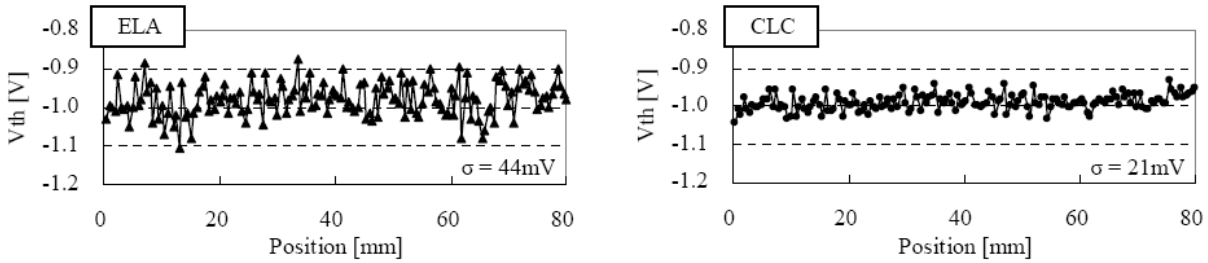


Figure 1-5 Global variation in PMOS threshold voltage: ELA (left), CLC (right). (L/W = 2.7μm/20μm, Tox = 30nm, TFT distance = 0.5mm) [1.28].

Chapter 2

Continuous-wave solid-state green laser lateral crystallized poly-Si films

---

2.1 Introduction

In regard to laser annealing, continuous-wave (CW) diode pumped solid-state lasers (DPSSL) typically exhibit several attractive features of small facility footprint and maintenance, excellent beam profile, highly stable output power, multi-wavelength (IR, visible, and UV) outputs. The absorption coefficient of amorphous silicon (a-Si) at wavelength (λ) of 532 nm is approximately one order in magnitude lower than that at λ= 308 nm, which wavelength is excimer laser output wavelength [2.1][2.2]. However, continuous output laser energy from such CW green solid-laser reportedly enables super lateral crystallization. Moreover, long-wavelength laser energy almost completely penetrates through non-alkali glass substrate [2.3], barely damaging glass panel substrates [2.4].

2.2 Crystallization mechanism of CLC poly-Si

Green light energy penetrates to a-Si as deep as 1μm, related to absorption coefficient of a-Si at λ= 532 nm. The thickness of active layer is generally in the range of 50-150 nm. Therefore, the laser energy is absorbed in the a-Si layer and directly melts the entire thickness of a-Si film. A maximum increase of surface temperature of irradiated films has been

estimated by Lax to be [2.5]

$$\Delta T_{\max} = \frac{(1-R)N}{(4\pi)^{1/2}K}\left(\frac{P}{W}\right) \qquad \text{eq. 2-1}$$

Where R is the reflectivity, K is the thermal conductivity ($Wcm^{-1}K^{-1}$), P is the laser power, W is the radius of the focused Gaussian beam, and N is the normalized temperature constant (for W>5μm, N is~1). As green laser power is 4-5 W, the surface temperature can reach melting point of a-Si. CW green laser continuously provides laser energy on irradiated a-Si films, thereby causing directional solidification due to large temperature gradient along scanning direction [2.6], because the liquid-solid interface runs parallel to the scan direction. In addition, the solidification time of Si materials molten by CW green laser annealing is several microseconds, much longer than ~100 ns of Si materials molten by excimer laser annealing [2.7]. For these reasons, CLC ensures super lateral grain growth, in a considerably range of laser energy and scanning rate, forming highly crystalline Si layers with grains of few micrometers. In ELA, laser energy is almost absorbed within the surface of the irradiated a-Si film. Fine crystals as seed crystals were usually formed at the bottom of the a-Si film. Therefore, in ELA, the vertical temperature gradient normally forms and the grain size is limited at few hundred nanometers to one micrometer. Figure 2-1 shows the crystallization mechanism between ELA and CLC.

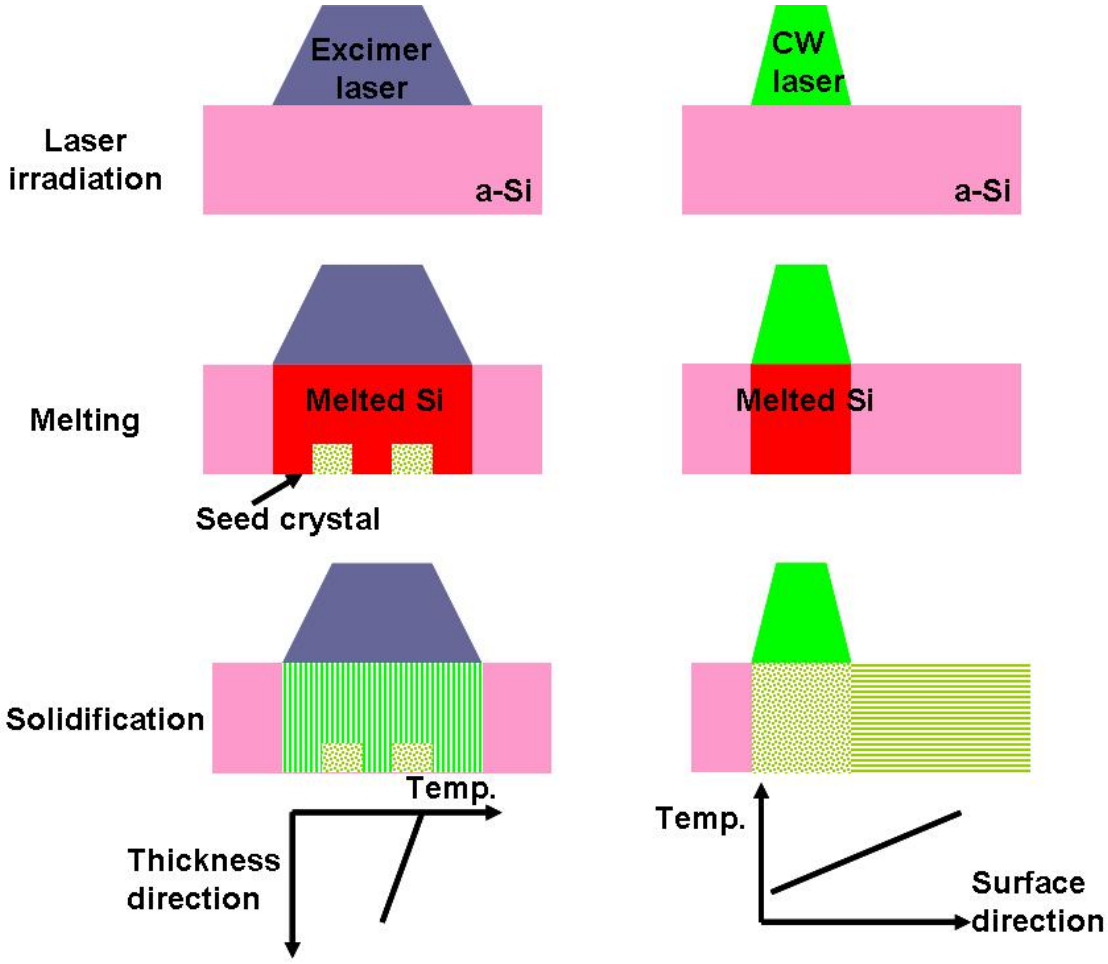


Figure 2-1 crystallization mechanism between ELA and CLC

2.3 Experimental Procedure

2.3.1 Laser beam size design

The Spectra-Physics *Millennia Pro s-Series* is a family of a diode-pumped, frequency-doubled CW visible laser capable of providing from 5 Watts of laser power at green wavelength of 532 nm. The *Millennia Pro s* design features a rugged laser head for simple, hands-off operation that delivers exceptional power stability and beam-pointing performance. Typical spot size of 532 nm wavelength is about 10-15 μm as obtained by Spectra-Physics DPSS laser [2.8][2.9].

$$W_0 \approx \left[4 \times \lambda \times \left(\frac{f}{D} \right) \times M^2 \right] \Big/ \pi \qquad \text{eq. 2.2}$$

Within any transverse plane, the beam intensity assume its peak value on the beam axis, and drops by the factor $1/e^2 \sim 0.135$ at the radial distance $\rho = W(z)$. Since 86% of the power is carried within a circle of radius W(z), we regard W(z) as the beam radius (also called the beam width). The rms width of the intensity distribution is $\sigma = W(z)$. The dependence of the beam radius on z is governed by [2.10],

$$W(z) = W_0 \left[1 + \left(\frac{Z}{Z_0} \right)^2 \right]^{1/2} \qquad \text{eq. 2.3}$$

It assumes its minimum value W_0 in the plane z =0, called the beam waist. Thus W_0 is the waist radius. The waist diameter $2W_0$ is called the spot size. Since the beam has its minimum width at z =0, it achieves its best focus at the plane z =0. In either direction, the beam gradually grows out of focus. The axial distance within which the beam radius lies

within a factor $\sqrt{2}$ of its minimum value is known as the depth of focus [2.10].

$$2z_0 = \frac{2\pi W_0^{\,2}}{\lambda} \qquad \text{eq. 2.4}$$

Calculating with equation 2.3-2.4, Figure 2-2 and Figure 2-3 show the different focus distance (10 cm and 12.5 cm) of spherical lens to obtain smallest short axis of spot size. The precise beam size design is devised into 480 μm×40 μm by cylindrical lens and spherical lens in our study. Figure 2-4 shows the real holder bar of the mirror and lens as well as laser beam morphology.

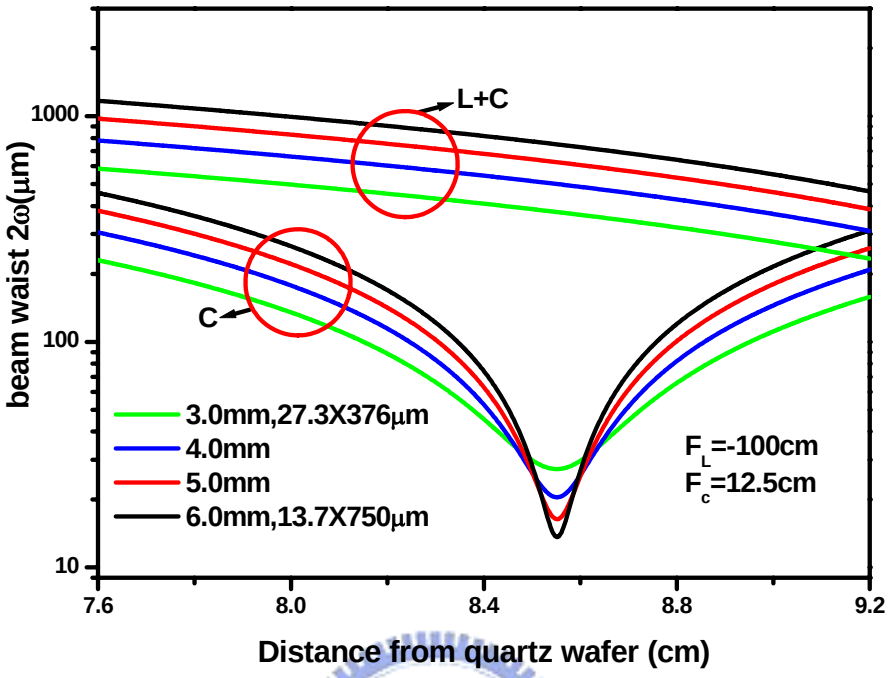


Fig. 2-2 Focus distance (12.5 cm) of spherical lens

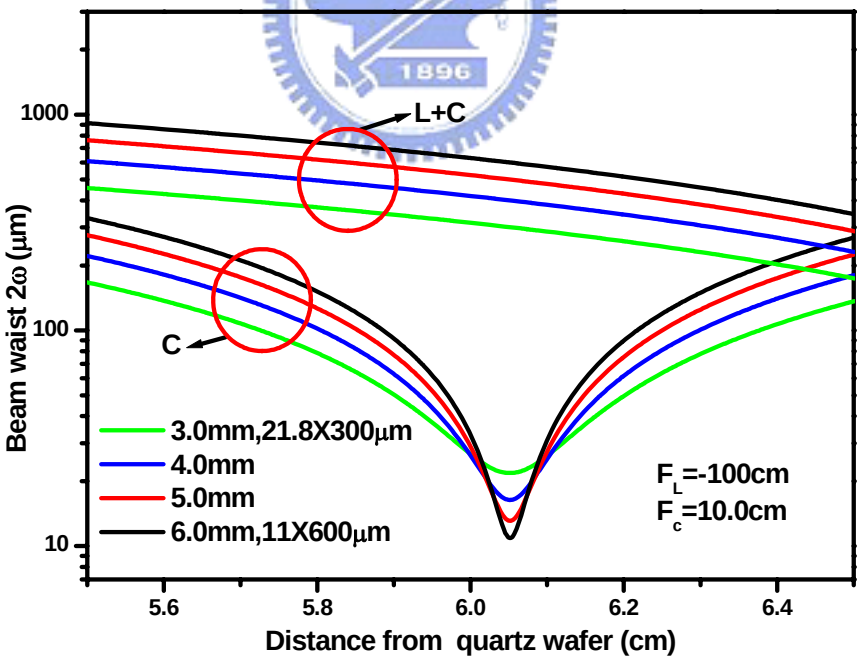


Figure 2-3 Focus distance (10 cm) of spherical lens

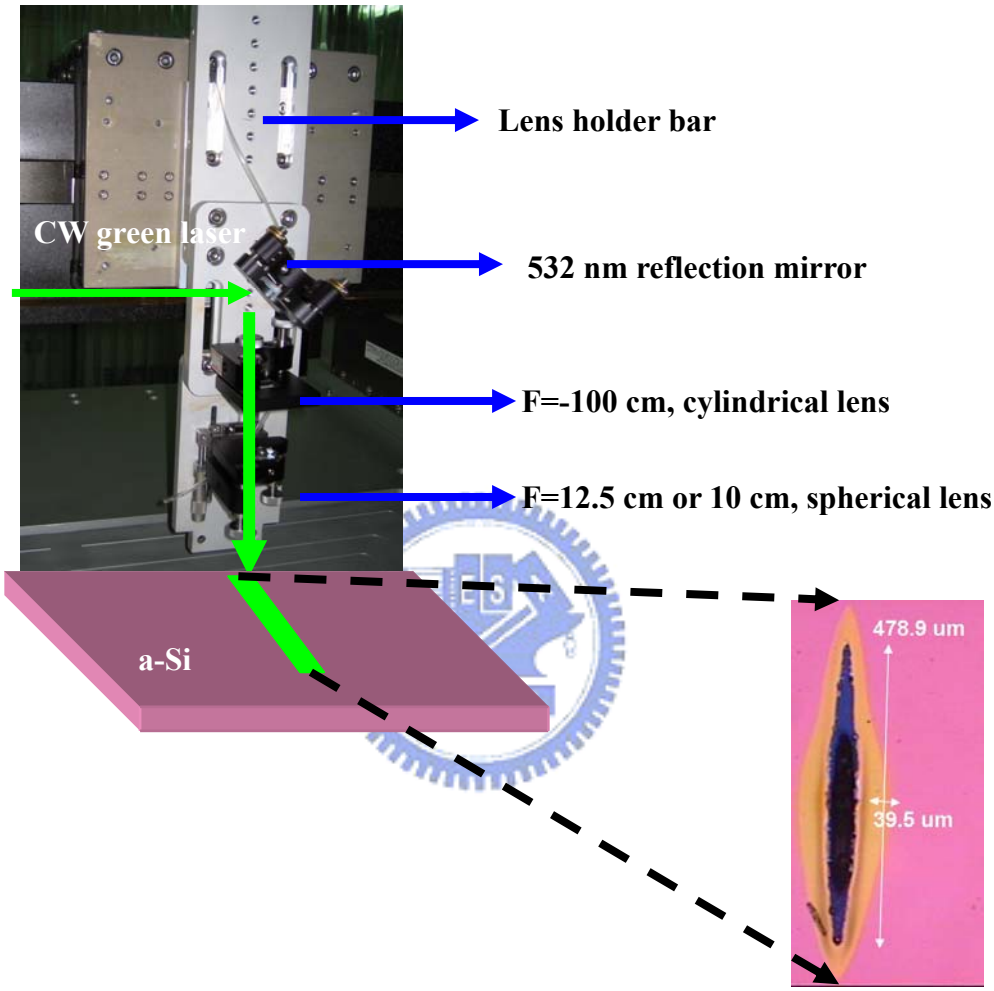


Figure 2-4 Laser beam image

2.3.2 Laser annealing system

A laser beam was precisely controlled at stripe shape of 480 μm×40 μm. The scanning range was wide enough to address 1-2 generation LTPS TFTs displays. The air bearing module in robot stage was introduced to enhance stepping and position precision (1 μm) in stage motion. Specs of laser scanning system were shown in Figure 2-5.

1. Iron core linear motor based design offers excellent performance and great value

2. Repeatable to ± 2 μm

3. XY travel sizes from 500 to 750 mm

4. Dual motor Y-axis option for high performance applications

5. Compact footprint maximizes use of production area

Figure 2-6 shows the optimization speed rate and the stability of scanning speed.

Figure 2-5 Laser scanning system

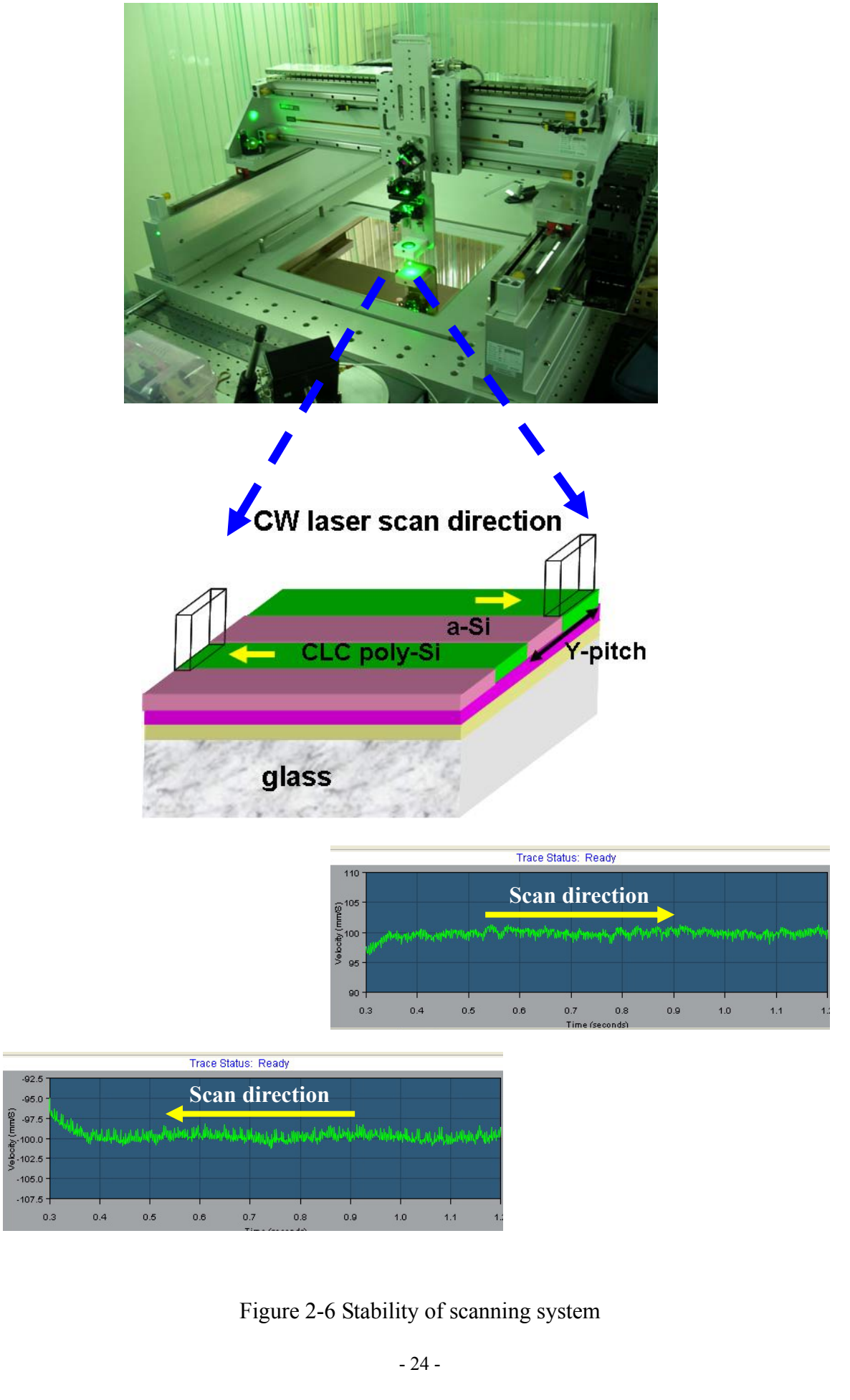


Figure 2-6 Stability of scanning system

2.3.3 Sample preparation and material analysis

In this study, two kinds of transparent substrates, glass and quartz substrates are prepared. For the case of glass substrates, the stack of SiN_x and SiO_2 thin films as an impurity barrier layer were deposited on the Corning Eagle 2000 glass substrates by plasma enhanced CVD (PECVD) and their thickness were 50 nm and 150 nm, respectively. Subsequently, a-Si films with thickness 50-150 nm was deposited by PECVD on the SiO_2/SiN_x/glass substrates, and was subjected to CW green laser annealing. For the case of quartz substrates, 100nm-thickness a-Si films were deposited on SiO_2 covered quartz wafer by low-pressure chemical vapor deposition (LPCVD) at 550°C. Before laser annealing, the native oxide on a-Si layers was removed by HF solution. Moreover, the a-Si films was pre-patterned by dry-etching into rectangle area 80μm×150μm in prevention of peeling. The samples were loaded on the table keep at room temperature and in the air environment. Several CW green laser energies were introduced to conduct laser annealing. The scanning rate was fixed at 10 cm/sec.

The grain microstructure and surface roughness of CLC poly-Si were analyzed through various material diagnosis tools. Scanning electron microscopy (SEM) analysis was used to analyze grain size and grain structure of poly-Si films after secco-etching. Atomic force microscopy (AFM) was intruded to examine the topography of poly-Si films. Moreover, micro-Raman Scattering Spectrometer was used to evaluate the crystallinity or defects of poly-Si films. Figure 2-7 summarize all details.

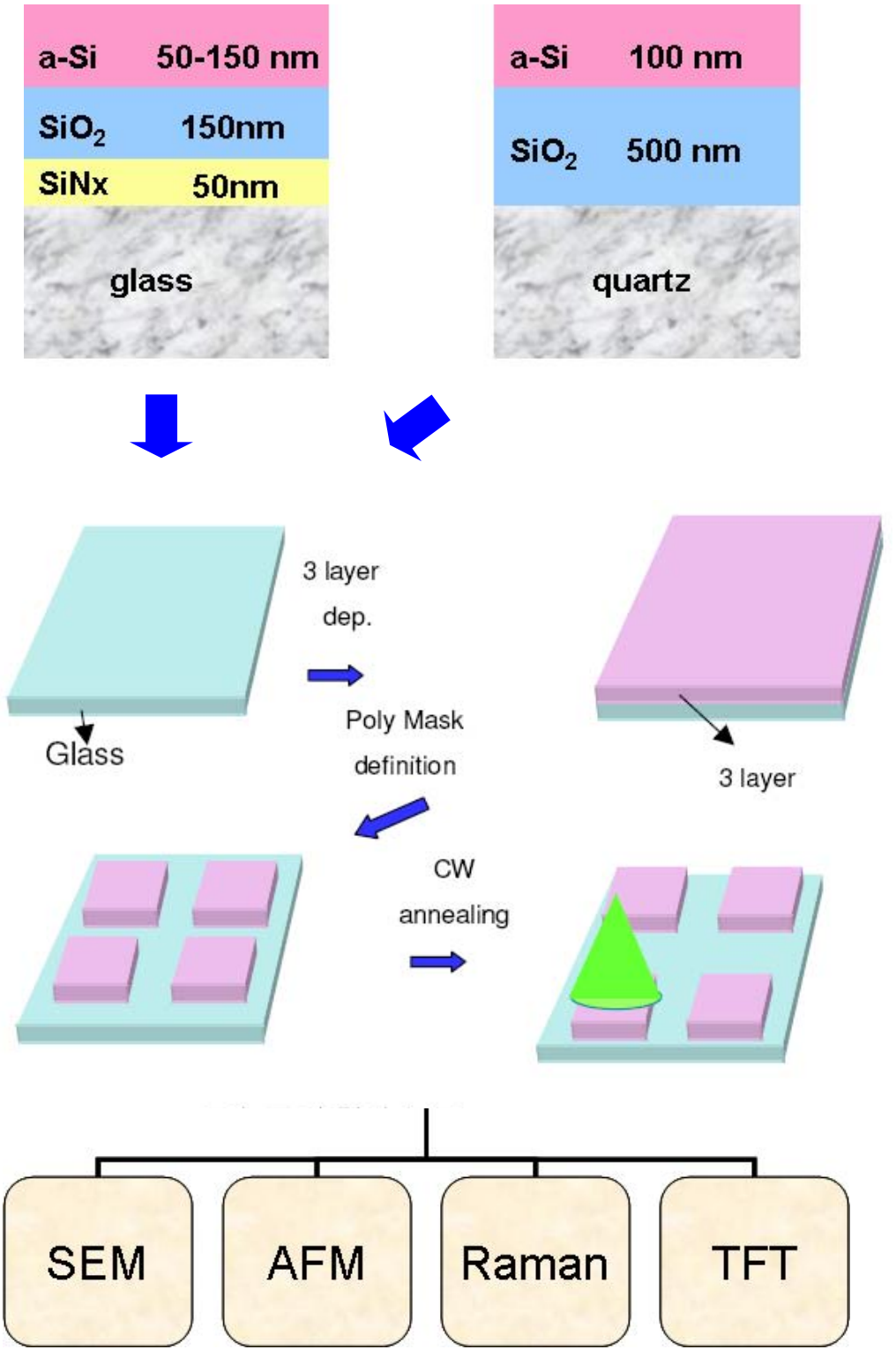


Figure 2-7 Flow diagram of sample preparation and analysis

2.4 Results and Discussion

2.4.1 OM and SEM analysis of CLC poly-Si films

Figure 2-8 (a)~(d) shows the OM and SEM images of 50 nm-thick poly-Si film that was crystallized by CW green laser annealing. Symmetrical surface morphologies of laser-crystallized films along scanning direction of laser beam, observed in 2-8(a)-(b), clearly reveal many frozen stream-like structures originated from central axes. The topography at the frozen stream-like region is quite similar to that of ZMR silicon [2.11], which means the occurrence of complete melting during CLC.

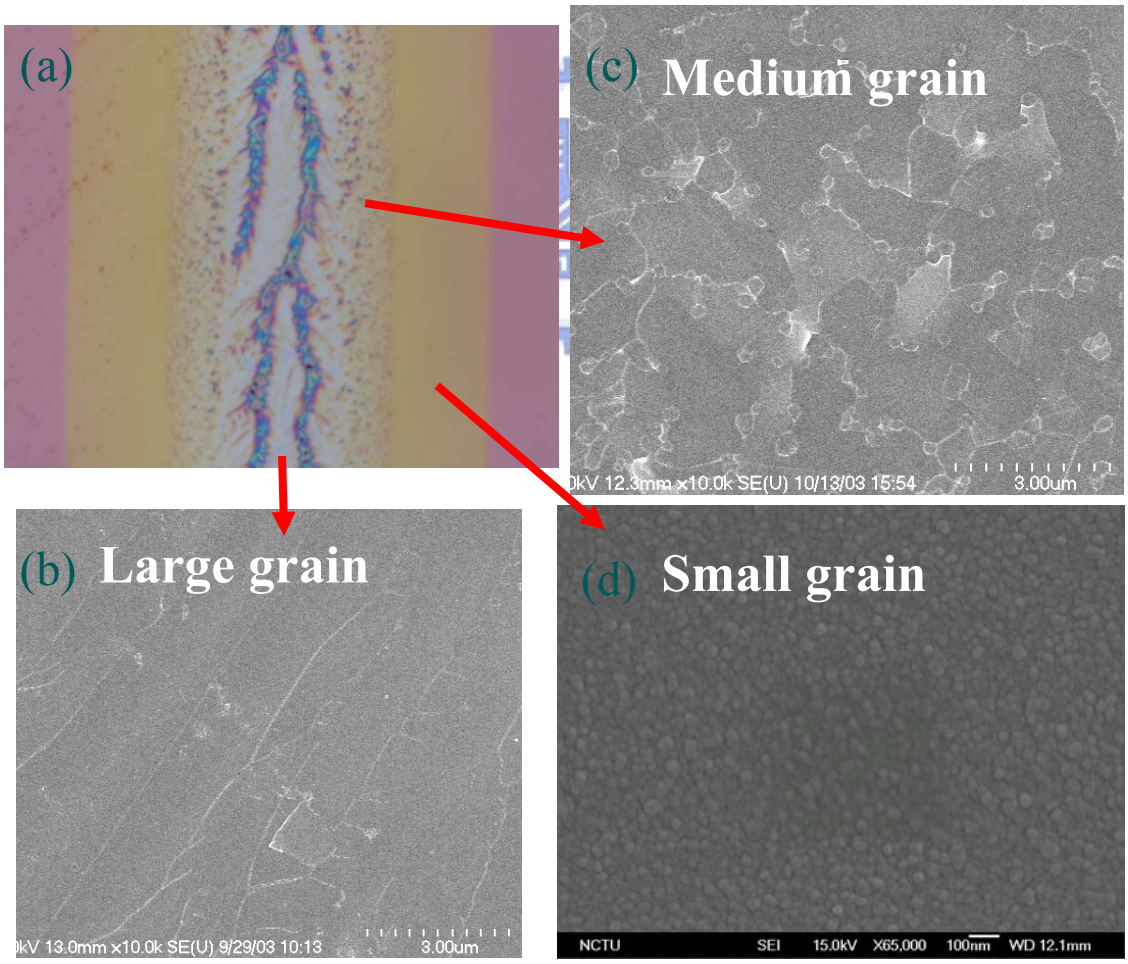


Figure 2-8 OM image of (a) and SEM graphs of (b)-(d) of CLC crystallized poly-Si films.

Figure 2-8 (b) indicated extremely large grains in the films that were irradiated by the central portions of Gaussian profile of laser beam. Away from the regions irradiated by the central portion of laser beam, Ku et al. also observed that grain size became smaller [2.12]. Moreover, SLG-like morphologies in microstructures of regions irradiated by the portion of laser-energy distribution away from beam center was observed and explained by partial melting (Figure 2-8(c)). The microstructure of region irradiated by the tail of laser beam was consisted of several ten nanometers and the grain morphology (Figure 2-8(d)) was described by solid phase crystallization.

Figure 2-9 shows the crystallized region of ~220 μm is much smaller than the spatial distribution of laser Gaussian beam of ~480μm. While laser scanning speed was larger, crystallized regions became narrower.

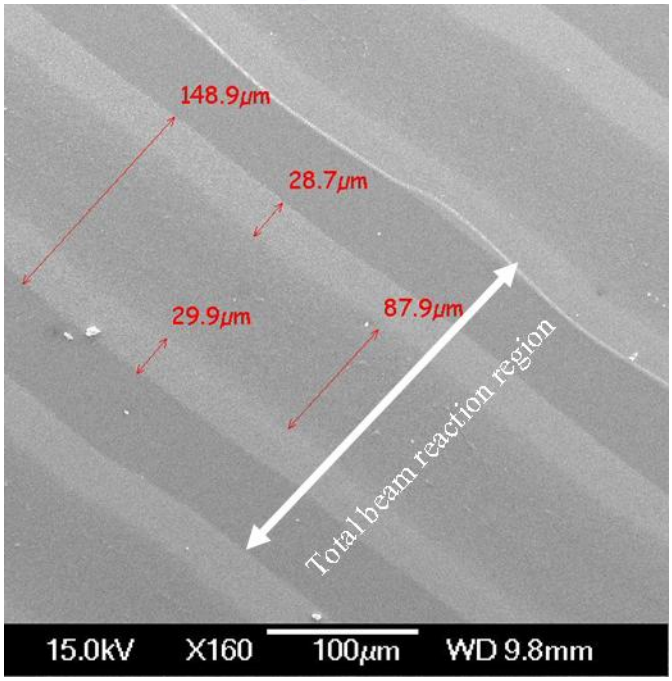


Figure 2-9 Dimension of different CLC poly-Si structure in the crystallized region

2.4.2 Grain size depends on laser power

Figure 2.10 (a)~(d) are the microstructure images of the poly-Si films that were crystallized by CW green laser irradiation of 3.5 W, 3.8 W, 4.1 W, and 4.4 W, respectively at room temperature and at a scanning rate of 10 cm/s. CLC under lower low laser power, Figure 2.10(a)-(b) show that micrographies of CLC poly-Si films comprised micro-grains of dimensions 0.5-1 μm^2 were similar to those of ELA poly-Si. CLC under middle power enlarges partial grains as large as 2-3 μm. Middle green laser power partially or nearly melts a-Si films and generates appreciable random seeds or nucleation sites in films such that the entire microstructure was consisted of both large grains and small grains (Fig. 2.10 (c)). Therefore, CLC under middle laser power, like ELA under SLG, limits grain size by solidification rate of liquid silicon and the retain-solid seed distance. The non-uniform grain distribution seriously affects the variation of TFT performance. CLC under high laser power greatly suppresses the nucleation sites. The uniform and continuous lateral grain growth forms (Figure 2.10 (d)). In generally, TFTs that were fabricated on highly crystalline poly-Si crystallized by high green laser energy, reveal excellent electrical characteristics.

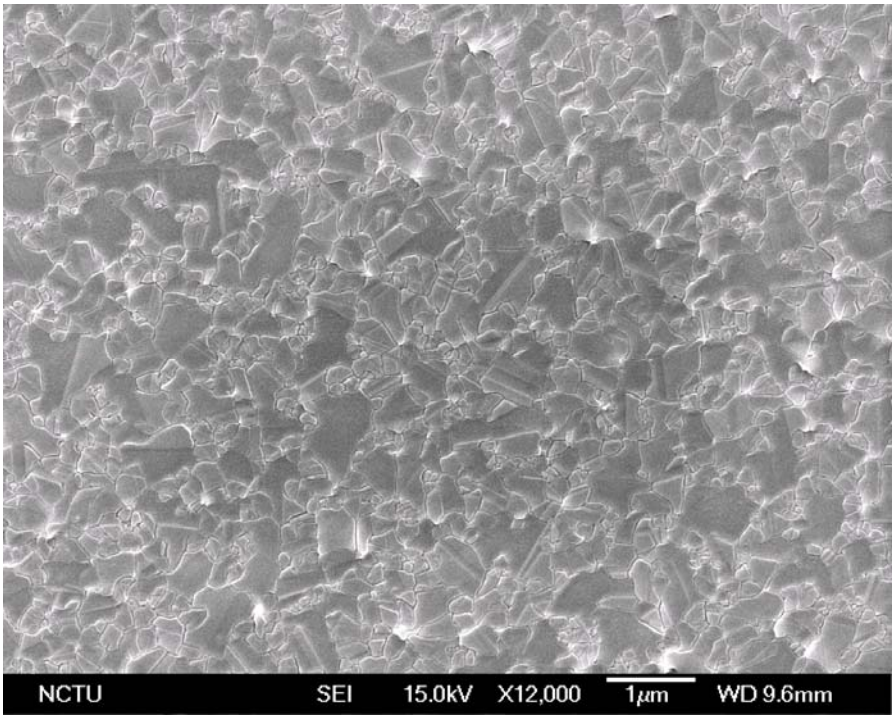


Figure 2.10 (a) SEM graph of 50 nm poly-Si thin film crystallized at 3.5 W.

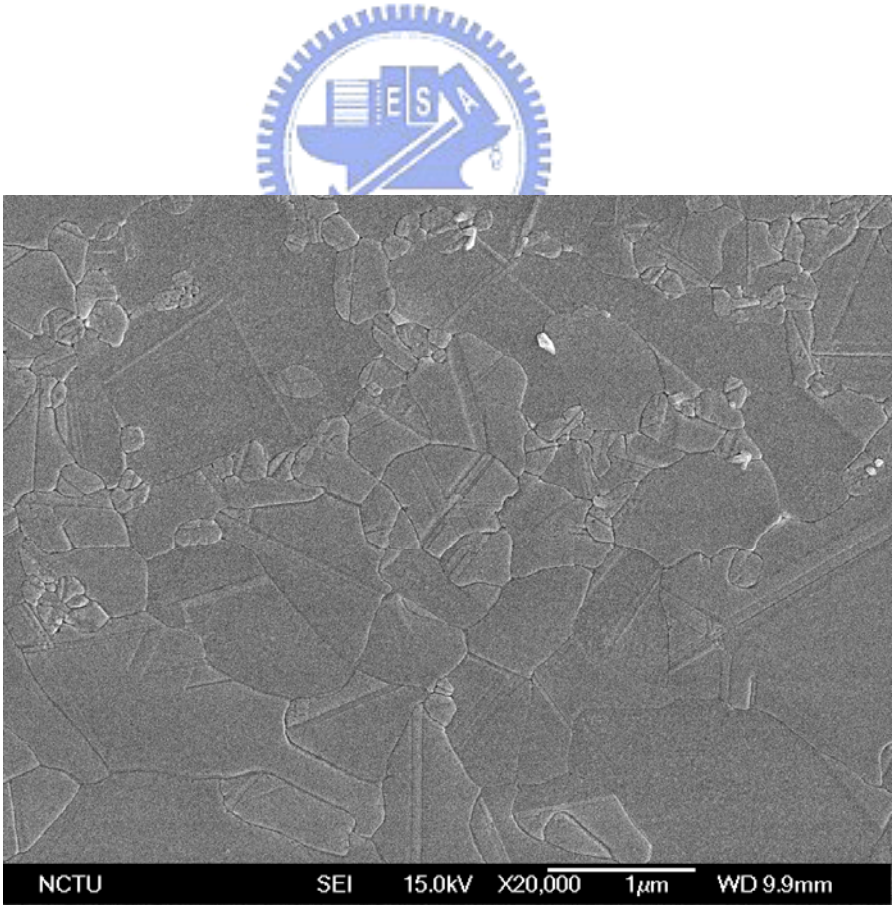


Figure 2.10 (b) SEM graph of 50 nm poly-Si thin film crystallized at 3.8 W.

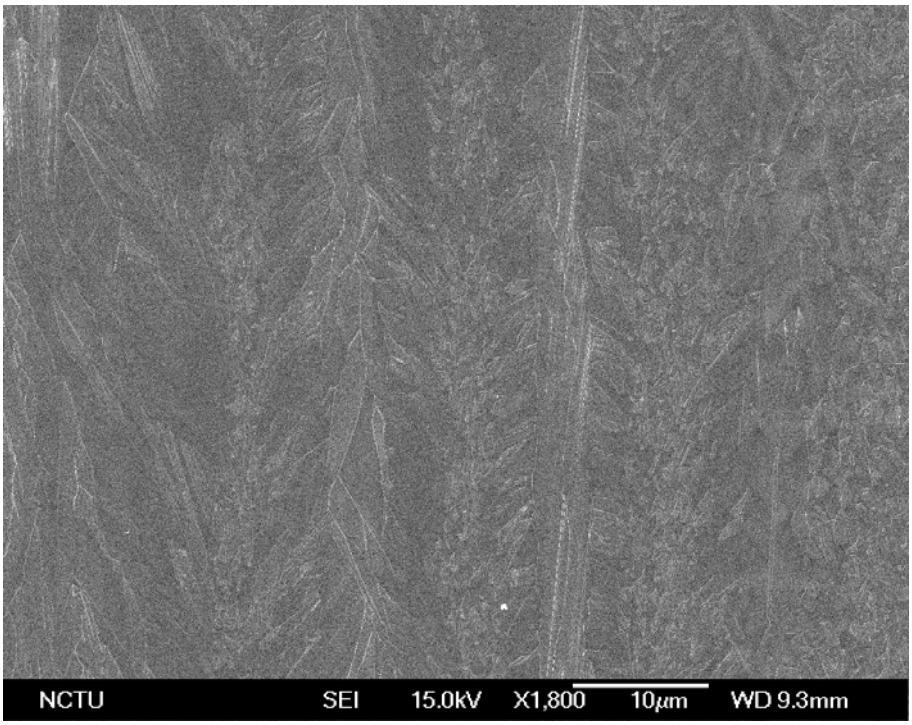


Figure 2.10 (c) SEM graph of 50 nm poly-Si thin film crystallized at 4.1 W.

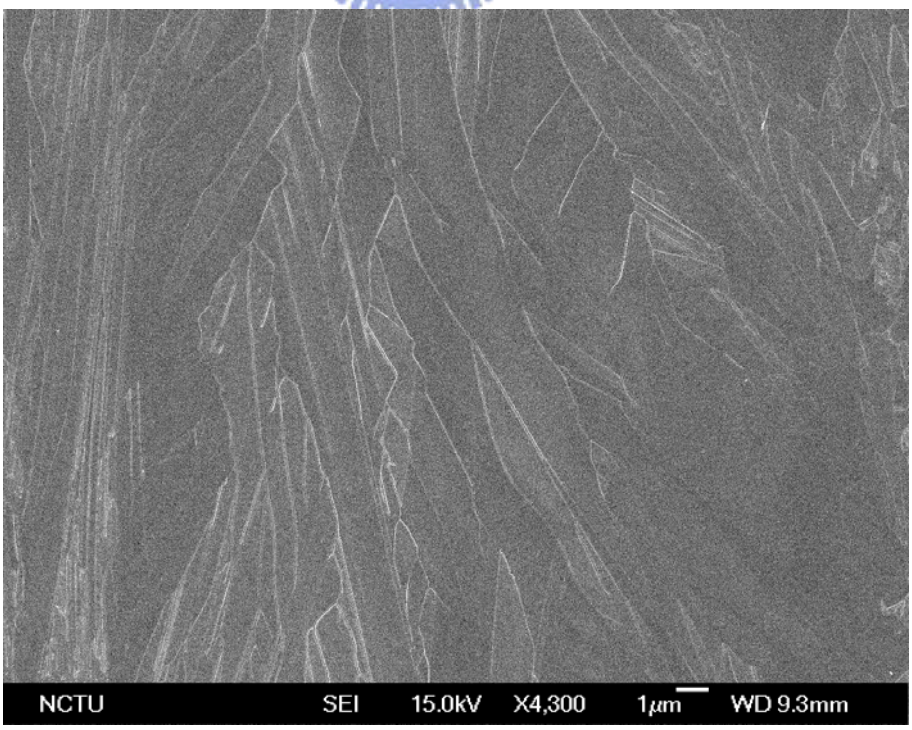
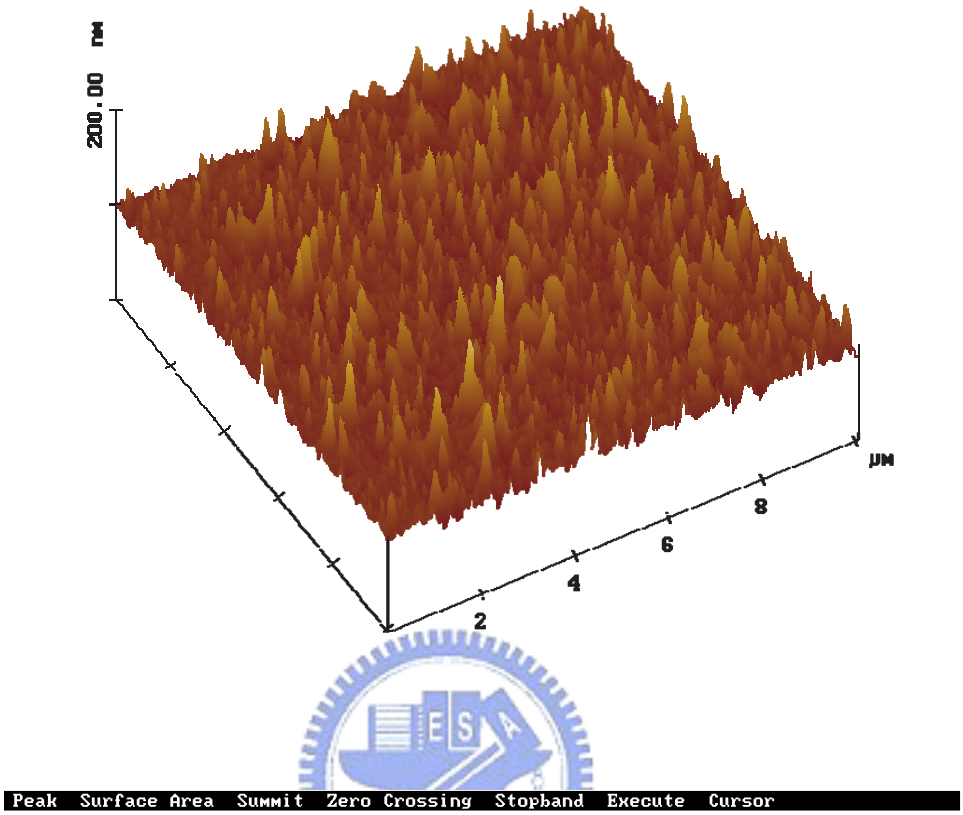


Figure 2.10 (d) SEM graph of 50 nm poly-Si thin film crystallized at 4.4 W.

2.4.3 Topographies of CLC poly-Si channels

Surface roughness of transistor channels affects the leakage currents of gate dielectrics and, therefore, the reliability of transistors [2.13-14].

Figure 2-11 (a)-(c) depicts the topographies of a-Si channels crystallized by the CLC method at different laser powers. As the laser power increases, CLC, instead of super-lateral-growth (SLG) or even solid-phase crystallization, dominates the growth of the grains [2.15]-[2.17]. Consequently, highly crystalline channels comprised micro-grains of dimensions $3x10\mu m^2$ forms. The surface roughness of the channels crystallized with an incremental laser power initially declines from 8.2 nm (3-3.7 W) to 2.8 nm (3.8-4.2W), before increasing to 5.1 nm (4.3-4.5 W), as indicated by these topographies. The initial decrease in the roughness reflects a change in the crystallization mode because the surface roughness of the SLG-crystallized channels was reported to exceed that of the CLC-crystallized channels [2.15][2.16]. The reversal in the roughening of the surface as the laser power is further increased is attributed to the increase in the numbers of hillocks at the grain boundaries, caused by high photo-energy irradiation [2.18].



Roughness Analysis

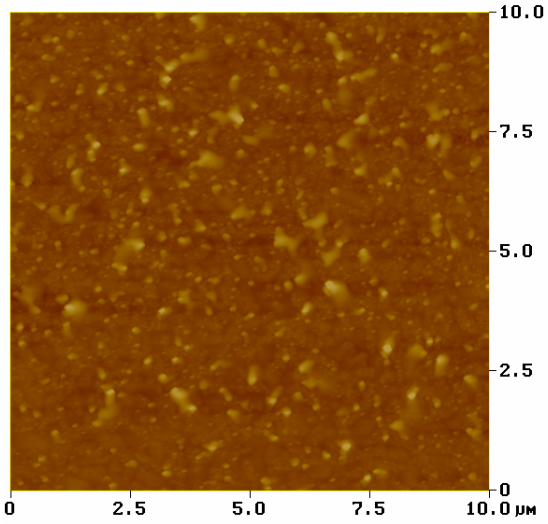


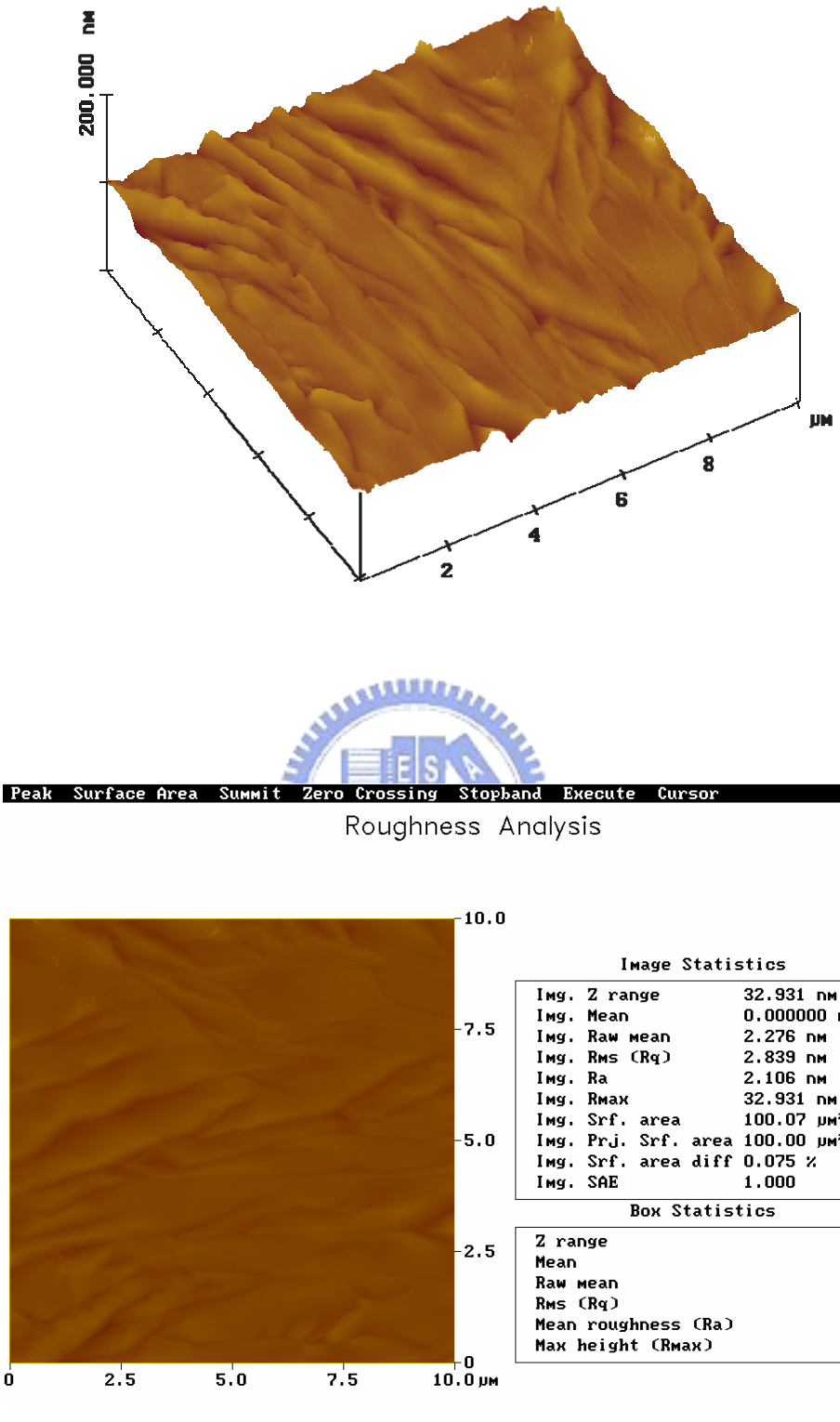
Image Statistics

Img. Z range	95.667 nm
Img. Mean	-0.000003 nm
Img. Raw mean	17.338 nm
Img. Rms (Rq)	8.216 nm
Img. Ra	5.501 nm
Img. Rmax	95.667 nm
Img. Srf. area	101.72 μm²
Img. Prj. Srf. area	100.00 μm²
Img. Srf. area diff	1.716 %
Img. SAE	1.016

Box Statistics

Z range
Mean
Raw mean
Rms (Rq)
Mean roughness (Ra)
Max height (Rmax)

(a)


200.000 nm
2
4
6
8
µm
Peak Surface Area Summit Zero Crossing Stopband Execute Cursor
Roughness Analysis
10.0
7.5
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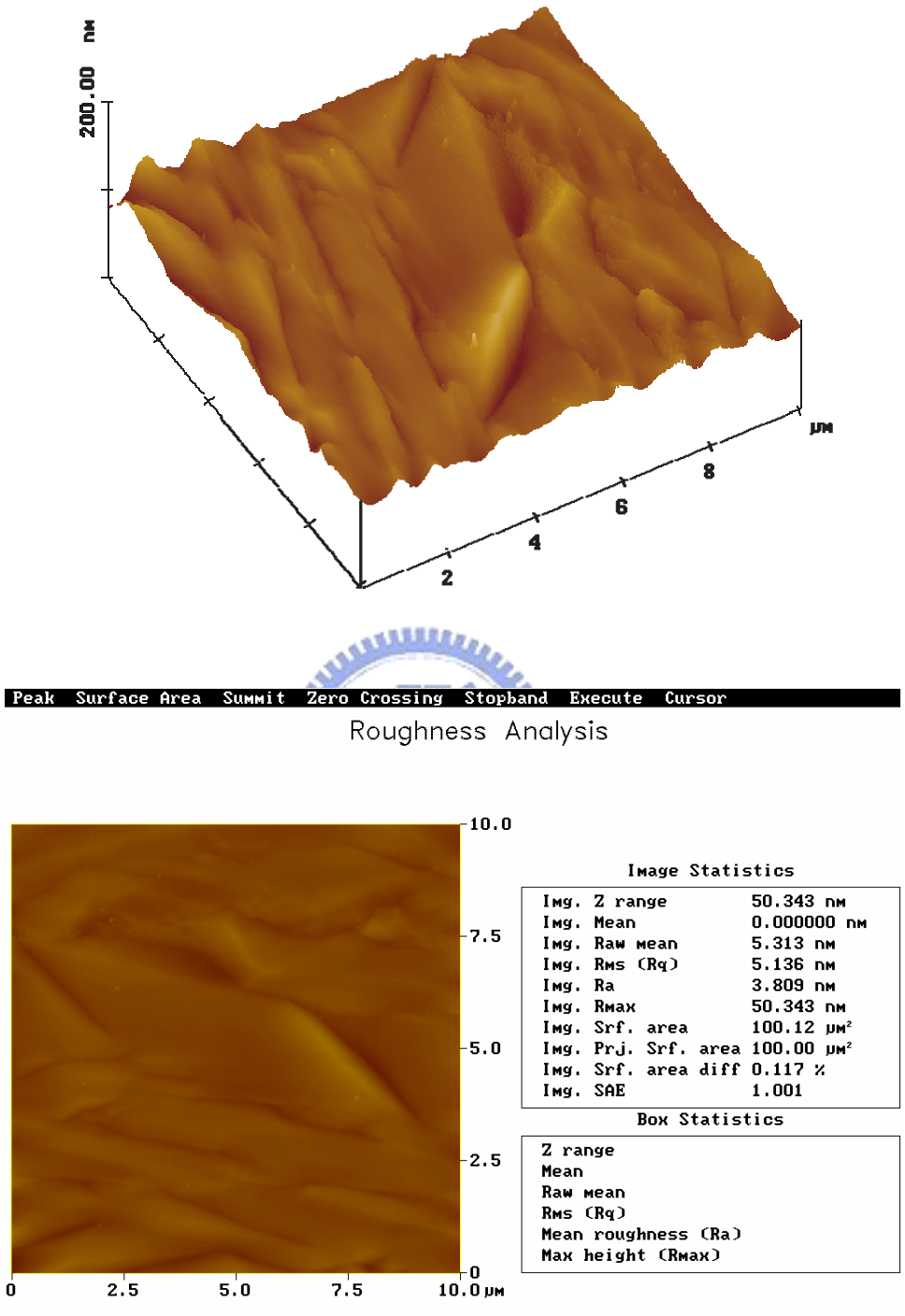
0
2.5
5.0
7.5
10.0 µm
Image Statistics
Img. Z range 32.931 nm
Img. Mean 0.000000 nm
Img. Raw mean 2.276 nm
Img. Rms (Rq) 2.839 nm
Img. Ra 2.106 nm
Img. Rmax 32.931 nm
Img. Srf. area 100.07 µm²
Img. Prj. Srf. area 100.00 µm²
Img. Srf. area diff 0.075 %
Img. SAE 1.000
Box Statistics
Z range
Mean
Raw mean
Rms (Rq)
Mean roughness (Ra)
Max height (Rmax)

(b)



(c)

Figure 2-11 AFM micrographs of channel topographies of polysilicon films crystallized by CW green laser at various laser powers of (a): 3.5, (b): 4.2 and (c): 4.5 W.

2.4.4 Raman Spectroscopy analysis of CLC poly-Si films

The crystalline fraction of films was evaluated by comparing the intensity of the transverse-optical (TO) phonon mode of a-Si at ~480 cm^{-1} with the optical-phonon mode of crystalline Si at ~520 cm^{-1} [2.19][2.20]. The full width at half maximum (FWHM) of the three-hold-degenerated optical-phonon mode detects the defects in the poly-Si thin films and in generally, the Si wafer has a value of 4.5 cm^{-1} in FWHM. Comparing Raman spectra of ELA and CLC poly-Si films that corresponded to different crystallinity to those of ELA poly-Si films at 512.2 cm-^{1} as well as value of CLC is closed at 517.3 cm^{-1} in the Figure 2-11 (inner graphs show the SEM images between ELC and CLC). This indicates the poly-Si films crystallized with CLC method in relation to complete melting silicon. The high degree of melting phase is provided with high crystallinity and lower defects. Compared with FWHM, CLC poly-Si films is significantly smaller about 4.62 cm^{-1} than the value is 9.96 cm^{-1} in the ELA poly-Si films because of fewer defects in CLC poly-Si films [2.21].

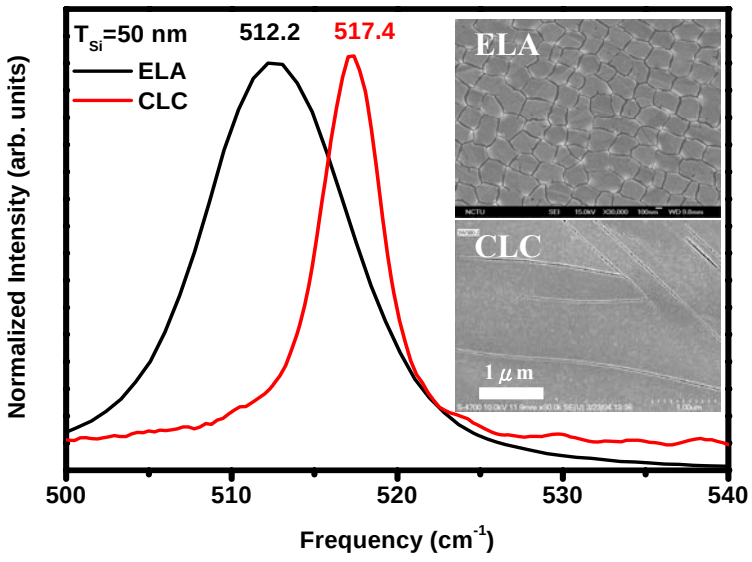


Figure 2-12 Comparison of the Raman spectra between ELA and CLC poly-Si films

2.4.5 X-ray diffraction of CLC poly-Si films

Figure 2-13 shows X-ray diffraction of CLC and ELA poly-Si films that there is some orientations including (111), (200), and weak (311) direction in the CLC poly-Si films. As the applied laser energy is increased, the orientation is the same. Compared with ELA poly-Si thin films the orientation peak is obviously changed. The crystallization orientation is affected by laser power, scanning rate, crystallization environment, capping layer, and so on. However, Hara et al. had been discovered the orientation at (110) and (111) direction in the CLC poly-Si films [2.22]. Hence the orientation of grains with CLC should be studied further.

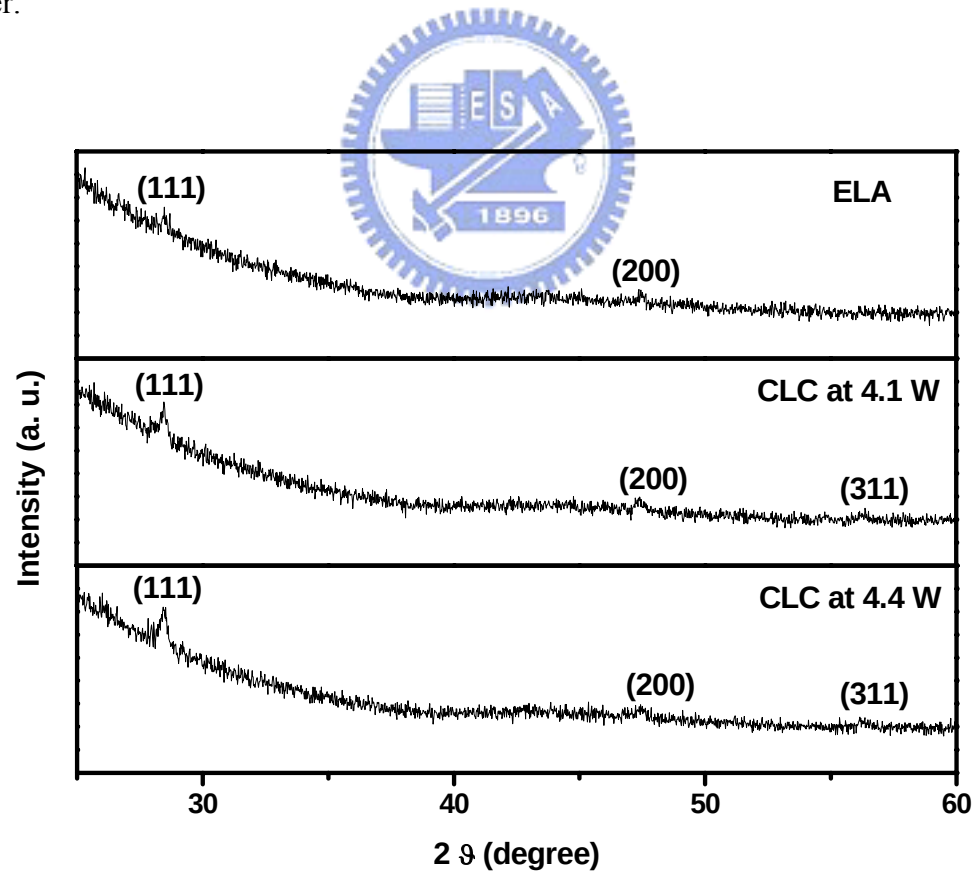


Figure 2-13 X-ray diffraction of ELA and CLC poly-Si films.

2.5 Fabrication of CLC poly-Si TFTs

The steps in CLC poly-Si TFT fabrication are shown in Figure 2-14. The active regions were performed on the pre-patterned Si islands with dry-etching. Gate dielectric of PECVD TEOS-SiO2 with a thickness of 100 nm was deposited at 300°C. Poly-Si film with a thickness of 200 nm with low pressure CVD (LPCVD) at 620°C is adopted to form self-aligned transistors. Then, poly-Si films were etched by reactive ion etching (RIE) as the gate electrode and subsequently etched SiO_2 for gate oxide. Poly-Si gates and source/drain regions were doped with PH_3 ($5.0x10^{15}cm^{-2}$ and 35 keV) for N-type TFTs. 400 nm-thick TEOS passivation oxide layers were deposited by PECVD and implant dopants were activated by thermally annealing at 600°C for 12 hr. Buffer oxide etching (BOE) solution was used to open the contact holes and 500 nm-thick aluminum films were deposited by thermal evaporation. Finally, aluminum films were patterned to form contact pads for completing CLC poly-Si TFTs and sintered the TFTs at 350°C for 30 minutes. The fabricated TFTs were used NH_3 plasma treatment to improve the gate oxide and interface quality for 30-60 minutes.

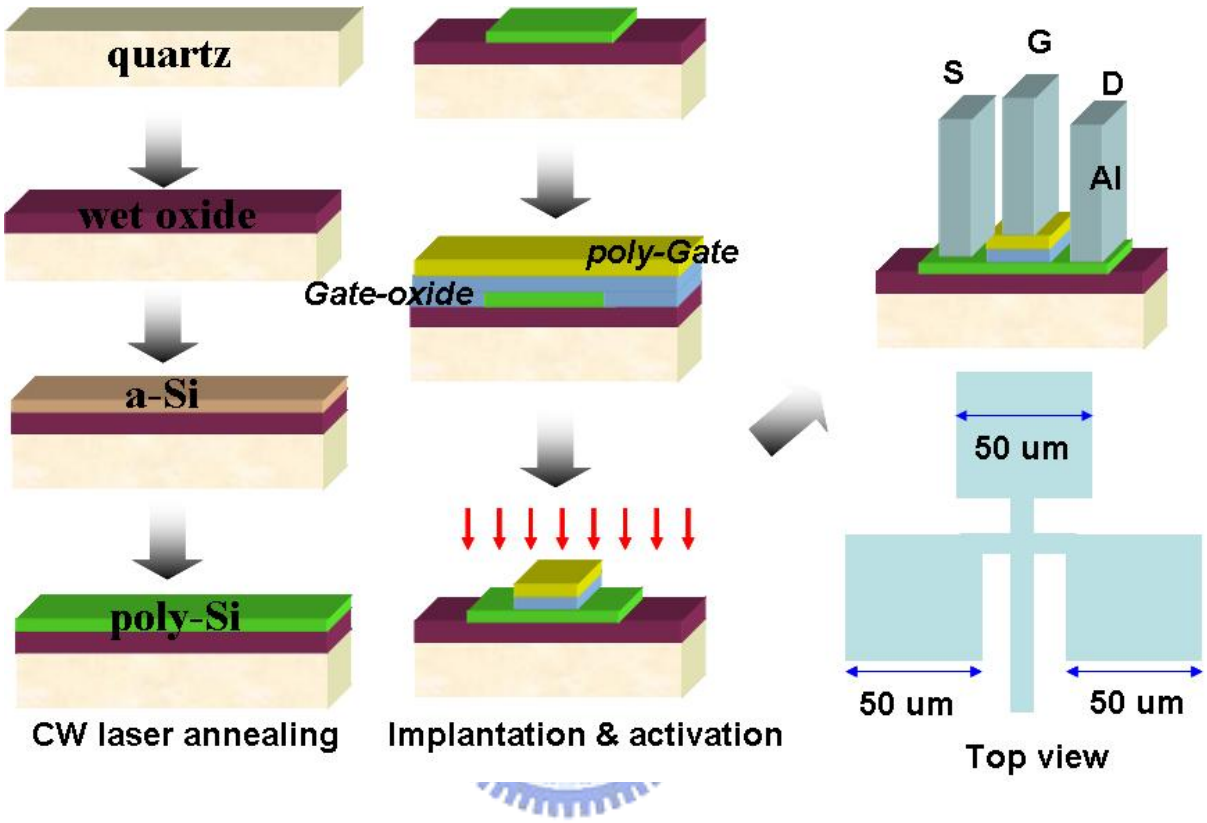


Figure 2-14 CLC poly-Si TFT fabrication process

Chapter 3

Electrical characterization and Density of states of continuous-wave laser-crystallized epi-like silicon transistors

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3.1 Electrical characterization of CLC poly-Si TFTs

Figure 3-1 (a) plots logarithmic transfer (drain current I_d versus gate voltage V_g) characteristics and linear transcondcutance (G_m) curves for some representative TFTs with 100 nm-thick active layer on the applied laser energy density, when a drain voltage V_d of 0.1 V was applied. The parameters of CLC poly-Si TFT devices were measured with a HP 4156 semiconductor parameter analyzer. The threshold voltage is extracted experimentally from the I_d-V_g characteristics. In the linear mode of operation, the I_d-V_g characteristics for devices can be approximated using [3.1]:

$$I_d=(W/L)\mu C_{ox}(V_g-V_{th})V_d \qquad \text{eq. 3-1}$$

The subthreshold slope (S) was also extracted from the maximum slope of the transfer curves, plotted on a semilog scale [3.1].

Since average grain size increases with laser energy density in ELA poly-Si technology, the results are similar in CW green laser annealing mode. And poly-Si films with laser annealing are grown from the molten phase, it is expected that many in-grain defects because of rapid cooling process [3.2]. Hence the high laser annealing energy causes the slower

cooling rate to form large grains and lower defect in grain as well as grain boundaries. As the laser energy density is increased from 3.5-4.5W, the on current and transconductance are enhanced in Figure 3-1 (a). Figure 3-1 (b) shows the small leakage current in the higher laser energy with a better crystallization structure [3.3] at V_d=5V and Figure 3-1 (c) shows the I_d-V_d current of 4.25 W crystallized poly-Si TFTs. On the other hand, low laser energy causes the small grains that have more grain boundary defect density near the drain junction to lead to increase the leakage current.

The grain size and the crystallinity of the poly-Si films pay an important role to relate to electrical characteristics of CLC poly-Si TFTs with different variation of the laser power. The field-effect mobility of CLC poly-Si TFTs in the Figure 3-2 (a) is enhanced apparently from 136-367 cm^2/Vs as a function of laser power. The results indicate that the grain size and crystallinity are improved by degrees. In addition, the reduction of threshold voltage with increasing laser power is due to decrease the grain boundaries of CLC poly-Si films in the Figure 3-2 (b). From the Figure 3-2 (c), it shows that subthreshold swing slope is lowered initially from 3.5 W to 4.0 W, however, it is enhanced slightly after 4.0 W. Since the subthreshold swing slope is usually made use of estimating the interface trap density in standard MOSFET technology. In poly-Si TFTs, the subthreshold swing slope is controlled by both bulk trap states and interface trap density near mid-gap [3.4].

The subthreshold swing slope *S* of poly-Si TFTs is given by

$$S=\frac{kT}{q}\cdot\ln 10\cdot\left(1+\frac{C_D+C_{ts}}{C_{ox}}\right) \quad \text{eq. 3-2}$$

where C_{ox} is the oxide capacitance per unit area, C_D is the depletion layer capacitance per unit area, and $C_{ts}=q^2D_{ts}$, where D_{ts} ($eV^{-1}cm^{-2}$) is the density of total trap states in the vicinity [3.1] of the intrinsic Fermi level. In poly-Si TFTs, the density of trap states near mid-gap D_{ts} includes both bulk trap density D_{bulk} and interface trap density D_{it}. Since the poly-Si film is thin and intrinsic, C_D 《 C_{ts} and the subthreshold swing slope of poly-Si TFTs is given by

$$S=\frac{kT}{q}\cdot\ln 10\cdot\left(1+\frac{C_{ts}}{C_{ox}}\right)=\frac{kT}{q}\cdot\ln 10\cdot\left(1+\frac{q^2\cdot D_{ts}}{C_{ox}}\right) \quad \text{eq. 3-3}$$

Considering that in a first approximation the devices are fully depleted, i.e., the energy band bending occurs over the whole poly-Si film thickness, the D_{ts} can be approximated as

$$D_{ts}=D_{bulk}\cdot t_{Si}+D_{it} \quad \text{eq. 3-4}$$

Where D_{bulk} is the mean bulk trap density, t_{Si} is the poly-Si film thickness, and D_{it} is the interface trap density.

Following above equations, subthreshold swing slope of poly-Si TFTs is reflected by bulk trap density and interface trap density. As the grain boundaries defects are terminated by increasing laser power, the subthreshold swing slope is decreased. However the reversal phenomenon of subthreshold swing slope is speculated on increasing interface trap density. It will be discussed in detail in chapter 4.

3.2 Density of states extraction using FEC method

Fortunato et al. had been proposed that poly-Si can be modeled using the "effective-medium" approach, in which the effects of grain boundary defects and intragranular defects are assumed to be uniformly distributed throughout the material [3.5]. This indicates that a model based on a spatially uniform distribution of gap states, such as those developed for amorphous-Si, constitutes a good and reasonable approximation [3.6]-[3.8].

3.2.1 Determination of flat-band voltage

The temperature method that is based on the temperature dependence of $\partial G/\partial V_G$ is used to calculate flat-band voltage. The equation is expressed by Weisfield and Anderson [3.9]:

$$\frac{\partial \log G}{\partial V_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 \ldots\right] \quad \text{Eq. 3-5}$$

The flat-band voltage (V_{FB}) can be determined as the gate voltage where $T\cdot\left(\partial \log G/\partial V_G\right)$ is temperature independent.

3.2.2 Current-voltage and surface band-bending

The incremental method [3.10] is utilized to establish the relationship between surface band-bending and current-voltage (I_d-V_g) characteristics. The field conductance is defined as [3.11]:

$$G = G_0 - \frac{G_0}{d}\int_0^{\psi_s} \frac{\exp\left(q\psi/KT\right)-1}{\partial\psi/\partial x}\partial\psi \quad \text{Eq. 3-6}$$

Where G_0 stands for the conductance for the flat band condition and d is the thickness of

poly-Si film.

The electric field of the semiconductor surface can be given from the voltage drop at the surface:

$$\frac{\partial \psi}{\partial x}|_{x=0} = -\frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{0x}}{t_{0x}} = -\frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_G - V_{FB} - \psi_s}{t_{0x}} \quad \text{Eq. 3-7}$$

Differentiating Eq. 3-6 and immediately substituting the Eq. 3-7 into the result, the following equation can be expressed:

$$\frac{\partial \psi_s}{\partial G} = \frac{1}{G_0} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{d}{t_{0x}} \cdot \frac{V_G - V_{FB} - \psi_s}{\exp(q\psi_s / KT) - 1} \quad \text{Eq. 3-8}$$

Substituting the field conductance into the drain current in Eq. 3-9 and the relationship between surface band-bending and current-voltage shows in Eq. 3-9 can be obtained by rewriting Eq. 3-8:

$$\frac{G_{i+1} - G_i}{G_0} = \frac{I_{D,i+1} - I_{D,i}}{I_{D,0}} \quad \text{Eq. 3-9}$$

$$\psi_{s,i+1} = \psi_{s,i} + \frac{I_{D,i+1} - I_{D,i}}{I_{D,flatband}} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i} - V_{FB} - \psi_{s,i}}{\exp(q\psi_s / KT) - 1} \quad \text{Eq. 3-10}$$

Placing the initial condition that $\psi_{s,i=0} = 0$, we can calculate $\psi_{s,1} \cdots \psi_{s,N}$ for $V_{G,1} \cdots V_{G,N}$.

3.2.3 Density of states (DOS) extracted from the band bending

The band bending is a solution of the one-dimensional Poisson's equation:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_{Si}} \quad \text{Eq. 3-11}$$

Where ε_{Si} is the poly-Si dielectric constant and ρ(x) is the local space-charge density. For

gate voltage below threshold, the free-carrier concentration can be neglected and sufficiently low temperatures:

$$\rho(x) = -q\int_{E_F}^{E_F+q\psi} N_g(E)\partial E \qquad \text{Eq. 3-12}$$

where $N_g(E)$ is the average gap state density. After multiplying by $2\partial\psi/\partial x$ and integrating from x=0 to x=d (oxide-semiconductor interface to bottom of channel),

$$\left(\frac{\partial\psi}{\partial x}|_{x=0}\right)^2 = \frac{2q}{\varepsilon_{Si}}\int_0^{\psi_s}\partial\psi_s'\int_{E_F}^{E_F+q\psi} N_g(E)\partial E \qquad \text{Eq. 3-13}$$

Where is the band bending at x=0. The density of state is expressed by

$$N_g(E_F+\psi_s) = \frac{\varepsilon_{Si}}{2q}\frac{\partial^2}{\partial\psi_s{}^2}\left(\frac{\partial\psi}{\partial x}|_{x=0}\right)^2 \qquad \text{Eq. 3-14}$$

where $E_F, \psi_s, \varepsilon_{Si}$ are Fermi energy, surface band bending at poly-Si film/gate-oxide interface, and dielectric constant of silicon, respectively.

3.2.4 Density of states (DOS) extracted for CLC poly-Si TFT

The CLC poly-Si TFT was measured the Id-Vg curves with the different temperature (25-150 °C), as shown in Figure 3-3. Figure 3-4 was shown the value of $T\cdot(d\log G/dV_g)$ was calculated and fitted for some gate voltage (V_g). Satisfied smallest slope of fitting curve is mean $T\cdot(d\log G/dV_g)$ is independent of the temperature. For this case, the value of -1 V is defined as the flat-band voltage. The surface band-bending and gate voltage was obtained with incremental method in Figure 3-5 and density of state was extracted in Figure 3-6.

3.3 Extracted channel resistance and the parasitic resistance by output characteristics

Laser activation engineering is a promising and useful technology for achieving high level poly-Si TFTs and advanced short channel devices. However, Busta et al. had been observed for short channel device where a reduction in the field mobility with the decrease of the channel length [3.12]. This effect has been generally attributed to the increased weight of the parasitic resistance at short channel lengths. From previous studies, these two contributions, of parasitic resistance and surface scattering, provided a full explanation of transconductance degradation across the range of TFT channel lengths from 1μm, where parasitic resistance dominated, to 60μm, where surface scattering dominated [3.13].

3.3.1 Determination of the R_{on}, R_{ch}, and R_p

For small drain voltages, V_d, at high gate voltage is assumed that the TFT ON resistance, R_{on}, consists of the channel resistance, R_{ch}, and the parasitic resistance, R_p.

That is,

$$R_{on} = \frac{\partial V_d}{\partial I_d}\Big|_{Vd\to 0}^{Vg} = R_{ch} + R_p \qquad \text{eq. 3-15}$$

and the channel resistance in the linear region is given approximately by

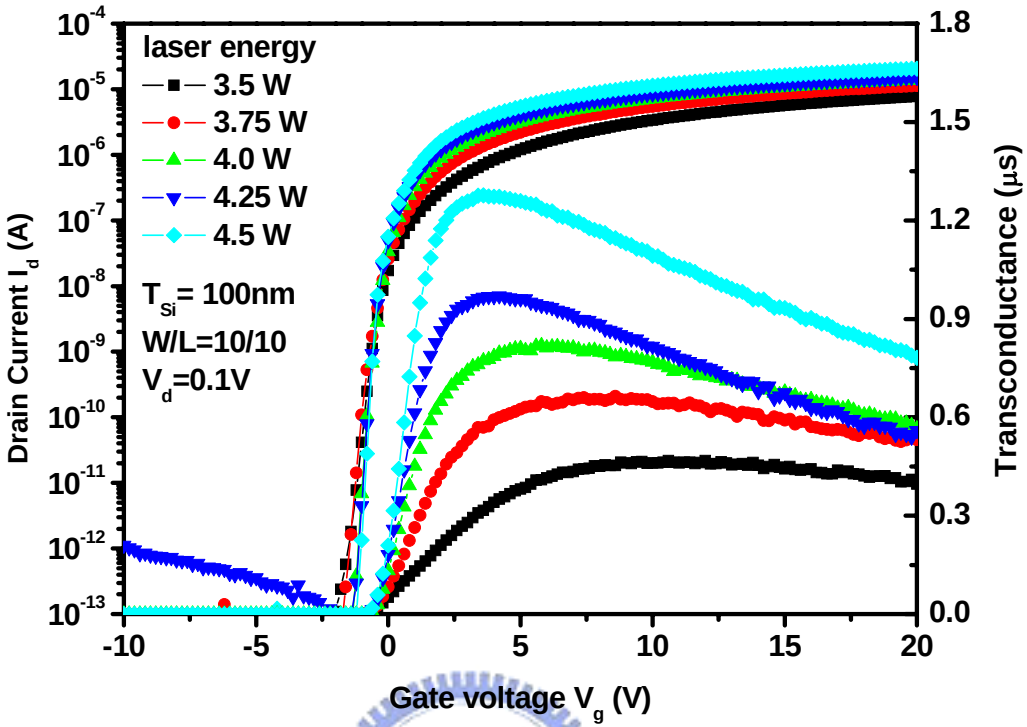
$$Rch = \frac{L}{W\mu C_i\left(V_g - V_{th}\right)} \qquad \text{eq. 3-16}$$

where C_i is the gate dielectric capacitance per unit area and W, L, and V_{th} are device channel width, length, and threshold voltage, respectively. The parasitic resistance R_p can be extracted by measuring the ON resistance, R_{on}, from the linear region of the TFT output

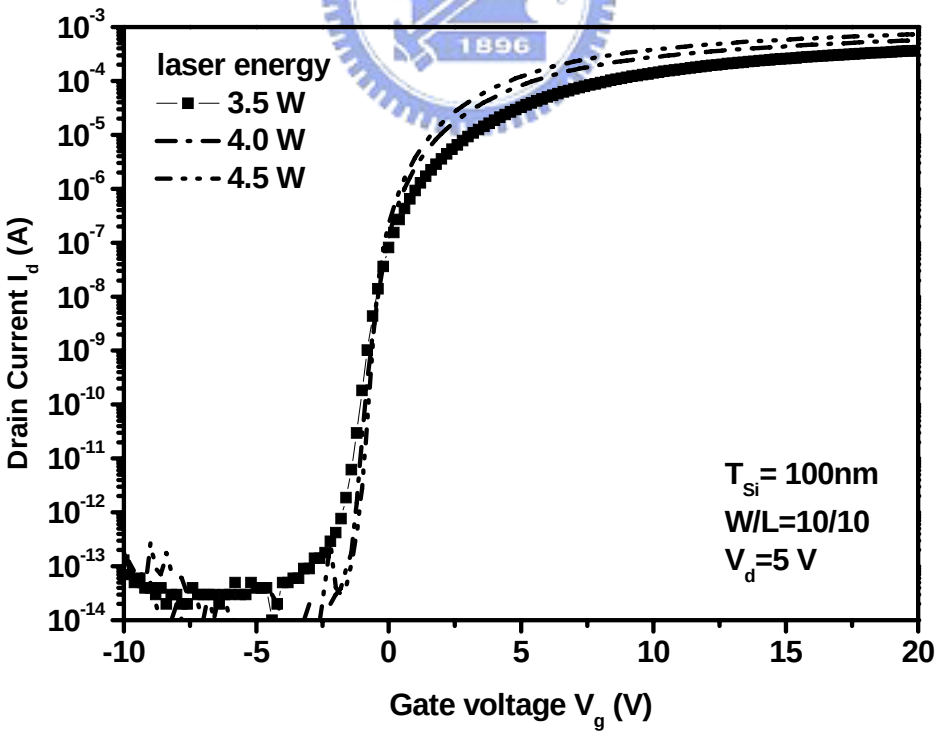
characteristics and by plotting R_{on} as a function of L [3.14].

3.3.2 Parasitic resistance measured for CLC poly-Si TFT

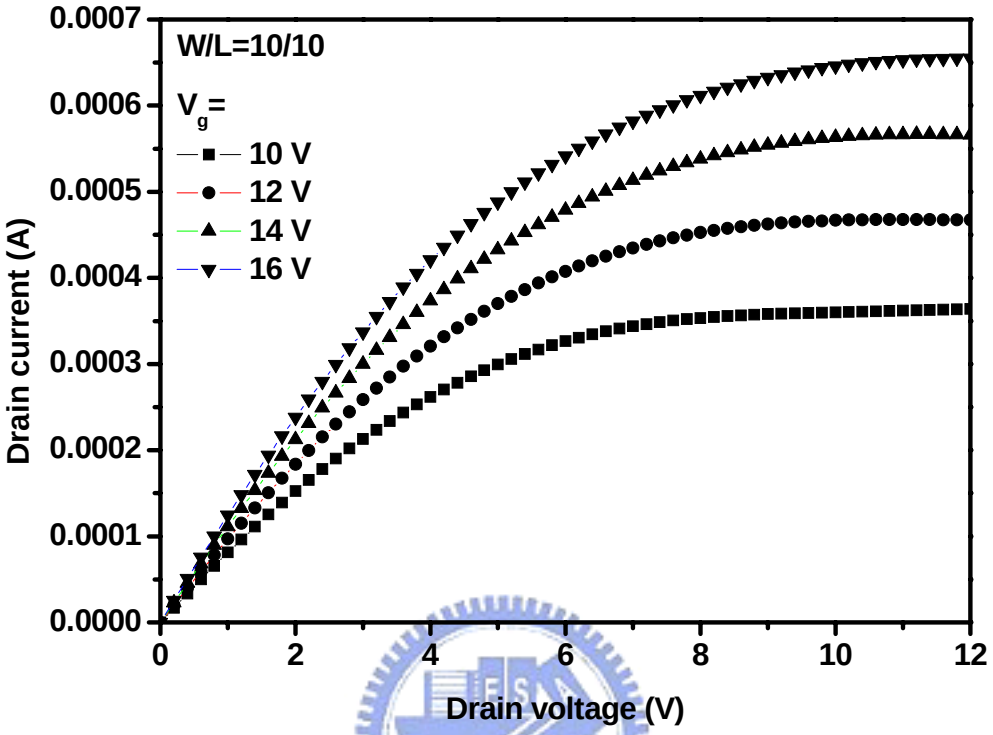
As the ON resistance and parasitic resistance can be extracted from the output characteristics of devices with various channel length. For example, the transfer characteristics of n-channel CLC poly-Si TFT with W=10μm and L=5μm is shown in Figure 3-7 (a) that the fabricated CLC poly-Si with high drive current and steep swing slope are similar the results in the Figure 3-1. The output characteristics of the CLC poly-Si TFT are depicted in Figure 3-7 (b). For obtaining On resistance and parasitic resistance, the linear region in Figure 3-7 (b) is fitted by least square regression. The parasitic resistance can be extracted by plotting width-normalized R_{on} versus L as in Figure 3-8. It is found that the value is 1.2 kΩ at the gate voltage independent parasitic resistance.


laser energy
3.5 W
3.75 W
4.0 W
4.25 W
4.5 W
T_Si= 100nm
W/L=10/10
V_d=0.1V
Drain Current I_d (A)
Transconductance (μs)
Gate voltage V_g (V)

(a)

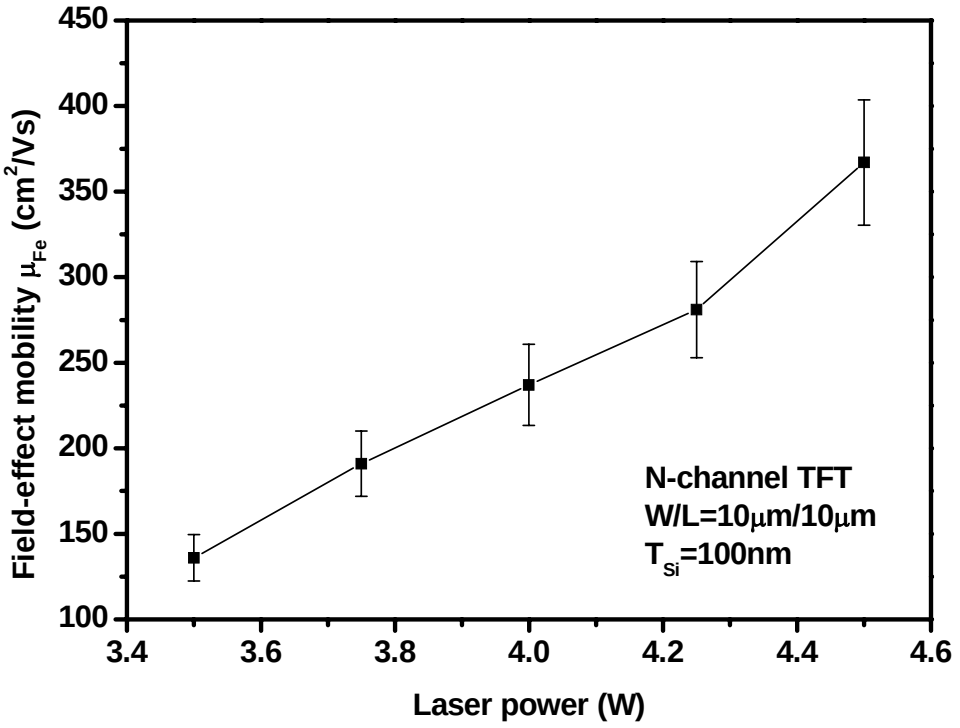

laser energy
3.5 W
4.0 W
4.5 W
T_Si= 100nm
W/L=10/10
V_d=5 V
Drain Current I_d (A)
Gate voltage V_g (V)

(b)

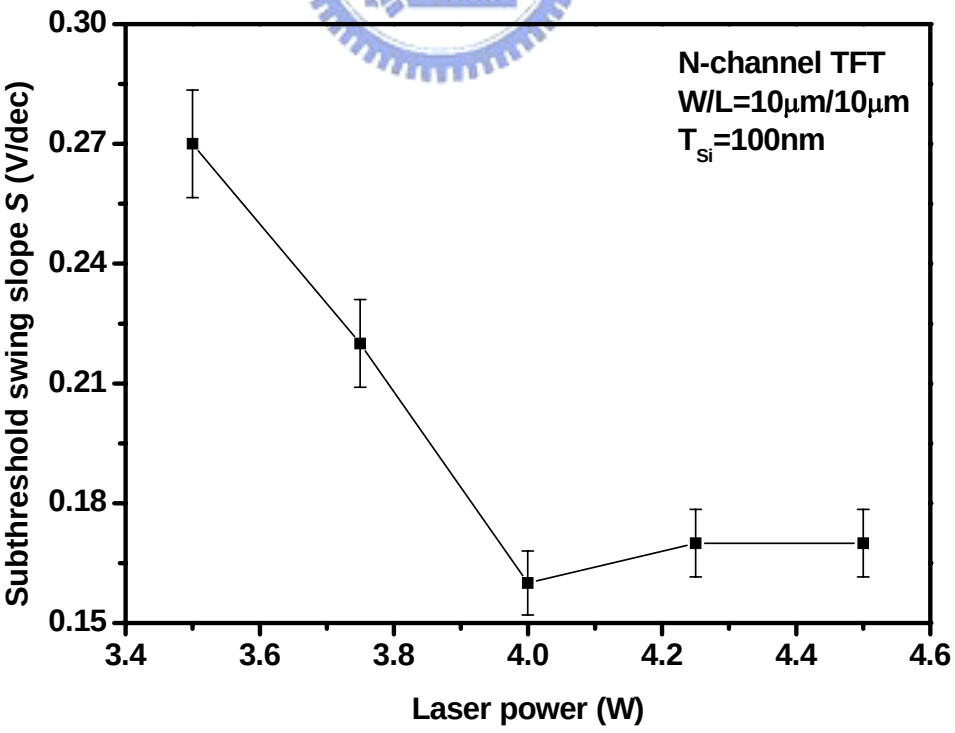


(c)

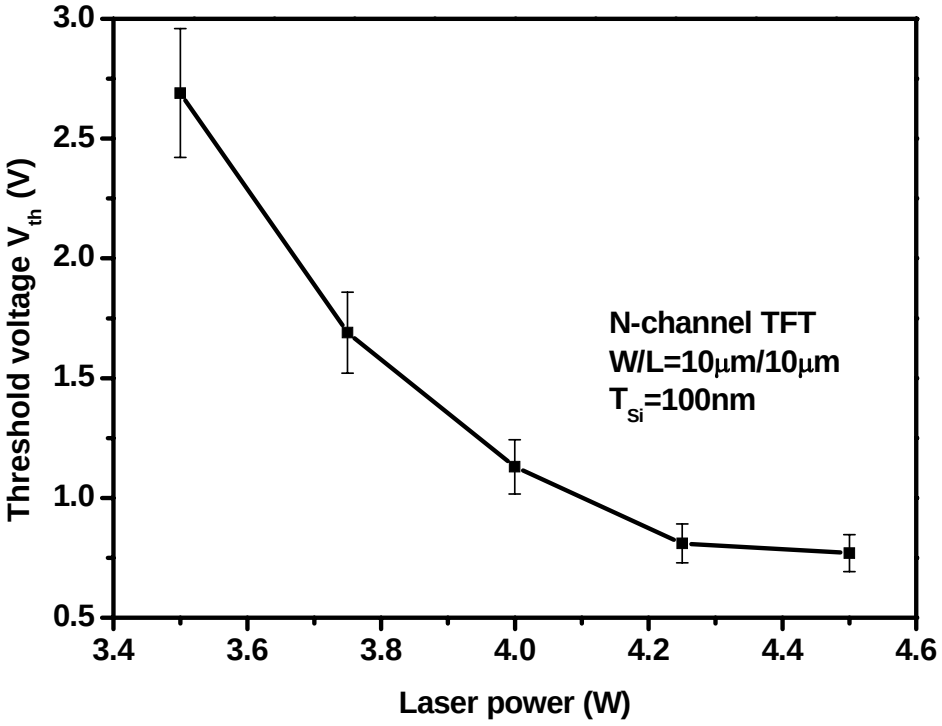
Figure 3-1 (a) Transfer characteristics and transconductance curves of polysilicon TFTs made from CLC at different laser energy (b) Transfer characteristics curve at V_d=5V (c) I_d-V_d current of 4.25 W crystallized poly-Si TFT


Field-effect mobility μ_{Fe} (cm^2/Vs)
Laser power (W)
N-channel TFT
W/L=10μm/10μm
T_{Si}=100nm

(a)


Subthreshold swing slope S (V/dec)
Laser power (W)
N-channel TFT
W/L=10μm/10μm
T_{Si}=100nm

(b)



(c)

Figure 3-2 Electrical characteristics dependence on CLC poly-Si TFTs with 100nm-thick active layer with the different laser energy (a) field-effect mobility, (b) threshold voltage, (c) subthreshold swing slope

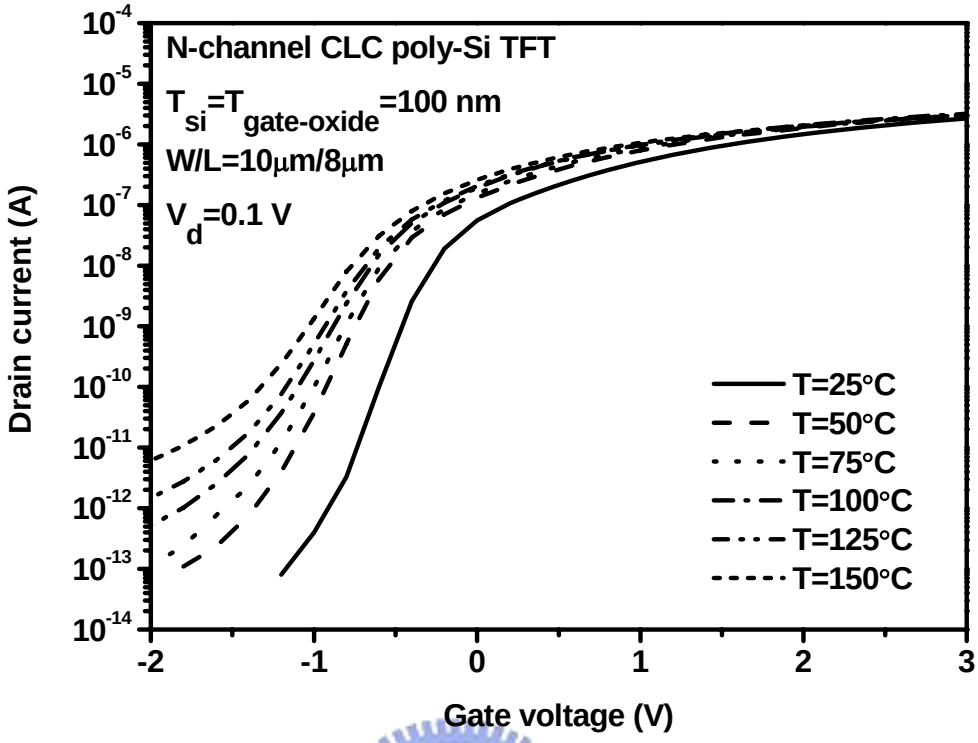


Figure 3-3 Electrical characteristics at different temperatures.

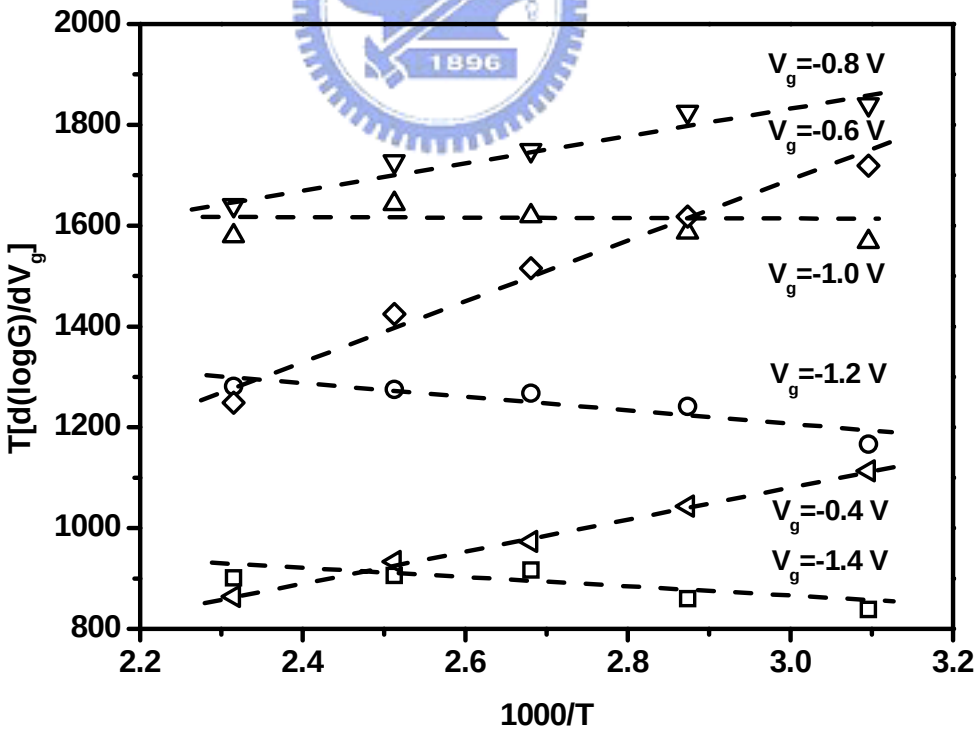


Figure 3-4 Plots of $T \cdot \left(d \log G / dV_g\right)$ as a function of temperature.

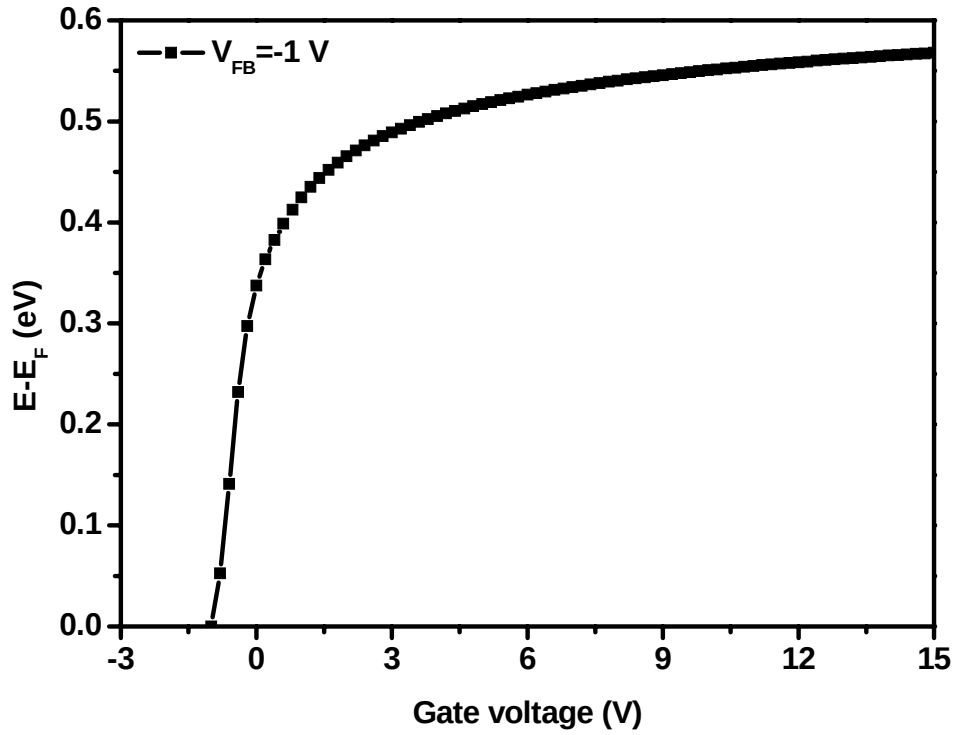


Figure 3-5 Surface band-bending as a function of gate voltage.

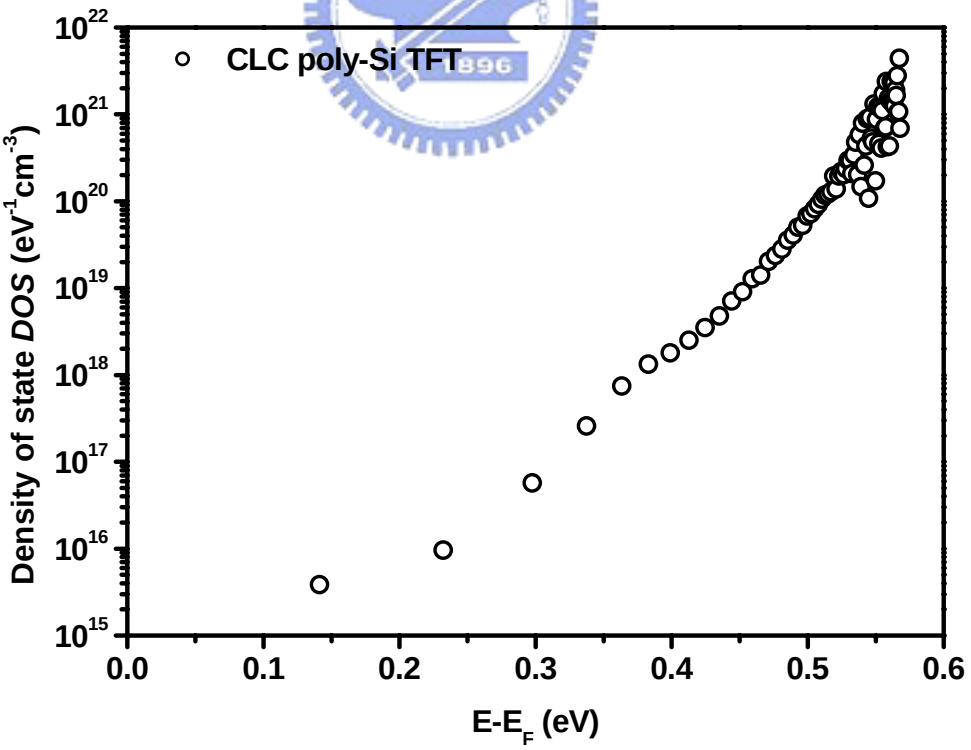


Figure 3-6 Extracted density of state as a function of surface band-bending.

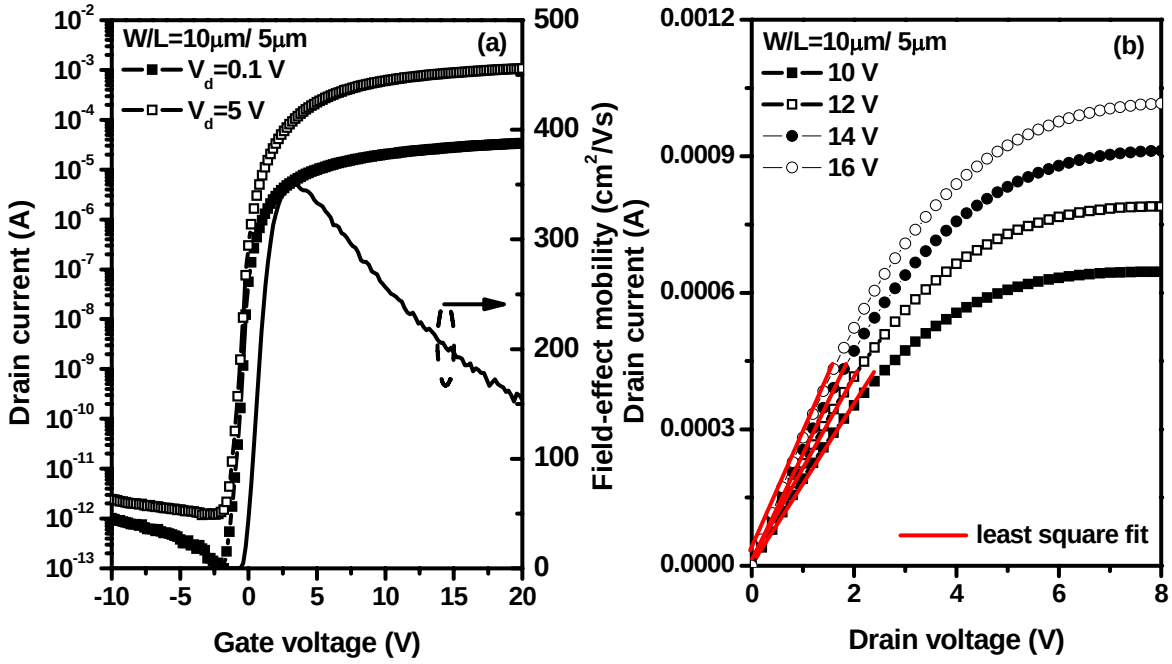


Figure 3-7 (a) Typical transfer characteristics of n-channel CLC poly-Si TFT with W=10μm and L=5μm. (b) ON resistance measurement in the linear regions of the CLC poly-Si output characteristics.

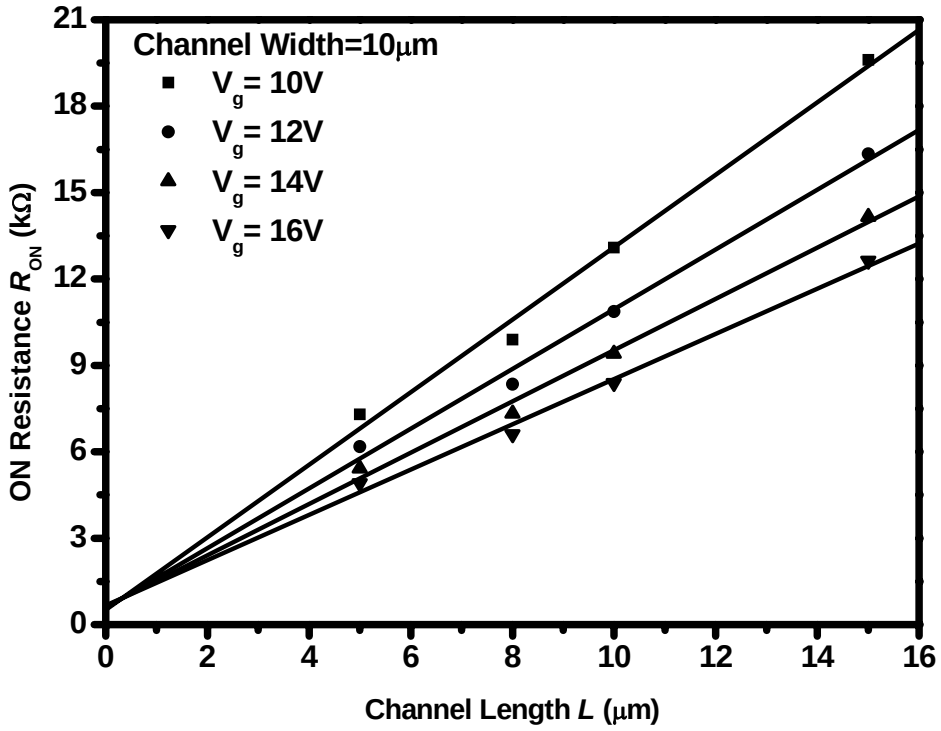


Figure 3-8 ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data. The channel width is fixed at 10 μm.

Chapter 4

Trap-state density and Stability of continuous-wave laser-crystallized epi-like silicon transistors

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4.1 Introduction

Recently, high-performance polycrystalline silicon thin-film transistors (polysilicon TFTs) on glass substrates have been implemented. They depend on the formation of laser-crystallized single-grain-like channels by sequential lateral solidification (SLS) [4.1][4.2]. The supply of photo-energy from CW green lasers facilitates the lateral crystallization of amorphous silicon (a-Si), even in the absence of capping layers and laser power masking [4.2]. Hence, CLC is more practical than excimer-laser-annealing-based (ELA) SLS [4.1][4.2].

A high laser power is commonly adopted to enhance the channel crystallinity in an attempt to improve all of the electrical characteristics of laser-crystallized polysilicon TFTs [4.3]. However, doing so also roughens the channel surfaces while degrading the threshold voltage and the sub-threshold slope, as reported by Angelis et al. in relation to ELA polysilicon TFTs [4.4]. A high-speed and reliable transistor should have a thin channel, which fact explains why interfacial properties dominate the performance of transistors. Accordingly, the surface roughness of thin CLC channels is a major concern. Several methods such as field-effect conductance (FEC) [4.5] and low-frequency noise methods [4.6],

have been developed and applied to measure channel quality in terms of the density of grain (grain boundary) and interface traps, which effectively specify the electrical parameters of the transistors [4.7]. Nevertheless, these issues have seldom been addressed for CLC-fabricated TFTs.

This study reveals an ultra-low trap-state density in CLC polysilicon, which is consistent with the demonstration of excellent electrical characteristics. Additionally, the formation of extra interface defects induced by the laser-crystallization-enhanced surface roughness (**LCESR**) leads to the reversal of deep-state density and, thus, the subthreshold slope, as well as a saturating reduction in threshold voltage.

Accordingly, two laser annealing approaches, CLC [4.8] and SLS [4.9], have attracted substantial interest due to their usefulness in the formation of epi-like microstructures and the maintenance of low surface roughness on crystallized channels [4.10].

Voutsas *et al.* investigated the dependence of degradation mechanisms on the thickness of SLS channels [4.11]. Changes in the degradation of electrical parameters that are caused by hot-carrier stressing (***HCS***) and related to channel thickness, were attributed to crystalline quality and partial depletion-induced carrier accumulation. However, in laser-induced crystallization methods, the thickness of irradiated films simultaneously affects channel crystallinity and roughness [4.12]. Hence the dependence of channel roughness and device reliability on the thickness of CLC channels warrants further study.

This investigation explores the mechanisms of degradation of CLC epi-like Si TFTs during

HCS, with reference to channel thickness.

4.2 Hot-carrier effect degradation

The large voltage drop across the pinch-off region results in a high lateral electric field close to the drain region. The carriers traversing this high field obtain energies which are higher than the equilibrium thermal energy in the semiconductor. These high energy carriers can be called hot-carriers. The hot carrier degradation will result from heating and subsequent injection of carriers into the gate oxide, which results in a localized and non-uniform buildup of interface states and oxide charges near the drain junction of MOSFET. In general, the created defect states produce threshold voltage shift, transconductance degradation, reduction of drain current, etc., and finally cause devices failure in the long term electrical stressing [4.13]-[4.16].

Reliability of poly-Si TFTs is one of the main concerns, especially when devices are operated under high drain and high gate voltage [4.4][4.7]. Many investigations have already been carried out the stability of poly-Si TFTs in which grain boundary defect states generation, interface states formation and injected carrier into gate oxide. All of the generated defect states can also result in electrical parameters degradation including in transcondutance, threshold voltage and subthreshold swing slope [4.4][4.7][4.11]. Beside, hot-carrier generation rates are significantly lower for p-channel than n-channel transistors. This is due to the lower impact ionization rate for holes. However, the greater peak gate

current is measured for p-channel transistors and the hole mobility in oxide is considerably smaller than that of electrons to cause higher getting trapped. The density of interface states at Si-SiO_2 interface and charges in the gate oxide will alter device current characteristics which can reduce the operating lifetime of these devices. In this study, it is very important point to explore the reliability of CLC poly-Si TFTs.

4.3 Experimental setup

The experiment was begun by sequentially depositing a 50 nm-thick layer of SiN_x, a 150 nm-thick layer of SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) on a Corning Eagle 2000 glass substrate. These poly-Si channels were formed by the CW green laser-crystallization of amorphous silicon islands with thicknesses of 50nm and 150nm, which were deposited by plasma-enhanced chemical vapor deposition (PECVD) on 150 nm-thick layer of SiO_2. Before laser crystallization, the deposited a-Si films were patterned into individual islands of 60μm /76μm (width/length) as active layers of TFTs to prevent peeling [4.2]. A solid-state CW green (**λ=532 nm**) laser with an output power of 3-5 W was then guided to crystallize islands laterally by line-scanning the samples at 10 cm/s. CLC experiments are conducted in ambient air at room-temperature and the laser beam is incident on samples with a strip spot of 220μm×40μm. In devices, PECVD SiO_2 grown at 380 ^{0}C with a thickness of 100 nm is applied as a gate dielectric. Source and drain regions that had been implanted with PH_3 ($5.0x10^{14}cm^{-2}$ and 25 keV) for n-type TFTs and B_2H_6 ($5.0x10^{14}cm^{-2}$

and 40 keV) for p-type TFTs were activated by rapid thermal annealing. The stability of fabricated devices with width/length= 60 μm/60 μm during ***HCS*** at room temperature was examined. As ***HCS*** proceeded, the transfer characteristics (drain current I_d versus V_g) of the devices were measured at V_d= -0.1 V, to extract transient electrical parameters [4.17][4.18]. Grain trap-state densities, n_{GT}, for all TFTs were examined using the field-effect conductance method [4.5].

4.4 Results and discussion

4.4.1 Electrical characteristics with different applied laser energy

On various crystallite channels, TFTs are fabricated with conventional polysilicon TFTs. Figure 4-1 plots logarithmic transfer (drain current I_d versus gate voltage V_g) characteristics and linear transcondcutance (G_m) curves for some representative TFTs, when a drain voltage V_d of 0.1 V was applied. Next, the maximum G_m was analyzed to yield the field-effect electron mobility (μ_{FE}), and the threshold voltage (V_{th}) was determined by linear extrapolation of the transcondcutance to zero [4.19]. In the poly-Si TFTs with small grains, threshold voltage can not always be determined by conventional linear extrapolation method since the slope of the transfer characteristic increases with increasing gate voltage. Thus, there is an increasing need for a reliable threshold voltage extraction method in TFT devices with discrete grains as the channel becomes shorter and grain size becomes larger.

The subthreshold slope (***S***) was also extracted from the maximum slope of the transfer

curves, plotted on a semilog scale. Figure 4-2 plots the subthreshold slope, the threshold voltage and the leakage current (at V_d=10 V) against field-effect mobility (laser power).

As expected, increasing the laser fluence increases the efficiency of grain lateral-growth, forming larger grains with fewer associated defects, while considerably reducing the height of the barrier to carrier transportation in the channels, associated with a higher G_m (Fig. 4-1), such that μ_{FE} is as plotted in Fig. 4-2 [4.20].

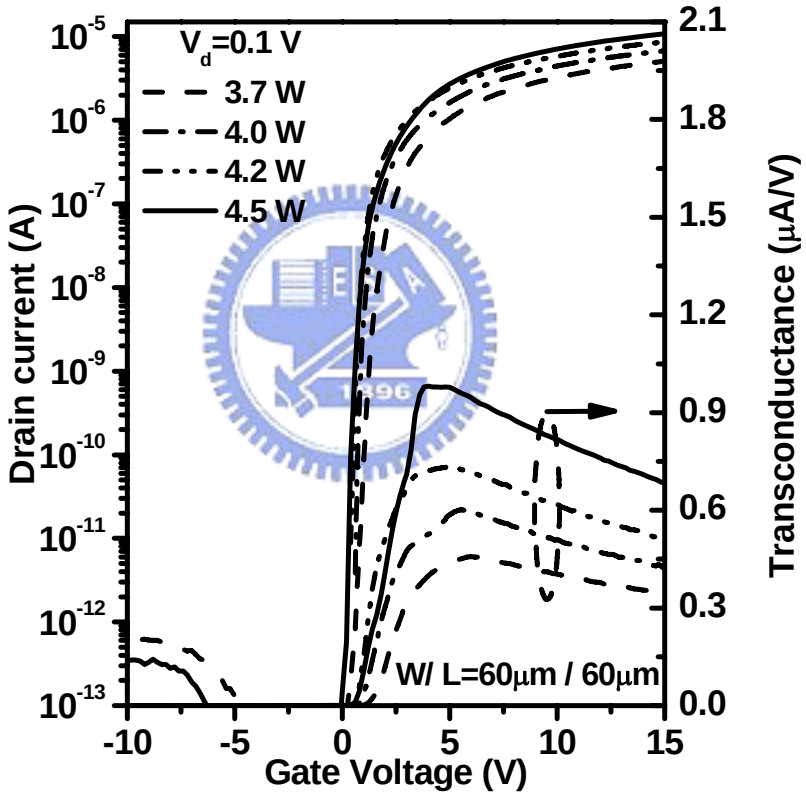


Figure 4-1 Transfer characteristics and transconductance curves of polysilicon TFTs made from CLC at laser powers of 3.7, 4.0, 4.2 and 4.5 W.

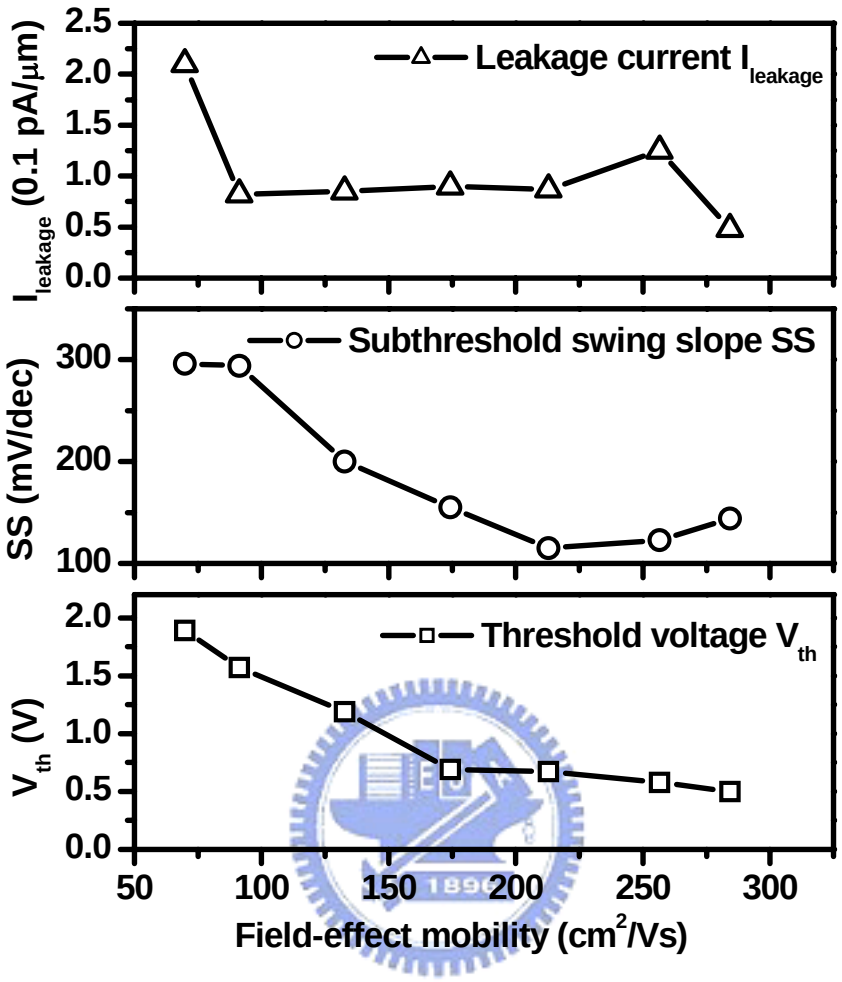


Figure 4-2 Threshold voltage, subthreshold slope and minimum leakage current for polysilicon TFTs made using CLC at different laser powers in the range 3-4.5 W.

4.4.2 Electrical characteristics in relation to density of states

Next, the densities of states (DOS) of traps are examined using the FEC method for CLC-fabricated TFTs, with reference to the crystallization conditions, as presented in Figure 4-3. As the laser power increases to 4.5 W, the tail-state density clearly decreases to $3x10^{19}$ $eV^{-1}cm^{-3}$ at $E-E_F=0.52$ eV where E_F is the midgap energy, whose value is almost one order of magnitude lower than that obtained from ELA-fabricated TFTs (See Figure 4-3) [4.21][4.22]. The enlargement of grains in channels as the laser power increases not only reduces the density of grain defects but also relieves the distortion of bonds in highly crystalline silicon [4.22][4.23]. Therefore, channel crystallinity is strongly related to the density of distorted-bond defects, regarded as the origination of tail states. Hence, the tail-state density declines as the laser power increases, as shown in Figure 3-4, and as indicated by ELA-related results reported elsewhere [4.22]. Extremely low tail-state densities associated with large grains in CLC polysilicon are responsible for the high μ_{FE} of 284 cm^2/Vs, independently of surface roughness.

Closely examining the four transconductance (G_m) curves in Figure 4-1 reveals that the slope at which G_m is away from the ascending stage and declines with V_g increases with the laser power. As the surface roughness increases, the mobility reduction at high gate voltages is increased because the surface scattering increases [4.23], which relation is consistent with the transconductance data. Note that the electric field enhanced at the rough polysilicon/SiO_2 interface [4.24] assists the electrons to be injected into the gate oxide [4.4].

In Figure 4-2, the threshold voltage decreases more slowly as the laser power increases above 4.0 W, suggesting that the injected electrons are trapped as negative charges in the oxide. The negative trapped charge reduces the electrical field near the drain, reducing the leakage current at high laser power (See Figure 4-2) [4.4].

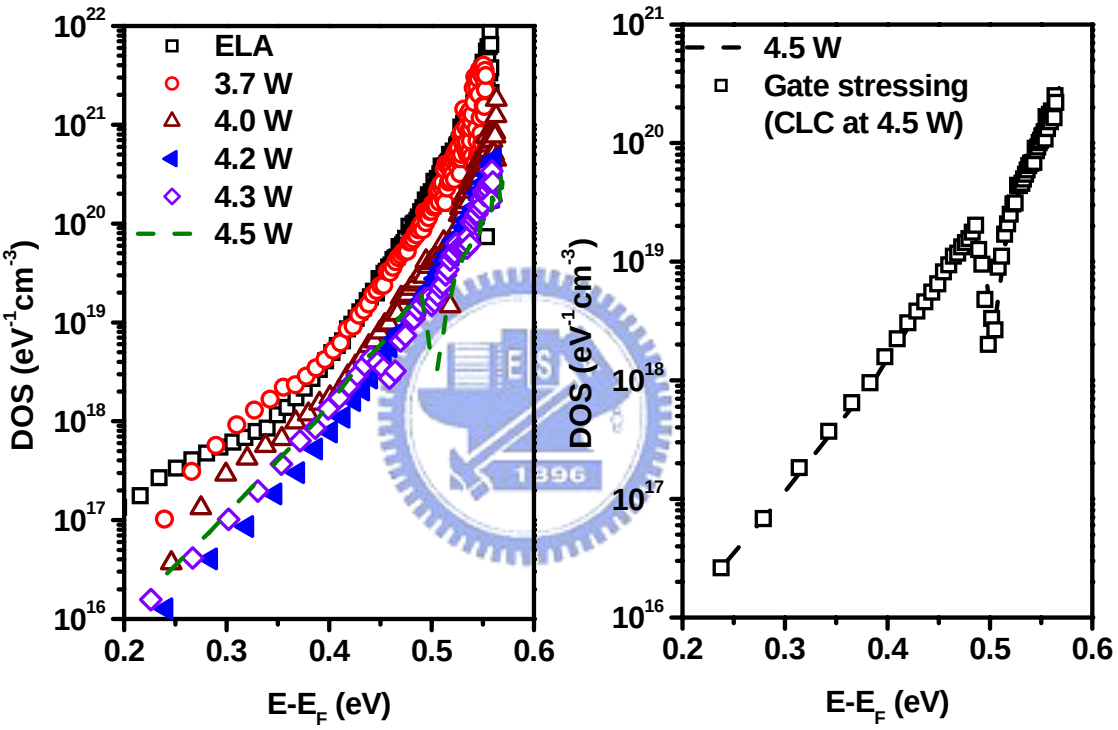


Figure 4-3 Energy distribution of DOS for polysilicon TFTs made using CLC at laser powers of 3.7, 4.0, 4.2, 4.3 and 4.5 W. For comparison, the DOS distribution for ELA-fabricated TFTs with μ_{FE} of 140 cm^2/Vs, V_{th} of 1.5 V, and S of 180 mV/dec is also presented.

4.4.3 Reliability of CLC poly-Si TFTs

The charge trapping mechanism can be further investigated by gate stressing and hot-carrier stressing [4.25][4.26]. Figure 4-4 plots the V_{th} shift (ΔV_{th}) versus the stressing time (t) for CLC-fabricated TFTs made at a laser power of 4.5 W during gate stressing (V_g=20 V and V_d=0 V) and hot-carrier stressing (V_g=8 V and V_d=16 V). The former test demonstrates a logarithmic time-dependence of ΔV_{th}, which is indicative of charge trapping in gate dielectrics. Moreover, the latter test indicates the power-law time dependence of ΔV_{th} with exponents of 0.25 ($\sim t^{0.25}$), as opposed to power-law exponents in the range of 0.4-0.6 associated with deep-state generation [4.26]. Comparing DOS distributions before and after either gate stressing (See Fig. 4-3) or hot-carrier stressing (not shown herein) shows almost overlapping trap-state densities. Hence, slightly roughened CLC polysilicon/SiO_2 merely induces charge trapping but trapped electrons into the gate oxide or at the interface create hardly any new deep-states.

Increasing the laser power initially reduces the deep-state densities, unlike the tail-state density, to as low as $1.0\text{x}10^{16}$ $eV^{-1}cm^{-3}$ at $E\text{-}E_F$=0.25 eV, and then increases it to $3\text{x}10^{16}$ $eV^{-1}cm^{-3}$. Deep-state densities extracted at other energetic states of $E\text{-}E_F$=0.25-0.35 eV also exhibit the same trend. Low-frequency noise measurements indicate that roughened surfaces formed extra interface traps [4.4][4.6][4.7], which are responsible for the reversal in the deep-state density [4.27]. For ELA polysilicon, the impact of LCESR on the deep-state density is difficult to observe because in such a material, the deep-states density is as high as

$5x10^{17}$ $eV^{-1}cm^{-3}$ (at $E-E_F=0.25$ eV), exceeding that of polysilicon-oxide traps, $3x10^{17}$ $eV^{-1}cm^{-3}$.[4, 12] The deep-state density of smooth and single-grain-like CLC polysilicon is below 10^{17} $eV^{-1}cm^{-3}$, causing LCESR to change the deep-states to reverse the decline, despite the fact that increasing channel crystallinity normally reduces the density of the grain defects, including deep-states defects. Therefore, the deep state- and/or the interface state-dominated subthreshold slope follow the variation in deep-states densities with laser power (See Fig. 4-2 and Fig. 4-3) [4.28][4.29].

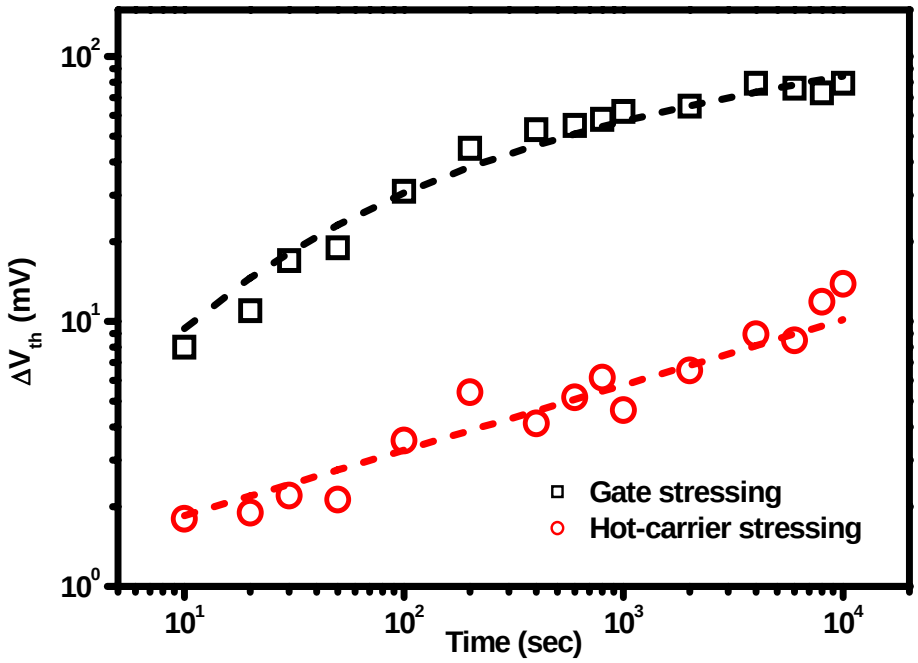


Figure 4-4 ΔV_{th} transients for CLC polysilicon TFTs made at laser power of 4.5 W during gate-stressing and hot-carrier stressing. Curve-fitting is also shown. The DOS distribution for the same device after gate stressing is also shown in Figure 3-4.

4.5 Thickness effect of active layer with CLC technology

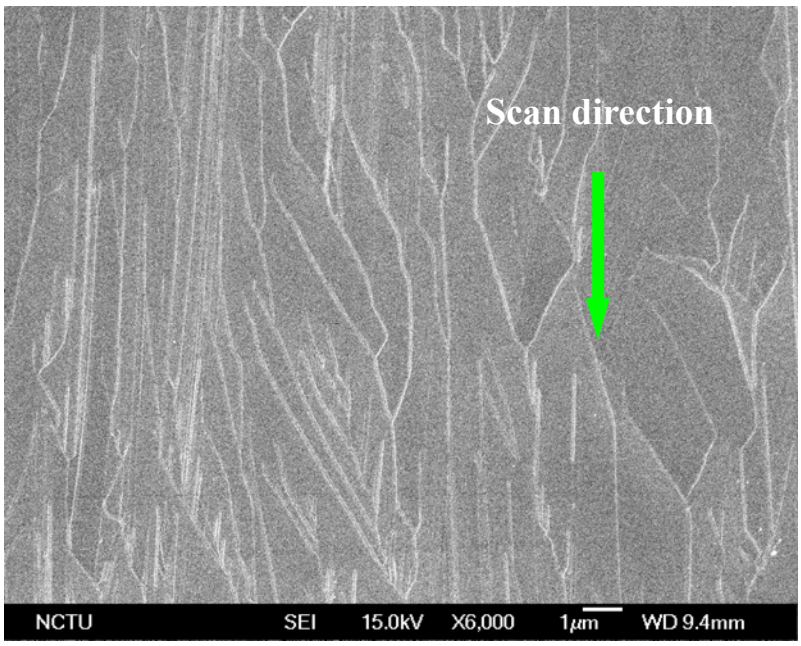
4.5.1 SEM and AFM observation of CLC channel with different thickness

Voutsas et al. were conducted that the Si film thickness was found to affect significantly the quality of the poly-Si microstructure, manifested by a decreased crystal-growth defect density and increased subboundary spacing in thicker film. Because of the crystallinity in laser-crystallized films normally increases with film thickness [4.9], as revealed by the SEM images of CLC poly-Si (in the Figure 4-5). Since the laser penetrates to a depth into the a-Si estimated of 1μm because of the medium absorption coefficient of a-Si at the wavelength of 532 nm. The silicon is easily melted as the thickness of silicon is 50-150 nm. And the laser power is continuously supplied into the full silicon layer [4.1][4.2]. Table 4- Ⅰ shows the N&K analyzer at wavelength of 532 nm. The absorption ratio is increased with thickness of a-Si layer. Hence it is not similar like excimer laser annealing that needs to enhance laser energy density for thicker silicon film. From the SEM images of Figure 4-5, it is also very clearly to observe the larger grain size (3×10 μm) of 150 nm-thick silicon layer that is compatible with previous studies. The laser power is used at 4.2 W for 150 nm-thick and 4.5 W for 50nm-thick silicon layer. This is quite obvious that this laser power is plentiful for melting the silicon and causing the liquid-solid interface along scanning direction. Figure 4-6 and Figure 4-7 display the topographies of CLC poly-Si. The RMS of the 50 nm-thick and 150 nm-thick silicon layers is 3.6 nm and 4.2 nm, relatively. This relationship is responsible for the larger channel roughness on thicker films because larger grains lead to

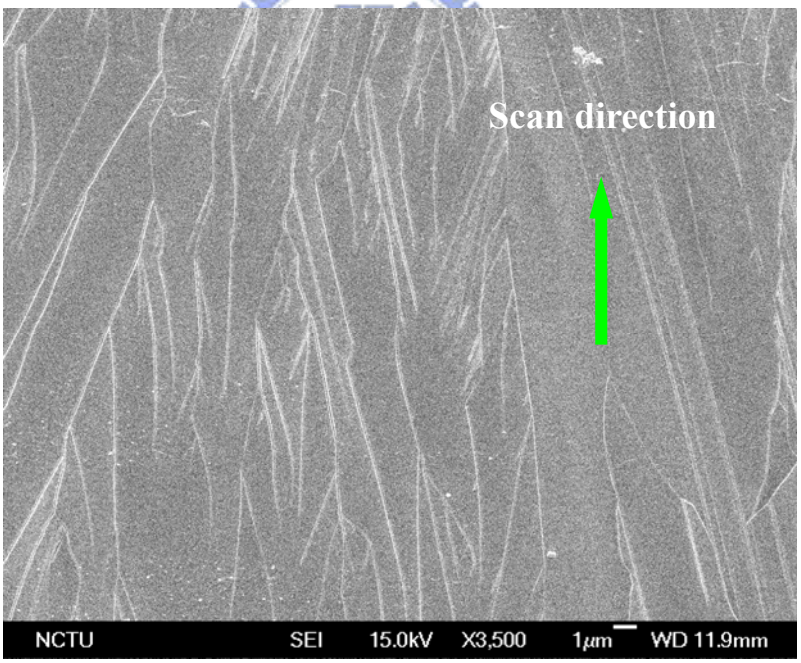
larger fluctuations in the surface profile [4.12].

Table 4- Ⅰ N&K analysis at 532 nm

At 532 nm	Absorption rate	Piercing through rate	Reflecting rate
50 nm a-Si	0.43	0.16	0.41
100 nm a-Si	0.52	0.07	0.41
150 nm a-Si	0.53	0.03	0.44
100 nm SiO_x	0.04	0.93	0.03



(a)



(b)

Figure 4-5 SEM image of different silicon thickness crystallized with CLC (a) 50 nm, 4.5 W, (b) 150 nm, 4.2 W.

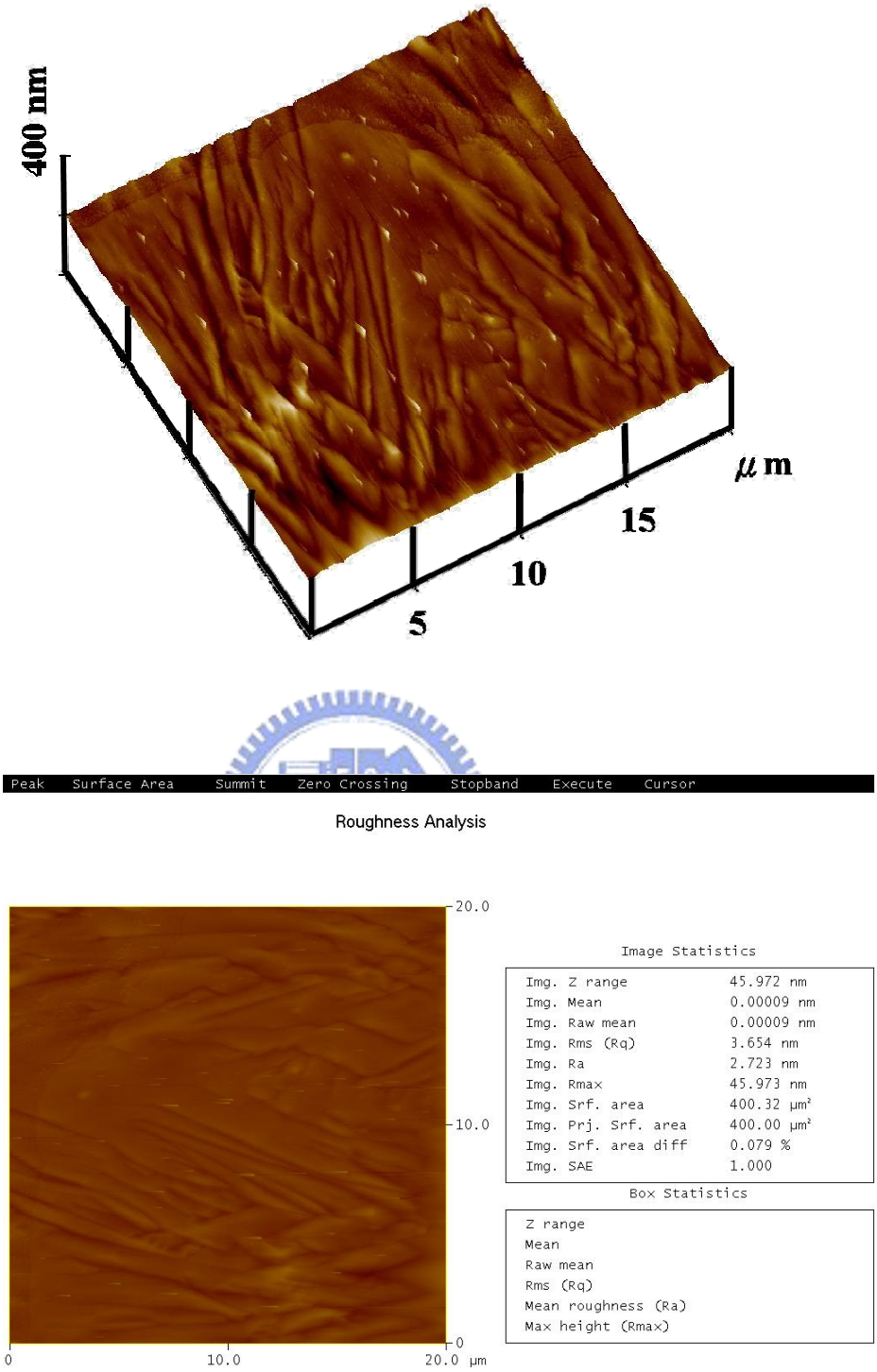


Figure 4-6 AFM topographies of CLC channels with thicknesses of 50nm.

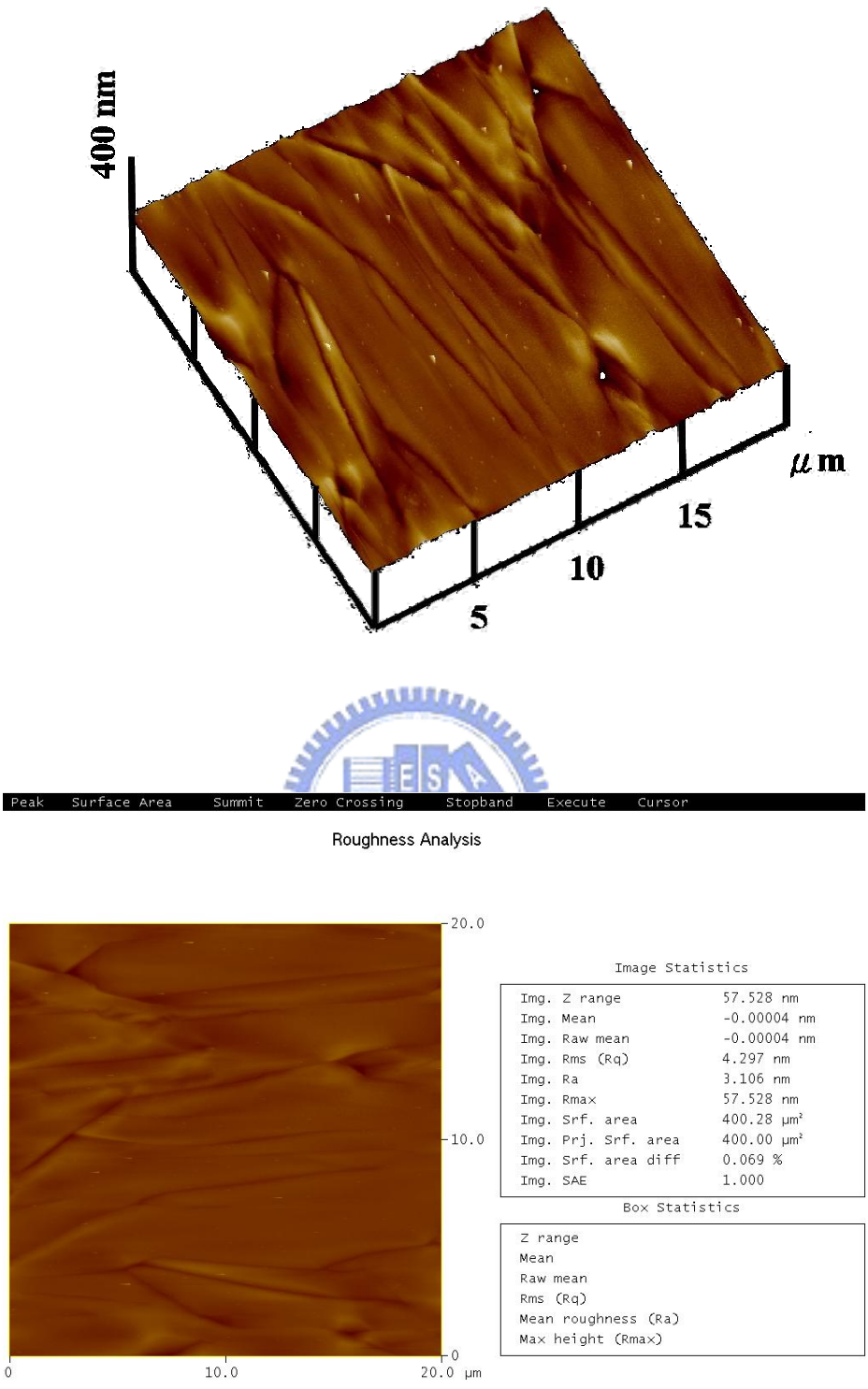


Figure 4-7 AFM topographies of CLC channels with thicknesses of 150nm.

4.5.2 Density of states of CLC channel with different thickness

Consequently, the tail-state density of grain traps, which was closely related to channel crystallinity [4.10], n_{GT} at an energetic level (E) that was far from the Fermi level (E_F), $\Delta E = E - E_F$ = -0.55 to -0.4 eV, was lower in thicker channels (Figure 4-8). Notably, the field-effect mobility (μ_{FE}) of TFTs was determined by the number of tail-states in such an epi-like CLC poly-Si of a particular thickness, rather than throughout the channel layer [4.30]. This finding explains why the μ_{FE} of devices obtained with CLC poly-Si with a thickness of 150 nm is as high as 315 cm^2/Vs, which is double that obtained with CLC poly-Si with a thickness of 50 nm, as revealed by the linear transcondcutance (G_m) curves plotted in Fig. 4-9.

4.5.3 Electrical characteristics and reliability of CLC channel with different thickness

Figure 4-9 plots forward and reverse transfer characteristics as well as transcondutance of fresh TFTs on CLC poly-Si with thicknesses of 50 nm and 150 nm and transient I_d-V_g curve of hot-carrier stressed TFTs with $V_g = V_d$=-20 V shows in Figure 4-10. Figure 4-11 (a)-(b) plots the transients of μ_{FE} and threshold voltage (V_{th}), and the degradation of the V_{th} shift (ΔV_{th}) and the normalized μ_{FE} shift ($\Delta\mu_{FE}/\mu_{FE0}$, where μ_{FE0} stands for initial μ_{FE}) for stressed devices in Figure 4-10 against film thickness and stress time (**t**). The degradation of $\Delta\mu_{FE}/\mu_{FE0}$ follows a power-law in time [4.31][4.32], with an exponent (β) of 0.28 ($\sim t^{0.28}$), and is independent of film thickness.

According to the carrier-induced defect creation model, the shift in threshold voltage

(V_{th}), ΔV_{th}, can be expressed as $\Delta V_{th}(t)=A.(V_g-V_{th}).t^n$ [4.17]. Furthermore, Takeda *et al.* found that the degradation of the normalized maximum transconductance (G_m) and, therefore, field-effect mobility (μ_{FE}) shift can be empirically modeled as $\Delta G_m/G_{m0}$ (or $\Delta\mu_{FE}/\mu_{FE0}$)~t^n [4.31]. However, a charge trapping model predicts that the instability in V_{th} is $\Delta V_{th} =\Delta V_{max}.[1-\exp(-(t/t_0)^n)]$ [4.18]. Under conditions of short stress time (t) or small exponent n, this formula is approximated as $\Delta V_{th} \sim(t/t_0)^n$. Therefore, the degradation in the electrical parameters due to bias stressing can be modeled as a power law of the form ~t^n, regardless of the instability mechanisms. Moreover, several studies have reported on the bias stress-induced instability in the electrical parameters of transistors, conferring that n=0.1-0.3 is related to hot-carrier injection while n=0.4-0.6 points towards deep-state creation [4.32][4.32]. In addition to transients of electrical parameters, this study also investigates grain and interface trap-state densities. Hence, the degradation mechanisms of CLC epi-like Si TFTs during hot-carrier stressing (***HCS*),** were explored with reference to channel thickness.

HCS negligibly changed the tail-state densities of grain traps in both channels (Figure 4-12). However, the power-law exponents associated with V_{th} degradation for thick and thin channels are 0.39 and 0.43, respectively, and are so not in the range 0.1-0.3, which is associated with hot-carrier injection [4.32][4.33].

Unlike μ_{FE}, V_{th} and the subthreshold slope (***S***) are governed by the numbers of interface and grain trap states per unit channel area, N_T [4.34][4.35], at ΔE ~0 to -0.3 eV, where ***S*** is

governed strongly by N_T near the intrinsic Fermi level (ΔE ~0 eV). For fresh TFTs, the areal density of grain trap-states, N_G, averaged over the range ΔE = 0 to -0.3 eV in thick CLC poly-Si was about $4.8\times10^{10}cm^{-2}eV^{-1}$ - less than that, $5.2\times10^{10}cm^{-2}eV^{-1}$ in thin CLC poly-Si, where N_G was estimated from $n_{GT}.t_{CLC}$ and t_{CLC} denotes the thickness of the CLC poly-Si. ***HCS*** clearly increased the n_{GT} of stressed TFTs at ΔE~ -0.1 to -0.3 eV in both channels (Figure 4-12), verifying that deep-state generation is involved in V_{th} degradation. Moreover, after ***HCS***, V_{th}, the averaged N_G and the change in n_{GT} at the deep energetic level in the thick channel exceed inversely those in the thin channel (Figures 4-11 (a)-(b), 4-12, and 4-13).

Fresh (stressed) devices on thick channels with a roughness of 4.2 nm had a worse ***S***, 117 (157) mV/dec, than the ***S***, 93 (97) mV/dec, of devices on thin channels with a roughness of 3.7 nm. Given these values of ***S***, the value of N_T at ΔE~0 eV was calculated [4.34]-[4.36]. N_G, at ΔE~ -0.1 eV for all samples was under 3×10^{10} $cm^{-2}eV^{-1}$, using an n_{GT} of $2x10^{15}$ $cm^{-3}eV^{-1}$; this value is one order of magnitude lower than the N_T obtained from ***S***. Accordingly, on such an epi-like poly-Si, interface trap-state densities, N_{IS} [4.36], given by the formula $N_{IS}=N_T-N_G$ [4.37], at ΔE~0 eV, and related to channel roughness, almost completely determines the ***S*** of fabricated TFTs (See Figure 4-13). Furthermore, the quality of the interface reportedly affects the deep-states of grain traps [4.38], such that the changes in n_{GT} due to ***HCS*** at the deep energetic level were observed. Very small changes in ***S*** and N_{IS} at the mid-gap energetic level in thin channels due to ***HCS*** was consistent with V_{th} and n_{GT} as well as the averaged N_G at the deep energetic level.

No hysteresis was observed in the transfer characteristics (Figure 4-9). Therefore, hysteresis was ruled out as a major mechanism in μ_{FE} and V_{th} degradation. In ***HCS***, a high drain bias ensures that carriers attain sufficient energy from the field to be injected into the gate dielectrics and to generate defect sites at the interface [4.39]. Hence, introducing a very low drain bias in ***HCS***, namely gate-bias stressing [4.39], facilitates the observation of the role of channel defects on the stability of electrical parameters of stressed devices. Stressed at V_g= -20 V and V_d= 0V, substantially reduced changes in V_t and grain trap-state densities were observed in both channels (See Figures 4-11 (c), 4-12, and 4-13) and explained by the fact that highly crystalline CLC poly-Si has a few densities of tail-states to accommodate accumulated carriers, inhibiting markedly deep-state generation in channel layers by bias stressing [4.39][4.40]. Under gate-bias stressing (or ***HCS*** with no drain bias), in thicker channels with greater channel crystallinity, the carrier-trapping effect is weaker because grain defects are fewer and so the change in V_t is smaller and larger exponents are associated with the ΔV_{th}, as observed in currently used devices (Figures 4-11 (c) and 4-13) [4.11]. For an Al-SiO_2-bulk Si (metal-oxide-semiconductor (MOS)) structure, a gate-stress of -20 V merely shifts the flat-band voltage of 30 mV; the value was much lower than those measured in stressed TFTs on CLC poly-Si (Figures 4-11 (b)-(c) and 4-13). This result indicates that charge trapping in gate dielectrics barely affects ***HCS***-induced degradations in present devices.

A slightly roughened CLC polysilicon/SiO_2 either provides trap sites or establishes a

local electric field, enhancing hot-carrier injection [4.4][4.37]-[4.39]. Under ***HCS*** with high drain bias, charge trapping at interfaces generates extra states, in response to increased interface and grain deep-state densities (Figures 4-12 and 4-13). For thicker channels with greater channel crystallinity, the larger changes in electric parameters, deep-state densities of grain defects and interface trap-state densities at the mid-gap energetic level due to ***HCS***, are attributed to their poorer interface quality (Figures 4-12 and 4-13). The poorer channel interface in thick channels than in thin channels causes the charge trapping mechanism to affect the V_{th} degradation more for thicker channels, which result agrees with the smaller exponents that are associated with the ΔV_{th} of these thicker channels. In thin channels with surfaces with a roughness of 5.1 nm, associated with increased laser power, the power-law exponents in V_{th} degradation by ***HCS*** were reduced to 0.32 (Figure 4-11 (b)), which finding is consistent with interface quality-dominated degradation.

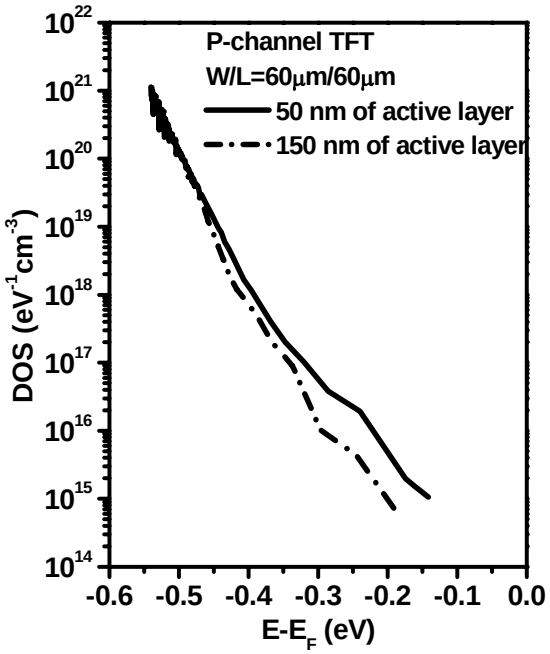


Figure 4-8 Energy distribution associated with grain trap-state densities in fresh TFTs made on CLC poly-Si with thicknesses of 50nm and 150nm.

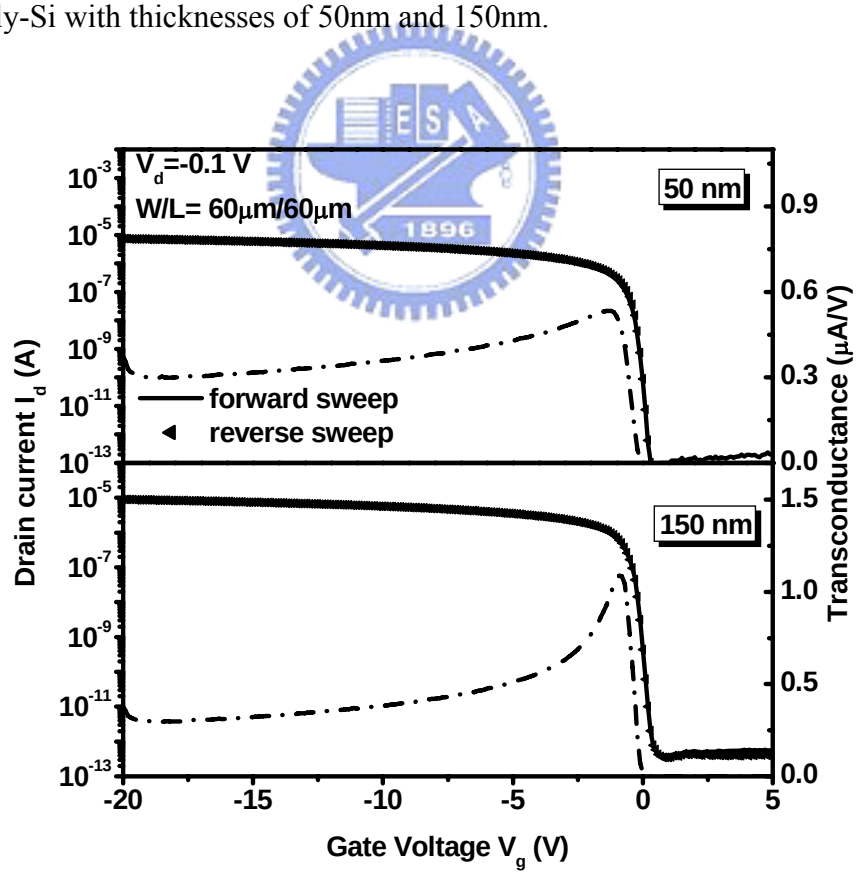


Figure 4-9 Transient transfer characteristics and transconductance curves of fresh TFTs made on CLC poly-Si with thicknesses of (a): 50nm and (b): 150nm. I_d-V_g hysteresis curves of fresh devices are also shown.

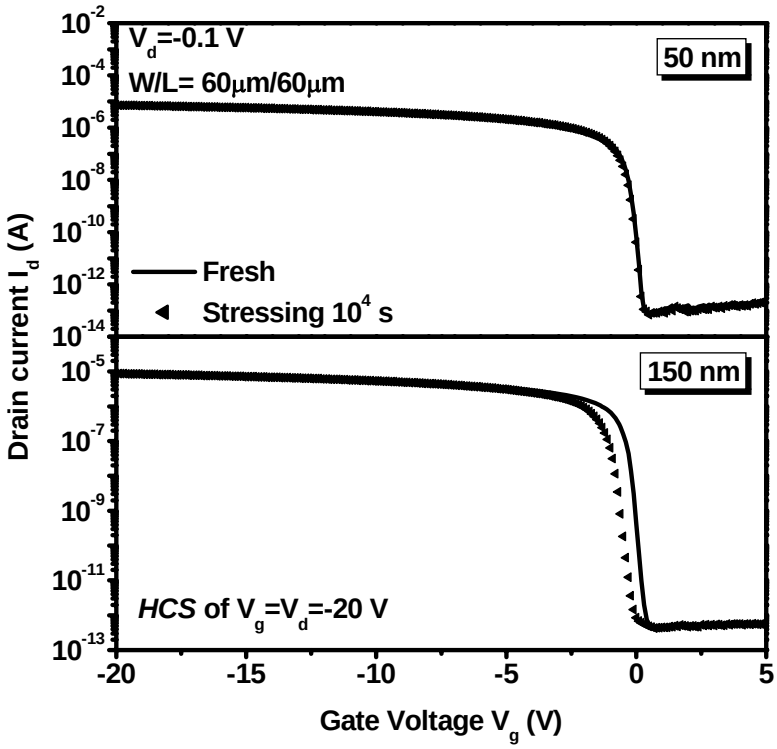


Figure 4-10 Transient transfer characteristics curves of stressed TFTs made on CLC poly-Si with thicknesses of (a): 50nm and (b): 150nm.

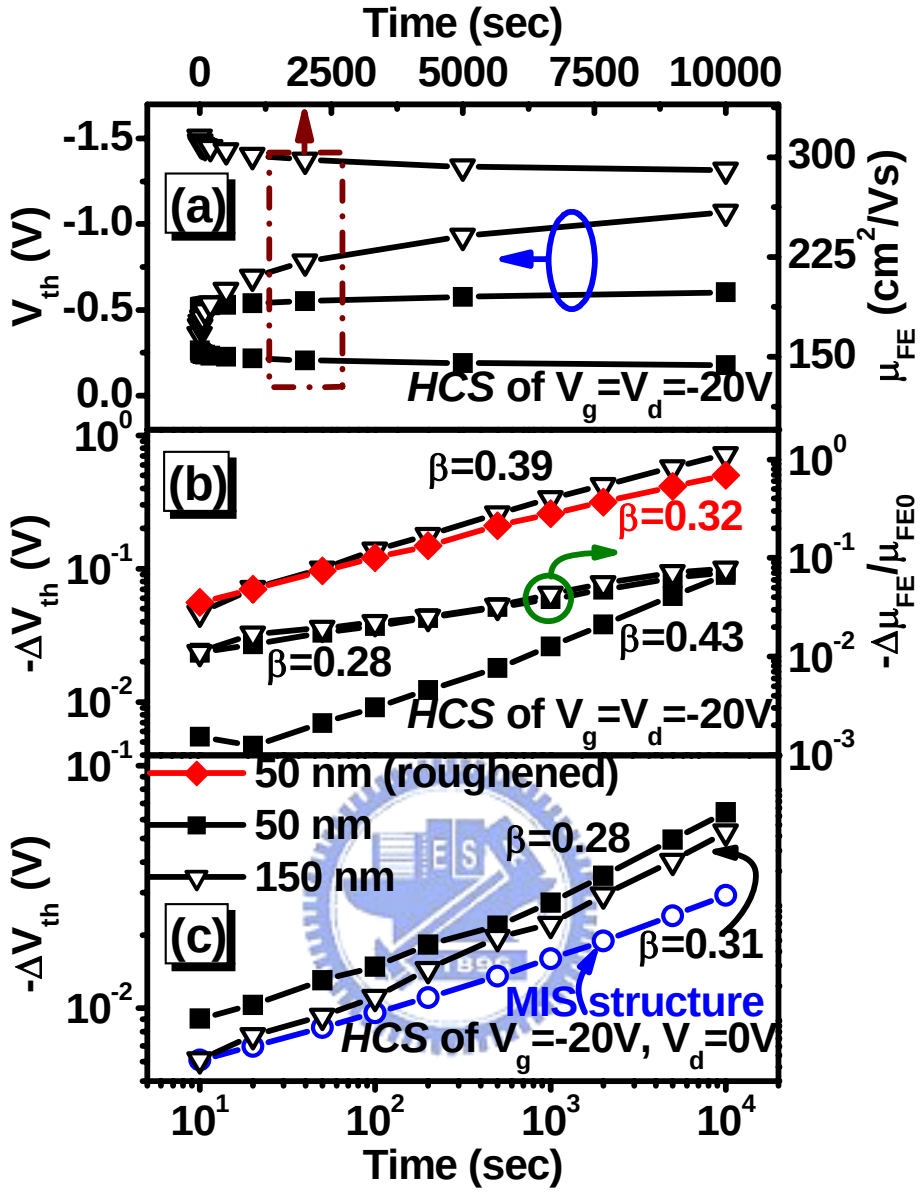


Figure 4-11 (a): Transients of field-effect mobility and threshold voltage of TFTs made on CLC poly-Si with thicknesses of 50nm and 150nm during ***HCS*** with V_g=V_d= -20 V. Degradation of V_{th} and μ_{FE} of TFTs made on CLC poly-Si with thicknesses of 50nm and 150nm during ***HCS*** with (b): V_g=V_d= -20 V, and (c): V_g= -20 V and V_d= 0 V. Degradation of flat-band voltage of a metal-SiO_2-bulk Si structure stressed at V_g= -20 V is also shown.

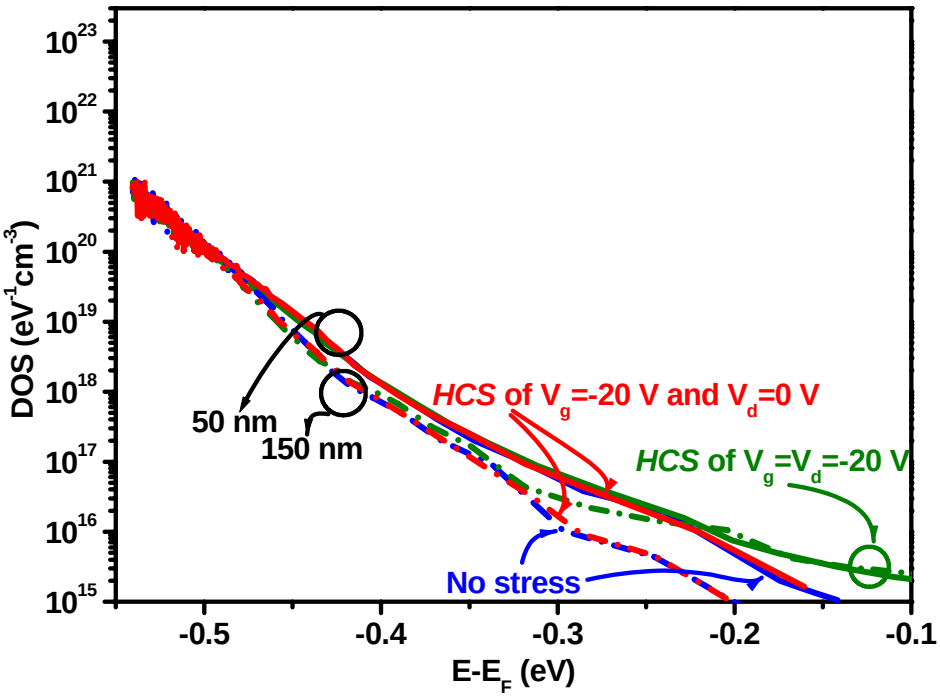


Figure 4-12 Energy distribution associated with grain trap-state densities in fresh, hot-carrier and gate-bias stressed TFTs made on CLC poly-Si with thicknesses of 50nm and 150nm.

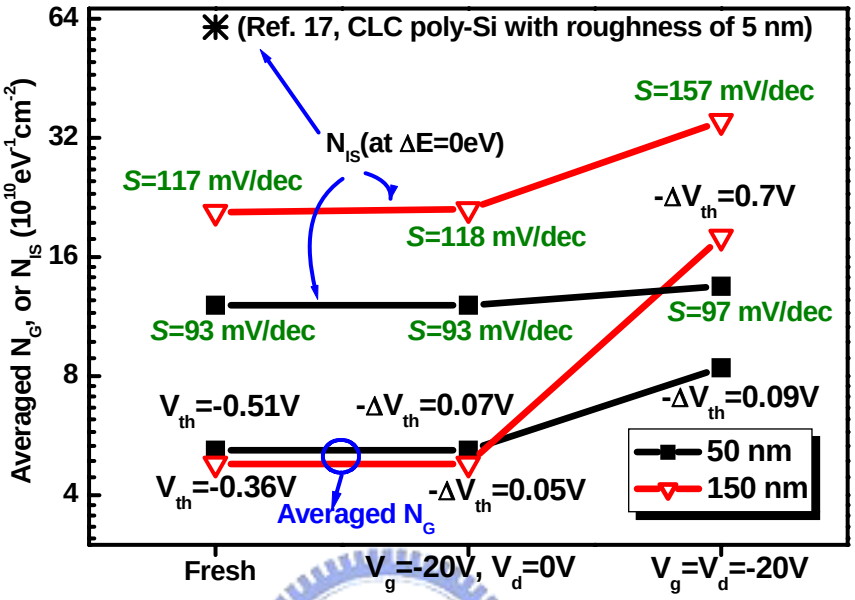


Figure 4-13 Threshold voltage, subthreshold slope, areal grain and interface trap-state densities at different energetic levels in fresh and stressed TFTs on CLC poly-Si with thicknesses of 50nm and 150nm.

4.6 Summary

In this chapter, the measurement of the trap-state densities of CLC polysilicon TFTs was reported to characterize the electrical parameters of devices with reference to channel crystal quality and surface morphology. Ultra-low trap-states densities associated with smooth and single-grain-like polysilicon are responsible for higher field-effect mobility, lower threshold voltage, steeper subthreshold slope and lower leakage current than those of ELA-fabricated TFTs. Moreover, low deep-state densities remain sensitive to the interfacial states, and are influenced by the LCESR effect.

In addition, channel roughness, rather than high crystalline channel layers, dominated the stability of high hole-mobility thin-film transistors on epi-like silicon channels formed by CLC. On such single-grainlike channels, an increase in channel roughness with channel thickness enhances charging trapping at the interfaces, generating substantially more new states at the deep energetic level. Hence, on thin channels with ultra-smooth surfaces, TFTs during ***HCS*** exhibited negligibly changed electrical parameters and generated fewer new-states than those on thick channels.

Chapter 5

Electrical characteristics and reliability of panel epi-like silicon transistors using CW green laser-activation

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5.1 Introduction

Temperature constrains the activation of source/drain junctions in several transistors, including panel transistors [5.1] and integrated-circuit transistors with novel channels and gate-dielectrics [5.2][5.3] or shallow junctions [5.4]-[5.6]. Accordingly, thermal annealing technologies must continue to advance. Dopant activation by ultraviolet (UV) [5.5], green [5.6] and near-infrared laser-irradiation [5.7] of source/drain regions has been demonstrated in transistor fabrication. However, laser-activation, unlike laser-crystallization, produces discontinuities in microstructures across junctions because of variations in the laser energy that is scanned over the device bodies, which are caused by gate structures [5.8]. With reference to panel applications, thin-film transistors (TFTs) on quartz wafers are reportedly activated by backside excimer-laser-irradiation and exhibit improved electrical characteristics [5.9].

CW green laser crystallization has attracted substantial interest because they are useful in the formation of epi-like microstructures and the maintenance of crystallized channels with low surface roughness, providing remarkably excellent device reliability and electrical characteristics [5.10][5.11]. Moreover, the fact that the absorption fraction of light energy in

transparent substrates decreases substantially as the laser wavelength increase, supports the introduction of backside long-wavelength (green) CW laser-activation (CLA) in mainstream glass panel displays, reducing laser-energy loss and negligibly damaging the interfaces near the substrates.

In addition, enlarged parasitic source/drain resistance due to shrinkage of the channel layer were usually reduced by the introduction of tungsten-clad [5.12] or SiGe-raised source/drain [5.13] structures or using advanced activation techniques. However, glass substrates, which do not support a fabrication temperature of over 600 ^{0}C, strictly constrain the temperature of activation of source/drain contacts in panel transistors. Laser-irradiation of source/drain regions was conducted using a low-temperature dopant activation procedure and has been demonstrated in transistor fabrication [5.14]. However, laser-activation, unlike laser-crystallization, produces discontinuities [5.8] and/or residual damage [5.15] in microstructures across junctions, because of variations in the laser energy that is scanned over the device bodies, which are formed from the gate structures.

In CLC, fast laterally scanned green laser-energy irradiates each area in under a millisecond, essentially enabling the activation of spike annealing. Furthermore, the fact that the absorption fraction of light energy in irradiated poly-Si layers declines substantially as the laser wavelength increases [5.16], supports the assertion that significant residual long-wavelength (green) laser-energy penetrates [5.17] through poly-Si gates of self-aligned transistors to channels, enhancing the uniformity of laser-energy across junctions, which is

barely influenced by the gate structures.

By introducing backside green laser-activation and spike CW green laser-activation (**CLA**) in panel transistors, this chapter demonstrates the enhanced field-effect mobility and fair reliability of such laser-activated TFTs.

5.2 Experiment on backside CW green laser activation

The samples and device fabrication are the same in the chapter 3 and chapter 4. Behind doped source and drain regions with B_2H_6 ($5.0x10^{14}cm^{-2}$ and 40 keV), the samples are activated by rapid thermal annealing (RTA) or backside CW green laser-irradiation at 2.1-2.8 W (shown in Figure 5-1). Cross-sectional transmission electron microscopic image is also used to observe the damage of the channel/drain junction. The sheet resistance of laser-(RTA) activated bare doped CLC layers was also evaluated using a four-point probe. And density of states of RTA and laser activated CLC poly-Si TFTs is extracted by FEC method that has been described in chapter 3.

5.3 Material and electrical characteristics with backside CW green laser activation

As laser-activation energy increases, the sheet resistance of the laser-activated layers slowly declines to 1-3 kΩ/sq, in the same range of that measured in RTP-activated layers (Figure 5-2). Laser-activation energy was almost half of the laser-crystallization energy.

Therefore, laser-activation hardly altered the crystallinity and roughness of the CLC epi-like Si channels. Accordingly, the surface roughness of activated layers, 3.8 nm, was almost identical to that, 3.7 nm, of un-doped CLC samples (Figure 5-3). Moreover, the tail-state density of grain traps measured in laser-activated devices, which was closely related to channel crystallinity [5.18], n_{GT} at an energetic level (E) that was far from the Fermi level (E_F), $\Delta E=E-E_F$= -0.55 to -0.47 eV, was independent of laser-activation energy and identical to that measured in RTA-activated devices (Figure 5-3) Moreover, this laser-activation energy was sufficiently high to repair amorphized source/drain regions due to implantation [5.4] and to re-crystallize a few small grains in the channels [5.19], as indicated by n_{GT} between the middle and the deep energetic levels (ΔE= -0.47 to -0.3 eV), which decreases markedly with laser-activation energy (Figure 5-3).

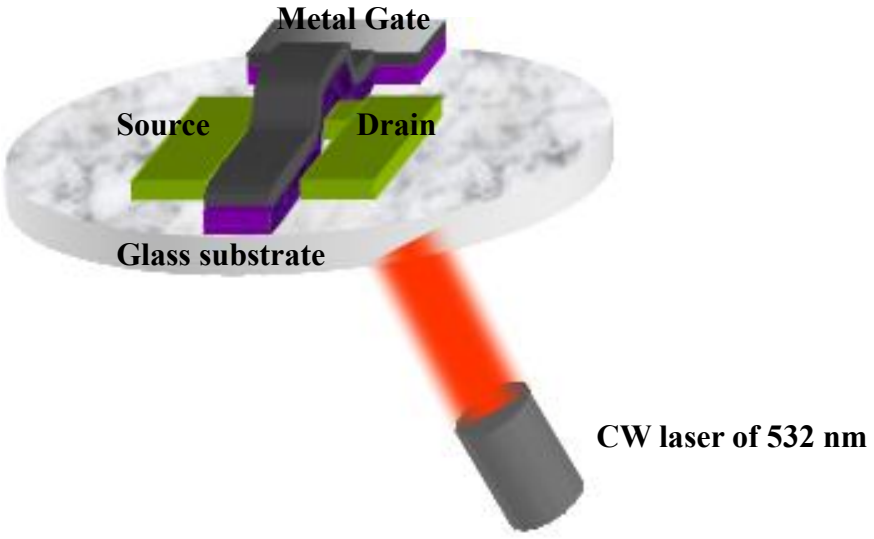

Figure 5-1 A diagram of backside CW green laser activated the CLC poly-Si TFTs

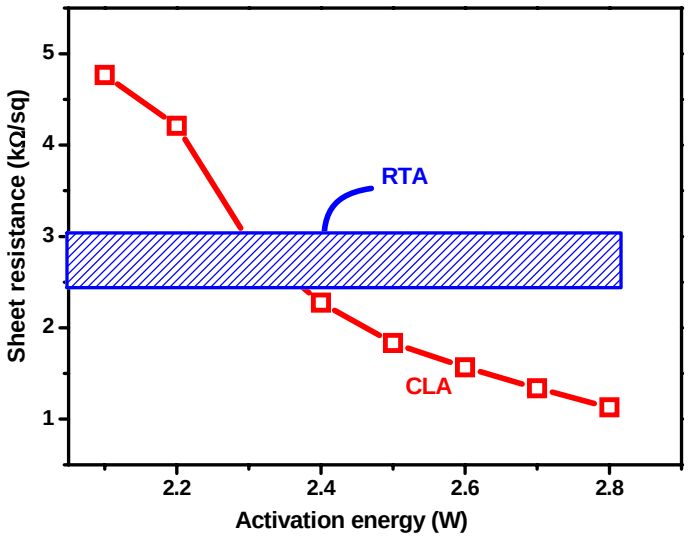

Figure 5-2 Sheet resistance of bare CLC layers that were doped with B_2H_6 and activated by RTA and back-side green laser-irradiation at 2.1-2.8 W.

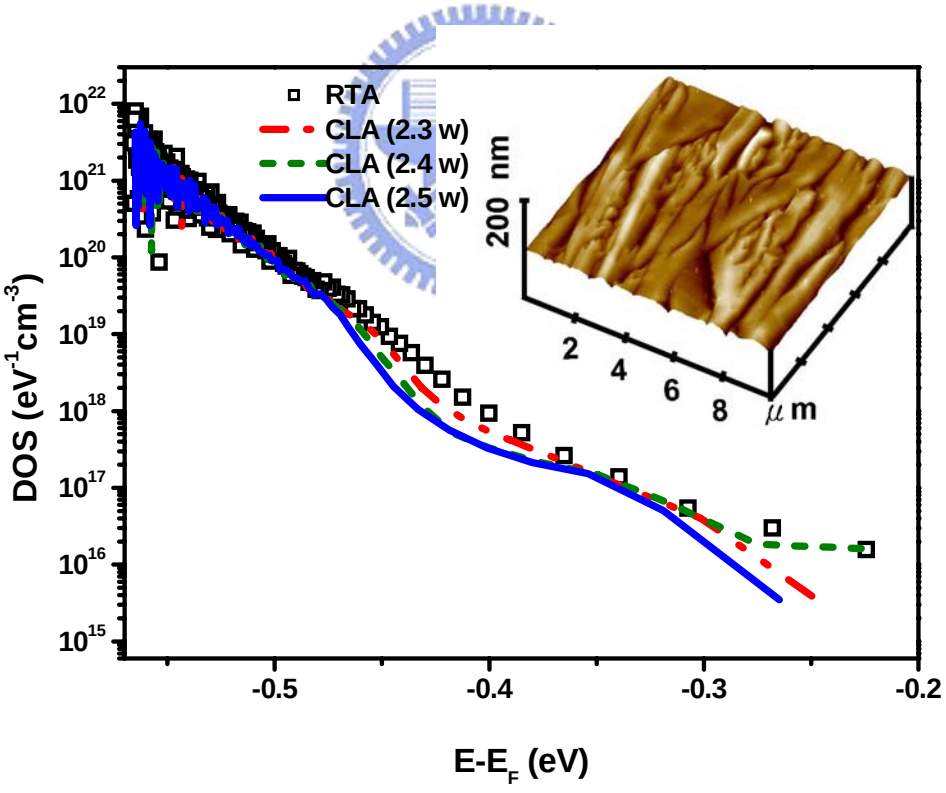

Figure 5-3 Surface roughness after backside laser activation at 2.5 W and energy distribution associated with grain trap-state densities in fresh TFTs that were made on CLC poly-Si and activated by RTA and back-side green laser irradiation at 2.3-2.5 W.

As laser-activation energy increases, the field-effect mobility (μ_{FE}) of laser-activated TFTs, increases significantly from 255 to 403 cm^2/Vs, which is around two times that of RTA-activated TFTs, as revealed by the linear transcondcutance (G_m) curves, which are plotted in Figure 5-4. The enhancement in the output drive current (Fig. 5-4 (b)) at V_d=-15 V and V_g=-15 V was as high as 1.4 times. However, similar changes in sheet resistance (1.5-3 kΩ/sq) by RTA parameters was responsible for no changes in hole-mobility and, therefore, temperature-dependent I_d-V_g curves (or n_{GT}) taken in such long-channel TFTs fabricated on CLC or Excimer-laser-annealed channels such that the reduction of contact resistance was ruled out as a major mechanism in hole-mobility enhancement.

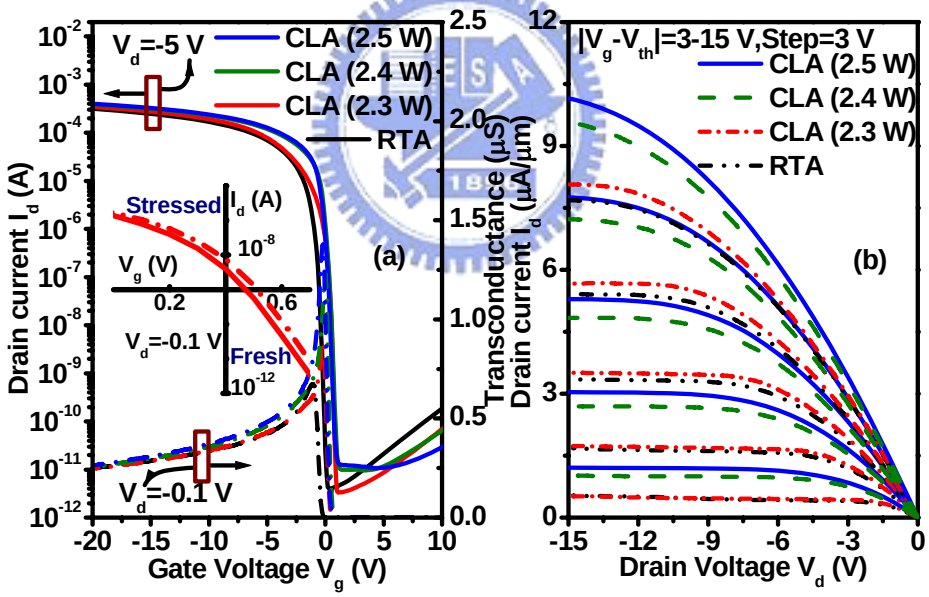

Figure 5-4 (a): Transfer characteristics (taken at V_d=-5 V) and transconductance curves (taken at V_d=-0.1 V); (b): output characteristics of TFTs that were made on CLC poly-Si and activated by RTA and back-side green laser-irradiation at 2.3-2.5 W. I_d-V_g curves (taken at V_d=-0.1 V) of fresh and stressed devices that were activated by back-side green laser-irradiation at 2.3 W are also plotted in (a).

Under back-side green laser-irradiation, the gate structures did not influence the distribution of laser-energy. Therefore, laser energy was uniformly scanned laterally from channels to source/grain regions and vice versa. Super visible-laser lateral-activation consequentially produces continuous epi-like Si microstructures with a reduced number of grain defects across junctions, as indicated by the cross-sectional transmission electron microscopic image in Figure 5-5, in response to the enhancement.

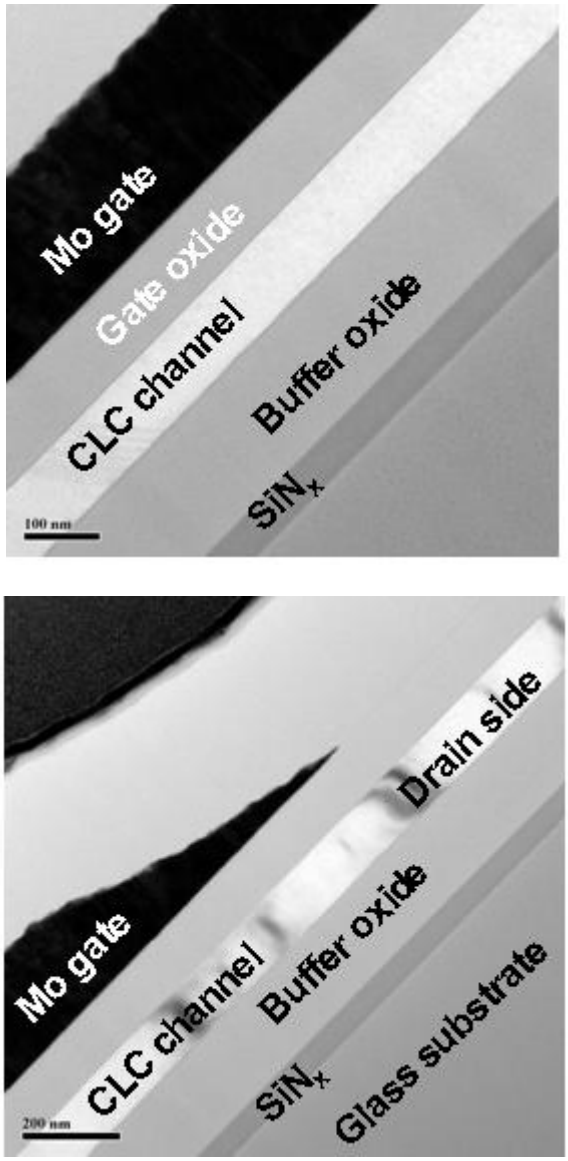

Figure 5-5 Cross-sectional transmission electron microscopic image of representative laser-activated TFT.

On such an epi-like poly-Si, interface trap-state densities (at ΔE~0 eV), which are related to channel roughness, influence the subthreshold slope (***S***) of fabricated TFTs [5.11]. The formation of extra interface defects is associated with the enhancement of surface roughness by laser activation, such that increasing the laser-activation energy initially reduced ***S*** to as low as 91 mV/dec, and then slightly increased it to 122 mV/dec (Figure 4-8), which value is better than 128 mV/dec for RTA-activated devices. The reversal in threshold voltage (V_{th}) due to the small increase in the number of interface defects [5.10][5.11], to an extent related to laser-activation energy was also observed (Figure 5-6). Furthermore, the quality of the interface affects the deep states of the grain traps, such that n_{GT} at a ΔE of above -0.28 eV for devices that were activated at a middle laser-activation energy of 2.4 W exceeded that for devices that were activated at a low laser-activation energy of 2.3 W (Figure 5-5) [5.11]. However, the greatly improved channel/junction microstructures, formed by relatively high laser-activation energy of 2.5 W, were responsible for the fact that the deep states of the grain traps were as low as $8.0\text{x}10^{15}\text{ev}^{-1}\text{cm}^{-3}$ (at ΔE~-0.26 eV).

Improvements in epi-like Si channel/junction microstructures caused by backside laser-activation reduces local electric fields near drain regions, originating in the discontinuity in the microstructures across junctions, were responsible for the decrease in the leakage current in the laser-activated TFTs (Figure 5-4(a)) [5.8].

5.4 HCS on backside CW green laser activation

Figure 5-6 (a)-(b) plots the transients of $\mathbf{V_{th}}$, ***S*** and the degradation of the V_{th} shift ($\Delta\mathbf{V_{th}}$)

for devices in Figure 5-4 during ***HCS***, against laser-activation energy and stress time (t). After ***HCS***, very small changes in ***S*** (ΔS) and V_{th} of 1 mV/dec and 50 mV, respectively, were observed in TFTs that were activated at a low laser energy of 2.3 W, which corresponded to the lowest value (91 mV/dec) of ***S*** among all laser-activated devices and a μ_{FE} of 255 cm^2/Vs (Figure 5-6 (a)). The worsening of electrical parameters for stressed TFTs activated at a high laser energy of 2.5 W, which corresponded to an ***S*** of 122 mV/dec and an extremely high μ_{FE} of 403 cm^2/Vs, was deteriorated to 17 mV/dec and -284 mV, respectively. However, these values are better than the 32 mV/dec and -425 mV in RTA-activated TFTs, which exhibited a μ_{FE} of 195 cm^2/Vs and an ***S*** of 128 mV/dec.

After ~3 h of ***HCS***, a positive rather than a negative shift in V_{th} for the laser-activated device with the lowest ***S*** was observed. (See the inset of Fig. 5-4 (a) and Fig. 5-6 (a). This result is attributed to hot-electron trapping near drain junction [5.20]. The creation of donor-type interface deep-states was excluded as a possible mechanism of positive V_{th} shift [5.20] because the changes in ***S*** (or interface defects) were negligible during ***HCS*** (Fig. 5-6 (a)). The V_{th} degradation for laser-activated devices due to ***HCS*** typically follow a power-law in time ($\sim t^{\beta}$) with exponents (**β**) of less than 0.4, as opposed to β=0.4-0.6 associated with deep-state generation (Figure 5-6 (b)) [5.11]. Moreover, ***HCS*** hardly changed the tail-state densities of grain traps in highly crystalline laser- (RTA) treated junctions/channels [5.11], which is consistent with β and reduction percentage of less than 0.3 and 8%, respectively, in μ_{FE} degradation for both junctions/channels (shown in Figure 5-7).

Enhanced reliability was irrelevant to relatively small variation in reliability of devices distributed over panels associated with fair uniformity of electrical parameters of μ_{FE}, V_{th}, and S of 12%, 0.1V, and 20%, respectively, and was barely ascribed to the formation of the lightly doped drain (LDD) structure in such long-channel TFTs by laser-induced lateral-diffusion of dopants.

Therefore, the formation of continuous improved epi-like Si microstructures with reduced grain defects and with a barely increased number of interface defects over the entire channel/junction inhibited markedly deep-state generation in laser-treated channels/junctions by bias stressing, in response to the enhancement of the stability of such laser-activated TFTs.

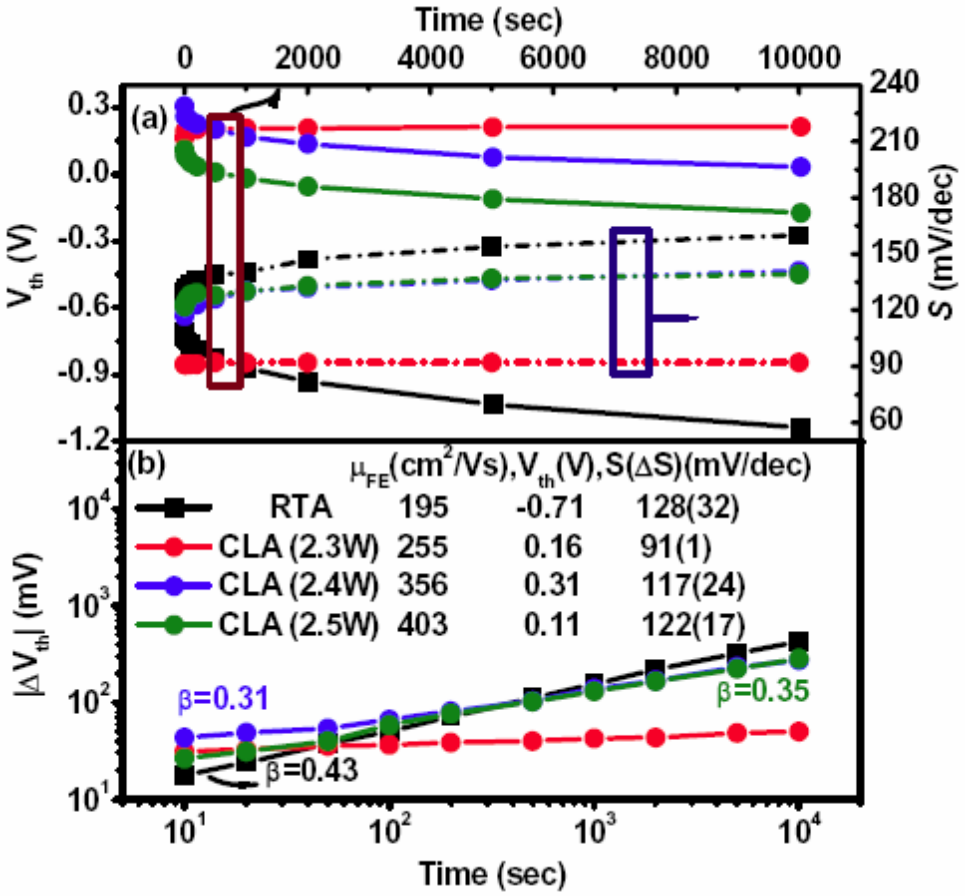

Figure 5-6 (a): Transients of threshold voltage and subthreshold slope, and (b): degradation of V_{th} of TFTs that were made on CLC poly-Si and activated by RTA and back-side green laser-irradiation at 2.3-2.5 W during ***HCS***. Electrical parameters for all fresh TFTs are also summarized.

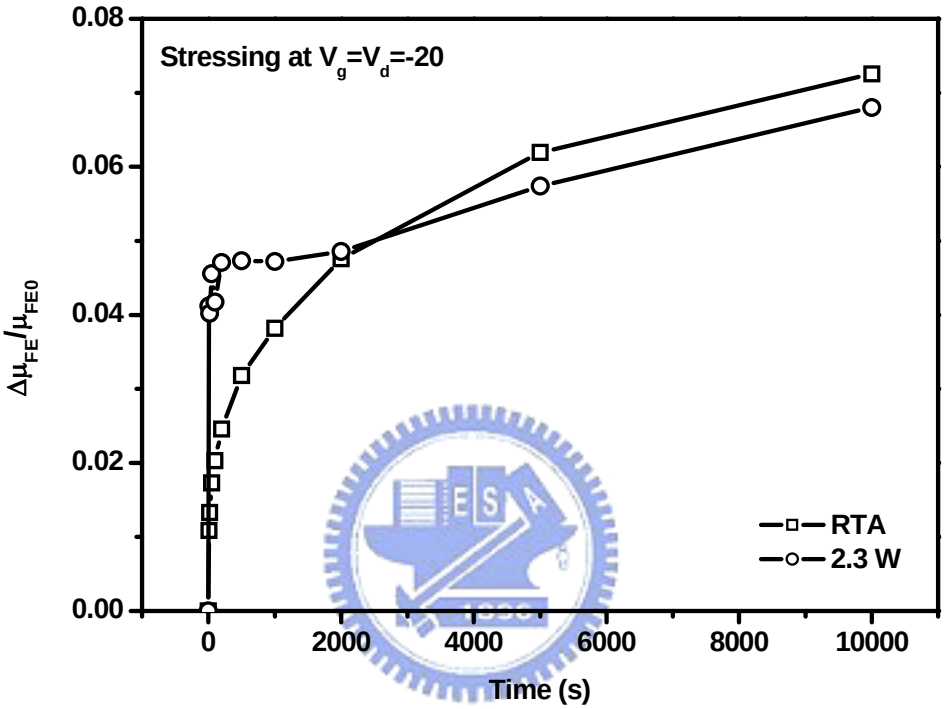

Figure 5-7 Degradation of μ_{FE} of TFTs that were made on CLC poly-Si and activated by RTA and back-side green laser-irradiation at 2.3 W during ***HCS***.

5.5 Spike green laser-activation

5.5.1 Experimental procedure

CW green laser crystallization and TFT fabrication are portrayal of chapter 3 and chapter 4. Poly-Si gates and source/drain regions were doped with PH_3 ($5.0x10^{14}cm^{-2}$ and 25 keV) and activated by rapid thermal annealing (RTA) for 90 s at 600 ^{0}C or CW green laser-irradiation at 2.1-2.8 W (shown Figure 5-8). The parasitic source/drain resistance of laser- (RTA) activated TFTs was determined from the relation between channel-width (***W***=10 μm) normalized ON resistance ($\mathbf{R_{ON}}$) and the length of the channel (***L***=5-15μm) that introduces in the section 3.3.

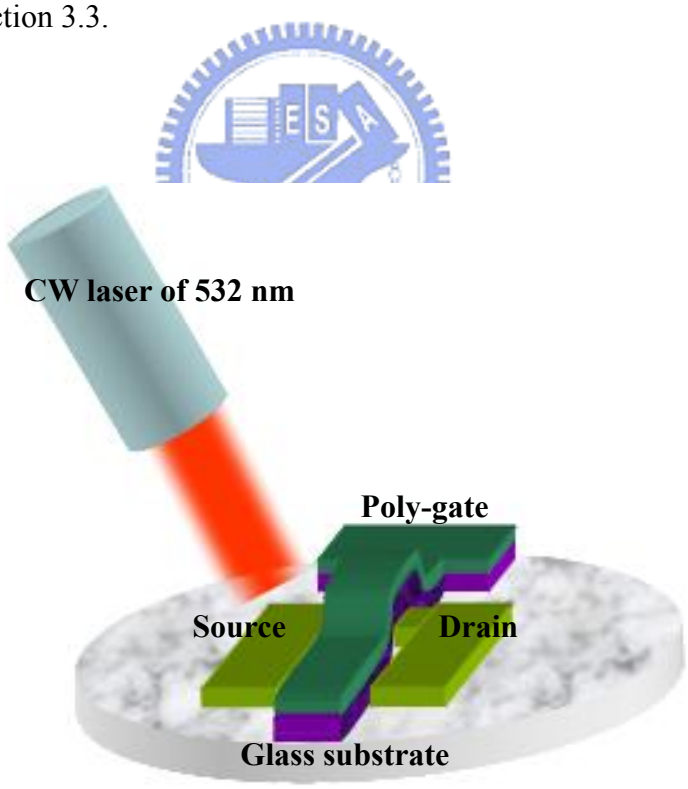

Figure 5-8 A diagram of spike CW green laser activated the CLC poly-Si TFTs

5.5.2 Electrical characteristics and DOS for spike CW green laser activated the CLC poly-Si TFTs

As laser-activation energy increases, the sheet resistance of the laser-activated layers slowly decreases to 0.3-0.5 kΩ/sq, which is in the range that was measured in RTP-activated layers. The laser-activation energy was almost half of the laser-crystallization energy; however, it sufficed to repair source/drain regions that were amorphized by implantation [5.4]. Parasitic source/drain resistance, which was obtained from merging numerous curves of $\mathbf{R_{ON}}$ ($\boldsymbol{V_g}$) against $\boldsymbol{L}$, for devices that were activated at a middle laser-activation energy of 2.5 W, which corresponded to a field-effect mobility (μ_{FE}) of 200-250 cm^2/Vs and depending on $\boldsymbol{L}$, $\boldsymbol{L}$=5-15μm (Figures 5-9 and 5-10 (a)), was as low as 5 kΩ (Figure 5-12 (a)), but slightly larger than 3 kΩ (Figure 5-12 (b)) for RTP-activated devices that corresponded to an μ_{FE} of 150-200 cm^2/Vs associated with $\boldsymbol{L}$ (Figures 4-11 and 4-12-a). Those values are much lower than 13.5 kΩ for conventional TFTs [5.12] because the devices herein were fabricated on fairly crystalline CLC layers rather than on excimer-laser-annealing (ELA)-crystallized or solid-phase-crystallized layers. Fewer grain defects in smaller channels result in better electrical characteristics of TFTs, which fact explains the dependence of μ_{FE} on $\boldsymbol{L}$ [5.21] in laser (RTA)-activated devices (Figure 5-10 (a)). Gate structures generally influence the distribution of laser-energy [5.15] under laser irradiation. However, the fact that the fraction of light energy absorbed in irradiated poly-Si layers significantly falls as the laser wavelength increases [5.16] ensures that significant green laser energy penetrates through the poly-Si

gates to the channels.

Green laser-energy was thus uniformly scanned laterally from the channels to the source/grain regions and vice versa in a sub-millisecond duration, and was hardly influenced by gate structures. Almost 40% of incident green laser energy penetrates through the poly-Si gates with a thickness of 200 nm [5.16], because the depth of penetration of green light in poly-Si is very long, re-crystallizing a few small grains in the channels, as indicated by the $\boldsymbol{n_{GT}}$ of laser-activated devices ($\boldsymbol{L}$=10μm), between the tail and the middle energetic levels (E) that were far from the Fermi level (E_F), such that $\Delta E=E-E_F$= 0.5 to 0.4 eV (Figure 5-11). This $\boldsymbol{n_{GT}}$ value decreases slightly as the laser-activation energy increases and is lower than that of RTP-activated devices ($\boldsymbol{L}$=10μm) (Figure 5-11). Moreover, grain tail-state densities at ΔE= 0.55 to 0.5 eV, which were strongly related to channel crystallinity [5.8][5.19], were also improved by a laser-activation energy of as low as 2.1-2.8 W, because of CLC channels that were crystallized by low green laser-energy at 3.7 W, comprised fairly crystalline microstructures, rather than epi-like microstructures, with many grain defects.

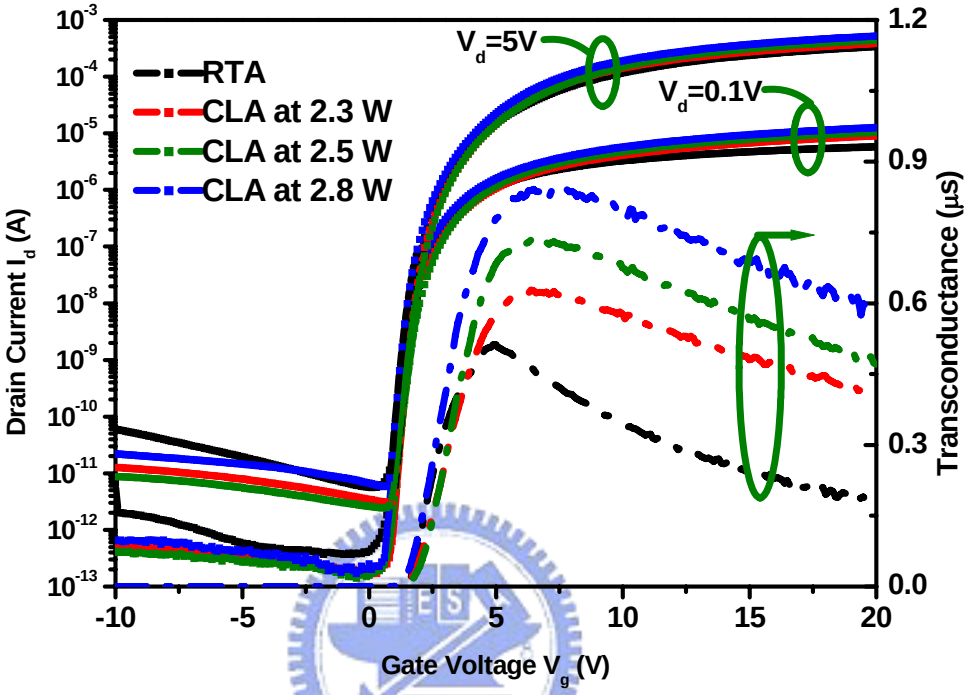

Figure 5-9 Transfer characteristics (at V_d=5 V and at V_d=0.1 V) and transconductance curves (at V_d=-0.1 V) of TFTs that were made on CLC poly-Si and activated by RTA and spike green continuous-wave laser-irradiation at 2.3-2.8 W, with channel dimensions of W = L= 10 μm.

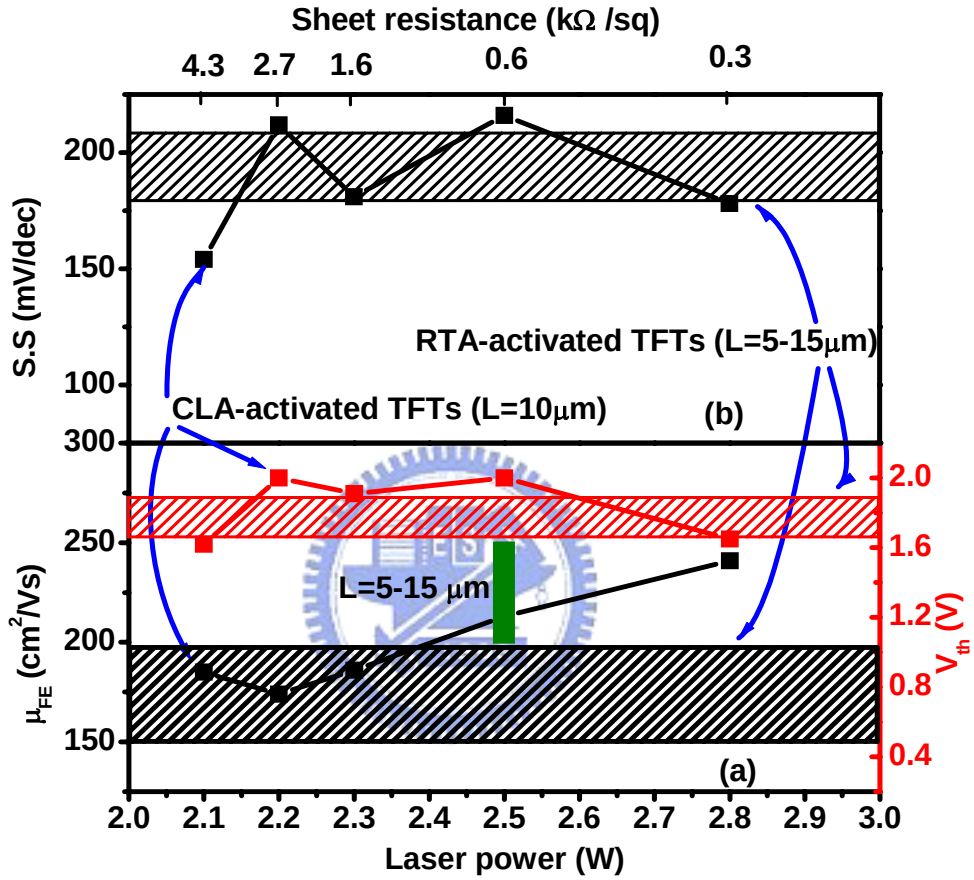

Figure 5-10 (a): Field-effect mobility and threshold voltage, and (b): subthreshold slope for TFTs that were made on CLC poly-Si and activated by RTA and spike green continuous-wave laser-irradiation at 2.1-2.8 W, with channel dimensions of W= 10 μm and L=5-15 μm.

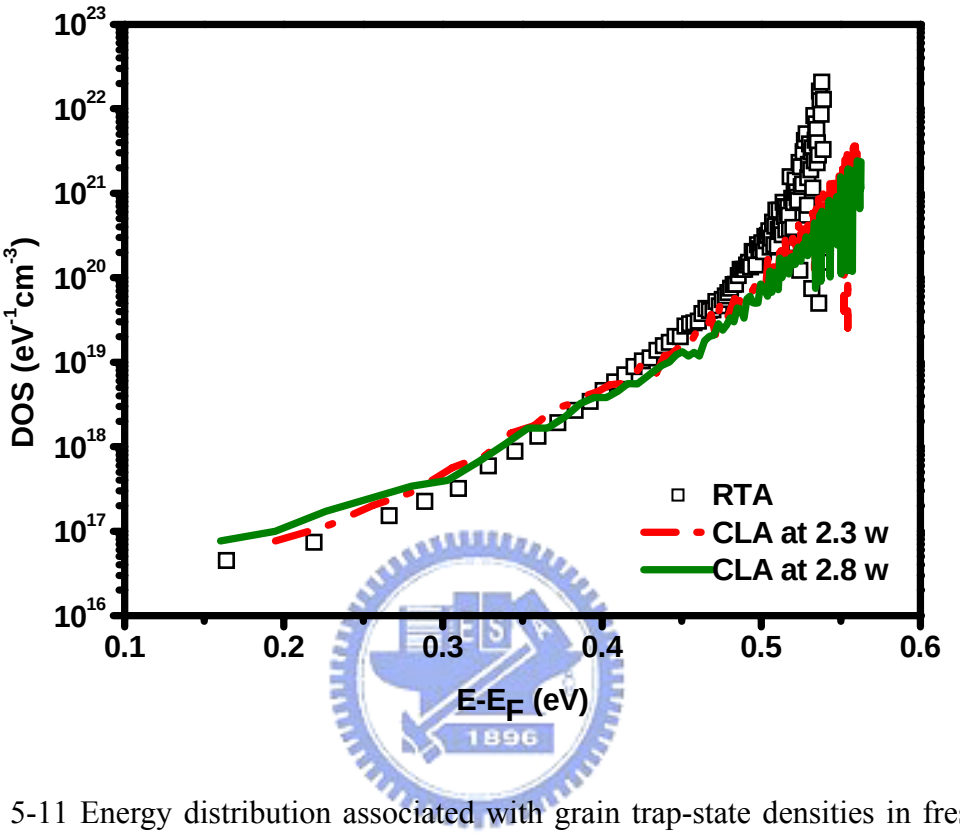

Figure 5-11 Energy distribution associated with grain trap-state densities in fresh TFTs that were made on CLC poly-Si and activated by RTA and spike green continuous-wave laser-irradiation at 2.3-2.8 W, with channel dimensions of W = L= 10 μm.

5.5.3 Parasitic resistance effect and hot-carrier stressing

Spike green-laser annealing produces low parasitic source/drain resistance and quasi-continuous improved poly-Si microstructures with fewer grain defects over the entire channel/junction, in response to an enhancement in μ_{FE} that depends on the laser-activation energy (Figures 5-9 and 5-10 (a)). In long-channel TFTs that are fabricated on poly-Si

layers, such a small parasitic source/drain resistance hardly influences the μ_{FE} of transistors [5.23], such that the μ_{FE} of laser-activated TFTs (L=10μm) increases to 245 cm^2/Vs as laser-activation energy increases to 2.8 W (Figures 5-9 and 5-10 (a)). This value exceeds 155 cm^2/Vs for RTA-activated TFTs (L=10μm) (Figures 5-9 and 5-10 (a)), even though RTA-activated devices have a lower parasitic resistance (Figure 5-12).

Spike CW green laser-activation was conducted under irradiation with low laser-energy, in an attempt to generate quasi-continuous poly-Si microstructures with lower grain tail-state densities and barely increased grain (interface) deep-state densities over the entire channel/junction (Figure 4-11), as compared to n_{GT} of RTA-treated devices, though low laser-activation energy results in slightly high R_{ON}. Hence, the threshold voltage (V_t) and the subthreshold slope (S), which were deteriorated by the increase in the grain/interface deep-state densities and enhancement of the local field near the drain, caused by the negligible discontinuity in the microstructures across junctions of TFTs [5.8] (L=10μm) that were activated at laser-activation energies of 2.1-2.8 W, are 1.6-2.0 V and 150-220 mV/dec, respectively (Figure 5-10). These values are comparable to those of RTA-activated devices (L=10μm) (Figure 5-10). Quasi-continuous improved poly-Si channel/junction microstructures have weaker local electric fields near the drain regions of laser-activated TFTs (L=10μm) given leakage currents as low as 20 pA at V_g=-10 V and at V_d=5 V, which are lower than the 70 pA currents of RTP-activated devices (L=10μm) (Figure 5-9). After ~3 h of ***HCS***, the shifts in the V_{th} (ΔV_{th}) and S ($\Delta S/S$) of laser-activated devices (L=10μm) are

0.53 V (0.41), less than the 0.71 V (0.42) of RTA-activated devices (***L***=10μm) (Figure 5-13), since the formation of improved poly-Si microstructures with fewer grain defects and barely increased interface defects throughout the channel/junction (Figure 5-11) markedly inhibited deep-state generation in laser-treated channels/junctions under bias stressing. Further increasing the laser-activation energy increases the channel/junction roughness and does not allow the formation of quasi-continuous microstructures across the junction, worsening off-state electrical characteristics and reliability.

CLC under middle laser power, like ELA under SLG, limits grain size to cause fairly electron-mobility. Figure 5-14 and figure 5-15 show electrical characteristics and density of states for epi-like microstructures with front-side CW green laser irradiation, electron-mobility and sub-threshold slope for such transistors that were fabricated on CLC channels of 100 nm, were remarkable values of 530 $cm^2/V.s$ and 120 mV/dec, related to extra-low tail-state and deep-state density, respectively.

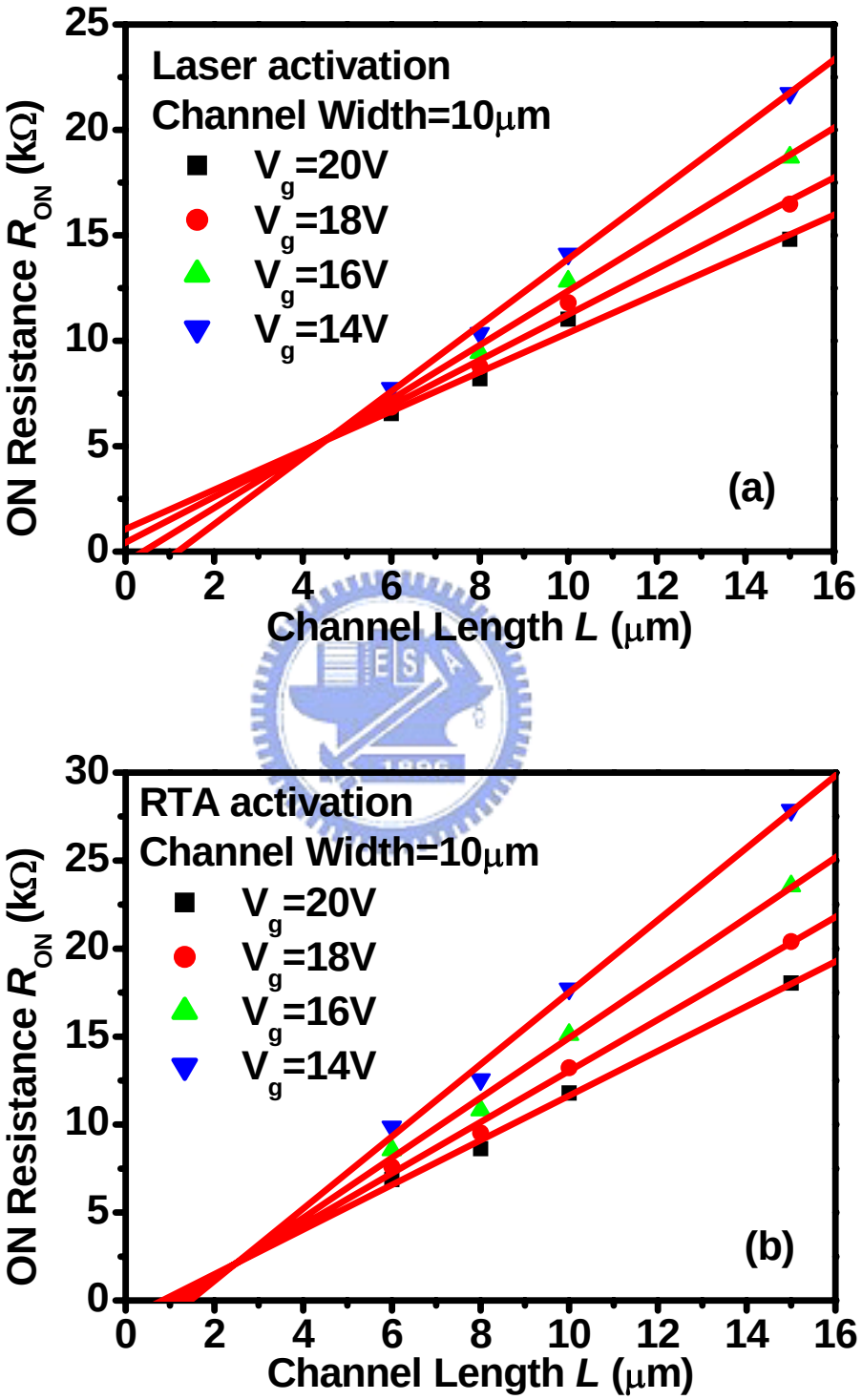

Figure 5-12 Channel width-normalized ON resistance of (a): laser-activated and (b): RTA-activated TFTs versus channel length.

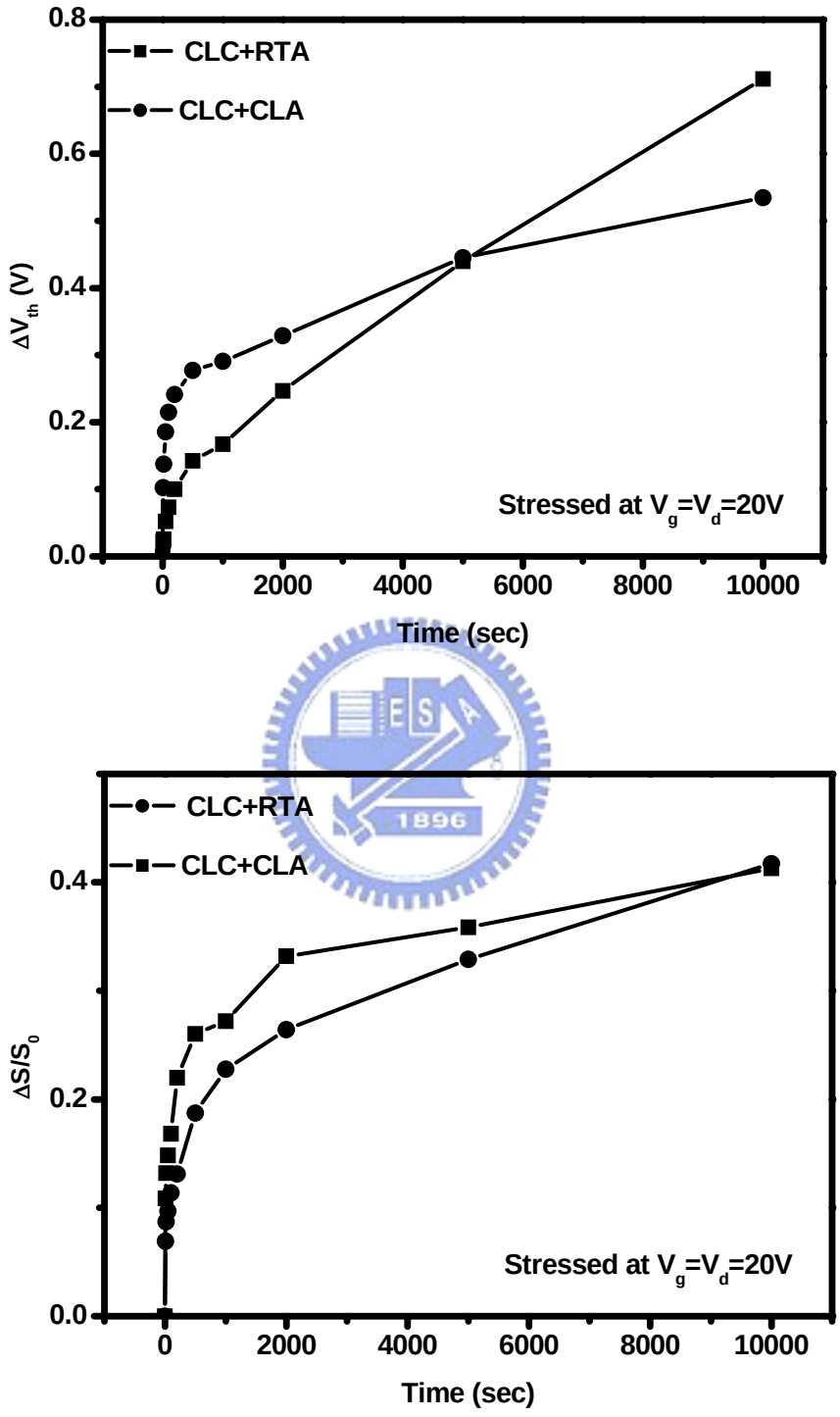

Figure 5-13 The shifts in the V_{th} (ΔV_{th}) and S ($\Delta S/S$) of laser-activated and RTA-activated devices.

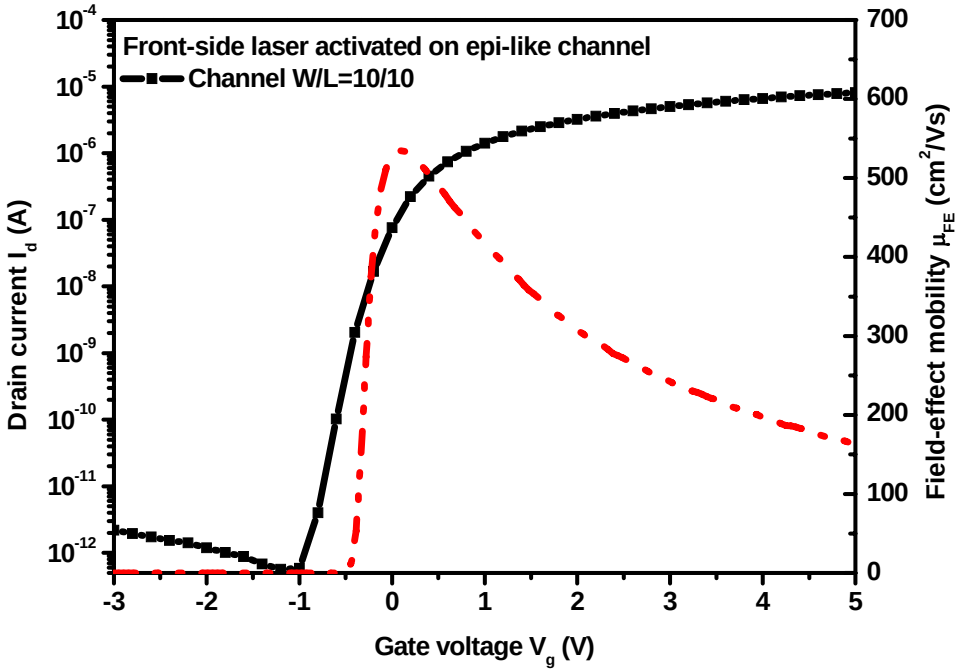

Figure 5-14 Transient transfer characteristics curves of front-side CW green laser activated epi-like poly-Si TFTs with thicknesses 100nm.

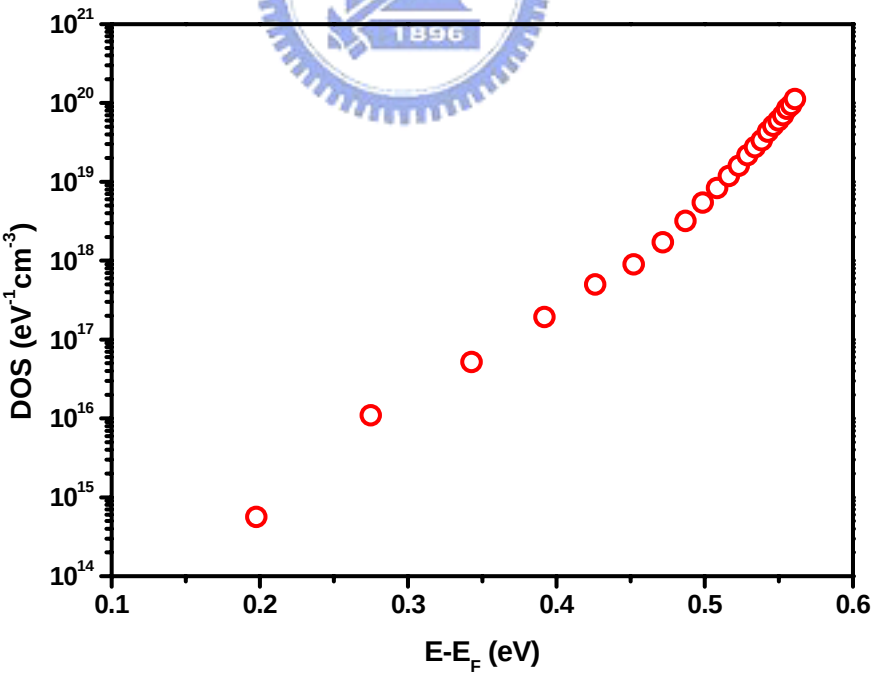

Figure 5-15 Energy distribution associated with grain trap-state densities in front-side CW green laser activated epi-like poly-Si TFTs with thicknesses of 100nm.

5.6 Summary

In this chapter, Backside continuous-wave green laser-irradiation was applied to activate TFTs that were fabricated on CLC epi-like poly-Si. Enhancement in the hole-mobility and reliability of such laser-fabricated transistors was demonstrated, and was explained by the formation of continuous enhanced epi-like Si microstructures with a barely increased number of interface defects over channels/junctions as a result of the lateral activation by uniformly scanned laser energy over the bottom of devices, in the absence of interference by gate structures.

In addition, Spike CW green laser-irradiation was applied also to activate TFTs that were fabricated on CLC poly-Si. The electrical parameters, leakage currents and stability of such laser-activated transistors was superior to those of thermally activated TFTs, because of the formation of quasi-continuous improved microstructures over channels/junctions as a result of the lateral activation by considerably uniformly scanned laser energy that was caused by the penetration of significant green laser energy into the channels, over the top of self-aligned poly-Si TFTs.

Chapter 6

Conclusions and future prospects

6.1 Conclusions

In this dissertation, high performance low temperature epi-like CW laser lateral crystallization polycrystalline silicon thin film transistors have been fabricated because of the lateral grain growth. Continuous-wave diode pumped solid-state laser is worthy of our anticipation since high field-effect carrier is ease of completion without extra layout, process and structure. The conventional CLC technology was provided by A. Hara and N. Sasaki in past year. However, the crystallization mechanism and defect density lacked for reporting in detail. In addition, a long-term reliability of CLC poly-Si TFTs has also been investigated. Finally, novel approach with CW green laser activation from front-side and back-side irradiation is also manifested and studied.

In the Chapter 2, the traditional CLC poly-Si films are achieved in this study. According to the material structure analysis, it has clearly been found that the difference of crystalline in one line laser beam due to the laser beam energy has a Gaussian distribution. From the Scanning electron microscopy (SEM) and atomic force microscopy (AFM) analysis were demonstrated that the lateral grain is very large about 1×3μm as a dependence of silicon film thickness and surface roughness is lower than 5 nm. Micro-Raman Scattering Spectra and X-ray diffraction are identified the quality and orientation of CLC poly-Si films. The

results are shown better optical-phonon mode and small low-frequency shift in comparison with ELA. This means the high quality and low defects in the lateral grain of CLC poly-Si films. The X-ray diffraction shows (111) and (200) orientation in the CLC poly-Si films. In the Chapter 3, the CLC poly-Si TFTs were successfully fabricated in this thesis. The electrical characteristics have been observed that applied laser power has a great effect on the performance of CLC poly-Si TFTs. With increasing the laser power, field-effect mobility and threshold voltage are enhanced because of the better crystallization condition. However, the subthreshold swing slope is degraded related to mid-gap state enhancement in surface states behind a threshold laser power. This point is discussed in detail in the Chapter 4.

Density of states distribution (DOS) for appraising the trap density was extracted by field effect conductance method (FEC). The trap state density transformed effectively from I_d-V_g measurement with various temperature. The surface band-bending was related defect states as a function of gate voltage. Hence the electrical parameters like field-effect mobility, threshold voltage, and subthreshold swing slope can be distributed into the different band state. In addition, ON resistance are related by quality of poly-Si thin films and activation degree. The detail is discussed into Chapter 4 and Chapter 5.

In the Chapter 4, the in-grain defects and strain-bonds related to field-effect mobility were terminated by increasing laser power as the poly-Si films had larger grain size and better film quality. In addition, the dangling-bonds at grain boundary and interface between poly-Si film and gate dielectric associated with threshold voltage and subthreshold swing

slope property. The extra low trap density with proposed CLC poly-Si TFTs was demonstrated by using DOS method in this thesis. However, the formation of extra interface defects caused by laser-crystallization-enhanced surface roughness was detected reversal in deep-state density.

The effect of the thickness of silicon layer is discussed in the chapter 4. Thicker silicon layer can obtain the larger grain size due to smaller subboundary spacing. The higher quality poly-Si films exist in the thicker silicon film and go along with slight large surface roughness. The mechanism of hot-carrier effect is very different in the thin and thick silicon films. The charge trapping in the power-law model is a dominant factor in the thicker silicon film. Because of the rough surface at poly-Si/oxide interface, more interface states and the local field can be enhanced to lead to carrier easy of trap. However, thin silicon film has few interface states build a defect creation relationship after hot-carrier stressing. In addition, the DOS is clearly also shown before and after hot-carrier stressing to confirm state creation in the deep-state.

In the chapter 5, a novel approach with CW green laser activation is adopted to successively fabricate high performance CLC poly-Si TFTs in this study. The wavelength of 532 nm can large amount of incident green laser energy passes through the glass substrate (in chapter 2). Backside continuous-wave green laser-irradiation was applied to activate the proposed devices. Continuous irradiation improved epi-like Si microstructures over channels/junctions as a result of the lateral activation by uniformly scanned laser energy over

the bottom of devices, in the absence of interference by gate structures. The high field-effect mobility and reliability were also demonstrated in our proposed transistors.

Continuous-wave green laser is irradiated from front-side cross a poly-Si gate structure. Our experiment called it “Spike CW green laser-activation”since the laser has a million-second level cross over a device body. Almost 40% of incident green laser energy penetrates through the poly-Si gates with a thickness of 200 nm. The partial laser energy can improve the defects which include the stained-bond termination in the channel. The leakage current, threshold voltage and subthreshold swing slope are compatible with RTA activation. However, the field-effect mobility is increased with enhancing incident green laser energy to obtain the quasi-continuous improved microstructures in the channel. In our study, electron-mobility and sub-threshold slope for such transistors that were fabricated on CLC epi-like channels of 100 nm, were demonstrated remarkable values of 530 $cm^2/V.s$ and 120 mV/dec, respectively.

6.2 Future prospects

6.2.1 Metal gate application for novel devices

To fabricate transistors, ohmic contacts were normally formed by thermal annealing of highly doped semiconductors at extremely high temperature of 1000 ^0C. Characteristics in nanostructured, and functionalized gate dielectrics, however, normally persist to temperature, i.e., 550 ^0C, much lower than activation temperature. Alternative fabrication procedures

should be proposed. Laser-induced activation is a reliable and low-temperature process as demonstrated in Si or polycrystalline silicon transistors. A metal gate, such as TiN and TaN, was formed on the gate dielectrics in transistors to reflect laser-irradiation such that photo-induced damage in nanostructured, and functionalized gate dielectrics was prevented. In TiN/SiO_2 (shown in Fig. 6-1) structures, laser-activated panel transistors that were fabricated on CLC channels of 100 nm, revealed electron-mobility as high as 230 $cm^2/V.s$.

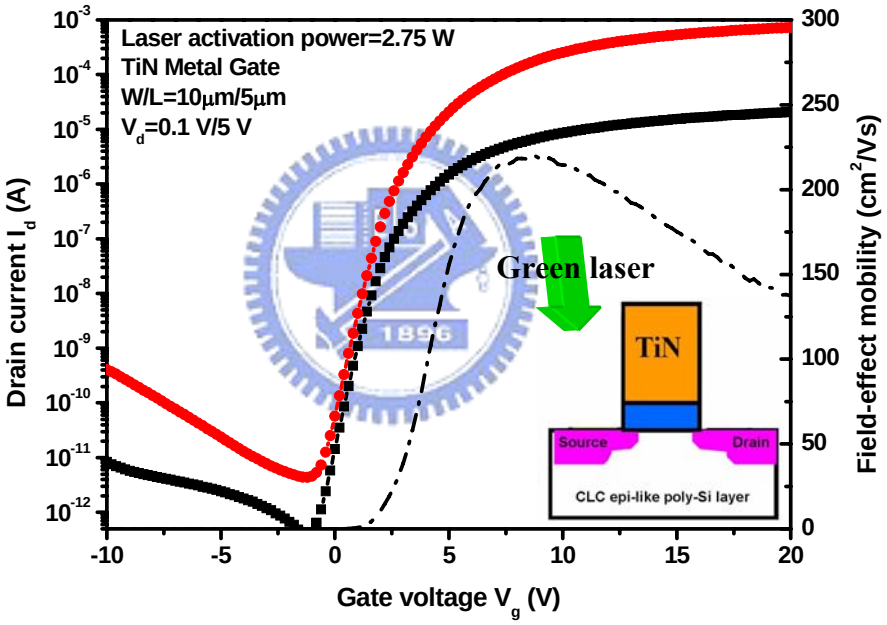

Figure 6-1 CW green laser-activated panel transistors with TiN metal gate.

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Chapter 1

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