國立交通大學

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博士論文

藉鎳捉聚改善鎳金屬誘發側向結晶之低溫複晶矽薄膜及奈米通道電晶體效能研究

Improved Performance of NILC LTPS Thin-Film & Nanowire Transistors through Ni-Gettering

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摘要

本論文主要研究鎳金屬誘發側向結晶(NILC)低溫複晶矽(LTPS)薄膜電晶體(TFTs)。其中，鎳金屬誘發複晶矽薄膜有鎳金屬殘留的問題，因此發展出有效的鎳金屬捉聚(Ni-gettering)方法來降低鎳金屬誘發複晶矽薄膜中的鎳金屬殘留，論文中所提出的鎳金屬捉聚結構為鎳金屬捉聚層/蝕刻停止層。鎳金屬捉聚層採用非晶矽薄膜及磷佈植非晶矽薄膜二種，厚度為 100 nm。蝕刻停止層為化學法製備之二氧化矽(Chemical oxide, chem-SiO_2)，厚度約 5 nm。論文最後應用此鎳金屬捉聚法於鎳金屬誘發側向結晶複晶矽薄膜電晶體及矽奈米線通道電晶體(Si NW channel transistors)製作上，以探討鎳金屬對元件特性的影響。

首先，利用非晶矽薄膜及化學法製備之二氧化矽作為鎳金屬捉聚基版，成功將複晶矽中殘餘鎳捕捉至鎳金屬捉聚基板中。由 SEM 分析可發現鎳金屬捉聚後聚集在兩相鄰鎳金屬誘發側向結晶晶界(NILC/NILC boundary)的 $NiSi_2$ 蝕刻孔洞明顯減少。此種捉聚方

式，是藉由濃度梯度的擴散使得複晶矽中殘餘鎳金屬能成功的透過蝕刻停止層捕捉至上層鎳金屬捉聚層，因此可發現上層非晶矽由於鎳金屬的擴散而成長出鎳金屬誘發側向結晶複晶矽。此方法與先前實驗室使用之非晶矽薄膜/電漿輔助化學沈積之氮化矽比較，可大大降低鎳金屬捉聚時間。其主要原因為鎳原子在氮化矽的擴散速度慢但通過化學氧化層卻速度快。

除此之外，為提高非晶矽薄膜之鎳金屬捉聚效率。進一步使用離子佈植法將磷雜質(Phosphorus dopant)佈植於非晶矽薄膜中，成功提高捉聚層之鎳金屬溶解度。由 SEM 分析可發現鎳金屬捉聚後聚集在兩相鄰鎳金屬誘發側向結晶晶界的 $NiSi_2$ 蝕刻孔洞幾乎不存在。磷離子佈植法雖可以提升鎳金屬捉聚效率，但其佈植濃度在 $1x10^{16}$ cm^{-2} 才有明顯效果。且由 SIMS 分析結果發現鎳在捉聚層的分佈與磷佈植曲線相當一致。

將鎳金屬捉聚法應用在鎳金屬誘發側向結晶複晶矽薄膜電晶體製備上，從元件特性得知，鎳金屬誘發側向結晶複晶矽薄膜電晶體在經過鎳捉聚處理後，可獲得較佳的電特性及均勻性，如降低漏電流(Leakage current)及抑制臨界電壓(Threshold voltage)負偏移等，其主要原因為鎳金屬誘發側向結晶複晶矽薄膜之鎳金屬殘留量可有效降低。

最後利用一個簡單及低成本的方法去製作矽奈米線通道電晶體。其製備之特點為利用一般製作 MOSFET 元件的側壁邊襯(Sidewall spacer)之概念，以底閘極薄膜電晶體結構在定義汲極和源極之同時，可自我對準形成奈米線通道。此複晶矽邊襯奈米線縱剖面近似三角形，其寬度及厚度可以控制至 70 nm。此奈米線通道薄膜電晶體比一般傳統薄膜

電晶體有比較好的通道控制能力。且經由鎳金屬捉聚處理後，鎳金屬誘發側向結晶複晶矽奈米線通道電晶體在電性與均勻性上獲得提升。主要原因為多晶矽邊襯奈米線通道內及其與氧化層之介面鎳金屬殘留量減少。

關鍵字：鎳捉聚、化學氧化層、磷雜質、鎳金屬誘發側向結晶、低溫複晶矽、奈米線、薄膜電晶體、矽奈米通道電晶體、側壁邊襯、漏電流

Improved Performance of NILC LTPS Thin-Film & Nanowire Transistors through Ni-Gettering

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Abstract

Low temperature polycrystalline silicon (LTPS) Ni-metal induced lateral crystallization (NILC) thin-film transistors (TFTs) have been investigated in this thesis. Ni impurities trapped inside the NILC poly-Si films is an issue. Therefore the Ni-gettering method is proposed to effectively reduce Ni residues within the NILC poly-Si films. It involves using gettering layers/etching stop layers as the Ni-gettering structure. The 100-nm-thick top α-Si and phosphorous-doped α-Si layers serve as the gettering layers, while the middle ~5-nm-thick chem-SiO_2 layer is used as an etching stop layer. Moreover the proposed gettering method is utilized in the fabrication of LTPS NILC TFTs and Si nanowire (NW) channel transistors to investigate the effect of Ni-metal inside poly-Si on the device performance.

First, the α-Si film is employed to getter Ni-silicides within NILC poly-Si film and Ni

reduction is demonstrated by SEM. After the gettering process, fewer and smaller silicide-etching holes are found at the NILC/NILC boundaries. It is found that top α-Si films, Ni-gettering layers, transfer into NILC poly-Si verified by SEM. This means that during the gettering process, Ni atoms diffused from the NILC poly-Si film through chem-SiO_2 into the Ni-gettering layer due to the concentration gradient. Compared with the previous α-Si/PECVD-SiN_x study, the thermal budget is greatly reduced. It's because of low Ni diffusivity in SiN_x films resulting a long annealing time as 90 h at 550^{o}C in N_2 ambient.

In order to improve the Ni-gettering efficiency, phosphorous-doped α-Si films are further used by ion implantation. After a gettering process, there are almost no silicide-etching holes observed at the NILC/NILC boundaries. These results indicate that phosphorous dopants could improve the gettering efficiency of α-Si due to the solubility enhancement of Ni impurities. But the gettering efficiency do not obviously improves until doping phosphorus ions reach a dose of 1×10^{16} cm^{-2}. The concentration distribution of Ni is similar to that of phosphorous atoms since the projection range of phosphorous ions is set at the middle of the α-Si film. This result also indicates that phosphorus could trap Ni atoms.

The proposed gettering method is further utilized in the fabrication of LTPS NILC TFTs. As NILC TFTs are treated with a Ni-gettering process, they reveal lower leakage current, higher on/off current ratio, higher mobility, and better uniformity. These improvements are

all attributed to the reduction of Ni impurities in gettered poly-Si films.

Finally, a simple method and low-cost process is used to manufacture the NW channels. The feature of process is the method of forming sidewall spacer of MOSFET. The poly-Si sidewall spacer NW channels self-alignment form in the process of defining source/drain (S/D). Both the vertical width (W_{NW}) and the horizontal sidewall thickness (T_{NW}) of poly-Si NWs are about 70 nm. The cross-section of fabricated poly-Si NWs is similar to triangular shape by an anisotropic etching. Compared with the traditional TFTs, the side-gated NWs TFTs have higher channel controllability. Moreover, the performance of NILC NWs TFTs is improved after a Ni-gettering process. This is because of the reduction of Ni and $NiSi_2$ precipitates randomly trapped at poly-Si/gate oxide interfaces and poly-Si grain boundaries.

Keywords: Ni-Gettering, Chemical Oxide (chem-SiO_2), Phosphorus Dopant, Nickel-Metal Induced Lateral Crystallization (NILC), Low Temperature Polycrystalline Silicon (LTPS), Nanowire (NW), Thin-Film Transistors (TFTs), Si Nanowire Channel Transistors, Sidewall Spacer, Leakage Current

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2010 年 2 月于新竹交大

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Chapter 1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays (AMLCDs) [1-3] and active-matrix organic light emitting displayers (AMOLEDs) [4-6] because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates. Since polycrystalline silicon (poly-Si) TFTs require glass substrates, intensive studies have been carried out to lower the crystallization temperature of amorphous silicon (α-Si) films. Ni-metal induced lateral crystallization (NILC) is one of these efforts. [7-12] Unfortunately, the NILC poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, which increase the leakage current and shift the threshold voltage. [12–16] Therefore, Ni contamination inside the NILC poly-Si film should be reduced. The goal of this work is to getter nickel impurities within NILC poly-Si to improve the performance of LTPS NILC TFTs.

In this chapter, an overview of poly-Si TFTs is first reviewed. Then the processes of low temperature poly-Si crystallization and the metal gettering from Si are introduced. Finally, the architectures of LTPS NILC nanowires (NWs) for improving the performance of TFTs are discussed, followed with the motivation of this work.

1.1 An Overview of Polycrystalline Silicon Thin-Film Transistors (TFTs)

The α-Si TFTs as the pixel switching device for active matrix liquid crystal displays (AMLCDs) is the mainstream technology due to low processing temperature (<350^{o}C) compatible with the glass substrate. [17, 18] However the poor field-effect mobility (typically < 1 cm^{2}/Vs) and the small on-current in α-Si TFTs limit themselves as the switching elements only. Therefore, the poly-Si becomes an attractive candidate for AMLCDs.

In 1980, the high temperature poly-Si TFTs with electron field-effect mobility around 50 cm^{2}/Vs were proposed. [19] This technique requires a high strain temperature substrate such as quartz, due to the gate insulator SiO_2 grown thermally at 1050^{o}C. Hence several techniques for poly-Si TFTs fabrication at low temperature (below 600°C) began in 1980s. The low-cost glass replaced quartz substrate and made high-definition AMLCD more practical and less expensive. In fact, the field effect mobility in poly-Si TFTs is significantly higher than that of α-Si about two orders of magnitudes. [20] The higher drive current allows small TFTs to be used as the pixel switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. [21]

Device structure of TFTs unlike MOSFETs, the active layer separately forms on the substrate, as shown in Fig 1-1. The quality of crystallized poly-Si films is therefore quite sensitive to the performance of poly-Si TFTs. The crystallized poly-Si fabricated by various

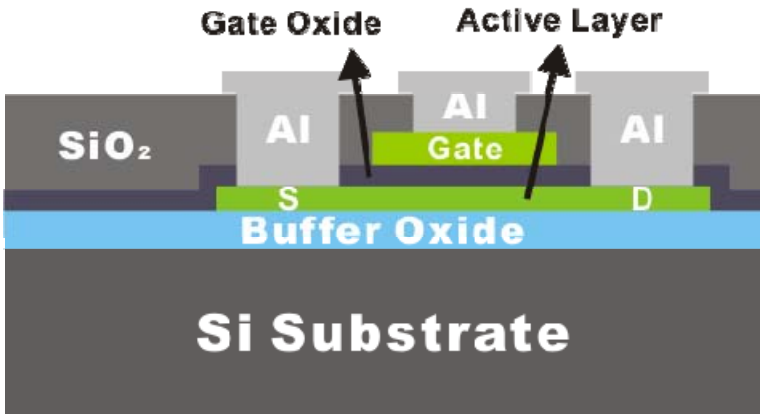


Figure 1-1 The device structure of a top-gated thin-film transistor (TFT).

techniques at low temperature such as: (1) solid phase crystallization (SPC), (2) Ni-metal induced lateral crystallization (NILC) will be reviewed in detail.

1.2 Low-Temperature Polycrystalline Silicon (LTPS) Crystallization

The most important step in the fabrication of LTPS TFTs has been considered as the crystallization of α-Si films. The quality of crystallized poly-Si films plays an important role on the performance of poly-Si TFTs. Historically, solid phase crystallization (SPC) [22] is the first technology to produce poly-Si films for display applications, followed by metal mediated induced crystallization. The ultimate goal of the LTPS technology is to integrate the pixel-driving circuits on the display substrate. These two low-temperature poly-Si crystallization methods are introduced as follows:

1.2.1 Solid-Phase Crystallization (SPC)

Amorphous Si (α-Si) is a thermodynamically meta-stable phase. It requires a sufficient energy to overcome the initial energy barrier for transformation to polycrystalline phase. The transformation is carried out by annealing in a furnace at certain temperature (typically at 600^{o}C) for duration time (about 24 h) to break and reorganize Si bonds. Since the solid state still stays during the phase transformation, the technique is called solid-phase crystallization (SPC). Deposited α-Si thin films transformed to poly-Si using SPC method have obtained better TFT device electrical performance than as-deposited poly-Si films. [23]

In general, the poly-Si crystallized from α-Si usually has larger grain size than that of as-deposited poly-Si. Most defects are generated at the grain boundaries in poly-Si films.

The phase transformation occurs through two processed, the nucleation and grain growth, and both have characteristic activation energies. [24] The nucleation activation energy is normally larger than the grain growth activation energy. [25] To enlarge poly-Si grains by SPC, it's necessary to suppress nucleation; therefore SPC is typically carried out at low temperature. Higher disorder structure requires higher energy barrier to form the Si nuclei. [26, 27] Hence SPC poly-Si grain size could be controlled by the selected α-Si deposition method and condition.

Moreover, many surface-nucleation techniques during SPC are proposed to improve the quality of poly-Si films by oxygen [28], silicon [29], argon [30] doping at α-Si/SiO_2 interface. After ion implantation, the heterogeneous nucleation at α-Si/SiO_2 interface is suppressed, and fewer homogeneous nucleation sites initiate on the top free surface of α-Si films. Therefore the larger SPC poly-Si grain size could be obtained.

1.2.2 Metal-Mediated Induced Crystallization

Several techniques based on the crystallization of the α-Si film were reported since 1964 as Wagner and Ellis [31] found that the presence of small amounts of a metallic phase could enhance the Si crystal growth. In general, two groups can be classified in the MIC/MILC

mechanism. One is to form eutectics with Si (Al [32], Au [33], and Sb [34]) and another is metastable silicide forming metals (Ni [35-38], Pd [39, 40] and Co [41]). For example, the Al/silicon eutectic temperature is 577^{o}C [42], but crystallization and type conversion of α-Si films in contact with Al occurs at temperatures as low as 200^{o}C.

Figure 1-2 shows the diamond structure of Si and the fluorite structure of $NiSi_2$. The lattice constant of Si and $NiSi_2$ is 5.430 Å and 5.406 Å, respectively, leading to very small lattice mismatch of 0.4 % with Si. The Ni-metal is considerably suitable for the formation of epitaxial Si and is therefore employed for the fabrication of NILC poly-Si films in this thesis. When a Ni film is deposited on a c-Si substrate and annealed, the Ni_2Si with $PdCl_2$ structure forms at ~200^{o}C and transforms into NiSi with the MnP structure at 350-750^{o}C. [43] These two phase-transformations are diffusion-controlled processes. Finally the NiSi transforms into the end phase $NiSi_2$ by a nucleation-controlled process at high transformation temperature in the range 450-750^{o}C. However, the NiSi transforming into the $NiSi_2$ is a diffusion-controlled process for the α-Si. Hence it's a low-temperature process as 350^{o}C for $NiSi_2$ precipitate formation, as shown in Fig. 1-3 [44]. Subsequently, the $NiSi_2$ crystallites serve as the nuclei for crystallization. The diffusivity of Ni [45] in α-Si is higher than that in c-Si. Thus the needle-like Si crystallite forms due to the diffusion of Ni in the α-Si network.

Figure 1-4 shows the equilibrium molar free-energy diagram [38] for $NiSi_2$ in contact

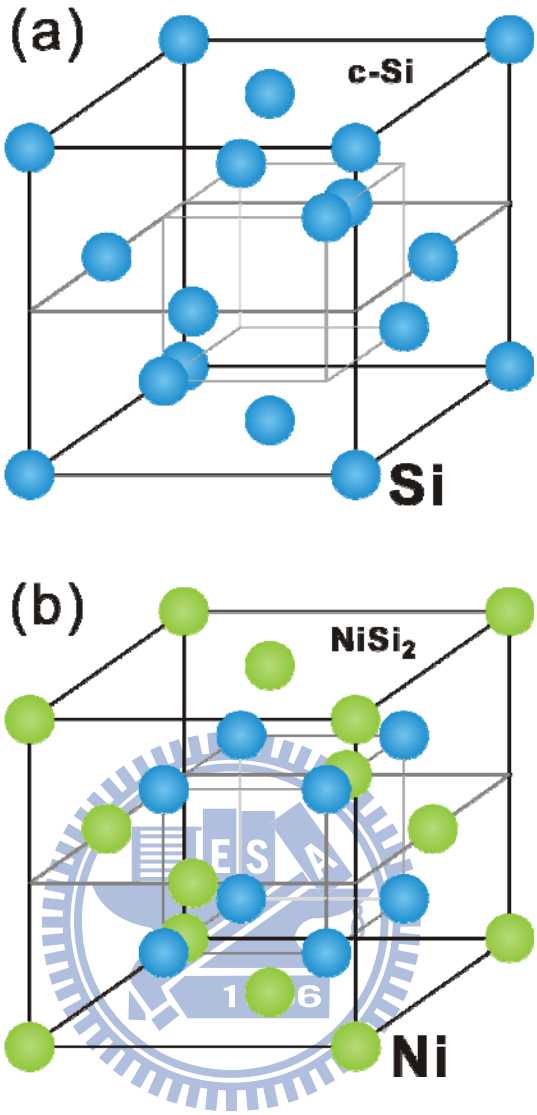


Figure 1-2 The crystalline structures: (a) the diamond structure of Si and (b) the fluorite structure $NiSi_2$.

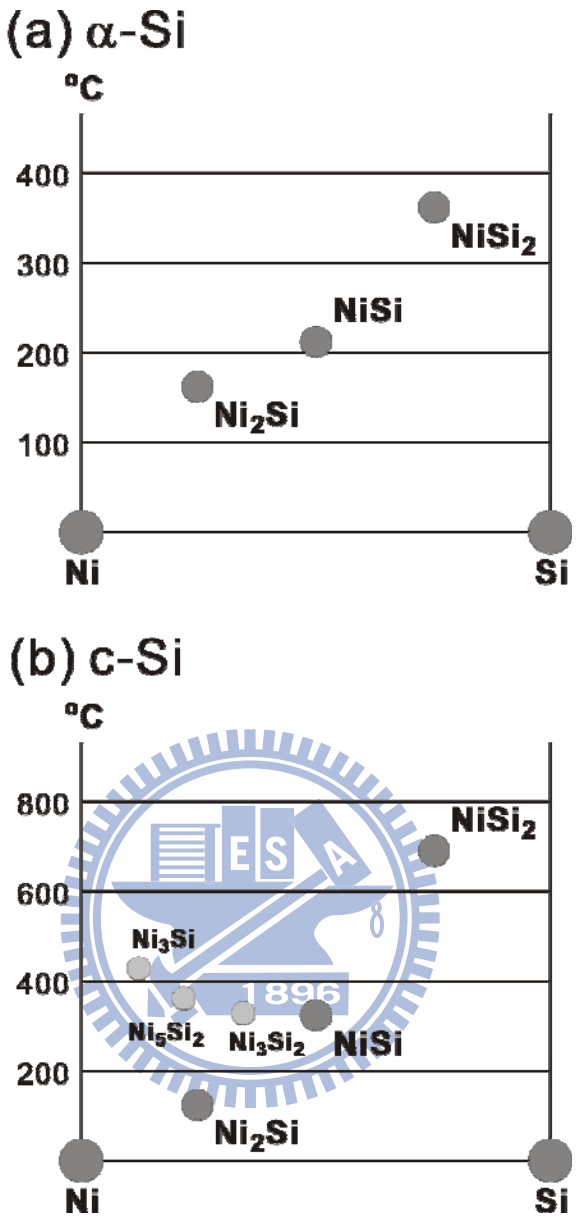


Figure 1-3 The formation temperature map of thin-film Ni silicides on (a) α-Si, and (b) c-Si [44].

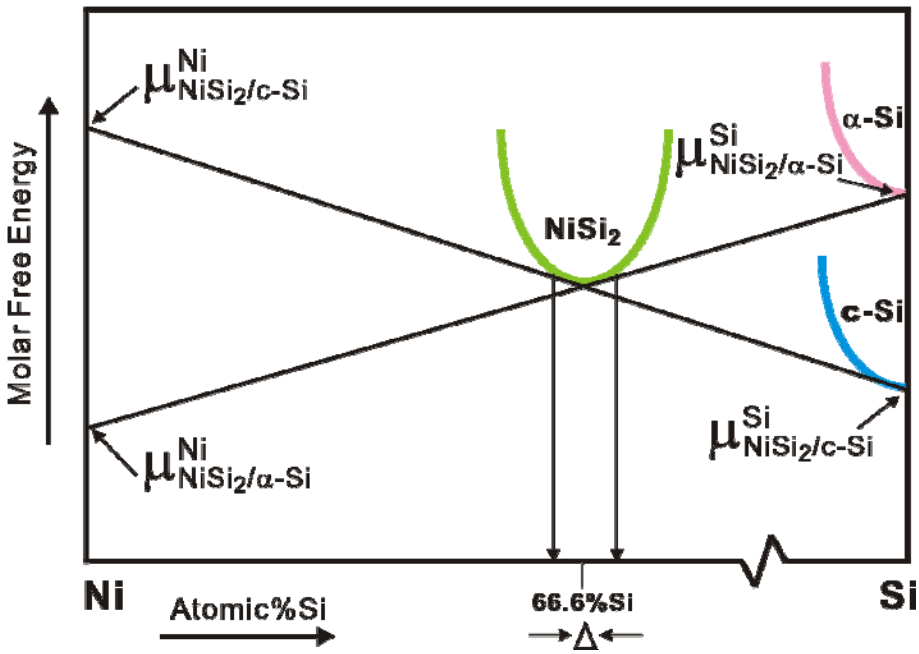


Figure 1-4 The equilibrium molar free-energy diagram for $NiSi_2$ in contact with α-Si and c-Si [38].

with α-Si and c-Si. Initially, several Ni-Si phases form in the silicide region and the $NiSi_2$ phase is found near the Si region [37]. The chemical potential of the Ni atoms is lower at the $NiSi_2$/α-Si interface and that of the Si atoms is lower at the $NiSi_2$/c-Si interface. Thus there is a driving force for Ni atoms diffusing through $NiSi_2$ to α-Si and for Si atoms diffusing reversely. This result indicates that the α-Si is consumed at the $NiSi_2$/α-Si during the migration of $NiSi_2$ crystallite. In 1993, C. Hayzelden and J. L. Batstone [38] found that a few layers of c-Si exist at the leading edge of the $NiSi_2$ precipitate. Therefore they propose a possible modification of the growth mechanism, as shown in Fig 1-5. The nucleation of c-Si on $NiSi_2$ initially occurs and Si atoms then diffuse through $NiSi_2$ to c-Si, as illustrated in Fig 1-5a. Next a c-Si nucleates at the leading edge of a migrating $NiSi_2$ precipitate. Ni atoms then diffuse through $NiSi_2$ to α-Si due to its ability to lower the chemical potential at the $NiSi_2$/α-Si, as shown in Fig 1-5b. A fresh c-Si forms at the $NiSi_2$/α-Si interface and the process repeats. Finally the needle-like Si crystallite is formed after the migration of $NiSi_2$ in a-Si network, as shown in Fig 1-5c

To enlarge poly-Si grain size, SPC is typically carried out at 600^{o}C to increase the incubation time and decrease the grain growth rate. Therefore a long annealing time is required for the SPC method. In the NIC/NILC method, a short annealing time and the low temperature (>600^{o}C) could be obtained, because of lower energy barrier of crystallization resulting from the reaction between Ni-metal and Si. However the undesirable Ni and $NiSi_2$

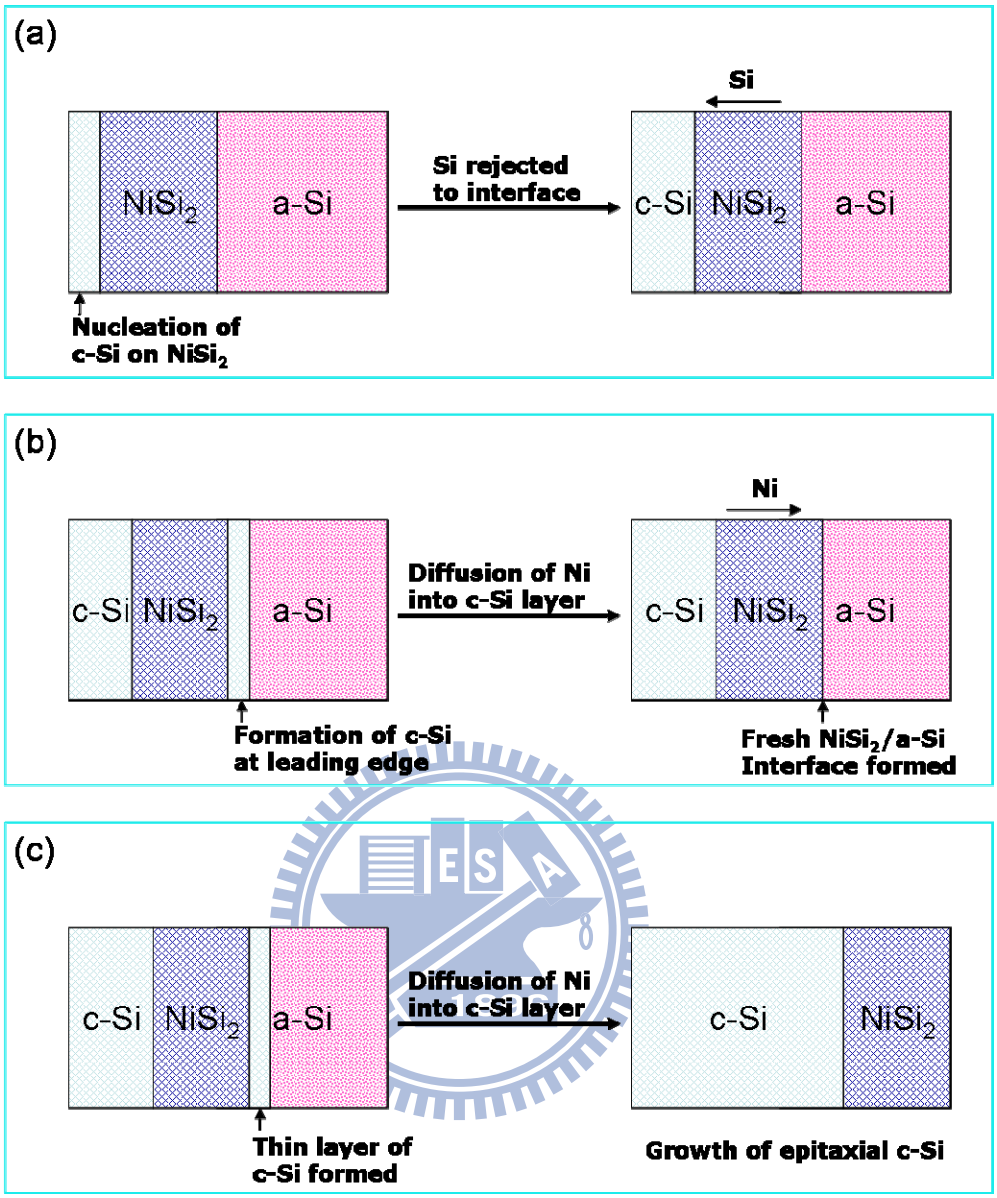


Figure 1-5 A possible modification of the c-Si growth mechanism involving the formation of a thin layer of c-Si at the α-Si/$NiSi_2$ interface [38].

precipitates would be trapped NILC poly-Si grain boundaries. The metal gettering from Si is a candidate to solve this issue.

1.3 Metal Gettering from Silicon

Transition-metals (Fe, Co, Ni and Pd) are ubiquitous in Si wafers, being introduced both during wafer growth and in subsequent processing. These metal impurities degrade the minority carrier lifetime and increase the leakage current. [46] The degradation of Si devices by metal impurities could be improved by metal gettering which is employed extensively in microelectronics and photovoltaics.

In general, the gettering process involves three steps: (1) the release of the impurities from the device region, (2) the diffusion of the impurities to the gettered region, and (3) the capture of the impurities at the gettered region, as shown in Fig. 1-6. [47] The energy barrier of the release of the impurities should be low and the captured impurities should not be release simply. Moreover, the distance between the captured region and the device region should be short; the impurities should diffuse quickly through the interface or the interlayer.

In 2000, S. M. Myers et al [48] proposed at least five distinct types of gettering mechanism, as follows: (1) metal-silicide precipitation, (2) segregation into second phase, (3) atomic trapping by defects, (4) interaction with electronic dopants, and (5) phosphorous-diffusion gettering and nonequilibrium processes. Gettering by metal-silicide precipitation

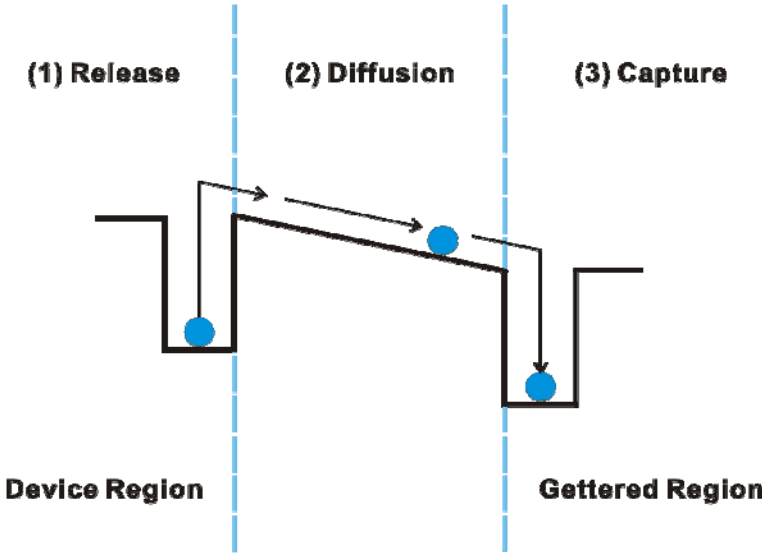


Figure 1-6 The concept of the gettering process including release, diffusion, and capture of the metal impurities [47].

is an effective method to remove metal impurities from the device region. This mechanism, as introduced in chapter 1-2-2, has been implemented by back-side polycrystalline silicon gettering [49]. The next mechanism also involves a second phase, but one formed by a third elemental species, with the transition metal being a dilute constituent. For example, gettering by segregation into a deposited Al can take place using Al–Si liquid on the back side of the wafer [50, 51]. That is because of a higher solubility of the metallic impurity in the liquid Al-Si phase compared with that in solid Si.

The imperfections or defects in Si are expected to be the gettering sits. These defects are incompletely coordinated being associated with open regions in the lattice and with Si atoms and therefore reactive. S. M. Myers et al refers to such solute-defect reactions not involving second-phase formation as trapping, Most researchers introduce the cavities into Si to getter metal (Fe [52], Co [53], Ni [54, 55], Pt [56], Au [57, 58], and Cu [59, 60]) by ion-implanting He or H. Trapping is believed to occur through a complex chemisorption-like reaction on the cavity walls.

Most transition-metal solutes are charged in Si and this characteristic can be developed for gettering by the electronic dopants. A charged metal atom and a dopant atom with opposite charge may form a bound pair, due to the electrostatic attraction. Moreover the energy of the charged metal atom is reduced, as the level of electronic doping is sufficient to

shift the Fermi level. Therefore metal impurity (Mn, Fe, and Co) segregates from an intrinsic or lightly doped region into a highly doped zone (B-doped and P-doped Si). [61, 62]

W. Schröter found that SiP precipitates form near Si/PSG interface in phosphorous-diffusion gettering and are capable of removing Ni impurities to produce $NiSi_2$ particles [63]. An influence of SiP precipitation during gettering is suggested by metal-silicide precipitation at the SiP particles. This phenomenon is also found during phosphorous- diffusion gettering of Pt [64].

These gettering methods have been effectively employed to reduce metallic impurities in Si. However these gettering methods are complicated and require high process temperatures. Even back-side gettering by ion-implanting damage is not suitable for TFTs device, due to a 500-nm-thick buffer oxide located between NILC poly-Si and the Si substrate. Hence we proposed a gettering structure, as shown in Fig. 1-7. [65-67] The mechanism of gettering is classified in metal-silicide precipitation. For effective gettering, the solubility of Ni impurities in the Ni gettering layer should be higher than that in the device region and the Ni diffusivity in the etching stop layer should be high. Thus the etching stop layer should be thin for Ni atoms diffusing quickly and well protect the device region during the removal of the Ni gettering layer. In addition, C.-M. Hu proposed the contact holes gettering [68] and wafer bonding gettering [69] with no etching stop layers.

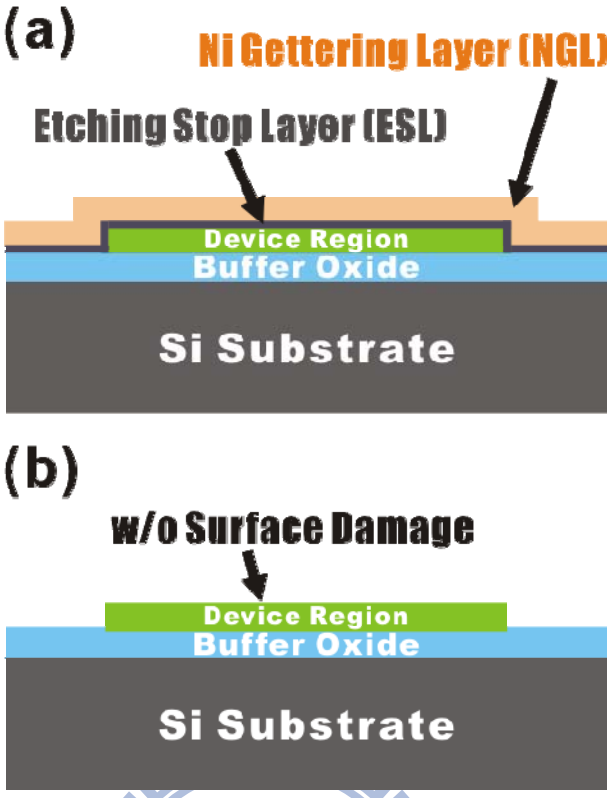


Figure 1-7 (a) A gettering structure with a Ni gettering layer and an etching stop layer, and (b) the device region protected well by an etching stop layer during the removal of the Ni gettering layer.

1.4 Silicon Nanowires (NWs) Fabrication

Low temperature poly-Si TFTs have been employed in flat panel displays. [1-6] The major advantage of poly-Si TFTs technology is its integration of driver electronics, sensors, memories, and peripheral circuits on the glass substrate for multifunctional active-matrix displays. Several techniques have been proposed to scale down poly-Si TFTs' device geometries for increasing the device density. Unfortunately, the undesirable short-channel effects (SCEs) in electrical characteristics have been found in the conventional planar short-channel poly-Si TFTs. Recently, lots of efforts on nonplanar device structures have been developed for better gate electrostatic control of the channel potential, such as nanowire channel. [70, 71] Si NWs with high surface-to-volume ratio feature have been adopted in memory devices [72], NW thin-film transistors (TFTs) [73], and biosensors [74]. In general, Si NWs fabrication could be classified into two types: top-down, and bottom-up, introduced as follows:

1.4.1 Top-Down Method

Top-down method generally requires the advanced lithography techniques, such as deep UV [75], e-beam [76]. Fist, nano-scale patterns are defined on the substrates and Si NWs then form by dry-etching. These approaches are well developed for mass production, but very expensive equipments and cutting-edge technologies are required. In addition,

several techniques, like thermal flow [77], chemical shrink [78], and spacer patterning [79] have been reported to assist the nano-scale patterns fabrication by the conventional lithography tools (G-line and I-line steppers). The conventional lithography is relatively cheap for Si NWs fabrication.

1.4.2 Bottom-Up Method

In general, Si NWs fabricated by bottom-up method need to be assembled and align for the electronics compared with top-down method. The assembly techniques such as electric-field-directed assembly [80], microfluidic channel [81] and Langmuir-Blodgett (LB) technique [82] have been proposed. Electric field method is via interaction between electric field of two parallel electrodes and polarity of NWs. Fluidic channel method could obtain assembled NW arrays by flowing NWs suspension inside a polydimethylsiloxane (PDMS) mold and LB method could assemble large-area anisotropic NWs by a compression process.

Typically the bottom-up method contains three steps: (a) deposition methods to prepare the NWs, (2) synthesis of the NWs on a substrate, and (3) dispersion of NWs into a solution. Some deposition methods have been proposed including, laser ablation catalyst growth [83], chemical deposition catalyst growth [84] and oxide-assisted catalyst-free method [85]. The first two techniques use a metal nanocluster catalyst as the nucleation

site for NWs growth. Hence metal contamination is a potential concern in this approach. Oxide-assisted catalyst-free method could fabricate NWs without metal contamination, but it is not adapted to electronic devices due to lots of defects in NWs.

Recently, H.-C. Lin et al proposed a novel TFT structure with sidewall-spacer poly-Si nanowire channels. [86-88] The feature of process is the simple method of forming sidewall-spacer of MOSFET, as shown in Fig. 1-8b. Here we fabricate NILC poly-Si NWs TFTs similar to the sidewall-spacer method to investigate the effect of Ni residues on the performance of NILC poly-Si NWs TFTs.

1.5 Motivation and Thesis Organization

High-performance low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in flat panel displays. NILC is particularly attractive for forming superior, poly-Si films with good electrical characteristics However, NILC poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates which increase the leakage current and shift the threshold voltage.

Here, we propose a technique that could effectively resolve the Ni-residue issues. Our method is using a gettering structure (Ni gettering layer/etching stop layer) to getter Ni impurities inside NILC poly-Si based on metal-silicide precipitation mechanism. It's a simple and effective process for improving the electrical properties of large area NILC TFTs. To

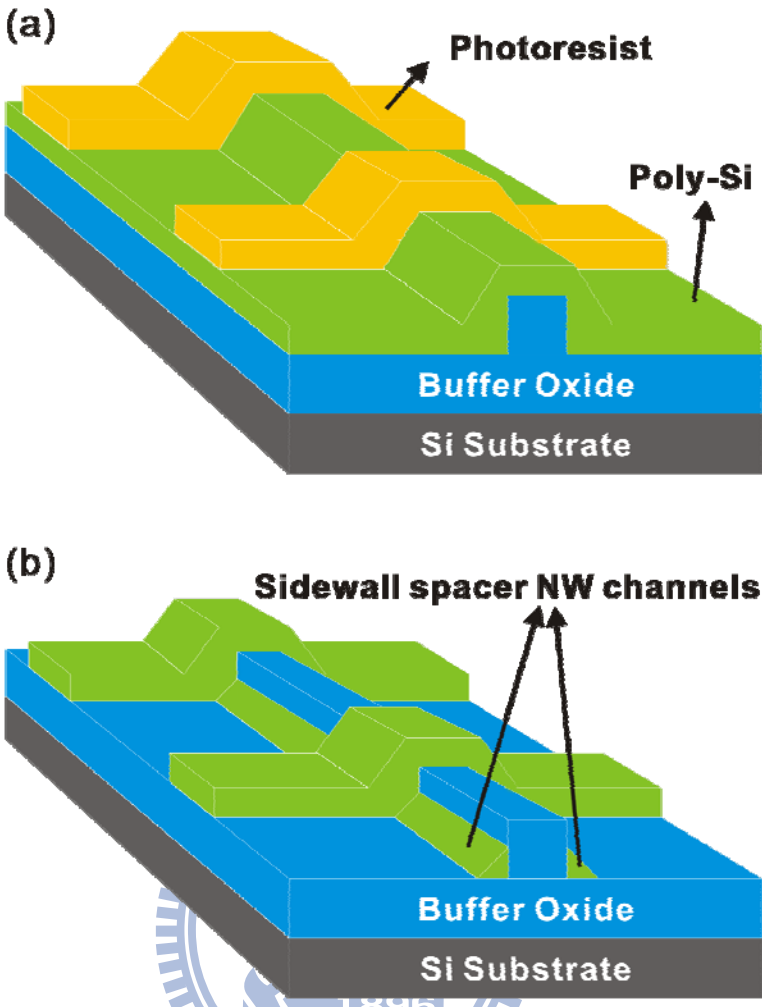


Figure 1-8 (a) Photoresist patterns on top of the poly-Si surface by the conventional lithography, and (b) the sidewall spacer NW channels fabricated by an anisotropic etching.

reduce thermal budget of the previous PECVD-SiN_x gettering, around 5-nm-thick chemical oxide is proposed as an etching stop layer. This approach is compatible to traditional TFTs fabrication and costs cheaper compared with PECVD deposition. To further improve the gettering efficiency of α-Si gettering layers, phosphorous dopant is introduced into α-Si film. This is because phosphorous-diffusion could obtain solubility enhancement of Ni impurities.

In addition to improving the performance of NILC poly-Si thin-film and NW channel transistors, the gettering of nickel impurities within NILC poly-Si is carried out. Reduction of Ni-related defects trapped in the channel layer due to NILC poly-Si nature, could suppress the leakage current and negative shift of the threshold voltage. Moreover, $NiSi_2$ precipitates are randomly trapped at poly-Si/gate oxide interfaces and poly-Si grain boundaries. Hence the uniformity of device performance could be improved through a Ni-gettering process.

The dissertation is divided into five chapters listed below:

In chapter 1, an overview of poly-Si TFTs is reviewed, and then the processes of low temperature poly-Si crystallization, the metal gettering from Si, and Si NWs fabrication are introduced. Finally, the motivation of this study and the outline of the dissertation are provided.

In chapter 2, a simple and effective Ni-gettering process is proposed to reduce Ni impurities inside NIC and NILC poly-Si films. The phosphorous-doped α-Si/chemical oxide

served as a gettering structure is introduced. Moreover, the influence of the phosphorous dopant concentration on the gettering efficiency is investigated. In this chapter, we also compare the effects of the phosphorous dopant and the argon dopant on NILC rate.

In chapter 3, the effects of Ni-gettering layers (p-α-Si/chem-SiO_2 films) on electrical characteristics of large area NILC TFTs is studied. The leakage current, threshold voltage, and the uniformity of NILC TFTs are studied after a Ni-gettering process.

In chapter 4, the fabrication of NILC poly-Si TFTs with a couple Si NWs is introduced. The effect of Ni residues on the performance of NILC poly-Si NWs TFTs is investigated. The proposed gettering method is employed to improve the electrical characteristics of NILC poly-Si NWs TFTs.

Finally, conclusions and future work are given in chapter 5.

Chapter 2 Ni Reduction of Nickel-Mediated Crystallization Polycrystalline Silicon Using A Ni-Gettering Process

2.1 Introduction

Several metal gettering methods have been employed to reduce the amount of undesired metallic impurities in Si. However these gettering methods are complicated and require high process temperatures. In previous studies [65], we have proposed a simple method for reducing Ni concentration inside the NILC film. It involves using α-Si and silicon-nitride (SiN_x) films as Ni-gettering layers. The top α-Si layer served as a gettering layer, while the middle SiN_x layer was used as an etching stop layer. However the gettering time required was 90 h due to low Ni diffusivity in SiN_x. To reduce the thermal budget of the Ni-gettering process, we use α-Si and chemical oxide (chem-SiO_2) films as Ni-gettering layers, because Ni atoms transfer quickly through the nanothick-SiO_2 layer [89].

During the gettering process, Ni atoms were diffused from the NILC film to the α-Si layer due to the concentration gradient. When the system reached equilibrium, no more Ni diffused into the gettering layer. At this point, the Ni concentration in the α-Si layer was the

same as that in NILC. To improve the Ni-gettering efficiency, phosphorus-doped α-Si (p-α-Si) films and chemical SiO_2 (chem-SiO_2) layers are used as gettering layers. The effect of phosphorus dopant on the Ni-gettering efficiency is investigated in this chapter.

2.2 Experimental Procedure

2.2.1 Gettering of Ni Residues from NILC Poly-Si Films

Three kinds of poly-Si films are investigated in this study. One is a poly-Si film fabricated by traditional NILC method without the gettering process (referred to as NoGET), and the others are poly-Si films fabricated by the same NILC method with different Ni-gettering layers (referred to as ASiGET and PSiGET). The NILC fabrication process began with capping 4-inch Si (100) wafers with 500-nm-thick wet thermal oxide. Silane-based 100-nm-thick α-Si films were then deposited using low-pressure chemical vapor deposition (LPCVD) at 550^{o}C in N_2 ambient. The photoresist was patterned to form desired Ni lines, and a 5-nm-thick Ni film was deposited on the α-Si.

To form NoGET poly-Si films, samples were annealed at 540^{o}C for 24 h in N_2 ambient, as shown in Fig. 2-1a. The unreacted Ni was then removed by a mixed solution of H_2SO_4 and H_2O_2 for 20 min. Finally, poly-Si films were dipped into 1% diluted hydrogen fluoride (DHF) solution to remove the annealing surface oxide, as illustrated in Fig. 2-1b.

As for the ASiGET poly-Si film, a NoGET poly-Si film was dipped into a mixed solution of

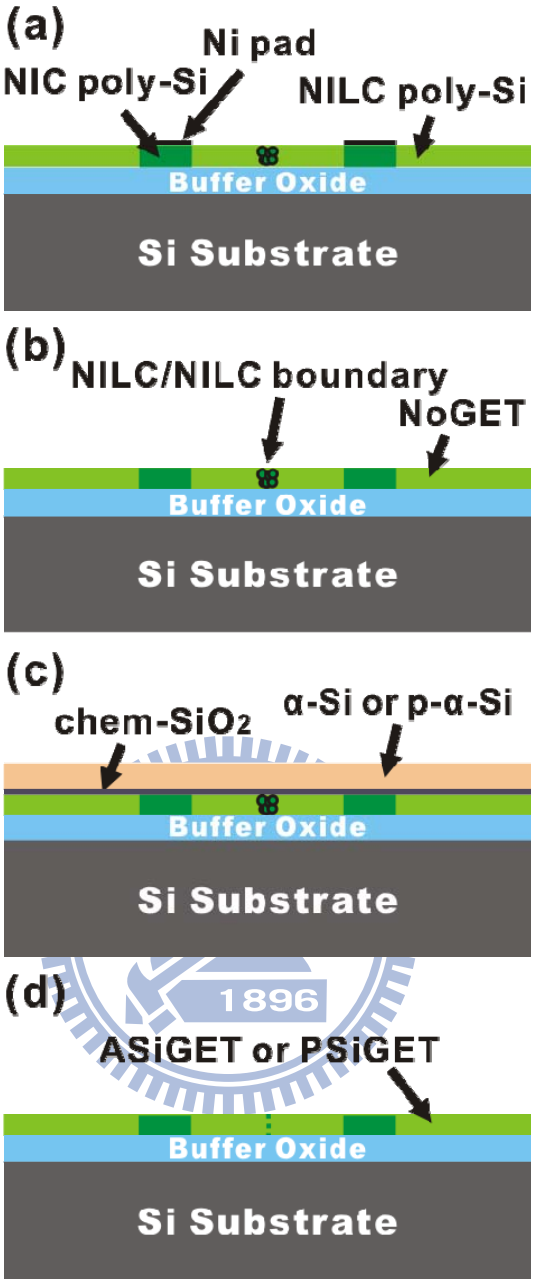


Figure 2-1 Schematic illustration of the Ni-gettering process: (a) fabrication of the NILC poly-Si film, (b) removal of unreacted Ni pads, (c) capped with an etching stop layer (chem-SiO_2) and a gettering layer (α-Si or p-α-Si), and (d) removal of the gettering layer and the chem-SiO_2 layer.

H_2SO_4 and H_2O_2 for 10 min to form a chem-SiO_2 layer on the top of NILC poly-Si films. A 100-nm-thick α-Si film was then deposited on the chem-SiO_2 layer using LPCVD at 550°C for 1 h in N_2 ambient, as shown in Fig. 2-1c. The top α-Si film served as the Ni-gettering layer.

As for the PSiGET poly-Si films, phosphorus ions were implanted into α-Si to form a p-α-Si film, as shown in Fig. 2-1c. The projection range (R_p) of ions was set at the middle of the α-Si film. The ion-accelerating energy was 35 keV. The dosage of phosphorus ions were 1×10^{14} cm^{-2}, 1×10^{15} cm^{-2} and 1×10^{16} cm^{-2}, respectively. Relevant parameters for the samples studied are summarized in Table 2-1.

Samples undergoing Ni-gettering were then annealed at 550°C for 12 h in N_2 ambient with the goal of removing the unwanted Ni metal inside the NILC poly-Si. Following the annealing process, the top Ni-gettering films were removed using 5% tetramethylammonium hydroxide (TMAH) solution for 2 min at 55°C, and the chem-SiO_2 layers were removed using 1% DHF solution, as illustrated in Fig. 2-1d. For the purpose of comparison, the NoGET poly-Si film was also subjected to an extended heat treatment at 550°C for 12 h in N_2 ambient.

2.2.2 Gettering of Ni Residues from NIC Poly-Si Films

The fabrication process of NIC poly-Si is shown in Fig. 2-2. Silane-based 100-nm-thick α-Si films were deposited using LPCVD at 550°C in N_2 ambient, as displayed in Fig. 2-2a. A

Table 2-1 Relevant parameters of the Ni-gettering layers.

Sample	Gettering Layer	Phosphorus Implantation
		Dose(/cm^2)
NoGET	w/o	w/o
ASiGET	α-Si	w/o
PSiGET-14	p14-α-Si	1x10^{14}
PSiGET-15	p15-α-Si	1x10^{15}
PSiGET-16	p16-α-Si	1x10^{16}

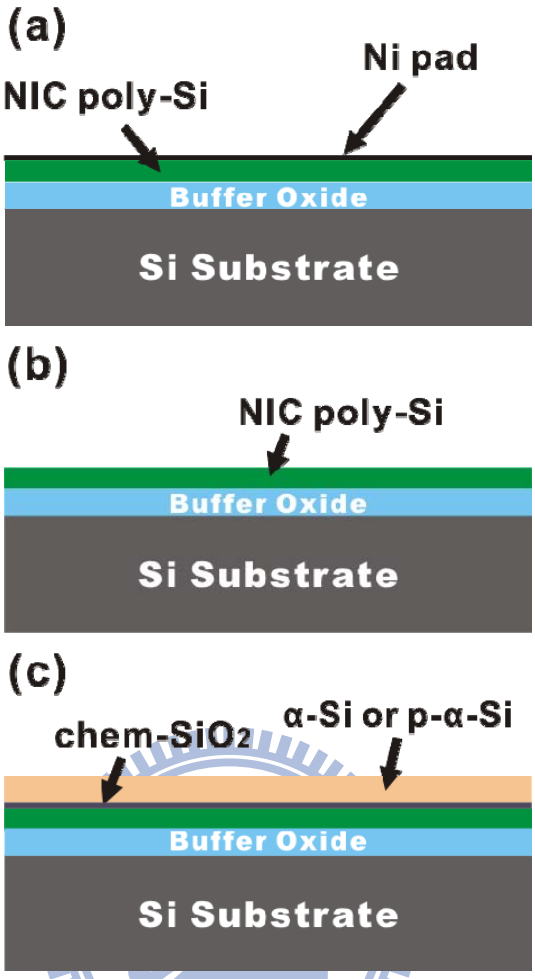


Figure 2-2 Schematic illustration of the Ni-gettering process of the NIC poly-Si: (a) fabrication of the NIC poly-Si film (b) removal of unreacted Ni films, and (c) capped with a chem-SiO_2 layer and a gettering layer (α-Si or p-α-Si).

5-nm-thick Ni film was then deposited on the α-Si, and subsequently annealed at 540^{o}C for 24 h to form NIC poly-Si. The unreacted Ni was then removed by a mixed solution of H_2SO_4 and H_2O_2 for 20 min. Finally, poly-Si films were dipped into 1% DHF solution to remove the annealing surface oxide, as shown in Fig. 2-2b. The poly-Si film was dipped into a mixed solution of H_2SO_4 and H_2O_2 to form a chem-SiO_2 layer. A 100-nm-thick α-Si film was then deposited on the chem-SiO_2 layer using LPCVD at 550^{o}C for 1 h in N_2 ambient to form the α-Si gettering layer, as illustrated in Fig. 2-2c. Phosphorous ions were implanted into α-Si to form the p-α-Si gettering layer. The dosage of phosphorus ions and the ion-accelerating energy were 1×10^{16} cm^{-2} and 35 keV, respectively. Samples were then annealed at 550^{o}C for 12 h in N_2 ambient.

2.2.3 Dopant Effect on NILC Rate

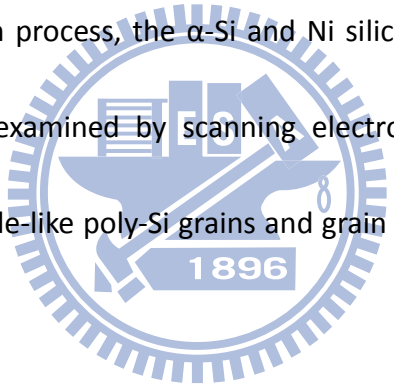
Three kinds of α-Si films are investigated in this study. One is intrinsic α-Si, and the others are α-Si films introduced by argon ions and phosphorus ions, respectively. First, silane-based 100-nm-thick α-Si films were deposited on oxide Si substrates using LPCVD, followed by ion implantation. The R_p of ions was then set at the middle of the α-Si film and the dosage was 1×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, and 1×10^{16} cm^{-2}, respectively. Then 5-nm-thick Ni lines were selectively deposited on sample surfaces. Finally the traditional NILC method was carried out at 540^{o}C for 16 h in N_2 ambient.

2.3 Results and Discussion

2.3.1 Characterization of NILC Poly-Si Films

The length of the NILC poly-Si is about 79μm and almost saturated, as shown in Fig. 2-3. Since solid-phase crystallization (SPC) poly-Si grains formed near interface between α-Si and NILC poly-Si, the NILC poly-Si grains laterally growth was blocked. Therefore we can obviously see the winding interface (α-Si/NILC poly-Si). Before the NILC got saturated, we can examine NICL rate as 3.59 μm/h, as shown in Fig. 2-4.

After a NILC fabrication process, the α-Si and Ni silicide were etched away with Secco etching solution [90] and examined by scanning electron microscope (SEM). The NILC poly-Si is composed of needle-like poly-Si grains and grain size is about 100 nm, as displayed in Fig. 2-5.



2.3.2 Quality of chem-SiO_2 Layers

To examine the quality of the chem-SiO_2 film, after the chem-SiO_2 layer was formed, platinum was deposited on top of the chem-SiO_2 film for image contrast in transmission electron microscopy (TEM) sample preparation. As shown in Fig. 2-6, the oxide layer is only about 5 nm thick. This chem-SiO_2 layer was used as an etching stop layer in the 5% TMAH etching solution. Moreover, this nano oxide layer also served as a diffusion interlayer during the Ni-gettering process. Ni atoms needed to diffuse from the NILC poly-Si through

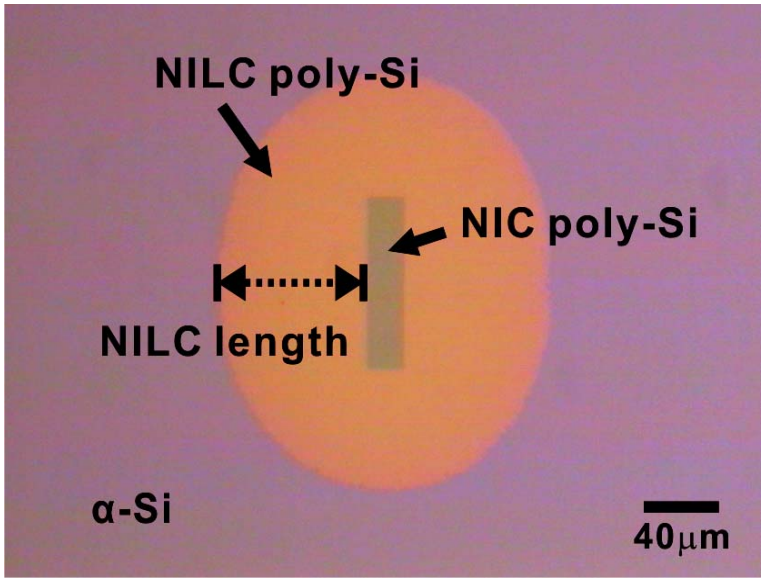


Figure 2-3 OM image of the α-Si film after a NILC process carried out at 540°C for 24 h in N_2 ambient.

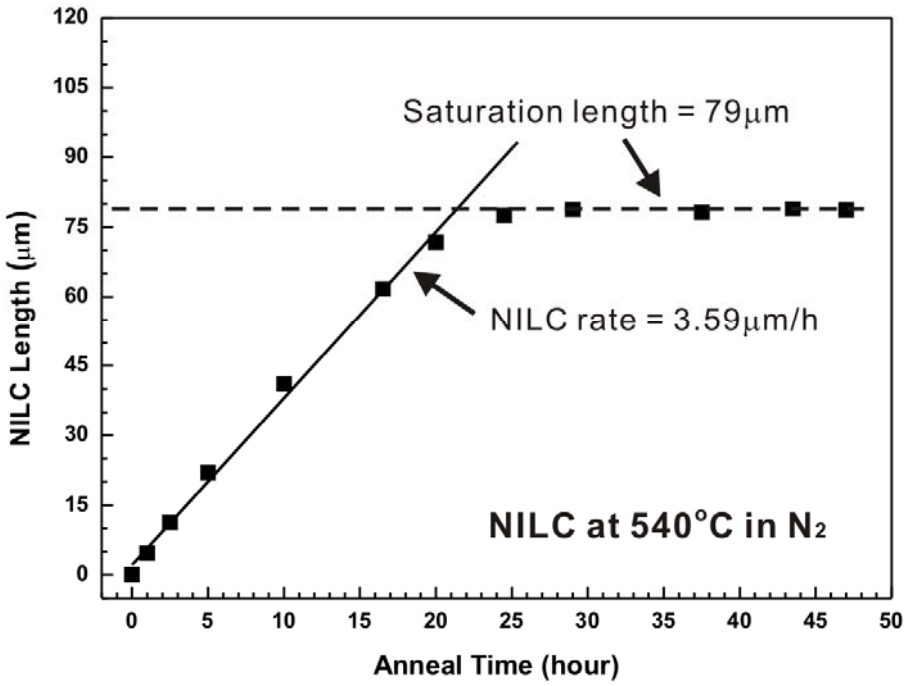


Figure 2-4 The dependence of the NILC length on the anneal time. The NILC was carried out at 540°C in N_2 ambient.

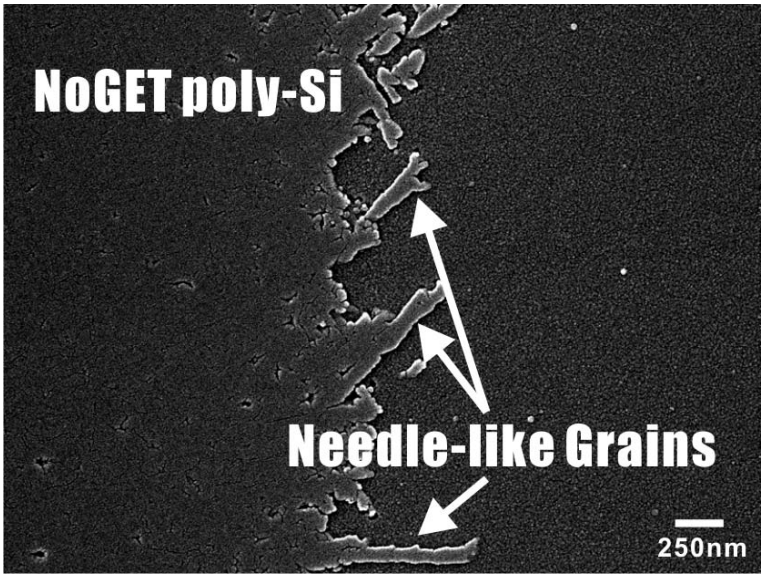


Figure 2-5 SEM image of the NILC poly-Si grains treated with Secco-etching.

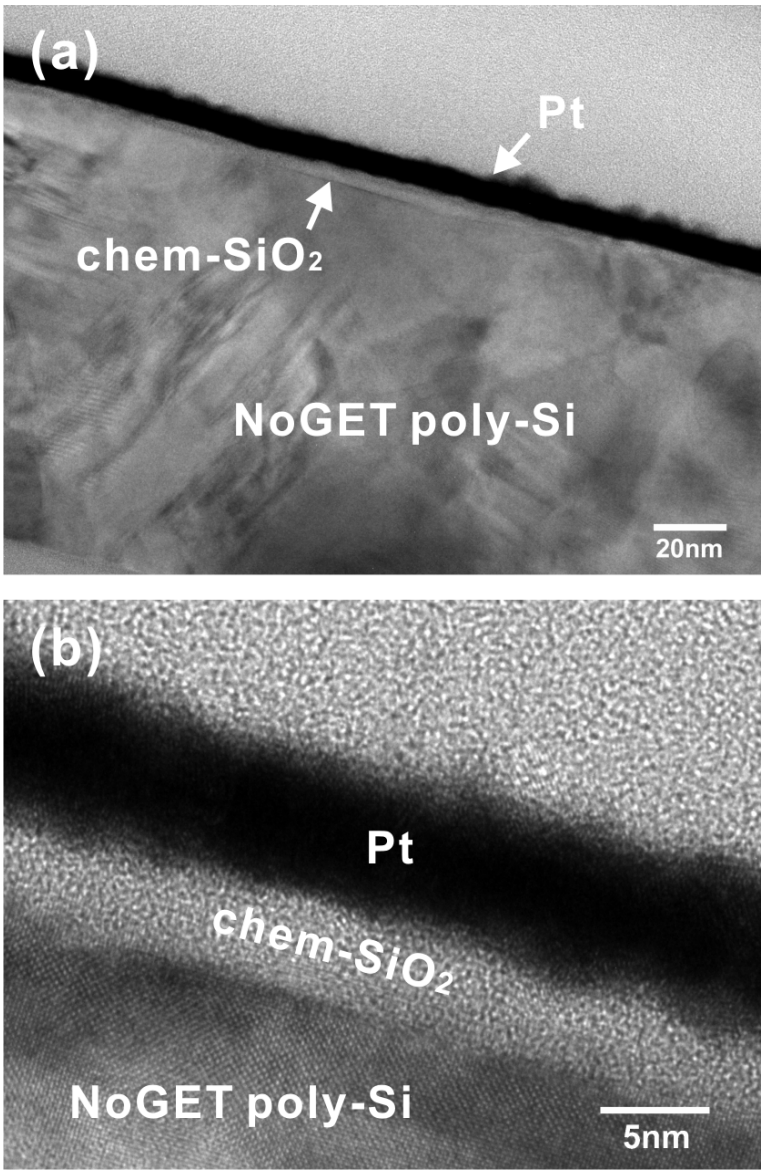


Figure 2-6 (a) Cross-sectional TEM images of the NILC Poly-Si films capped with the chemical oxide films, and (b) the high magnification of a chemical oxide film around 5 nm thick. Platinum (Pt) films were deposited on top of the chem-SiO_2 layers for image contrast.

the thin chem-SO_2 into the Ni-gettering layer. The chem-SiO_2 in Fig. 2-6b tends to be porous and amorphous. Therefore Ni atoms possibly diffused through 5-nm-thick chem-SiO_2 faster compared with 30-nm-thick SiN_x [65] used before.

To study the effect of Ni-gettering on the surface roughness of the NILC poly-Si after gettering layers removal, the NILC poly-Si surfaces were measured using atomic force microscopy (AFM). As shown in Fig 2-7, the metal gettering did not change the surface roughness greatly: the root-mean-square (RMS) roughness of ASiGET (0.65 nm) and PSiGET-16 (0.69 nm) are almost the same as that of NoGET (0.64 nm). This seems that 5-nm-thick chem-SiO_2 layer did protect ASiGET and PSiGET-16 poly-Si surfaces during wet etching by 5% TMAH solution.

2.3.3 Ni-Gettering Using chem-SiO_2 Interlayer

Figure 2-8a shows the optical microscopy (OM) images of the Ni-gettering layers after it was deposited on top of the chem-SiO_2 layer using LPCVD at 550°C for 1 h in N_2 ambient. The pink region is α-Si and the green regions are disk-like poly-Si. This result indicates that during the deposition of α-Si film, some Ni atoms had already diffused from the NIC area through the chem-SiO_2 layer into the gettering layer and caused α-Si to be transformed into poly-Si grains by the NILC mechanism. However in the case of the α-Si/SiN_x-gettering process [65], no NILC poly-Si was observed on the gettering layer during the deposition of

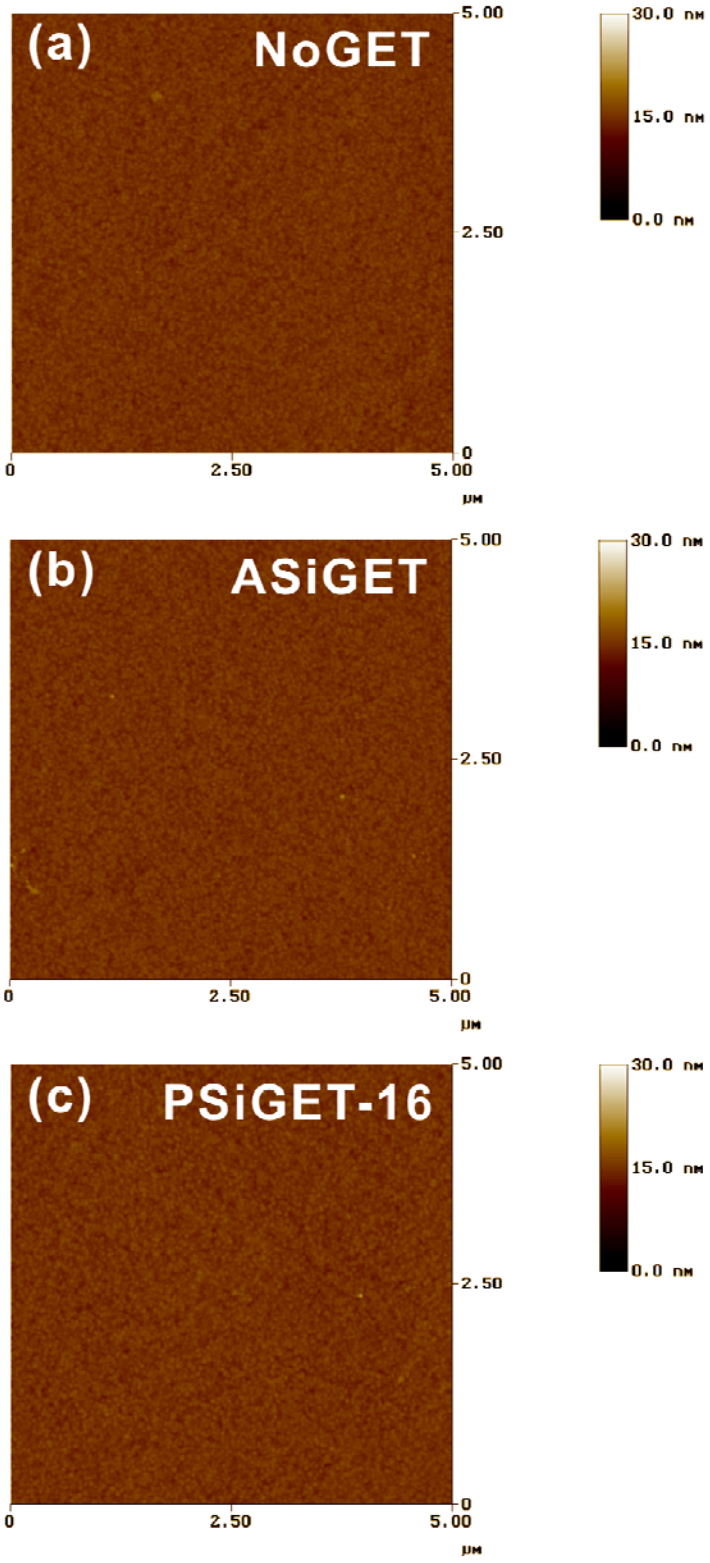


Figure 2-7 AFM images of the NILC poly-Si surfaces (a) without Ni-gettering, and with Ni-gettering by (b) a α-Si layer, and (c) a p-α-Si layer (the dosage was 1×10^{16} cm^{-2}).

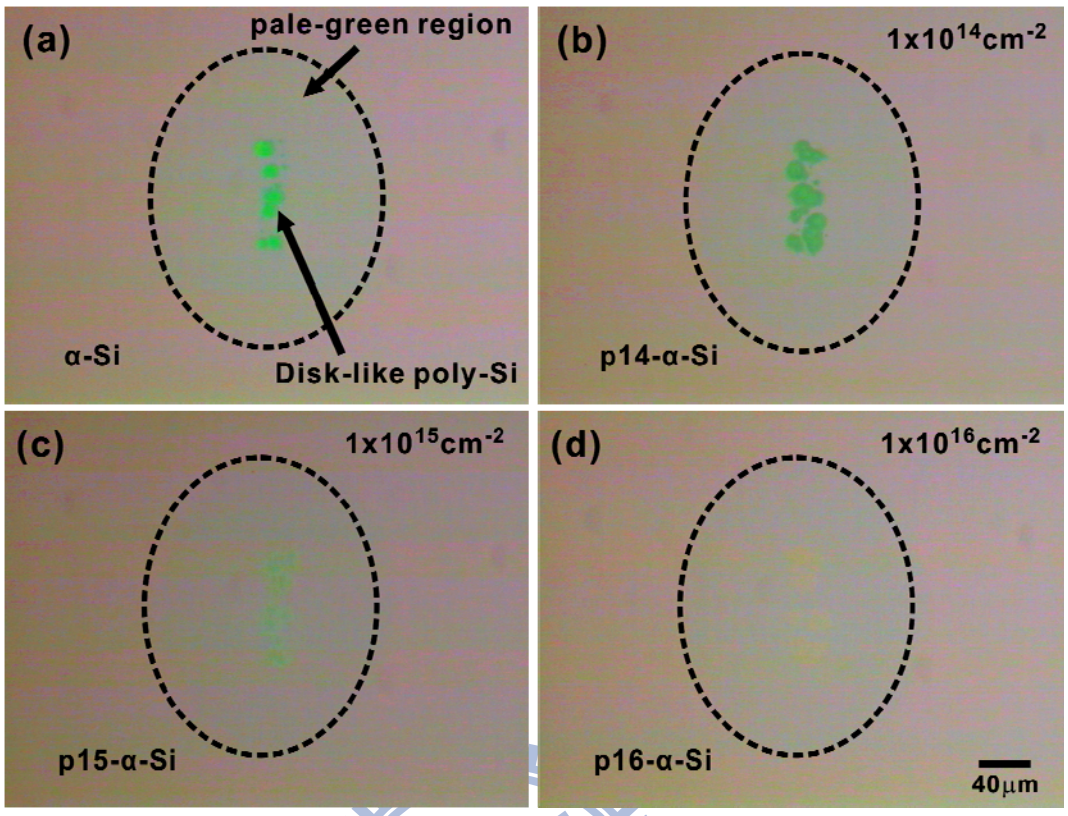


Figure 2-8 OM images of the Ni-gettering layers: (a) a α-Si film deposited on a chem-SiO_2 layer by LPCVD and then phosphorous ions implanted at a dosage of (b) 1×10^{14} cm^{-2}, (c) 1×10^{15} cm^{-2}, and (d) 1×10^{16} cm^{-2}, respectively.

α-Si. After phosphorus ions implantation, the green regions disappear, as illustrated in Fig. 2-8d. This means the original NILC poly-Si grains became amorphous through phosphorus ions bombard.

The pale-green region in Fig. 2-8a is the NILC poly-Si on the NoGET film underneath a chem-SiO_2 layer. This means that during the gettering process, Ni atoms diffused from the NoGET film through chem-SiO_2 into the Ni-gettering layer due to the concentration gradient. When Ni atoms reached the gettering film, enough Ni metal would be accumulated to form $NiSi_2$ precipitates, and α-Si would then be transformed into needle-like poly-Si grains by the NILC mechanism. NILC poly-Si grains first appear right above the top of the NIC area, and then extend to the surrounding areas. This is because the Ni concentration above the NIC area was higher than that in other areas of the gettering film. Therefore, we can still see the NIC strip patterns, as displayed in Fig. 2-9.

2.3.4 Improved Ni-Gettering Efficiency by Phosphorus Ions Implant

After the gettering process, the gettering layers were examined by OM to investigate the gettering efficiency. The results are shown in Fig. 2-9. In Fig. 2-9a, the pink region is α-Si and the green region is needle-like NILC poly-Si verified by SEM, as shown in Fig. 2-10a. The microstructure of NILC poly-Si, in Fig. 2-9d, is composed of needle-like poly-Si grains but etched away mostly by Secco etching solution, as illustrated in Fig. 2-10b. This means

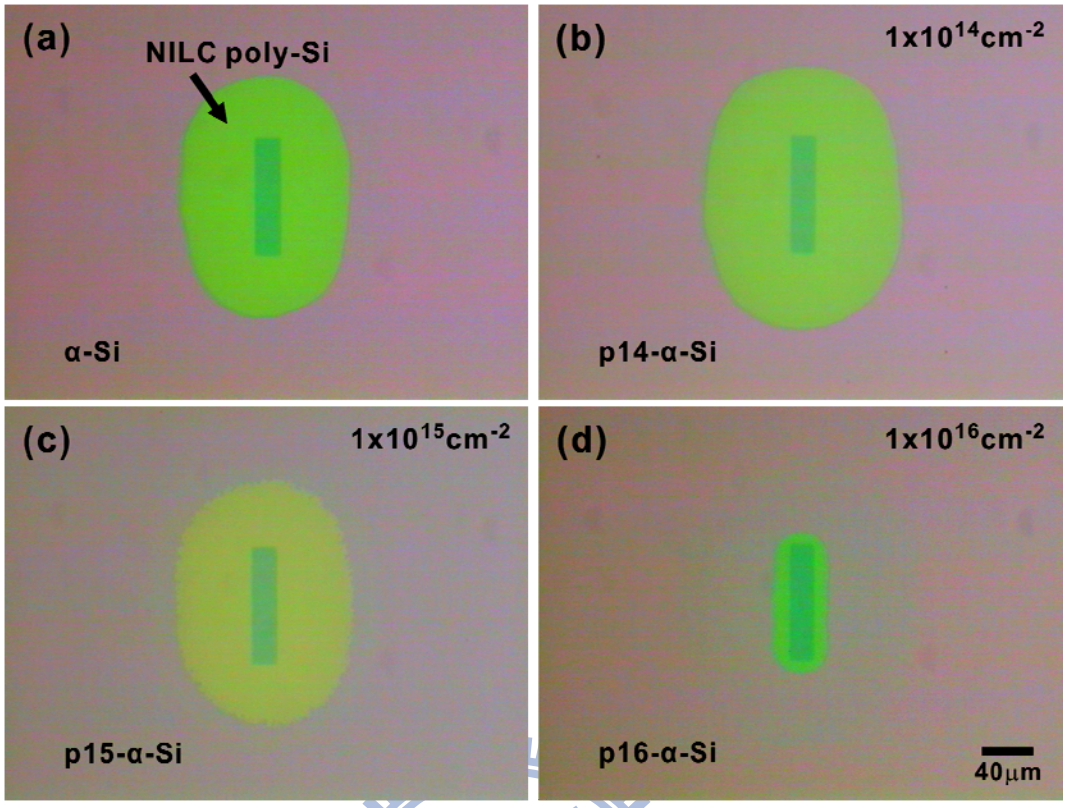


Figure 2-9 OM images of the Ni-gettering phenomenon by (a) a α-Si film, and the phosphorous-doped α-Si films at a dosage of (b) 1×10^{14} cm^{-2}, (c) 1×10^{15} cm^{-2}, and (d) 1×10^{16} cm^{-2}, respectively.

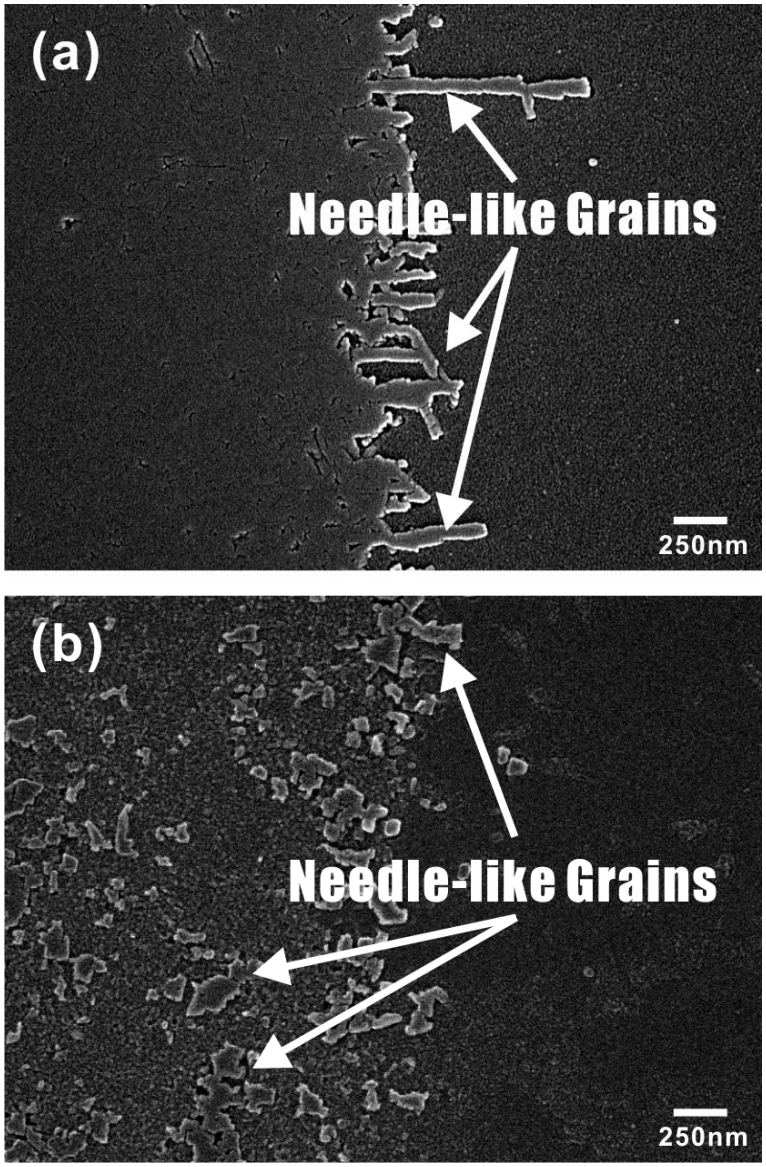


Figure 2-10 SEM images of the NILC poly-Si grains of Ni-gettering layers: (a) a α-Si film, and (b) a phosphorous-doped α-Si film at a dosage of 1×10^{16} cm^{-2}. Samples were treated with Secco-etching.

that some implant damages formed in intrinsic α-Si during ion implantation. When p16-α-Si was transformed into NILC poly-Si, the crystalline quality was poor and these damages or defects trapped Ni. Therefore a lot of NILC poly-Si grains were etched away.

Figure 2-9d also shows that the length of the NILC poly-Si growth on the p16-α-Si gettering layer is 13μm, which is much shorter than that (60 μm) on the α-Si gettering layer. Since the NILC grains were induced by indiffusion of Ni atoms, it seemed that phosphorus dopant did not improve the gettering efficiency of α-Si. The further investigation of the dopant effect on the NILC rate is discussed in chapter 2-3-5.

In addition to the gettering layer, the gettering efficiencies of ASiGET and PSiGET poly-Si films are also investigated. The NILC/NILC boundary in Fig. 2-11 is examined by SEM to compare Ni-gettering efficiency. After the gettering layer and chem-SiO_2 were removed, the samples were dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O=4:1:50). As shown in Fig. 2-12a and b, numerous holes are observed at the boundaries where two NILC poly-Si fronts intersected (NILC/NILC boundaries). These holes are residues of the Ni silicide that had been etched away by the silicide-etching solution. These silicide-etching holes seen in Fig. 2-12b are quite sensitive to the reduction of Ni residue in the NILC poly-Si, and are therefore ideal for elucidating the ‘‘Ni gettering’’ phenomenon observed.

After the gettering process, fewer and smaller silicide-etching holes are found at the

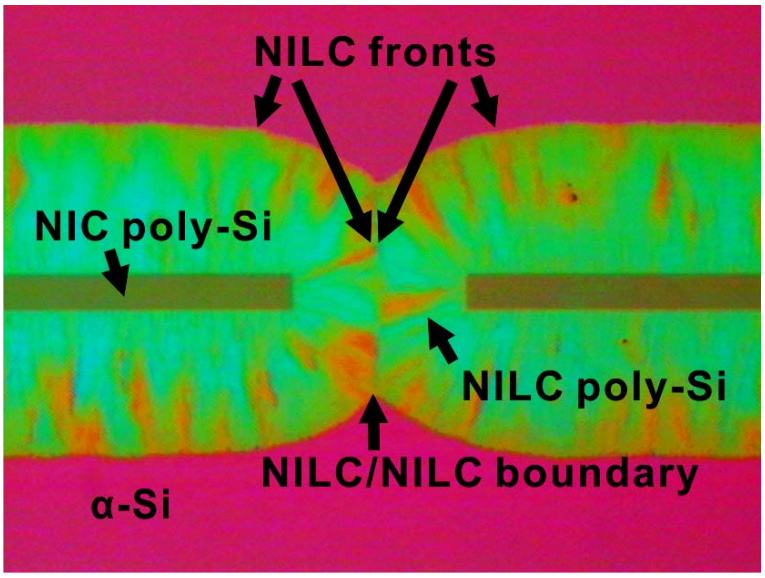


Figure 2-11 OM image of NILC/NILC boundary treated with TMAH etching.

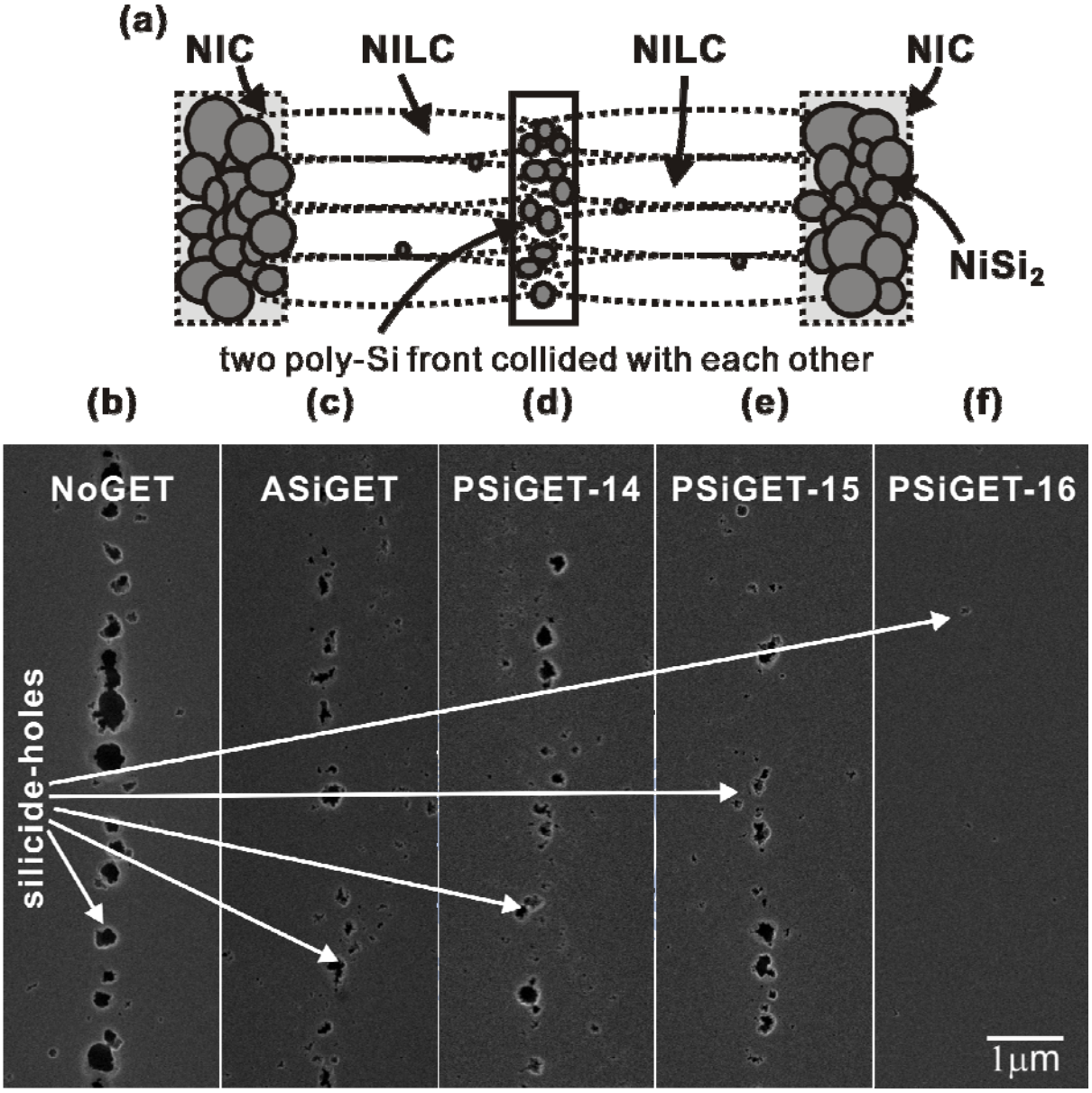


Figure 2-12 Schematic illustration of (a) silicide-etching holes at NILC/NILC boundaries, and SEM images of etching holes of (b) NoGET, (c) ASiGET, (d) PSiGET-14, (e) PSiGET-15, and (f) PSiGET-16. Samples were treated with the silicide-etching solution.

NILC/NILC boundaries of ASiGET, PSiGET-14 and PSiGET-15 as shown in Fig. 2-12c-e. Furthermore, there are almost no silicide-etching holes observed at the NILC/NILC boundaries of PSiGET-16, as shown in Fig. 2-12f. These results indicate that phosphorous dopant did improve the gettering efficiency of α-Si, which is different from our OM observation of gettering layers (Fig. 2-9). But the gettering efficiency obviously improves until doping phosphorus ions at a dose of 1×10^{16} cm^{-2}.

Secondary-ion mass spectroscopy (SIMS) was employed to clarify the Ni concentration in PSiGET-16 and ASiGET. Unfortunately, the Ni concentration in the NILC poly-Si is hard to measure since the SIMS sputtering area (125 μm × 125 μm) is much larger than that in the NILC poly-Si area. Therefore, we used NIC poly-Si to demonstrate that phosphorus dopant did improve the gettering efficiency of α-Si. Furthermore, we verified the microstructure of gettering samples by TEM. The results are shown in Fig. 2-13. The top region of the gettering layer displays darker than the bottom region does. This means that implant strains remained inside the top region of p16-α-Si layer. The R_p in Fig 2-13b is about 50 nm in depth and the gettering layer is about 110 nm thick.

Even though the Ni concentration in NIC poly-Si was much higher than that in NILC poly-Si, we can still have a preliminary understanding of the gettering efficiency of α-Si films. Figure 2-14 shows that the Ni concentration of NIC poly-Si is reduced after the Ni-gettering

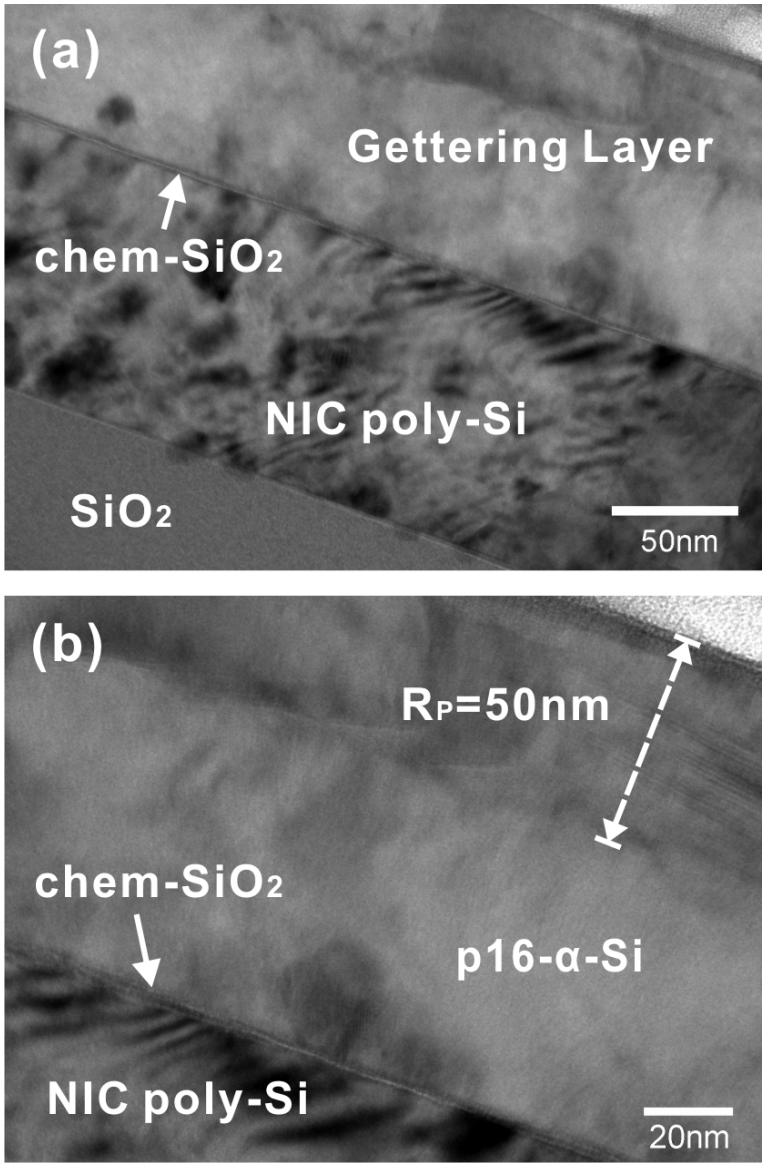


Figure 2-13 (a) Cross-sectional TEM images of NIC Poly-Si films capped with chemical oxide films and gettering layers, and (b) the high magnification of a gettering layer around 110 nm thick. The gettering layer was implanted with 1×10^{16} cm^{-2} phosphorous ions and the projection range (Rp) was about 50 nm in depth.

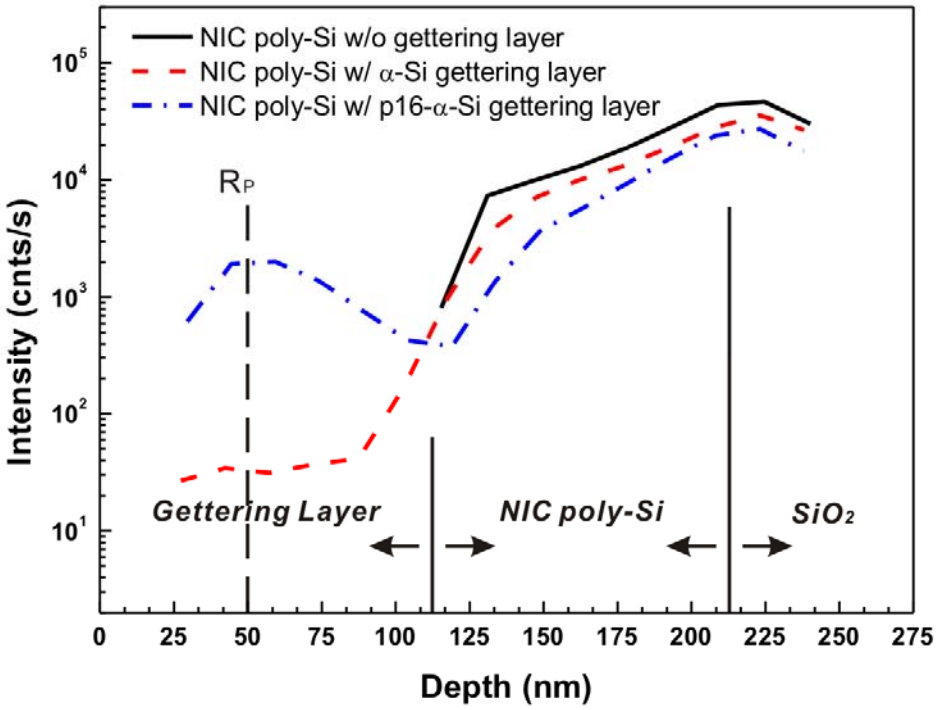


Figure 2-14 SIMS depth profiles of NIC poly-Si films treated with and without a Ni-gettering process.

process. As can be seen, the Ni concentration in NIC poly-Si with the α-Si gettering layer is relatively higher than that with the p16-α-Si gettering layer. Moreover, p16-α-Si layer traps many more Ni atoms than does α-Si layer. These results indicate that phosphorous dopant did improve the gettering efficiency of α-Si.

Figure 2-14 also shows that the middle of the p16-α-Si layer has a higher Ni concentration than other parts of the layer. This concentration distribution of Ni is similar to that of phosphorous atoms since the projection range of phosphorous ions is set at the middle of the α-Si film. This result also indicates that phosphorus did trap Ni atoms.

In the gettering process, when more Ni atoms diffused into the gettering layer, more α-Si would be transformed into poly-Si by the NILC mechanism. The gettering efficiency increased with the growth of NILC poly-Si grains. However, when the system reached equilibrium, no more Ni could diffuse into the gettering layer. At this point, the Ni concentration in the α-Si gettering layer will be the same as that in ASiGET. However, the Ni concentration in the p16-α-Si gettering layer will be higher than that in PSiGET-16 since phosphorus implant traps Ni atoms. In other words, the gettering efficiency of α-Si is indeed improved by phosphorous dopant at a dose of 1×10^{16} cm^{-2}.

2.3.5 Effect of Phosphorus Ions and Implant Damages on NILC Rate

To further investigate the dopant effect on NILC rate, either phosphorus dopant or

defects were introduced into the α-Si, before NILC process. Figure 2-15 shows that the phosphorus dopant slows down NILC rate. As a result, the length of the NILC poly-Si growth on p-α-Si (Fig. 2-9) is much shorter than that on α-Si. Figure 2-15 also shows that the NILC rate on the P-doped α-Si film is 0.55 μm/h, which is shorter than that (1.81 μm/h) on the Ar-doped α-Si film. Figure 2-16 reveals that the reduction in the NILC rate of the P-doped α-Si film is more than for that of the Ar-doped α-Si film. Compared to an intrinsic sample, a monotonic reduction in the NILC rate with an increasing dose of both implanted samples is observed. This seems that the phosphorus dopant trapped many more Ni atoms than did the argon dopant. A unified explanation is Ni trapping due to gettering by phosphorous, implant damage [91].

2.4 Summary

Two kinds of films are employed to investigate the effect of phosphorus dopant on the gettering efficiency of α-Si. To form the ASiGET and PSiGET, a ~5-nm-thick porous chem-SiO_2 layer was capped on the top of the NoGET film, and then either α-Si or p-α-Si film was deposited on the top of the chem-SiO_2 film. The chem-SiO_2 layer was used as an etching stop layer, while the Si film served as a gettering layer. It is found that the Ni concentration in the NoGET film is greatly reduced after gettering at 550^{o}C for 12 h in N_2 ambient. Compared with those on the NoGET film, the silicide-etching holes found at the NILC/NILC boundaries of ASiGET are fewer and smaller, while almost no holes are

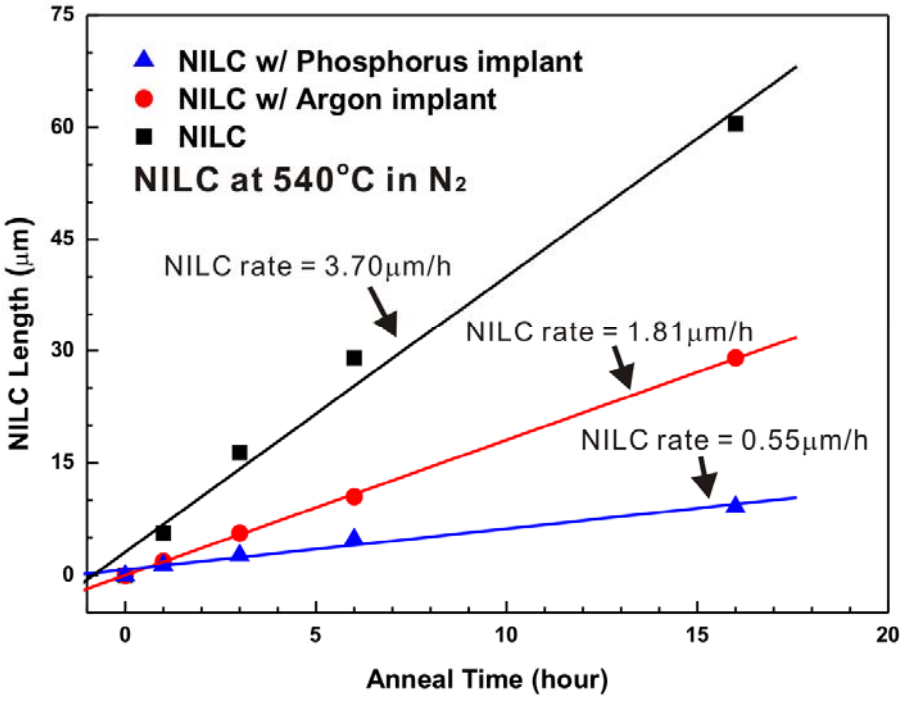


Figure 2-15 NILC length vs. anneal time and different doping type. NILC was carried out at 540°C in N_2 ambient.

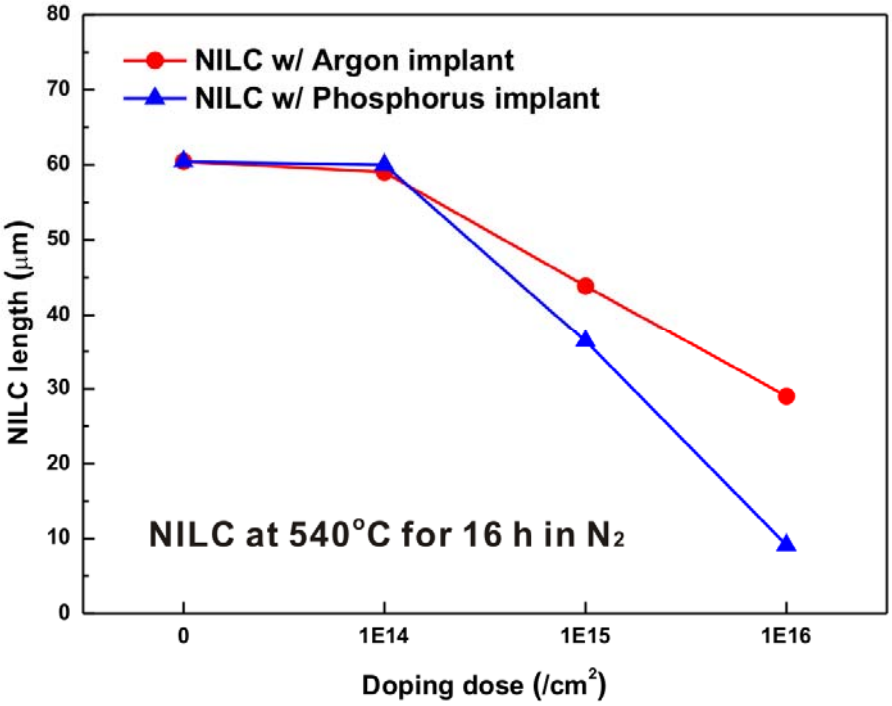


Figure 2-16 NILC length vs. different doping type and dose after heat treatment at 540°C for 16 h in N_2 ambient.

observed at the boundaries of PSiGET-16. These results indicate that phosphorous dopant could improve the gettering efficiency of α-Si due to the solubility enhancement of Ni impurities.

It is also found that the gettering layer is transformed into poly-Si by the NILC mechanism. This is because the concentration gradient acts as a driving force for transport of Ni atoms from the NoGET poly-Si films through the chem-SiO_2 layers to the gettering layers. The NILC fraction in the gettering layer increases with an increase in annealing time and temperature, as expected from the kinetic nature of the diffusion process. Moreover, the length of NILC poly-Si growth on the p16-α-Si gettering layer is much shorter than that on the α-Si gettering layer. This is because phosphorus implant and implant damage trap Ni and slow down the NILC rate on the gettering layer. In other words, the gettering efficiency of α-Si is indeed improved by the doping of phosphorous ions at a dose of 1×10^{16} cm^{-2}.

Chapter 3 Using Phosphorous-Doped α-Si Gettering Layer to Improve NILC Poly-Si TFTs Performance

3.1 Introduction

High-performance low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in liquid crystal displays and organic light emitting diode displays on cheap glass substrates. [4-6] Some methods, including excimer laser crystallization (ELC) [92], nickel-metal induced crystallization (NIC), and nickel-metal induced laterally crystallization (NILC) [7-12], for fabricating high-quality poly-Si have been extensively investigated. Among these techniques, NILC not only could obtain high-uniformity poly-Si, but could also reduce manufacturing costs. However, NILC poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates which increase the leakage current and shift the threshold voltage. [12-16] To improve performance of device, Ni contamination inside the NILC poly-Si film should be reduced.

In chapter 2, our previous work used a phosphorous-doped amorphous silicon (p-α-Si) layer and an etching stop layer to reduce Ni residues inside NILC poly-Si [66, 67]. The results

indeed reveal that Ni residues inside NILC poly-Si grain and trapped at grain boundaries reduce. Here, the performance of these TFTs is extensively investigated, especially on the leakage current and the threshold voltage. It was found that the performance and the uniformity of the NILC poly-Si TFTs were improved after a Ni-gettering process.

3.2 Device Fabrication

Typical top-gated NILC poly-Si TFTs are used in this study. Figure 3-1a shows the top view of the fabricated device. NILC/NILC boundaries are located at the middle of the channel region. Two kinds of poly-Si films are investigated in this study. One is "NILC-Si" poly-Si film fabricated by the traditional NILC method, and the other is "GETR-Si" poly-Si film fabricated by the same NILC method with an additional Ni-gettering process.

The basic NILC fabrication process of both poly-Si films began with four-inch Si (100) wafer substrates where wet oxide films of 500 nm were grown using a H_2/O_2 mixture. Silane-based α-Si films with a thickness of 100 nm were then deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C in N_2 ambient. The photoresist was patterned to form the desired Ni lines, and a 5-nm-thick Ni film was deposited onto the α-Si. The samples were then dipped into acetone for 5 min to remove the photoresist, and subsequently annealed at 540°C for 24 h in N_2 ambient to form the NILC-Si film. To reduce Ni contamination, the unreacted Ni metal was removed by chemical etching. The active

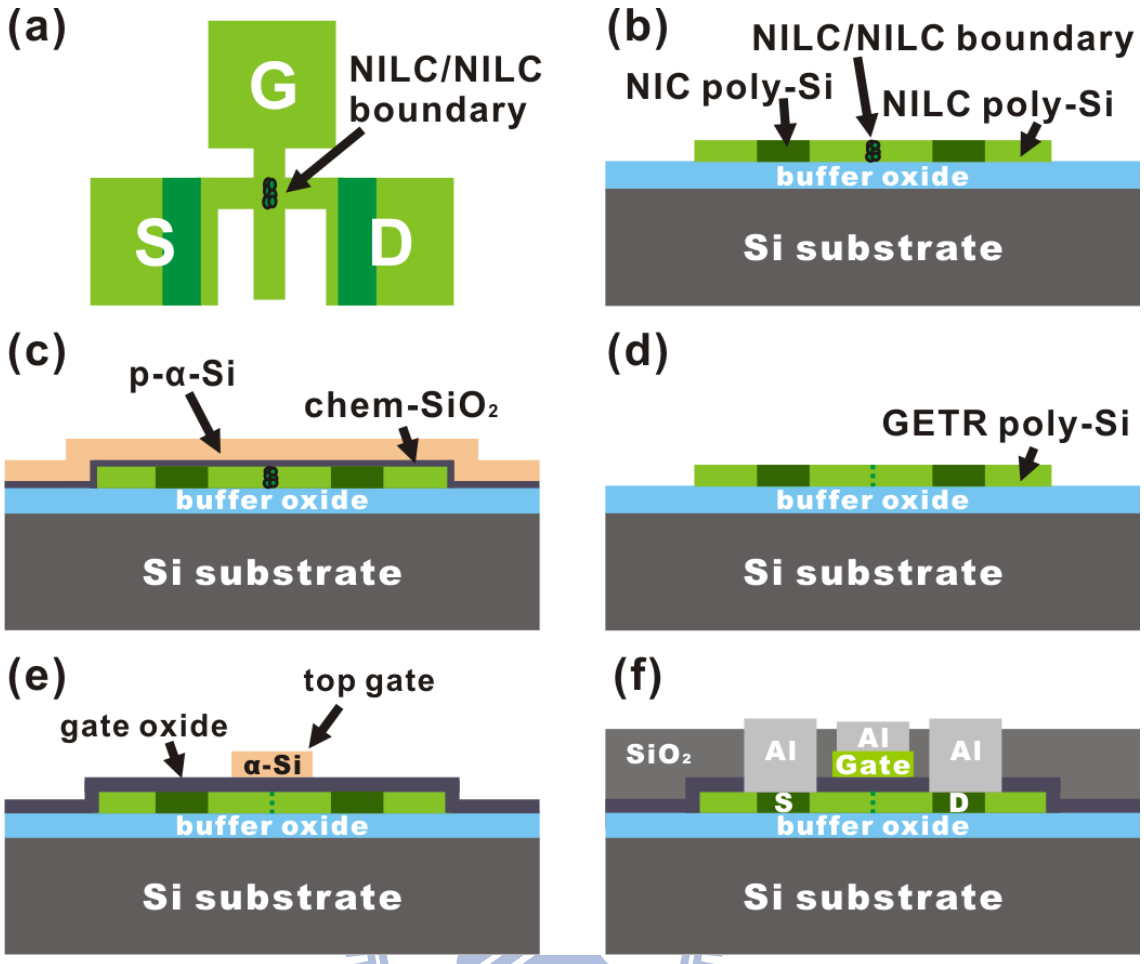


Figure 3-1 Schematic illustration of the TFTs device fabrication: (a) the top view of the fabricated device, (b) fabrication of NILC-Si, (c) capped with an etching stop layer (chem-SiO_2) and a gettering layer (p-α-Si), (d) removal of the gettering layer and chem-SiO_2 layer, (e) capped with a low-temperature oxide (LTO) as gate-oxide and a α-Si film as gate material, and (f) capped with a LTO as the isolation layer and fabrication of Al electrodes.

islands of poly-Si films were defined by reactive ion etching (RIE), as shown in Fig. 3-1b.

To fabricate GETR-Si film, NILC-Si film was dipped into a mixed solution of H_2SO_4 and H_2O_2 for 10 min to form a chem-SiO_2 layer on the top of NILC poly-Si [66, 67]. A 100-nm-thick α-Si film was then deposited onto the chem-SiO_2 layer using LPCVD at 550°C in N_2 ambient. Phosphorous ions were implanted into α-Si at a dose of 1×10^{16} cm^{-2}. The projection range of phosphorous ions was set at the middle of the α-Si film. The phosphorus-doped amorphous silicon (p-α-Si) served as a Ni-gettering layer, while the middle chem-SiO_2 film was used as an etching stop layer. The chem-SiO_2 film was about 5 nm thick. Even though the thickness of chem-SiO_2 was not uniform, this oxide film could be a good etching stop layer in the 5% tetra-methyl ammonium hydroxide (TMAH) etching solution. Moreover, chem-SiO_2 also serves as a diffusion interlayer during the Ni-gettering process. Ni atoms need to diffuse from the NILC-Si through the chem-SiO_2 into the Ni-gettering layer. Despite non-uniform thickness of SiO_2, the gettering efficiency remains unaffected. This is because the time required for Ni to pass through the chem-SiO_2 (about 5 nm thick) is much shorter than that for Ni to diffuse in the NILC-Si and p-α-Si gettering layers.

Samples undergoing Ni-gettering were then annealed at 550°C for 12 h in N_2 ambient for removing the unwanted Ni metal inside the NILC-Si, as illustrated in Fig. 3-1c. Following the annealing process, the phosphorus-doped amorphous silicon (p-α-Si) was removed using

5% TMAH, and the chem-SiO_2 was removed using a 1% HF solution, as shown in Fig. 3-1d. For the purpose of comparison, the NILC-Si (without Ni-gettering layers) film was also subjected to an extended heat treatment at 550°C for 12 h in N_2 ambient.

Then, a 100-nm-thick low-temperature oxide (LTO) was deposited by plasma-enhanced CVD (PECVD) as gate-oxide. A 100-nm-thick α-Si film was also deposited as gate material by LPCVD. After defining the gate, self-aligned 35-keV phosphorus ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate, as shown in Fig. 3-1e. They were then activated at 600°C for 12 h. A 500-nm-thick LTO was deposited by PECVD as the isolation layer. Contact holes were formed and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode, as present in Fig. 3-1f. The sintering process was finally performed at 400°C for 30 min in N_2 ambient. All device performances of poly-Si TFTs were measured with Keithley 4200.

3.3 Results and Discussion

3.3.1 Ni-Gettering Phenomenon

The length of the NILC poly-Si is about 79μm, as shown in Fig. 3-2a. The NILC-Si film is composed of needle-like NILC poly-Si grains, as displayed in Fig. 3-2b. After a 100-nm-thick α-Si film was deposited onto the chem-SiO_2 layer, disk-like poly-Si formed, as illustrated in Fig. 3-3a. Then a lot of p-α-Si transformed into NILC poly-Si during a Ni-gettering process, as

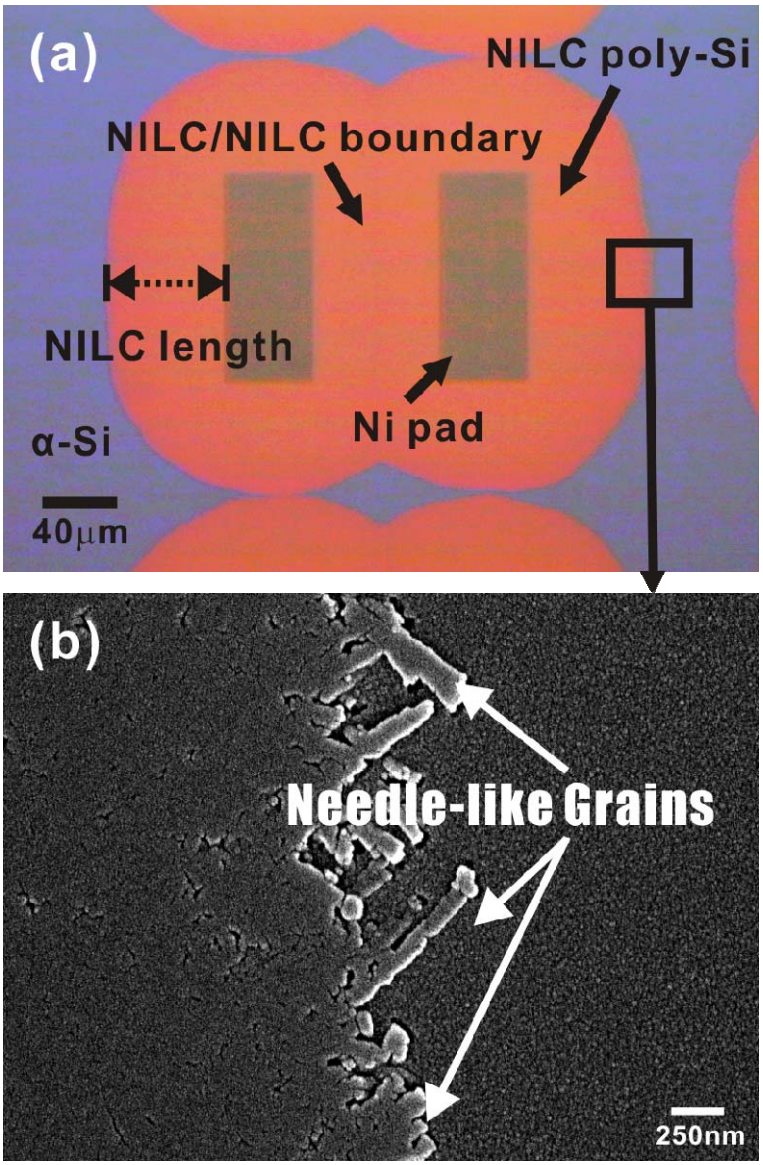


Figure 3-2 (a) OM image of the α-Si film after a NILC process carried out at 540°C for 24 h in N_2 ambient, and (b) SEM image of the NILC poly-Si grains treated with Secco-etching.

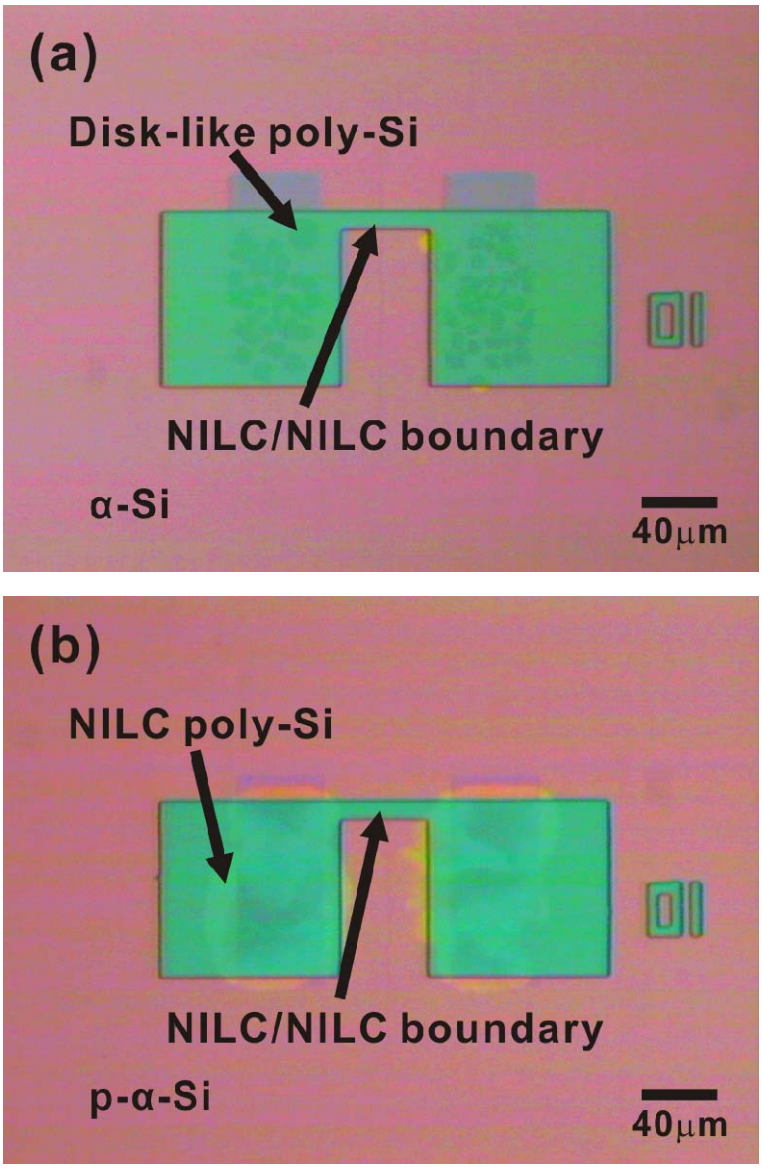


Figure 3-3 OM images of (a) a Ni-gettering layer, α-Si film, deposited on a chem-SiO_2 layer by LPCVD, and (b) the Ni-gettering phenomenon by a phosphorous-doped α-Si film at a dosage of 1×10^{16} cm^{-2}.

shown in Fig. 3-3b.

Figures 3-1 and 3-4a show the schematic illustrations of silicides observed at the boundaries where two NILC poly-Si fronts intersected (NILC/NILC boundary). As they were dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O = 4:1:50), numerous holes were formed at the NILC/NILC boundary, as shown in Fig. 3-4b. These holes are residues of the Ni silicides that have been etched away by the silicide-etching solution. They are quite sensitive to the reduction of Ni residues in the NILC-Si film, and are therefore ideal for elucidating the "Ni-gettering" phenomenon. After the Ni-gettering process, there were almost no silicide-etched holes found at the NILC/NILC boundaries of GETR-Si films, as shown in Fig. 3-4c, indicating that that lots of Ni atoms diffused through the chem-SiO_2 and reached p-α-Si layers during the gettering process.

3.3.2 Basic Electrical Characteristics of Poly-Si TFTs

Figure 3-5 displays the typical I_D -V_G transfer characteristics of the poly-Si TFTs for W/L = 10/10 μm measured at V_D = 5 V and V_D = 0.1 V, respectively. The measured and extracted key device parameters are summarized in Table 3-1. The threshold voltage (V_{TH}) is defined at a normalized drain current of I_D = (W/L) × 100 nA at V_D = 5 V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_D = 0.1 V. The minimum leakage current (I_{OFF_min}) is defined as the minimum current along the gate voltage at V_D = 5 V.

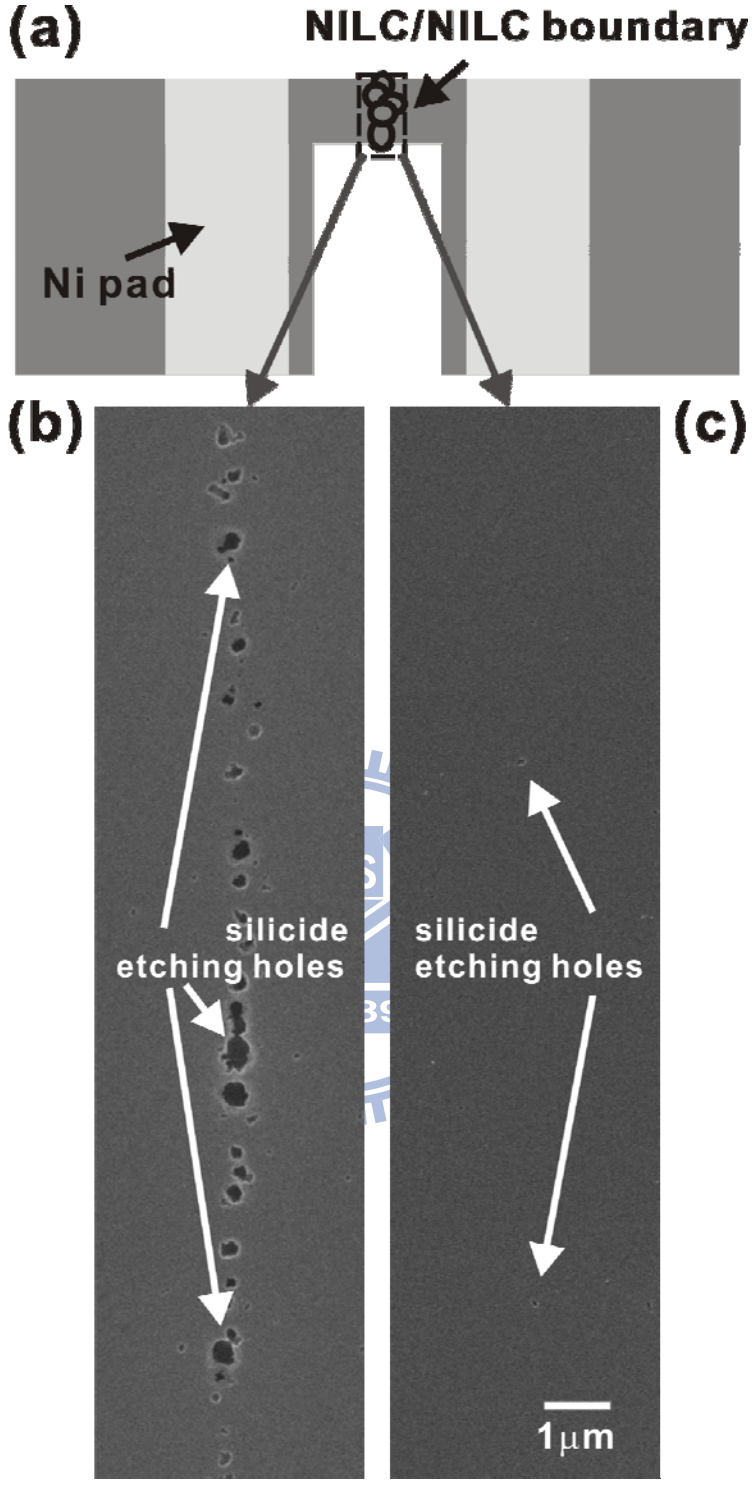


Figure 3-4 Schematic illustration of (a) silicide-etched holes at NILC/NILC boundaries, and SEM images of these holes in (b) the NILC-Si films and (c) the GETR-Si films. Samples were treated with the silicide-etching solution.

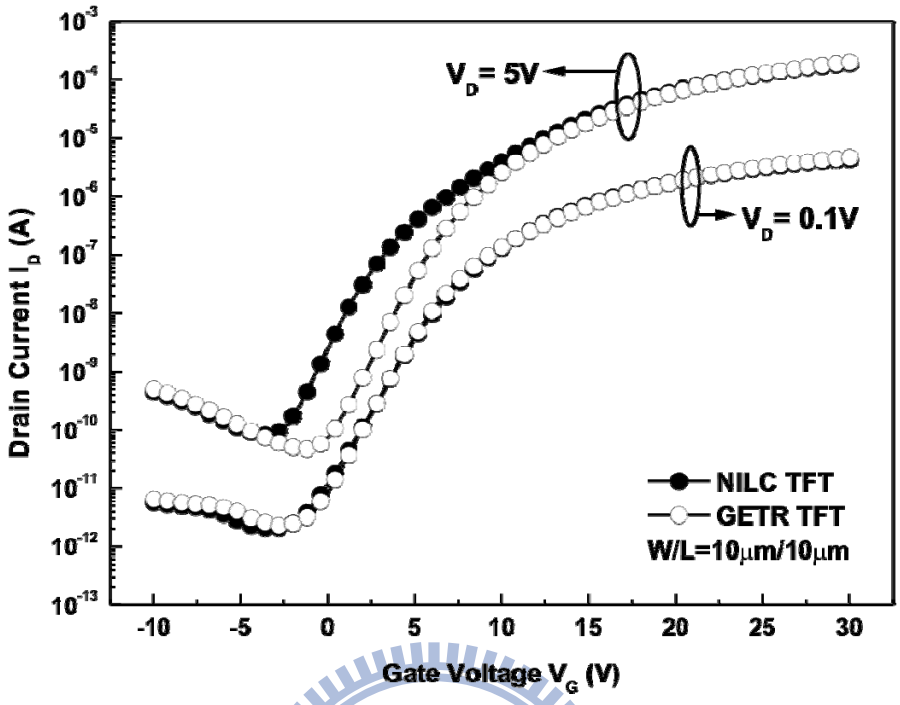


Figure 3-5 Typical I_D-V_G transfer curves of the NILC TFT and the GETR TFT measured at V_D = 5 V and V_D = 0.1 V, respectively.

Table 3-1 Device characteristics of the NILC TFTs and the GETR TFTs. Data were measured in ten devices, respectively.

W/L=10μm/10μm	NILC TFTs	GETR TFTs
Mobility (cm^2/V-s) @V_D=0.1V	75.7±6.3	88.4±4.8
Subthreshold slope (V/dec) @V_D=0.1V	1.51±0.18	1.58±0.12
Threshold voltage (V) @ V_D=5V	2.9±0.54	6.0±0.3
I_{ON}/I_{OFF} ratio (10^6) @ V_D=5V	2.27±0.60	3.88±0.33
I_{OFF_min}/W (pA/μm) @ V_D=5V	8.4±1.8	4.9±0.2

As shown in Table 3-1, GETR TFTs reveal lower I_{OFF_min}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC TFTs. These improvements are attributed to the reduction of the Ni concentration in the GETR-Si film. In NILC TFTs, Ni-related defects would degrade electrical performance because the trap states introduce dangling bonds and strain bonds. These defects trap traveling carriers and reduce the mobility of NILC TFTs. [93] Since there were less Ni residues in GETR TFTs than in NILC TFTs, the defects (caused by Ni residues) in the channel of GETR TFTs were fewer than that of NILC TFTs. As a result, the mobility of GETR TFTs is higher than that of NILC TFTs, as shown in Table 3-1.

Furthermore, NILC/NILC boundaries are the major source of off-state leakage current. [7] In n-type NILC poly-Si TFTs, Ni residues play the roles as deep-level traps, which promote thermionic emission-dominated leakage current. [94, 95] Hence, the leakage current can be easily induced at higher V_D. With the reduction of Ni concentration, the minimum leakage current (measured at V_D = 5 V) is reduced, and the on/off current ratio of GETR TFTs is thus increased. On the other hand, when V_D is low (0.1 V), the minimum leakage current of GETR TFTs do not change much, as shown in Fig. 3-5.

In addition, as shown in Table 3-1, the V_{TH} of the GETR TFT is 6.0 V, while that of NILC TFT is 2.9 V. This is because Ni residues could cause a high density of positive charge at the oxide/NILC poly-Si interface. [69, 96] Moreover, Ni residues promote thermionic emission

dominated leakage current at higher V_D. With the reduction of the Ni concentration, the leakage current is reduced and the negative shift of V_{TH} is suppressed at high V_D. Compared with that of NILC TFTs, as shown in Table 3-1, the V_{TH} of GETR TFTs have a positive shift at V_D = 5 V. On the other hand, when V_D is low (0.1V), the V_{TH} of GETR TFTs do not change much, as shown in Fig. 3-5.

These results are similar to the conclusions drawn by our previous study on Ni-gettering substrate fabricated by coating 100-nm-thick α-Si films on both sides of Si wafer. [69] To form the GETR-Si film, the NILC-Si film was bonded to the Ni-gettering substrate and then annealed at 550°C for an additional 12 h. Following the gettering process, the Ni-gettering substrate was separated by a razor blade. After the Ni-gettering process, it was also found that the number of silicide-etched holes at the NILC/NILC boundaries was greatly reduced, while the V_{TH} of the GETR TFTs was increased. The device transfer characteristics of GETR TFTs showed an 8.5-fold increase in on/off current ratio and a 34.1-fold decrease in minimum leakage current compared with those of NILC TFTs. However the mobility of GETR TFTs was less than that of NILC TFTs because the crystal quality of GETR-Si was poorer than that of NILC-Si. This is because, in our previous study on gettering substrate, the gettering of Ni in GETR-Si results in less complete crystallization.

In contrast, both the on/off current ratio and minimum leakage of GETR TFTs are

improved in this study though the improvements are not as good as those previously reported. [69] This might be because, in this study, only single 100-nm-thick p-α-Si film was used as the gettering layer, while, in the study on gettering substrate, two α-Si films and Si wafer were used as gettering layers. As a result, the gettering efficiency of gettering substrates was better than that of p-α-Si films.

Another difference from the previous study is the improvement in GETR-Si mobility. This might also be attributed to the lower gettering efficiency of p-α-Si films than that of gettering substrates. Compared with the results in the study on gettering substrate, the Ni concentration in this study was higher; and hence, the crystal quality of GETR-Si was also better.

The gettering efficiency of gettering substrates was better than that of p-α-Si films. Nevertheless, the gettering substrate method is not suitable for large area NILC poly-Si films. On the other hand, the gettering process of p-α-Si films is compatible with NILC TFT processes and is suitable for large area NILC poly-Si films. The gettering efficiency of p-α-Si films could be improved by increasing α-Si thickness. This is because, during the Ni-gettering process, when more Ni atoms diffused into the gettering layer, more α-Si would be transformed into poly-Si by the NILC mechanism. [66] Since the poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, the gettering efficiency increases with α-Si thickness.

3.3.3 Improved Uniformity of NILC Poly-Si TFTs by Ni-Gettering

The other important issue of poly-Si TFTs is their uniformity. Figure 3-6 and 3-7 show the cumulative distribution parameter $\triangle V_{TH}$, and I_{OFF_min} extracted from the I_D-V_G transfer curve. The shift of threshold voltage ($\triangle V_{TH}$) is defined as $V_{TH,1}$ - $V_{TH,2}$ where $V_{TH,1}$ and $V_{TH,2}$ denote V_G of drain current of I_D = (W/L) × 10 nA at V_D = 0.1 V and 5 V, respectively. Compared with NILC TFTs, GETR TFTs show a 2.5-V reduction in $\triangle V_{TH}$ and ~42% decrease in I_{OFF_min}. There is a greater variation of 21-24% in the relative scattering degree (standard deviation/average value) of both parameters in the case of NILC TFTs, but a smaller variation of only 4-8% in the case of GETR TFTs. The smaller relative scattering degree of the device performance for GETR TFTs may be attributed to the reduction of Ni.

3.4 Summary

An investigation of the effects of Ni-gettering layers (p-α-Si/chem-SiO_2 films) on electrical characteristics of NILC TFTs has led to the development of a simple and effective process for improving the electrical properties of large area NILC TFTs. It is found that the silicide-etched holes at NILC/NILC boundaries are almost eliminated after the Ni-gettering process. Compared with NILC TFTs, GETR TFTs reveal lower I_{OFF_min}, higher I_{ON}/I_{OFF} ratio, higher μ_{FE}, and better uniformity. Compared with NILC TFTs, GETR TFTs show a 2.5-V reduction in $\triangle V_{TH}$ and ~42% decrease in I_{OFF_min}. There is a greater variation of 21-24% in

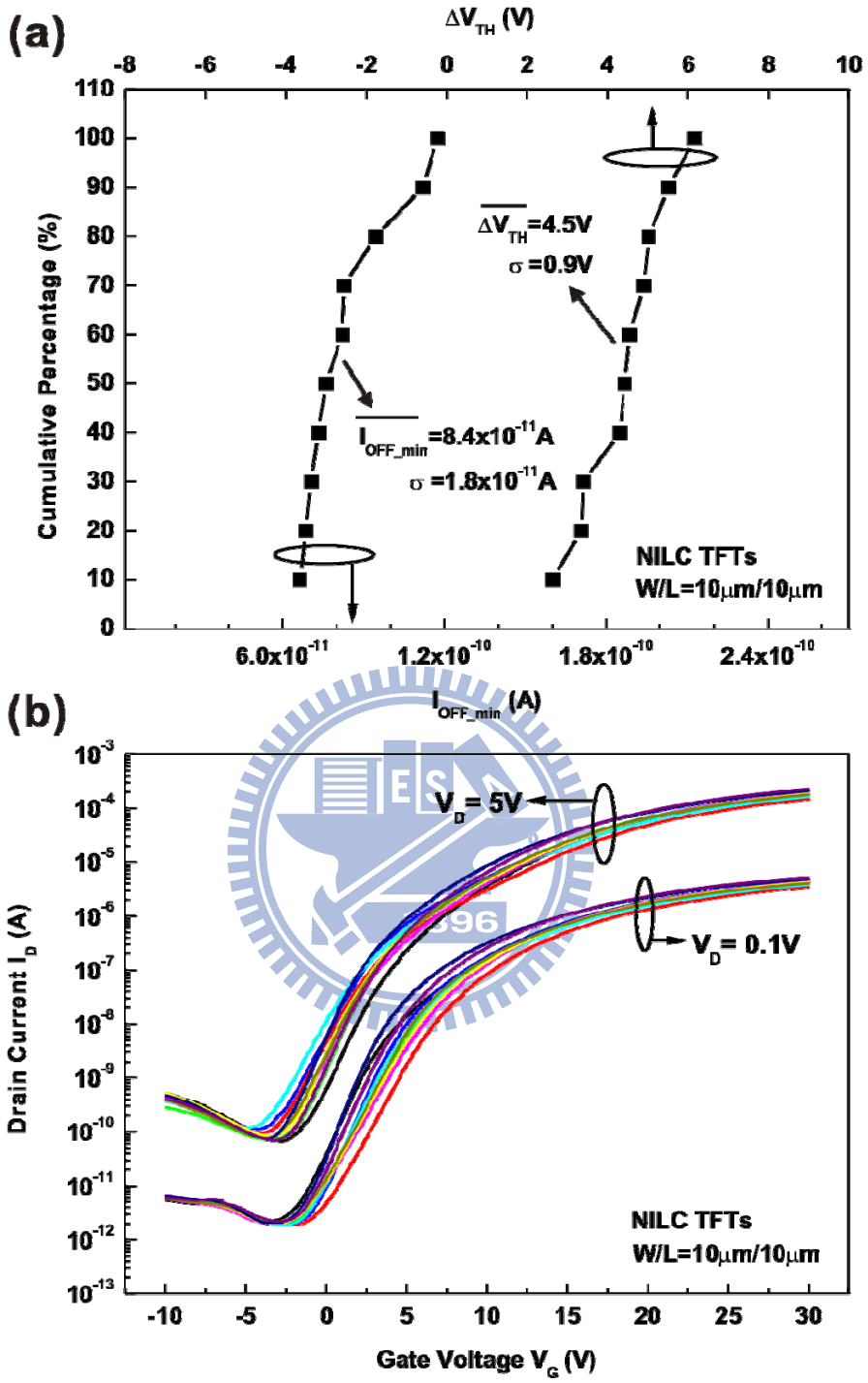


Figure 3-6 (a) $\triangle V_{TH}$ and I_{OFF_min} were measured in ten NILC TFTs to investigate the device-to-device variation, and (b) the I_D-V_G transfer curves of ten NILC TFTs measured at V_D = 5 V and V_D = 0.1 V, respectively.

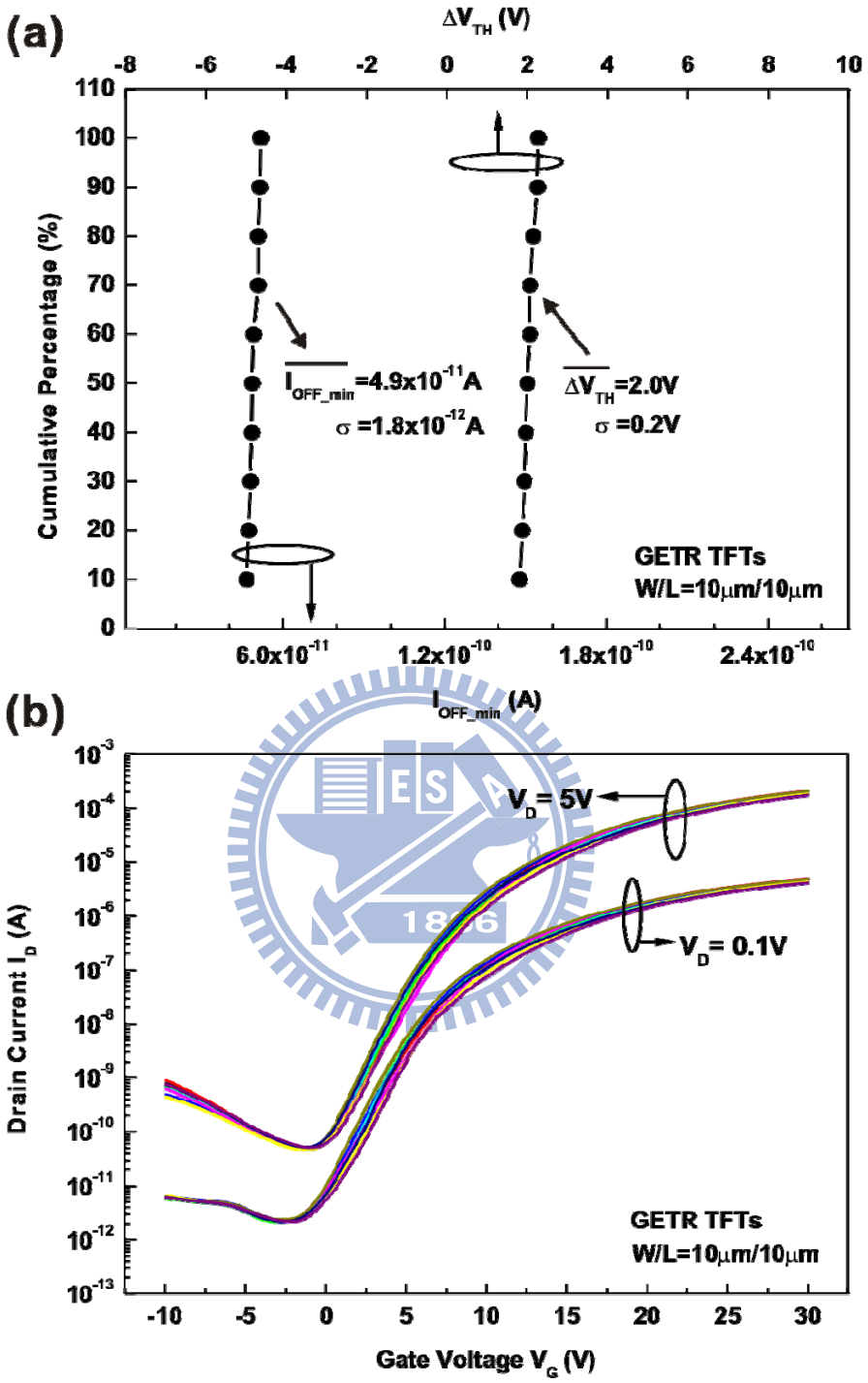


Figure 3-7 (a) $\triangle V_{TH}$ and I_{OFF_min} were measured in ten GETR TFTs to investigate the device-to-device variation, and (b) the I_D-V_G transfer curves of ten GETR TFTs measured at V_D = 5 V and V_D = 0.1 V, respectively.

the relative scattering degree of $\triangle V_{TH}$, and I_{OFF_min} in the case of NILC TFTs, but a smaller variation of only 4-8% in the case of GETR TFTs. These improvements are all attributed to the reduction of Ni concentration in the GETR-Si films.

Chapter 4 Improved Performance and Uniformity of NILC Poly-Si Nanowires TFTs through Ni-Gettering

4.1 Introduction

Recently, high performance poly-Si nanowires (NWs) TFTs have been fabricated by nickel-metal induced lateral crystallization (NILC). [86, 97] Since NILC grain could be formed parallel to the channel direction, it becomes feasible to form Si NWs with nearly monocrystalline structures. [98] Unfortunately, poly-Si/oxide interfaces and poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, thus increasing the leakage current and shifting the threshold voltage. [12-16] Therefore, Ni contamination inside the NILC poly-Si should be reduced to improve the device performance, especially for side-gated TFTs with NILC poly-Si NW channels. Ni-related defects trapped at top surfaces could be removed simply by chemical etching, including HCl and H_2SO_4 solutions but doesn't the bottom poly-Si/gate oxide interface. For high channel controllability of side-gated NWs TFTs, this could be an important issue.

In previous studies, we have proposed several methods to reduce Ni concentration

inside NILC poly-Si, including bonding with α-Si-coated Si wafer [69], and direct deposition of the gettering layers on NILC poly-Si [65-67]. In this chapter, phosphorous-doped α-Si/chem-SiO_2 films are used to reduce Ni residues within NILC NWs. It was found that the performance and the uniformity of side-gated NILC NWs TFTs were improved after a Ni-gettering process. The Ni-related defects inside poly-Si NW channels and trapped at poly-Si/gate oxide interfaces were reduced.

4.2 Device Fabrication

Three kinds of poly-Si NWs are investigated in this study. One is "SPC" NWs fabricated by solid phase crystallization (SPC), and the others are "NILC" and "GETR" NWs fabricated by NILC method without and with a Ni-gettering process, respectively.

An approach for making NILC NW channels similar to the ref. [86, 87] is followed. The detailed procedures are basically identical to those described in the ref. [87]. First, a gate (n^+ poly-Si) was formed on a Si wafer capped with a 500-nm-thick wet oxide film. Next a 40-nm-thick TEOS oxide was deposited by low-pressure CVD (LPCVD) as gate-oxide, followed by the deposition of 100-nm-thick LPCVD α-Si films, as shown in Fig. 4-1a. Basic NILC process was then carried out at 540^{o}C for 24 h in N_2 ambient. In this study, the major difference compared with the ref. [86] is the NILC process performed before the NW channels are defined, as illustrated in Fig 4-1b. Before the NILC process, 5-nm-thick Ni lines

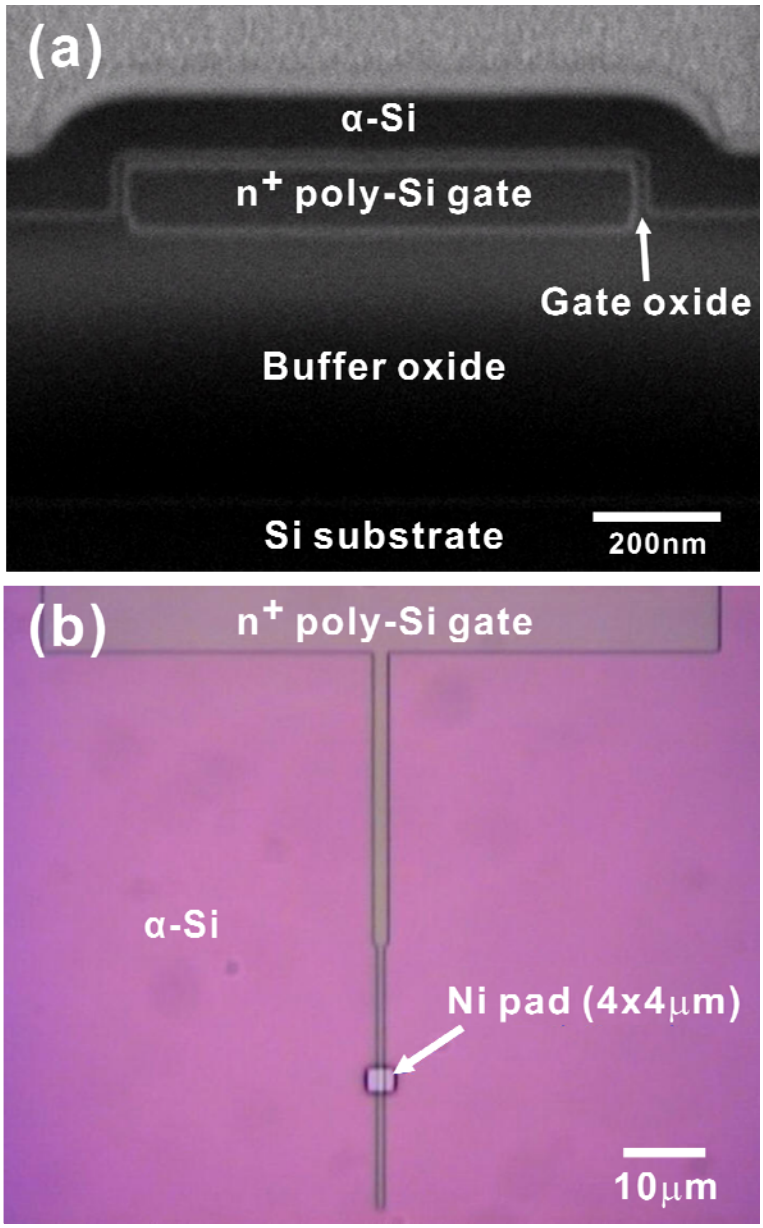


Figure 4-1 (a) Cross-sectional SEM image of a 100-nm-thick LPCVD α-Si film capped on a 40-nm-thick TEOS oxide, and (b) OM image of a 4x4 μm Ni pad on a α-Si film before basic NILC process.

were selectively deposited on the α-Si films using lift-off method [67]. NILC length is about 17 μm after lateral crystallization, as shown in Fig. 4-2a. The unreacted Ni was removed by a mixed solution of H_2SO_4 and H_2O_2. NILC poly-Si films were then dipped into 1% diluted hydrogen fluoride (DHF) solution to remove top annealing oxide, as illustrated in Fig. 4-2b. The top and side views of the device structure are shown in Fig. 4-3a and b.

As for GETR films, an additional Ni-gettering process was carried out to reduce the Ni impurities in the NILC films [67]. The Ni-gettering structure (phosphorous-doped α-Si/chem-SiO_2) is shown in Fig. 4-2c. After gettering at 550°C for 12 h in N_2 ambient, phosphorous-doped α-Si and chem-SiO_2 layers were removed using 5% tetra-methyl ammonium hydroxide (TMAH) and 1% DHF solution, respectively. As for SPC films, sample was crystallized by SPC at 600°C for 24 h in N_2 ambient.

For comparison, NILC and SPC films were also subjected to an extended heat treatment as Ni-gettering condition. Subsequently, source/drain (S/D) implant was performed. The implant energy was kept low as 15 keV so that most phosphorous ions were located near the top surface of the poly-Si surface. After S/D photoresist formation, these three poly-Si films were subjected to an anisotropic etching to form poly-Si sidewall spacers in a self-aligned manner, as illustrated in Fig. 4-4a and b. The activation was carried out at 600°C for 12 h in N_2 ambient. A 350-nm-thick TEOS oxide film was then deposited by LPCVD as the isolation

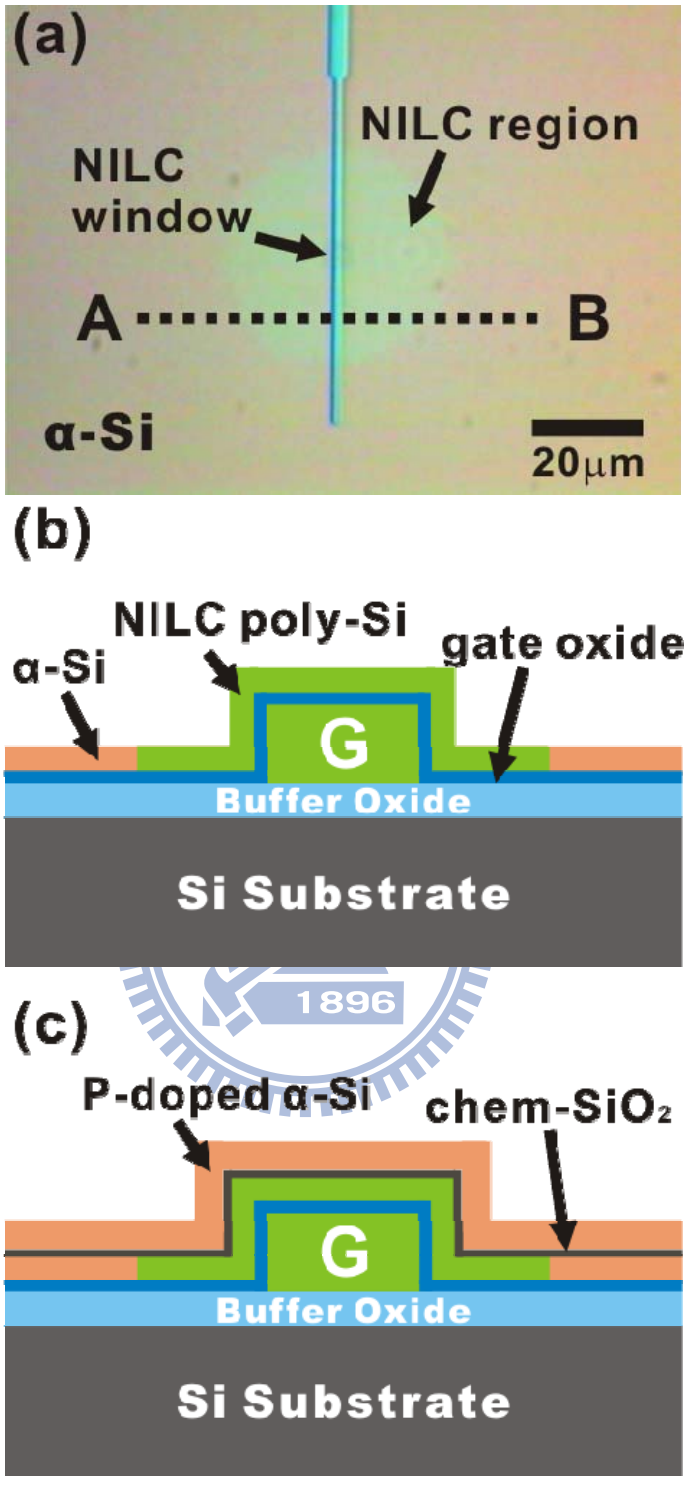


Figure 4-2 (a) OM image of NILC poly-Si after annealing at 540°C for 24 h in N_2 ambient, (b) the cross-sectional view along the dashed line A to B in Fig. 4-2a, and (c) the Ni-gettering structure.

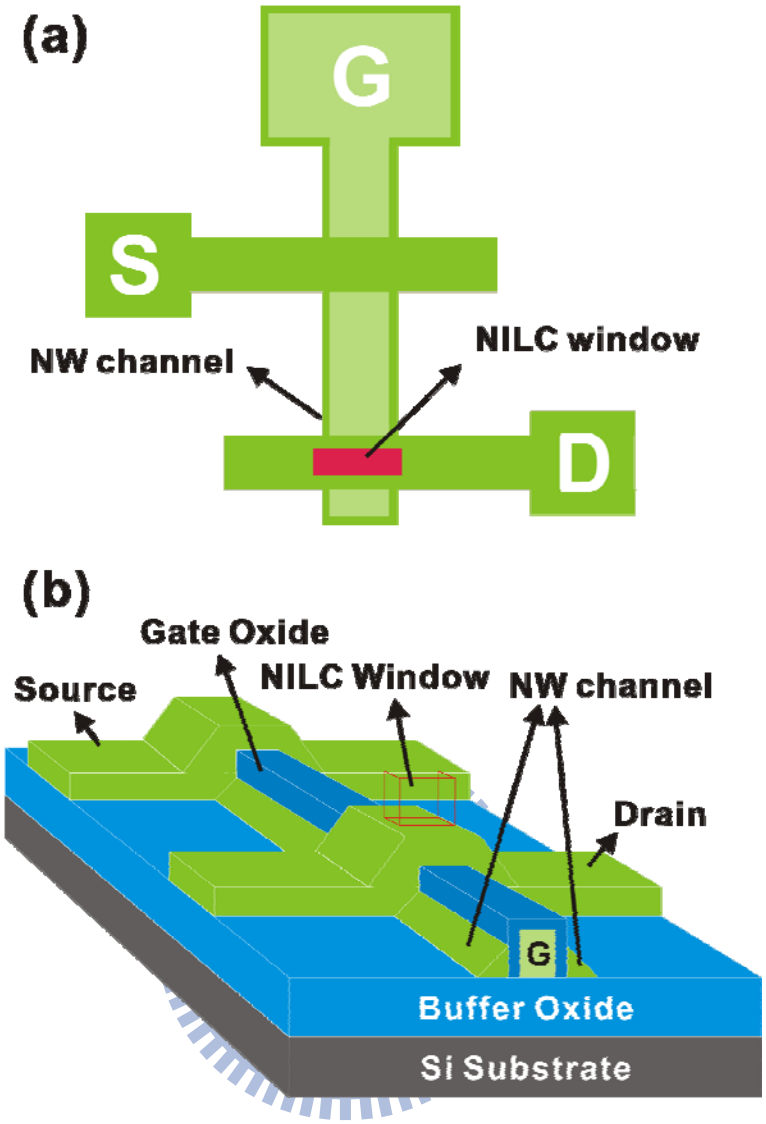


Figure 4-3 (a) Top view of the proposed NILC poly-Si NWs TFT structure, and (b) the 3-D schematic of poly-Si NWs TFTs.

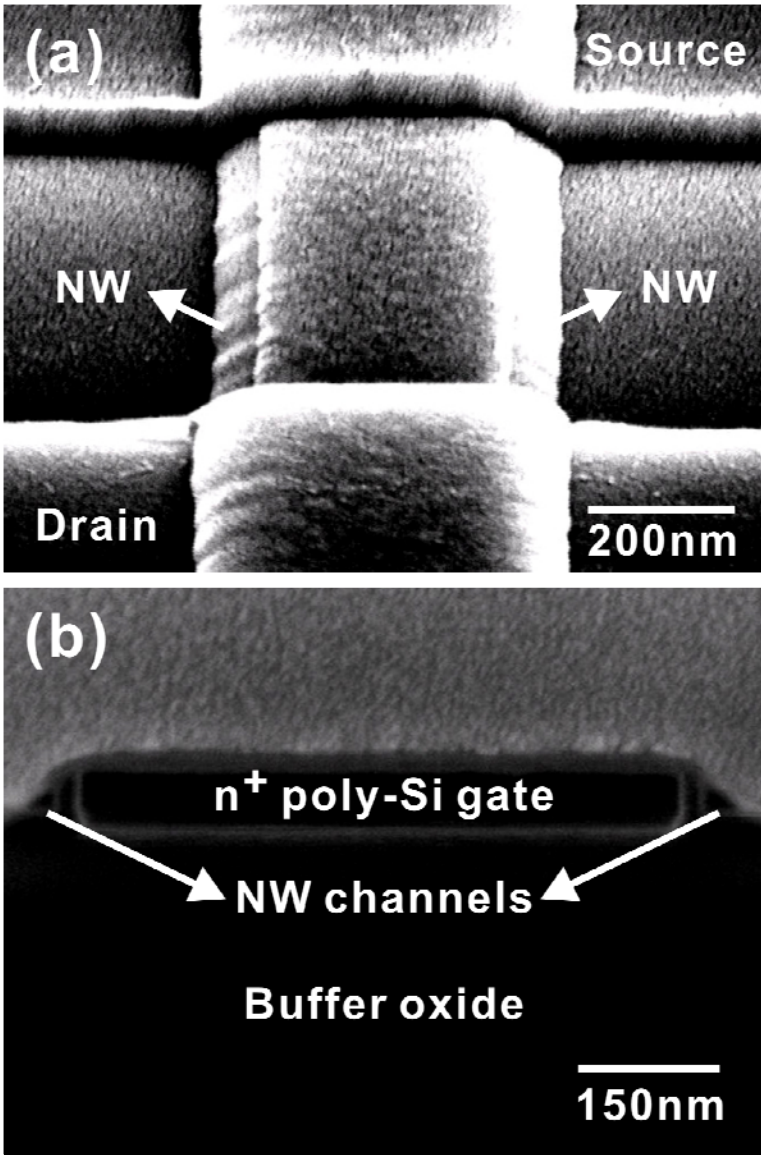


Figure 4-4 SEM images of (a) top view and (b) side view of the source/drain (S/D) formation with a couple of poly-Si NW channels after an anisotropic etching.

layer. Next contact holes were formed and a 500-nm-thick AlSi(1%)Cu(0.5%) layer was then deposited by physical vapor deposition (PVD) and patterned as the electrode. The sintering process was finally performed at 400°C for 30 min in N_2 ambient. All device performances of poly-Si NWs TFTs were measured with Keithley 4200.

4.3 Results and Discussion

4.3.1 Characterization of Fabricated Poly-Si NWs

Figure 4-5 shows the cross-sectional transmission electron microscopy (TEM) images of NILC NWs TFT. Both the vertical width (W_{NW}) and the horizontal sidewall thickness (T_{NW}) are about 70 nm. The gate oxide is 40 nm thick, as illustrated in Fig. 4-5b. The cross-section of fabricated poly-Si NWs is similar to triangular shape by an anisotropic etching. The width of poly-Si gate is 0.8 μm. H. C. Lin et al [88] reported that the off-state leakage current is actually proportional to the gate width (or the area of the top gate-to drain overlap region). Gate induced drain leakage (GIDL) is the most likely cause for the anomalously high off-state current [99]. The gate width is therefore fixed in 0.8 μm in the measure of the electrical characteristics.

4.3.2 Device Performances of Poly-Si NWs TFTs

The TFT devices with a couple of NW channels have a nominal channel (L) of 0.8 μm and an effective channel width (W) of 140 nm ($2 \times W_{NW}$). Typical I_D-V_G transfer characteristics of

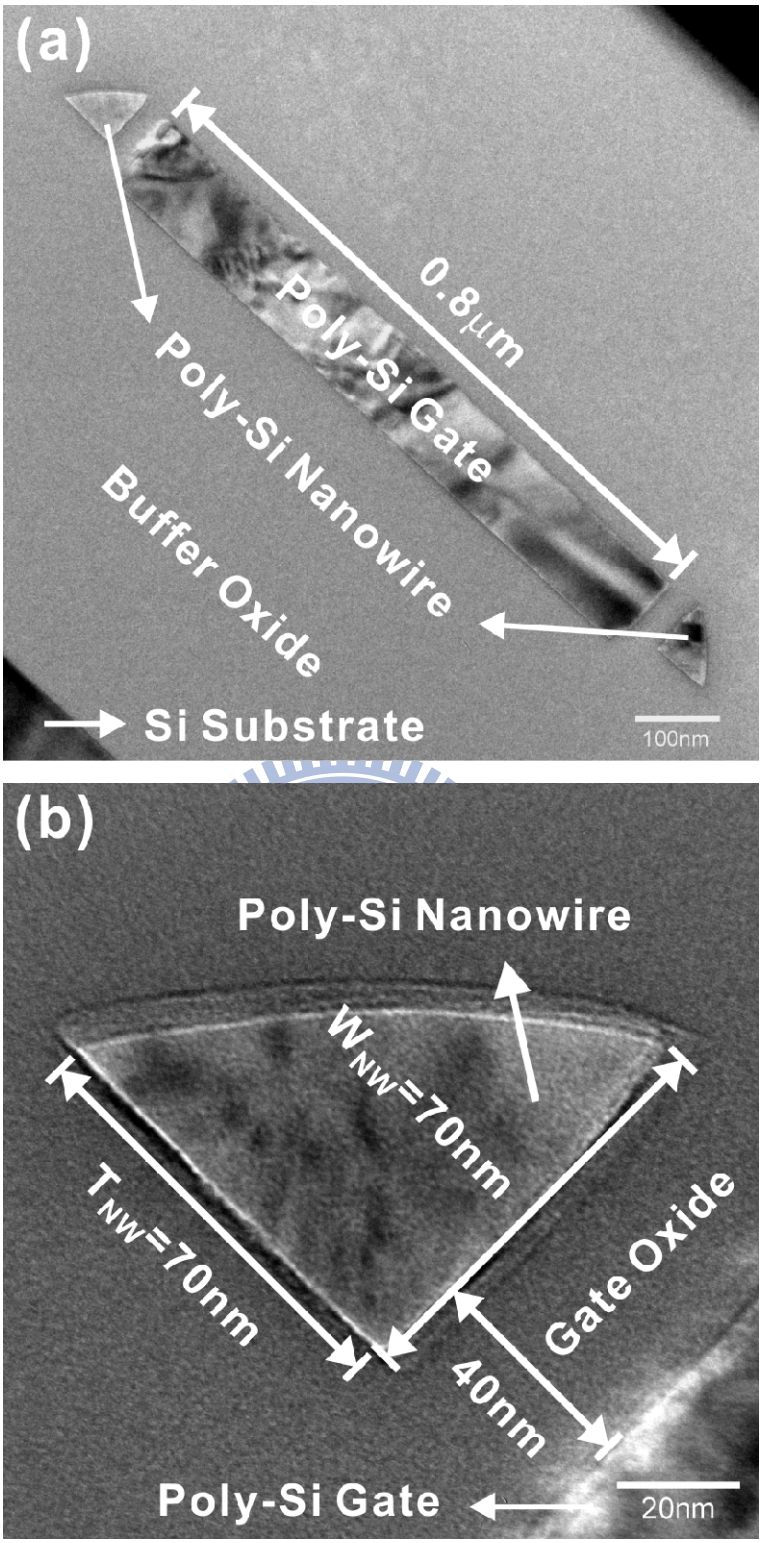


Figure 4-5 (a) Cross-sectional TEM image of the NILC NWs TFT with a couple of poly-Si NW channels, and (b) the high magnification of poly-Si NWs in Fig. 4-3a.

NWs TFTs at V_D = 0.5 and 3 V are compared in Fig. 4-6. The measured and extracted key device parameters are summarized in Table 4-1. The threshold voltage (V_{TH}) is defined at a normalized drain current of I_D = (W/L) × 100 nA at V_D = 0.5 V. The subthreshold swing (S.S.) is extracted at V_D = 0.5 V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_D = 0.5 V. The leakage current (I_{OFF}) is defined as the minimum drain current along the gate voltage at V_D = 3 V.

As shown in Table 4-1, GETR and NILC NWs TFTs reveal higher μ_{FE}, better subthreshold swing (S.S.), and higher I_{ON}/I_{OFF} ratio compared with SPC NWs TFTs. This is because the NILC grain is large, needlelike, and parallel to the channel [86]. Besides, Table 4-1 also indicates the performance of NILC TFTs is improved after a Ni-gettering process. GETR TFTs have lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC TFTs. This improvement indicates the trap state density is effectively reduced using phosphorous-doped α-Si gettering processes.

Figure 4-7 shows the trap state density of the TFTs extracted using Levinson and Proano's method [100], which can estimate the N_{trap} from the slop of the linear segment of $\ln(I_D/V_G\text{-}V_{FB})$ versus $1/(V_G\text{-}V_{FB})^2$ at low V_D and high V_G, where V_{FB} is defined as the gate voltage that yields the minimum drain current at V_D=0.1V. The trap density of GETR NWs TFTs is 2.52×10^{12} cm^{-2}, which is less than that of NILC NWs TFTs (3.95×10^{12} cm^{-2}). The reduction

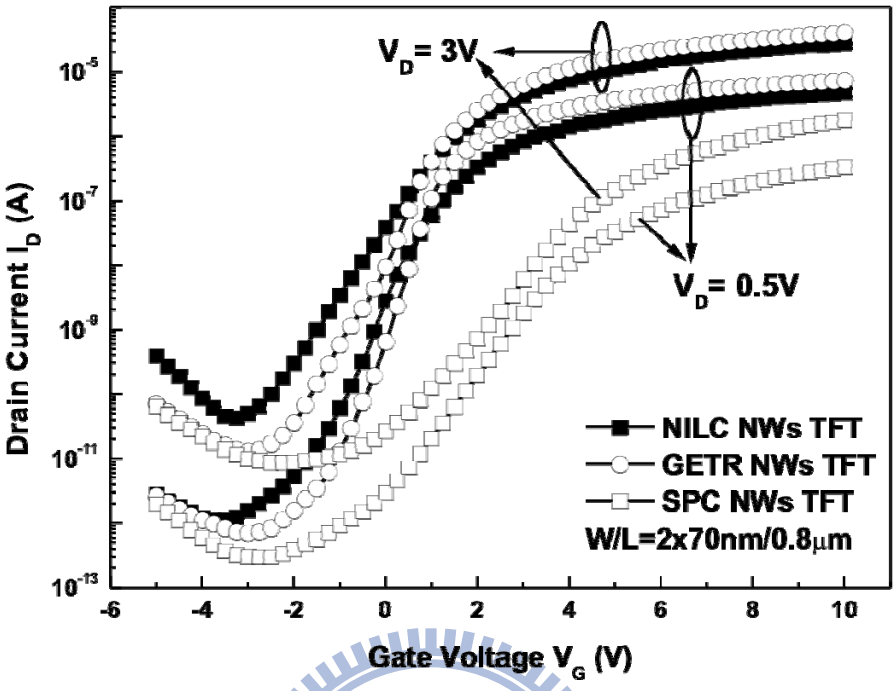


Figure 4-6 Comparison of transfer characteristics among SPC, NILC, and GETR NWs TFTs.

Table 4-1 Device characteristics of NILC, GETR and SPC NWs TFTs. Data were measured in ten devices, respectively.

Parameters (W/L=2x70nm/0.8μm)	NILC NWs TFTs	GETR NWs TFTs	SPC NWs TFTs
μ_{FE} (cm^2/V-s) @V_D=0.5V	117.32±17.75	140.73±38.21	24.50±4.14
S.S. (mV/dec) @V_D=0.5V	395±66	418±63	694±76
V_{TH} (V) @ V_D=0.5V	0.19±0.40	0.35±0.22	4.12±0.21
I_{ON}/I_{OFF} ratio (10^6) @ V_D=3V	1.4±1.2	3.2±1.0	0.4±0.1
I_{OFF} (pA) @ V_D=3V	81.86±95.71	13.03±5.41	6.37±2.50

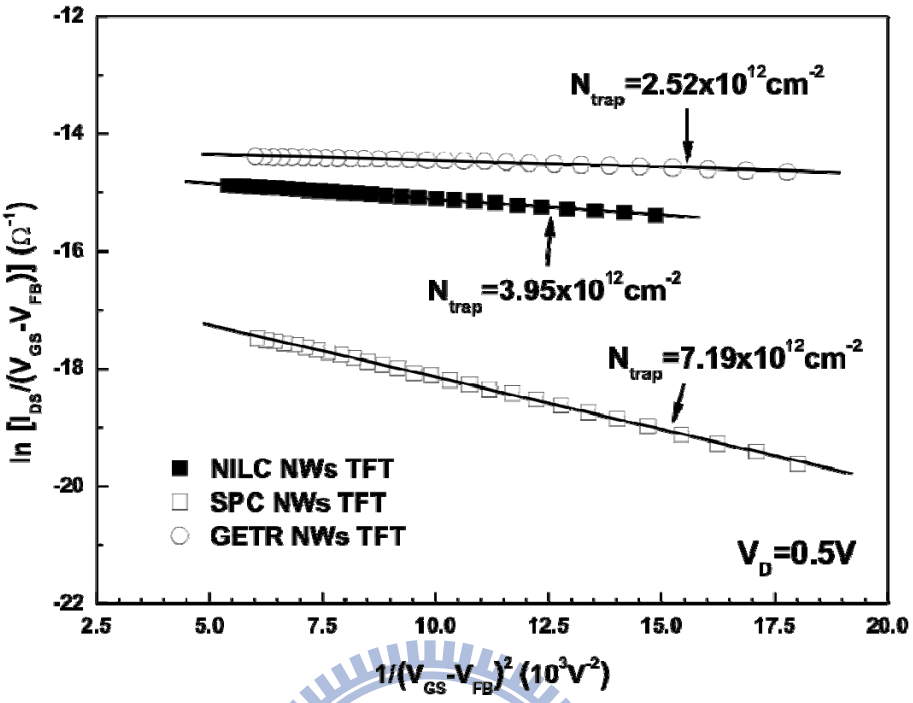


Figure 4-7 Plot of $\ln(I_D/V_G-V_{FB})$ versus $1/(V_G-V_{FB})^2$ and the extracted trap state density of SPC, NILC and GETR NWs TFTs. I_D was measured at V_D = 0.5 V.

in N_{trap} values implies that those Ni-related defects have been effectively reduced using phosphorous-doped α-Si/chem-SiO_2 -gettering. [69, 93-95]

Besides, as shown in Table 4-1, the V_{TH} of the NILC TFT is 0.19 V, which is less than that of GETR TFT (0.35 V). This is because Ni residues could cause a high density of positive charge at the oxide/NILC poly-Si interface [96]. The negative shift of V_{TH} of NILC TFT is due to the presence of these positive charges and nickel-related donor-like defects.

4.3.3 Uniformity Improved in Poly-Si NWs TFTs by Ni-Gettering

The other important issue of poly-Si NWs TFTs is their uniformity. Figure 4-8, 4-9 and 4-10 show the threshold voltage and the leakage current of ten NWs TFTs measured in each case to study device-to-device variation. It is found that the uniformity of SPC TFTs is better than that of GETR and NILC TFTs. There is a small variation of ~5% in the relative scattering degree (standard deviation/average value) of V_{TH} in the case of SPC NWs TFTs. This is because Ni and $NiSi_2$ precipitates are randomly trapped at poly-Si/oxide interfaces and poly-Si grain boundaries. [12-16, 69] Figure 4-9 and 4-10 also indicate the uniformity of GETR NWs TFTs is better than that of NILC NWs TFTs. Compared with NILC NWs TFTs, GETR NWs TFTs show a ~81% decrease in I_{OFF}. Moreover, there is a ~3-fold greater variation in the relative scattering degree of both parameters in the case of NILC NWs TFTs compared with GETR NWs TFTs. This is due to the reduction of the Ni concentration inside NILC poly-Si NWs

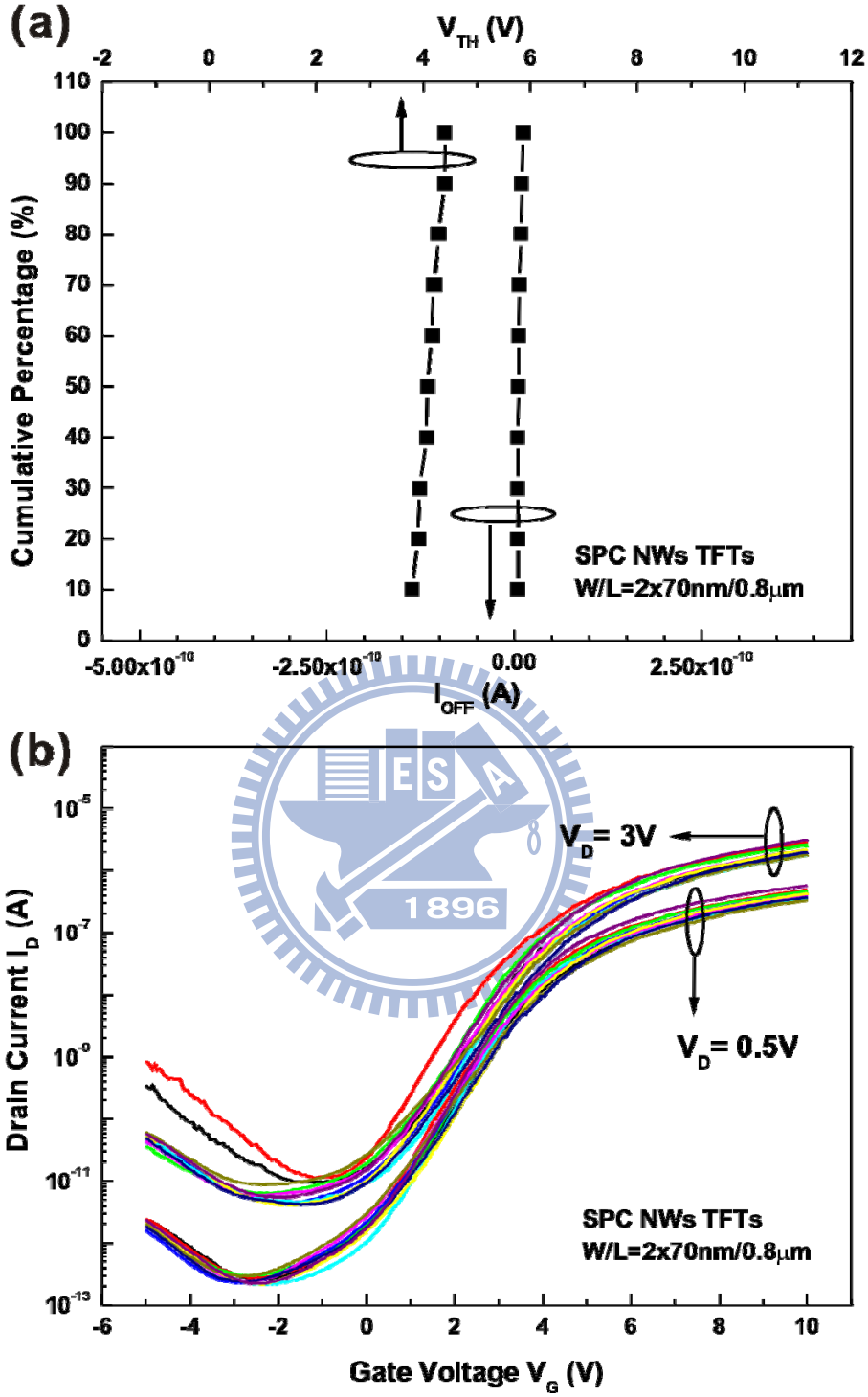


Figure 4-8 (a) V_{TH} and I_{OFF} were measured in ten SPC NWs TFTs to investigate the device-to-device variation, and typical I_D-V_G transfer curves of ten (b) SPC NWs TFTs measured at V_D = 3 V and V_D = 0.5 V, respectively.

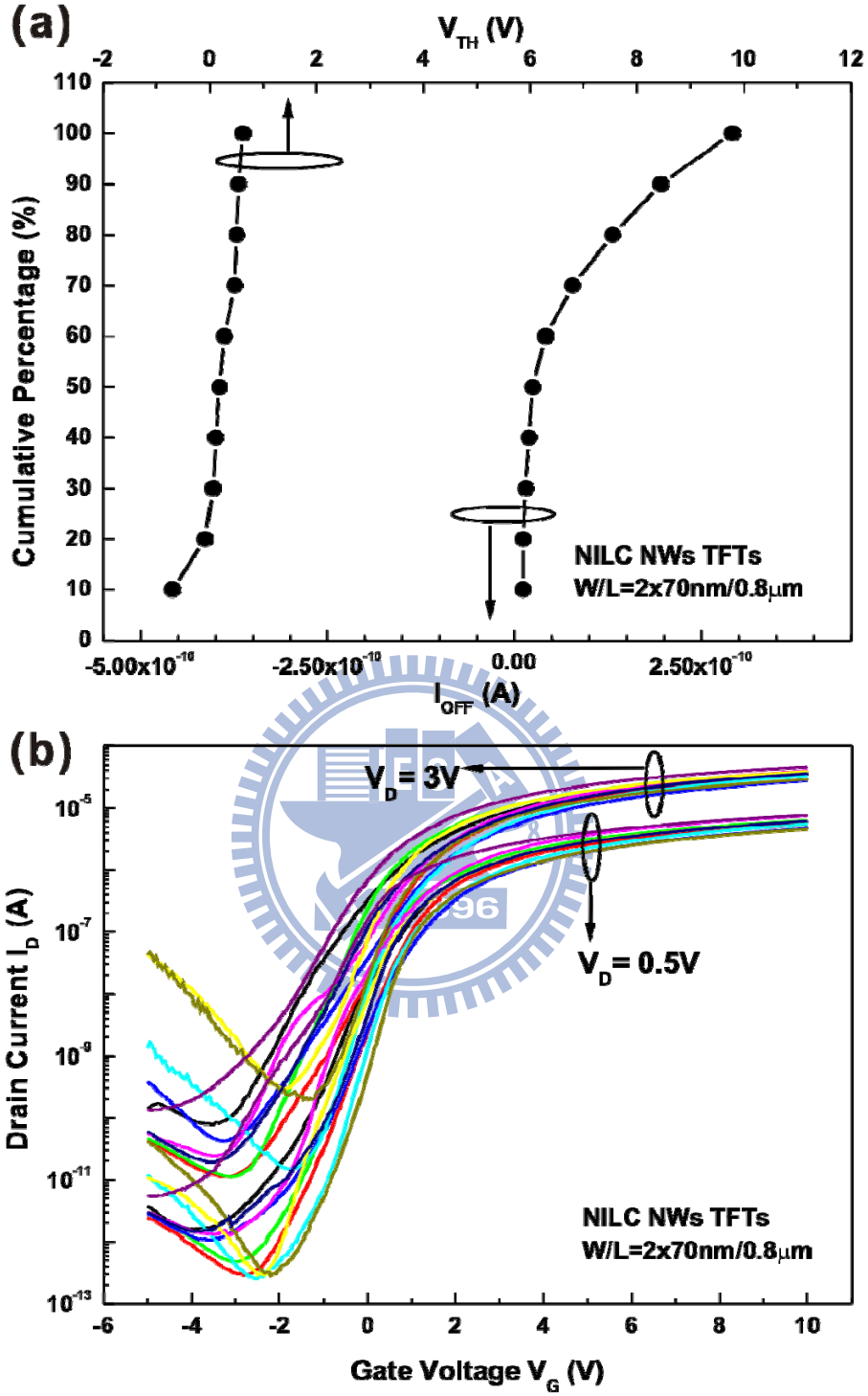


Figure 4-9 (a) V_{TH} and I_{OFF} were measured in ten NILC NWs TFTs to investigate the device-to-device variation, and typical I_D-V_G transfer curves of ten (b) NILC NWs TFTs measured at V_D = 3 V and V_D = 0.5 V, respectively.

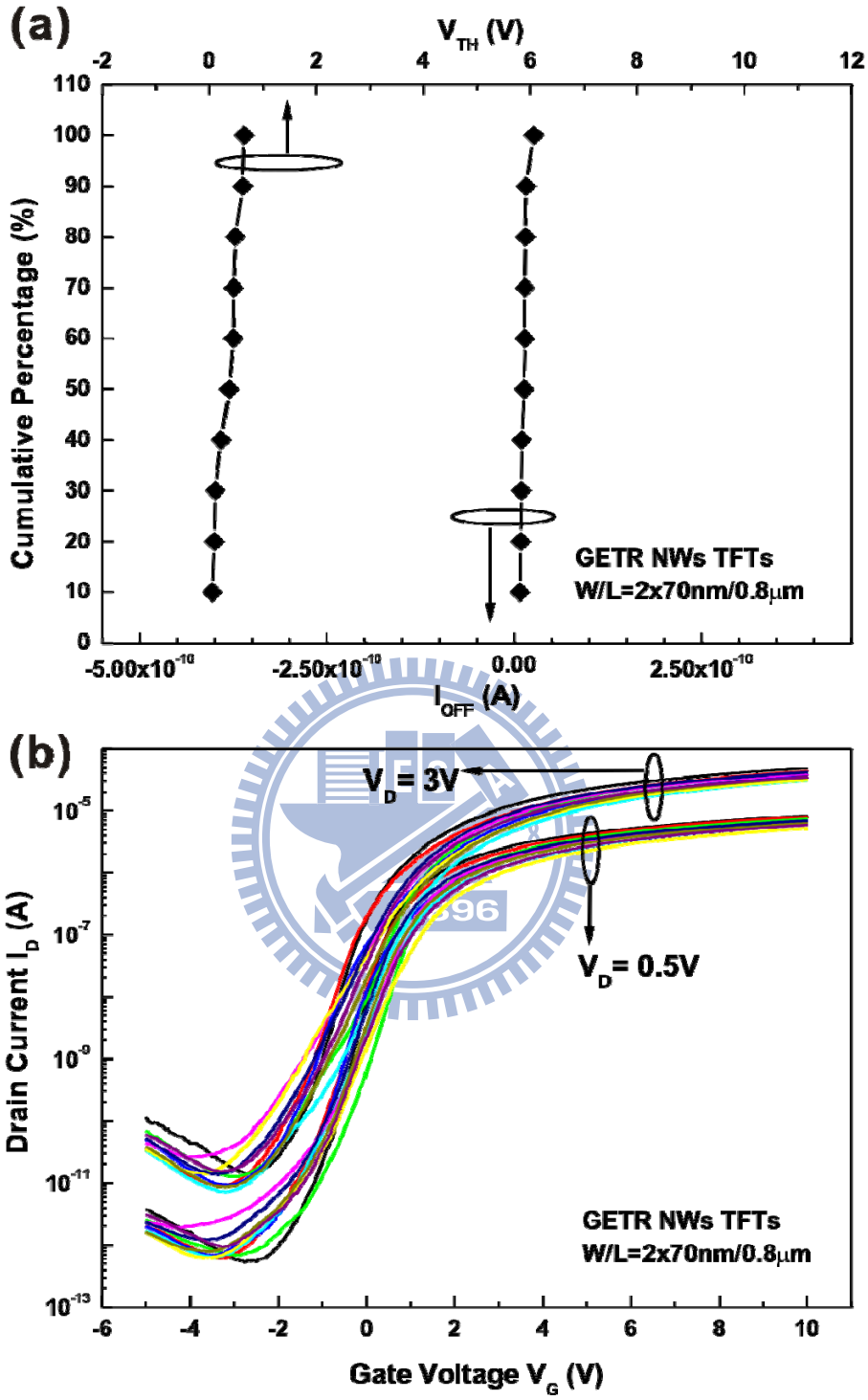


Figure 4-10 (a) V_{TH} and I_{OFF} were measured in ten NILC NWs TFTs to investigate the device-to-device variation, and typical I_D-V_G transfer curves of ten (b) NILC NWs TFTs measured at V_D = 3 V and V_D = 0.5 V, respectively.

channel, trapped at poly-Si/oxide interfaces and poly-Si grain boundaries. In a brief, the uniformity of NILC NWs TFTs is improved through Ni-gettering.

4.4 Summary

In this study, high performance NILC NWs poly-Si side-gated TFTs with a couple of 70-nm NW channels are fabricated, and then improved by a Ni-gettering process. The phosphorous-doped α-Si/chem-SiO_2 films are employed as Ni-gettering layers to reduce Ni residues within NILC poly-Si films. After a Ni-gettering process, the performance of NILC NWs TFTs is improved. GETR NWs TFTs have lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC NWs TFTs. The uniformity of GETR NWs TFTs is better than that of NILC NWs TFTs. This is because Ni and $NiSi_2$ precipitates are randomly trapped at poly-Si/gate oxide interfaces and poly-Si grain boundaries. With the gettering of the Ni residues, the uniformity of NILC NWs TFTs is improved in terms of the threshold voltage and the leakage current. Furthermore, the reduction in N_{trap} of GETR NWs TFTs implies that those Ni-related defects have been effectively reduced.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

In this study, several techniques are utilized for the fabrication of high-performance low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), including Ni-gettering methods and Si nanowire (NW) channels fabrication. Low-temperature poly-Si is fabricated by nickel-metal induced lateral crystallization (NILC). To improve the performances of NILC poly-Si thin-film and NW channel transistors , especially on the leakage current and the threshold voltage, the gettering of nickel impurities within NILC poly-Si is carried out.

In chapter 2, two kinds of films are employed to investigate the effect of phosphorus dopant on the gettering efficiency of α-Si. From the results, it has been found that the gettering efficiency of α-Si is indeed improved by the doping of phosphorous ions at a dose of 1×10^{16} cm^{-2}. Increasing the doping concentration of phosphorous ions could improve the gettering efficiency of α-Si. Improved gettering efficiency of α-Si by the phosphorous dopant may be due to the solubility enhancement of Ni impurities. A ~5-nm-thick porous chem-SiO_2 layer could reduce the thermal budget of the Ni-gettering process compared with

the previous PECVD-SiN_x study. Moreover, the results show that ~5-nm-thick chem-SiO_2 layer can protect NILC poly-Si surfaces during wet etching by 5% TMAH solution.

It is also found that the gettering layer is transformed into poly-Si by the NILC mechanism. The NILC fraction in the gettering layer increases with an increase in annealing time and temperature, as expected from the kinetic nature of the diffusion process. The concentration gradient acts as a driving force for transport of Ni atoms from the NILC poly-Si films through the chem-SiO_2 layers to the gettering layers.

An investigation of the effects of Ni-gettering layers (p-α-Si/chem-SiO_2 films) on electrical characteristics of NILC TFTs has led to the development of a simple and effective process for improving the electrical properties of large area NILC TFTs. Compared with NILC TFTs, GETR TFTs reveal lower I_{OFF_min}, higher I_{ON}/I_{OFF} ratio, higher μ_{FE}, and better uniformity. These improvements are all attributed to the reduction of Ni concentration in the GETR-Si films.

In chapter 4, high performance NILC NWs poly-Si side-gated TFTs with a couple of 70-nm NW channels are fabricated, and then improved by a Ni-gettering process. After a Ni-gettering process, the performance of NILC NWs TFTs is improved. GETR NWs TFTs have lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC NWs TFTs. The uniformity of GETR NWs TFTs is better than that of NILC NWs TFTs. This is because Ni and

$NiSi_2$ precipitates are randomly trapped at poly-Si/gate oxide interfaces and poly-Si grain boundaries. With the gettering of the Ni residues, the uniformity of NILC NWs TFTs is improved in terms of the threshold voltage and the leakage current.

5.2 Future Work

There are some interesting topics that are valuable for the further future research on LTPS NILC TFTs:

(1) Nanocrystalline p-n junction diodes have been fabricated by the NILC process for the solar cell devices [101]. However the preparation of the p-n junction diode is limited. This is because Ni metal diffuses downward during crystallization and more Ni-silicides therefore trapped at the interface of the p-n junction. These Ni-related defects lead a large leakage current and thus degrade the performance of the solar cell [102]. Therefore, Ni contamination inside the Ni-metal mediated crystallized poly-Si should be reduced. Our proposed Ni-gettering method would effectively reduce Ni residue inside NILC poly-Si and improve the electrical properties of the thin-film and nanowire transistors. Hence, the proposed method could be a candidate to solve this issue.

(2) High-performance poly-Si nanowires (NWs) TFTs have been fabricated by nickel-metal induced lateral crystallization (NILC). The cross-section of the fabricated Si NWs is similar to the triangular shape. H. C. Lin et al even could fabricate Si NWs in the

square shape of the cross-section. Therefore it is desired to investigate the effect of NW geometry on NILC rate for the fabrication of NILC poly-Si NWs TFTs. Moreover much research has been done to clarify the basic NILC mechanism, none has been reported on its geometry dependence.

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Publication List

Journal Paper:

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