# 國立交通大學

## 材料科學與工程研究所

## 博士論文

高速與低功率邏輯應用之砷化銦鋁/砷化銦鎵變異結構高電子移動率電晶體之研究

The Study of InAlAs/$In_xGa_{1-x}As$ Metamorphic High Electron Mobility Transistors for High Speed and Low Power Logic Applications

研 究 生：郭 建 億

指導教授：張　翼 博士

中華民國九十七年七月

# 高速與低功率邏輯應用之砷化銦鋁/砷化銦鎵變異結構高電子移動率電晶體之研究

# The Study of InAlAs/$In_xGa_{1-x}As$ Metamorphic High Electron Mobility Transistors for High Speed and Low Power Logic Applications


研 究 生：郭 建 億　　Student: Chien-I Kuo

指導教授：張　翼 博士　　Advisor: Dr. Edward Yi Chang


國立交通大學

材料科學與工程研究所

博士論文

**A Dissertation**

Submitted to Department of Materials Science and Engineering

College of Engineering

National Chiao Tung University

In Partial Fulfill of the Requirements

For the Degree of

Doctor of Philosophy in Engineering

2008

Hsinchu, Taiwan, Republic of China

中華民國九十七年七月

# 高速與低功率邏輯應用之砷化銦鋁/砷化銦鎵變異結構高電子移動率電晶體之研究

研究生：郭 建 億　　指導教授：張 翼 博士

國立交通大學材料科學與工程研究所

## 摘要

本研究成功製作高頻與低功率邏輯應用之高效能砷化銦鋁/砷化銦鎵變異結構高電子移動率電晶體 (Metamorphic High Electron Mobility Transistors，MHEMTs)，並且對此元件做了深入的分析與探討。為了增進此變異結構高電子移動率電晶體之特性，在改善元件磊晶結構的同時，也搭配了奈米級閘極線寬與白金閘極掘入 (Pt-buried gate) 的技術。另外，也對未來 N 型金氧半場效電晶體極具潛力的三五半導體通道材料其表面處理方式做了詳細的探討。

在論文中，研發出以白金閘極掘入的技術應用在以砷化銦 (InAs) 為通道的 HEMT 元件上。利用此方式有許多的優點，白金的功函數較傳統以鈦金屬閘極高，在掘入蕭基特層後，不但可以縮短電極與通道間距離，藉以抑制短通道效應外，還可以降低漏電流與源極阻抗等等，進而改善微波與邏輯特性。用此方法製作的 HEMT 元件具有 1418 mA/mm 的汲極-源極電流以及 1600mS/mm 的高轉導值。此元件與未有閘極掘入元件相較下，截止頻率($f_T$)由原本的 390 GHz 提升到 494 GHz，最大震盪頻率($f_{max}$)也由原本的 360 GHz 提升到 390 GHz。在雜訊指數方面，在 17 GHz 頻率下為 0.82 dB 且相對應的增益(associated gain)為 14 dB，其量測的汲極偏壓為 0.3V 而直流消耗功率僅 1.14 mW，顯現此元件極有潛力作

為低電壓的小訊號放大器，此外由於閘極掘入後，閘極漏電與閘極-源極電容值皆變小，使得在元件閘極延遲時間上達到 0.78 picosecond 且其開關電流比值依舊維持在三個數量級。

另外，更進一步的縮小源極與汲極間距，期使元件的邏輯特性更加優異，並且成功的應用在 HEMT 元件製作上，同時也分析了這種窄能隙半導體其撞擊離子化的現象並與先進的矽半導體元件及砷化銻(InSb)元件做了詳細的比較與邏輯特性分析。此砷化銦為主通道，銦含量高達 70%的砷化銦鎵為次通道的元件，其發生撞擊離子化偏壓點約為 0.8 V 左右。在邏輯特性方面，此元件的汲極引致能障下降為 200mV/V，次臨界擺幅約 115 mV/dec，在偏壓 0.5 V 時展現了 0.54 picosecond 的閘極延遲，但由於其通道為窄能隙半導體，關閉態的漏電流較大，起因於蕭基特閘極漏電與能帶能帶間的穿遂電流，但相較於砷化銻通道元件佳。此外，與先進的矽奈米元件相比，砷化銦通道 HEMTs 展現了優異的閘極延遲與 3.1 倍高的 $f_T$ 於相同直流消耗功率上等特性。因此，III-V 高速元件將會是在後矽半導體世代扮演重要的角色。

另外，論文中也探討了以 10 奈米厚的二氧化鋯高介電常數材料製作的假晶砷化銦鎵($In_{0.53}Ga_{0.47}As$)金氧半電容結構。在成長介電薄膜時砷化銦鎵的表面也做了以硫化銨與稀釋鹽酸處理。比較兩者之後發現，經過硫化處理與 350 度退火後的電容結構具有良好的電容-電性特性(強反轉現象)，高崩潰電壓，與低漏電等，可見其具有較低的介面缺陷或是較少的不完美鍵結因而減低了費米釘札(Fermi-level pinning)。由材料分析得知，在高解析度的穿透式電子顯微鏡下可看到約 20Å 的薄膜介於半導體與介電薄膜中，進一步透過二次離子質譜儀分析，此薄膜為硫元素。因此證明了以硫化銨處理後其可以保護三五半導體表面發生原生氧化層導致元件特性變差。

# The Study of InAlAs/$In_xGa_{1-x}As$ Metamorphic High Electron Mobility Transistors for High Speed and Low Power Logic Applications

Student: Chien-I Kuo Advisor: Dr. Edward Yi Chang

Department of Materials Science and Engineering

National Chiao Tung University

## Abstract

High performance eighty nanometer gate length InAlAs/$In_xGa_{1-x}As$ metamorphic high electron mobility transistors (MHEMTs) have been fabricated successfully and characterized for high frequency and low-power logic applications. The performance of the MHEMTs was improved by optimizing the device structure, using the Pt-buried gate techniques and shrinking the source-drain spacing. In addition, the surface pre-treatments of III-V channel material before high-k deposition for future III-V nMOSFET were also studied.

In this dissertation, the fabrication of 80 nm InAs channel MHEMTs using Pt gate-sinking was developed. There are several advantages to improve RF and logic performance with gate-sinking process such as high metal work function, suppression the short channel effect, the reduction of the gate leakage current and decrease of the source resistance. The fabricated InAs MHEMT using this technique shows a drain-source current of 1418 mA/mm and transconductance of 1600 mS/mm. The cutoff frequency $f_T$ and maximum oscillation frequency $f_{max}$ of the MHEMT with Pt-buried gate are 494 GHz and 390 GHz as compared with that of 390 GHz and 360

GHz for device without gate sinking, respectively. The noise figure of the InAs MHEMT was 0.82dB and the associated gain was 14 dB at 17GHz under the bias condition of $V_{DS}$ = 0.3 V, indicating great potential for low-power LNA application. Because of the reduction of gate leakage current and gate-to-source capacitance, the intrinsic gate delay of the device is 0.78 picosecond, while maintaining an $I_{ON}/I_{OFF}$ ratio above $10^3$.

In addition, to promote the logic performance of InAs HEMT, device with small source-drain spacing were fabricated for high speed and low-voltage digital applications. Care must be taken while biasing device with such narrow energy bandgap when the impact ionization occurred in order to avoid the degradation of devices. Performance degradations were observed on the DC and RF characteristics due to impact ionization when the drain bias $V_{DS}$ > 0.8 V. For logic parameters, a drain-induced barrier lowering of 200 mV/V, a subthreshold slope of 115 mV/dec and a very low gate delay of 0.54 ps were obtained. Besides, InAs HEMTs exhibit excellent logic performances such as gate delay and 3.1 times higher $f_T$ at the same DC power dissipation when benchmarking advanced Si MOSFETs. Therefore, III-V high speed device has great potential to play an important role in Post-Si era.

In addition, the electrical properties of the metamorphic $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors with a 100-Å-thick $ZrO_2$ layer as high-k dielectrics were investigated. The $In_{0.53}Ga_{0.47}As$ surface was pretreated by either sulfur passivation or HCl cleaning before the $ZrO_2$ deposition. Owing to the lower interface-state density or Fermi-level unpinning after sulfidation, the sulfur-passivated capacitor exhibited better accumulation capacitance and strong inversion at capacitance-voltage measurement than the HCl-cleaned capacitor after post deposition annealing at 350 $^oC$. On the basis of material analyses including High Resolution TEM and Secondary Ion Mass Spectrometer, the capacitors that subjected to sulfur

treatment were found to contain a thin sulfur layer on the interface, which protects the surface from oxidation and prevents performance degradation.

# 誌　謝

漫長的博士班生涯隨著論文的結束即將劃上完美的句號，首先最要感謝我的博士班指導教授 張翼博士。這些年裡，在老師的開明作風與悉心指導下，使我在獨立思考與解決問題能力上成長許多，此外老師提供了相當充足的儀器資源，讓我能全程參與美國英代爾半導體公司的尖端研究計畫，並且有機會前往日本東京工業大學（TITech）學習先進電子束微影技術，拓展研究的視野與世界觀，並學習日本人嚴謹的研究精神，同時老師也給予我許多機會參加國際會議，吸取國外半導體的新知，這些難能可貴的經歷與學習經驗，讓我受用無窮。

在這裡同時要特別感謝元智大學許恆通博士，他的耐心指導與每每在深夜裡的討論、實驗分析，使我減少許多摸索的時間也一起渡過許多英代爾 quarter review 準備報告的日子。此外也要謝謝在 TITech 的日子裡，Yasuyuki Miyamoto 教授，Takeshi Yamaguchi 先生以及 Susumu Kenmochi 先生，對我在日本東京做研究時的關心照顧以及實驗上的協助。感謝國家奈米元件實驗室(NDL)許多的工程師（邱佳松、鄧裕民、陳文林與廖國祥先生等）及交大奈米中心，同時提供優良的儀器設備與環境，使實驗能夠更加順利進行。

另外我也要感謝 CSD Lab.的許多伙伴，謝炎璋博士、連亦中博士、褚立新博士，陳俊淇博士等學長的鼓勵，還有陪伴我走過五年同窗生活的黃瑞乾同學、張家源同學、呂宗育同學，林龔樑同學與吳雲驥同學，還有許多可愛的學弟妹，張家達、許立翰、李芳銘、唐士軒、王景德、曾文仲、蕭佑霖、黃偉進、曾育玲、吳建瑩、陳鈺霖、蘇詠萱等，在實驗與生活上的幫忙使我不致感到孤立無援，以及詹前璋先生在儀器設備及廠務方面的幫忙。也要謝謝江韵涵、陳善理、黃碧玉、余蕙馨及鍾盈怡等諸位美麗的小姐在行政上的協助幫忙。

謝謝大學同學，柯利昇、邱介宏、張耀仁與許智明等伙伴與友達光電的王賢軍先生、力晶半導體的林嘉柏先生及茂德科技李偉強博士的相助與相挺，讓我

在無趣博士班日子裡過得充實。

最後，我要特別感謝在我的背後精神上支持與鼓勵的親人等，郭芳永先生、房春生先生、蘇真女士、楊春霞女士，以及哥哥與大嫂，感謝您們的關心、支持、包容與鼓勵，使我無後顧之憂，能夠專心順利完成學業，當然還有最重要的貼心女友妤真，謝謝她一路相伴，默默的支持，一同度過許多低潮時光，不如意日子，畢業是人生另一階段的開始，也是換我好好照顧妳的日子。願這份榮耀與您們分享。

# Contents

# Table Captions

## Chapter 1



## Chapter 2



## Chapter 4

# Figure Captions

## Chapter 1



## Chapter 2



## Chapter 3

## Chapter 4

## Chapter 5

# Chapter 6

# Chapter 1

# Introduction

## 1.1 General Background and Motivation

With the rapid progress of wireless communication industries, the applications have moved from the microwave toward millimeter wave frequency range. Consequently, the required performance specifications for the key components are getting more and more rigid. III-V based compound semiconductor devices such as GaAs pseudomorphic high electron mobility transistors (PHEMTs), metamorphic HEMTs (MHEMTs), conventional lattice-matched or pseudomorphic InAlAs/InGaAs/InP HEMTs (InP HEMTs) with high indium mole fraction channel, have shown superior performance as compared to the Si devices in high-frequency and high-speed applications. Many efforts have been made to improve the high-frequency performance of the III-V devices by means of refined heterjunction structure, and sub-nanometer gate length. Nanometer-T-shaped gate is generally used for the HEMTs to maximize the device performance.

On the other hand, the size scaling of CMOS has followed the famous Moore's law for over 30 years. In the current 65nm technology node, the gate length of a Si MOSFET is about 30 nm and such dimension is expected to reach about 10 nm by 2011, which is believed to be the ultimate limit for CMOS scaling. The trend of transistor technology is shown in Fig. 1.1 and several novel devices technology candidates that are often mentioned to replace Si CMOS including carbon nanotube

(CNT) transistors, semiconductor nanowires and spintronics [1-1]. While the majority of the above mentioned technologies are still in the prototyping stage, recent development in device technology of III-V FETs, especially the heterostructure HEMT devices has shown great potential to be the next generation high-speed logic device technology due to its maturity in device fabrication technologies and excellent RF performance.

Attention has recently been paid to III-V channels as a promising candidate of high performance n-MOSFETs beyond strained-Si devices [1-2]. This is because III-V compound semiconductors have ~ 50-100 x higher electron mobility than Si and III-V nMOSFET can exhibit very attractive and tangible worth. Table 1.1 lists the properties of some channel materials [1-3]. It is confirmed that III-V materials can play an important role in future high-speed, and low power CMOS logic transistors in the Post-Si era. However, the key challenge for III-V-based MOSFET is the lack of high-quality, thermodynamically stable insulators that passivate the interface states and prevent Fermi level pinning at III-V-gate dielectric interface [1-4 - 1-6]. Many research groups have reported the necessary of special treatment on the III-V substrate surface prior to depositing the gate dielectrics such as interface passivation layer or plasma nitridation [1-7,1-8].

In this study, HEMTs with several device structures were fabricated successfully and evaluated characteristics of these devices for high frequency, high speed and logic applications. In addition, fabrication of high-k material on III-V compound semiconductor capacitors using different surface treatments was also studied.

## 1.2 Overview of High Electron Mobility Transistor

High electron mobility transistor (HEMT) or called Quantum-well field-effect

transistor (QWFET) is one of the most mature III-V semiconductor transistors which rely on the use of heterojunction for its operation. The first demonstration of the HEMT was made by Fujitsu Lab. in 1980 [1-9]. Fig. 1.2 represents a cross-sectional view of a conventional HEMT structure. The epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer with an un-doped spacer in the wide band gap material and narrow band gap material to separate the ionized donors from the channel. The detailed description of energy band diagram of InAlAs/InGaAs Metamorphic HEMTs is shown in Fig. 1.3 [1-10]. As a result, HEMTs have superior carrier transport properties due to the band-gap engineering design.

For the past 5 years, GaAs-based MHEMTs and InP-based HEMTs with remarkable device performance for high frequency applications have been published and these results are listed in Table 1.2. As seen from this table, high indium content channel material HEMTs with nanometer gate length is the main way to enhance the device performance.

## 1.3 Logic Suitability of HEMTs for Beyond-CMOS Applications

Lately, III-V technologies have attracted again for logic circuit when CMOS roadmap comes to the end. The main reason is the manufacturing technology for III-V devices is relatively mature compared to other novel devices such as carbon-nanotube transistors and semiconductor nanowires. In digital application, a transistor operates as a switch and is different form in microwave or millimeter wave application. Fig. 1.4 shows the electrical figures of merit of a transistor as a switch [1-11]. As seen from the figure, figures of merit relevant to logic application, for example drain-induced barrier lowering (DIBL), subthreshold slope (S), on-state and off-state

current ratio, and the delay time (CV/I), these are important parameters for these devices to be used for future digital applications.

In this study, we have applied a methodology that was recently proposed to analyze new devices which often feature nonoptimized values of $V_T$ [1-12]. The evaluation methodology is shown in Fig. 1.5. First, we select gate-to-source voltage at 1mA/mm of drain-source current as the threshold voltage. Then we selected $I_{ON}$ as 2/3 $V_{CC}$ swing above the threshold voltage, and $I_{OFF}$ as 1/3 $V_{CC}$ swing below the threshold voltage. Based on this definition, we extracted and compared the device's logic parameters, such as subthreshold slope, DIBL and $I_{ON}/I_{OFF}$ ratio for the $In_xGa_{1-x}As$ HEMTs developed in this study.

## 1.4 Outline of this dissertation

This dissertation covers the study of RF and logic evaluation of $In_xGa_{1-x}As$ channel HEMTs and the metamorphic $In_{0.53}Ga_{0.47}As$ MOS capacitors with zirconium dioxide ($ZrO_2$) high-k dielectrics. It is divided into 7 chapters.

In chapters 2, the details of the fabrication process of the $In_xGa_{1-x}As$ HEMTs are introduced, including the mesa isolation, ohmic contact formation, T-shaped gate process, gate recess, $SiN_x$ passivation and airbridge formation.

In chapter 3, the DC and RF characterizations of the device are described.

In chapter 4, the results of RF and logic evaluation of the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ channel HEMTs with Pt-buried gate are given. The current gain cutoff frequency of the 80 nm gate-length device increased from 390 GHz to 494 GHz and the gate delay time decreased from 0.83 psec to 0.78 psec after the gate sinking process. The improvements of the device characteristics are due to the reduction of gate-to-source capacitance ($C_{gs}$) and the source resistance (Rs) after

gate sinking. In addition, for ultra-low power low-noise amplifier application, the InAs channel device demonstrates excellent dc power consumption with higher gain compared with other GaAs- or InP –based HEMTs to date.

In chapter 5, the figures of merit relevant to logic, such as gate delay, $I_{ON}/I_{OFF}$, DIBL, and S of the InAs-channel HEMTs with 2 μm source-drain spacing for low-voltage digital applications, are studied. Besides, the bias conditions for the narrow energy bandgap electron devices before occurrence of impact ionization are studied.

In chapter 6, the electrical properties of metamorphic $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors with a 100-Å-thick $ZrO_2$ as high-k dielectrics are studied. The $In_{0.53}Ga_{0.47}As$ surface was pretreated by either sulfur passivation or HCl cleaning before the $ZrO_2$ deposition. Owing to the lower interface-state density after sulfidation, the sulfur-passivated capacitor exhibited better accumulation capacitance and strong inversion at capacitance-voltage measurement than the HCl-cleaned capacitor after post deposition annealing at 350°C. On the basis of material analyses including high resolution TEM and SIMS, the capacitors that subjected to underwent sulfur treatment were found to contain a thin sulfur layer on the interface, which protects their surface from air exposure and prevents performance degradation.

Finally, chapter 7 is the conclusion of the dissertation. The RF and Logic performances of the InAs channel HEMTs was improved by using Pt-buried gate due to the reduction of gate-to-channel distance, small $C_{gs}$ and the small Rs. The InAs HEMTs showed excellent DC and RF performances after gate sinking, indicating great potential for this device for low voltage high-speed digital applications.

In addition, the metamorphic $In_{0.53}Ga_{0.47}As$ MOS capacitors with $ZrO_2$ exhibit better C-V characteristics and show reduced leakage current after sulfur pretreatment.

The removal of the defective bonding states and the enhanced barrier for the electron conduction due to the unpinning of Fermi level, are primarily responsible for the improvement of the electrical characteristics.

| | Si | Ge | GaAs | InP | InAs | InSb |
|---|---|---|---|---|---|---|
| electron mob. ($cm^2/Vs$) | 1600 | 3900 | 9200 | 5400 | 40000 | 77000 |
| electron effective mass ($/m_0$) | $m_t$: 0.19<br>$m_l$: 0. 916 | $m_t$: 0.082<br>$m_l$: 1.467 | 0.067 | 0.082 | 0.023 | 0.014 |
| hole mob. ($cm^2/Vs$) | 430 | 1900 | 400 | 200 | 500 | 850 |
| Hole effective mass ($/m_0$) | $m_{HH}$: 0.49<br>$m_{LH}$: 0.16 | $m_{HH}$: 0.28<br>$m_{LH}$: 0.044 | $m_{HH}$: 0.45<br>$m_{LH}$: 0.082 | $m_{HH}$: 0.45<br>$m_{LH}$: 0.12 | $m_{HH}$: 0.57<br>$m_{LH}$: 0.35 | $m_{HH}$: 0.44<br>$m_{LH}$: 0.016 |
| band gap (eV) | 1.12 | 0.66 | 1.42 | 1.34 | 0.36 | 0.17 |
| permittivity | 11.8 | 16 | 12 | 12.6 | 14.8 | 17 |

Table 1.1 The bulk electron and hole mobility, the electron and hole effective mass, and the bandgap and the permittivity of Si, Ge, and main III-V semiconductor.

| **Devices** | **In (%)** | **$L_g$ (nm)** | **$g_m$ (S/mm)** | **$f_T$ (GHz)** | **$f_{max}$ (GHz)** | **Published** | **Affiliation** |
|---|---|---|---|---|---|---|---|
| **InP HEMT** | 65 | **50** | 1.25 | 286 | 207 | 2003, 11th GaAs sym. | Chalmers Univ. |
| **GaAs MHEMT** | 53 | **70** | 1.45 | 293 | 337 | 2003, 11th GaAs sym | IAF., Germany |
| **InP HEMT** | 70 | **30** | 1.5 | 547 | 400 | May. 2004, *IEEE, EDL.* | CRL., Fujitsu. |
| **GaAs MHEMT** | 53 | **50** | 1.028 | 440* | 400 | Nov., 2005, *IEEE, EDL* | Glasgow Univ. |
| **GaAs MHEMT** | 53 | **50** | 1.27 | 489 | 422 | July 2007 *IEEE, EDL* | Dongguk Univ. |

Table 1.2 Best performance of InP HEMTs and GaAs-based MHEMTs published in recent years.

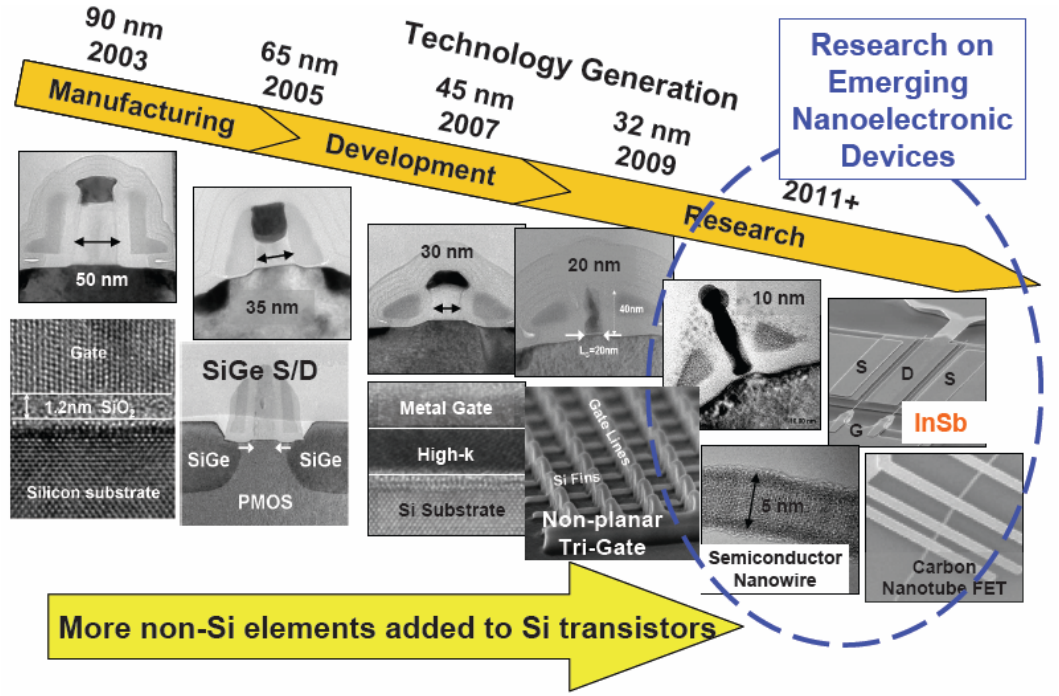



Fig. 1.1 The trend of transistor technology

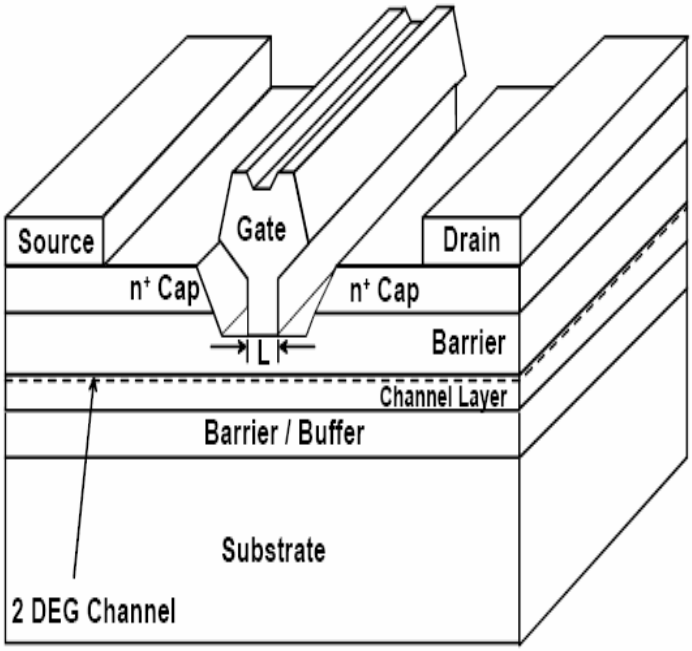



Fig. 1.2 Conventional HEMT structure.

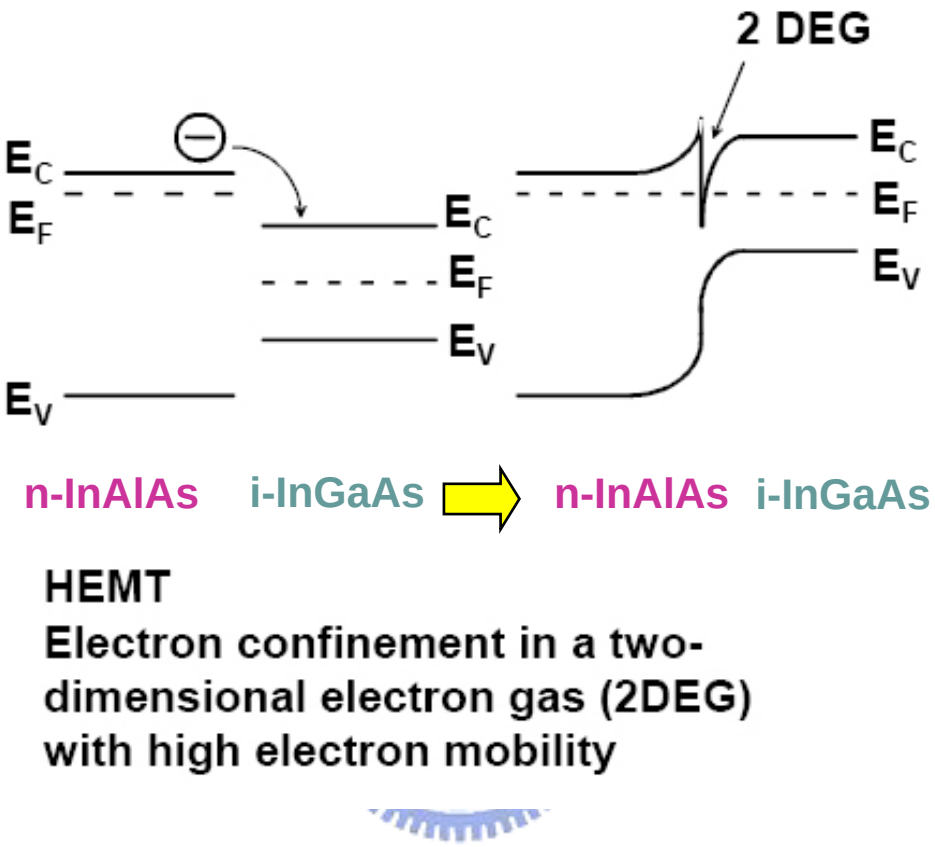



Fig. 1.3 Band Diagram of InAlAs/InGaAs MHEMTs

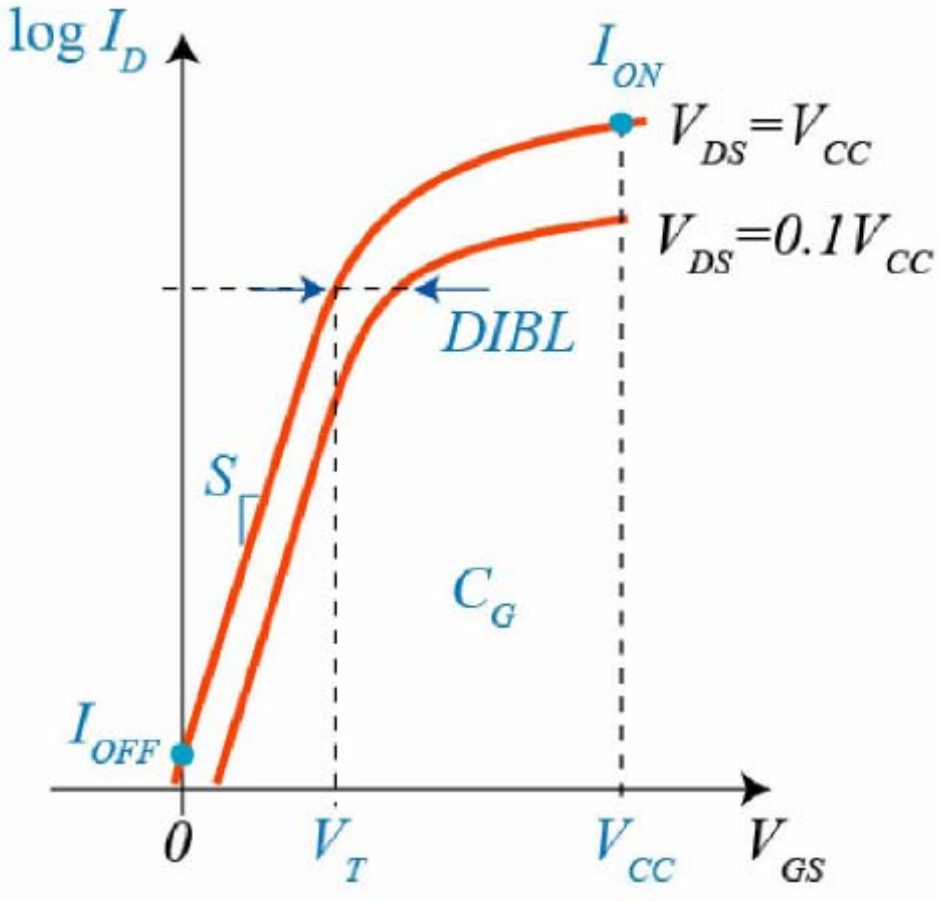



Fig. 1.4 Electrical figures of merit of a transistor as a switch

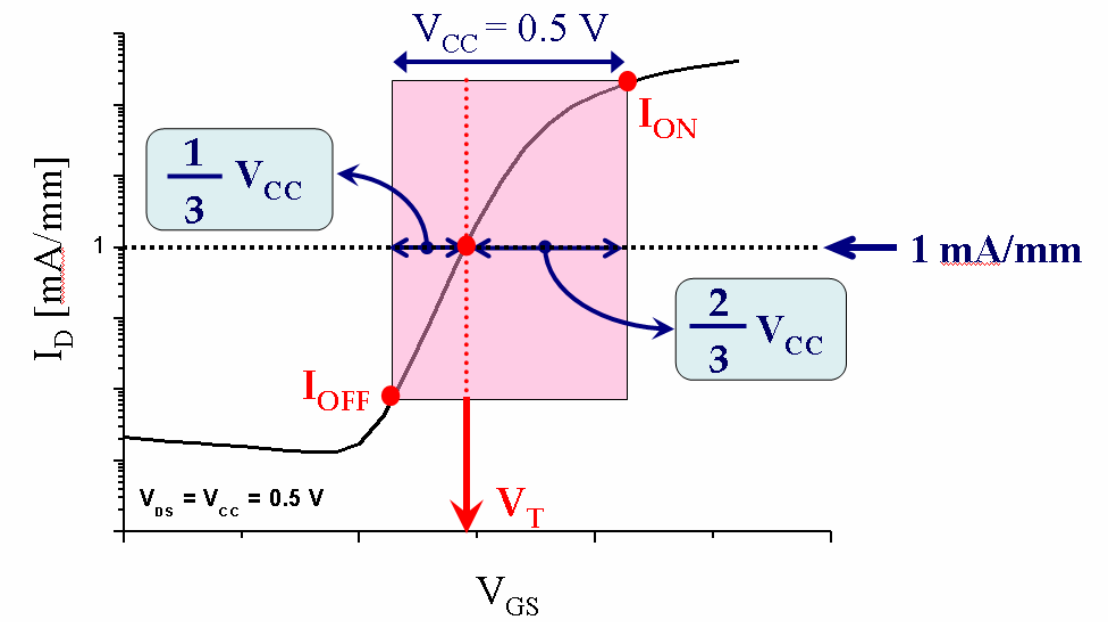



Fig. 1.5 Evaluation methodology for the logic performance of HEMTs

# Chapter 2

# Fabrication of $In_xGa_{1-x}As$-Channel Metamorphic High Electron Mobility Transistors

## 2.1 Device structure

The epitaxial layers of the $In_xGa_{1-x}As$-channel metamorphic HEMT with $In_xAl_{1-x}As$ grading buffer layer were grown on GaAs substrate or InP substrate by molecular beam epitaxy (MBE). Using metamorphic buffer layer provides the ability to accommodate the lattice mismatch between $In_xGa_{1-x}As$ channel and GaAs substrate. Therefore, the high indium content in the $In_xGa_{1-x}As$ channel can be achieved in spite of the large lattice mismatch between the active epilayers and the substrate. In this study, the detailed expitaxial structures of the devices with different Indium content in $In_xGa_{1-x}As$ channel from 52%, 70% to 100% are shown in Table. 2.1.

## 2.2 Device fabrication

The fabrication process of HEMTs in this study includes several steps:

1. Mesa isolation
2. Ohmic contact formation
3. Fabrication of T-shaped gate process by E-Beam lithography
4. Gate recess
5. Device passivation

6. Airbridage formation

2.2.1 Mesa isolation

Device isolation is the first step of the whole HEMT fabrication process which was used to define the active region of the device on the wafer. For mesa isolations, the active areas were first masked by Shipley S1818 photo resist and then, the InGaAs/InAlAs layers was etched by a phosphoric based solution, following that, a hydrochloric acid based wet etch was used to etch the InP stopper layer [2-1]. According to the device structure, the mesa was etched to the buffer layer to provide good device isolation. Finally, the etching depth was measured by α-step after the photo-resist was stripped and the etched profile was checked by scanning electron microscopy.

2.2.2 Ohmic contact formation

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner were used to define the Ohmic pattern and to form the undercut profile for the metal lift-off. HCl-based solution was used as the pre-metallization cleaning solution to remove the native oxide of the InGaAs surface before Ohmic metallization. Ohmic metals multilayer Au/Ge/Ni/Au, from the bottom to the top, was deposited in the appropriate composition by e-gun evaporation system. After lift-off process, source and drain Ohmic contacts were formed by annealing at adequate temperature for 25 sec in forming gas atmosphere. Fig. 2.1 shows the drain current as a function of RTA temperature at the drain bias of 0.5 V before gate recess. The best RTA temperature was 250 $^{o}$C. Germanium atoms diffused into the heavily doped InGaAs during the

thermal annealing process [2-2]. The specific contact resistance was checked by the transmission line method (TLM) in the process control pattern monitor (PCM). In this particular approach, a linear array of contacts is fabricated with various spacings between them as shown in Fig 2.2. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively in this study. The typical measured contact resistance was $< 1 \times 10^{-6}$ Ω-cm$^2$ and the illustration of utilizing TLM to measure ohmic contact resistance was shown in Fig 2.3.

### 2.2.3 Fabrication of T-shaped gate process by E-Beam lithography

Short gate length with low gate resistance is necessary for high frequency and high speed application. T-shaped gate structure was the most common approach for achieving low gate resistance and a small gate foot [2-3]. In this study, T-shaped gate was achieved by using a conventional multilayer resist (ZEP-520/PMGI/ZEP-520-12) with Electron Beam lithography. Fig. 2.4 summarizes the process flow of the fabrication of nanometer T-shaped gate. The first E-beam exposure for top two layers was used to only define the head (Tee-top) of the T-shaped gate by modulating the exposure doses. After that, the ZEP and PMGI development were executed by using xylene and MF622, respectively. Then, single center exposure with high dose was used to define the footprint of the bottom ZEP-520 layer. Fig. 2.5 shows the dose dependence of the gate foot size after development. The 40 nm T-shaped gate resist profile is illustrated in Fig. 2.6.

### 2.2.4 Gate recess

The recess etching was performed using PH-adjusted solution of succinic (S.A.)

and $H_2O_2$ mixture for selective etching of the heavily doped InGaAs cap layer over InAlAs Schottky layer [2-4,2-5]. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over the recess process, thus enable the operation to approach the target current value, without over etching it. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was above 100. The target current after the gate recess is a critical parameter affecting the HEMT performance. In order to get the desired recess depth, the recess process was controlled by monitoring the ungated $I_{ds}$. The method used to control the recess depth is to monitor the source-to-drain current during the etching process. For the low noise PHEMT, the saturation current and the slope of the linear region go down as the recess groove was etched deeper and deeper. The wet etchant usually leaves a thin oxide layer on the InAlAs. HCl-based solution was used to remove the surface oxide. After recess etching, Ti/Pt/Au gate metal was evaporated and lifted off using ZDMAC remover (ZEON Corporation) to form T-shaped gate.

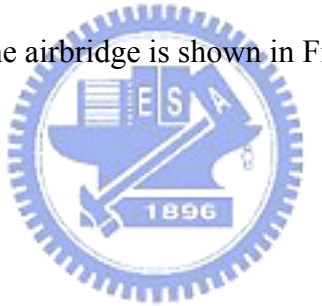
2.2.5 Device passivation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spaces of source-to-drain and gate-to-drain become smaller. In situation like this, the devices are very sensitive to the damages and contaminations such as chemicals, gases, and particles. The passivation layer protects the device from damage during process. The dielectric layer $SiN_x$ is a common choice for GaAs device passivation. In this study, STS PECVD system was used for depositing the silicon nitride film. The processing gases of the passivation PECVD were silane, ammonia, and nitrogen. The process condition was as following: process pressure: 900 mtorr, process temperature: 250°C and process

time: 10 minutes the silicon nitride film thickness was 600 Å. The reflection index was 2.0 as inspected by N&K anaylzer.

### 2.2.6 Airbridge formation

Airbridge is built by metal with air between the metal interconnect and the wafer surface beneath. Airbridges are used extensively in GaAs analog devices and MMICs for interconnections. They may be used to interconnect sources of FETs, to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor to adjacent metallization. The use of airbridge had several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents. The SEM image of the airbridge is shown in Fig. 2.7



| Layer | In= 52% | In=70% | In=100% |
|---|---|---|---|
| n+ Cap | InGaAs, x =0.52 | InGaAs, x =0.52 | InGaAs, x =0.53 |
| Etch stop | - | InP | InP |
| Barrier | InAlAs, x = 0.52 | InAlAs, x = 0.52 | InAlAs, x = 0.52 |
| Si δ-doping | $4.5x10^{12}$ | $5x10^{12}$ | $5x10^{12}$ |
| Spacer | InAlAs, x = 0.52 | InAlAs, x = 0.52 | InAlAs, x = 0.52 |
| Sub-Channel | - | - | InGaAs, x = 0.7 |
| Channel | InGaAs, x =0.52 | InGaAs, x =0.7 | InAs |
| Sub-Channel | - | - | InGaAs, x = 0.7 |
| Buffer | InAlAs, x = 0.52 | InAlAs, x = 0.52 | InAlAs, x = 0.52 |
| substrate | GaAs | GaAs | InP |

Table 2.1 The detailed expitaxial structures of the devices with different Indium content in $In_xGa_{1-x}As$ channel from 52%, 70% to 100%.

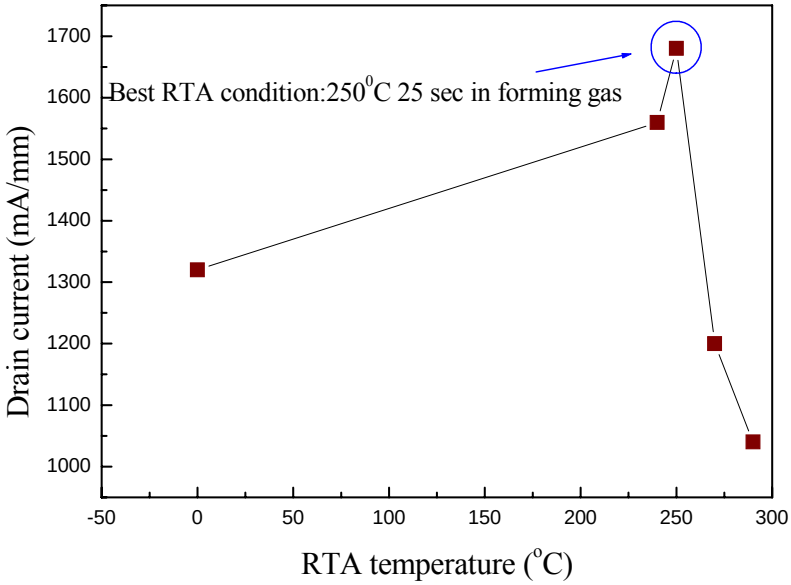



Fig. 2.1 Optimization of RTA Temperature for Ohmic Contact.

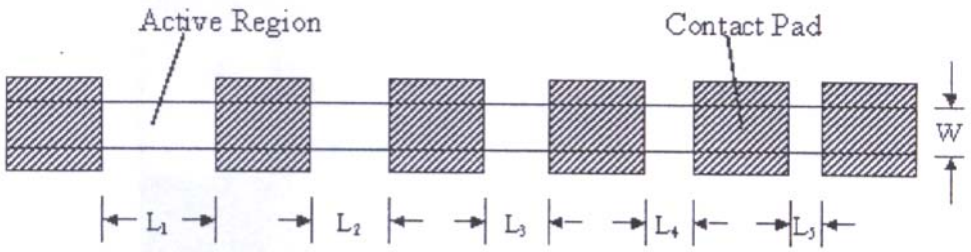



Fig. 2.2 TLM pattern

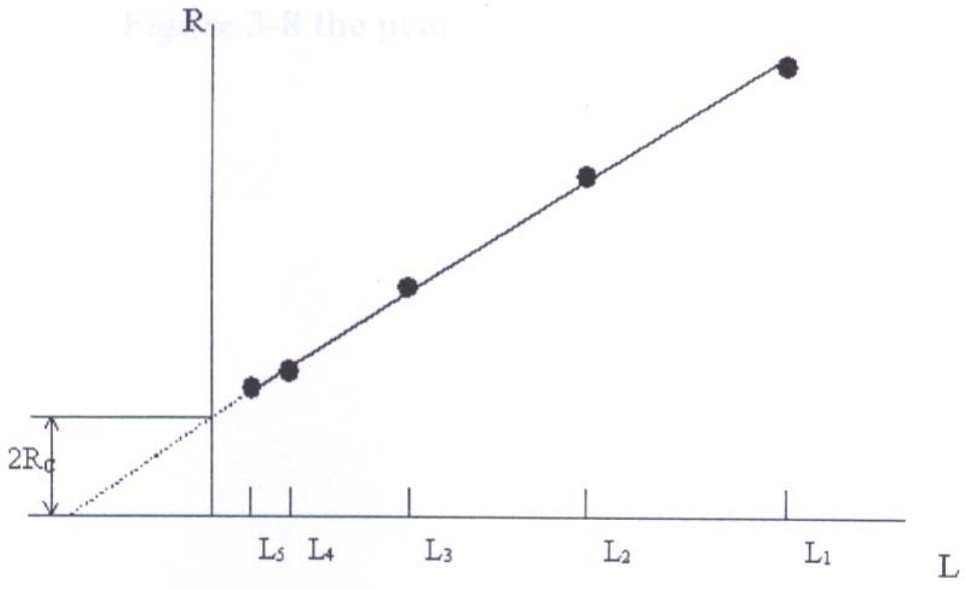



Fig. 2.3 The illustration of utilizing TLM to measure ohmic contact resistance

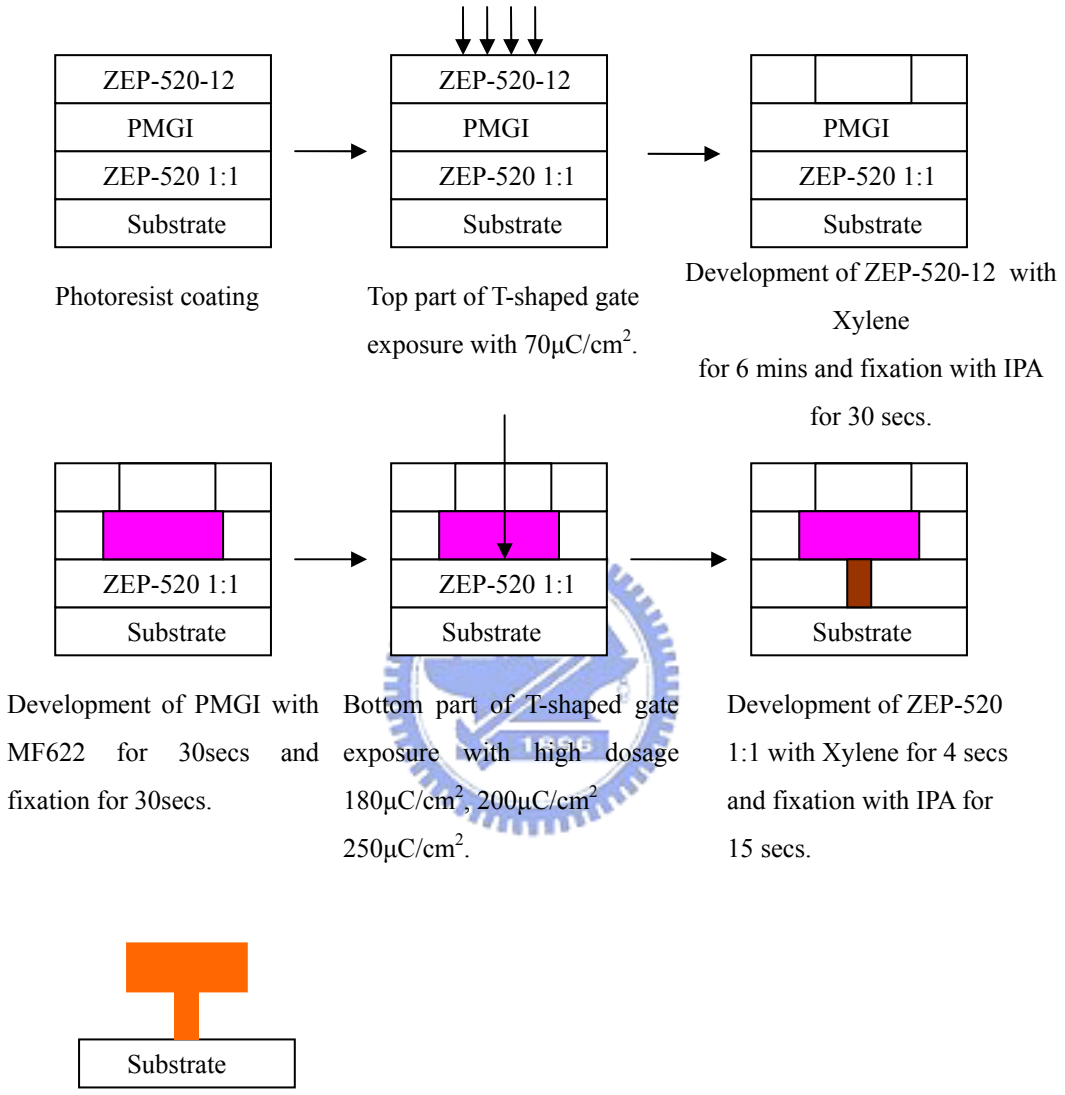



Fig. 2.4 T-shaped gate process flow

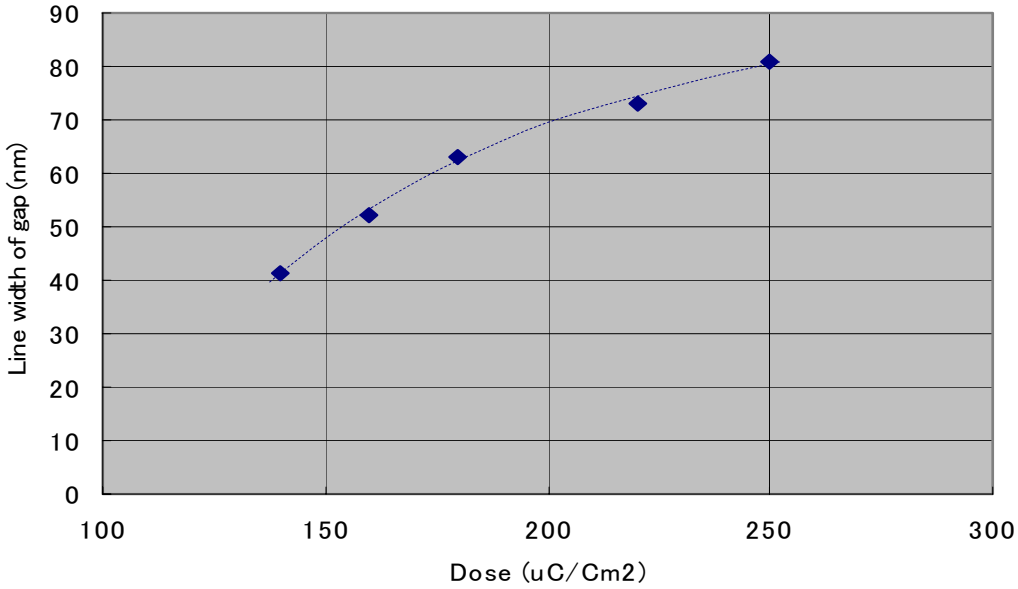



Fig. 2.5 The dose dependence of the gate foot size after development.

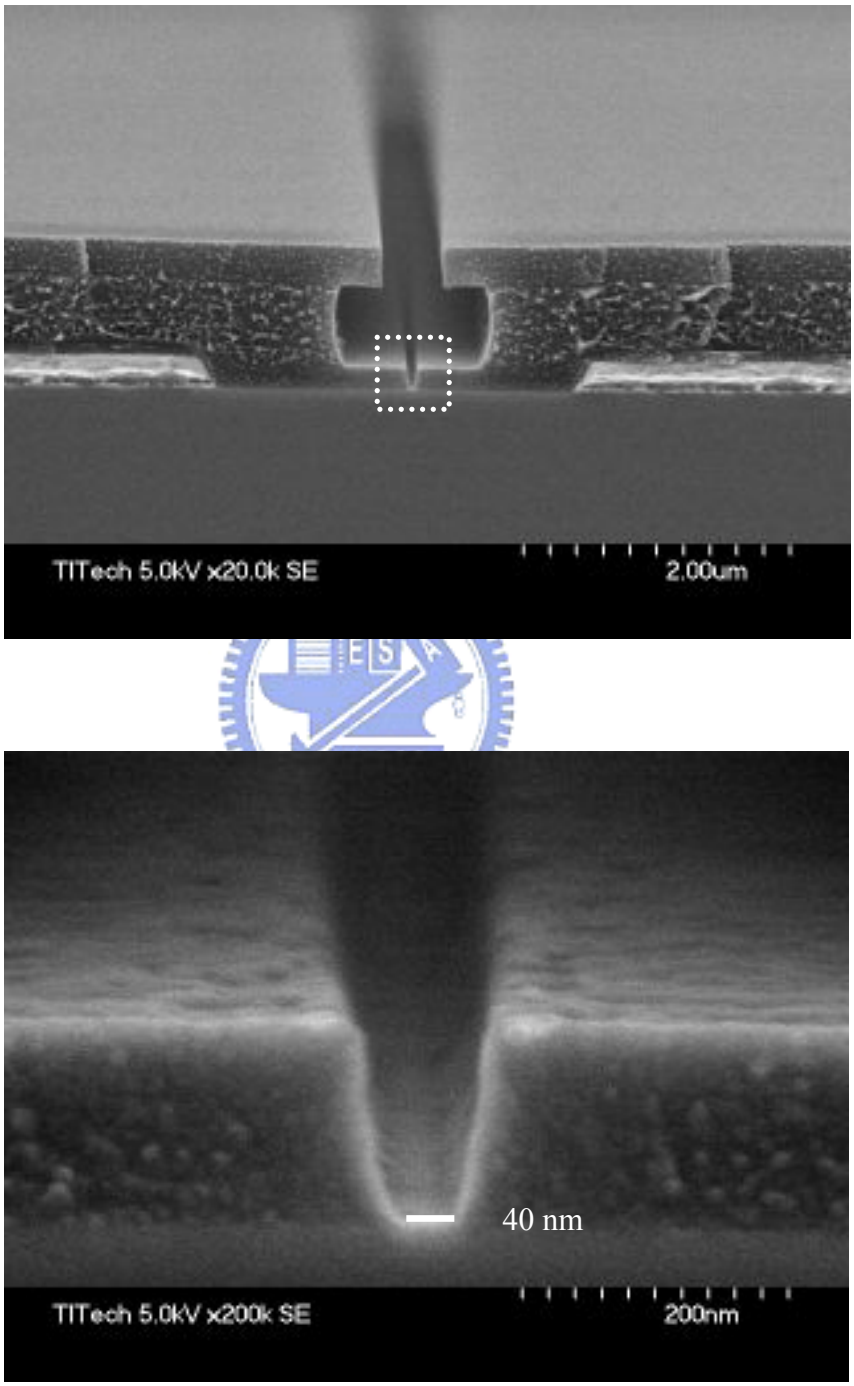



Fig. 2.6 The 40 nm T-shaped gate resist profile.

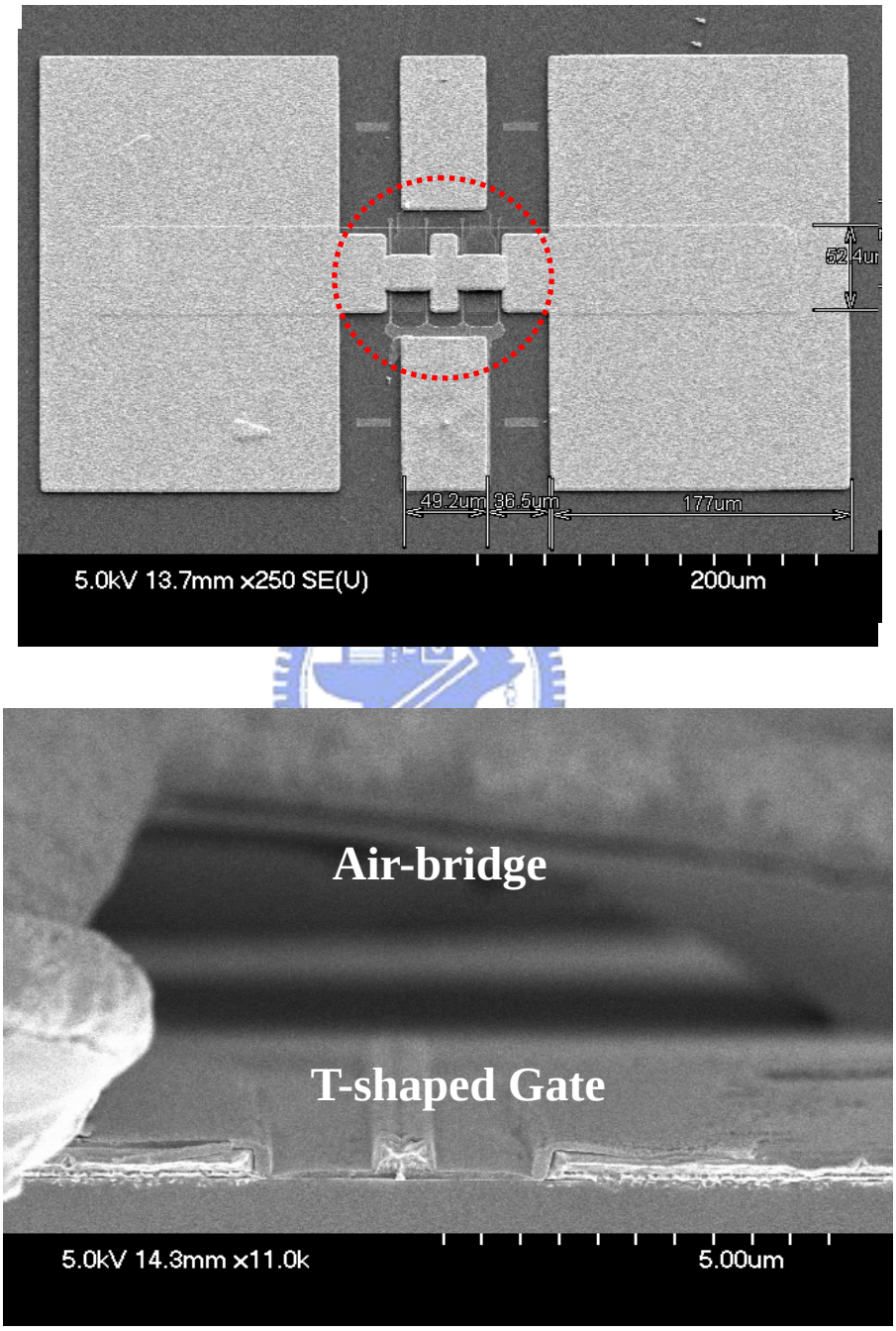



Fig. 2.7 SEM image of the finished airbridge

# Chapter 3

# DC and RF Measurements of $In_xGa_{1-x}As$ Metamorphic High Electron Mobility Transistors

## 3.1 Device Characterization

After the device fabrication process, DC and RF performance of the GaAs MHEMTs must be measured using on-wafer measurement. For the DC measurement, the I-V characteristics were obtained easily by using an HP4142B Modular DC Source/Monitor and SUSS PA200 Semi-Auto Probe Station. The Transmission Line Model (TLM) method for determining specific contact resistance was adopted by using 4-wires measurement. The *S*-parameters for the MHEMT devices were measured by HP8510XF Vector Network Analyzer using on-wafer GSG probes from Cascade MicroTech. However, finding the RF behavior of a device on a wafer was a complicated process. For conventional RF measurement of a packaged device, the wafer needs to be diced and then an individual die should be mounted into a text fixture. Discriminating between the die's and the fixture's responses became an issue. Furthermore, fixturing die was a time-consuming process, making it impractical for high-volume screening. Thus the need for on-wafer RF characterization was arisen [3-1].

Before examining the RF measurement process for the MHEMTs, the electrical behavior and characterization of the HEMT device are stated in the following section. In this study, de-embedding which must also be performed to

discover the true RF performance of the device is discussed.

### 3.2 DC characteristics [3-2]

The band diagrams at three different locations along the channel are illustrated in Fig. 3.1. There is a potential drop of channel charge density in the direction parallel to the channel, causing $q'_{CH}$ to be a function of the position $x$. In order to relate the HEMT equations to the well-developed MOSFET equations, a per area gate oxide capacitance was define as $C'_{OX}$. [3.3] Therefore, the channel charge sheet density is expressed as:

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \tag{3-1}$$

We denote the channel-to-source potential resulting from the applied Gate-Source voltage $V_{GS}$ and Drain-Source voltage $V_{DS}$. $V_T$ is threshold voltage and the $x$ means the position along the channel. The additional potential $V_{CS}(x)$ is called the channel-source potential. When $V_{DS} \neq 0$, the channel channel-source varies with $x$. In this figure, the channel-source potential measures the potential difference between any point $x$ along the channel with respect to the potential of the source. The channel current equation which we are familiar with $I = qA\mu_n\varepsilon$ (A=area) is proportional to the cross-section area of the current conduction, the charge density, the mobility $\mu_n$, and the electric field. Therefore, we obtain the form of the drift equation in HEMT:

$$I_{CH}(\chi) = -WC_{OX}\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \tag{3-2}$$

We note that $q'_{CH}$ is a negative quantity in HEMT, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, we find:

$$\int_0^L I_{DS}\,dx = -C'O\int_{V_{CS(O)}}^{V_{CS(L)}} C_{OX}\,\mu_n[V_{(GS)} - V_{(T)} - V_{(CS)}(\chi)]dV_{CS}(\chi) \tag{3-3}$$

To carry out the integration in Eq. (3-3), we assume temporarily that we are working in the linear region such that current saturation due to channel pinch off at the drain does not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX}\,\mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \tag{3-4}$$

Eq. (3-5) is plotted schematically in Fig. 3.2, with $I_D$ shown as a function of $V_{DS}$. The value of $V_{DS}$ corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of $I_D$ will respect to $V_{DS}$ and setting the result to zero. We find that:

$$V_{DS,SAT} = V_{GS} - V_T \tag{3-5}$$

At this saturation voltage, $q'_{CH}$ calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically, the channel at the drain does not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which $q'_{CH}$ $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the drain current is given by:

$$I_{DS} = \frac{W_g\, C'_{OX}\,\mu_n}{Lg}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} < V_{DS,SAT} \tag{3-6}$$

$$= \frac{W_g C'_{OX}\ \mu_n}{L_g}\left[\frac{(V_{GS}-V_T)^2}{2}\right] \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}7)$$

For HEMTs, it is convenient to define the *saturation index (α)* as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,SAT}} \qquad \text{for } V_{DS} < V_{DS,SAT}$$

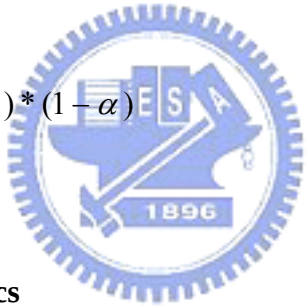
$$= 0 \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}8)$$

The drain current increases due to the perturbations in $V_{GS}$ and $V_{DS}$. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const.}$$

We also can write:

$$g_m = \frac{W_g C'_{OX}\ \mu_n}{L_g}(V_{GS}-V_T) * (1-\alpha)$$



### 3.3 Breakdown characteristics

Breakdown mechanisms and models have been discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier

scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage $BV_{gd}$ is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

### 3.4 Scattering parameters [3-2]

Generally, the Scattering parameters, which referred to as S-parameters, are fundamental to microwave measurement. S-parameters are a way of specifying return loss and insertion loss. The relation of the microwave signals and s-parameters are defined as follows:

*s*-parameters: $\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix}$

Microwave signals going into or coming out of the input port are labeled by a subscript 1. Signals going into or coming out of the input port are labeled by a subscript 2. The electric field of the microwave signal going into the component ports is designated a; that leaving the ports is designated b. Therefore,

$a_1$ is the electric field of the microwave signal entering the component input.

$b_1$ is the electric field of the microwave signal leaving the component input.

$a_2$ is the electric field of the microwave signal entering the component output.

$b_2$ is the electric field of the microwave signal leaving the component output.

By definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}$$

$$s21 = \left.\frac{b2}{a1}\right|_{a2=0}$$

$$s12 = \left.\frac{b1}{a2}\right|_{a1=0}$$

$$s22 = \left.\frac{b2}{a2}\right|_{a1=0}$$

Consequently, $s_{11}$ is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output. Because $b_1$ and $a_1$ are electric fields, their ratio is a reflection coefficient. Similarly, $s_{21}$ is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, $s_{21}$ is a transmission coefficient and is related to the insertion loss or the gain of the device. $s_{22}$ is similar to $s_{11}$, but looks in the other direction into the device.

### 3.5 Current gain cutoff frequency $f_T$ and maximum oscillation frequency $f_{max}$

The $f_T$ of a device is the frequency at which the short circuit current becomes unity. $f_T$ is defined as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

, and the ($C_{gs}$ + $C_{gd}$) is the total capacitance related to the Schottky gate contact. From this relation, we could see that in order to achieve high $f_T$, large $g_m$ and small total gate capacitance must be achieved. Small total gate capacitance is accomplished by short gate length; for millimeter-wave applications the gate length is usually smaller than 0.15μm. In this equation

$$f_T = \frac{g_m}{2\pi C_G} = \frac{Z_G v_{sat}\varepsilon}{w} \bullet \frac{w}{\varepsilon Z_G L_G} \bullet \frac{1}{2\pi} = \frac{v_{sat}}{2\pi L_G}$$

the $L_G$ is the is the gate length; therefore, the shorter the gate length the higher the $f_T$ and higher the $g_m$. The intrinsic *S* parameters are used to determine the unity current-gain cut-off frequency ($f_T$). It can be determined by extrapolation of the short-circuit current gain $h_{21} = 0$ dB. $h_{21}$ can be defined as

$$h_{21} = \frac{2 s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12} s_{21}}$$

Another important parameter is $f_{max}$, which is the frequency where the power gain falls to unity. $f_{max}$ is expressed as

$$f_{\max} = \frac{f_T}{2\left(\frac{R_g + R_i + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right)^{\frac{1}{2}}}$$

This expression shows that to obtain useful power gain at high frequency, the $f_T$ of a device must be large; in addition, the resistances of gate, source and drain must be small.

### 3.6 Device modelling technique

When defining the high frequency RF performance of the HEMTs, it is essential to de-embed all the conductors on the top surface of the wafer such as the pad, metal, and interconnect. Detailed layout of the device in this study is shown in Fig. 3-3. This helps us to understand what is going on at the active region of the device. A number of different semiconductor device models exist like small-signal, large-signal, and noise models.

In this paper, an approach that combines the conventional way and 3-D full wave electromagnetic analysis is proposed and extracted the intrinsic parameters of devices. To accurately determine the equivalent circuit model, the overall structure is divided

into several blocks, including gate parasitic, drain parasitic, source parasitic and intrinsic part according to the scalability of the device size as shown in Fig. 3-4, where the parasitic elements should be kept at fixed values and not scalable with device size. The intrinsic block could further be divided into different equivalent circuit elements and shown in Fig. 3-5. Standard gradient optimization routine is used to minimize the error function value, which is defined as the difference between the modelled and measured S-parameters. Standard gradient optimization routine is used to minimize the error function value, which is defined as the difference between the modelled and measured S-parameters. In order to rigorously determine the parasitic elements, CST Microwave Studio which is based on finite integration algorithm in time domain (FIT) is applied to analyse the structure. It is observed from the filed plot that the two source buses are held at a lower potential referenced to the gate and source pads thus the E-filed lines tend to terminate at these buses indicating a strong capacitive parasitic (Fig. 3-6 a). To illustrate the difference, a similar structure without the two source buses is simulated and the electric filed at 10 GHz is plotted in Fig. 3-6 b, where a much coarser electric field distribution between the gate (drain) pad and source region is observed. Based on the EM analysis of the structure, the strong capacitive parasitic behavior between the gate (drain) pad and the source buses suggests two additional capacitors to be included in the equivalent circuit.

### 3.7 Noise figure

High-frequency noise relates with the device channel and capacitive coupling between the channel and the gate. The gate noise is represented by a gate-current noise generator $i_{ng}^2$ and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The channel

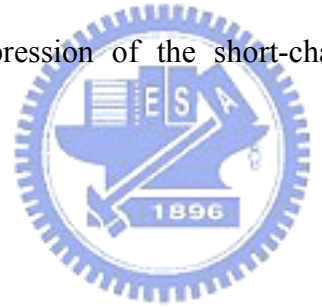
noise is represented by a drain-current noise generator $i_{nd}^2$ and is caused by various physical mechanisms driven by the electric field in the channel. Another noise source is gate leakage. The noise performance of a FET may be quantified by the noise figure, *NF*, which is a function of frequency, FET bias voltages, and impedance matching.

NF can be well approximated by the semi-empirical equation given by Fukui [3-4] and is shown as the following equation:

$NF = 1 + k\,(f/f_T)\,[g_m\,(R_g+R_s)]^{1/2}$,

$= 1 + 2\pi\,kf\,(Cgs + Cgd)\,[g_m\,(R_g+R_s)]^{1/2}$ , where k is a fitting parameter.

Generally, the reduction in Lg does not necessarily minimize the $NF_{min}$ because $R_g$ tends to increase due to a vertical resistance component of gate resistance, and also gm decreases due to a degraded gate drive so-called “short-channel effect”. Therefore, a reduction in $R_g$ and suppression of the short-channel effect are necessary to minimize $NF_{min}$.



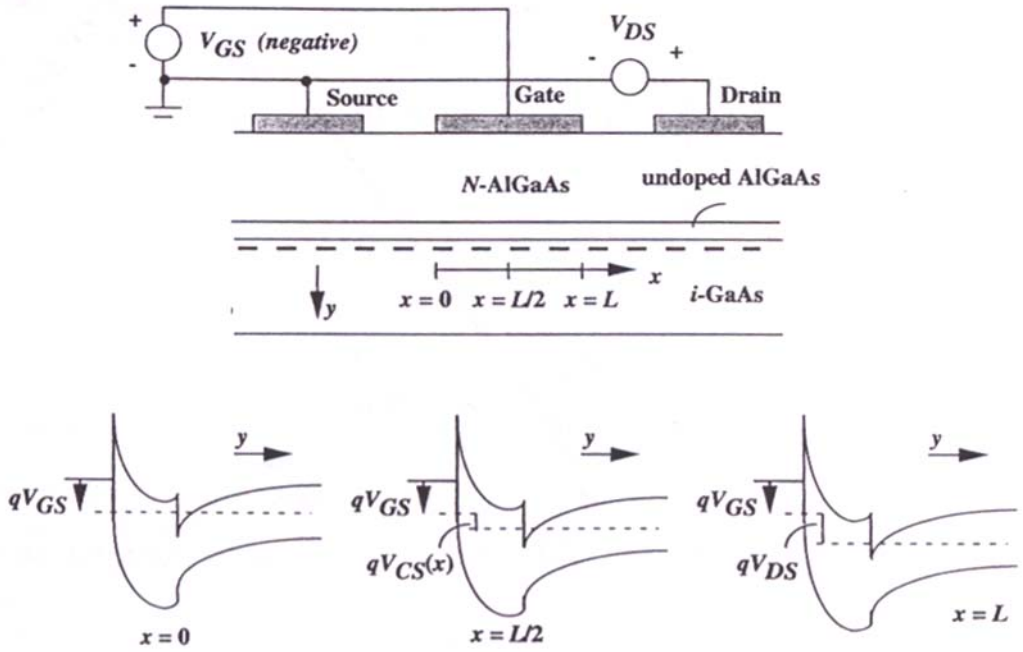



Fig. 3.1 Band diagrams at three different locations along the channel of a HEMT

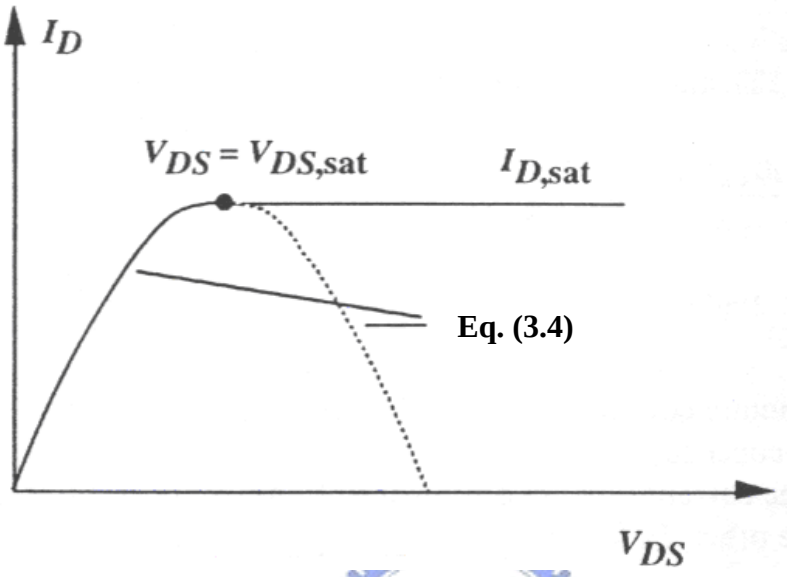



Fig. 3.2 Actual characteristics and those predicted by Eq. (3-3)

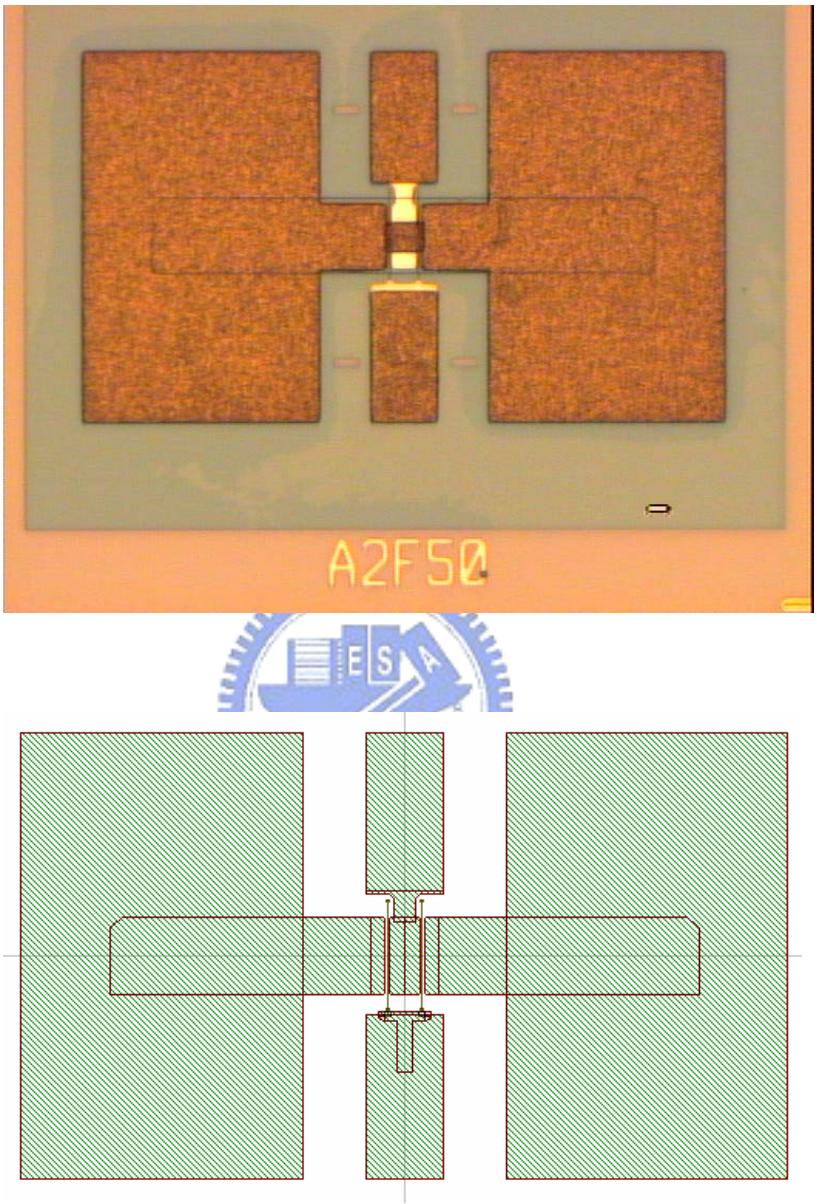



Fig. 3-3 Detailed layout of the device, the pads connecting the gate and drain are about 50×100um$^2$.

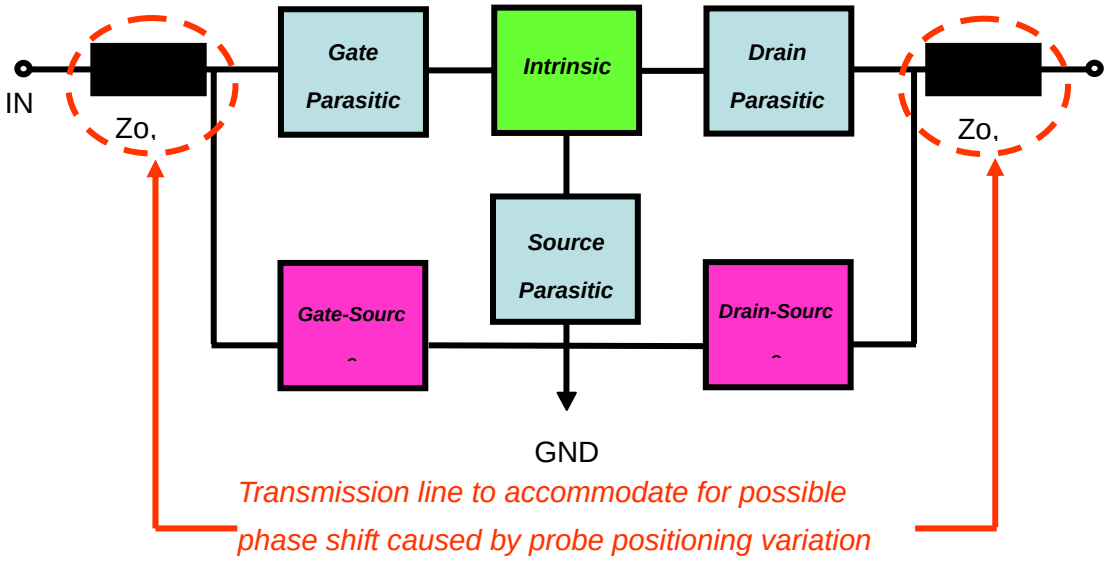



Fig. 3-4 The block diagram with determined parasitic elements for the overall device structure.

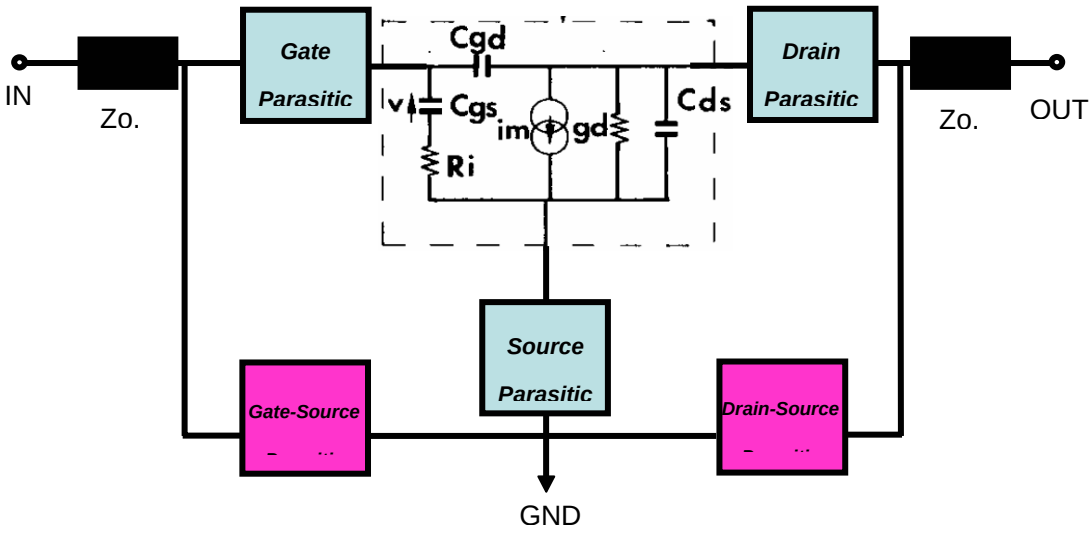
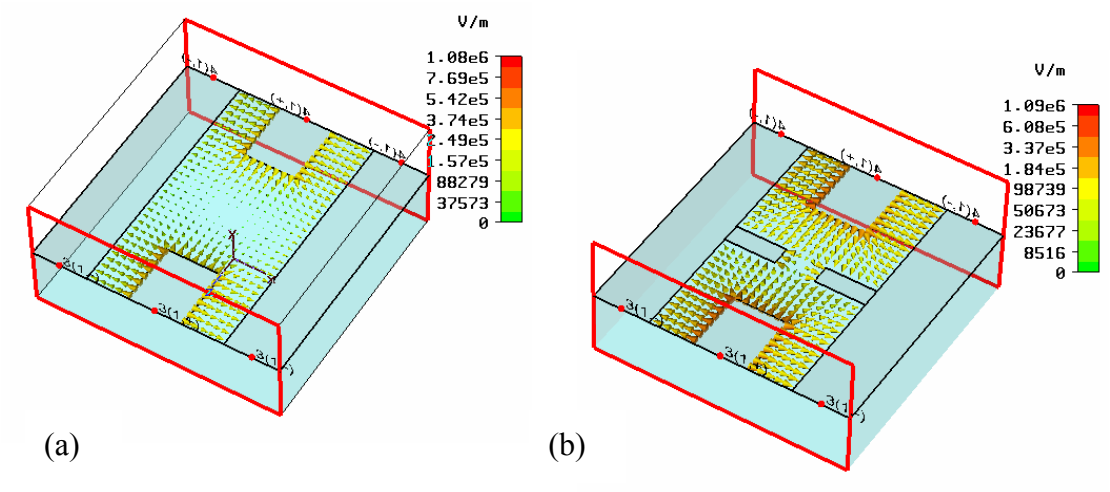



Fig. 3-5 Functional blocks of the equivalent circuit model, divided according the scalability with device size.




(a) (b)

Fig. 3-6 Analyzed electric field plot of the 2x50um device at 10 GHz. (a) with the source buses of the device (b) without the source buses of the device

# Chapter 4

# RF and Logic Performance Improvement of $In_{0.7}Ga_{0.3}As$ /InAs/$In_{0.7}Ga_{0.3}As$ Composite Channel HEMT Using Gate Sinking Technology

## 4.1 Introduction

For the advanced wireless communications, InP-based high electron mobility transistors (HEMTs) have attracted many attentions and demonstrated excellent high-frequency performance because of its superior electronic transport properties and high saturation velocity [4-1, 4-2]. Moreover, it is also a potential candidate FETs for low-power logic applications beyond Si CMOS technology in 22 nm node era [4-3,4-4]. InP HEMTs usually use In-rich InGaAs channel or InAs/InGaAs composite channel for good RF performance with large current drivability of the device. Meanwhile, the gate-recess structure also plays a critical role in the high frequency performance for HEMT devices. In general, the transconductance ($g_m$) of the device is mainly influenced by the gate-channel distance and the reduction of the distance can effectively increase the current gain cutoff frequency ($f_T$) because of the enhancement of average electron velocity underneath the gate electrode.

Additionally, the shape of the recessed region not only affects the source and drain resistance ($R_s$ and $R_d$) and the capacitances of gate-source and gate-drain ($C_{gs}$ and $C_{gd}$), but also modulates the electric field in the channel. K. Shinohara et al. reported $f_T$ value of 547 GHz in 30-nm gate pseudomorphic HEMTs by means of

multilayer cap structure to reduce parasitic source and drain resistances [4-5]. H. Matsuzaki et. al. have employed Tiered-Edge Ohmic structure and low-k benzocyclobutene (BCB) passivation to effectively minimize parasitic gate capacitance and achieve relatively high $g_m$ and $f_T$ values [4-6]. Although the results seemed rather promising, yet relatively complicated fabrication processes were involved in the reduction of the parasitic elements.

In this study, the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel HEMTs were fabricated with Pt buried gate technology. The adoption of Pt buried gate is because Pt can diffuse into the barrier layer and the channel can be further recessed [4-7 – 4-9]. The diffused gate has lower parasitic capacitance and resistance as compared to that of the recessed gate. Additionally, the Pt has higher metal work function (5.65eV) than that of Titanium (4.1eV). The measurement results in this study clearly evidenced that superior device performance can be achieved through very simple and straightforward gate sinking fabrication process with optimal epi structure as compared to those proposed in [4-5] and [4-6].

## 4.2 Experiment

The HEMT structure was grown by molecular beam epitaxy on a 2-in diameter InP substrate. The schematic of the structure is shown in Fig.1 and given as follows, a 50-Å InAs channel layer with 20-Å $In_{0.7}Ga_{0.3}As$ upper subchannel and 30-Å $In_{0.7}Ga_{0.3}As$ lower subchannel were grown on top of the 500-nm-thick InAlAs buffer layer. The $In_{0.7}Ga_{0.3}As$ sub-channels were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [4-10]. A 40-Å-thick InAlAs spacer, a Si-δ-doping with $5\times10^{12}$ $cm^{-2}$, a 10-nm-thick InAlAs barrier. A 4-nm-thick InP etching stop, and a 35-nm-thick InGaAs cap layer

with $2\times10^{18}$ $cm^{-3}$ Si-doping were grown on top of the composite channel layers.

For the device fabrication, the active area of the device was isolated by wet etch. The ohmic contacts were formed with 3 μm source-drain spacing by evaporating Au/Ge/Ni/Au on heavily doped n-InGaAs cap layer and then alloyed at 250°C for 25 second to attain low contact resistance ($R_c$). For the T-shaped gate process, it was performed by the 50kV JEOL electron beam lithography system (JBX 6000 FS) with trilayer e-beam resist. Succinic acid/$H_2O_2$/$NH_4OH$ solution was used for gate recess and then Pt (12nm)/Ti (60nm)/Pt (80nm)/Au (180nm) were deposited as Schottky gate metal and lift off by ZDMAC to form 80-nm T-shaped gate. The insert SEM image is the unpassivated T-shaped gate formed after recess. A 100-nm thick silicon nitride was deposited as passivation layer by PECVD at 250°C for 10 min. Finally, thermal annealing at 250°C for 3 minutes in forming gas ambient was carried out for gate sinking to further recess the channel. The contact resistance was 0.032 Ω • mm after gate sinking process, which remained almost unchanged as compared to that of 0.021 Ω • mm before annealing.

### 4.3 Result and Discussion

Fig. 2 shows the DC I-V curve of the device with 2×50 μm gate width using gate sinking technology. The device exhibited very good pinch-off characteristic and the saturation current of 1418 mA/mm at $V_{DS}$ = 1V and $V_{gs}$ = 0V as compared to the drain current of 1267 mA/mm for device before gate sinking showed in Fig. 3. This very high drain current density was mainly due to the superior electron mobility in the $In_{0.7}Ga_{0.3}As$/InAs/$In_{0.7}Ga_{0.3}As$ composite channel and the non-degrading performance of the ohmic contact during gate annealing. In addition, the gate sinking occurrence might cause the decrease of the drain current. In this studied, although the gate

sinking occurred, the drain current increased. The extracted values of source resistance Rs was 1.35 Ω for device without gate sinking compared to 1.22Ω for device with gate sinking. As a result, it is conclude that the reduction of parasitic resistance by the suppression of the formation of surface traps is the main reason for the performance enhancement of the device, because the increase in current is as high as 151 mA/mm [4-10]. As for the gate-drain breakdown voltage ($V_{DG,BR}$), the value decreased from 3.6V for device without sinking (Fig. 4a) to 2.4V for that with sinking (Fig. 4b), which is mainly due to the reduction in the Schottky barrier thickness after gate sinking process.

The transconductance $g_m$ and the drain source current plotted as functions of $V_{gs}$ for devices without and with gate annealing are included in Fig. 5. As is observed from the figure, the peak $g_m$ value has increased from 1470 mS/mm for the device without gate sinking to 1590 mS/mm for that with gate sinking, both measured at $V_{DS}$ = 0.5 V. This increase is mainly attributed to the sinking of Pt atoms into the InP etching stop layer which in turn shifted the gate metal front closer to the two-dimensional electron gas (2DEG) channel. Meanwhile, the threshold voltage shifted from -0.91 (without gate sinking) to -0.8 V (with gate sinking) when biased at $V_{DS}$ = 0.5V. The threshold voltage is defined as the $V_{gs}$ when $I_{ds}$ reaches 1mA/mm. A slight reduction in the gate leakage current from $1.66 \times 10^{-6}$ A (without gate sinking) to $6.3 \times 10^{-7}$A (with gate sinking) was also observed when biased at $V_{DS}$ = 0.8V and $V_{gs}$ = 0V owing to the increase in the thickness of the amorphous layer under gate which diminished the leakage path because of the reduction of the grain boundaries [4-8], [4-11].

The S-parameters of the 2×50 μm device were measured from 5 to 80 GHz using on-wafer probing system with HP8510XF network analyzer. Fig. 6 and Fig. 7 show the frequency dependence of the current gain $H_{21}$, the power gain MAG/MSG, and the

Mason's unilateral gain U of the device with/without gate sinking measured at $V_{DS}$ = 0.8V and $V_{gs}$ = -0.5V. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured S-parameters using the same method as in [4-12] and the equivalent circuit model in [4-13]. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have been carefully characterized through full-wave electromagnetic simulations with measurement. Standard gradient optimization routine with tolerance level of delta S less than 0.01% were set as the convergence criterion during the fitting process. The capacitance at the gate-source end was extracted to be 10.2 fF and the capacitance at the gate-drain end was about 8.6 fF. The extracted gate resistance was about 4Ω. A very high current gain cut-off frequency $f_T$ of 494 GHz and the maximum oscillation frequency $f_{max}$ of 390 GHz were obtained for device with sinking as compared to that of $f_T$ = 390 GHz and $f_{max}$ = 360 GHz for the device without sinking. This improvement in the RF performance was due to the increase of $g_m$ and the decrease of the gate-to-source capacitance ($C_{gs}$) in the applied gate bias range resulting from the gate sinking process. This decrease in $C_{gs}$ was also evidenced from the measured S-parameters (even before the removal of parasitic elements) where a $S_{11}$ contour with smaller "radius" with respect to the center of Smith Chart was observed as shown in Fig. 8, indicating a small capacitance value seen at the input port. Similar trend of reduction in ($C_{gs}$) values due to gate sinking process has also been observed in [4-14]. Table 4.1 summarizes the extracted intrinsic parameters for devices with and without gate sinking at same bias conditions. The increase in $f_T$ is mainly caused by the decrease of $C_{gs}$ and increase of the transcondutance.

The noise performances for devices with/without gate sinking at drain voltage biases $V_{DS}$ = 0.3 V, and $V_{DS}$ = 0.1 V are shown in Fig. 4-9 and 4-10 with frequency

range from 1 GHz to 17 GHz at optimum bias conditions. The measured minimum noise figures ($NF_{min}$) at 17 GHz were 0.82 dB and 1.19 dB for devices with gate sinking and without gate sinking at $V_{DS}$ = 0.3 V, respectively. In addition, the corresponding associated gains (Ga) were 14 dB and 10 dB, respectively. The ultra-low dc power dissipation for gate sinking device (without gate sinking) is 1.14 (1.32) mW/mm, respectively. These results show great potential for ultra-low power high frequency LNA applications.

The effect of gate sinking on the gate delay performance of the HEMT device is also evaluated. To avoid erroneous and physically meaningless values of logic parameters in characterizing such non-optimized threshold voltage device, we have followed the method proposed in [4-15]. A sub-threshold slope of 115mV/dec and Drain Induced Barrier Lowering (DIBL) of 200mV/V after gate sinking were obtained. For device without gate sinking, the subthreshold slope and DIBL were 115 mV/dec and 178 mV/V, respectively. Fig. 10 shows the calculated intrinsic gate delay (CV/I) as function of $I_{ON}/I_{OFF}$ ratio for the device with and without gate sink and with various choices of the threshold voltage as defined in [4-16] at $V_{DS}$ = 0.6V. As is observed from the figure, a low calculated gate delay of 0.78 psec for gate-sinking device with $I_{ON}/I_{OFF}$ ratio maintained in the order of $10^3$ was achieved as compared to that of 0.83 psec for the device without gate sink. The very low intrinsic gate delay performance is again attributed to the decrease in the $C_{gs}$ after the gate sinking process. These superior performances have also made such device a potential candidate for future high-speed and low-power logic applications.

### 4.4 Conclusion

In this paper, the use of the Pt buried gate technology for the enhancement of the

RF and logic performance of the HEMTs has been demonstrated. The HEMTs exhibit high $I_{ds}$ =1418mA/mm; high $g_m$ =1590 mS/mm, and a $f_T$ ($f_{max}$) of 494 GHz (390 GHz) after gate sinking. This is believed to be the highest value ever achieved for an 80 nm HEMT devices. In evaluating the devices for ultra-low DC power consumption LNA applications, the device exhibits the minimum noise figure at 17 GHz was 0.82 dB with corresponding associated gains 14 dB when biased at a $V_{DS}$ of 0.3 V.

Additionally, the logic performance of such device has also been characterized and a very low intrinsic gate delay (0.78 psec) with an $I_{ON}/I_{OFF}$ ratio in the excess of $10^3$ were obtained at $V_{DS}$ = 0.6 V. Overall, the performance improvement after gate sinking was mainly attributed to the increase of $g_m$ and the decrease in the corresponding capacitances of the device. The results demonstrate that superior HEMT device performance for high frequency, high-speed and low-power logic applications can be achieved through very simple gate sinking process with optimal epitaxy structure.

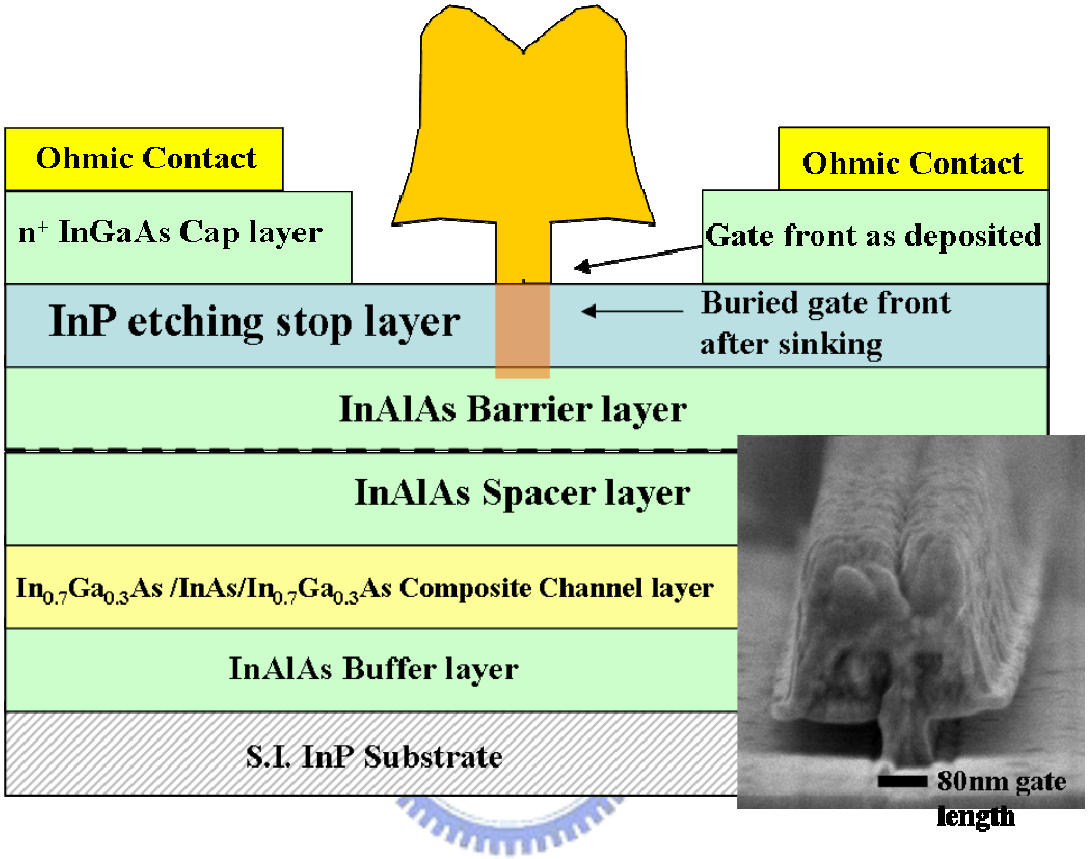



Fig. 4-1 The schematic view of the device structure and the insert SEM image is the 80-nm T-shaped gate after recess before silicon nitride passivation.

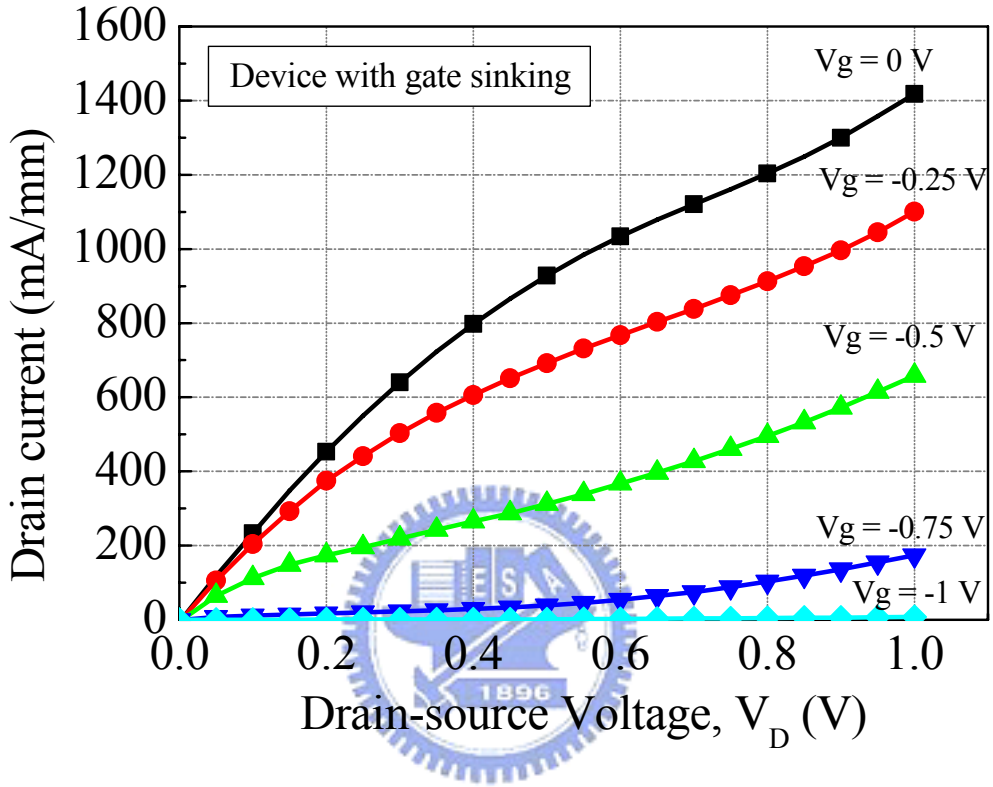



Fig. 4-2 Drain-source current versus drain-source voltage curve for device with gate sinking.

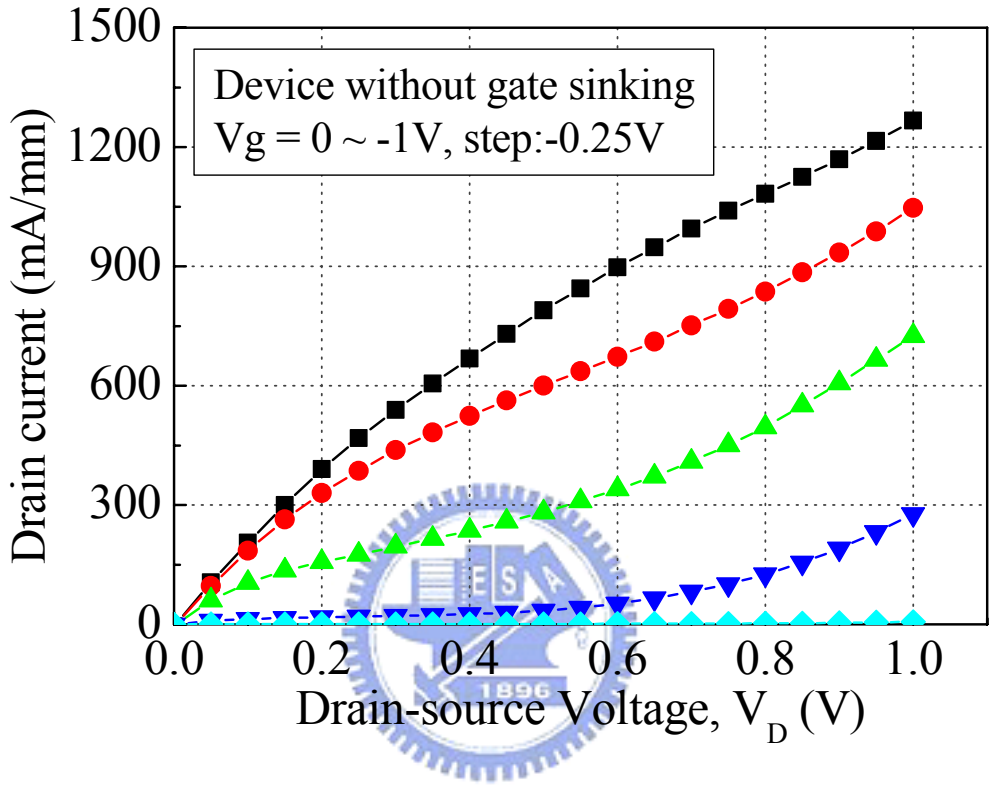



Fig. 4-3 Drain-source current versus drain-source voltage curve for device without gate sinking.

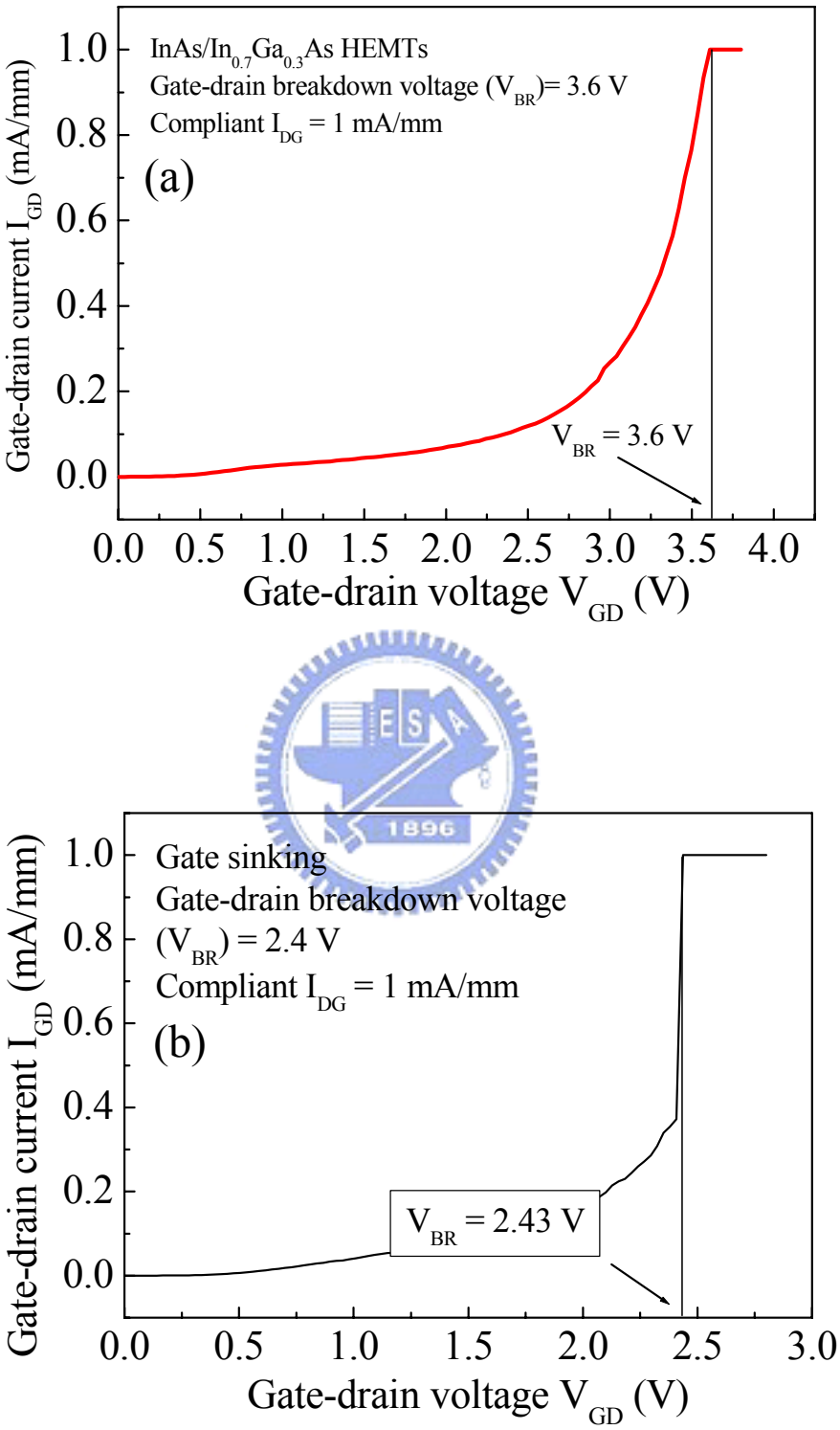



Fig. 4-4 Two terminal gate-to-drain breakdown characteristics of device with/without gate sinking

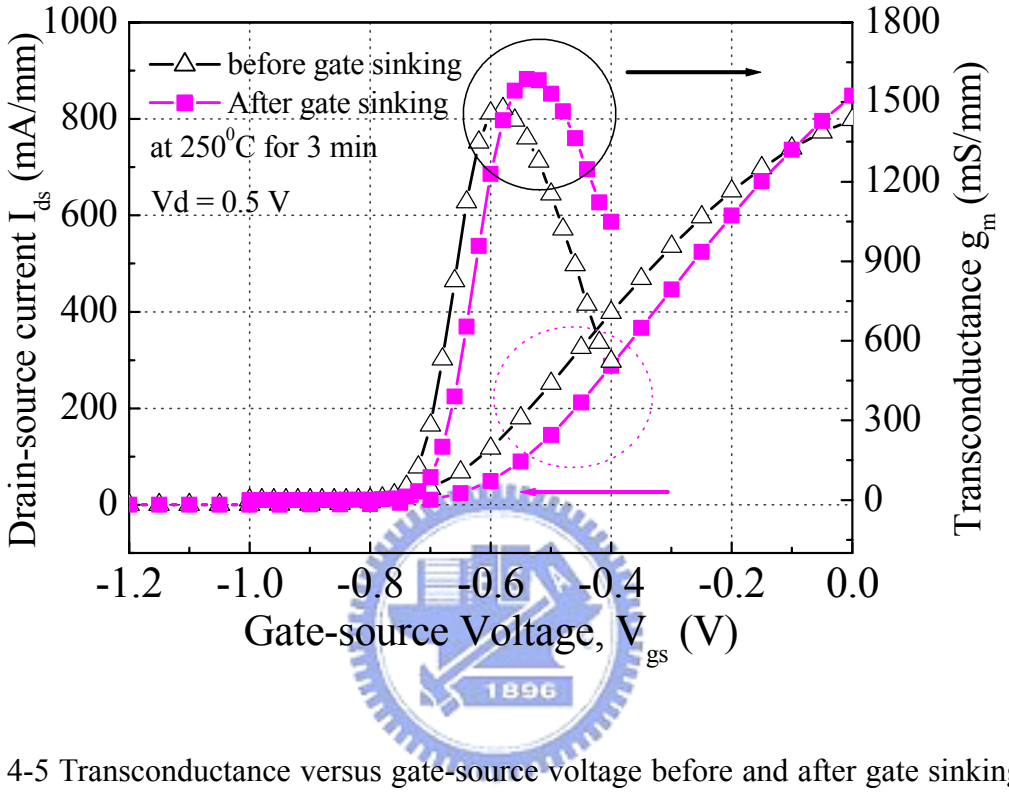



Fig. 4-5 Transconductance versus gate-source voltage before and after gate sinking at 250°C for 3 min.

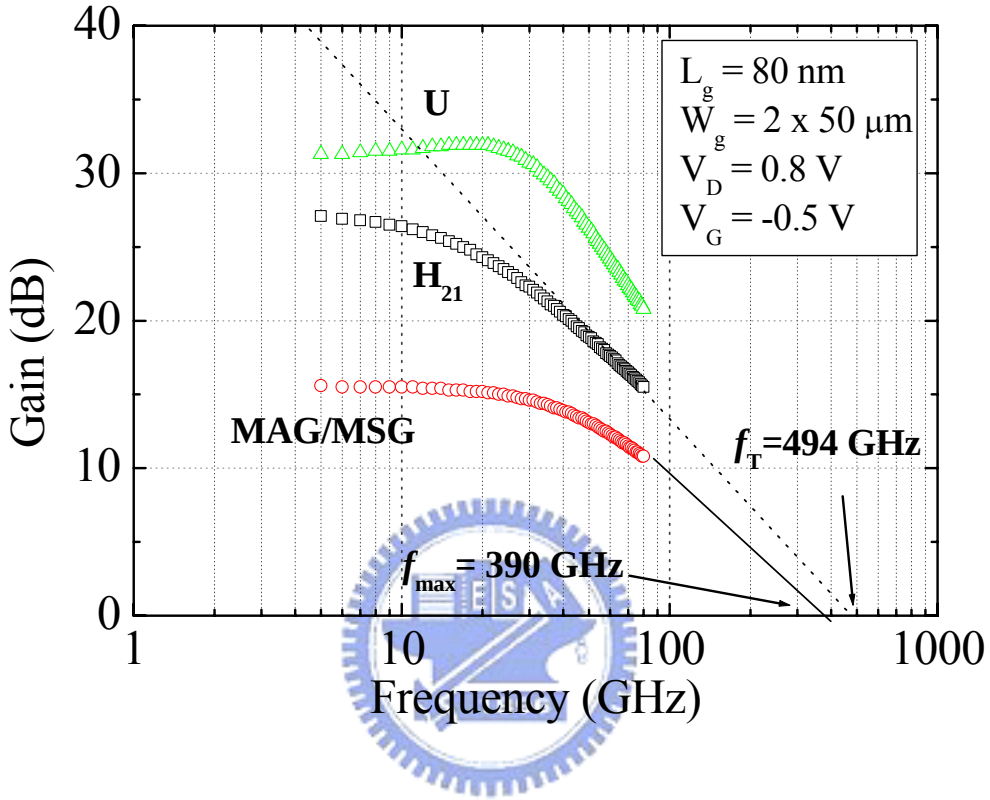



Fig. 4-6 Frequency dependence of the current gain $H_{21}$, the power gain MAG/MSG, and the unilateral gain $U$ of the InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs. The frequency range was from 5 to 80 GHz, and the device was biased at $V_{ds}$ = 0.8V and $V_{gs}$ = -0.5V.

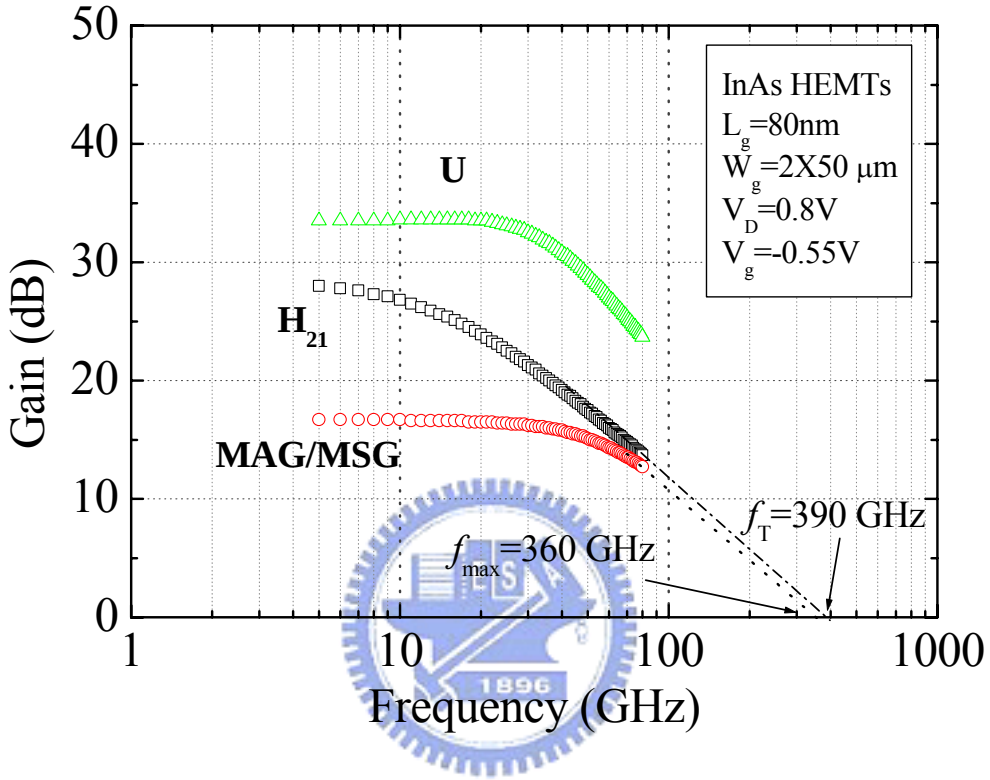



Fig. 4-7 Typical current gain $H_{21}$, MAG/MSG, and unilateral gain U as a function of frequency of the 0.08 × 100 μm$^2$ HEMTs before gate sinking.

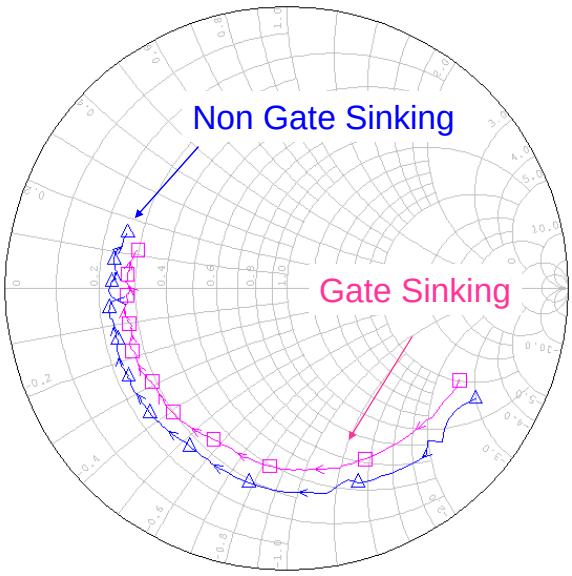



Fig. 4-8 Measured S11 of devices with and without gate sinking under the same bias condition. Note that this bias condition gives the smallest intrinsic gate delay for the devices.

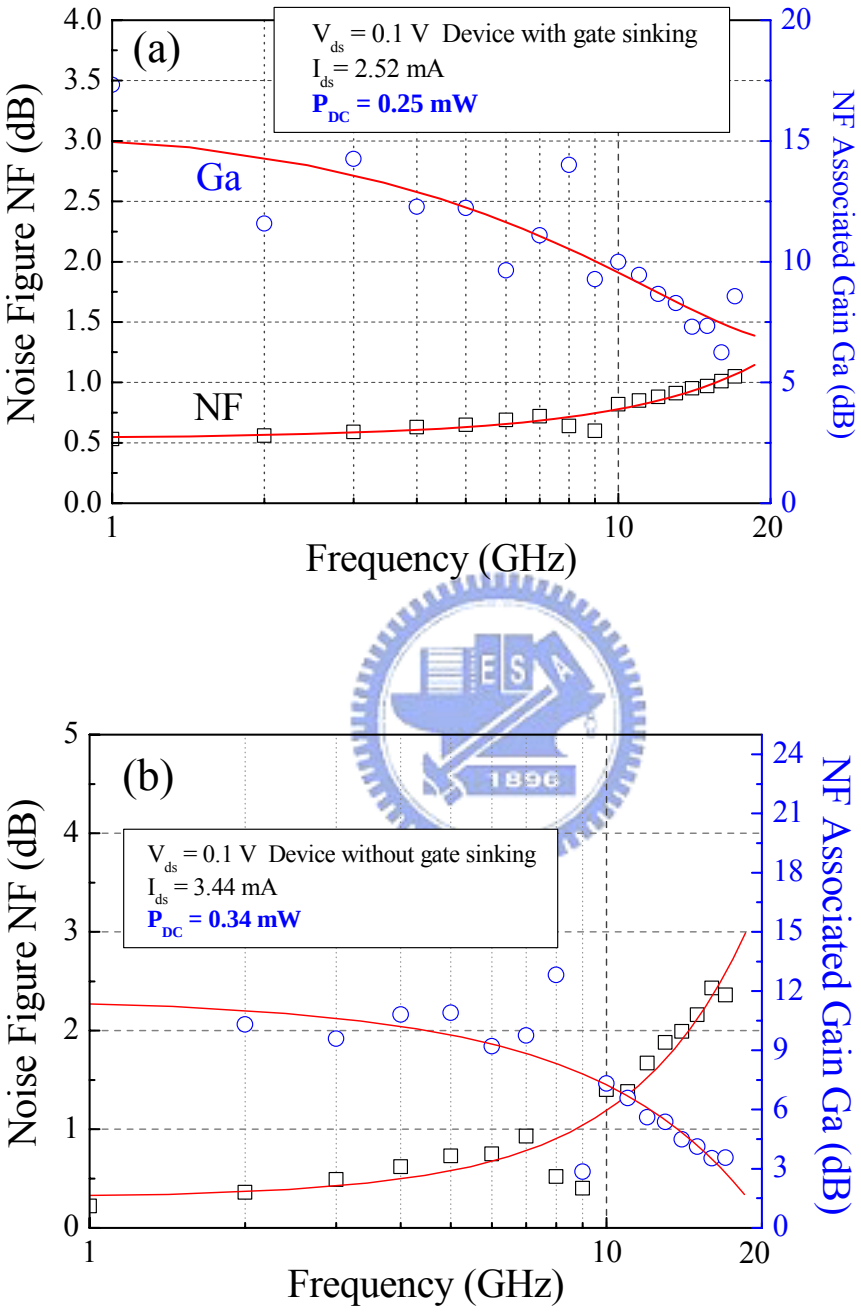



Fig. 4-9 Measured noise performance of the device at drain voltage $V_{DS}$ = 0.1V (a) device with gate sinking, $I_{ds}$ = 0.25 mA/mm (b) device without gate sinking, $I_{ds}$ = 0.34 mA/mm.

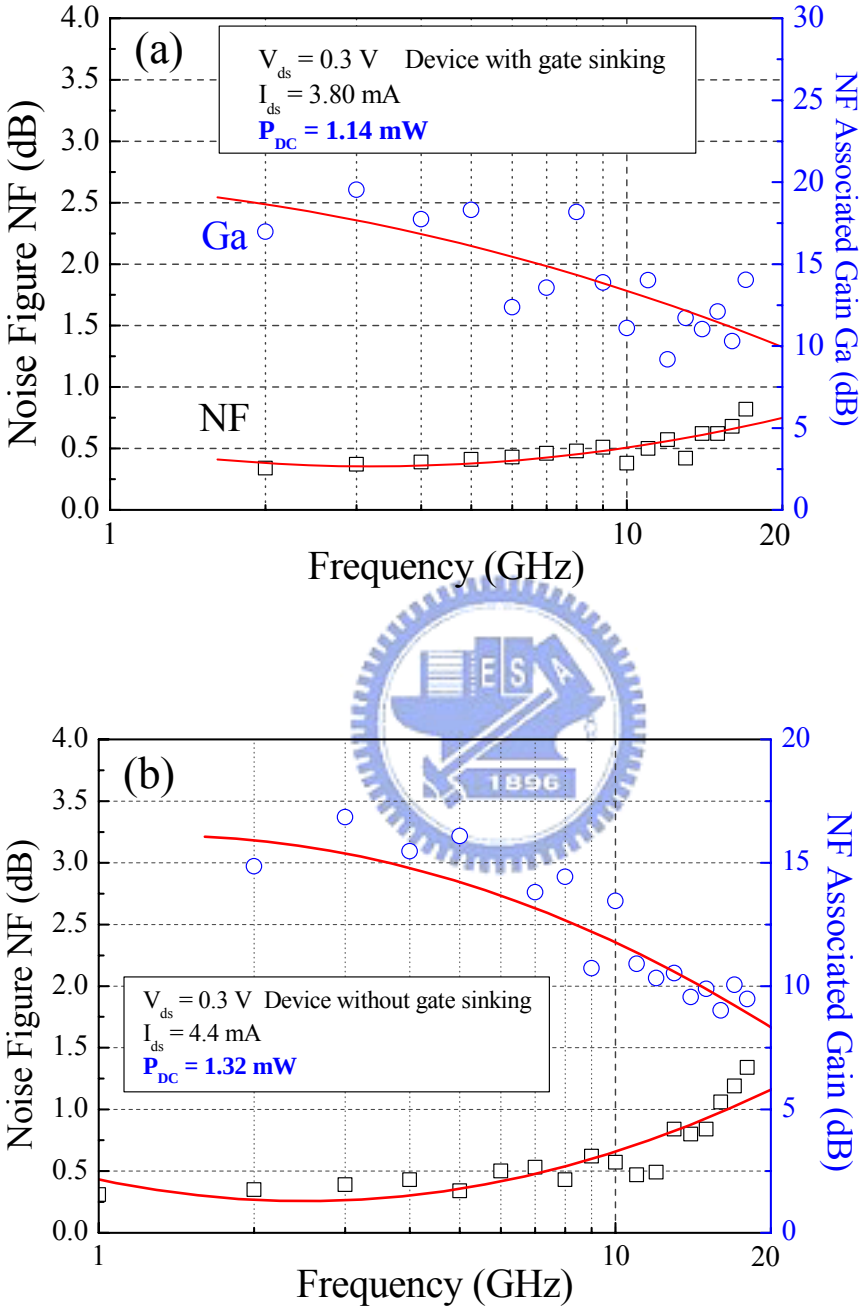



Fig. 4-10 Measured noise performance of the device at drain voltage $V_{DS}$ = 0.3V (a) device with gate sinking, $I_{ds}$ = 3.80 mA/mm (b) device without gate sinking, $I_{ds}$ = 2.52 mA/mm.

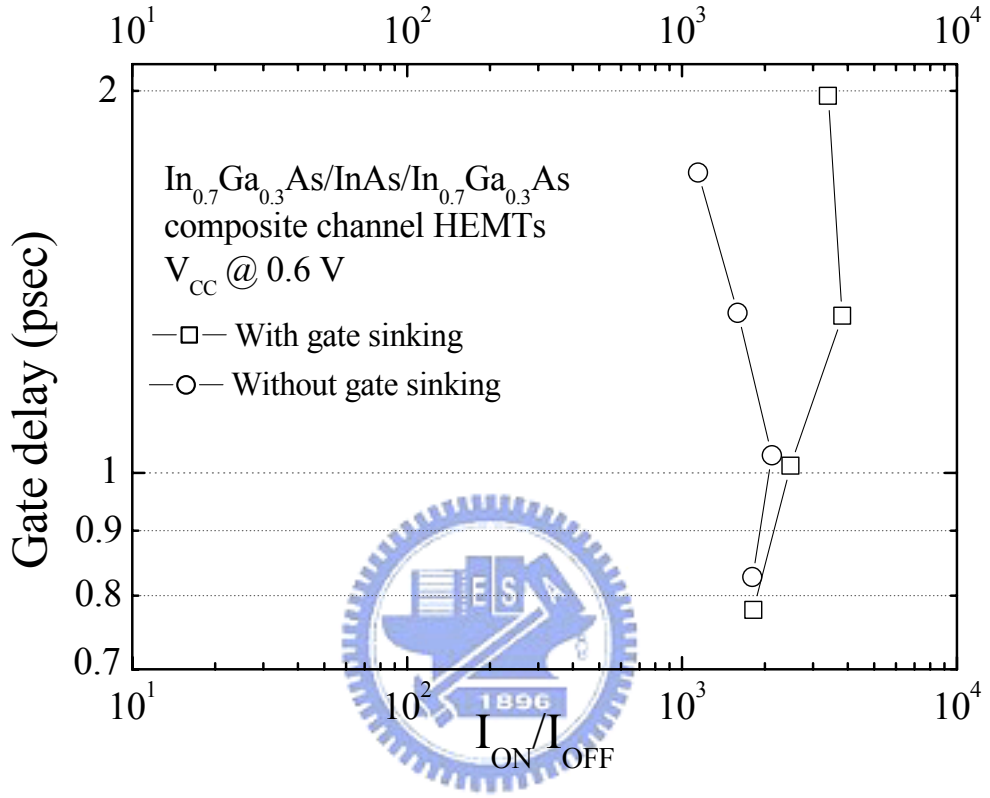



Fig. 4-11 The calculated intrinsic gate delay as a function of $I_{ON}/I_{OFF}$ ratio with various choices of the threshold voltage for device with/without sink.

Table 4.1 Summary of the HEMT device parameters with and without gate sinking.

| InAs/ $In_{0.7}Ga_{0.3}As$ HEMTs | $C_{gs}$ | $C_{gd}$ | $C_{ds}$ | $G_m$ (RF) | $f_T$ (GHz) | $f_{max}$ (GHz) |
|---|---|---|---|---|---|---|
| Without gate sinking | 73.3 fF | 16.3 fF | 5.3fF | 201mS | 390 GHz | 360 GHz |
| Gate sinking | 60.5 fF | 16.6 fF | 3.7fF | 208mS | 494 GHz | 390 GHz |

# Chapter 5

# InAs-Channel Based Quantum Well Transistors for High-Speed and Low-Voltage Digital Applications

## 5.1 Introduction

For device scaling in Si technology, the physical gate length of Si transistors used in the current 65 nm generation node is about 30 nm and the size of the transistor will reach 10 nm in 2011. The International Technology Roadmap of Semiconductors Winter Public Conference 2007 (ITRS 2007) also forecasted integration of planar III-V compound semiconductor FETs with Si technology is one of the promising solutions for the CMOS technology to extend Moore's law well into the next decade [5-1] – [5-5]. Generally, III-V materials have about 50 to 100 times higher electron mobility than Si and the resulting III-V-based transistors are showing very attractive merits over scaled Si MOSFETs. The extremely high transconductance and excellent RF performance have been demonstrated recently by InAlAs/InGaAs MHEMTs on GaAs substrate or InP substrate with ultra short gate length [5-6,5-7].

Low DC power consumption is always a highly desired property for practical system applications. However, maintaining device performance with low drain bias can only be achieved through optimized device technology which also plays a critical role for high-speed low-power digital applications. Having the properties of electron mobility as high as 20,000 $cm^2/Vs$ at room temperature, higher electron peak velocity, low electron effective mass and a reasonable energy bandgap (0.36 eV), InAs

materials have attracted numerous attentions as channel layer of Quantum Well FETs (QWFETs) for future high-speed and low-power digital applications [5-8].

In this letter, nano scale $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel QWFETs were fabricated and evaluated for high-speed and low-power digital applications. The devices demonstrated excellent DC, RF, and logic performances, indicating the suitability for ultra-high speed and low power digital applications.

## 5.2 Experimental

The epitaxial layer structure of the InAs-channel QWFETs was grown by molecular beam epitaxy (MBE) on 2-in InP substrate. Fig. 5-1 shows the detailed epitaxial structure of the 80 nm InAs-channel QWFETs in this study. The $In_{0.7}Ga_{0.3}As$ sub-channels were applied to enhance the electron confinement in the thin InAs layer and improve the electron transport properties [5-8]. An InP layer could provide a good gate etching stop layer as well as a good surface passivation of InAlAs layer to avoid kink effect and reduce the hot-electron surface damage [5-9]. Besides, with the use of the InP etching stop layer, the lateral recess length ($L_r$) can be easily controlled and RF performance can be improved [5-10,5-11]. The room temperature 2DEG density and electron mobility measured were $4.34\times10^{12}$ /cm$^2$ and 12,000 cm$^2$/Vs, respectively.

For the device fabrication, mesa isolation was done by a phosphoric based solution first. The device was etched to the buffer layer in order to attain a good isolation. After rapid thermal annealing of ohmic metal (Au/Ge/Ni/Au) in forming gas ambient, low ohmic contact resistance ($R_C$) and sheet resistance were achieved and measured by transmission line method. The values were 0.02 Ω • mm and 37.4Ω/□, respectively. A conventional tri-layer resist system of ZEP-520/PMGI/ZEP520 was used for the T-shaped gate fabrication by E-Beam lithography with double exposure

and double development. The recess etching was performed carefully using pH-adjusted solution of succinic acid (S.A.) and $H_2O_2$ mixture to selectively etch heavily doped cap layer over InP layer. After gate metal deposition, the T-shaped gate was formed by lift-off technique. The gate length of the T-shaped gate was 80nm with 2μm source-to-drain spacing achieved. Finally, a 100-nm thick silicon nitride was deposited as passivation layer by PECVD at 250 $^oC$ for 10 min. Special attention must be paid during the heat treatment process to avoid the degradation of the contact resistance values since these values are critical for high-speed low-power digital applications.

**5.3 Results and Discussion**

Fig. 5-2 shows the measured current-voltage characteristics of a 0.08 × 40 $\mu m^2$ device. As observed from the figure, this device can be well pinched off with a threshold voltage ($V_T$) of -0.81 V and the maximum drain-source current of 1015 mA/mm at $V_{DS}$ = 0.5 V and $V_{gs}$ = 0V. The threshold voltage is defined as the $V_{gs}$ when $I_{ds}$ reaches 1mA/mm. This very high drain current density was mainly due to the superior electron mobility in the $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel and the very low ohmic contact resistance. The transconductance $g_m$ and the drain source current versus $V_{gs}$ with various $V_{DS}$ are shown in Fig. 5-3. The maximum gm peak of the device at a $V_{DS}$ of 0.5 V was 1900 mS/mm. The extremely high transconductance was due to higher carrier concentration and superior electron transport properties in the InAs channel. Compared with $In_xGa_{1-x}As$ QWFETs, the $In_{0.52}Ga_{0.48}As$ QWFETs shows a transconductance of 823 mS/mm at $V_{DS}$ = 1.5 V and is shown in Fig 5-4. On the other hand, the transconductance of $In_{0.7}Ga_{0.3}As$ QWFETs is 1050 mS/mm at $V_{DS}$ = 1.5 V showing in Fig 5-5. The results clearly indicated that the InAs-channel

QWFETs can be biased at a low supply voltage to reduce overall dc power consumption, while maintaining relatively high current density and transconductance. The two terminal gate-to-drain breakdown voltage ($BV_{GD}$) was measured to be -2.5 V, defined at $I_{GD}$ = -1mA/mm.

The S-parameter of the device was measured using Cascade Microtech™ on-wafer probing system with HP8510XF vector network analyzer from 5 to 80 GHz. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system and the calibrated reference planes were at the tips of the corresponding probes. The parasitic effects (mainly capacitive) from the probing pads have been carefully removed from the measured S-parameters using the same method as in [12] and the equivalent circuit model in [13]. Since the geometry of the probing pads are relatively large compared to the device itself, the S-parameters of the open probing pads have also been rigorously characterized through full-wave electromagnetic simulations with measurement. The capacitance at the gate-source end and gate-drain end were extracted to be 13.9 fF and 10.3 fF, respectively. Before RF measurements, we must find the optimum DC bias to obtain the maximum current gain and power gain. Fig. 5-6 shows the $I_{ds}$ and $V_{DS}$ dependence of $f_T$ curves. From the figure, InAs device could exhibits exceeding 360 GHz at $V_{DS}$ = 0.5 V at the range of 200 mA/mm to 500 mA/mm. The current gain cutoff frequency ($f_T$) and maximum available (stable) gain (MAG/MSG) as a function of frequency are plotted in Fig. 5-7. The extracted current gain cut-off frequency $f_T$ and maximum oscillation frequency $f_{max}$ are 393 GHz and 260 GHz at drain bias of 0.5 V, respectively, by extrapolating $H_{21}$ and MAG/MSG with a -20 dB/decade slope. Apparently, the excellent $f_T$ is owing to the extremely high transconductance value. Moreover, the dc power dissipation was 5.8 mW when the device was biased at peak $f_T$ and $f_{max}$.

Care must be taken while biasing devices with such narrow energy bandgap values

since the occurrence of impact ionization will certainly degrade the performance of devices. Fig. 5-8 (a) shows the measured $H_{21}$ at 80 GHz as a function of drain voltages for InAs/$In_{0.7}Ga_{0.3}As$ channel HEMTs. It is obvious that $H_{21}$ has the highest gain at drain voltage 0.8 V and decreases when the bias voltage increases. The main reason is that the impact ionization occurred at $V_{DS}$ = 0.8 V and the generated electrons failed to keep up with the electronic field modulation at RF frequency, causing a drop in RF gain even at higher drain voltages. The gate current plotted as a function of gate voltage at different drain bias is shown in Fig. 5-8 (b). The dramatic increase in gate leakage current further evidenced the occurrence of impact ionization for biases higher than 0.8. This is because some holes produced during gate voltage increase transferred over the barrier to the gate region due to the impact ionization phenomenon.

The procedure as proposed by R. Chau, et. al [5-1] was adopted for the evaluation of digital performance of such non-optimized $V_T$ device to avoid possible erroneous and physically meaningless values of logic parameters. The on-state (off-state) current was defined as the $I_{ds}$ corresponding to a $V_{gs}$ 2/3 (1/3) of the difference between the drain bias and the threshold voltage. Fig. 5-9 shows the sub-threshold characteristics of the device with different drain biases. The Drain Induced Barrier Lowering (DIBL) and sub-threshold slope (SS) were calculated to be 200 mV/V and 115 mV/dec, respectively. The DIBL and SS for device with $In_{0.7}Ga_{0.3}As$ channel were 156 mV/V and 110 mV/dec, shown in Fig. 5-10.

The very important figure of merit for high speed operation of logic transistors, the intrinsic gate delay ($C_{total}V/I_{ON}$), has also been investigated. According to the definition, $C_{total}$ is the total gate capacitance including gate-to-source capacitance ($C_{gs}$) and gate-to-drain capacitance ($C_{gd}$) extracted from high-frequency S-parameter measurement at corresponding bias conditions. V and $I_{ON}$ are the applied drain

voltage and on-state current, respectively. As is observed from such definition, the gate delay is strongly dependent on the choice of the gate bias. The Lundstrom at Purdue university proposed this kind of methodology to explore suitability of novel devices with non-optimized $V_T$, as shown in Fig. 5-11. Thus, the extracted gate delay as a function of the gate bias, $V_T$' as defined by Lundstrom et al.[14], is shown in Fig. 5-12. It is observed that the device yields a very low intrinsic gate delay time of 0.54 psec at 0.5 V drain bias with $V_T$' = - 0.56 V. This very low intrinsic gate delay value is also attributed to the very high effective channel mobility. Fig. 5-13 shows the $I_{ON}/I_{OFF}$ current ratio as function of various $V_T$ as defined in reference 14. Peak $I_{ON}/I_{OFF}$ ratio in the excess of $10^3$ has been observed in the Fig. 5-13, indicating the excellent performance of such devices for high speed logic application.

The comparisons of 80 nm InAs QWFETs, 200 nm InSb QWFETs and advanced 40 nm Si MOSFET between gate delay and $I_{ON}/I_{OFF}$ ratio were plotted in the Fig. 5-14. The InAs QWFETs exhibits a far better $I_{ON}/I_{OFF}$ ratio than the InSb QWFETs while getting up to subpicosecond intrinsic speed at the same time. Furthermore, the gate delay of InAs or InSb QWFETs are very much dependent on the $I_{ON}/I_{OFF}$ as compared to the Si MOSFETs. This is mainly due to the off-state current of QWFETs determined by the gate leakage current. It was limited resulting from band-to-band tunneling (BTBT) in such small energy band gap and lower effective conductivity mass (m*). Therefore, the use of a high-k gate dielectric between the metal gate and the III-V device layers will eliminate such gate leakage and potentially improve the $I_{ON}/I_{OFF}$ ratio [15].

Cutoff frequency ($f_T$) versus DC power consumption of the 80 nm device under different drain biases are plotted in Fig. 5-15 with the published data [16] of 80 nm Si MOSFETs biased at 0.7 V also included for comparison. We can conclude from the plot that InAs channel-based QWFETs can achieve higher $f_T$ under the same level of

DC power consumption since the InAs channel can provide better electron transport properties. Fig. 5-16 shows the comparison of delay time as a function of gate length for different device technologies [5-1,5-3]. It is clear that InAs QWFETs exhibit lower gate delay than the state-of-the-art Si n-channel MOSFETs when compared at the same gate length.

Finally, to further improve the $I_{ON}/I_{OFF}$ ratio, a suitable high-k material and metal gate stack for QWFETs can reduce the gate leakage current effectively. The I-V characteristics of the Metal-Insulator-Semiconductor QWFETs capacitor were compared with those of the schottky metal gate QWFETs formed on the same epiwafer, as shown in Fig. 5-17. As seen from the plot, the insulated gate structure reduced the leakage current by more than 5 orders of magnitude under a negative bias and 9 orders of magnitude under a positive bias compared to schottky metal gate.

## 5.4 Conclusion

The 80 nm $In_{0.7}Ga_{0.3}As$ /InAs/$In_{0.7}Ga_{0.3}As$ composite channel QWFETs have been fabricated and evaluated its for high-speed low-power digital applications. The device exhibited high $I_{ds}$ =1015 mA/mm; high gm =1900 mS/mm, and a $f_T$ ($f_{max}$) of 393 GHz (260 GHz) at low drain bias voltage ($V_{DS}$ = 0.5 V). Additionally, a very low intrinsic gate delay of 0.54 psec was achieved due to the superior transport properties of the InAs channel. The InAs QWFETs exhibit better $I_{ON}/I_{OFF}$ performance than InSb QWFETs at an equivalent gate delay. With further combination of high-k dielectric and schottky metal gate, the off-state current could be reduced significantly. These results demonstrated that the InAs channel-based QWFETs have great potential for high-speed and low-power digital applications and are potential candidates for applications in post-Si generations.

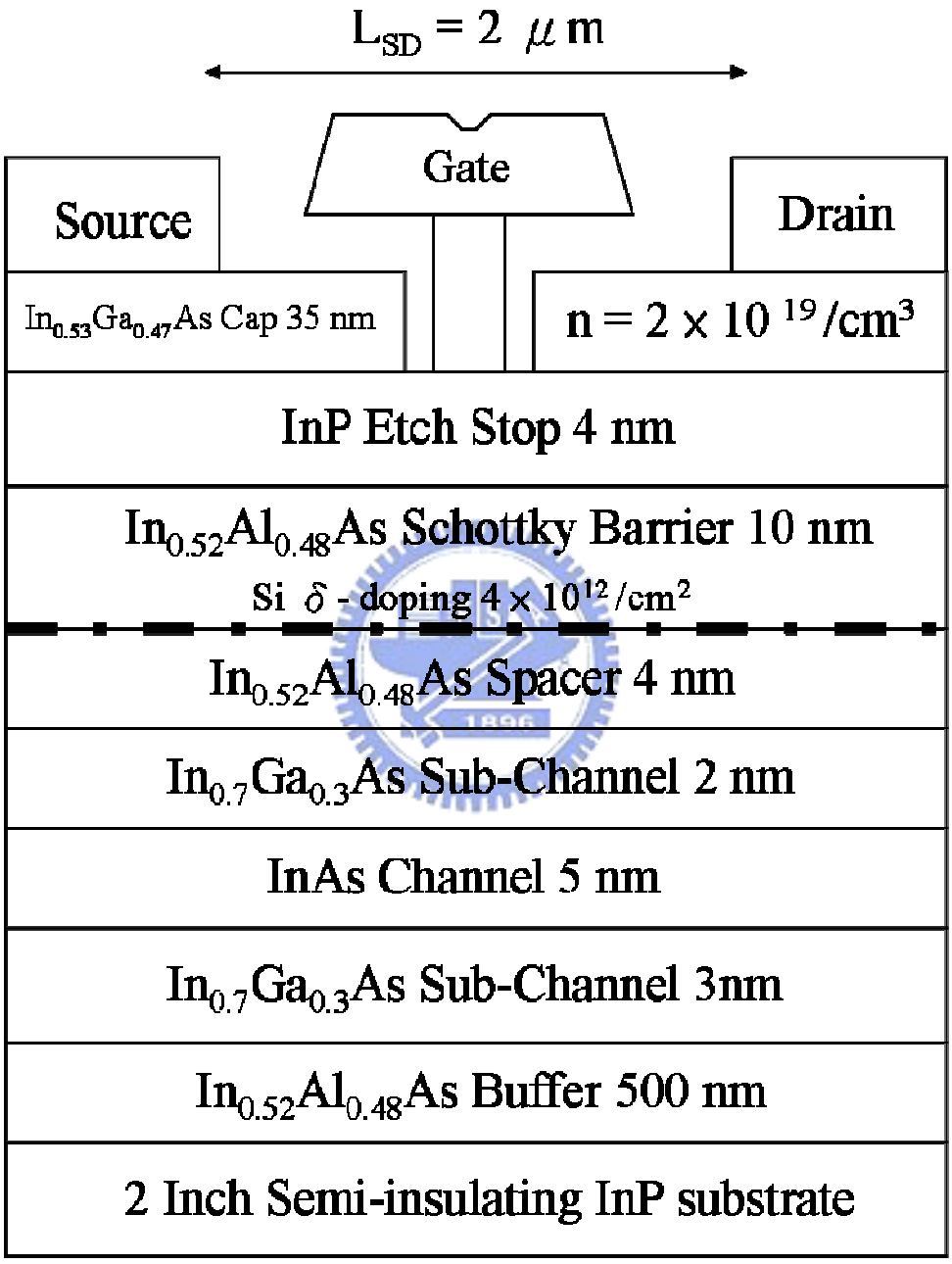



Fig. 5-1. Epitaxial layer structure of the InAs/$In_{0.7}Ga_{0.3}As$ HEMTs.

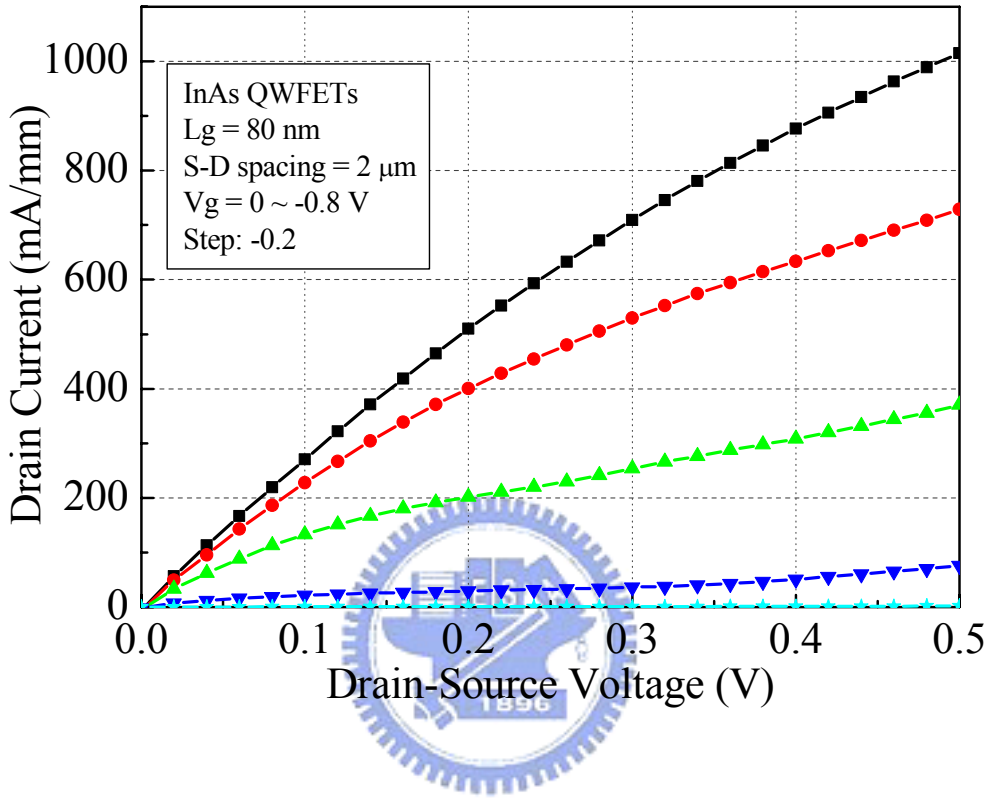



Fig. 5-2. Drain-source current versus drain-source voltage curve

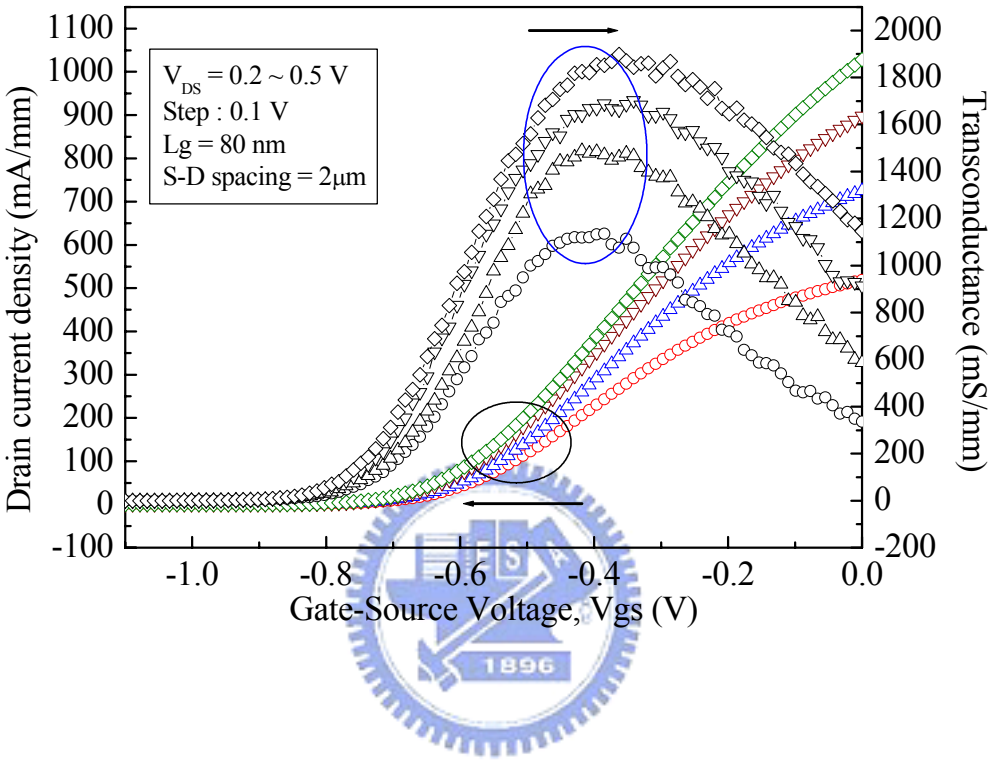



Fig. 5-3. Current-voltage characteristics at different $V_{DS}$ of 0.08 × 40 $\mu m^2$ QWFETs.

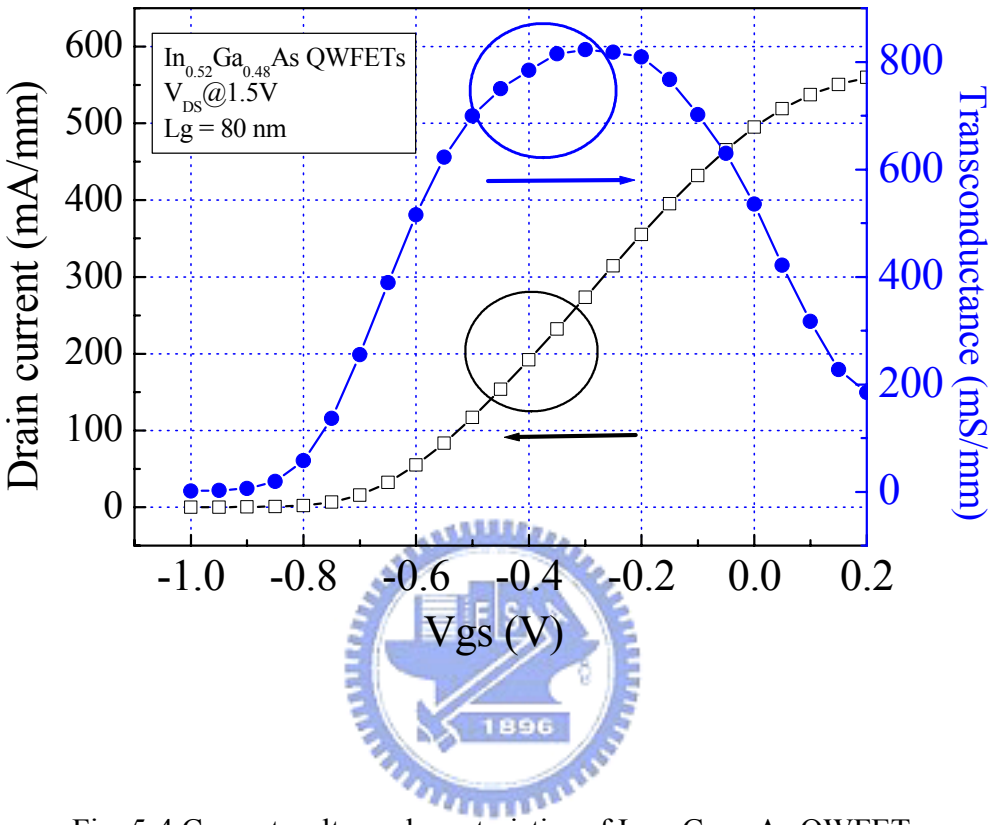



Fig. 5-4 Current-voltage characteristics of $In_{0.52}Ga_{0.48}As$ QWFETs.

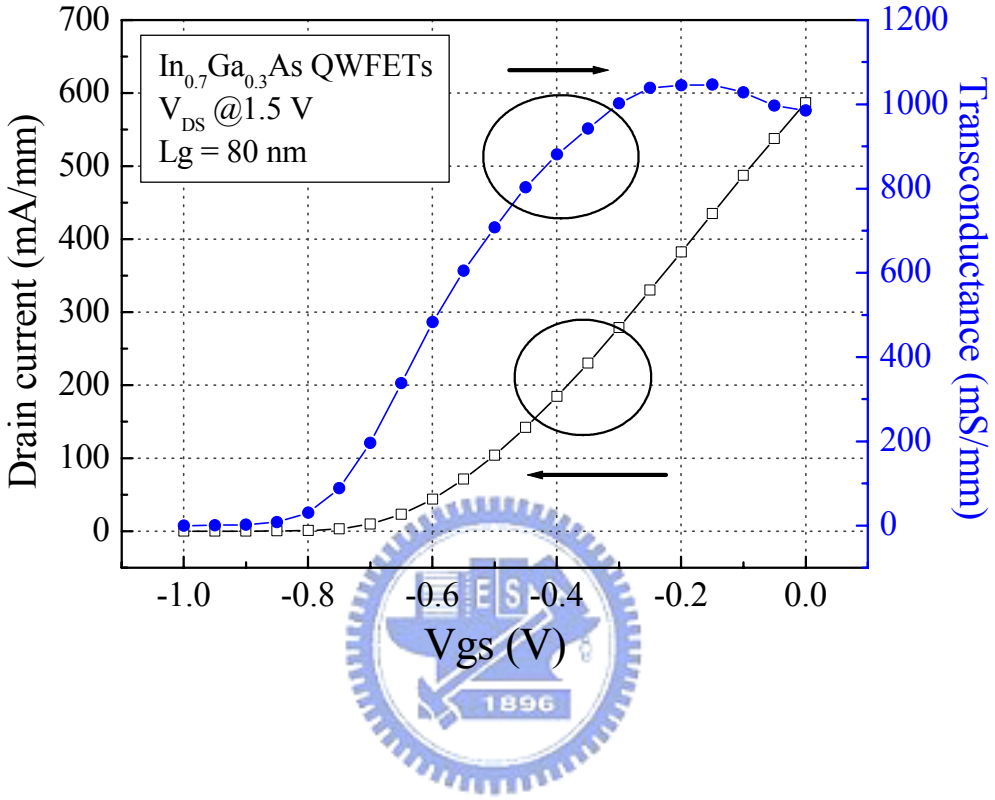



Fig. 5-5 Current-voltage characteristics of $In_{0.7}Ga_{0.3}As$ QWFETs.

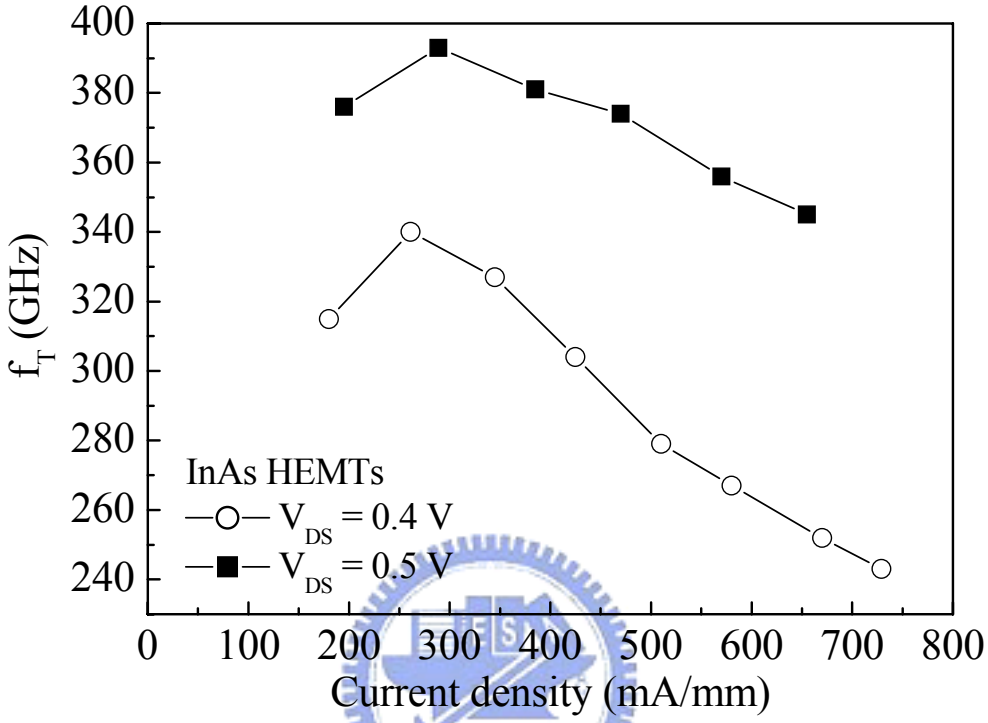



Fig. 5-6. Cutoff frequency vs. $I_{ds}$ and $V_{DS}$ of InAs HEMTs

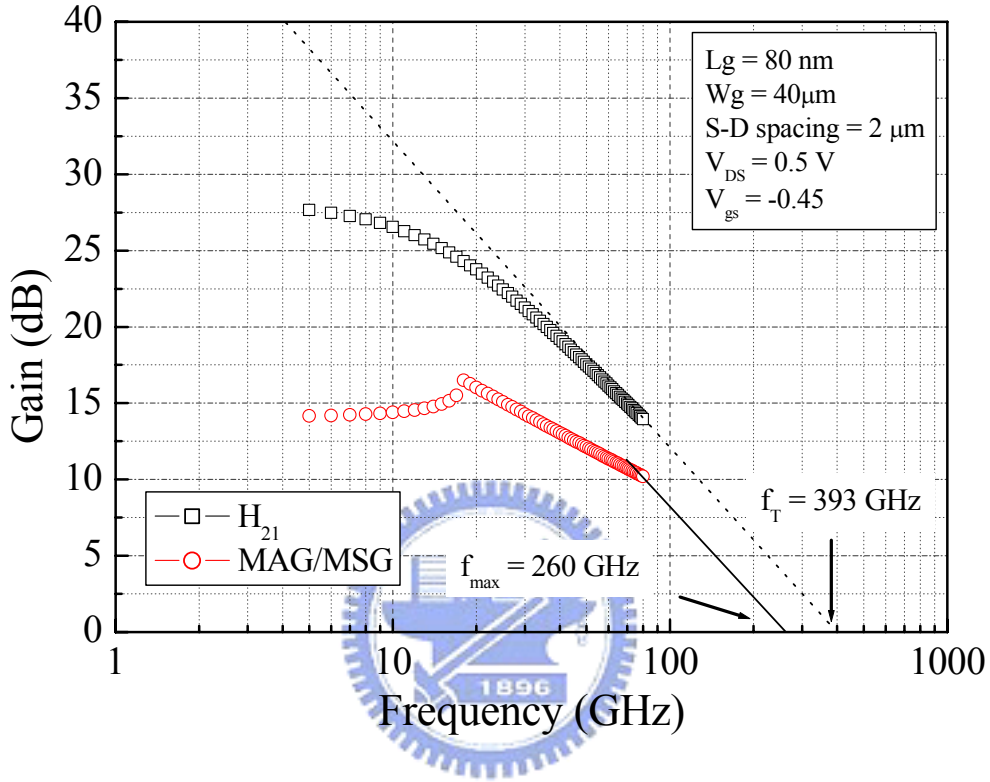



Fig. 5-7. Frequency dependence of the current gain $H_{21}$, and the power gain MAG/MSG of the InAs/$In_{0.7}Ga_{0.3}As$ composite channel QWFETs. The frequency range was from 5 to 80 GHz, and the device was biased at $V_{DS}$ = 0.5 V and $V_{gs}$ = -0.45 V.

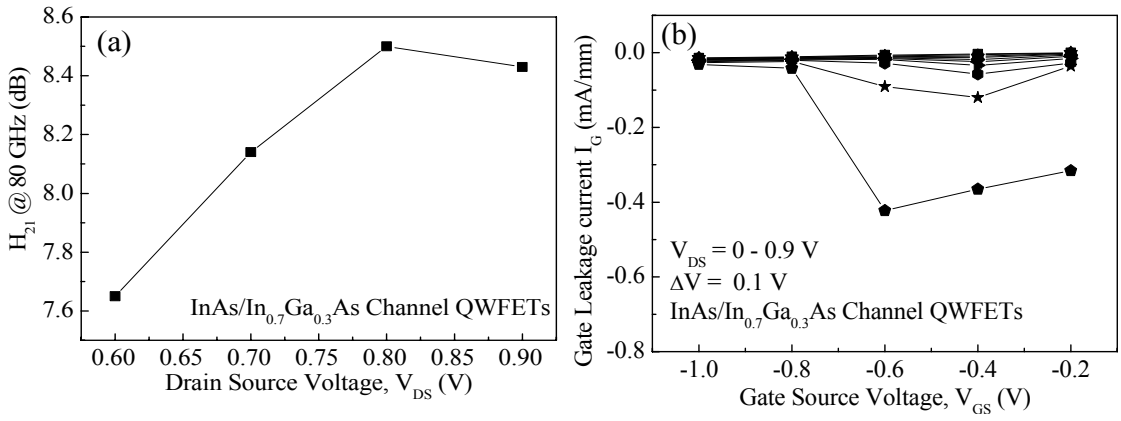



Fig. 5-8. $InAs/In_{0.7}Ga_{0.3}As$ Channel HEMTs (a) Plot of $H_{21}$ measured at 80 GHz versus drain-source voltage of $0.08 \times 100\ \mu m^2$ (b) Gate current $I_G$ plotted as a function of $V_G$ at different $V_{DS}$ from 0 V to 0.9 V.

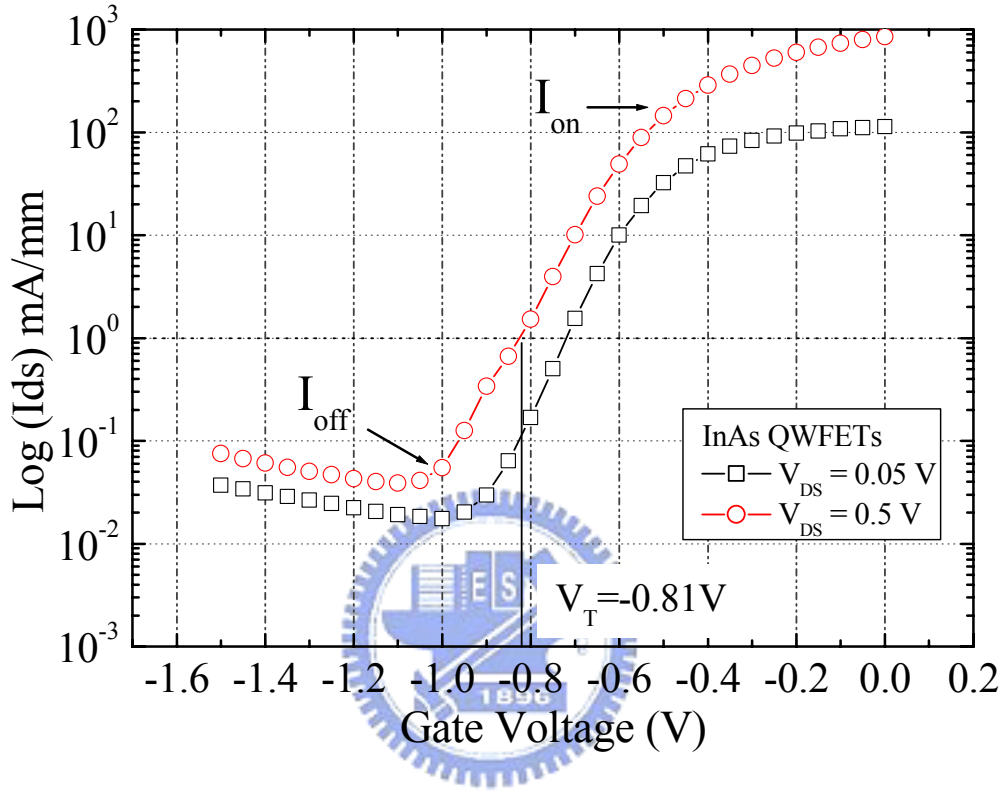



Fig. 5-9. The sub-threshold characteristics of the device with InAs channel at the $V_{DS}$ of 0.05 and 0.5V.

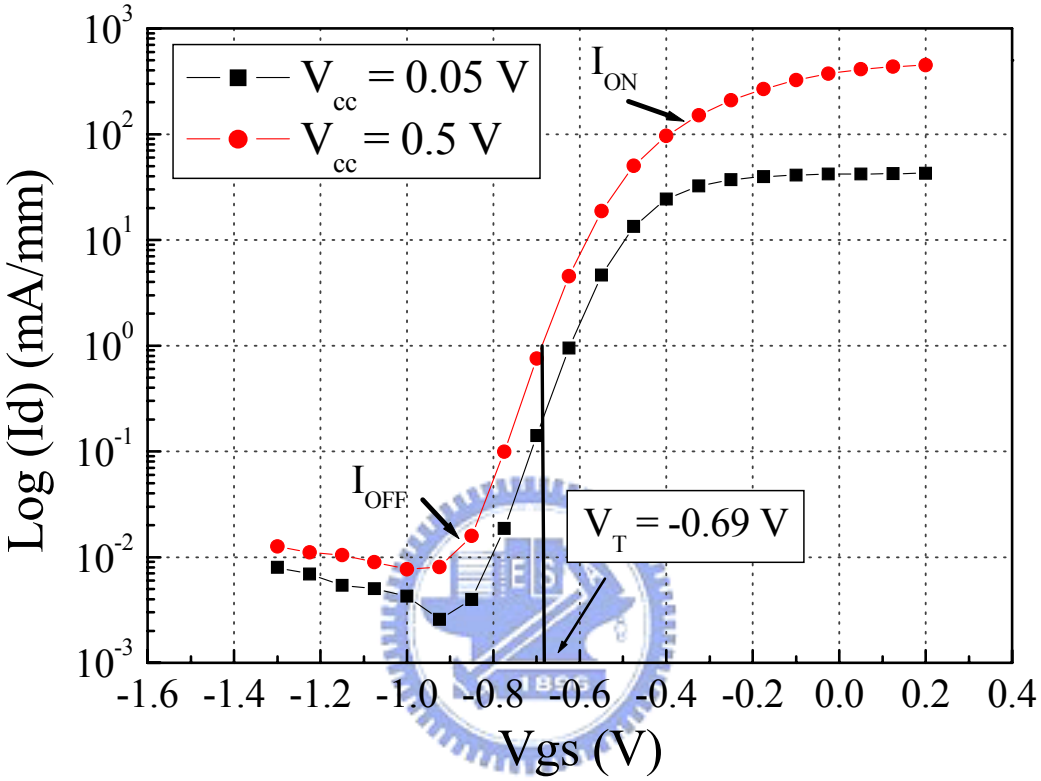



Fig. 5-10. The sub-threshold characteristics of the device with $In_{0.7}Ga_{0.3}As$ channel at the $V_{DS}$ of 0.05 and 0.5V.

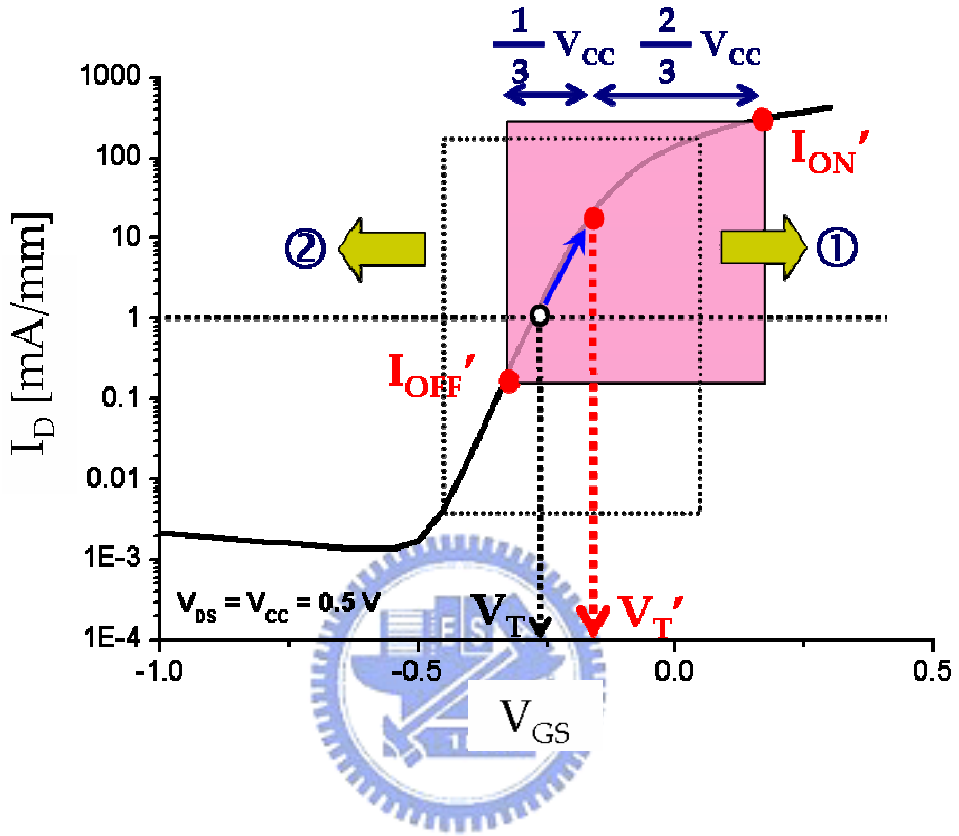



Fig. 5-11. The methodology for the evaluation of the logic performance of novel devices with non-optimized $V_T$. Different definitions of $V_T$ result in a new set of logic parameters of C'V'/I'.

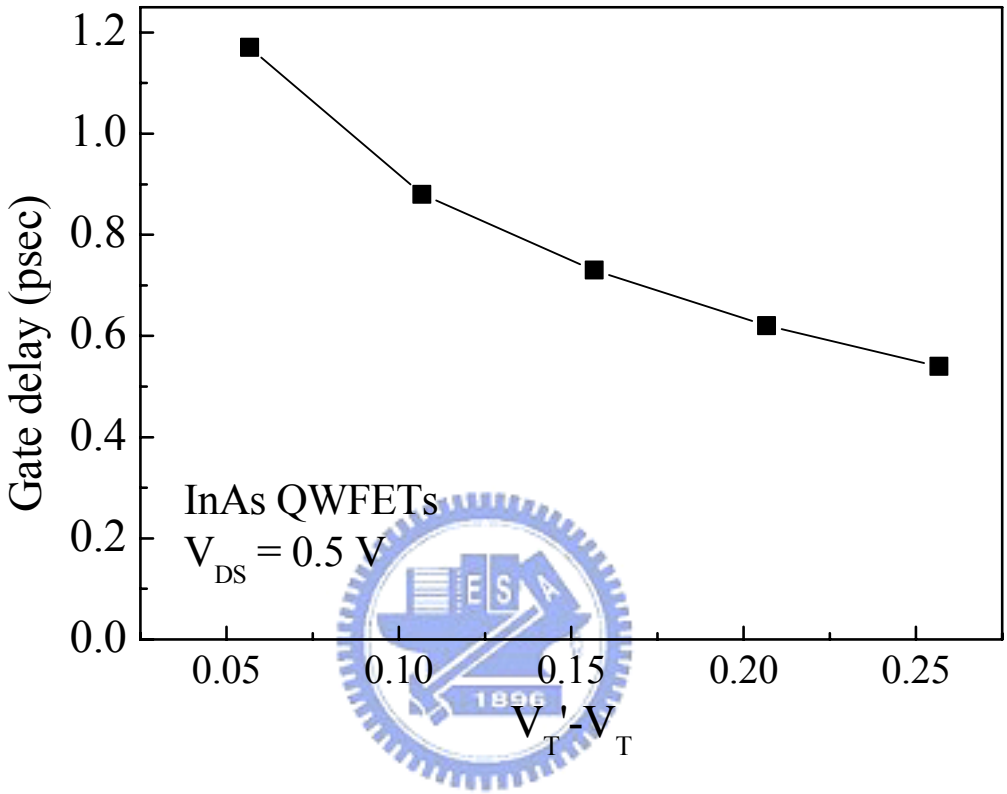



Fig. 5-12. Gate delay as a function of the selected threshold voltage.

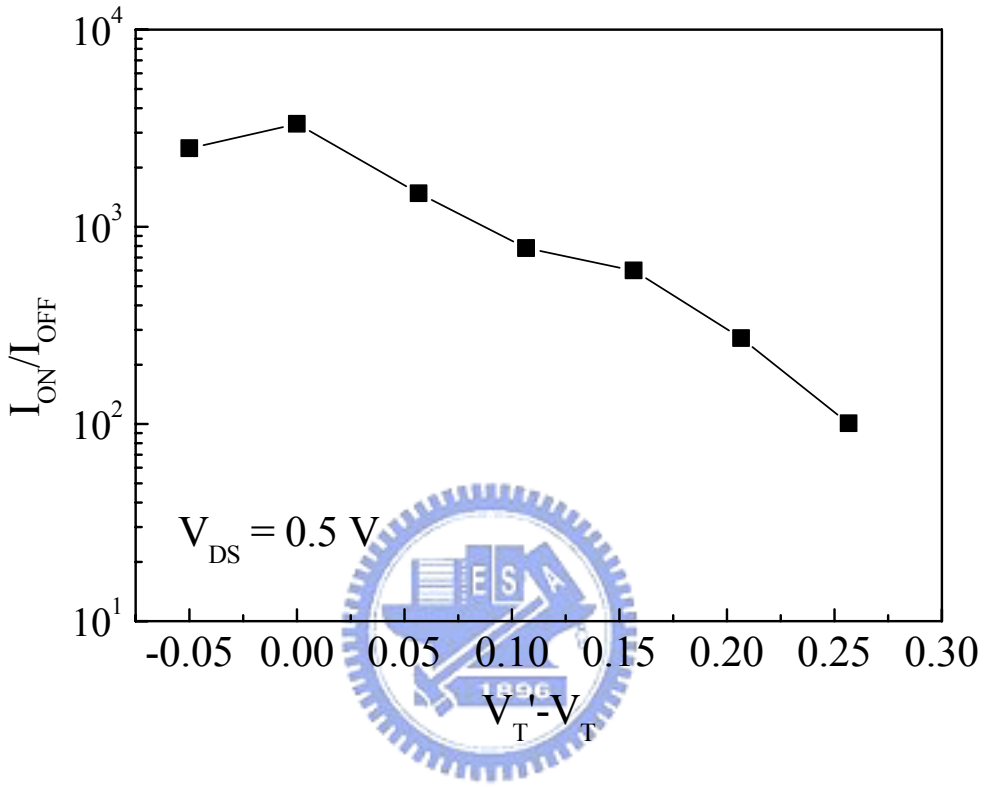



Fig. 5-13 $I_{ON}/I_{OFF}$ ratio as function of various $V_T$ at the drain voltage 0.5 V.

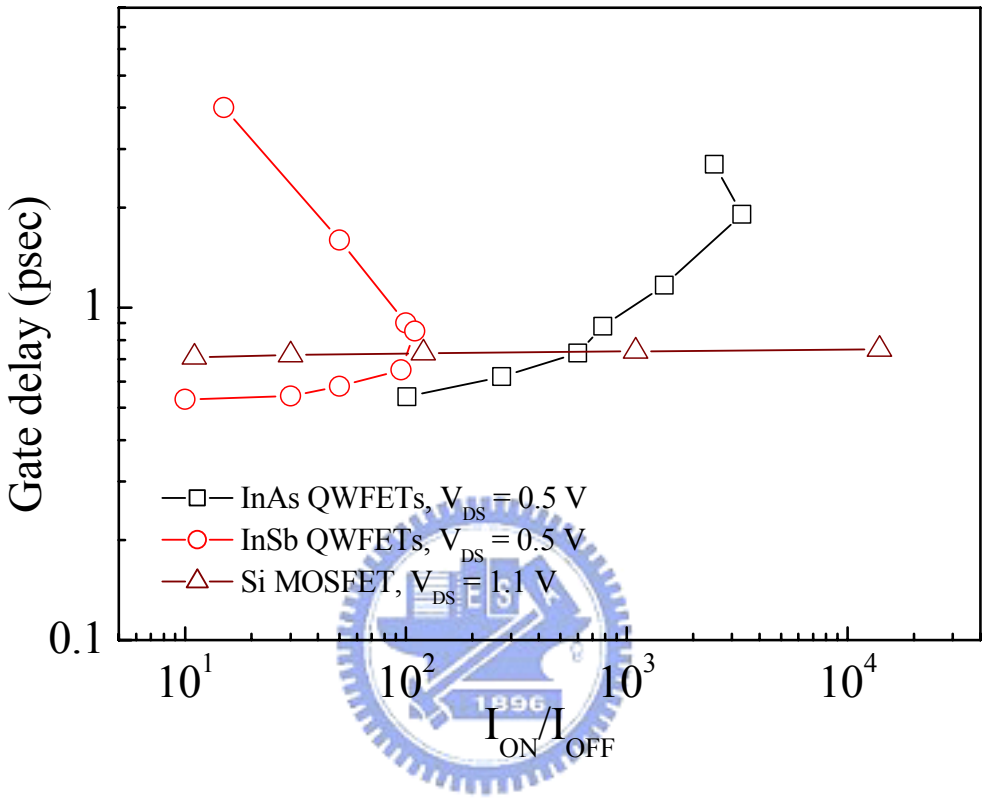



Fig. 5-14 Comparison between gate delay and $I_{ON}/I_{OFF}$ of 80 nm InAs QWFETs, 200 nm InSb QWFETs and 40 nm Si MOSFETs.

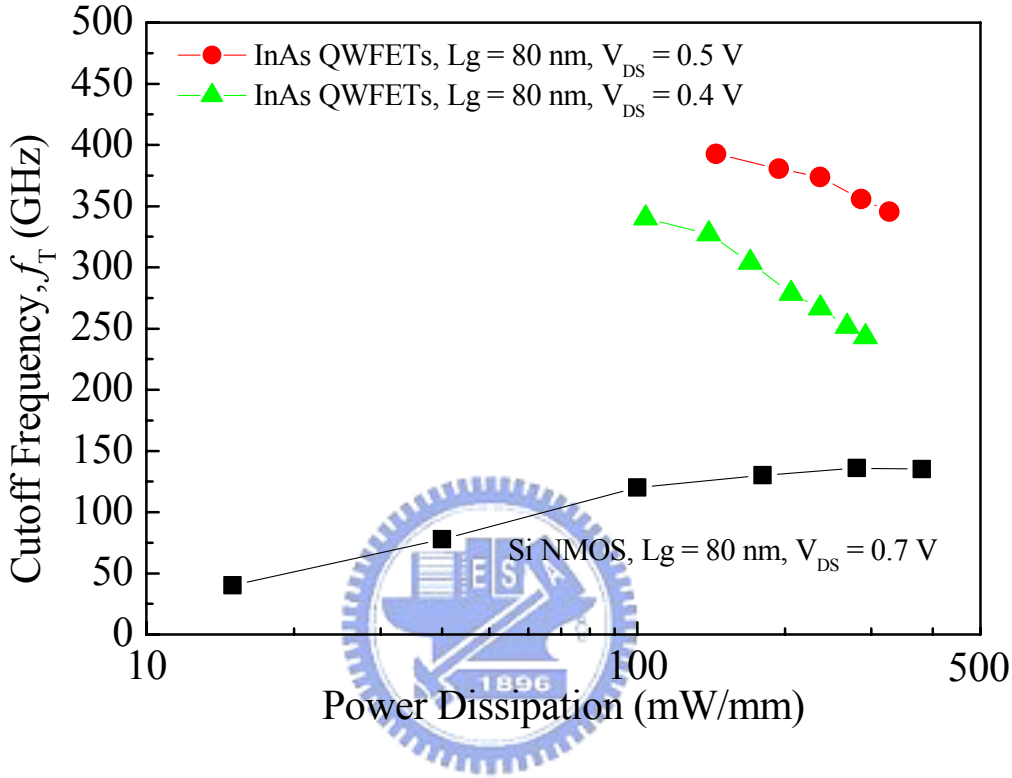



Fig. 5-15. Cutoff frequency of InAs QWFETs and 80 nm Si MOSFETs as a function of the power dissipation

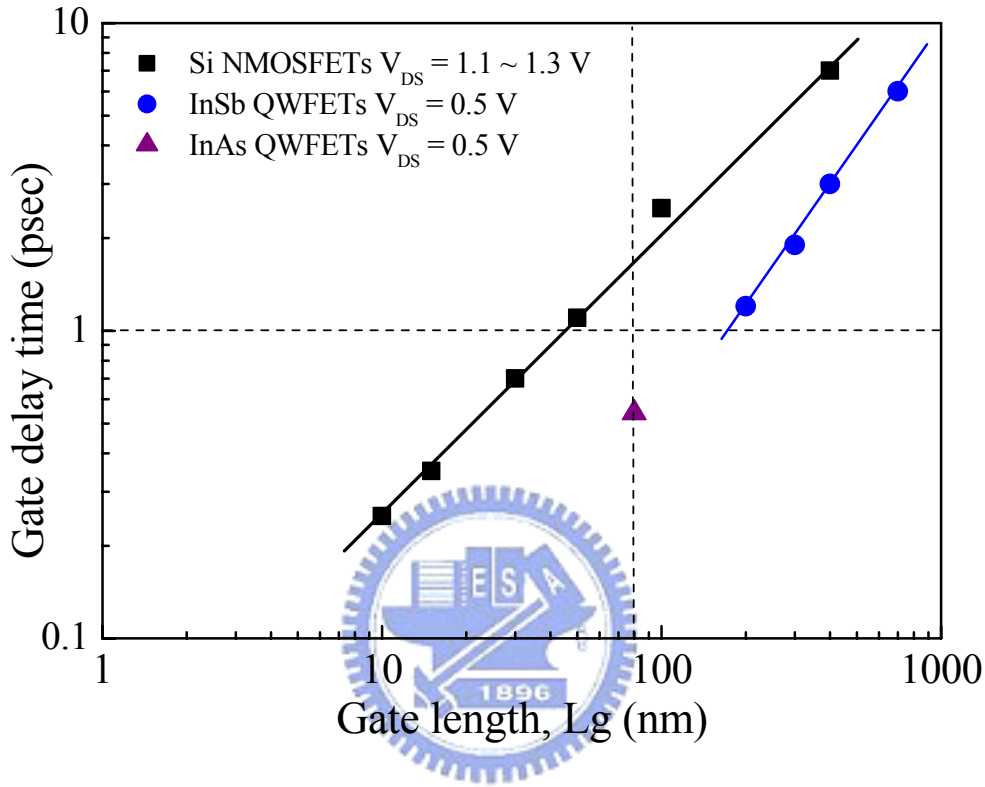



Fig. 5-16. Gate delay of InAs, InSb QWFETs and Si NMOSFETs as a function of gate length.

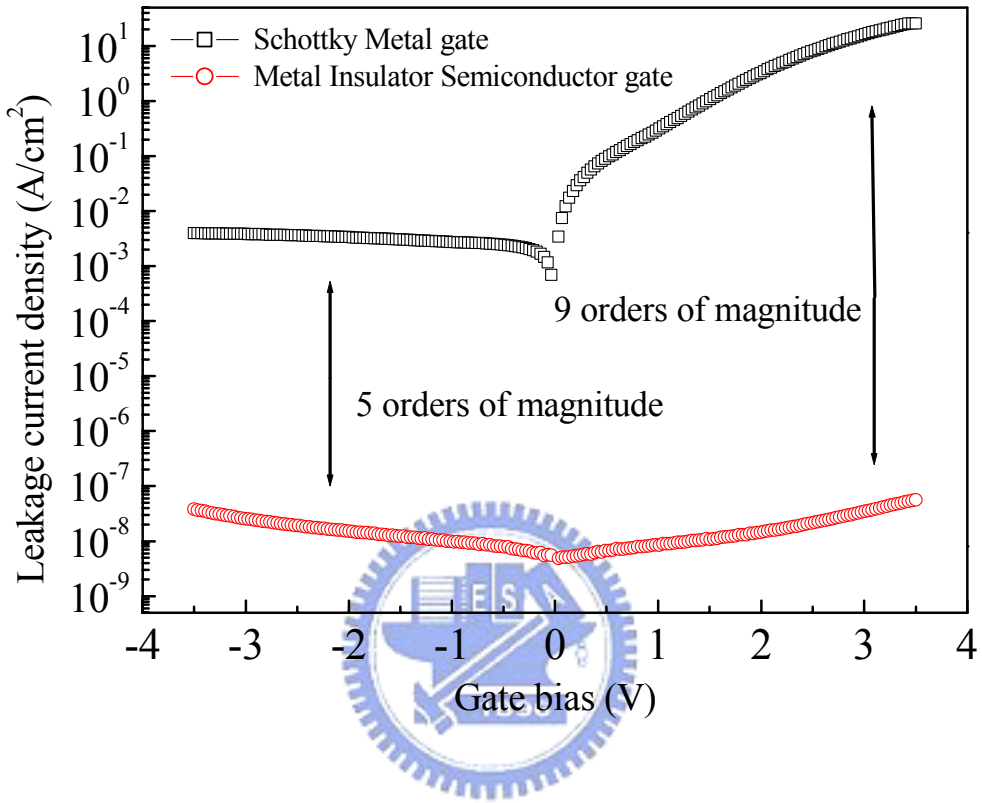



Fig. 5-17. I-V characteristics of MIS QWFETs and Schottky metal gate QWFETs.

# Chapter 6

# Metamorphic $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Structure on a GaAs Substrate with $ZrO_2$ High-k Dielectrics

## 6.1 Introduction

The downscaling of complementary metal-oxide-semiconductor (CMOS) devices in the past few decades has followed Moore's law. Si-based MOS device technology has moved into the deep sub-nanometer generation phase. However, in the 21st century, it has approached its intrinsic mobility limits for Si technology beyond a 22 nm node. In recent years, III-V compound semiconductor devices, such as $In_xGa_{1-x}As$-based quantum-well field-effect transistors (QWFETs), have attracted considerable attention for high-speed digital applications because of the high electron mobility of the III-V materials [6-1,6-2]. As a result, III-V-based devices are considered very promising alternatives to the current Si-based devices.

To date, silicon dioxide, silicon nitride and alumina have been investigated as gate insulators on III-V materials. However, the high dielectric permittivity of ε～25, large band gap of $E_G$ ～ 7.8 eV, good thermal stability, high hardness and high melting point have made zirconium dioxide ($ZrO_2$) an ideal candidate as the gate oxide for III-V materials [6-3,6-4]. However, unlike the stable interface between Si and silicon dioxide in a Si MOS structure, there is no high-quality insulator suitable for compound semiconductors. Consequently, for the deposition of insulator film on III-V materials, an appropriate surface passivation process is required to diminish the

surface state and to prevent air exposure of the semiconductor surface. Many studies have shown that chemical treatment with sulfur compounds can reduce the GaAs or germanium surface-state density and control the Fermi-level position [6-5]-[6-8]. Moreover, it has also been reported that the sulfur absorption of the Ga-terminated surface plays an important role in reducing the energy states within the bandgap and in enhancing the resistance against oxidation during further process flow [6-9]. In this letter, the MOS capacitor structure consisting of a metamorphic $In_{0.53}Ga_{0.47}As$ layer grown on a GaAs substrate with a thin high-k $ZrO_2$ film is discussed. The $In_{0.53}Ga_{0.47}As$ lattice-matched to an InP was grown on a GaAs substrate using an InAlAs metamorphic buffer. By using a buffer layer, the epilayers can be grown on GaAs substrates with a substantial reduction in cost, reduced brittleness and increased size. The $In_{0.53}Ga_{0.47}As$ material possesses high peak velocity and has a high electron mobility of 13,000 $cm^2/(V \cdot s)$, which is eight times higher than that of Si. Different surface pretreatments for $In_{0.53}Ga_{0.47}As$ before $ZrO_2$ deposition were investigated in an attempt to improve the oxide/semiconductor interface quality and MOS characteristics. From the experimental results, the sulfur-treated capacitors demonstrated better capacitance-voltage characteristics and a lower leakage current than the HCl-treated capacitors. These advantages are beneficial for the manufacture of MOS-based III-V semiconductor devices.

## 6.2 Experimental

MOS capacitors were fabricated on the n-type 100-nm-thick metamorphic $In_{0.53}Ga_{0.47}As$ layer. The $In_{0.53}Ga_{0.47}As$ metamorphic layer was grown on a 3-in. semi-insulating GaAs substrate by molecular beam epitaxy (MBE) with a Si doping concentration of $1 \times 10^{17}$ $cm^{-3}$ and an $In_xAl_{1-x}As$ layer as the metamorphic graded

buffer layer to accommodate the large lattice mismatch between the $In_{0.53}Ga_{0.47}As$ and GaAs substrates. Figure 6-1 shows the structure of the MOS capacitor in this study. Annealed Au-Ge-Ni-Au ohmic contacts were used with low contact resistance. Before dielectric deposition, surface pretreatment was performed to improve the interface quality. Two surface pretreatments, namely, Treatment A and Treatment B, were investigated in this study. In Treatment A, the native oxide was removed by dipping the surface into a diluted HCl solution (1:10) for 60 s. Treatment B was first performed as Treatment A and then the surface was also dipped into an ammonium sulfide solution [$(NH_4)_2S_x$] at 75°C for 15 min, followed by a deionized water rinse and a $N_2$ blow dry. A $(NH_4)_2S_x$ dip was performed because it can etch the native oxide and GaAs to provide a fresh surface, as well as to tie up the dangling bonds of the $In_{0.53}Ga_{0.47}As$ [6-10,6-11]. A 10-nm-thick $ZrO_2$ film was sputtered onto the surface of the substrate after it was treated in order for the film to function as the gate dielectric. The film was deposited at room temperature in an Ar + $O_2$ ambient [$O_2$/（Ar + $O_2$) = 0.2] with a power of 60 W and a base chamber pressure of $5 \times 10^{-6}$ Torr. Post deposition annealing (PDA) was performed in accordance with the RTA system at different temperatures in the forming gas for 60 s. Finally, a Ti-Pt-Au gate electrode was formed by a lift-off process. The electrical characterization of the MOS capacitor was performed using an HP4294A precision LCR meter with a bias sweep rate of 50 mV/s, which was used to measure the capacitance voltage and a HP4142B semiconductor parameter analyzer was used for the leakage-current density measurement.

### 6.3 Result and Discussion

Figures 6-2(a) and 6-2(b) show the $1 \times 1$ μm$^2$ atomic force microscope (AFM)

images of the samples after the deposition of the $ZrO_2$ dielectric film using Treatment A and Treatment B, respectively. A smooth surface is desired because a rough surface usually causes an enhanced local electric field, which would affect the performance of the device. After $ZrO_2$ deposition, the AFM images show smooth surface morphologies with RMS roughnesses of 0.841 and 0.730 nm for Treatment A and Treatment B, respectively. From these results it can be observed that neither surface treatment causes any appreciable change in the surface roughness. Figure 3 shows the high-resolution cross-sectional transmission electron microscope (TEM) images of the $ZrO_2/In_{0.53}Ga_{0.47}As$ interface with Surface Treatment A [Fig. 6-3(a)] and Surface Treatment B [Fig. 6-3(b)]. When the native oxide was removed by initial HCl wet etching (Treatment A), a thin interfacial oxide layer was still observed between the $ZrO_2$ film and $In_{0.53}Ga_{0.47}As$ substrate. For samples subjected to Treatment B, the interface contains a 20-Å-thick interlayer as seen in Fig. 6-3(b). Figure 6-4 shows the secondary ion mass spectroscopy (SIMS) depth profiles of the MOS structure ($Ti/ZrO_2/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$) obtained by sputtering $O_2^+$ ions at an energy level of 5.5 keV. The depth= 0 corresponds to the Ti surface and the Ti and Al signals were removed. Despite the signal broadening, it can be clearly observed that the $^{34}S$ distribution is located on top of the $In_{0.53}Ga_{0.47}As$ layer. This indicates the existence of a sulfur-passivated layer between the $ZrO_2$ film and $In_{0.53}Ga_{0.47}As$ substrate.

The high-frequency (1 MHz) capacitance-voltage (*C-V*) characteristics of the MOS capacitors fabricated using Treatment A and Treatment B on the same epi wafer were compared and the results are shown in Fig. 6-5 and 6-6, respectively. The diameter of the MIS diode is 75 μm. For samples subjected to Treatment A, the large dispersion of the C-V curves in the inversion region, as shown in Fig. 4a, could be due to the presence of the dangling bonds or the As-rich states in the interface without sulfur passivation, which results in high surface states and the deterioration of the

inversion properties of the device after PDA at 250°C [6-5]. However, after 350°C annealing, the curves improved significantly when compared with their states at 250°C annealing. This is due to a decrease in the number of dangling bonds after 350°C annealing. However, it still shows a slight dispersion in the inversion area compared with the sample subjected to sulfur pretreatment after 350°C annealing. As can be seen in Fig. 6-6, for samples precleaned using Treatment B, the accumulation region exhibits complete horizontal curves and good inversion behavior after PDA at 350°C owing to the unpinning of the Fermi level. Consequently, it is conceivable that the sulfur passivation layer could prevent a bare $In_{0.53}Ga_{0.47}As$ surface from being exposed to air and from generating poor native oxide. Figure 6-7 shows the leakage current density as a function of the gate bias for the MOS capacitors subjected to different surface treatments. The leakage current was significantly suppressed and a higher breakdown voltage was obtained for the $In_{0.53}Ga_{0.47}As$ MOS subjected to sulfur pretreatment compared with the $In_{0.53}Ga_{0.47}As$ MOS subjected to HCl etch pretreatment only. Hence, it can be concluded that a low leakage current and a high breakdown voltage can be achieved for $In_{0.53}Ga_{0.47}As$ MOS subjected to sulfur pretreatment, owing to the low imperfect bonding states with a high barrier height for the electrons after the sulfur pretreatment.

## 6.4 Conclusion

In summary, the C-V curves of the metamorphic $In_{0.53}Ga_{0.47}As$ MOS capacitors on a GaAs substrate with $ZrO_2$ as the dielectric subjected to different surface treatments have been investigated. The $In_{0.53}Ga_{0.47}As$ MOS subjected to sulfur treatment before oxide deposition exhibited lower interface-state density, which leads to a strong inversion, a high breakdown voltage and less leakage current. Finally,

with additional optimizations of the PDA temperature and wet chemical pretreatment, further reduction in the interface trap density is feasible and the results could be applied to the production of future III-V/Si integrated circuits for the next generation of nanoelectronics.

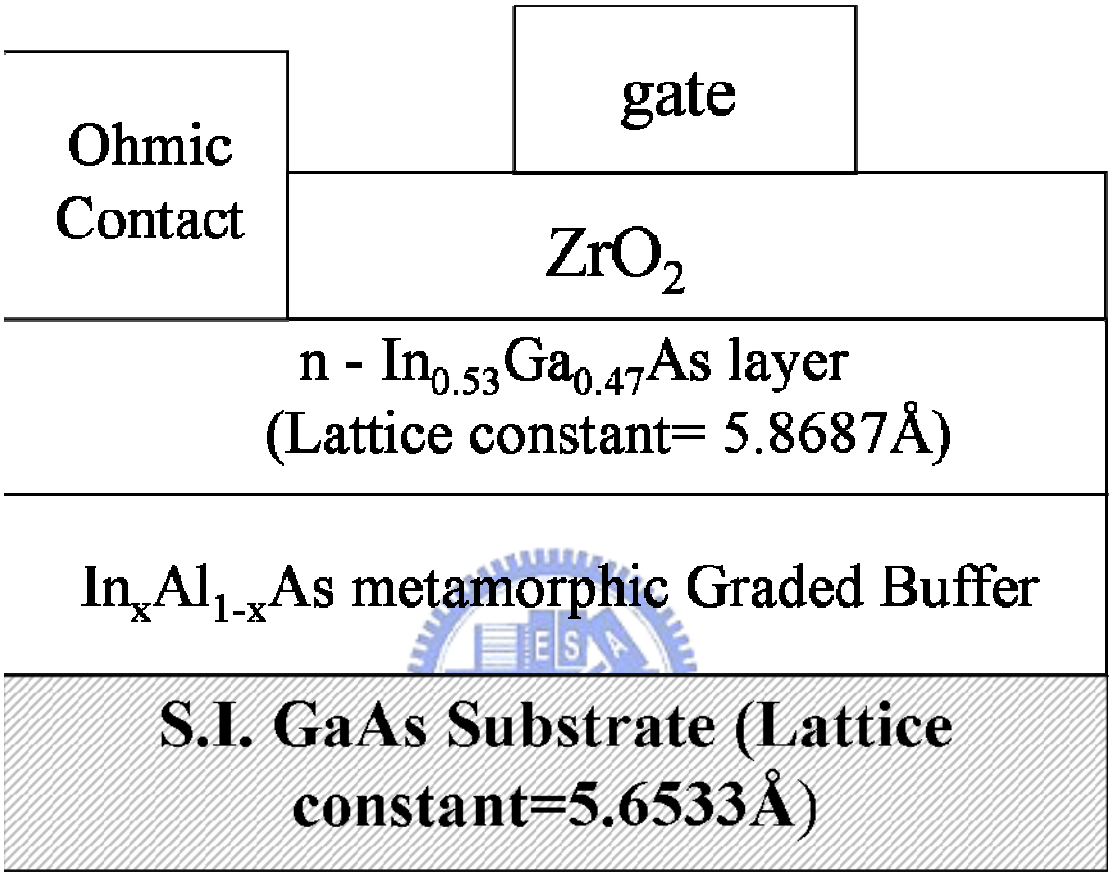
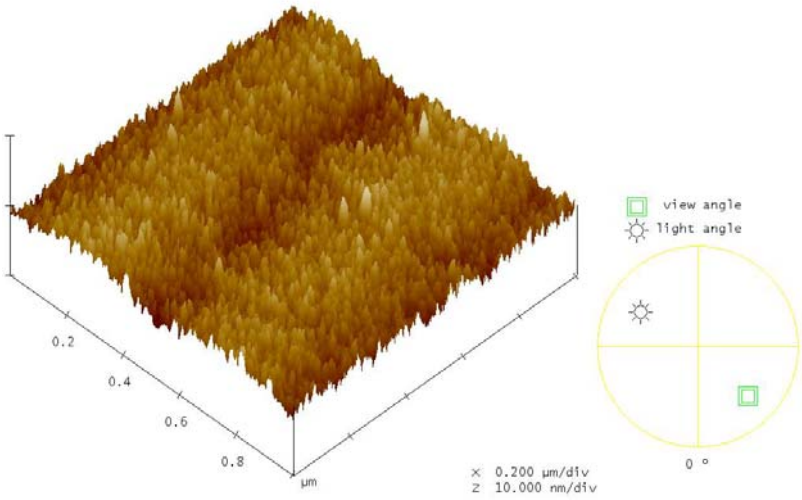
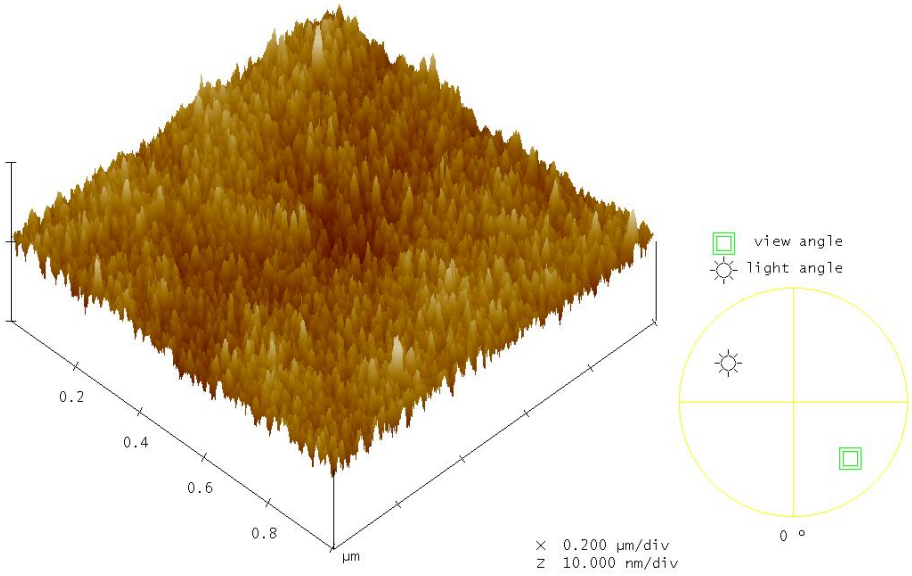



Fig. 6-1. Cross-sectional view of MOS capacitor structure.




(a)




(b)

Fig. 6-2. (a) AFM image of surface of HCl-cleaned (Treatment A) MOS after $ZrO_2$ deposition, RMS = 0.841 nm. (b) AFM image of surface of sulfur-passivated (Treatment B) MOS after $ZrO_2$ deposition, RMS = 0.730 nm.

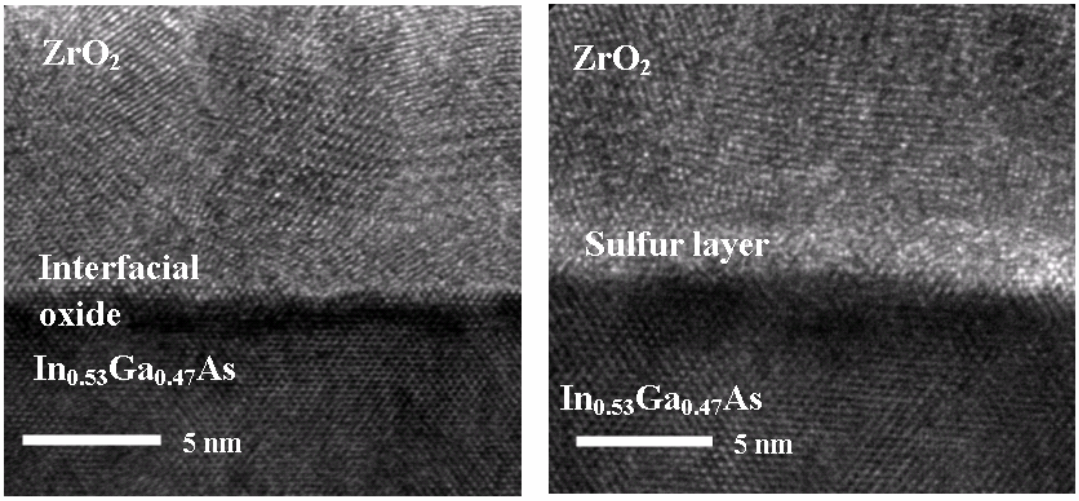



Fig. 6-3. High-resolution TEM cross-sectional images of $ZrO_2$/ $In_{0.53}Ga_{0.47}As$ gate dielectric stack: (a) HCl-cleaned sample, (b) $(NH_4)_2S_x$-treated sample.

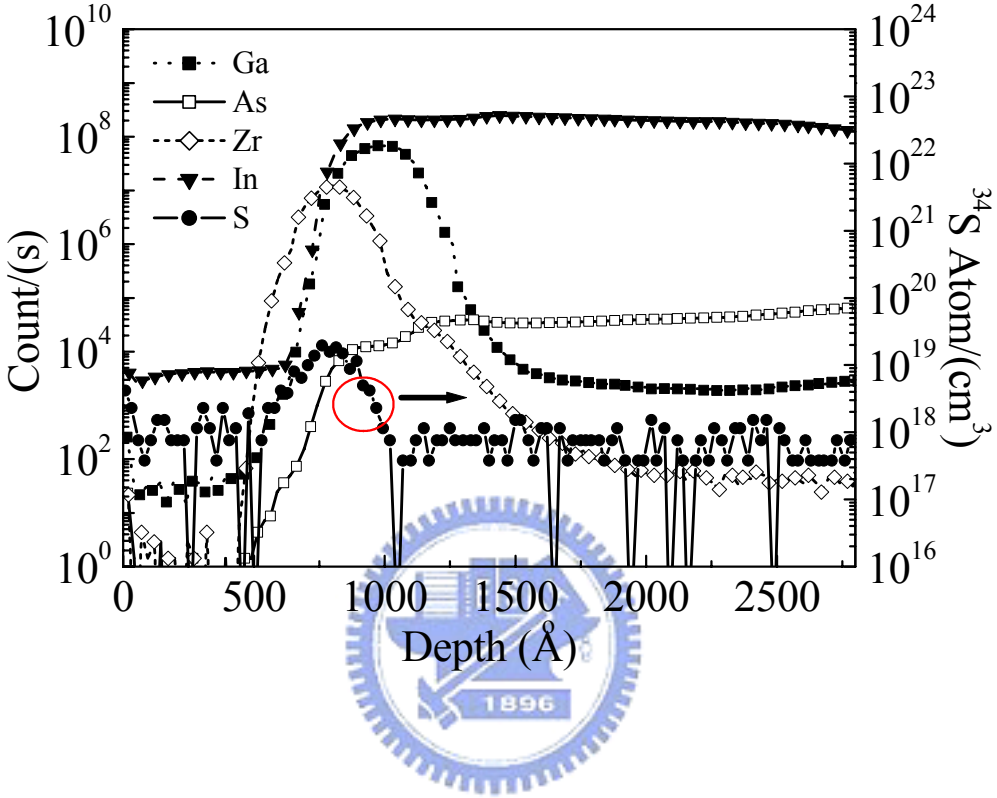



Fig. 6-4. SIMS depth profiles of S, Zr, In, Ga, and As elements and $^{34}$S density of MOS capacitor subjected to Surface Treatment B.

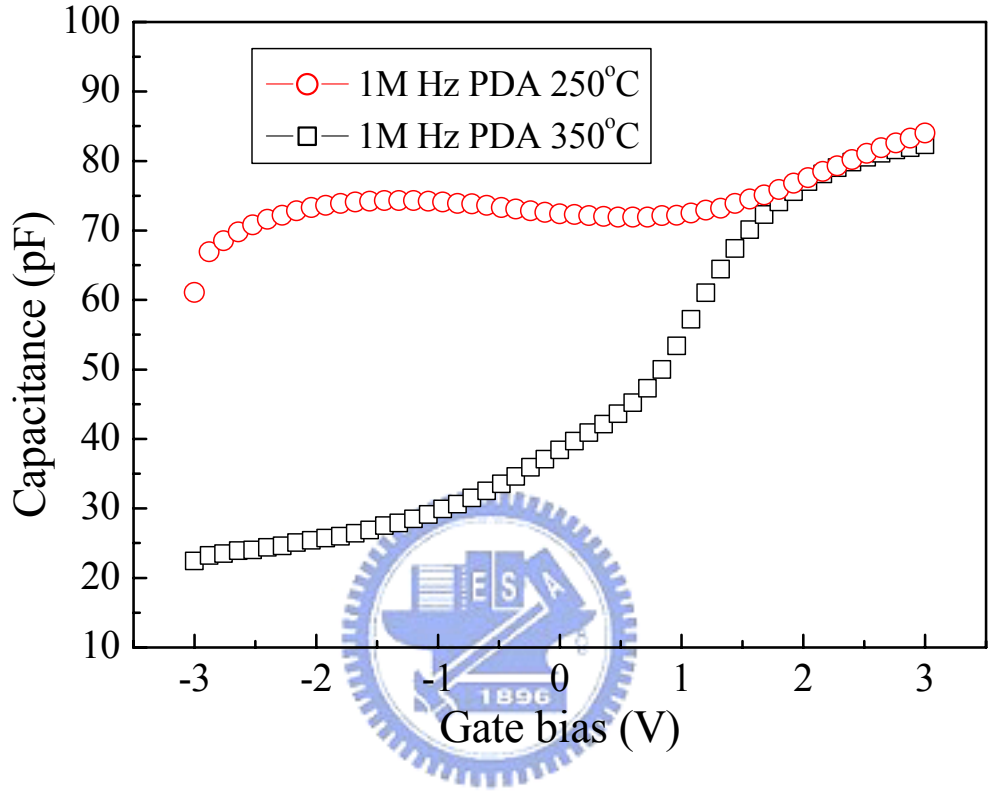



Fig. 6-5. High-frequency C-V characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with surface Treatment A after different PDA temperatures

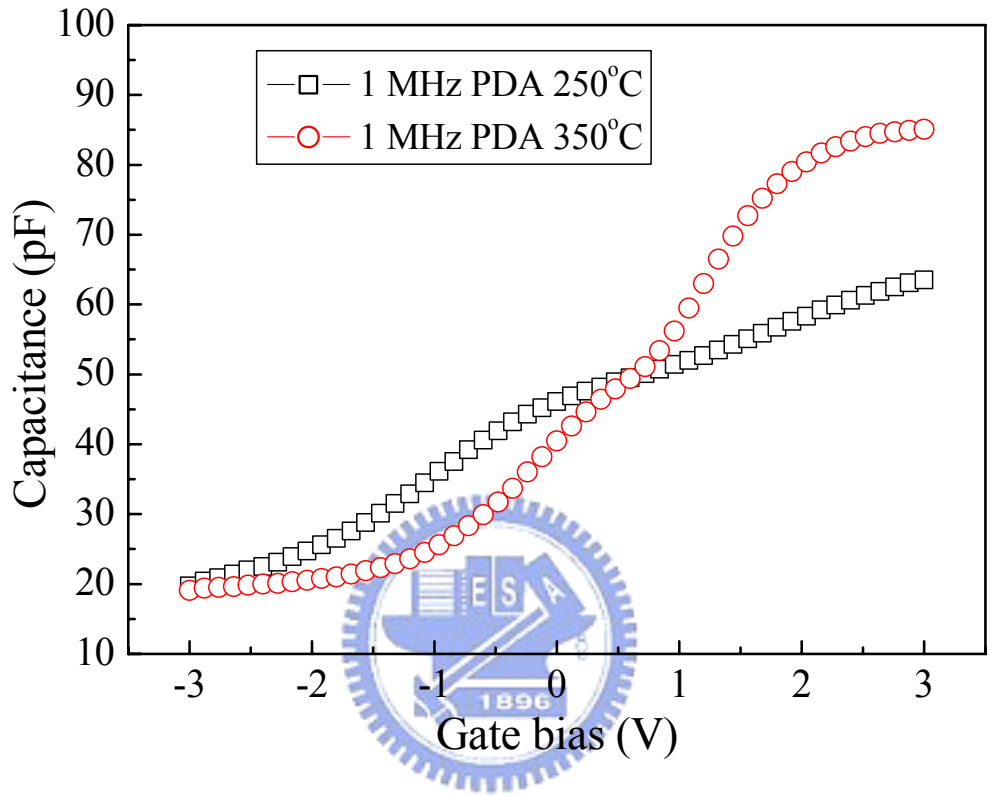



Fig. 6-6. High-frequency C-V characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with surface Treatment B after different PDA temperatures.

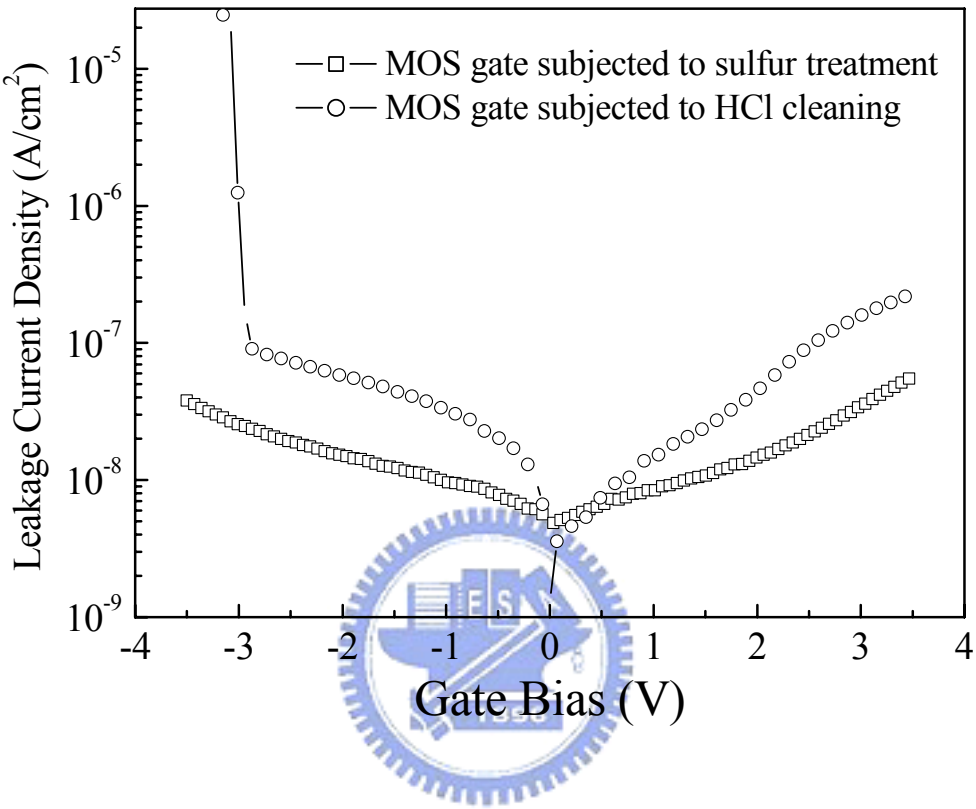



Fig. 6-7. Comparison of leakage current of MOS structure after different surface treatments.

# Chapter 7

## Conclusion

In this dissertation, the high performances HEMTs with different indium concentrations in the channel layers were fabricated successfully. RF and logic performance improvement of the 80 nm InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs was demonstrated by using Pt-buried gate technique. Superior DC characteristics are attributed to the high electron mobility in the channel layer and the low ohmic contact resistance. In addition, the reduction of gate-to-channel distance does not only increase the transconductance but also suppress the short channel effect after gate sinking. As for the current gain cutoff frequency, the value increases from 390 GHz to 494 GHz due to the increase of gm and the decrease of the gate-to-source capacitance in the applied gate bias range after the gate-sinking process. The noise figure of the fabricated InAs HEMTs with gate sinking was 0.82 dB with 14.02 dB associated gain at 17 GHz. The corresponding DC power consumption was 1.14 mW at this bias point, indicating its great potential for ultralow-power and low-noise applications. The effect of gate sinking on the intrinsic device speed of the device was also evaluated. Smaller $C_{gs}$ after gate sinking was obtained resulting in excellent gate delay time (0.78 psec).

For low-voltage logic evaluation, the InAs HEMT with 2 μm source-draing spacing were developed and analyzed the digital characteristics. The drain-induced barrier lowering and subthreshold slope were 200 mV/dec and 115 mV/V, respectively. Comparison of novel devices, InAs HEMT exhibits better $I_{ON}/I_{OFF}$ ratio than InSb device and show much higher gain and smaller delay time than the state-of-the-art Si

MOSFET when fixed at the same bias condition. However, such narrow bandgap device suffers from serious schottky gate leakage and band to band leakage current. It is effective to solve this problem by inserting high-k material between gate metal and semiconductor layer. With further device optimization and incorporation with high k materials to reduce the gate leakage current, InAs HEMTs could be the technology of choice when the CMOS roadmap comes to 30 nm and beyond.

To incorporate the high k material to the InGaAs devices, physical characteristics and electronic properties of the metamorphic $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor (MOS) capacitors on GaAs substrate with 100Å-thick $ZrO_2$ as the high-k dielectrics were investigated. The $In_{0.53}Ga_{0.47}As$ surface was pre-treated by either sulfur passivation or HCl cleaning before $ZrO_2$ deposition. The sulfur-passivated capacitor exhibited well-behaved capacitance-voltage and current-voltage characteristics after Post Deposition Annealing (PDA) at 350$^{o}$C as compared to that of the HCl-cleaned capacitor. Judged from the results of material analysis, the MOS capacitors with sulfur treatment showed a thin sulfur layer in the interface which protects the $In_{0.53}Ga_{0.47}As$ layer from exposing to air and avoid performance degradation. The results show that $[(NH_4)_2S_x]$ treatment on III-V semiconductor can effectively protect the surface from forming native oxide when fabricating MOS-HEMTs or III-V MOSFETs.

## References

### Chapter 1


[1-1] Ken David, Intel Corporation, Dec. 2005.

[1-2] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 294-296, April. 2008.

[1-3] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-Transport-Enhancement Channel CMOS for Improved Power Consumption and Performance," *IEEE Trans. Electron Devices,* vol. 55, no. 1, pp. 252-257, Jan. 2008.

[1-4] K. C. Saraswat, C. O. Chui, D. Kim, T. Krishnamohan, and A. Pethe, "High Mobility Materials and Novel Device Structures for High Performance Nanoscale MOSFETs" in *IEDM Tech. Dig.*, 2006, pp.659-662.

[1-5] Y. Sun, S. J. Koester, E. W. Kiewra, J. P. D. Souza, N. Ruiz, J. J. Bucchignano, A. Callegari, K. E. Fogel, D. K. Sadana, J. Fompeyrine, D. J. Webb, J. P. Locquet, M. Sousa, and R. Germann, "Post-Si CMOS: III-V n-MOSFETs with High-k Gate Dielectrics," in CS MANTECH Conference, 2007, pp. 231-234.

[1-6] X. W. Wang, N. Li, J. Zheng, S. Shim, and T. P. Ma, "Gate Quality $Al_2O_3$ by Molecular-Atomic-Deposition (MAD) and its Potential Application in III-V Semiconductor CMOS Technology," Trans. Electrochem. Soc. 6, 321 2007.

[1-7] S. Koveshnikov, W. Tsai, I. OK, J. C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, "Metal-oxide-semiconductor capacitors on GaAs with high-k gate

oxide and amorphous silicon interface passivation layer," *Appl. Phys. Lett.*, vol. 88, pp. 0221061-0221063, 2006.

[1-8] F. Gao, S. J. Lee, R. Li, S. J. Whang, S. Balakumar, D. Z. Chi, C. C. Kean, S. Vicknesh, C. H. Tung, and D. L. Kwong, "GaAs p- and n-MOS devices integrated with novel passivation (plasma nitridation and AlN-surface passivation) techniques and ALD-$HfO_2$/TaN gate stack," in *IEDM Tech. Dig.*, 2006, pp.833-836.

[1-9] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-AlGaAs Heterojunctions," *Jpn. J. Appl. Phys.*, vol. 19, pp. L225-L227, 1980.

[1-10] S.M.Sze, "High Speed Semiconductor Device," Murryay Hill, New Jersey.

[1-11] J. A. del Alamo and D. H. Kim, "Beyond CMOS: Logic Suitability of InGaAs HEMTs," in *Proc. 19th Int. Conf. InP and Related Materials*, 2007, pp. 51-54.

[1-12] D. H. Kim and J. A. del Alamo, "Beyond CMOS: Logic Suitability of $In_{0.7}Ga_{0.3}As$ HEMTs," in CS MANTECH Conference, 2006, pp. 251-254.

**Chapter 2**

[2-1] Y. He, B. W. Liang, N. C. Tien and C. W. Tu, "Selective Chemical Etching of InP Over InAlAs," J. Electrochem. Soc. 139, pp. 2046, 1992.

[2-2] R. Williams, "Modern GaAs Processing Methods," Artech House, Inc., pp. 221 1991.

[2-3] W. Liu, "Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs," John Wiley & Sons, Inc., pp. 422 1999.

[2-4] S. Bollaert, Y. Cordier, V. Hoel, M. Zaknoune, H. Happy, S. Lepilliet, and A. Cappy, "Metamorphic $In_{0.4}Al_{0.6}As/In_{0.4}Ga_{0.6}As$ HEMT's on GaAs Substrate," *IEEE Electron Device Lett.*, vol. 20, pp. 123-125, March 1999.

[2-5] L. Hongqin, X. Guanqun, and S. Xiaowei, "A Study of the Selective Gate Recess Etching Technology and Its Effects on the Microwave Properties of PHEMTs," Microwave and Optical Technology Letters, vol. 30, No. 6, September 20, 2001.

**Chapter 3**

[3-1] G. F. Engen, and C.A. Hoer, "Thru-Reflect-Line:An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," IEEE Trans. on Microwave Theory and Techniques, vol. 27, no. 12, pp. 987-993, Dec. 1979.

[3-2] W. Liu, "Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs," John Wiley & Sons, Inc., pp. 293 1999.

[3-3] A. W. Scott, "Understanding Microwaves," John Wiley & Sons, Inc., pp. 65 1993.

[3-4] H. Fukui, "Optimal Noise Figure of Microwave GaAs MESFET's," *IEEE Trans. Electron Devices,* vol. 26, no. 7, pp. 1032-10377, July 1979.

**Chapter 4**

[4-1] K. Shinohara, Y. Yamashita, A. Endoh, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "Extremely High-Speed Lattice-Matched InGaAs/InAlAs High electron Mobility Transistors with 472 GHz Cutoff Frequency," *Jpn. J. Appl. Phys.*, vol. 41, pp. L437-L439, 2002.

[4-2] Y. Yamashita, A. Endoh, K. Shinohra, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Pseudomorphic $In_{0.52}Al_{0.48}As$/ $In_{0.7}Ga_{0.3}As$ HEMTs with an ultrahigh $f_t$ of 562 GHz," *IEEE Electron Device Lett.*, vol. 23, pp. 573-575, Oct. 2002.

[4-3] D. H. Kim, J. A. Alamo, J. H. Lee, and K. S. Seo, "Performance Evaluation of

50 nm $In_{0.7}Ga_{0.3}As$ HEMTs for beyond-CMOS logic applications," in *IEDM Tech. Dig.*, 2005, pp.767-770.

[4-4] R. Chau, S. Datta, and A, Majumdar, "Opportunities and Chanllenges of III-V Nanoelectronics for future high-speed,low-power logic applications," in *Proc. IEEE CSIC Dig.*, pp. 17-20, 2005.

[4-5] K. Shinohra, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547 GHz $f_t$ $In_{0.7}Ga_{0.3}As$/ $In_{0.52}Al_{0.48}As$ HEMTs With Reduced Source and Drain Resistance," *IEEE Electron Device Lett.*, vol. 25, pp. 241-243, May 2004.

[4-6] H. Matsuzaki, T. maruyama, T. Kosugi, H. Takahashi, M. Tokumitsu, and T. Enoki, "Laterally Scaled Down Tiered-Edge Ohmic Structure of InP-Based HEMTs for 2 S/mm $g_m$ and 500 GHz $f_T$," in *IEDM Tech. Dig.*, 2005, pp.775-778.

[4-7] K. J. Chen, T. Enoki, K. Arai, and M.yamamoto, "High-performance InP-based enhancement-mode HEMT's using Non-Alloyed Ohmic Contacts and Pt-based Buried-Gate Technologies," *IEEE Trans. Electron Devices,* vol. 43, no. 2, pp. 252-257, Feb. 1996.

[4-8] L. H. Chu, E. Y. Chang, L. Chang, Y. H. Wu, S. H. Chen, H. T. Hsu, T. L. Lee, Y. C. Lien, and C. Y. Chang, "Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT," *IEEE Electron Device Lett.*, vol. 28, pp. 82-85, Feb. 2007.

[4-9] N. Harada, S. Kuroda, T. Katakami, K. Hikosaka, T. Mimura, and M. Abe, "Pt-based gate enhancement-mode InAlAs/InGaAs HEMTs for large-scale integration," in *Proc. 3rd Int. Conf. InP and Related Materials*, 1991, pp. 377-380.

[4-10] S. Kim, K. Jang, G. Seol, J. Her, and K. Seo, "Passivation Effects of 100 nm

$In_{0.4}AlAs/In_{0.35}GaAs$ Metamorphic-High-Electron-Mobility Transistors with a Silicon Nitride layer by Remote Plasma-Enhanced Chemical Vapor Deposition," Japan Journal of Applied Physics, Vol. 46, no. 4B, pp. 2341-2343, 2007.

[4-11] T. Akazaki, K. Arai, T. Enoki, and Y. Ishii, "Improved InAlAs/InGaAs HEMT Characteristics by Inserting an InAs Layer into the InGaAs Channel," *IEEE Electron Device Lett.*, vol. 13, pp. 325-327, June. 1992.

[4-12] D. H. Ko and R. Sinclair, "Amorphous phase formation in an as-deposited platinum-GaAs interface," *Appl. Phys. Lett.*, vol. 58, no. 17, pp. 1851-1853, Apr. 29, 1991.

[4-13] Y. Yamashita, A. Endoh, K. Shinohara, M. Higashiwaki, K. Hikosaka, T. Mimura, S. Hiyamizu, and T. Matsui "Ultra-short 25nm Gate Lattice Match InAlAs/InGaAs HEMTs Within the Range of 400GHz Cut Off Frequency," *IEEE Electron Device Lett.*, vol. 22, pp. 367-369 August 2001

[4-14] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp.1151-1159, 1988

[4-15] S. Kim, I. Adesida, and H. Hwang, "Measurements of the thermally induced nanometer-scale diffusion depth of Pt/Ti/Pt/Au gate metallization on InAlAs/InGaAs high-electron mobility transistors," *Appl. Phys. Lett.*, vol. 87, no. 23, p. 232102, Dec. 2005.

[4-16] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalierous, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications" *IEEE Transcations On Nanotechnology*, vol. 4, no. 2, MAR. 2005

[4-17] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design

optimization of near ballistic carbon nano tube field effect transistors," in *IEDM Tech. Dig.*, 2004, pp.703-706.

**Chapter 5**

[5-1] Robert Chau, Suman Datta, Mark Doczy, Brian Doyle, Ben Jin, Jack Kavalieros, Amlan Majumdar, Matthew Metz, and Marko Radosavljevic, "Benchmarking Nanotechnology for High Performance and Low Power Logic Transistor Applications," *IEEE Transactions On Nanotechnology,* 4, 153, 2005.

[5-2] D. H. Kim, J. A. Alamo, J. H. Lee, and K. S. Seo, "Logic Suitability of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs for Beyond-CMOS Applications," *IEEE Transactions on Electron Devices,* 54, pp.2606, 2007.

[5-3] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra Speed and Very Low Power Digital Logic Applications," in *IEDM Tech. Dig.*, pp.763-766, 2005.

[5-4] International Technology Roadmap for Semiconductors, in ITRS Winter Public Conference, Japan 2007.

[5-5] R. Chau, S. Datta, and A, Majumdar, "Opportunities and Challenges of III-V Nanoelectronics for Future High-Speed, Low-Power Logic Applications," in *Proc. IEEE CSIC Dig.*, pp. 17-20, 2005.

[5-6] S. J. Yeon, M. Park, J. Choi, and K. Seo, "610 GHz InAlAs/In0.75GaAs Metamorphic HEMTs with an Ultra-Short 15-nm Gate," in *IEDM Tech. Dig.*, pp.613-616, 2007.

[5-7] K. Shinohara, W. Ha, M. J. W. Rodwell, and B. Brar, "Extremely High gm >

2.2 S/mm and $f_T$ > 550 GHz in 30-nm Enhancement-Mode InP-HEMTs with Pt/Mo/Ti/Pt/Au Buried Gate," *Proc. 19th IEEE Indium Phosphide and Related Material (IPRM) Conference*, pp. 18-21 May, 2007.

[5-8] C.Y. Chang, H. T. Hsu, Edward Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, Y. Miyamoto, and G. W. Huang, "Investigation of Impact Ionization in InAs-Channel HEMT for High Speed and Low Power applications" *IEEE Electron Device Lett.*, vol. 28, pp.856-858, 2007.

[5-9] T. Akazaki, K. Arai, T. Enoki, and Y. Ishii, "Improved InAlAs/InGaAs HEMT Characteristics by Inserting an InAs layer into the InGaAs Channel," *IEEE Electron Device Lett.*, vol. 13, pp.325,1992.

[5-10] G. Meneghesso, D. Buttari, E. Perin, C Canali, and E. Zanoni, "Improvement of DC, low frequency and reliability properties of InAlAs-InGaAs InP-based HEMTs by means of InP etch stop layer,"in *IEDM Tech. Dig.*, pp.227-230 1998.

[5-11] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, "30-nm two step-recess gate InP-based InAlAs/InGaAs HEMTs"*IEEE Trans. Electron Devices,* Vol. 49, no. 10, pp.1694-1700, Oct. 2002.

[5-12] Y. Yamashita, A. Endoh, K. Shinohara, M. Higashiwaki, K. Hikosaka, T. Mimura, S. Hiyamizu, and T. Matsui, "Ultra-short 25nm Gate Lattice Match InAlAs/InGaAs HEMTs Within the Range of 400GHz Cut Off Frequency," *IEEE Electron Device Lett.*, vol. 22, pp.367, 2001.

[5-13] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp.1151, 1988.

[5-14] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field effect transistors," in

*IEDM Tech. Dig.*, pp.703-706, 2004.

[5-15] R. Chau, J. Brask, S. Datta, G Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Application of high-k dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology, Microelectronic Engineering, 80, pp. 1-6 2005.

[5-16] K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn, and I. Young, "A comparison of state-of-the-art NOMS and SiGe HBTs device for analog/mixed-signal/RF circuit applications," in *VLSI symp. Tech. Dig.* , pp. 224-225,2004.

**Chapter 6**

[6-1] K. S. Seo, and D. H. Kim, "Nanometer Scale InGaAs HEMT Technology for Ultra High Speed IC" Proc. 18th IEEE Indium Phosphide and Related Material (IPRM) Conference, pp. 30-35 May (2006).

[6-2] R. Chau, S. Datta, and A. Majumdar, "Opportunities and Challenges of III-V Nanoelectronics for Future High-Speed, Low-Power Logic Applications" IEEE Compound Semiconductor Integrated Circuit Symposium, pp. 17-20, 2005.

[6-3] Y. Z. Hu, and S. P. Tay, "Characterization of high-k dielectric $ZrO_2$ films annealed by rapid thermal processing" *J. V. Sci. Technol. B* 19, 1706, 2001.

[6-4] S. Ventkataraj, O. Kappertz, C. Liesch, R. Detemple, R. Jaya, M. Wutting, "Thermal stability of sputtered zirconium oxide films" *Vacuum*, 75, 7, 2004.

[6-5] J. K. Yang, M. G. Kang, and H. H. Park, "Chemical and electrical characterization of $Gd_2O_3$/GaAs interface improved by sulfur passivation" *J. Appl. Phys.* 96, 4811, 2004.

[6-6] M. M. Frank, S. J. Koester, M. Copel, J. A. Ott, V. K. Paruchuri, H. Shang, and R. Loesing, "Hafnium oxide gate dielectrics on sulfur-passivated germanium"

*Appl. Phys. Lett.* 89, 11295, 2006.

[6-7] K. Remashan, and K. N. Bhat, "Stable gallium arsenide MIS capacitors and MIS field effect transistors by $(NH_4)_2S_x$ treatment and hydrogenation using plasma deposited silicon nitride gate insulator" *IEEE Trans. Electron Devices.* 49, 343, 2002.

[6-8] E. O'Connor, R.D. Long, K. Cherkaoui, K.K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurley, B. Brennan, G. Hughes, and S. B. Newcomb, "In situ $H_2S$ passivation of $In_{0.53}Ga_{0.47}As$/InP metal-oxide-semiconductor capacitors with atomic-layer depositioned $HfO_2$ gate dielectric" *Appl. Phys. Lett.* 92, 022902, 2008.

[6-9] T. Ohno, and K.shiraishi, "First-principles study of sulfur passivation of GaAs (001) surfaces" *Phys. Rev. B* 42, 11194, 1990.

[6-10] H. Oigawa, J. Fan, Y. Nannichi, H. Sugahara, and M. Oshima, "Universal Passivation Effect of $(NH_4)_2S_x$ Treatment on the Surface of III-V Compound Semiconductors" *Jpn. J. Appl. Phys.*, vol. 30, pp. L322-L325, 1991.

[6-11] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, "Metal gate HfO2 metal-oxide-semiconductor structures on InGaAs substrate with varying Si interface passivation layer and postdeposition anneal condition," *J. Vac. Sci. Technol.* B 25, 1491, 2007.

# 簡歷(Vita)

姓名：郭建億

性別：男

生日：民國 68 年 1 月 23 日

籍貫：嘉義縣

學歷：

國立東華大學物理學系學士

（民國 86 年 9 月－民國 90 年 6 月）

國立清華大學原子科學研究所物理組碩士

（民國 90 年 9 月－民國 92 年 6 月）

國立交通大學材料科學與工程研究所博士

（民國 92 年 9 月－民國 97 年 7 月）

博士論文題目：

高速與低功率邏輯應用之砷化銦鋁/砷化銦鎵變異結構高電子移動率電晶體之研究

The Study of InAlAs/$In_xGa_{1-x}As$ Metamorphic High Electron Mobility Transistors for High Speed and Low Power Logic Applications

## Publication List

Journal Paper：

1. **Chien-I Kuo**, Heng-Tung Hsu, Edward Yi Chang, Chia-Yuan Chang, Yasuyuki Miyamoto, Suman Datta, Marko Radosavljevic, Guo-Wei Huang, and Ching Ting Lee "**RF and Logic Performance Improvement of $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ composite channel HEMTs Using Gate-Sinking Technology**" *IEEE Electron Device Lett*., vol. 29, No. 4, Apr., 2008.
2. **Chien-I Kuo**, Edward Yi Chang, Heng-Tung Hsu, Chun-Chi Chen, and Chia-Yuan Chang, "**Metamorphic $In_{0.53}Ga_{0.47}As$ Metal-Oxide-Semiconductor Structure on a GaAs substrate with $ZrO_2$ high-k dielectrics**," Japan Journal of Applied Physics, Vol 47, No. 5, 2008.
3. **Chien-I Kuo**, Heng-Tung Hsu, Edward Yi Chang, Yssuyuki Miyamoto, and Wen-Chung Tsern, " **An InAs HEMTs with Buried Gate for Ultra-Low-Power Consumption Low Noise Amplifier Application**," Japan Journal of Applied Physics, Vol 47, No. 9, 2008.
4. **Chien-I Kuo**, Heng-Tung Hsu, and Edward Yi Chang, "**InAs Channel-based Quantum Well Transistors for High-Speed and Low-Voltage Digital Applications,**" Electrochemical and Solid-State Letter, 11(7), H193-H196, 2008.
5. C.Y. Chang, Edward Yi Chang, Y. C. Lien, Y. Miyamoto, **C.I. Kuo**, S. H. Chen, and L. H. Chu, " **High-Performance $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Power Metamorphic High Electron Mobility Transistor for Ka-band Applications**", Japanese Journal of Applied Physics, Vol 46, No. 6A, pp. 3385-3387, 2007.
6. C.Y. Chang, H. T. Hsu, Edward Yi Chang, **C.I. Kuo**, Suman Datta, Marko Radosavljevic, Yasuyuki Miyamoto,and Guo-Wei Huang, "**Investigation of Impact Ionization in InAs-Channel HEMT for High Speed and Low Power Applications**" *IEEE, Electron Device Lett.* Vol. 28, No. 10 pp. 856-859 2007.

7. H.L. Chen, Y. H. Chu, **C. I. Kuo**, F. K. Liu, F. H. Ko, and T. C. Chu, "**Rapidly Selective Growth of Nanoparticles by Electron-Beam and Optical Lithographies with Chemically Amplified Resists**" , Electrochemical and Solid-State Letters, 8 (2) G54-G56 2005.

Conference Paper

1. H. T. Hsu, C. Y. Chang, Edward Yi Chang, **C. I. Kuo**, and Yssuyuki Miyamoto, "**High Performance InAs-Channel HEMT for Low Voltage Milimeter Wave Applications**", Asia-Pacific Microwave Conference, TH A2-F4, Thailand 2007
2. Edward Yi Chang, **Chien-I Kuo**, Hung-Tung Hsu, "**InAs Quantum Well Transistors for High-Speed Low Power Applications**", *213th ECS Meeting* May 18-23, 2008, Phoenix, AZ ECS Transactions Vol.13.
3. **Chien-I Kuo**, Heng-Tung Hsu, Edward Yi Chang, Chia-Ta Chang, Chia-Yuan Chang and Yasuyuki Miyamoto, "**Investigation of Impact Ionization from $In_xGa_{1-x}As$ to InAs Channel HEMTs for High Speed and Low Power Applications,**" in 20th IPRM WP 62 2008.
4. Edward Yi Chang , **Chien-I Kuo**, Heng-Tung Hsu, and Chia-Yuan Chang, "**InAs/$In_{1-x}Ga_xAs$ Composite Channel High Electron Mobility Transistors for High Speed Applications,**" in EuMW IC 2008.
5. Chien-Ying Wu, Heng-Tung Hsu, **Chien-I Kuo**, Edward Yi Chang, and Yu-lin Chen, "**Evaluation of RF and Logic Performance for 40 nm InAs/InGaAs Composite Channel HEMTs for high-speed and low-voltage applications,**" summated to Asia-Pacific Microwave Conference, Hong Kong 2008.
6. Heng-Tung Hsu, **Chien-I Kuo**, and Edward Yi Chang, "**On the Noise Performance of 80nm InAs/$In_{0.7}Ga_{0.3}As$ HEMTs Using Gate Sinking Technology,**" summated to Asia-Pacific Microwave Conference, Hong Kong

2008.

7. **Chien-I Kuo**, Heng-Tung Hsu, Chia-Yuan Chang, Edward Yi Chang, and Heng-shou Hsu, "**Evaluation of RF and Logic Performance of 80 nm InAs/ $In_{0.7}Ga_{0.3}As$ Composite Channel HEMT using gate sinking technology,**" *2007 IEEE Electron Device and Solid-State Circuits,* OE 07,pp. 255-258, Tainan.
8. Yi-Chung Lien, Edward Yi Chang, Sze-Hung Chen, Li-Shin Chu, Guo-Wei Huang, Yi-Shuan Peng, and **Chien-I Kuo**, "**High RF Performance GaAs Metamorphic HEMTs with 90-nm Sidewall T-gate,**" *Symposium on Nano Device Technology 2005*, pp. 272-273, Taiwan, 2005.
9. **Chien-I Kuo**, Hsuen-Li Chen, Fu-Ken Liu, F.H. Ko, and Tieh-Chi Chu, "**Patterning Colloidal Gold Nanoparticles by Optical Lithography**", *Symposium on Nano Device Technology* 2003, pp.143-146.

Patent：

1. 陳學禮、朱育宏、**郭建億**、劉福鯤、柯富祥、朱鐵吉,"奈米粒子圖形的形成方法， 中華民國專利專利公告號 I281098 (2007)。
2. 陳仕鴻、**郭建億**、張翼," 形成電子裝置閘極圖案之方法" 中華民國專利證號 I265564 (2006)。