Digital Control of a Multi-Phase Interleaved PWM Inverter with Minimal Total Harmonic Distortion

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***Abstract*—This paper presents a digital repetitive control scheme for the minimization of output voltage total harmonic distortion (THD) of a PWM inverter under large unknown nonlinear load. The multi-phase interleaved PWM inverter has been adopted to enhance the effective switching frequency as well as to share the load current. The realization of a digital control for PWM inverter, such as sampling delay and quantization error, may introduce many nonlinear effects to distort its output waveforms. A systematic design procedure is developed to minimize selected range of harmonic spectrum by shaping the output impedance by so that its output voltage THD can be lower than a specified value with given design constraints. The proposed control scheme has been realized with fully digital design by using a single-chip FPGA implementation and verified by using co-simulation technique via a VHDL simulator Modelsim combined with a system-level block diagram oriented simulator Simulink.**

Index Terms*—PWM inverter, digital repetitive control, minimal THD control, Modelsim and Simulink co-simulation, single-chip FPGA implementation.

I. Introduction

The PWM inverters for generation of a regulated ac sinusoidal voltage can be found in many applications in modern information appliances, such as CCFL back light, HID lamp, UPS, and ac power sources. High efficiency, high power density, and low THD with nonlinear load are major design challenges in implementation of slim-type inverter modules. Digital control technique with its high accurate and programmable timing control capabilities exhibits significant advantages over conventional analog control technique when applying to multi-phase interleaved PWM inverter to achieving high power density inverter modules.

Digital control techniques have been widely applied to the control of PWM inverters for ac voltage regulation under highly versatile nonlinear loads. With the availability of 16-bit high-performance DSP chips, most of its instructions can be accomplished in one instruction cycle, complicated control algorithms can be executed with fast speed. Sophisticated digital control algorithms can be more easily realized by using software with the employment of advanced digital signal processors [1]-[2].

Applications of digital control techniques to the PWM inverters can provide a lot of advantages in the promotion of an inverter embedded power converting system. This paper make a study of the quantization effect resulted by the digital PWM generator and the ADC converters for current sampling and voltage regulation and presents a digital repetitive control scheme for the minimization control of the THD of the output voltage of a multi-phase interleaved PWM inverter. The results can be used for the synthesis of the digital controller for closed-loop regulation of PWM inverters with lowest resolution of ADC converter to achieve a design goal of specified THD under nonlinear load.

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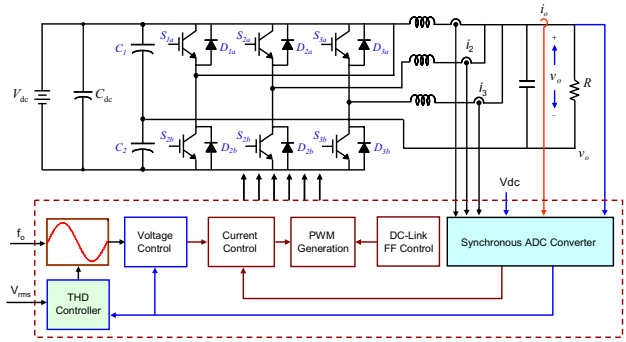

Fig. 1. Digital control of a multi-phase interleaved PWM inverter.

Fig. 1 shows the functional block diagram of a digital control of a multi-phase interleaved PWM inverter. The controller consists of two major controllers: an inner loop current controller and an outer loop voltage controller. A feed-forward controller is included to improve transient response under large input voltage variations. A minimal THD controller based on the digital repetitive control scheme is used to generate a periodic compensation waveform to eliminate low-frequency distortions resulted by highly nonlinear load.

The digital PWM generator and ADC converters will introduce large quantization effect and result limit-cycle oscillations (LCO) when a low bit-length ADC and low resolution digital PWM is adopted. The computation delay and sampling noise also significantly deteriorate the transient performance of a PWM inverter under large load variations. In order to eliminate the limit cycles in digitally controlled PWM converters, [3] suggests a design criterion in determination of the ADC and DPWM resolutions under a single voltage control loop condition. However, because

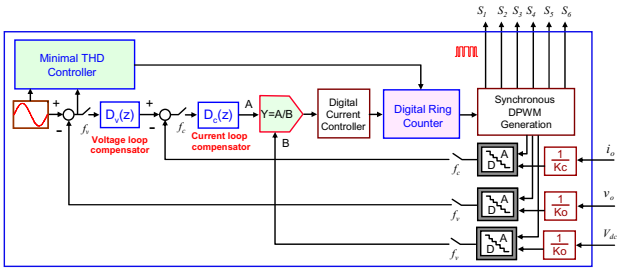

Fig. 2. Control architecture of digital control IC for PWM inverters.

major LCO comes from the DPWM and ADC, and the reduction of LCO by the reduction of loop gain will slow down the dynamic response. Prediction of LCO can be obtained by using extensive time-domain simulations based on dynamic model under different load and input voltage conditions [4]. A statistical model can be constructed by considering the quantization error as a white noise and evaluating the correlation between state variables [5]. The statistical model can then be used to predict the existence of LCO in a switching dc-dc converter. However, this approach is impractical for inverters under large nonlinear load variations and also is not suitable for real-time control applications.

Most of the existing models in prediction of LCOs are based on dynamic models derived from the describing functions and therefore are limited for sinusoidal oscillations. In practical applications LCOs of digital-controlled power converters depend on many factors, such as quantization effect, dead-zone, converter losses, output filter damping, output limit, computation delay, control bandwidth, etc.. and these factors are almost impossible to be treated by analytical models. As the application requirement of higher bandwidth using limited switching frequency, the LCO impose a more serious design challenge in application of digital control techniques to switching power converters. It is therefore we need an more intensive investigation by using time-domain simulation-oriented schemes to verify the presence of LCOs for any possible load current and input voltage conditions. This paper presents a digital repetitive control scheme with synchronized current sampling technique for the control of a multi-phase interleaved PWM inverter with minimal voltage THD under large nonlinear load, and the output LCOs result can be eliminated by digital quantization effect.

II. Periodic Disturbances Rejection

Fig. 2 shows the control architecture of the proposed digital inverter control scheme with minimal THD control. The analog signal is converted to a time-sampled and magnitude-quantized digital signal with a specified sampling frequency and resolution to digital controller, through appropriate regulate, to make output have good transient response and minimal distortion in steady response.

A. Multi-loop Digital Deadbeat Controller Design

Deadbeat control is an inverse model control scheme [6].

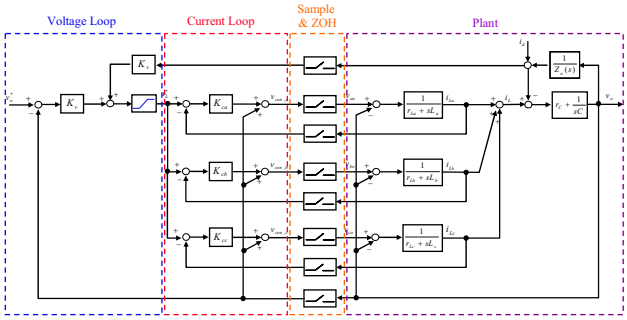

Fig. 3. Block diagram of the multi-loop digital control for interleaved PWM inverter.

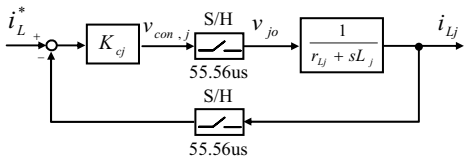

Fig. 4. Block diagram of the simplified diagram digital-controlled current-loop.

Its main principle is to locate all closed-loop poles at the origin of the unit circle as following

$$z^n = 0 \tag{1}$$

Based on the above condition, we can achieve a deadbeat response to a step input for a *n*-th order system. It is assumed that both the sampling and switching frequencies are high enough so that the controlled current can reach its reference command at the next sampling instant.

Fig. 3 is the block diagram of the multi-loop digital control for interleaved PWM inverter, including current inner loop and voltage outer loop. The current-loop is adopted sharing control to make same quantity per phase, Fig. 3 shown the output voltage feed-forward compensated for current-loop per phase can eliminate output voltage disturbance effect make current-loop. Simplification current-loop was shown in Fig. 4. corresponding current-loop plant, we may obtain *z*-domain transfer function and consider ZOH by using *z*-transform

$$G_i(z) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)\cdot\left(\frac{1}{r_{Lj}+sL_j}\right)\right\} = \frac{1}{r_{Lj}}\cdot\frac{1-e^{-\frac{r_{Lj}}{L_j}T_s}}{z-e^{-\frac{r_{Lj}}{L_j}T_s}},\quad j=a,b,c \tag{2}$$

where L_j is inductor, r_{Lj} is inductor ESR, T_s is sampling time, j represents the j-th phase of the inverter. From Fig. 4, we can derive closed-loop characteristic equation as

$$\Delta_{ic}(z) = z - e^{-\frac{r_{Lj}}{L_j}T_s} + \frac{K_{cj}}{r_{Lj}}\left(1-e^{-\frac{r_{Lj}}{L_j}T_s}\right) = 0,\quad j=a,b,c \tag{3}$$

Setting these poles to origin of the unit circle by based on (1), (3) can obtain as follow

$$K_{cj} = r_{Lj}\frac{e^{-\frac{r_{Lj}}{L_j}T_s}}{1-e^{-\frac{r_{Lj}}{L_j}T_s}},\quad j=a,b,c \tag{4}$$

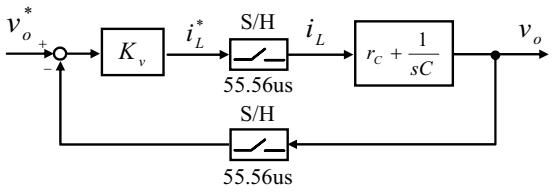

Fig. 5. Block diagram of the simplification voltage-loop.

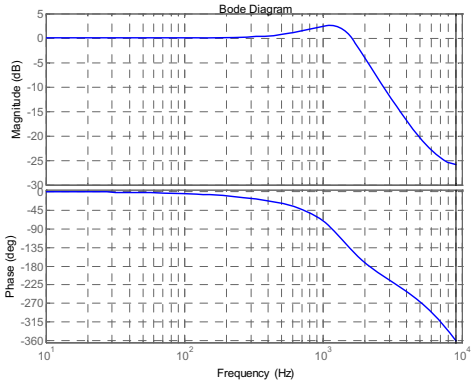

Fig. 6. Frequency response of the closed-loop reference-to-output response.

Assume that r_{Lj} can be neglected, than (4) can be obtained further more as

$$K_{cj} = \frac{L_j}{T_s}, \quad j = a,b,c \tag{5}$$

the current-loop control law can be obtained

$$v_{ci}(k) = \frac{L_i}{T_s}[i_{com}(k) - i_{Li}(k)] + v_o(k), \quad i = a,b,c \tag{6}$$

The voltage-loop is very similar with current-loop, Fig. 5 shown block diagram of the simplification voltage-loop. Like the current-loop, the addition output current feed-forward compensated can eliminate load disturbance effect. Using z-transform under consider ZOH can obtain z-domain transfer function for voltage-loop

$$G_v(z) = Z\left\{\left(\frac{1-e^{-sT_s}}{s}\right)\cdot\left(r_C + \frac{1}{sC}\right)\right\} = r_C + \frac{T_s}{C(z-1)} \tag{7}$$

where C is output capacitance, r_C is its ESR, and T_s is sampling time. The closed-loop characteristic equation of the voltage-loop is derived as

$$\Delta_{vc}(z) = z - \frac{1 + K_v\left(r_C - \frac{T_s}{C}\right)}{1 + K_v r_C} = 0. \tag{8}$$

From (1), the poles are set to origin of the unit circle, and (8) can be written as

$$K_v = \frac{C}{T_s - Cr_C}. \tag{9}$$

Assume r_C can be neglected, than (9) can be obtained further more as

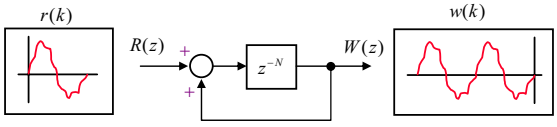

Fig. 7. Periodic signal generator.

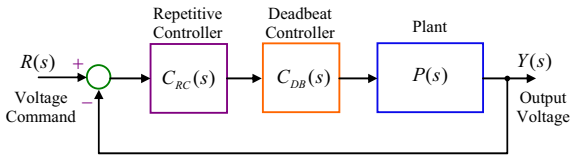

Fig. 8. Block diagram of the voltage-loop controller.

$$K_v = \frac{C}{T_s} \tag{10}$$

and the voltage-loop control law can be obtained as

$$i_{com}(k) = \frac{C_o}{T_s}[v_{com}(k) - v_o(k)] + \frac{1}{m} i_o(k) \tag{11}$$

where m is number of phase.

Fig. 6 shows the frequency response of the closed-loop reference-to-output under digital control with a bandwidth about 1.5 kHz. Although the deadbeat control can achieve a faster dynamic response, it also suffers from large load dynamics or parameter variations. Moreover, in high-power applications, where low-frequency switching is a must, the performance of deadbeat controller will severely degraded due to inevitable time delay and large nonlinear load variations. In this paper, the digital repetitive controller is designed to eliminate periodic error due to nonlinear load and quantization error due to digital sampling and computation effects with a minimal bit-length. This is important for practical implementation of low cost digital inverter control IC.

B. Digital Repetitive Controller

The basic concept of repetitive control theory originates from the internal model principle [7]. The principle states that the output of a control system can track the reference input without steady-state error if the model that generates the same reference is included in the closed-loop system. To implement a repetitive control system, a periodic actuating signal is used to cancel the periodic disturbance which must be generated. A periodic signal can be generated with a given initial condition as shown in Fig. 7. The positive number N denotes the number of samples taken in one period. If this periodic signal generator can be synthesized into a feedback system with asymptotic stability, it is possible to track a periodic command or reject a cyclic disturbance with the same period.

The repetitive controller functions as an auxiliary controller that modifies the original actuating signal by adding a periodic compensation signal. However, faster convergence of the periodic error will result a system with smaller stability margins. Therefore, we have to compromise between stability and convergence rate for design repetitive

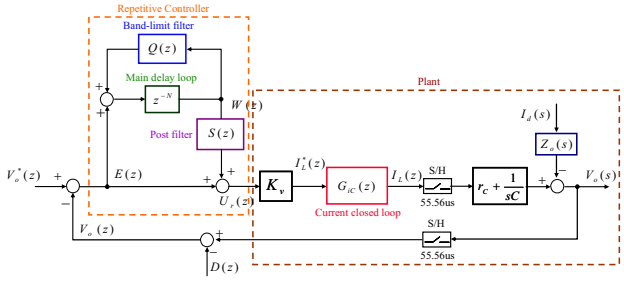

Fig. 9. Block diagram of the repetitive control scheme for voltage loop.

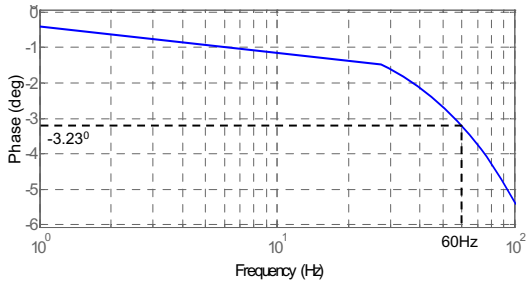

Fig. 10. Phase response of the loop gain without repetitive controller.

controller. This paper adopted architecture of the repetitive controller is plug-in for voltage-loop by showing in Fig. 3 to correct voltage error and make reduce to minimal. We can derive input to error relationship as

$$\frac{E(z)}{R(z)} = \frac{1 - Q(z)z^{-N}}{\left(1 + C_{DB}(z)P(z)\right)\cdot\left[1 - z^{-N}\left(Q(z) - H(z)S(z)\right)\right]} \quad (12)$$

$$H(z) = \frac{C_{DB}(z)P(z)}{1 + C_{DB}(z)P(z)} \quad (13)$$

where $H(z)$ is system added deadbeat control closed-loop transfer function. From (12), we can derive that if repetitive control system is stable, then $H(z)$ is need to be stable, and poles of $H(z)$ must be within the unit circle. The stability criterion based on

$$\left|1 - \frac{H(z)S(z)}{Q(z)}\right| < 1, \quad 0 < \omega < \pi \quad (14)$$

can be derived from small gain theory [8]. Fig. 8 shows the augmented repetitive controller within the dead beat control loop. voltage-loop to modified error signal, the repetitive controller included three main blocks in Fig. 9, the main delay loop is resulted periodic signal to make the control system to track the reference input without steady-state error. The band-limit filter $Q(z)$ is modified from delay loop result periodic signal to make system poles not on unit circle. So the magnitude of $Q(z)$ must be less than one. We usually implement by $Q(z)$ have two type, one is less than one constant, and the other one is adopted low pass filter to implement. From Fig. 9, we can obtain

$$W(z) = Q(z)\cdot W(z - N) + E(z - N) \quad (15)$$

This equation reveals that $W(z)$ is a periodic error compensation signal with a period of N samples. If $Q(z)$ is less than unity within the gain cross-over frequency, then

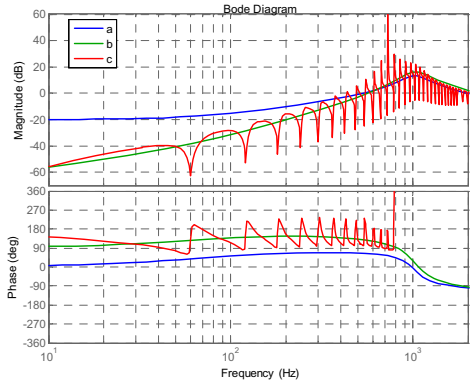

Fig. 11. Output impedance of the inverter under (a) open loop control, (b) closed-loop control without repetitive control, and (c) closed-loop with repetitive control.

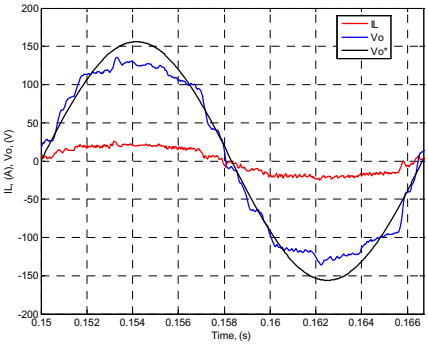

Fig. 12. Simulation result of output voltage with a 5-bit ADC and 10-bit DPWM.

this repetitive compensation signal is asymptotically stable with no periodical disturbances. However, if there are some high-frequency periodical disturbances with their signal spectrum higher than unity, then the system will be unstable due to these periodical disturbances. As the results, $Q(z)$ with low pass filter can filter high-frequency noise and avoid effect about system stable. But when filter bandwidth is not designed appropriately, the system will also be unstable. Therefore, choosing $Q(z)$ is less than one constant as

$$Q(z) = q, \quad 0 < q < 1 \quad (16).$$

The post-delay filter $S(z)$ compensates both the phase delay of the basic servo plant and the main delay loop such that the repetitive control signal can keep the same phase with the cycle disturbance to be eliminated. It has the form of

$$S(z) = gz^{M}, \quad 0 < g < 1 \quad (17)$$

In order to compensate the phase response, the original system $H(z)$ delay angle was shown in Fig. 10, at (17), M is

$$M = N \cdot \left(\frac{\theta}{360}\right) \quad (18)$$

where N is the number of samples fetched in one period. M, as defined in the following, is the equivalent delay samples of the basic servo plant and the main delay loop. Due to the

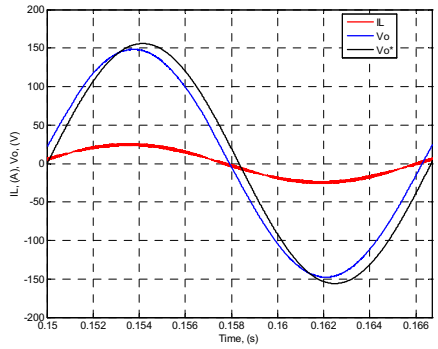

Fig. 13. Simulation results of digital-controlled PWM inverter with a 10-bit ADC and 10-bit DPWM.

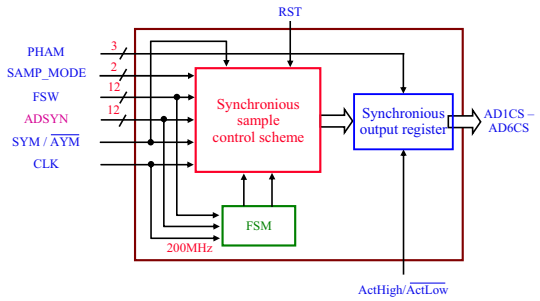

Fig. 14. Function diagram of digital interleaved synchronous sampling controller.

system causality, (17) is impossible implement in real system. Fortunately, error signal is preiodic, so that control force can be compensated at after one period. Therefore, (17) can be modified as

$$S(z) = gz^{M} z^{-N} = gz^{-(N-M)}, \quad 0 < g < 1 \qquad (19)$$

where θ is the phase delay of the basic servo plant and main delay loop at the frequency of the periodic signal. The factor g denotes the convergence rate of the cyclic error and it should be set as a positive real number which is less than one.

Fig. 11 shows the frequency responses of the output impedance of the inverter with and without the repetitive controller. It can be observed that the feedback control with proper phase compensation can achieve an output impedance reduction over a frequency range up to 600 Hz and has a reduction of -20dB compared with open-loop at 60Hz. The repetitive controller can further reduce the output impedance at integer multiple of the reference frequency. It can be observed that an additional -20dB reduction has been obtained at these multiple frequencies.

III. Non-periodic Disturbances Rejection

The limit-cycle-oscillations (LCOs) occur in a nonlinear system may be unstable due to external disturbances. The quantization effect of a digital control system is one major cause that produces significant LCOs due to low bit length or low PWM control resolution. The LCOs is a nonlinear phenomenon, we can't accurately analyze and compensate, [3] proposed the way to avoid LCOs if the DPWM generator resolution is large than ADC resolution. On the other hand,

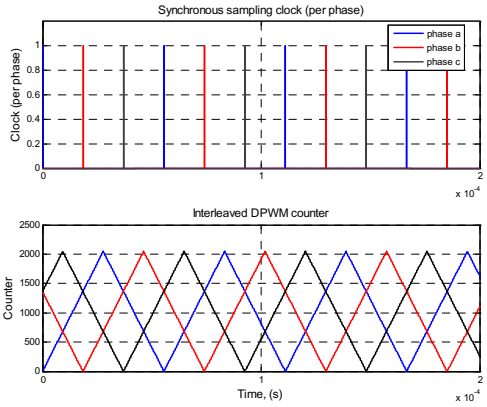

Fig. 15. Simulation results of multi-phase interleaved inverter with synchronous sampling controller.

increasing loop-gain also cause LCOs, [9], [11] uses describing function to derive loop-gain maximum value and predict LCOs occurred condition. However, LCOs still can be resulted from other nonlinear factor. This paper uses repetitive control to reduce quantization device which causes LCOs under setting condition. Fig. 12 and Fig. 13 shows simulation result of output voltage and inductor current under different ADC bit length. In Fig. 12, adopted 5-bit ADC and 10-bit DPWM is shown, the THD is 11.93%. It shows the bit length of the ADC is too low and causes serious LCOs and distortion. Fig. 13 is adopted 12-bit ADC and 10-bit DPWM, the THD is 0.8%. The THD can be reduced with increasing of the ADC resolution.

From Fig. 9 we can obtain the disturbance to error transfer function as

$$\frac{E(z)}{D(z)} = \frac{1 - Q(z)z^{-N}}{(1 + C_{DB}(z)P(z)) \cdot [1 - z^{-N}(Q(z) - H(z)S(z))]} \qquad (20)$$

if $Q(z)$ =1, then $E(z)$ = 0, the error which influence by disturbance can be completely eliminated. In practical case, $Q(z)$ =1 can cause poles on unit circle, which is, based on (16). Appropriately choosing q can reduce disturbance result effect of error signal.

IV. Digital Controller Hardware Circuit Implementation

Using FPGA to implement digital controller has several advantage in PWM converter. In this paper, main project is to implement interleaved synchronize sampling controller and digital phase-shifted PWM generator. Detail analysis is discussed as follow.

A. Interleaved Synchronize Sampling Scheme

In order to reduce the sampling noises inducted by the switching of the power devices and get an accurate value of the average current of the switching inductor current, a synchronized controller for the multiplexed ADC converter is designed. Fig. 14 shows the functional block diagram of the digital synchronous controller. A double frequency sampling signal is generated to sample the mid-point of the

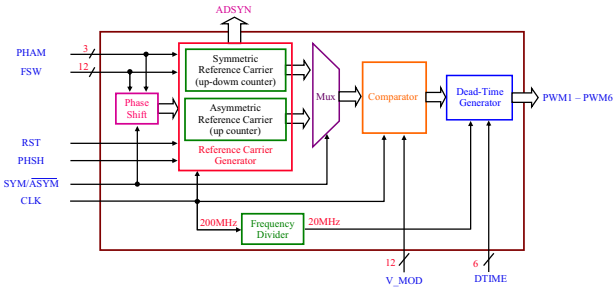

Fig. 16. Functional diagram of programmable digital phase-shifted PWM generator.

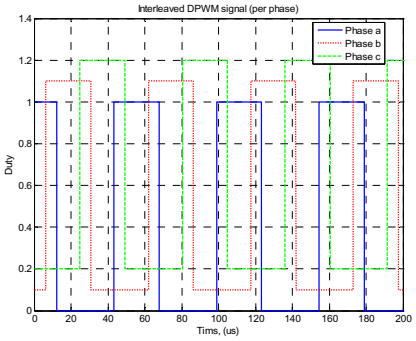

Fig. 17. Simulation results of the three-phase interleaved PWM signals.

rising and falling slope of each phase inductor current.

Fig. 15 shows digital interleaved synchronous sampling controller simulation result, send sampling clock at digital counter to zero, can sampling inductor current each phase mid-point of the rising slope, it can also set sending sampling clock at digital counter to maximum value, and sampling inductor current per phase mid-point of the falling slope.

B. Digital Phase-Shift PWM Generator

The error signal is processed through a digital control algorithm to generate a digital actuating signal. This signal is then converted to a switching signal via a digital PWM (DPWM) generator with a specified switching frequency and duty at the each sampling instant. The DPWM is usually realized by a programmable counter and its resolution will be limited by its highest clock frequency and maximum switching frequency. The PWM frequency is usually synchronized with an integral multiplier of the sampling frequency for the digital loop compensator to avoid beat phenomenon. Implementation function diagram of programmable digital phase-shifted PWM generator is shown as Fig. 16. Fig. 17 shows simulation results of the three-phase interleaved PWM signals, with a 120 degree phase shift, setting switching frequency is 24KHz. The digital circuit implementation of the interleaved PWM signal generator can achieve fast and high accuracy timing control even with a limited control resolution.

V. System Integration Simulation Results

This paper simulation platform is based on integrated with

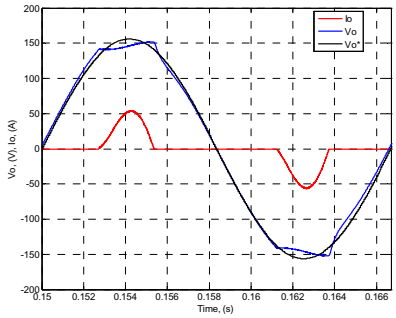

Fig. 18. Simulation results of output voltage under nonlinear load without employing the repetitive controller.

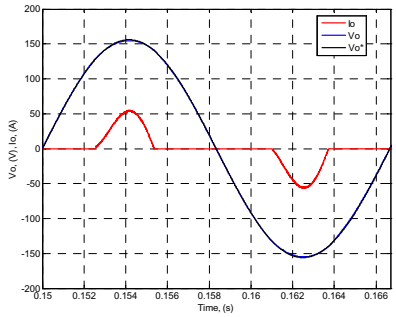

Fig. 19. Simulation results of output voltage under nonlinear load with employing the repetitive controller.

the Matlab/Simulink and Modelsim simulation software. The Simulink not only simulate the digital signal processing, it can also simulate in the analog environment. Thus, we could quickly revise the errors. We used the power block set toolbox of Simulink and constructed a three-phase inverter system in Modelsim, we aloes use VHDL language design to implement digital controller. The programmable feature of FPGA allows designers to construct complex digital circuits easily. Therefore, it is applicable to employ FPGA as a digital controller for power conversion. One special feature of the EP2C35 is that it provides a virtual embedded processor, the NIOS II. It processes many soft IPs such as RAM or ROM controllers, communication interfaces, etc. Designers can employ these IPs to build a communication bridge to the host computer or other multiple applications. Table I shows system specification in this paper.

Fig. 18 shows simulation results of output voltage under nonlinear load without employing the repetitive controller, the output power P_o is 1350W, the output current $I_{o,\mathrm{rms}}$ is 18A, and the current crest factor is 3. Fig. 18 shows a serious distortion effect due to the nonlinear current, and output voltage THD is 6.45%. Fig. 19 shows simulation results of output voltage under nonlinear load with employing the repetitive controller and it shows output voltage distortion has been reduced significantly by repetitive control. The output voltage can reach a very low THD of 1.78% even with a highly nonlinear load. Fig. 20 shows simulation results of output voltage error convergence when the repetitive controller at activated at 0.4sec, the convergence

TABLE I
SYSTEM PARAMETERS

Symbol	Quantity	Data
$V_{o(\mathrm{rms})}$	reference voltage	110V
V_{dc}	input voltage	400V
P_o	full load output power	2KW
m	number of phase	3
f_{sw}	switching frequency	18KHz
L_i	phase inductors (i=1, 2, 3, 4)	675uH
C_o	output capacitor	36uF
r_L	inductance equivalent series resistance	0.5Ω
r_C	capacitor equivalent series resistance	0.1Ω
f_{sample}	sample frequency	18KHz

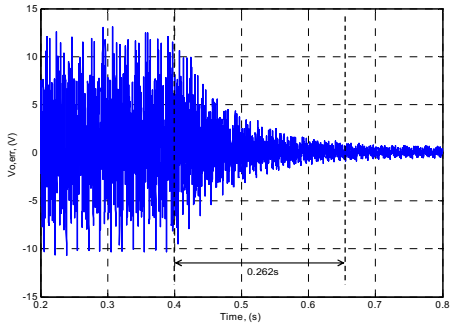

Fig. 20. Simulation results of output voltage error convergence under repetitive controller.

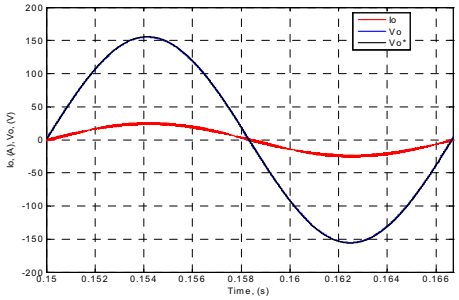

Fig. 21. Simulation results of output voltage under linear load with repetitive controller.

time is about 0.262sec, and the steady-state error can be reduced from 20V to 1.8V. The simulation results illustrate that the designed digital PWM inverter controller can achieve a robust transient response and a steady-state response with very low THD. Fig. 21 shows simulation results of output voltage under linear load with repetitive control, the ADC is 5-bit, and control resolution of the DPWM generator is 10-bit. It can be observed that the THD is reduced to 2.8%. Though still higher than THD of the nonlinear load in Fig. 19, but below a performance specification of THD ≤ 3% under repetitive control is satisfied.

VI. CONCLUSION

In application of digital control technique to the design of a high-performance PWM inverter, quantization effect of the ADC and DPWM may result significant limit cycle oscillations (LCOs) with a reduction of bit length. This paper presents a digital repetitive control scheme for the output voltage of a multi-phase interleaved PWM inverter under nonlinear load, to reduce periodic error, and achieve minimization control of the THD. The results can be used for the synthesis of the digital controller for closed-loop regulation of PWM inverters with lowest resolution of analog-to-digital converter to realization of the digital control of PWM inverter. In order to improve the current sharing control and the dynamic response, a digital-controlled synchronous sampling controller and digital phase-shifted PWM generator have been developed. The implementation of the digital controller was realized by using an Altera's single-chip FPGA device EP2C35. A co-simulation technique by using Modelsim and Simulink has been used to verify the proposed control scheme and designed hardware circuit. Simulation results shows the THD of a multi-phase interleaved PWM inverter can be reduced to 1.78% with a rated rectifier load of crest factor 3 by using only a 5-bit ADC converter. This reveals the great opportunity of design low-cost high-performance digital inverter control IC for high power CCFL back light modules.

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