IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

Fabrication of Novel Three-Step Drift-Doped Low-Temperature Polycrystalline Silicon Lateral Double-Diffusion Metal–Oxide–Semiconductor Using Excimer Laser Crystallization

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2009 Jpn. J. Appl. Phys. 48 031204

(http://iopscience.iop.org/1347-4065/48/3R/031204)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 25/04/2014 at 11:20

Please note that terms and conditions apply.

Fabrication of Novel Three-Step Drift-Doped Low-Temperature Polycrystalline Silicon Lateral Double-Diffusion Metal–Oxide–Semiconductor Using Excimer Laser Crystallization

Jyh-Ling Lin*, Huang-Jen Chen, Fang-Long Chang[1], and Huang-Chung Cheng[1]

Department of Electronic Engineering, Huafan University, Shintin, Taipei 223, Taiwan
[1]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan*

Received September 1, 2008; accepted December 6, 2008; published online March 23, 2009

Low-temperature polycrystalline silicon (poly-Si) thin-film transistor lateral double-diffusion metal–oxide–semiconductor field-effect transistors (LTPS TFT LDMOSFETs) and lateral insulated-gate bipolar transistors (LIGBTs) were fabricated by combining a thin-film transistor with a power structure, three-step drift doping, and excimer laser annealing. The maximum breakdown voltage of the three-step drift-doped LTPS-LDMOS after excimer laser annealing is 286 V with a 35 μm drift region length (L_{drift}). The specific on-resistance is low (approximately 9 Ω cm^2) and the ON/OFF current ratio is about 1.28 x 10^6 with L_{drift} = 15 μm. The subthreshold swing (SS) is about 1 V/decade. Comparing the three-step drift-doped LDMOS with the three-step drift-doped LIGBT under the same processing conditions clearly indicates that the breakdown voltage and current capacity of LIGBT exceeds those of LDMOS.
© 2009 The Japan Society of Applied Physics

DOI: 10.1143/JJAP.48.031204

1. Introduction

Recently, power devices and related products have been continuously studied and improved for applications in many fields. In particular, lateral power devices are continuously being developed to improve system-on-chips (SOCs) and to facilitate integration with other circuits in the complementary metal–oxide–semiconductor (CMOS) process. Lateral power devices include conventional lateral double-diffusion metal–oxide–semiconductors (LDMOSs), super-junction LDMOSs, and lateral insulated-gate bipolar transistors (LIGBTs), among others.[1–5] LDMOS is a voltage-controlled device with a gate control circuit that is simple and suitable for integration. LIGBT has the high input impedance of an MOS-gate structure and a higher overall current density during forward conduction than power MOS field-effect transistors (MOSFETs).

In recent years, low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been widely studied and discussed for devices such as active-matrix liquid crystal displays (AMLCDs), active-matrix organic light-emitting displays (AMOLEDs), and plasma display panels.[6–9] Accordingly, the requirement for high-voltage circuits in these devices has increased. Thus, low-temperature poly-Si high-voltage TFTs (LTPS HVTFTs) will become increasingly important in the future as system-on-panel (SOP) and three-dimensional (3D) circuits are integrated.

In this investigation, LTPS-LDMOS and LTPS-LIGBT were implemented in three steps of doping and by combining silicon-on-insulator (SOI), low-temperature thin-film transistor technology and a power device, with the structure shown in Fig. 1. A linear doping profile in the drift region is necessary to provide a more uniform electrical field distribution and to yield a high breakdown voltage. To obtain a linear doping profile in the drift region, a sequence of small opening oxide slits, called the variation in lateral doping (VLD) technology, is used. However, this technology has some shortcomings: for example, it requires a complex mask layout and a long annealing time to ensure linear doping.[10,11] In 1995, Sunkavalli *et al.* used the distinct doping region along the lateral direction to replace the linear profile in the drift region.[12] Subsequently, some numerical analyses (including that performed by our group) yielded models that can optimize the doping profile, step-doping number, and thermal process time.[13,14]

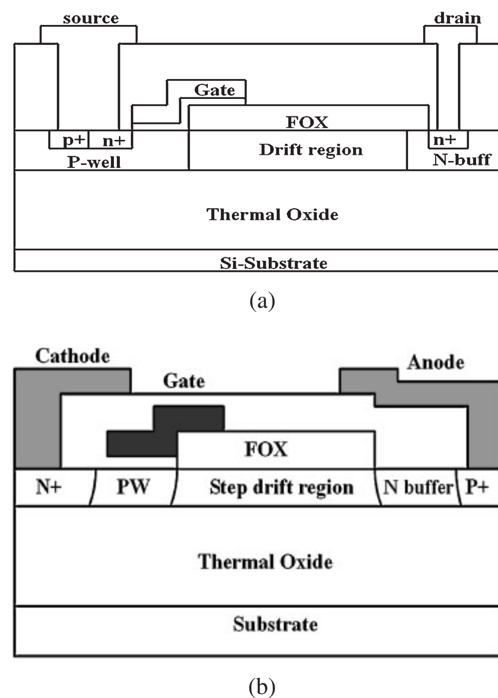

Fig. 1. Structure of (a) LTPS-LDMOS and (b) LTPS-LIGBT.

A structure with a step doping profile in the drift region shows a high performance in LDMOSFETs.[15] Thus, in this work, three doping steps in the drift region were designed and excimer laser crystallization (ELC) and solid phase crystallization (SPC) were performed to crystallize amorphous silicon (a-Si) in an LDMOSFET and an LIGBT fabricated on the same oxide substrate. ECL is the most promising technique for growing large poly-Si grains and it cannot cause damage to the glass substrate because of a large

*E-mail address: cllin@huafan.hfu.edu.tw

 © 2009 The Japan Society of Applied Physics

absorption coefficient for a-Si in the UV light region (optical absorption coefficient > 10^6 cm^{-1}).[16–19] The grain boundary causes many defects, which act as trap states in the band gap and degrade the electrical characteristics of devices, such as threshold voltage, mobility, and subthreshold swing. In this work, we focused on the study of LTPS-LDMOSFETs and compared LDMOS with LIGBT.

2. Device Fabrication

The key processes in the fabrication of LTPS-LDMOS are as follows. Step 1: grow a 1-μm-thick layer of thermal oxide on a (100) silicon wafer, replacing the glass substructure. Step 2: deposit amorphous silicon to a thickness of 1000 Å on the oxide with pure silane (SiH_4) by low-pressure chemical vapor deposition (LPCVD) at 550 °C to form the device active layer. Step 3: use ion implantation to produce the p-well and n-buffer to increase the size of the depletion region, using a boron dose of 3.0×10^{13} cm^{-2} at 60 keV and a phosphorous dose of 3.0×10^{13} cm^{-2} at 60 keV. In the drift region, three doping steps were adopted to produce a linearlike doping profile, reducing drift region resistance. The implantation phosphorus doses are 2.3×10^{11}, 7.0×10^{11}, and 1.3×10^{12} cm^{-2} at 50 keV. The n-buffer layer, the drift region, and the p-well form the punch-through diode, reducing the surface-field (RESURF) effect and increasing the integration area of the electric field. Step 4: crystallize the 1000-Å-thick layer of amorphous silicon using a KrF excimer pulse laser ($\lambda = 248$ nm) with an optimal laser energy of 430 mJ/cm^2 and 100 shots per cm^2 with substrate heating at 400 °C in a vacuum chamber of 10^{-3} Torr. It was found that a large grain size could be realized by controlling the solidification of silicon under these conditions.[19,20] Figure 2 shows a scanning electron microscopy (SEM) image of poly-Si. Step 5: deposit a 3000-Å-thick layer of tetraethylorthosilicate (TEOS) as the field oxide (FOX) by LPCVD. FOX can reduce the surface electric field between the gate and the anode edge in the drift region. Step 6: deposit a 1000-Å-thick layer of TEOS as the gate oxide by LPCVD and a 2000-Å-thick layer of amorphous silicon as the gate electrode by LPCVD at 550 °C. Step 7: implant phosphorus at 5.0×10^{15} cm^{-2} and 60 keV to form the n+ source and drain, and improve the conductivity of the gate. Step 8: deposit a 5000-Å-thick TEOS layer as a passive oxide layer by LPCVD and then activate all dopants by furnace annealing at 600 °C for 12 h. Finally, deposit four metals (Ti/TiN/AlSiCu/TiN) on the passive oxide as contact metals by metal-CVD. The thickness of the metal layer should be fixed at 6000 Å.

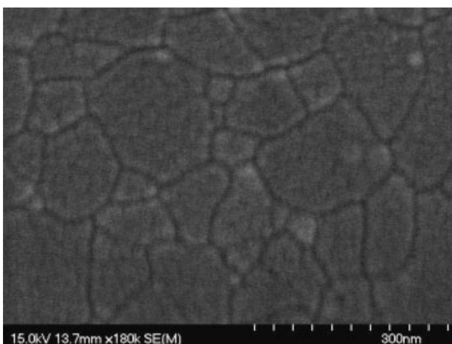

Fig. 2. SEM of excimer laser-crystallized poly-Si at laser density of 430 mJ/cm^2 with substrate heating at 400 °C.

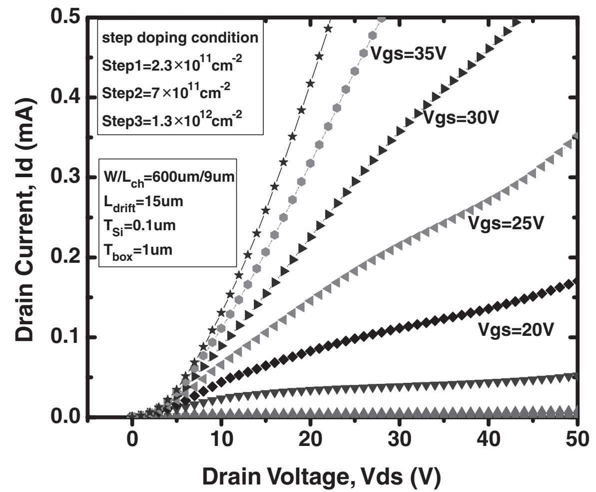

Fig. 3. Output characteristics of ELC LTPS-LDMOS with three-step doping.

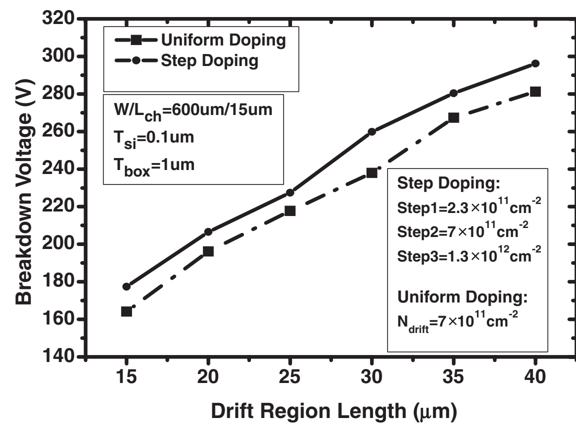

Fig. 4. Breakdown voltages of uniform and three-step doping drift regions versus length of drift region.

3. Results and Discussion

3.1 Electrical characteristics

Figure 3 shows the basic output characteristics of ELC LTPS-LDMOS. The drain current is about 0.35 mA at $V_{ds} = 50$ V and $V_{gs} = 25$ V. The device dimensions and doping concentration are $W = 600$ μm, $L_{ch} = 9$ μm, $L_{drift} = 15$ μm, $N_{drift\text{-}step} = 2.3 \times 10^{11}$, 7×10^{11}, and 1.3×10^{12} cm^{-2}, $T_{si} = 0.1$ μm, and $T_{box} = 1$ μm. Figure 4 shows the breakdown voltages of uniform and step doping in the drift region as a function of drift region length with $L_{ch} = 15$ μm at $V_g = 0$ V. The breakdown voltage varies with the length of the drift region. When the drift region was extended, the breakdown voltage of uniform doping increased from about 160 to 280 V at a fixed channel length (L_{ch}) of 15 μm, following a linearity of about 4.8 V/μm. The breakdown voltage of step doping also increased from about 180 to 300 V. This phenomenon is also clearly observed with other channel lengths. The results clearly show that devices with three-step doping provide a more uniform electrical field distribution along the drift region with higher breakdown voltages than uniformly doped devices.

© 2009 The Japan Society of Applied Physics

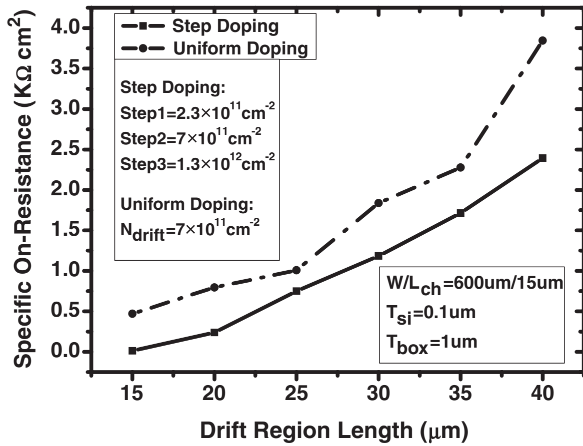

Fig. 5. Specific on-resistances of uniform and three-step doping drift regions versus length of drift region.

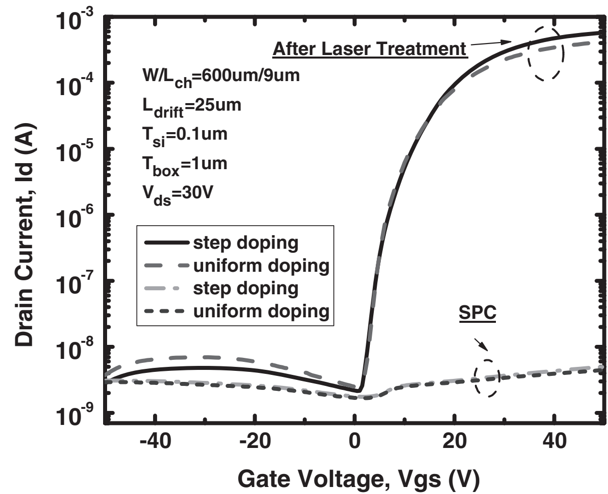

Fig. 6. LTPS-LDMOS transfer characteristics of SPC and ELC for uniform and three-step doping with $L_{drift} = 25\,\mu$m and $L_{ch} = 9\,\mu$m.

Figure 5 shows specific on-resistances ($R_{on,sp}$) for various drift lengths and doping profiles. The specific on-resistances were defined as

$$R_{on,sp} = \left(\frac{V_{ds}}{I_d}\right) \times [W \times (L_{ch} + L_{drift})],$$

where W, L_{ch}, and L_{drift} represent the device width, channel length, and drift region length, respectively. V_{ds} and I_d are the drain–source voltage and its corresponding drain current in the triode region, respectively. The gate-source voltage was set at $V_{gs} = 30$ V. The specific on-resistances of step doping increased from about $9\,\Omega\,\mathrm{cm}^2$ to $2.5\,\mathrm{k}\Omega\,\mathrm{cm}^2$ when the drift region length ranged from 15 to $40\,\mu$m, and they were clearly lower than those of uniform doping.

Excimer laser annealing crystallizes silicon thin film from amorphous to single-crystal material within a very short time by melting the silicon. The amorphous thin film is heated to a temperature of about 1200 °C during laser irradiation for approximately 10 ns. The thin film rapidly melts and solidifies, without thermal damage to the substrate, thermal compaction problems, or impurity diffusion from the substrate to the silicon thin film. Thus, this technology yields high-quality and large-grained poly-Si thin films for LTPS LDMOSs on glass substrates. The performance of poly-Si thin film has been shown to be related to the initial status of a-Si precursor film and the ELC conditions, such as laser energy density, laser pulse duration, laser shot number per area, ambient, and substrate temperature.[20–23] If the process and excimer laser systems exhibit optimal conditions, the specific on-resistance of uniformly doped LTPS LDMOS may be reduced to about $0.54\,\Omega\,\mathrm{cm}^2$, which is only five times higher than that of single-crystalline silicon LDMOS, with the same order of block capability.[19] In this study, uniformly doped and three-step-doped LTPS LDMOSs were manufactured by the same process within the same time. The performance of specific on-resistance is lower than that reported in our previous paper. However, three-step doping could clearly improve block capability and on-resistance even in LTPS LDMOSs. Thus, a high-performance LTPS-LDMOS with a low specific on-resistance of less than $0.54\,\Omega\,\mathrm{cm}^2$ can be realized.

Figure 6 shows four gate transfer curves of TFT-LDMOS between SPC and ELC for uniform and three-step doping. The SPC process temperature was maintained at 600 °C in N_2 ambient and the process time was about 24 h. The drain current of the TFT-LDMOS fabricated by ELC and step doping was about 0.8 mA at $V_{ds} = 30$ V and $V_{gs} = 50$ V. The negative gate bias current was almost constant even as the drain voltage was increased to 30 V, because the extended gate and drift region design effectively reduced the junction electric field in the p-well and the n-drift region.[14] The ON/OFF current ratio of step doping was 2.06×10^5 higher than that of uniform doping after laser treatment. The subthreshold swing (SS) of the three-step drift-doped LTPS-LDMOS was about 1 V/decade, showing a low number of deep states in polysilicon.[24]

3.2 Uniformity

In this section, the uniformity of excimer laser treatment for three-step drift-doped LTPS LDMOSFETs is discussed. Figure 7 shows the percentage distribution of variation voltage for maximum transconductance under different drift region lengths. For each length, five devices were taken from different regions (A, B, C, D, and E) of the same wafer. The devices were fixed at $15\,\mu$m channel length. The transconductance is defined as

$$g_m = \frac{\partial I_d}{\partial V_{gs}},$$

where V_{ds} is fixed at 10 V. The corresponding voltage of g_m maximum is

$$V_{gs,max} = V_{gs}\left(\frac{\partial g_m}{\partial V_{gs}} = 0\right).$$

The percentage of variation voltage is taken from

$$\Delta\% = \frac{V_{gs,max} - V_{gs,ave}}{V_{gs,ave}}\ (\%),$$

where $V_{gs,ave}$ is the average voltage of $V_{gs,max}$ for a fixed drift region length. In Fig. 7, the variation in maximum transconductance is less than ±5% for a $25\,\mu$m channel length.

© 2009 The Japan Society of Applied Physics

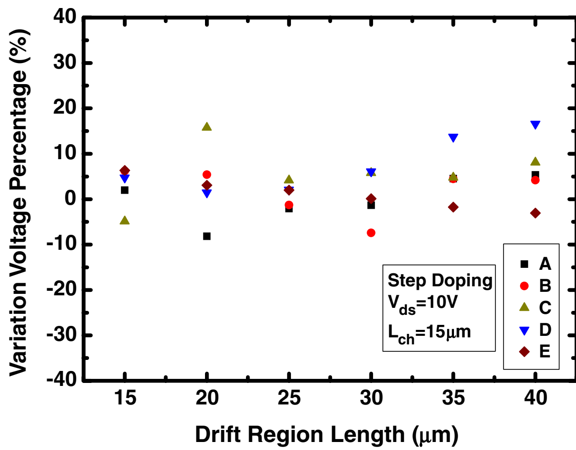

Fig. 7. (Color online) Percentage distribution of variation voltage for transconductance maximum versus drift region length.

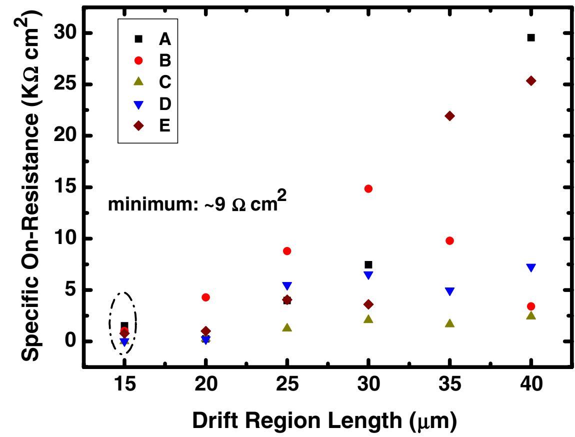

Fig. 9. (Color online) Statistics and uniformity of specific on-resistance. Five ELC LTPS-LDMOSs with three-step doping were measured at a fixed drift region length.

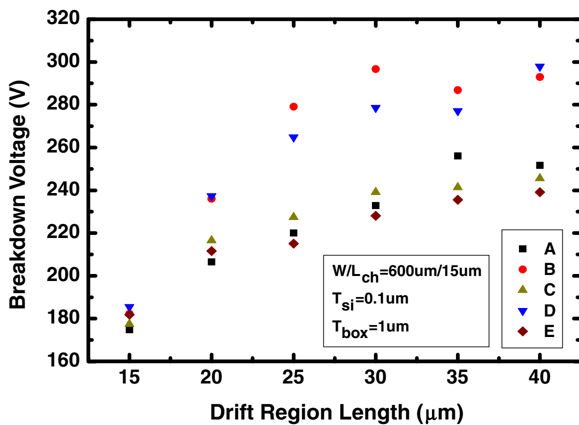

Fig. 8. (Color online) Statistics and uniformity of breakdown voltage. Five ELC LTPS-LDMOSs with three-step doping were measured at a fixed drift region length.

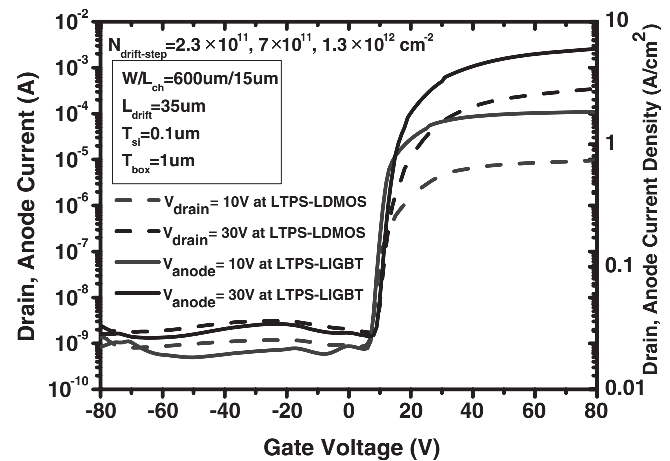

Fig. 10. Transfer characteristics of three-step doped LTPS-LDMOS and LTPS-LIGBT using ELC.

Figure 8 shows the corresponding breakdown voltage distribution. The breakdown voltage variation is small when the drift region length is 15 μm. However, the variation clearly increases when the drift region length exceeds 25 μm. Although excimer laser crystallization has the potential to improve the crystallinity of poly-Si thin films, the narrow excimer laser crystallization process window and the uniformity of the crystallized poly-Si thin films are serious problems. In addition, the shot-to-shot laser energy of the excimer laser is insufficiently stable and the seeds of crystallization distribute randomly during laser recrystallization. These phenomena cause the excimer laser crystallization to result in a poor device-to-device uniformity, particularly for large-area devices. Therefore, the uniformity is a problem when the drift region length exceeds 25 μm and the variation in breakdown voltage is large. These phenomena were also observed for specific on-resistance. The distributions of specific on-resistance for various drift region lengths are shown in Fig. 9. The drift region lengths of less than 15 μm have low specific on-resistance and low variation. The variation range increases with drift region length extension.

Regarding the issues mentioned above, many laser crystallization technologies have been proposed to produce large grains with more uniform distribution, such as phase-modulated ELC, dual beam ELA, continuous-wave laser lateral crystallization, and selectively enlarging laser crystallization.[25–28] Low-temperature poly-Si thin-film power devices combining the new technology and new structure that produce large grains to promote uniformity and high performance will be our next topic for investigation.

3.3 Comparison of LDMOSFETs and LIGBTs with three-step doping

In this section, we compare the performance characteristics of the LTPS-LDMOS and LTPS-LIGBT fabricated on the same wafer. The on current of LTPS-LIGBT exceeds that of LTPS-LDMOS, as shown in Fig. 10, clearly indicating that LIGBT has a high current density. Figure 11 shows the corresponding ON/OFF current ratios for 15, 25, and 35 μm drift region lengths. The ON/OFF current ratios of LTPS-LDMOS are smaller than those of LTPS-LIGBT. The on current of LIGBT with $L_{drift} = 15$ μm is limited by the measurement system. Figure 12 shows the average breakdown voltage and specific on-resistance of LDMOS and LIGBT with $L_{drift} = 25$ μm and $L_{ch} = 15$ μm. The breakdown voltage and specific on-resistance of LIGBT are improved by about 7 and 90% compared with those of

 © 2009 The Japan Society of Applied Physics

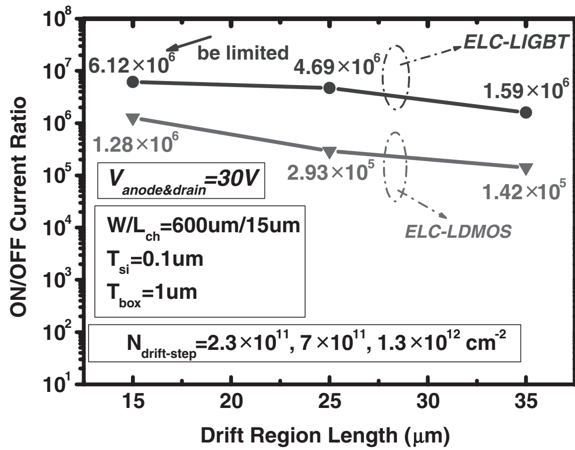

Fig. 11. ON/OFF current ratios for three-step doped LTPS-LDMOS and LTPS-LIGBT using ELC at $V_{\text{drain,anode}} = 30\,\text{V}$.

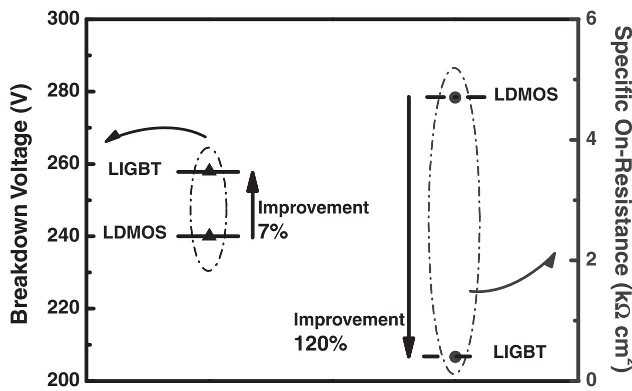

Fig. 12. Breakdown voltage and specific on-resistance improvement of three-step doping LDMOS and IGBT with excimer laser crystallization.

LDMOS, respectively. As we know, insulated-gate bipolar transistors possess superior on-state characteristics, an excellent safe operating area, and a reasonable switching speed. They have replaced bipolar power transistors in medium power applications. However, LDMOS is a unipolar device, so it has a high inherent switching speed. The results presented in this paper reveal that the total DC performance of the LTPS-LDMOS and LTPS-LIGBT using thin films supports integration with other driving circuits on the panel.

4. Conclusions

In this work, we investigated the three-step doping drift region of LTPS-LDMOS and LTPS-LIGBT following excimer laser annealing. The step-doping drift region treated by excimer laser annealing was herein linearly doped instead. The breakdown voltage of LTPS-LDMOS depends on not only the drift region length but also the doping profile. Our research conclusions are summarized as follows:

(1) The maximum breakdown voltage of LTPS-LDMOS reaches about 220–300 V when the drift region lengths of the devices are designed to exceed 25 μm. The specific on-resistance is low (about $9\,\Omega\,\text{cm}^2$) with $L_{\text{ch}} = 15\,\mu\text{m}$ and $L_{\text{drift}} = 15\,\mu\text{m}$.

(2) The $I_{\text{ON}}/I_{\text{OFF}}$ ratio for three-step doping exceeds that for uniform doping and the subthreshold swing (SS) is about 1 V/decade.

(3) Comparing the three-step doped LDMOS with the three-step doped LIGBT under the same processing conditions clearly indicates that the breakdown voltage of LIGBT exceeds that of LDMOS.

Acknowledgments

The authors wish to thank the National Nano Device Laboratories (NDL) and National Science Council of the R.O.C., Taiwan for financially supporting this research under Contract no. NSC 95-2221-E-211-021.

1) B. J. Baliga: *Power Semiconductor Devices* (PWS, Boston, MA, 1995) Chap. 7, p. 335.
2) D. A. Grant and J. Gowar: *Power MOSFET: Theory and Applications* (Wiley, New York, 1989) Chap. 1, p. 15.
3) R. Allen and J. R. Hefner: IEEE Trans. Power Electron. **5** (1990) 459.
4) N. Thapar and B. J. Baliga: Proc. ISPSD, 1994, p. 177.
5) T. Fujihira: Jpn. J. Appl. Phys. **36** (1997) 6254.
6) Y. Oana: J. Soc. Inf. Disp. **9** (2001) 169.
7) J. G. Blake, J. D. Stevens III, and R. Young: Solid State Technol. **41** (1998) 56.
8) M. Kimura, I. Yudasaka, S. Kanbe, H. Kobayashi, H. Kiguchi, S. Seki, S. Miyashita, T. Shimoda, T. Ozawa, K. Kitawada, T. Nakazawa, W. Miyazawa, and H. Ohshima: IEEE Trans. Electron Devices **46** (1999) 2282.
9) C. W. Chen, T. C. Chang, P. T. Li, H. Y. Lu, K. C. Wang, C. S. Huang, C. C. Ling, and T. Y. Tseng: IEEE Electron Device Lett. **26** (2005) 731.
10) S. Zhang, J. K. Sin, T. M. Lai, and P. K. Ko: IEEE Trans. Electron Devices **46** (1999) 1036.
11) F. Udrea, D. Garner, K. Sheng, A. Popescu, H. T. Lim, and W. I. Milne: Electron. Commun. Eng. J. **12** (2000) 27.
12) R. Sunkavalli, A. Tamba, and B. J. Baliga: Proc. Int. Conf. IEEE SOI, 1995, p. 139.
13) F. L. Chang, M. J. Lin, G. Y. Lee, Y. S. Chen, C. W. Liaw, and H. C. Cheng: Solid-State Electron. **47** (2003) 1693.
14) Y. Guo, Z. Li, and B. Zhang: Microelectron. J. **37** (2006) 861.
15) J. Luo, G. Cao, S. N. Ekkanath Madathil, and M. M. De Souza: Solid-State Electron. **47** (2003) 1937.
16) Y. Nonaka, H. Tsuchi, H. Haga, H. Asada, H. Hayama, N. Takada, and K. Sera: SID Int. Symp. Dig. Tech. Pap. **34** (2003) 1392.
17) T. F. Chen, C. F. Yeh, C. Y. Liu, and J. C. Lou: IEEE Electron Device Lett. **25** (2004) 396.
18) F. L. Chang, M. J. Lin, C. W. Liaw, and H. C. Cheng: IEEE Electron Device Lett. **25** (2004) 547.
19) H. C. Cheng, F. L. Chang, M. J. Lin, C. C. Tsai, and C. W. Liaw: J. Electrochem. Soc. **151** (2004) G900.
20) H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, H. Kawata, M. Osumi, S. Tsuda, S. Nakano, and Y. Kuwano: Jpn. J. Appl. Phys. **30** (1991) 3700.
21) S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, and M. J. Trainor: J. Appl. Phys. **82** (1997) 4086.
22) H. Kuriyama, T. Nohda, S. Ishida, T. Kuwahara, S. Noguchi, S. Kiyama, S. Tsuda, and S. Nakano: Jpn. J. Appl. Phys. **32** (1993) 6190.
23) A. T. Voutsas, A. M. Marmorstein, and R. Solanki: J. Electrochem. Soc. **146** (1999) 3500.
24) I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang: IEEE Electron Device Lett. **12** (1991) 181.
25) C. H. Oh, M. Ozawa, and M. Matsumura: Jpn. J. Appl. Phys. **37** (1998) L492.
26) R. Ishihara and A. Burtsev: Jpn. J. Appl. Phys. **37** (1998) 1071.
27) A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, and M. Chida: Jpn. J. Appl. Phys. **43** (2004) 1269.
28) M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, and T. Shiba: IEEE Trans. Electron Devices **51** (2004) 934.

© 2009 The Japan Society of Applied Physics