Resist-Related Damage on Ultrathin Gate Oxide During Plasma Ashing

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***Abstract*— This paper presents an important observation of plasma-induced damage on ultrathin oxides during O_2 plasma ashing by metal "antenna" structures with photoresist on top of the electrodes. It is found that for MOS capacitors without overlying photoresist during plasma ashing, only minor damage occurs on thin oxides, even for oxide thickness down to 4.2 nm and an area ratio as large as 10^4. In contrast, oxides thinner than 6 nm with resist overlayer suffer significant degradation from plasma charging. This phenomenon is contrary to most previous reports. It suggests that the presence of photoresist will substantially affect the plasma charging during ashing process, especially for devices with ultrathin gate oxides.**

I. Introduction

PLASMA damage on thin oxides has been studied extensively in recent years [1]–[4]. As devices keep scaling down to the deep-submicrometer regime, plasma damage becomes a major issue for maintaining device reliability. Among several plasma processes, plasma ashing is often thought to induce the most serious damage, as the wafers are directly exposed to the plasma at the end of process [5]. It is intuitively thought that fully exposed wafers without resist protection will suffer more severe damage from plasma ashing [6]. Usually, the experiments were performed either under deliberate nonuniform plasma environment [5] or prolonged direct exposure without resist covering [6], in order to magnify the degree of damage for easy analysis. In this paper, we report observations which are contrary to this hypothesis. To be specific, our results show that only insignificant damage on thin oxides is found by direct plasma exposure, even for devices with oxide thickness as thin as 4.2 nm and an antenna area ratio $(A_f/A_g = ARR)$ of 10^4. In contrast, when the metal electrodes are covered with resist overlayer, the presence of photoresist induces an alternate charging process which causes severe degradation for oxides thinner than 6 nm. This resist-related charging phenomenon in plasma ashing, to the best of our knowledge, has never been reported before. Since the wafers are always covered with resist layer in actual fabrication processes, this resist-related charging damage during ashing could have significant impacts on the reliability of future devices employing ultrathin gate oxides.

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II. Experiments

The plasma damage on thin gate oxide was measured through metal antenna test structure which is illustrated in the inset of Fig. 1. MOS capacitors were fabricated on 6-in p-type (100) 15–25 Ω-cm silicon wafers. Active regions with area of 20×20 μm^2 were defined by LOCOS isolation with field oxide thickness of 500 nm. Ultrathin gate oxides were grown in dry oxygen ambient at 900 °C, followed by polysilicon deposition at 620 °C and saturation-doping with $POCL_3$ at 950 °C. Poly-electrodes, which completely cover the entire active regions to prevent the thin oxides from direct exposure to UV radiation and ion bombardment, were patterned by electron-cyclotron-resonance (ECR) plasma etching. A 0.5-μm TEOS oxide was then deposited for dielectric passivation. Finally, antenna structures were defined by wet etching after 1-μm thick aluminum film deposition. The antenna area ratios $(AR = A_f/A_g)$, were varied from 16 to 10^4. A commercial O_2/CH_3OH downstream plasma resist asher was used to evaluate damage on thin oxides. The ashing process was performed at 13.56 MHz, 1.5 torr, and 800 W. Wafers were kept at 200 °C during ashing. Capacitors were split into two groups. One group was processed with wet resist removal prior to ashing, while the other was processed with the presence of resist during ashing. All samples received the normal ashing process for 170 s. Finally, as devices received a 400 °C post-metal-anneal (PMA) for 30 min the current–voltage (I–V) characteristics were measured using the HP 4145B parameter analyzer.

III. Results and Discussion

Fig. 1 shows the radial charge-to-breakdown (Q_{bd}) distributions of different thin oxides across the wafer after plasma exposure for wafers without [Fig. 1(a)] or with [Fig. 1(b)] resist overlayer on the antenna electrodes. A constant stress current density of -200 mA/cm^2 (i.e., gate injection) at 25 °C was applied during Q_{bd} measurements. AR values of 16 and 10^4 are employed to clarify the antenna area effect. The position-independent variation of Q_{bd} is clearly illustrated in Fig. 1(a) for those devices without resist protection. Specially, only about 1 Coulomb/cm^2 degradation is observed even when oxide thickness is reduced to 4.2 nm and the antenna ratio (AR) is increased from 16 to 10^4. However, for those samples with resist overlayer, surprising results are observed. As shown in Fig. 1(b), 8-nm oxides do not suffer any degradation by evaluation of the constant current stress method. While for

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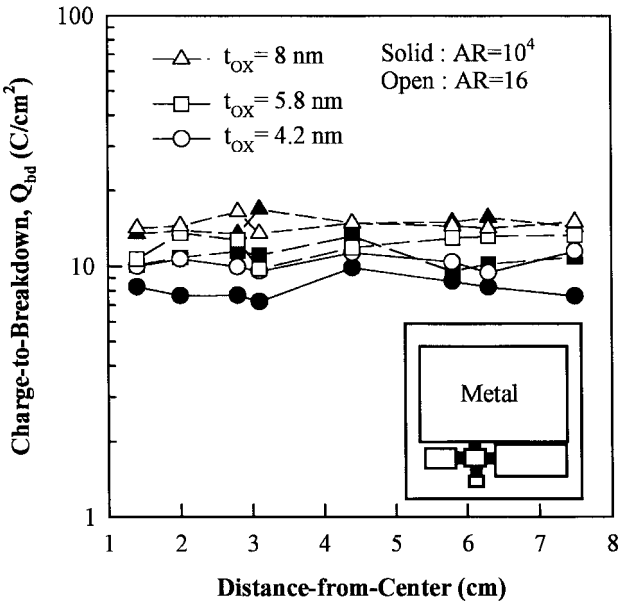
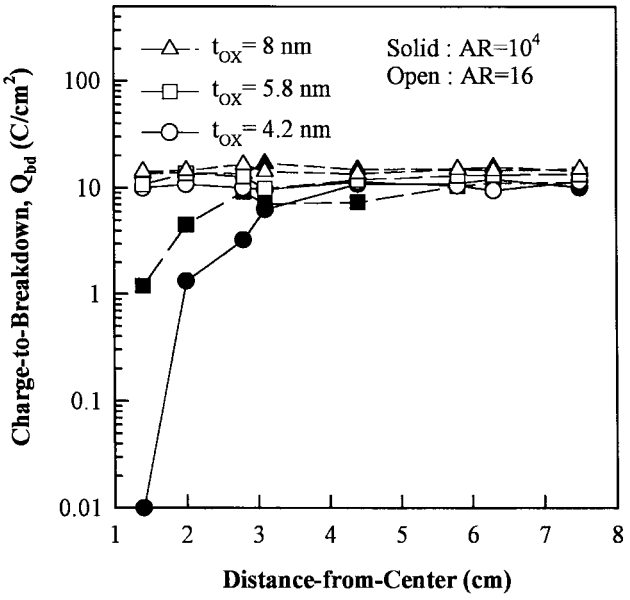


(a)



(b)

Fig. 1. The radial charge-to-breakdown (Q_{bd}) distribution of different thin oxides across the wafer after exposure to O_2 plasma (a) without resist, and (b) with resist overlayer on the antenna electrodes. The active region area is $20 \times 20\ \mu m^2$ and the constant current stress density is -200 mA/cm^2 (i.e., gate injection). The thicknesses of thin oxides are 8 nm, 5.8 nm, and 4.2 nm, respectively. Solid symbols represent the antenna area ratio of 10^4 and open symbols represent the antenna ratio of 16. The inset is the diagram of metal antenna structure.

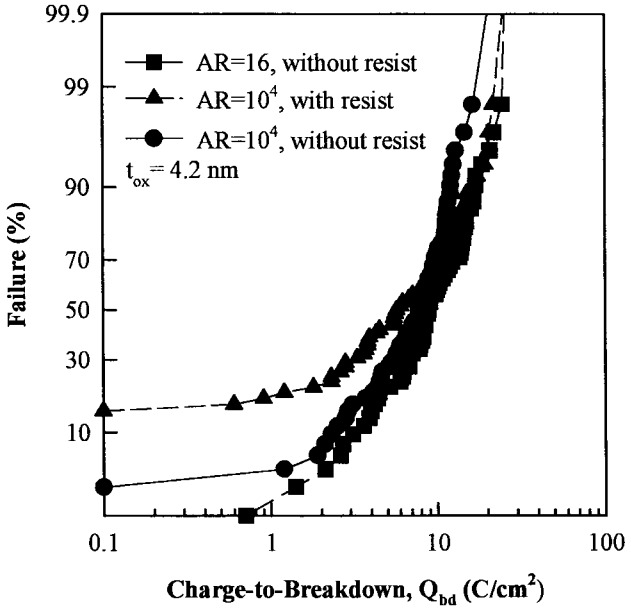


Fig. 2. The cumulative failure of charge-to-breakdown for 4.2-nm thick oxides after plasma ashing with 10^4 area ratio. Triangle symbols are those samples with resist overlayer, circle symbols are uncovered samples and square symbols are those uncovered samples with an antenna ratio of 16.

the sub-6-nm oxides used in this study, a significant "antenna effect" becomes visible and very severe. Specially, samples with 10^4 area ratio and location close to the central region of the wafer endure severe degradation. We have also applied another efficient method proposed by K. P. Cheung [7], which is very sensitive in detecting minor plasma damage in the bulks. The results (data not shown) confirm that indeed no observable degradation occurs for the samples without resist overlayer. These results suggest that photoresist plays an important role in the plasma ashing charging for ultrathin oxides and can not be ignored for future technology employing thin gate oxides.

This phenomenon could not be explained by the "electron shading effect" [9], as the electron shading effect should not be detectable by the area-intensive antenna used in our experiment. Also in order to exclude possible contamination from photoresist, bias-temperature-stress (BTS) measurements were performed for those samples with resist overlayer. No flatband voltage shift is detected from the high frequency C–V measurement (data not shown), suggesting that this damage is not caused by mobile ions in the resist [8]. Actually, the radial distribution of Q_{bd} across the wafer shown in Fig. 1(b) is similar to that in a previous report [10], and we believe that Fang's model [5] is still applicable to this resist-assisted charging mechanism in plasma. Oxide damage is dominated by the electron current from plasma due to the polarity dependence of charge-to-breakdown for thin oxides. This suggests that surface charging [11] into resist in etching can not explain what we observe in ashing process. Because according to this mode, at the wafer center where the plasma potential is usually low, the negatively charge resist will reduce the excess electron current and the resist on the electrodes acts as an insulator preventing samples from charging, which contradicts with out experimental observation. Since the resist ashing rate decreases from the wafer center to the edge in our experiments, the plasma nonuniformity actually exist in our asher. It indicates that plasma is still the source of damage on thin oxide, and the presence of resist induces an alternative charging mechanism, which does not exist in the previous studies [6] where the resist was deliberately stripped prior to ashing.

Fig. 2 compares two cumulative failure rates of charge-to-breakdown between 4.2-nm oxides with or without resist

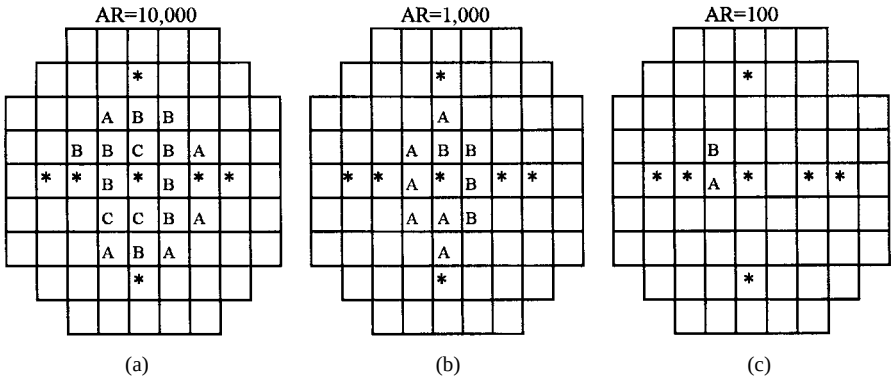


Fig. 3. The wafer maps of plasma-induced damage for samples with antenna ratio (AR) of (a) 10^4, (b) 10^3, and (c) 100, respectively. The oxide thickness is 4.2 nm. Three destructive modes, namely, stress-induced leakage current (SILC), quasi-breakdown, and complete breakdown are represented by symbols **A**, **B**, and **C**, respectively.

covering during ashing. The distributions of three destructive modes, namely, complete breakdown, quasi-breakdown, and stress-induced leakage on the wafer are clearly illustrated in Fig. 3. It should be noted that the quasi-breakdown is defined as in [12] and is caused by the local weak spot, not dependent on the active region area [13]. For the MOSFETs applications, the magnitude of the leakage will reach a few nanoampere at operating voltage and should be classified as a failure. In spite of reduced hot-carrier degradation for devices with thinner gate oxides [14], Figs. 2 and 3 clearly demonstrate the enhanced oxide failure rate, including complete and quasi-breakdown, induced by plasma with the presence of photoresist. This could have significant reliability impacts on future oxide thickness scaling. Our findings also suggest that oxides should not be evaluated by only using samples directly exposed to the plasma.

IV. Summary

A resist-related phenomenon during plasma ashing has been reported in this work. The fully exposed samples, which are often thought to be most susceptible to plasma, do not suffer obvious damage through plasma charging. Instead, those with resist overlayer exhibit severe damage. Although the detailed charging mechanism needs further investigation, presence of photoresist indeed induces change of plasma charging condition and severely degrades ultrathin gate oxide reliability. Our results show that plasma damage could be underestimated by direct plasma exposure. The effect of photoresist must be taken into careful consideration. Otherwise some severe reliability problems could be encountered in the deep-submicron devices employing the gate oxides.

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