A 1.2 V 114 mW Dual-Band Direct-Conversion DVB-H Tuner in 0.13 μm CMOS

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***Abstract*—A fully integrated direct-conversion tuner is implemented in 0.13 μm CMOS technology. A broadband noise-canceling balun LNA with the proposed dual cross-coupling technique helps achieve an overall receiver noise figure from 3.7 to 4.3 dB while consuming only 3.6 mW. The proposed current-mode switching scheme improves the achievable SNIR with a gain step of 15 dB, providing IIP3 improvement of 18 dB and NF degradation of only 6 dB. Moreover, design trade-offs are carefully considered in designing the baseband circuit, which provides wide gain tuning and bandwidth accuracy with a DC offset residual less than 6 mV. The measured maximum SNR values are better than 30 dB over wide input power levels, ensuring robust reception in a mobile environment. All circuit blocks are operated at 1.2 V. As a result, the tuner consumes power as low as 114 mW in the continuous mode. This compact tuner supports both UHF and L-bands, and occupies only 7.2 mm^2 die area.**

***Index Terms*—Balun, CMOS RF, current-mode switching, direct-conversion, DVB-H, DVB-T, mobile TV, noise-canceling LNA, OFDM, passive mixer, receiver, tuner.**

I. Introduction

MOBILE TV systems are in great demand for multi-function mobile entertainment platforms. Among the newly introduced mobile TV standards, DVB-H is currently considered as the globally dominant one. To be successfully integrated into a crowded handheld device, a DVB-H solution must meet the requirements of a small form factor and low power consumption. Several direct-conversion tuners have been reported in an attempt to address these needs in recent years. Implemented in SiGe BiCMOS [1]–[3] or in 0.18 μm CMOS [4], [5] technologies, these tuners consume 200–300 mW in the continuous receiving mode from the supply voltage around 2.7 V. In order to further reduce the power consumption and to provide a high level of integration, a mobile TV system-on-a-chip (SoC) is the optimal solution by integrating a radio tuner, a baseband demodulator, and even a decoder into a single die. Towards this evolution, the first step is to develop a tuner in a finer deep-submicron or even nanometer CMOS technology [6].

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The trend of technology scaling in advanced CMOS technologies benefits digital demodulators in both speed and power dissipation. The associated supply voltage reduction, which could be as low as 1.2 V, however, causes issues to RF tuner design. In practice, a low supply voltage constrains stacking of several devices, and limits applications of many conventional circuit topologies. The reduced voltage headroom further degrades circuit linearity and an achievable signal-to-noise-and-interference ratio (SNIR). Therefore, the tuner architecture and each circuit block must be carefully designed to overcome the limitations of a low supply voltage and to comply with system requirements.

Implemented in 0.13 μm CMOS technology from a single 1.2 V supply, this work focuses on the tuner design to tackle the challenges of a single low supply voltage and trade-offs among noise, linearity, power consumption, silicon area, and external bill-of-materials (BOM). Section II briefly states the system requirements. Section III characterizes the architecture and frequency plan of the RF tuner. Section IV describes the detailed circuit implementation, focusing on: 1) a low power consumption noise-canceling balun LNA; 2) an SNIR enhanced gain switching scheme with a current-mode instead of voltage-mode signal processing; 3) a wide-dynamic-range, highly integrated tunable channel-selection filter with auto-tuned bandwidth; 4) a fractional-N phase-locked loop (PLL) with agile automatic frequency calibration (AFC). Section V reports the experimental results, and Section VI concludes this paper.

II. System Specification

The MBRAI document details DVB-T/H RF specifications such as noise figure, sensitivity, selectivity, and linearity tests [7], [8]. Fig. 1 depicts the block partition of a DVB-T/H system. The defined requirements are referred to the RF reference point. In the updated MBRAI (MBRAI 2.0), it specifies a stringent noise figure (NF) requirement below 4 dB without the GSM-reject filter, which is 1 dB lower than that in MBRAI 1.0. Hence, the sensitivity for 8 MHz channel bandwidth shall be lower than -96.6 dBm for the QPSK 1/2 modulation scheme, having an SNR requirement of 4.6 dB. The use of the 64-QAM modulation scheme further poses difficult challenges on lowering impairments such as LO phase noise and I/Q mismatch. The associated SNR becomes as high as 27.5 dB in mobile reception conditions. The additive noise level from those impairments shall be at least 33 dB below the desired signal according to the MBRAI specification. This leads to the requirement of LO integrated phase noise below -37 dBc and I/Q mismatch below -35 dBc [1], translating into an equivalent SNR of 33 dB if neglecting the

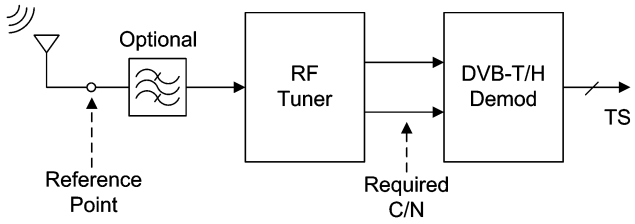

Fig. 1. Block diagram of a DVB-H system.

AWGN contribution. However, the distortion due to I/Q mismatch can be estimated and compensated in the baseband processor [9]. Therefore, the requirement of I/Q mismatch in the RF receiver can be largely mitigated if the digital demodulator supports I/Q correction.

The wide frequency spectrum of DVB-T/H causes the issue that the desired signal usually comes with multiple in-band interferers. Several types of interference tests are specified in the MBRAI document to characterize the interference from strong undesired signals. The interference tests include two categories: 1) receiver selectivity testing with a single analog or digital interferer, and 2) receiver linearity testing with two analog and/or digital TV interferers. From these test specifications, linearity together with NF requirements can thus be derived by analytical calculations and system simulations [1], [3], [6]. For example, the L3 test leads to a minimum requirement of -7 dBm IIP3 and 12 dB NF [3]. In addition, the S2 test with a large TV interferer at the $N+2$ channel requires a baseband IIP2 in excess of $+30$ dBm [6]. Conforming to these stringent tests requires a large dynamic range. Thus, a gain tuning scheme at the very front-end is necessary to protect the following stages from being saturated by far-off blockers, and to optimize the SNIR performance. This is especially important for a tuner having a low supply voltage.

III. Frequency Plan and Tuner Architecture

Frequency downconversion is essential in an RF tuner. A small LO frequency tuning range permits a small chip area and high performance. In previous work, frequency downconversion required an LO source with dividers of divide-by-2 and/or divide-by-4 to cover the UHF and the L bands [1]–[4]. Such a scheme calls for very wide frequency tuning of the LO source up to 62%, from 1.88 to 3.56 GHz or from 0.94 to 1.78 GHz. To reduce the required VCO tuning range, the LO chain was designed using divide-by-2 and divide-by-3 dividers for UHF quadrature LO generation, and using a first-order polyphase filter for the L-band in [5], [6]. The required VCO range is thus reduced to 40%, from 1.2 GHz to 1.8 GHz. This work utilizes a similar frequency plan while multiplying the frequency by two, requiring the VCO range from 2.56 to 3.84 GHz. The quadrature LO signals are generated using divide-by-4 and divide-by-6 dividers in the UHF band, and using a divide-by-2 circuit in the L-band. Such a plan avoids using a polyphase filter and a divide-by-3 circuit, which potentially produces high I/Q mismatch. Furthermore, operating at higher frequencies enables the use of on-chip inductors with smaller area and higher Q-factors.

The tuner adopts the direct-conversion architecture to fulfill small physical size and low power consumption. The block diagram of the tuner is as shown in Fig. 2. Except for the front-end, all circuit blocks are shared for dual-band operation to save chip area. The signal received from the UHF- or L-band antenna is amplified and down-converted to the baseband in two separate signal paths. This facilitates the connection to different external RF filters for each band. Moreover, two sets of I/Q mixers avoid complicated combinations required in both RF signal and LO paths. After down-conversion, both UHF and L-band signal chains are combined in the current mode at the input of the transimpedance amplifier (TIA). Subsequently, the analog baseband circuitry removes the out-of-channel interferers and amplifies the signal to the desired amplitude. Finally, the tuner produces I/Q balanced outputs for further signal processing at the baseband demodulator.

The single-ended-input differential-output low-noise amplifier (LNA), or balun LNA, facilitates the connection to the front antenna and to the following mixer of double balanced topology. It eliminates the need of an off-chip balun in front of the LNA for low noise figure and low external BOM. Also, it needs no on-chip balun after LNA, effective for low distortion as well as low power consumption. In this design, digitally controlled variable-gain function is included in both the front-end and the analog baseband to achieve the optimal SNIR. A wideband detector senses the total received RF power and then delivers an RSSI signal to the baseband demodulator to assist rapid front-end gain adjustment. Gain control can be done via a serial control bus or via an on-chip 7-bit SAR ADC by interfacing an analog signal from the baseband demodulator. To facilitate time slicing operation in the DVB-H system, one independent pin is ready for the baseband demodulator to switch the receiver on and off.

IV. Circuit Implementation

A. RF Front-End

The front-end consists of two sets of LNAs and I/Q mixers for the UHF and L-band, respectively. Fig. 3 shows the simplified schematic for the UHF band. Identical topology is used for L-band implementation except replacing the LNA resistor load with the on-chip inductor load.

Recently the Balun LNA has been demonstrated successfully by using the hybrid common-gate (CG) and common-source (CS) amplifier topology, which exhibits not only broadband single-to-differential conversion but also noise cancellation [10]–[12]. The conventional topology is as shown in Fig. 4(a). The input impedance is dominated by the CG amplifier M1. If $1/g_{m1} = R_s = 50\ \Omega$, broadband impedance matching is achieved. A balanced voltage output is obtained if $g_{m1}R_{L1} = g_{m2}R_{L2}$. As a result, the differential output voltage gain is as $2R_{L1}/R_s$. Note that it requires only $R_{L1} = 250\ \Omega$ to have a voltage gain of 20 dB, indicating the topology is applicable to low supply voltage applications. This load resistance causes no significant dc drop across the load, and also allows a loading capacitance as large as 600 fF to ensure 1 GHz bandwidth. As to noise performance, the noise from M1 appears as the common-mode response and contributes

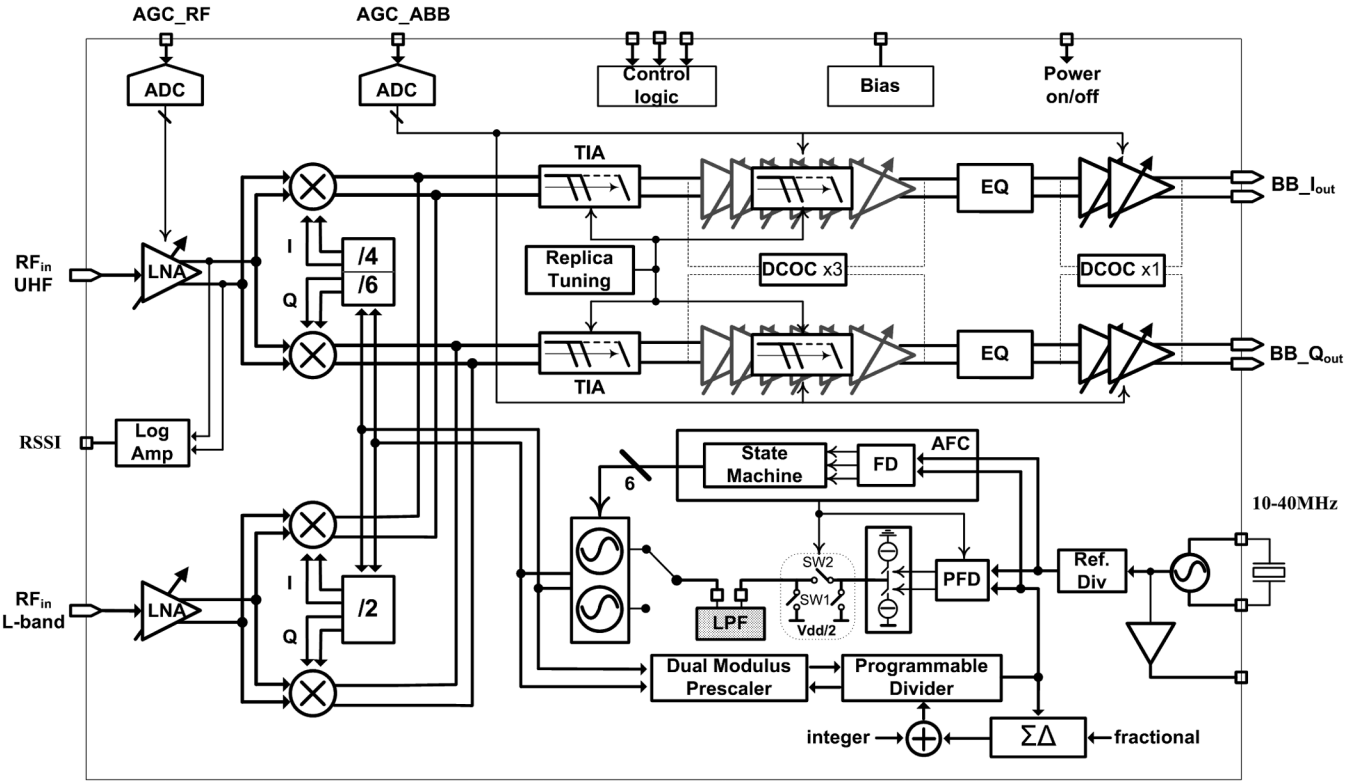

Fig. 2. Block diagram of the designed RF tuner.

almost no output in the balanced condition. As such, only M2 noise contributes significantly to the noise factor in the form of $(2R_{L2}/R_sA_v)(\gamma/\alpha)$, where A_v represents the voltage gain of the LNA and γ/α stands for the excess noise factor. Unfortunately, the LNA noise performance is still poor. For example, the total noise figure of LNA will be larger than 3.8 dB assuming $\gamma/\alpha = 1$, $g_{m1} = g_{m2} = 1/R_s$, and $R_{L1} = R_{L2} = 250\ \Omega$. One method to resolve this issue is by increasing the input transconductance g_{m2} and decreasing the load resistance R_{L2} accordingly, keeping a balanced output. By designing g_{m2} larger than four times of g_{m1}, an NF less than 3 dB is achieved at the expense of 14 mW power consumption in [11], [12].

The proposed LNA design in this work utilizes the technique of dual cross coupling (DCC) as shown in Fig. 4(b) to improve noise performance. DCC allows symmetric device dimensions in the two branches without increasing current dissipation. It includes two types of cross coupling. One type is the bulk cross-coupling (BCC) applied to the input transconductance stage by connecting the body terminals to the source nodes of the devices. The body source cross-coupled configuration successfully incorporates an extra bulk-driven transconductor [13] with the conventional gate-driven one. The input transconductance is thus enhanced by 20% in such dual-gate transistor implementation without consuming extra dc current. The boosted input transconductance increases the voltage gain and reduces the noise contribution from the current buffer and the load resistors. It is worth mentioning that increasing voltage gain without relying on more current dissipation or larger load resistors might mitigate the problem of insufficient voltage headroom in low-voltage design.

The other type of cross coupling is the capacitive cross-coupling (CCC) applied to the cascode stage using a pair of cross-coupled feed-forward capacitors (C_c). As compared to the conventional topology, the proposed CCC technique helps reduce the contribution from M2 channel noise, $i_{\mathrm{n,M2}}$, without increasing g_{m2}. The coupling results in a negative feed-forward path to improve NF performance. The output noise due to $i_{\mathrm{n,M2}}$ is analyzed by the simplified schematic as shown in Fig. 4(c), where the cross-coupling capacitor (C_c) is ignored $(C_c \gg C_{gs3,4})$. The total output noise current is the difference of the two output noise current $i_{\mathrm{no1,M2}}$, and $i_{\mathrm{no2,M2}}$ generated from $i_{\mathrm{n,M2}}$ as $i_{no,M2} = i_{no1,M2} - i_{no2,M2}$. The equivalent circuit for noise analysis is shown in Fig. 4(d), with M1, M2, and M4 each replaced by an effective impedance. The output noise current $i_{\mathrm{no2,M2}}$ is determined by using the impedance ratio based upon the current division principle at node X, while $i_{\mathrm{no1,M2}}$ is generated through M3 acting as a CS amplifier with a degenerative resistance Z_{inl1}. Therefore, the two output noise current $i_{\mathrm{no2,M2}}$ and $i_{\mathrm{no1,M2}}$, can be expressed, respectively, as

$$i_{no2,M2} = \frac{Z_{inl2}}{Z_{inl2} + Z_{inu2}} \cdot i_{n,M2}. \quad (1)$$

$$i_{no1,M2} \approx -\frac{g_{m3}}{1 + g_{m3} \cdot Z_{inl1}} \cdot (Z_{inu2} \| Z_{inl2}) \cdot i_{n,M2}. \quad (2)$$

Thus, the total output noise current is approximately as

$$i_{no,M2} = i_{no1,M2} - i_{no2,M2} \approx -\frac{1 + \frac{Z_{inl2}}{Z_{inl1}}}{1 + \frac{Z_{inu2}}{Z_{inl2}}} \cdot i_{n,M2}. \quad (3)$$

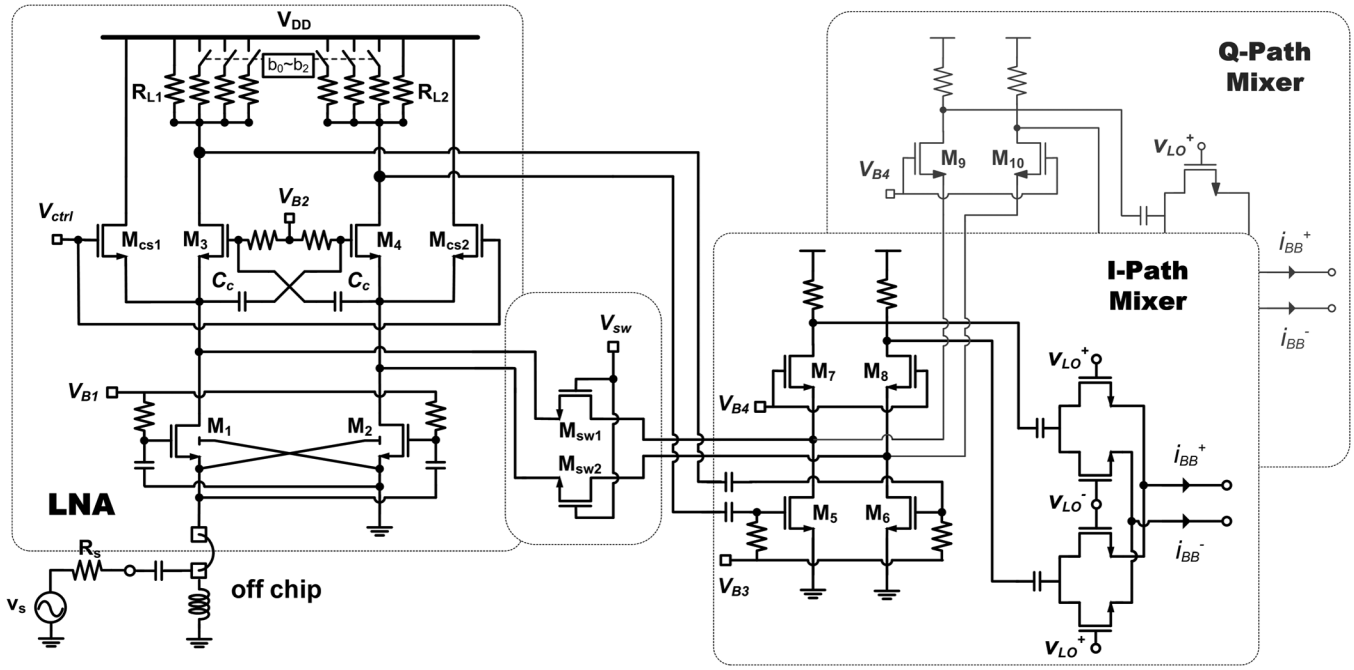

Fig. 3. Simplified schematic of RF front-end for operation at UHF band.

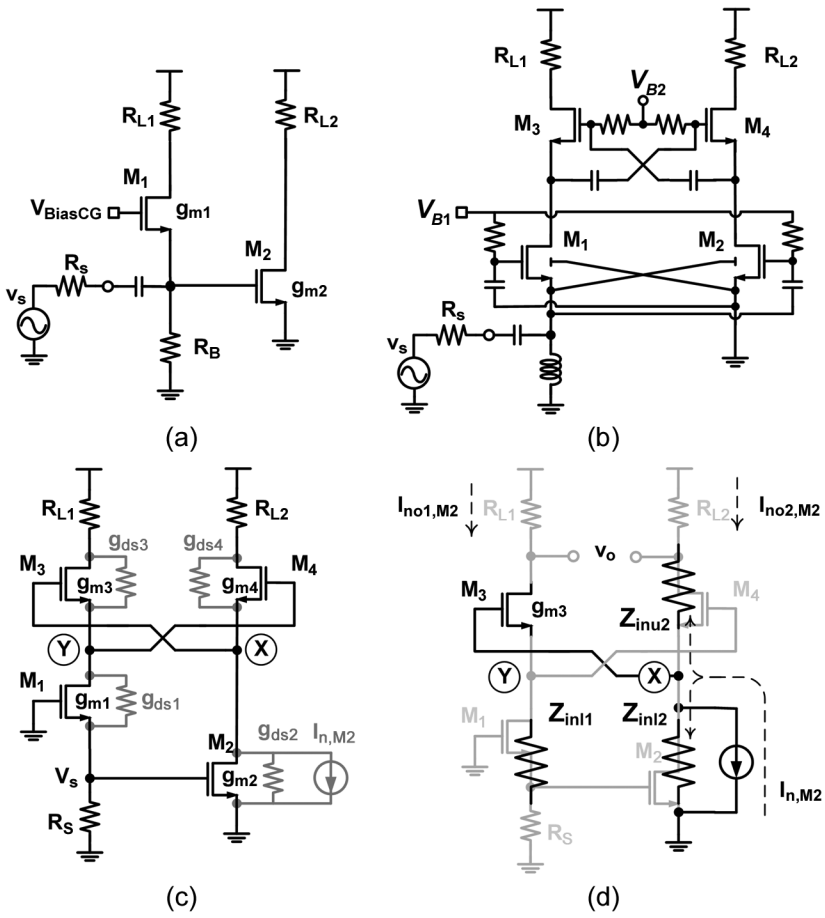

Fig. 4. Balun LNA in (a) the conventional hybrid CG and CS amplifier, and (b) the proposed hybrid CG and CS amplifier with the DCC technique. (c) Simplified schematic of LNA for noise analysis. (d) The equivalent circuit for M2 channel noise analysis.

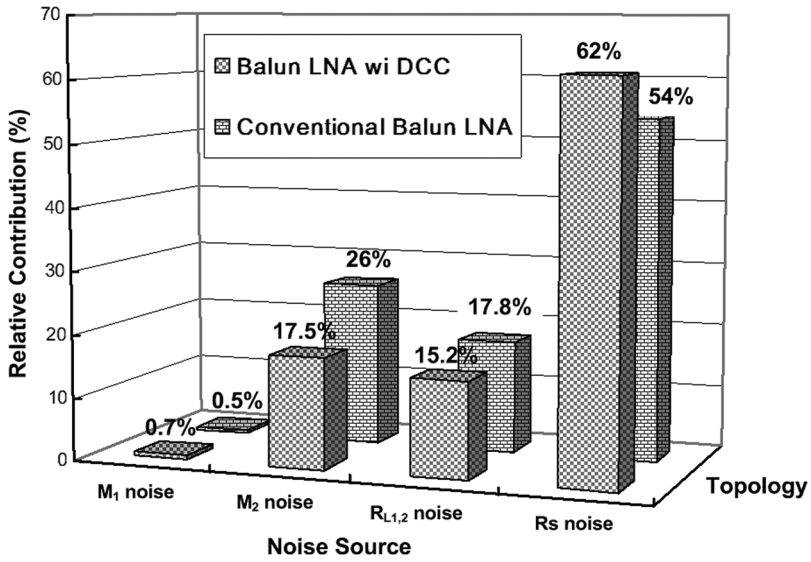

Fig. 5. Simulated noise contribution of dominant devices to the total output noise between the proposed and conventional LNAs.

Performing KCL/KVL at node X and Y, we obtain the three terminal impedances as

$$Z_{inu2} = \frac{1}{g_{m4}} \frac{1 + g_{ds4} R_{L2}}{\left(\frac{A}{1+A} + \frac{g_{ds4}}{g_{m4}}\right)}, \tag{4}$$

$$Z_{inl2} = \frac{1}{g_{ds2}} \frac{1}{1 + \frac{g_{ds1}}{g_{ds2}} \left(\frac{g_{m1} R_s}{1 + g_{m1} R_s}\right)}, \tag{5}$$

$$Z_{inl1} = \frac{1}{g_{ds1}} \cdot [1 + (g_{m1} + g_{ds1}) \cdot R_s] \tag{6}$$

where A is a shorthand notation standing for

$$A \equiv \frac{g_{ds3}}{g_{m3}} + \frac{g_{ds1}}{g_{m3}} \left(\frac{1 + g_{ds3} R_{L1}}{1 + (g_{m1} + g_{ds1}) R_s}\right). \tag{7}$$

The effect of the proposed CCC technique can be observed from these impedances. From (4), Z_{inu2} is boosted about 0.4 times of M_4 intrinsic gain, or $0.4 g_{m4}/g_{ds4}$, due to the negative feed-forward through the path from M_3 to the gate of M_4, if compared to $1/g_{m4}$ in the case of a simple CG transistor as a current buffer. From (5), Z_{inl2} is reduced about one half due to the shunt feedback through the path from M_3, then M_1, to the gate of M_2. From (6), Z_{inl1} is enlarged by a factor larger than two due to the series feedback by the source resistance ($\mathrm{R_s}$). Consequently, in this design, Z_{inu2} is close to Z_{inl2} and Z_{inl1} is about 4 times of Z_{inl2}, leading to the noise current gain $i_{no,M2}/i_{n,M2}$ about 0.64 from (3). As a result, the transistor M2 contributes $0.41(\gamma/\alpha)$ to the noise factor, reduced by a factor of 0.41 as compared to the conventional balun topology without the CCC technique.

Fig. 5 illustrates the simulated noise contribution of M_1, M_2, $R_{L1,2}$, and source resistance of 50 Ω ($\mathrm{R_s}$) to the total output noise. The conventional balun LNA without the DCC technique is also explored for comparison with this proposed balun LNA with DCC technique. As can be seen, the percentage of noise contribution from M2 is much reduced in the proposed balun LNA. Further analysis shows that noise figure improvement of 0.7 dB is achieved as compared to the conventional balun LNA. The proposed balun LNA exhibits a noise figure of 2.1 dB, a nominal gain of 21 dB, and IIP3 of 0 dBm while drawing only 3 mA, 75% of power reduction as compared to the previous work [10], [11].

A cascode amplifier M_{5-8} is cascaded to the proposed balun LNA to obtain maximum front-end gain. Variable gain control is implemented by three methods in combination of these two cascode amplifiers. Fine gain tuning is realized by a bank of digitally controlled resistor load $R_{L1,2}$, providing 12 dB gain range in 2 dB steps. Coarse gain stepping is carried out by the current steering technique of switching $\mathrm{M}_{\mathrm{cs1,2}}$ [14] with a gain step of 5 dB, and by a novel current-mode scheme of switching the signal path. Furthermore, an additional gain switch path not shown is also implemented using the pre-attenuation method [15]. It provides a -5 dB gain attenuation and $+15$ dBm IIP3 to further extend the input dynamic range.

As shown in Fig. 3, a pair of switch transistors $\mathrm{M}_{\mathrm{sw1,2}}$ is inserted between the low impedance terminals of the two cascode amplifiers, providing the signal path of gain attenuation. Fig. 6 illustrates how to achieve high-gain and low-gain by switching the signal path. When the switch transistors are turned off, the front-end is configured as cascaded two-stage amplifiers, providing a transconductance of $g_{m1} R_{L1} g_{m5}$ to the input voltage V_{in}. When the switch transistors are turned on and transistors M_{3-6} are all off, the front-end is configured as one single-stage cascode amplifier, giving a transconductance of g_{m1}. As a result, one-step gain attenuation of $g_{m5} R_{L1}$ is achieved. This current-mode scheme effectively reduces the distortions caused by voltage modulation. It avoids large voltage swings across the switch transistors as compared to the conventional voltage switching method. Besides, it also substantially helps achieve high linearity by avoiding inter-stage intermodulation since the two cascaded amplifiers are reduced to a single-stage amplifier. In addition to linearity, this scheme causes negligible loading effect on the low-impedance terminals due to switch transistor parasitics. It avoids degrading the operating frequency range.

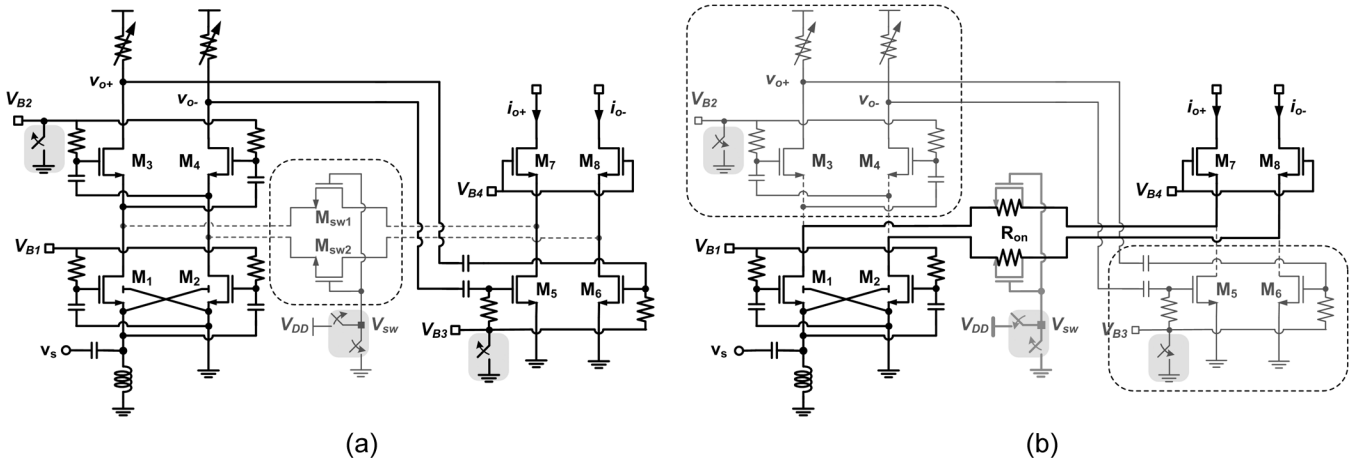

Fig. 6. (a) Front-end configuration at high-gain mode. (b) Front-end configuration at low-gain mode.

Another important advantage is that this scheme affects no input and output interface after gain switching so that the input matching condition can be maintained. Furthermore, this scheme also features much better noise performance if compared with the conventional variable load or current steering methods when the gain attenuation becomes much larger. The measured results show that this switched path offers a stepped attenuation of 15 dB with a high IIP3 level of $+5$ dBm, improved by 18 dB from that at the maximum gain configuration while noise figure degrades only by 6 dB in overall receive chain, 9 dB better than the conventional pre-attenuation method [16]. However, a gain step of 19 dB is measured in the L-band due to the inductor load having higher resonant resistance, and an IIP3 up to $+8$ dBm is achieved.

Instead of using a Gilbert mixer, a current-mode passive mixer is utilized to achieve high linearity with a flexible output DC level. The mixer output must have a DC level compatible to the analog baseband input, since it is directly coupled to the analog baseband in a direct-conversion receiver. With a common-mode level of half supply voltage, the analog baseband built using an active RC structure achieves output swing that is almost rail to rail, alleviating the constraints of a low supply voltage. For 1.2 V operation, such a low common-mode level would pose a difficult challenge for a Gilbert mixer because it requires stacking of multiple devices. Instead, a current-mode passive mixer avoids a large voltage swing across the transistor and has no dc current dissipation. Thus, the control of DC level is much more flexible. As shown in Fig. 3, the quadrature mixer is composed of a transconductance amplifier followed by a mixing quad. It helps minimize quadrature inaccuracy by sharing one common input transconductor between I and Q paths. After down-conversion through the mixing quad, the baseband current is driven into the TIA in an OP-amp RC structure and then converted to voltage. The TIA achieves a maximum allowable output swing of over 2 V peak-to-peak differential at the expense of 7 mA current dissipation. One tracked pole placed in the TIA can pre-filter the adjacent interference which may saturate the first stage of the following filter because its full swing is limited by the low 1.2 V supply voltage.

B. Analog Baseband

The analog baseband functions as channel selection and programmable amplification for both In-phase and Quadrature signal processing. Programmable gain function provides the flexibility to optimize noise, linearity and power consumption. To optimize noise, power consumption and silicon area, it is necessary to make trade-offs in the Op-amp together with the input/feedback resistor pair. In this design, the analog baseband provides total gain control from 0 to 63.5 dB in 0.5 dB steps. It includes several circuit blocks as shown in Fig. 7: a variable-gain low-pass channel filter (VGCF) with cutoff frequency calibration, a first-order all-pass filter, a programmable-gain amplifier, four independent dc-offset cancellation (DCOC) loops with on-chip capacitors, and a unit-gain buffer.

The channel filter is a seventh-order Chebyshev type-I implemented using the leap-frog topology. Embedded into the filter blocks, gain control provides a range from 0 to 48 dB with a tunable cutoff frequency from 2 to 5 MHz depending on the channel bandwidth in use. In the VGCF, the first two Op-amps consume high current for low noise and large signal-handling capability. Also small input/feedback resistor pairs are applied to reach better noise performance at the expense of large capacitor area. The remaining five Op-amps consume less current since the noise contributions are less critical. In addition, the input/feedback resistor pairs have high resistances to reduce the capacitor area. Following the VGCF, the first-order all-pass filter is added to improve the group delay. Then two PGA stages provide an extra gain of 15.5 dB.

On-chip RC auto-calibration activated at power up accurately sets up the channel bandwidth from 2.5 to 4 MHz against PVT variations. The architecture and the timing diagram are depicted in Fig. 8. A duplicate RC integrator compares the RC time constant with a reference clock generated from the crystal output through a programmable divider. The detailed procedure is described as follows.

Two successive states are utilized to complete the auto-calibration process in an iterative process. In the first phase, the clock $CLKB$ is set to high. The integrator is configured as a resistive feedback amplifier with gain attenuation. As a result, both integrator outputs, V_{op} and V_{on}, are reset to the Op-amp's

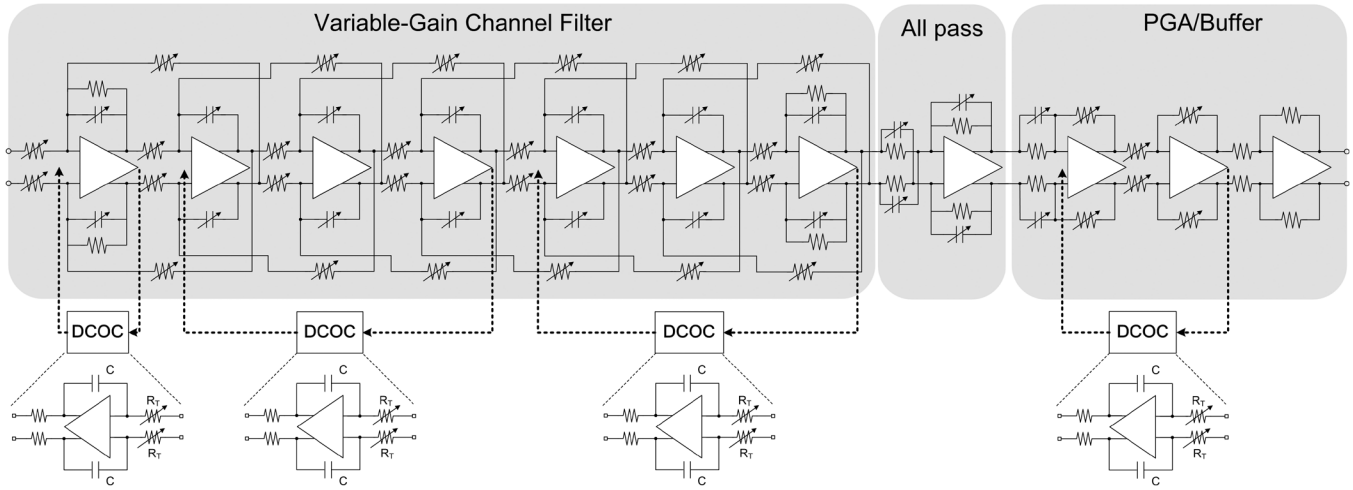

Fig. 7. Architecture of analog baseband.

common-mode voltage. In the second phase, $CLKB$ is low. The integrator is configured as a lossless integrator, which forces its positive output V_{op} to charge toward VDD and its negative output V_{on} to discharge to ground. Once V_{on} voltage becomes smaller than the reference voltage, the comparator will deliver a control signal to stop counting. The 6-bit counter's code is subsequently subtracted from the Bandwidth Code, a default value of RC time constant corresponding to the channel bandwidth. After that, the subtracted output code is sent to update the Capacitor Code used to control the capacitor banks. The calibration will continue until the capacitor code remains constant for several consecutive iterations. As soon as the calibration is finished, another control signal will be sent to power off the calibration circuits and stop the input clock. Finally, a 5-bit control word is provided to adjust the capacitors in the TIA and filter stages within $\pm 3\%$ bandwidth accuracy.

DC-offset cancellation is indispensable in a direct conversion receiver because DC offset may saturate the baseband output and degrade the dynamic range. Featuring a high-pass response in the signal chain, the DCOC has a cutoff frequency less than 1 kHz to ensure sub-carriers around DC are not affected too much. However, if a single loop cancellation is utilized, such a low cutoff frequency will demand for large loop capacitors, inevitably implemented in off-chip components at the expense of four extra package pins [2], [3]. Since the high-pass corner frequency is proportional to the signal processing gain, but inverse to the loop capacitance, multi-loop cancellation can effectively reduce the required loop capacitances. For example, as the signal chain is uniformly divided into M segments in cascade and each segment has an independent servo-loop for DCOC, the processing gain and the used capacitance in each loop can be expressed by $A^{(1/M)}$ and C_{ml}/M, respectively, where A is the total gain of the signal chain and C_{ml} is the total capacitance required in M loops. To maintain the same high-pass corner frequency in the single-loop and multi-loop implementations, the ratio of the total required loop capacitance in single-loop calibration to that in multi-loop can be approximated as

$$\frac{C_{sl}}{C_{ml}} = \frac{A^{\left(1-\frac{1}{M}\right)}}{M} \tag{8}$$

where C_{sl} is the total capacitance required in single-loop cancellation. In this design, four independent servo-loops are utilized to reject DC offset, in total using 16 pF capacitance which is much easier to integrate on chip since 60 times less total capacitance is required compared with a single loop implementation.

The final high-pass cutoff frequency is set constant at 1 kHz for all gain settings by keeping the gain of feedback loop inversely proportional to that of the signal path. Furthermore, the remaining DC offset resulting from the last stage of the servo loop chain is carefully minimized by enhancing transistor symmetry and by using larger dimensions. The measured DC offset is less than 6 mV with an average of 4 mV characterized over 50 samples at the maximum gain setting. The analog baseband totally dissipates 22 mA current, where 8.3 mA is dissipated by the first two stages. The simulated input-referred noise level is about 6 nV/$\sqrt{\text{Hz}}$.

C. Frequency Synthesizer

A fractional-N PLL synthesizer using a third-order delta-sigma modulator with 24-bit accumulators is employed to achieve a high resolution and fast switching time as well as good phase noise. The frequency step of this synthesizer is less than 10 Hz to meet the requirement of multi-standard operation where different channel spacing is specified. In addition, fractional synthesis provides the flexibility to share the same crystal with the existing cellular platform to reduce the BOM cost and PCB area.

The synthesizer generates a wide frequency output from 2.56 to 3.84 GHz by using two VCOs with overlapped tuning characteristics. As shown in Fig. 9, each VCO consists of two PMOS cross-coupled transistors with an internal regulator and one LC tank. The on-chip voltage regulator reduces the impact of power supply noise [17]. Moreover, the tank which is terminated into DC ground enables a wide range of analog control almost from rail to rail, which is crucial for low-voltage VCO design.

As far as phase noise is concerned, the entire tuning range is divided into 64 sub-bands by a 6-bit capacitor bank to decrease the voltage-to-frequency gain. Consequently, adaptive frequency calibration (AFC) is needed to select a specific sub-

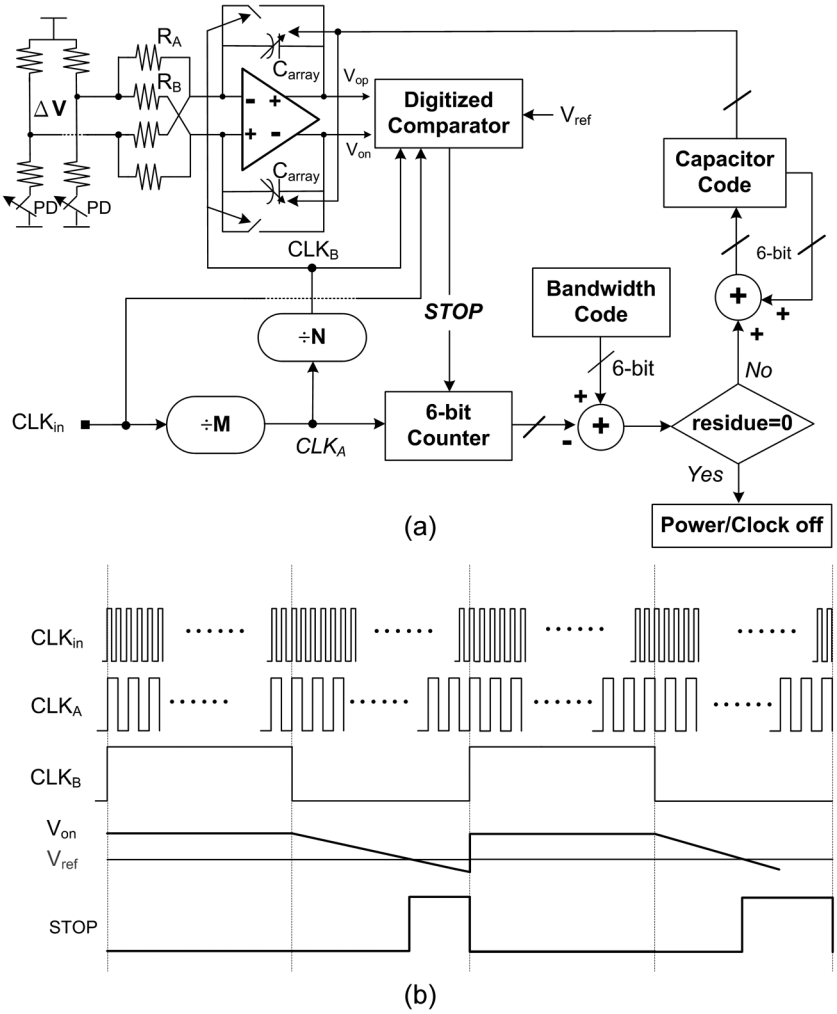

Fig. 8. (a) Architecture of the RC calibration loop. (b) Timing diagram of the RC calibration loop.

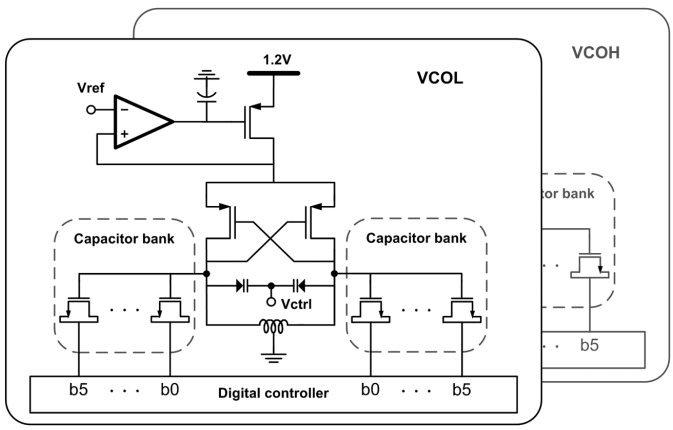

Fig. 9. Schematic of VCOs.

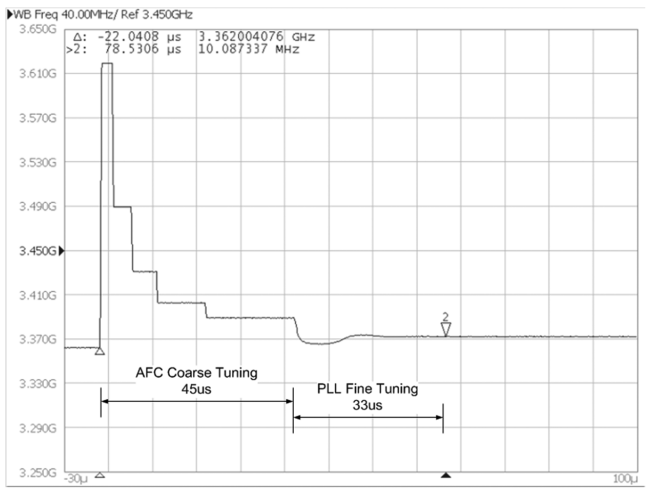

Fig. 10. Measured locking process of frequency synthesizer.

band prior to starting the process of phase locking. The AFC procedure is described as follows. In the beginning, the PLL loop is open and the analog control terminal of the VCO is biased at half supply voltage. Subsequently, AFC is activated, trying to select an appropriate sub-band using the binary search method by comparing the divided VCO frequency with the reference one. Instead of using counters [18], the frequency detector is implemented using a quadri-correlator to shorten the comparison time [19]. After one suitable sub-band has been chosen, the PLL loop is closed achieving phase locked, and AFC is turned off. The measured transient frequency response during the locking process is as shown in Fig. 10, showing a locking

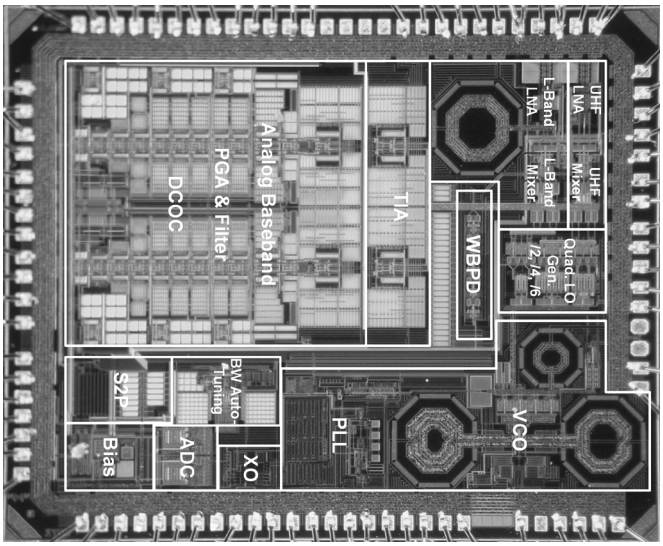

Fig. 11. Die photograph.

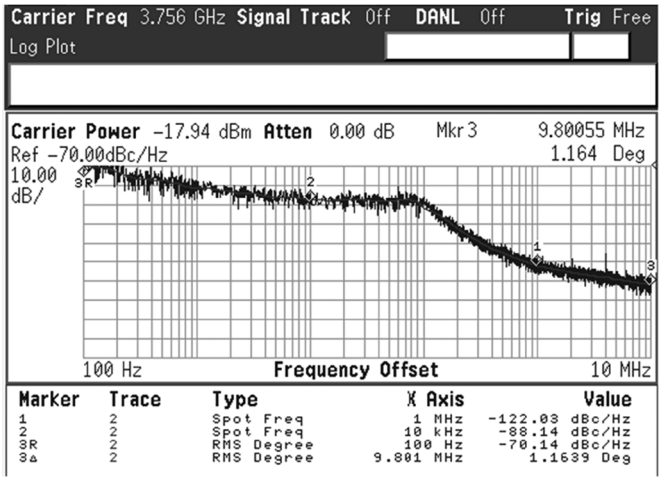

Fig. 12. Phase noise profile measured at synthesizer output.

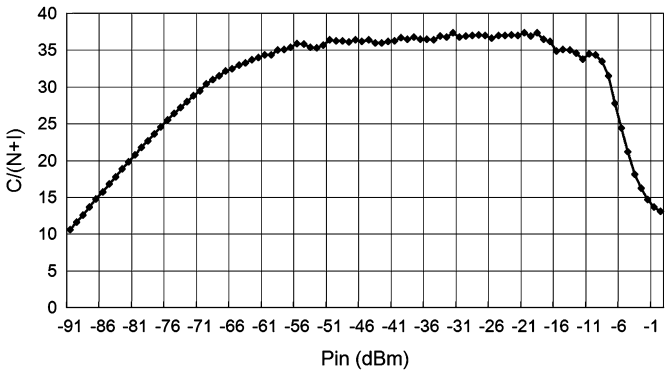

Fig. 13. Measured $\mathrm{C}/(\mathrm{N}+\mathrm{I})$ vs. input power for the test chip comprising digital front-end.

TABLE I
PERFORMANCE SUMMARY OF RF TUNER

Frequency Band (MHz)	UHF-band (470–862MHz)	L-band (1670–1675MHz)
Input Return Loss (dB)	<-12	<-12
Gain Max/Min/Step (dB)	95/-5/0.5	100/10/0.5
RF range/BB range (dB)	40/63.5	30/63.5
NF @ Max Gain (dB)	3.7~4.3	4.3
NF @ (Max RF -15dB) (dB)	9~10.5	13 [a]
IIP2 (N+2) @ Max Gain/ (Max RF -15dB) (dBm)	+35/+50	+27/+46 [a]
IIP3 (N+2,N+4) @ Max Gain/ (Max RF -15dB) (dBm)	-13/+5	-13/+8 [a]
Integrated phase noise (100-4MHz)	0.5° rms	1° rms
Filter rejection with 4MHz BW setting @ 5.25/13.25MHz	32/102 (dB)	
DC offset	6mV	
I/Q matching	<-35dBc	
Power consumption in continuous RX	114mW @ 1.2V	103mW @ 1.2V
Die size	7.2 mm^2 in 0.13 um CMOS	

[a] Measured at (Max RF -19 dB).

time of 78 μs including coarse and fine tuning. The locking time is still less than 100 μs in the worst case of the power-up sequence.

V. MEASUREMENT RESULTS

The tuner chip was fabricated in 0.13 μm 1P8M CMOS process. It occupies a total silicon area of 7.2 mm^2 including all ESD pads. The chip is housed in a 5×5 mm^2 40-pin QFN package. The micrograph of the die is as shown in Fig. 11, where the analog baseband occupies a significant portion of the chip area due to using lower-density MIM capacitors of 1 $fF/\mu m^2$. The measured performance referred to the SMA connector input from a single 1.2 V supply is summarized in Table I.

The measured NF ranges from 3.7 dB to 4.3 dB in the UHF band. The stated IIP3 values are measured, applying two-tone frequencies at 13.25 MHz and 29.25 MHz away from the desired frequency, whereas, for the IIP2, a two-tone test with blockers at 13.25 MHz and 16 MHz offset was performed. At 11 dB back-off from maximum RF gain, which is convergent by the RSSI-AGC loop for L3 blocking test, IIP3 is -4.3 dBm while

TABLE II
SELECTIVITY/LINEARITY AND SENSITIVITY MEASUREMENT RESULTS

Pattern	Modulation	Interferer location	U/D (dB) Spec.	U/D (dB) Measured
S1 (PAL-G)	8k 64-QAM 3/4 (C/N>19.9dB)	N+1	35	42
		N-1	35	43
		N+2	43	46.5
		N-2	43	46.5
S2 (PAL-G)	8k 64-QAM 3/4 (C/N>19.9dB)	N+1	27	35
		N-1	27	35
		N+2	40	45
		N-2	40	45
L1	8k 16-QAM 2/3 (C/N>12.7dB)	N+2, N+4	40/45	42.8/47.8
L2	8k 16-QAM 2/3 (C/N>12.7dB)	N+2, N+4	45	46.7
L3	8k 16-QAM 2/3 (C/N>12.7dB)	N+2, N+4	40	41.8
	Modulation	**C/N (dB)**	**Spec. (dBm)**	**Measured (dBm)**
Sensitivity	8k 64-QAM 3/4	19.9	-81.3	-80.9
	8k 16-QAM 2/3	12.7	-88.5	-88.4
	8k 16-QAM 1/2	10.6	-90.6	-90.7
	8k QPSK 1/2	4.6	-96.6	-96.7

TABLE III
BENCHMARK OF RF TUNERS FOR DVB-H APPLICATIONS

Ref.–Year	Technology	Power (mW)	Vdd (V)	Die size (mm^2)	Operation Band	NF (dB) (UHF)	IIP3 (dBm)	IIP2 (dBm)	Phase Noise
P. Antoine [1] JSSC '05	0.35µm SiGe:C	240	2.775	11.5	UHF	8.5	+12 at (Max RF-20dB)	+45	0.8°
M. Womac [2] ISSCC '06	0.35µm SiGe	340	2.7	12.3	UHF L-Band	3.6	+4 at (Max RF-20dB)	+27	0.3°
K. Iizuka [3] JSSC '07	0.5µm SiGe	184	2.8	16	UHF	3.1 - 4.6	-6.8 at (Max RF-8dB)	N/A	N/A
I. Vassiliou [5] ISSCC '06	0.18µm CMOS	295	2.7	9.7	UHF L-Band	3.5 [a]	-0.5 at (Max RF-10dB)	+34	0.3°
Y. J. Kim [4] ISSCC '06	0.18µm CMOS	185	2.8	7.8	UHF L-Band	4.5	-5 at (Max RF-0dB)	+40	1.0°
I. Vassiliou [6] JSSC '08	65nm CMOS	138	1.2/2.5	7	UHF/VHF L-Band	2.2 - 3.2	-3 at (Max RF-5dB)	+40 [b]	0.5°
This work	0.13µm CMOS	114	1.2	7.2	UHF L-Band	3.7 – 4.3	+5 at (Max RF-15dB)	+50	0.5°

[a] 5 dB Noise Figure is measured at the channel above 800 MHz
[b] Measured at (Max RF −10 dB).

NF is 8.7 dB. The current switch path provides a 15 dB RF gain backoff, achieving a baseband IIP2 of 50 dBm in the UHF band.

The measured phase noise spectrum at the synthesizer output is as shown in Fig. 12. The noise profile will be lowered by 15 dB after 6 divisions for 626 MHz channel, resulting in an integrated noise from 400 Hz to 4 MHz better than 0.3 degrees. The C/N plot at the baseband output, evaluated in terms of EVM, is exhibited in Fig. 13 by applying an input signal of the 16-QAM 1/2 modulation scheme. The SNR shown is better than 30 dB from −70 dBm to −7 dBm, allowing for robust operation in a mobile environment. Because the BER test (system performance) depends on not only the radio chip but also the baseband demodulator, the estimates in sensitivity, selectivity, and linearity tests are given according to the measured MER not exceeding one specific value based on the modulation scheme defined in the MBRAI specification. In Table II, these measurement results are summarized.

Compared with the previously reported work related to DVB-H tuner, shown in Table III, this chip achieves the lowest power consumption from a single 1.2 V supply while maintaining comparable performance. The maximum power consumption is 114 mW in the UHF band as all circuits are activated in the continuous mode. However, the power consumption reduces to 103 mW in the L-band. The reduced power mainly results from the operation with divide-by-2 instead of divide-by-6 as well as no usage of RF power detector.

VI. CONCLUSION

A 1.2 V highly integrated RF tuner for DVB-T/H applications in 0.13 μm CMOS technology is demonstrated. Utilizing a direct-conversion structure and a smart frequency plan, the tuner consumes only 114 mW in the continuous mode and occupies a silicon area of 7.2 mm^2. Together with system and circuit design techniques, this tuner complies with the MBRAI 1.0 requirement, while slightly insufficient to meet the stringent MBRAI 2.0 specifications. However, low BOM as well as small PCB size are achieved, requiring a minimum number of external components: an inductor and a coupling capacitor for each LNA input, a crystal, and RC components for the loop filter. Since the supply voltage is as low as 1.2 V, it is straightforward to convert to advanced technologies of 65 nm and beyond towards a more competitive SoC solution.

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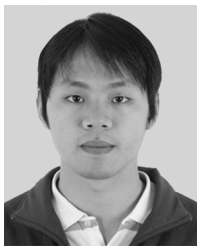

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