

# Due-date performance improvement using TOC's aggregated time buffer method at a wafer fabrication factory

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## Abstract

Due-date performance is one of the most important production indexes for success utilized by wafer fabrication factories. Traditionally, the industry sets a specific due-date tightness level and a dispatching rule based on the total processing time, the production capacity, pre-defined order release criteria and historical data, to ensure deliveries are made on-time. However, such policies typically do not solve the due-date performance problem at wafer fabrication factories, since the processes are highly complex. This investigation explores the due-date performance problem using the concept of the aggregated time buffer in critical chain project management (CCPM), which was developed by Dr. Goldratt. A simulation model was constructed and the performance of the proposed method is evaluated based on four dispatching rules at a wafer fabrication factory. The findings reveal that applying aggregated time buffer control system improved the overall due-date control, in terms of on-time delivery rate, average tardiness, and variances in average tardiness and lateness.

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## 1. Introduction

The due-date control performance, finishing the products without tardiness, is one of the most important production indexes used by wafer fabrication factories. Due-date performance is controlled by determining the high work in process (WIP) level, a long manufacturing lead time, because a high WIP level on the shop-floor increases the manufacturing lead time. Also, unsuitable WIP controlling levels and machine failures lead to a high variation in lead time. Setting an exact order due-date and delivering the goods in a timely manner to the customer improves customer service (Chung, Yang, & Cheng, 1997). However, an accurate due-date cannot be assigned unless the manufacturing lead time can be accurately estimated.

Traditionally, a firm sets a particular due-date tightness level and a dispatching rule according the total processing time of a plan or historical data. However, most evaluations of such manufacturing management policies are too conservative to determine a due-date tardiness level. Many research projects and programs have been developed to overcome these inherent limitations, and to help solve production planning and scheduling problems (Ahmadi, Ahmadi, Dasu, & Tang, 1992; Fowler, Phillips, & Hogg, 1992), integrated shop-floor scheduling systems based on a variety of methods (Fargher, Kilgore, Kline, & Smith, 1994; Ovacik & Uzsoy, 1994), and using combinations of dispatching rules and order release policies (Chang, Pai, Yuan, Wang, & Li, 2003; Lu & Kumar, 1994; Wein, 1988). However, few such projects and programs have demonstrated the effective and efficient solving of the due-date control problems in wafer fabrication factories. Several problems are included as follows. First, most due-date control rules use the decentralized time buffer method to spread to each manufacturing process to control the flow-time and

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**List of notations**

$i$	$i$ th lot	$LT'_i$	lead time of lot $i$ , according to JIQ method
$j$	$j$ th workstation	$n_i$	the throughput of the bottleneck workstation per day
$k$	$k$ th monitor workstation	$p_i$	the processing time of $i$ th lot
$e$	the last work station to proceed lot $i$	$P_{ij}$	processing time for the lot $i$ in workstation $j$
$a_i$	the releasing date of lot $i$	$Q_i$	the number of jobs in the work center queues on the job's routing when lot $i$ arrives
$AB_i$	aggregated time buffer when lot $i$ enter the system	$SB_{ik}$	remaining of the aggregated time buffer when lot $i$ arrives at monitor workstation $k$
$AB_{ik}$	aggregated time buffer for the lot $i$ in the $k$ th monitor workstation	$t_{ik}$	time at which lot $i$ arrives at monitor workstation $k$
$d_i$	the due-date of the lot $i$	$W_i$	the waiting time to be processed of the lot $i$ ,
$d'_i$	time at which probability that the $i$ th lot has been completed is 50%	$\eta$	an unbiased evaluated constant obtained from historical data in the factory
$et_{ik}$	expected time of completion of lot $i$ on monitor workstation $k$	$\theta$	the safety allowance
$\hat{F}_i$	an unbiased estimate of the flow-time of lot $i$	$\hat{\sigma}_e$	the standard deviation of the estimated error
$K_1, K_2$	the parameters of the state of the system based on the historical data		

the due-date. Second, only a few have examined those rules, with reference to shop status information. Third, the shop status in a job shop arrangement is extremely dynamic and the due-date tightness in the regulations is very difficult to set. Finally, the most important and difficult to control due-date in a wafer fabrication system is associated with a complex production process that includes: (1) many process steps; (2) machines with very different processing capacities; (3) unpredictable machine downtime and process yields, which combine to make the task of managing material flow through the facilities particularly challenging; (4) re-entrance of the product flows, as numerous products must be returned to the stations several times before completion; and (5) the visiting of bottlenecks several times before final completion. Consequently, the throughput of the system is highly unstable, the lead time is long, and the WIP level is excessive (Chung et al., 1997). Therefore, in solving due-date performance problems, it is important to simultaneously calculate the due-date tightness level and determine the appropriate dispatching rules.

Recently, a number of researchers have implemented shop-floor control procedures to efficiently control the due-date based on the Theory of Constraints (TOC), which was developed by Goldratt (1990). The TOC states, "Any system must have a constraint that limits its output." Hence, the system's constraint is likely to be the weakest link in a chain. Regardless of how other links in the chain are improved, the chain itself does not become stronger unless the strength of the weakest link is improved (Leach, 2000). Therefore, Goldratt (1997) proposed that when project managers estimate due-date control, three uncertainties in project planning and scheduling must be considered. These are task time, path time and resource uncertainties. Most project planners add a safety allowance or time buffer in the total estimated time required to reduce the uncertain-

ties of a task (Goldratt, 1997). The question is how much safety allowance or time buffer should be added in the activity time? Fortunately, in CCPM, the above problems can be solved by applying aggregated time buffer (ATB) theory, which brings together all time buffers in a single time buffer (Steyn, 2000; Yeo & Ning, 2002).

In this study, the due-date performance problem of wafer fabrication factories is converted into a project problem by the TOC aggregated time buffer method, because the concept of a project is similar to the concept of a customer order. A project involves several activities/tasks and an order includes several processes. Therefore, the due-date control component of a customer order problem is converted into a project dilemma. The objective of this research is to develop and discover a combinational dispatch rule of job shop flow scheduling to improve the due-date performance by using the TOC's time buffer approach. In addition, the safety allowance is aggregated and calculated using an aggregated time buffer based on the due-date estimation according to the concept of TOC. By constructing and monitoring the aggregated time buffer with different dispatching rules, it is expected that the aggregated time buffer control model could reduce the mean tardiness and tardiness jobs. A simulation model is also constructed and the performance of the presented aggregated time buffer method is examined based on several dispatching rules for a wafer fabrication factory.

The rest of the article is organized as follows. Section 2 reviews the literature on the TOC and due-date assignment problems. Section 3 describes the aggregated time buffer control model and explains how to determine flow time controlling parameters? Section 4 simulates and applies the aggregated time buffer control model using actual data. Finally, conclusions are drawn and avenues for further research are provided.

2. Literature review

Since the duration of each project activity is unpredictable, Goldratt (1997) developed a CCPM method to solve problems that are inherent in the traditional project planning and scheduling methods. The critical chain method, applied in the TOC, offers an improved process to manage the risk and uncertainty associated with a project and enhances the project time management (Yeo & Ning, 2002). This method solves the problem of project planning and scheduling and also overcomes the risk and uncertainty associated with the on-time completion of the projects.

2.1. Project activity performance

Most studies in this field use a beta ( $\beta$ ) distribution to describe and estimate project activity time (Fig. 1), because the  $\beta$  distribution effectively describes the inherent variability in time estimates (Stevenson, 1999), and has a left skewed probability distribution and a long tail to the right,

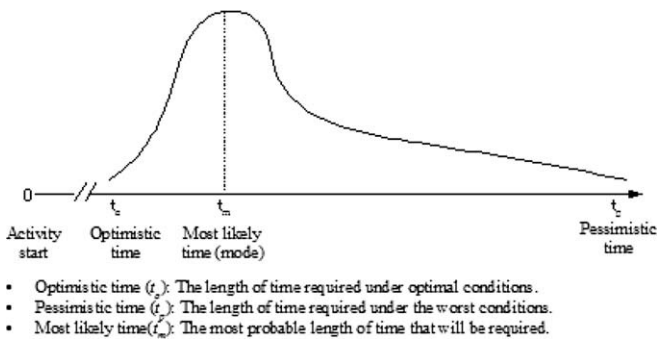


Fig. 1.  $\beta$  distribution for probabilistic time estimates.

above the average activity time. Time wastage is associated with student syndrome, Parkinson’s law, multi-tasking, and merging events (Yeo & Ning, 2002).

2.2. Buffer control

A project planner must add a time buffer to enable project activities to be controlled effectively. Tu and Li (1998) defined the time buffer as “the processing time plus the setup time plus an estimated aggregated protective time required ensuring that the released product will arrive at the constrained machine when needed”. In CCPM, two buffers are defined – feeding and project buffers. Feeding buffers (FBs) are incorporated whenever a non-critical chain activity joins the critical chain, both to protect the critical chain from disruptions in the activities that feed it, and to allow critical chain activities to start early to ensure that the project proceeds effectively. The project buffer (PB) protects the project due-date promised to the customer from variations in the critical chain tasks. Dr. Goldratt further suggested that a buffer associated with the critical chain tasks should be shifted to the end of the critical chain in the form of a project buffer, as shown in Fig. 2.

For a 90% level of confidence estimation, all original time buffer estimates should be by halved by 50% to yield the average time estimates ( $t_m$ ) in the TOC. The time buffer is aggregated to against uncertainties in estimates and the activity performance and due-date. Fig. 3 displays the aggregated time buffer,  $B$ , which equals the sum of  $b_i$ , where  $i = 1, 2, \dots, n$

$$B = \sum_{i=1}^n b_i, \quad b_i \text{ is the buffer between processes}$$

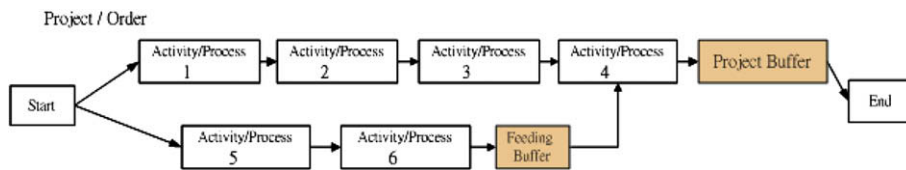


Fig. 2. Buffers in CCPM.

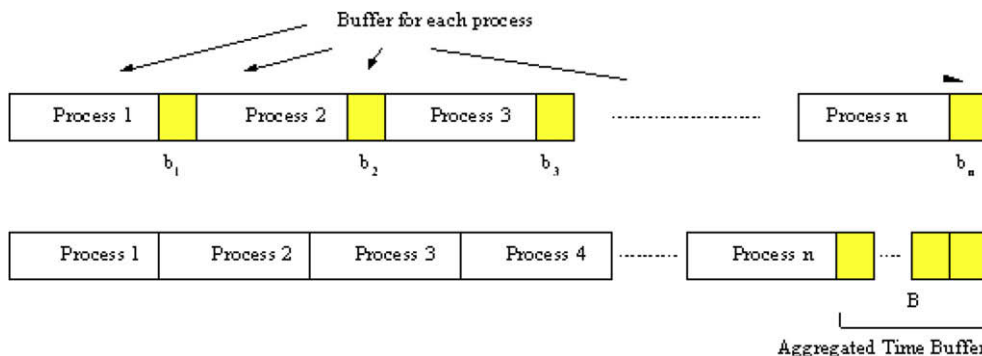


Fig. 3. Aggregated time buffer.

As described above, the calculated buffer increases linearly with the length of the critical chain with which it is associated. Fig. 4 displays the size of the buffer as follows:

- *A*: Aggressive but possible time estimate (ABP), within which probability of completing the project is 50% if it is pushed aggressively.
- *C*: High-probability time estimate (HP), within which probability of completing the project is 90% if the project is performed conservatively.
- *B*: It equals to *C* minus *A*. Generally, it is defined as the buffer size.

The time buffer size of each activity is assigned by the manager, according to his or her experience and business policies. Figs. 5a and b display the different ways in which managers establish project buffers to ensure on-time delivery. Dr. Goldratt stated that, regardless of the project, the ratio  $B/C$ , where  $B = C - A$ , should be approximately 50%.

2.3. Issues associated with setting due-dates

Due-dates could be external or internal (Chen & Gupta, 1989). The external due-dates are set by the sales department, usually neglecting job shop conditions. They tend to be later than actual delivery dates. Internal due-dates consider shop conditions, and are set by a scheduler. They are closer to the actual delivery dates. Approaches for setting due-dates fall into four categories.

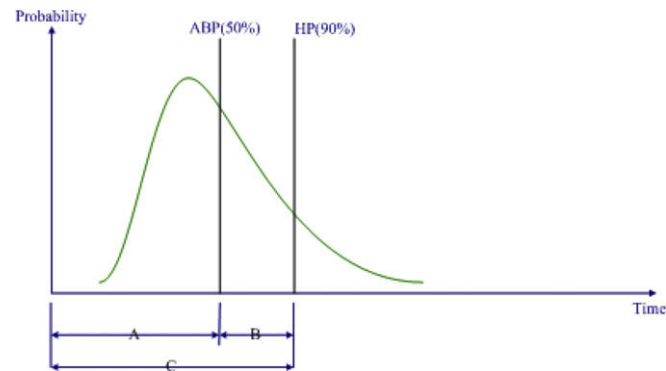


Fig. 4. Uncertainty in activity time.

1. Direct procedures. This approach sets a due-date based on data such as job characteristics, shop conditions and dynamic shop conditions. Although, this approach is convenient and easily implemented, some parameters must be pre-specified (Smith & Seidman, 1983).
2. Simulation method. The advantage of this approach is that the effects of the policies can be easily evaluated without actual execution. Numerous researchers have used simulation (Vig & Dooley, 1991; Weeks, 1979). Kaplan and Urral (1993) determined flow-time data from the results of a simulation. They evaluated the relationships among several variables and flow-time by performing a correlation analysis.
3. Analytical method. This approach is based on queuing theory, and estimates the mean and standard deviation flow-times of orders.
4. Statistical analysis. This approach uses regression or relational analysis to determine the relationships between the flow-times of orders and other variables (Kaplan & Urral, 1993; Smith, Minor, & Wen, 1995).

3. Aggregated time buffer control model

The aggregated time buffer control model concerns the macro and dynamic factors to meet the due-date. The aggregated time buffer control model is described below. It involves: (1) calculating the total aggregated time buffer; (2) selecting the monitoring point; and (3) constructing the model.

3.1. Calculating the total aggregated time buffer

For any lot *i*, the total aggregated time buffer is defined as in Eq. (1). Fig. 6 displays the aggregated time buffer

$$AB_i = d_i - d'_i \tag{1}$$

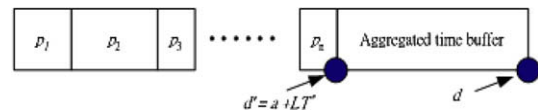


Fig. 6. Aggregated time buffer calculation.

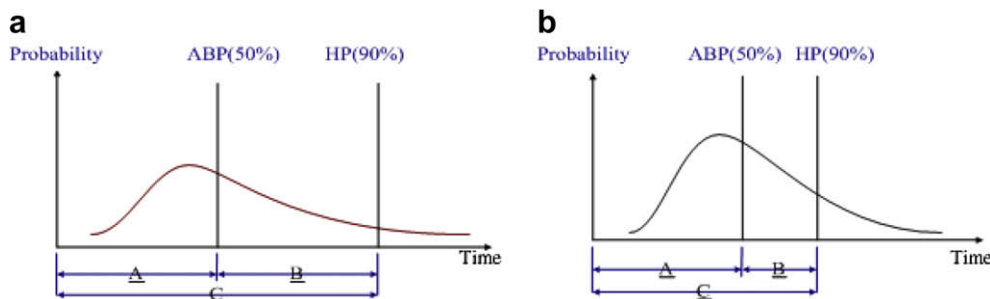


Fig. 5. (a,b) The difference lengths for *A*, *B*, and *C*.

where  $d_i$ : due-date of the lot  $i$ ;  $d'_i$ : it is a 50% opportunity to finish the lot  $i$ .

The due-date is set herein, using both simulation and queuing theory to estimate the flow-time and identify its control parameters (Enns, 1993; Kaplan & Ural, 1993). The analytical method is used to estimate time,  $d_i = a_i + \hat{F}_i + \theta\hat{\sigma}_e$ , where  $a_i$  is the releasing date of lot  $i$ ;  $\hat{F}_i$  is an unbiased estimate of the flow-time of lot  $i$ ;  $\theta$  is the safety allowance, and  $\hat{\sigma}_e$  is the standard deviation of the estimated error. The allowance includes the processing time, the waiting time, and other uncertainties associated with tardiness. The setting of the due-date is further simplified as  $d_i = a_i + p_i \times \eta$ , where  $p_i$  is an unbiased estimate of the processing time for lot  $i$ , and  $\eta$  is an unbiased evaluated constant obtained from historical data in the factory. Generally, the ratio of real production cycle time to theoretical production cycle time is between 2.5 and 10 (Lu & Kumar, 1994). The real number is dependent on the actual situation of production loading. In this research, the  $\eta$  is determined by pre-simulation according to the achievement of the due-date.

The next step is to determine the time point ( $d'_i$ ) at which the lot  $i$  has a 50% of being completed. It is calculated as  $d'_i = a_i + LT'_i$ . The estimate of  $LT'_i$  is based on the jobs in queue due-date rule (JIQ), where JIQ assign flow-times allowance on the basis of the total number of jobs in the system waiting to be processed on machines encountered on the job's path (Tsai, Chang, & Li, 1997). The reason for using the JIQ method is that it can reflect the manufacturing processes of a wafer fabrication factory. In the JIQ method, each job receives a random due-date, usually following a probability distribution (Gordon, Proth, & Chu, 2002). By using this method, it can consider the different total processing times for various product types and the WIP levels for the lead time effects. As generally known, the release function controls the level of WIP inventory, and the level of WIP determines the flow-time of the orders. Also, the parameters used in this method can consider the production queue. For details of the JIQ method, refer to Chang's (1996), Ramasesh (1990), Vig and Dooley (1991), Gee and Smith (1993) papers

$$LT'_i = K_1P_i + K_2Q_i \tag{2}$$

where  $P_i$ : the total processing of the lot  $i$ ;  $Q_i$ : the number of jobs in the work center queues on the job's routing when lot  $i$  arrives;  $K_1, K_2$ : the parameters of the state of the system based on the historical data.

JIQ considers the shop congestion status. Their flow-time allowance estimate is static. This method accounts for the effects of lead times on the products total processing times and the total amount of WIP. Also, the selection of  $K_1$  and  $K_2$  is based on the actual situation on the loading in a production line.

### 3.2. Selecting the monitoring point

Aggregated time buffer control can be regarded as inventory control. For some orders, the time buffer is used up

quickly, while for others, it is not. Therefore, the buffer size must be determined and the rules set to protect and monitor the use of a time buffer. As lot  $i$  continues to be processed, the uncertainty that lot  $i$  will be finished increases, because the aggregated time buffer decreases. Fig. 7 displays the dynamic aggregated time buffer as the job shop process continues.

Based on the above, the best method is to set each control point in each workstation to control the use of the time buffer. However, this method overloads the entire control system. Therefore, in this work, the control point will be a bottleneck workstation that generally has a large WIP. This idea is based on the TOC: a workstation with a high utilization will have a long queue, and therefore, constitutes a high-probability of using the time buffer.

### 3.3. Constructing the model

Three aggregated time buffers are considered, according to the TOC. Goldratt (1997) recommended a simple “green–yellow–red” warning system. If overruns on activities that lead to a buffer cause less than one third of the buffer to be used, then no action is taken; if between 1/3 and 2/3 of the buffer is used, a warning is issued; if more than 2/3 of the buffer is used, a serious corrective action must be taken. This concept is also adopted to apply to buffer control in this study. To control the buffer effectively, first, if it is within the first third of the aggregated time buffer, then no action is taken. Second, if it enters the middle third of the aggregated time buffer, then the problem is addressed and a plan of action implemented. Third, if it penetrates the final third of the buffer, then the buffer manager must increase the priority of the order to ensure that it is completed on time. The buffer manager must set emergency policies for the order. Also, the status of aggregated time buffer must be updated as required. The algorithms for determining the total aggregated time buffer are summarized as follows (Fig. 8):

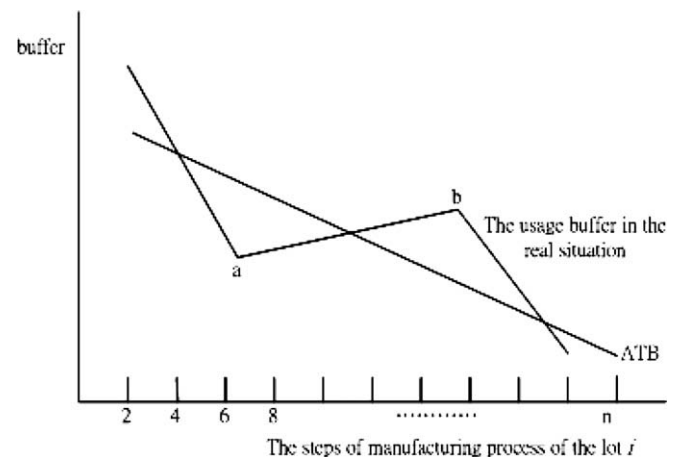


Fig. 7. Dynamic ATB as the process is continued.



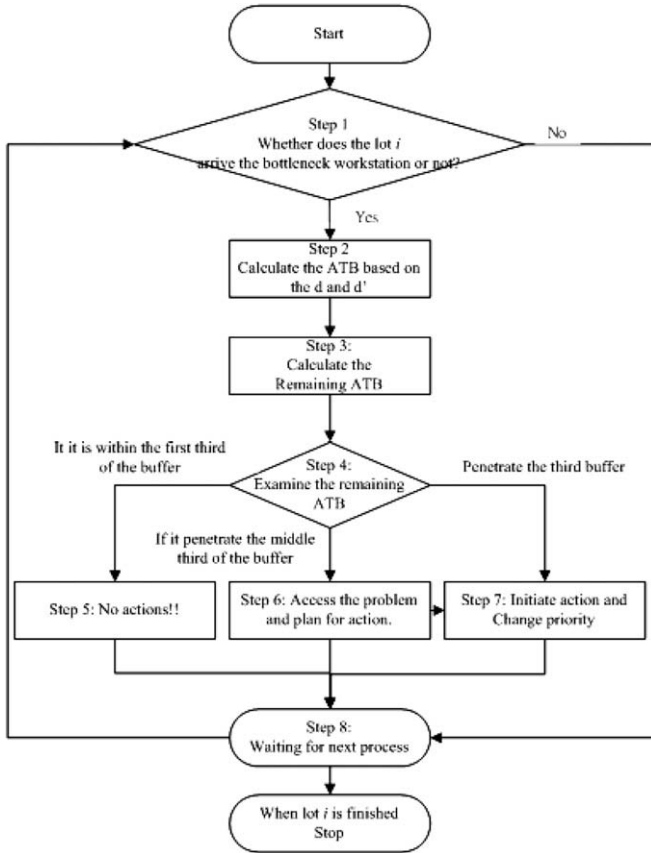


Fig. 8. Aggregated time buffer control model.

Step 1. When lot  $i$  arrives at the bottleneck workstations, the monitoring process begins. IF the arrival date of lot  $i$  is before the due-date, then go to step 2; otherwise, go to step 8.

Step 2. Determine the total aggregated time buffer from the activity time. As the order is processed, the time buffer linearly declines, as shown in Fig. 7. Therefore, the aggregated time buffer for lot  $i$  at the  $k$ th monitor workstation is as follows:

$$AB_{ik} = AB_i \times \frac{\sum_{j=k}^{j=e} P_{ij}}{\sum_{j=1}^{j=e} P_{ij}} \quad (3)$$

where  $i$ :  $i$ th lot;  $j$ :  $j$ th workstation;  $k$ : the  $k$ th monitor workstation;  $e$ : the last work station to proceed lot  $i$ ;  $P_{ij}$ : processing time for the lot  $i$  in workstation  $j$ ;  $AB_i$ : aggregated time buffer when lot  $i$  enter the system;  $AB_{ik}$ : aggregated time buffer for the lot  $i$  in the  $k$ th monitor workstation.

Step 3. Calculate the remaining of the aggregated time buffer

The aggregated time buffer is affected by the lead time, which is determined by the order and manufacturing processes. Determining the lead time while considering all the job status information simultaneously is important.

(1) Calculate the time at which the probability that the  $i$ th lot has been completed is 50%

$$d'_i = a_i + LT'_i \quad (4)$$

where  $d'_i$ : time at which probability that the  $i$ th lot has been completed is 50%;  $a_i$ : the releasing date of the lot  $i$ ;  $LT'_i$ : lead time of lot  $i$ , according to JIQ method.

(2) Determine the expected time for completing the order according to the due-date  $d'_i$

$$et_{ik} = a_i + (d'_i - a_i) \times \frac{\sum_{j=k}^{j=e} P_{ij}}{\sum_{j=1}^{j=e} P_{ij}} \quad (5)$$

where  $et_{ik}$ : expected time of completion of lot  $i$  on monitor workstation  $k$ .

(3) Determine the remaining of the aggregated time buffer

$$SB_{ik} = AB_{ik} - (t_{ik} - et_{ik}) \quad (6)$$

where  $t_{ik}$ : time at which lot  $i$  arrives at monitor workstation  $k$ ;  $SB_{ik}$ : remaining of the aggregated time buffer when lot  $i$  arrives at monitor workstation  $k$ .

Step 4. Examine the feedback on the consumption of the aggregated time buffer. The buffer control rules are as follows:

- (1) If the first third of the aggregated time buffer ( $AB_{ik} - SB_{ik} \leq \frac{1}{3}AB_{ik}$ ) is penetrated, go to step 5; take no action.
- (2) If the middle third of the buffer ( $\frac{1}{3}AB_{ik} \leq AB_{ik} - SB_{ik} \leq \frac{2}{3}AB_{ik}$ ) is penetrated, go to step 6; address the problem and plan for action.
- (3) If the final third of the buffer ( $AB_{ik} - SB_{ik} \geq \frac{2}{3}AB_{ik}$ ) is penetrated, go to step 7; initiate action.

Step 5. Lot  $i$  can be finished before the due-date; set the manufacturing priority to “normal lot”, then go to step 8.

Step 6. Henceforth, the lot must be closely monitored because it could be late. If  $AB_{ik} - SB_{ik} \geq \frac{2}{3}AB_{ik}$ , then go to step 7, otherwise, go to step 8.

Step 7: The usage of the time buffer shows that the order will not be completed on time. Therefore, the priority is set to “hot lot”, which is the highest priority.

Step 8: Wait for the subsequent process.

### 3.4. Illustration

The above procedure is illustrated using the following example. Lot 1 is assumed to arrive on Day 0. It is processed at three workstations,  $w_1$ ,  $w_2$  and  $w_3$ , at which the processing times are 2 ( $p_{11}$ ), 6 ( $p_{12}$ ) and 1 ( $p_{13}$ ) day, respectively. Also, the  $w_2$  is the bottleneck workstation of the three machines based on utilization. Estimated lead times

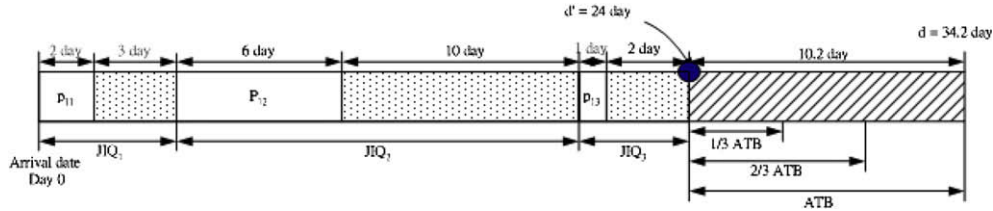


Fig. 9. Calculation of ATB.

for the workstations, based on the queue, are three, ten and two days. Parameters  $K_1$  and  $K_2$  are fixed and dependent on the actual loading of a production line. In this example, they are assumed both to be one.

Therefore,

$$d' = a + (LT'_1 + LT'_2 + LT'_3)$$

$$= 0 + [(2 + 3) + (6 + 10) + (1 + 2)] = 24 \text{ day}$$

Based on historical data from the factory on the completion of lot 1,  $h = 3.8$  is assumed. Therefore,  $d = \sum_{i=1}^3 p_{1i} = (2 + 6 + 1) \times 3.8 = 34.2$ . The aggregated time buffer can be determined to be  $AB_1 = d - d' = 34.2 - 24 = 10.2$ . The manager can monitor the aggregated time buffer at the  $w_2$  and she/he can make a decision in real time, as presented in Fig. 9.

#### 4. Simulation experiment

In this study, the dispatching rules and the aggregated time buffer rules were developed and applied to simulate a process in a wafer fabrication factory using the simulation software, Simple++. During the simulation, four dispatching rules were grouped and evaluated by adding an aggregated time buffer based on the due-date control, as presented in Fig. 10. The first group comprises first-in-first-out (FIFO) and smallest remaining processing time (SRPT) rules, which are not related to the due-date in the consideration of the priorities of the process sequences. In contrast, the other two dispatching rules, early due-date

(EDD) and slack per operation (SLACK/OPN) are related to the due-date. For all of those dispatching rules, two experiments – I (without aggregated time buffer control) and II (with aggregated time buffer control) – are simulated and assessed. All data were collected after the simulation had reached a steady state.

#### 4.1. Simulation input data and assumptions

Four different equal product-mixed products in a wafer fab factory (A, B, C, and D) are selected and simulated. The manufacture of each product involves at most 270 manufacturing processes on 24 workstations. In these workstations, two types of machines are used – one for batch processing ( $w_i$ , where  $i = 1-4$ ) and the other for serial processing ( $w_i$ , where  $i = 5, 6, \dots, 24$ ). The machine down time, MTBF (mean time between failure) and MTTR (mean time to repair) are simulated as being exponentially distributed. Table 1 summarizes all data.

Table 1  
Related data for each workstation

Work station	No. of machine	MTBF (h)	MTTR (h)	MTBPM (h)	MTPM (h)	Process type
w <sub>1</sub>	4	42.18	2.22	716	4	B
w <sub>2</sub>	4	101.11	10.00	600	1	B
w <sub>3</sub>	4	113.25	5.21	180	7	B
w <sub>4</sub>	2	103.74	12.56	150	6	B
w <sub>5</sub>	2	100.55	6.99	336	12	S
w <sub>6</sub>	2	113.25	5.21	96	8	S
w <sub>7</sub>	2	16.13	4.38	166	2	S
w <sub>8</sub>	2	13.22	3.43	716	4	S
w <sub>9</sub>	2	10.59	3.74	150	6	S
w <sub>10</sub>	2	47.53	12.71	163	5	S
w <sub>11</sub>	2	52.67	19.78	600	6	S
w <sub>12</sub>	2	72.57	9.43	166	2	S
w <sub>13</sub>	8	22.37	1.15	480	24	S
w <sub>14</sub>	6	21.76	4.81	60	3	S
w <sub>15</sub>	2	387.20	12.80	480	24	S
w <sub>16</sub>	4	–	–	–	–	S
w <sub>17</sub>	2	119.20	1.57	130	2	S
w <sub>18</sub>	2	–	–	–	–	S
w <sub>19</sub>	4	46.38	17.42	120	6	S
w <sub>20</sub>	2	36.58	9.49	168	8	S
w <sub>21</sub>	4	36.58	9.49	163	5	S
w <sub>22</sub>	4	118.92	1.08	162	4	S
w <sub>23</sub>	4	–	–	–	–	S
w <sub>24</sub>	4	55.18	12.86	96	8	S

Remarks: B, batch process, each time can process 6 lots; S, single process, each time can only process 1 lot.

		Dispatching Rules	
		Not related to due date	Related to due date
Buffer Control	Without Aggregated Time Buffer Control	FIFO SRPT	EDD SLACK/OPN
	With Aggregated Time Buffer Control	FIFO SRPT	EDD SLACK/OPN

Fig. 10. Experiments on buffer control with dispatching rules.

The other input data used in this simulated model are as follows:

1. The machine setup time is included in the machine processing time.
2. The lot might visit the workstation  $i$  few times.
3. The order arrival distribution is assumed to be exponentially distributed.
4. The order release dates are assumed to be exponentially distributed.
5. Only  $w_7$  and  $w_{14}$  (both utilization level are greater than 90%) are used as the bottleneck workstations, to simplify the monitor system.
6. All due-dates are simulated and collected when the system reaches a steady state, based on historical information. During the simulation, the on-time delivery rates obtained using the four dispatching rules without monitoring the aggregated time buffer, are 76%, 76%, 88% and 90% (Table 4), respectively, where  $h = 3.8$ .

$$d_i = a_i + p_i \times 3.8$$

where  $d_i$ : the due-date of  $i$ th lot;  $a_i$ : the releasing date of  $i$ th lot;  $p_i$ : the processing time of  $i$ th lot.

Table 2  
Due-date estimation for different dispatching rules

Dispatching rules	Due-date estimation
FIFO	$d'_i = a_i + (-668768) + 9351.61q_i + 3.20p_i$
SRPT	$d'_i = a_i + (-2645955) + 5647.23q_i + 6.05p_i$
EDD	$d'_i = a_i + (-1999098) + 13870.38q_i + 3.98p_i$
SLACK	$d'_i = a_i + (-1639576) + 15596.58q_i + 3.29p_i$

$d'_i$ : time at which probability that the  $i$ th lot has been completed is 50%.  
 $p_i$ : the total processing of the lot  $i$ .  
 $q_i$ : the number of jobs in the work center queues on the job's routing when lot  $i$  arrives.

Table 3  
Utilization of the workstations

	$w_1$	$w_2$	$w_3$	$w_4$	$w_5$	$w_6$	$w_7$	$w_8$	$w_9$	$w_{10}$	$w_{11}$	$w_{12}$
U%	11	9	16	15	80	52	94	58	86	69	58	62
WIP	13.24	11.89	13.59	11.77	3.74	1.4	12.44	1.95	5.16	3.45	3.79	3.05
	$w_{13}$	$w_{14}$	$w_{15}$	$w_{16}$	$w_{17}$	$w_{18}$	$w_{19}$	$w_{20}$	$w_{21}$	$w_{22}$	$w_{23}$	$w_{24}$
U%	22	99	22	3	8	3	36	84	86	60	87	47
WIP	0.32	19.58	0.51	0.04	0.11	0.04	1.83	13.10	7.18	1.60	3.20	2.73

Table 4  
The mean value of the cycle time in experimental I and II (unit: h)

Rule	AL		AT		VAT		CT		OTD%	
	I	II	I	II	I	II	I	II	I	II
FIFO	20.95	11.68	-64.25	-73.27	84.99	79.29	781.46	769.81	0.76	0.81
SRPT	22.28	17.89	-67.96	-72.50	105.57	100.12	774.52	770.94	0.76	0.79
EDD	4.65	4.02	-75.07	-79.66	54.03	56.15	769.22	764.43	0.88	0.90
SLACK	3.40	2.29	-75.30	-82.91	51.26	56.79	769.40	761.01	0.90	0.93

I: without aggregated time buffer control; II: with aggregated time buffer control.

#### 4.2. Due-date estimation based on JIQ method

As indicated above, the lead time is determined to be 50% using a regression method (Kaplan & Urnal, 1993). Different dispatching rules yield different sequences, so the lead times under various dispatching rules are simulated using a regression method when the system runs for 100 days and enters a steady state (1700 lots/day), as presented in Table 2. (The number in the Table 2 is based on historical data and the simulation.)

#### 4.3. Determining the control point

As stated in Section 3.2, only bottleneck workstations need to be monitored, so the utility of each workstation is calculated from the CCPM. The simulation results indicate that  $w_7$  (deposition) and  $w_{14}$  (photolithography) have the highest utility, 99% and 94%. Also, the WIP at these two workstations is higher than in the others. In this work, only  $w_7$  and  $w_{14}$  (both utilization level are greater than 90%) are used as the bottleneck workstations and applied in the aggregated time buffer system, to simplify the monitor system. Table 3 presents the utilization of all workstations. However, a production manager should monitor workstations with utilization levels of  $\geq 80\%$  to prevent bottleneck shifting in the fabrication of wafers.

#### 4.4. Results and analysis

The result of the experiments indicate that the dispatching rule with an aggregated time buffer control, in terms of mean value and standard deviation, average lateness (AL), average tardiness (AT), variance in the average tardiness (VAT), cycle time (CT) and on-time delivery rate (OTD%) (Tables 4 and 5). The on-time delivery rates obtained using the aggregated time buffer (76%, 76%, 88%, and 90%) exceed



Table 5

The standard deviation of the cycle time in experimental I and II (unit: h)

Rule	AL		AT		VAT		CT		OTD%	
	I	II	I	II	I	II	I	II	I	II
FIFO	8.99	7.23	35.83	28.36	9.16	7.92	35.29	28.47	0.1183	0.0997
SRPT	11.68	10.78	31.97	27.25	13.12	21.30	31.97	28.65	0.1008	0.0917
EDD	4.40	4.27	32.91	29.25	8.62	15.35	32.96	29.33	0.1088	0.0984
SLACK	3.15	2.54	22.83	22.92	8.79	20.57	22.15	21.38	0.0866	0.0592

I: without aggregated time buffer control; II: with aggregated time buffer control.

Table 6

The comparison between experiment I and II

Rule	AL	AT	VAT	CT	OTD%
FIFO	**	**	**	**	**
SRPT	**	*	*	*	**
EDD	*	*	–	*	*
SLACK	–	**	–	*	*

\*\* : Significant with aggregated time buffer control at  $\alpha = 0.01$ \* : Significant with aggregated time buffer control at  $\alpha = 0.1$ .

those obtained without an aggregated time buffer (81%, 79%, 90%, and 93%), indicating that the due-date is set effectively when the aggregated time buffer control is used.

The experimental results were further studied by performing a *t* test at confidence levels of 99% and 90%. Table 6 shows that FIFO and SRPT dispatching rules significantly improve the control of order due-dates when the aggregated time buffer control system is integrated, at a confidence level of 99%, because these two dispatching rules do not consider the due-date in determining the production sequences. Therefore, implementing the aggregated time buffer control system greatly improves the order due-date control.

## 5. Conclusions

The data herein indicate that due-date control was improved, in terms of on-time delivery rate, average tardiness, variance of average tardiness and average lateness. The aggregated time buffer control system based on TOC theory is used to ensure that the order due-date is met. In this study, various dispatching rules with aggregated time buffer control in a wafer fabrication factory are simulated and analyzed. The results are summarized as follows:

1. The aggregated time buffer control system yields a significant improvement in meeting the due-date for various dispatching rules.
2. Experiment II yielded the results that were better than those in experiment I, regardless of the dispatching method used. Because the aggregated time buffer improves the accuracy of due-date performance.
3. In terms of average tardiness index, the aggregated time buffer control system is better when the due-date unrelated dispatching rules, FIFO and SRPT, are applied, indicating that the aggregated time buffer control system improves the accuracy of the due-date performance. In

contrast, the aggregated time buffer control does not significantly affect the accuracy of the due-date when the dispatching rules related to the due-date are used.

4. The aggregated time buffer control system yields better average lateness than obtained without such a buffer control system reducing the cost.

This study demonstrates that the aggregated time buffer control system with dispatching rules outperforms a system without aggregated time buffer control.

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