國 立 交 通 大 學

電子物理學系

碩士論文

具抬升式源汲極之多晶矽奈米線穿隧式薄膜電晶體之研究

A Study on Polycrystalline-Silicon Nanowire Tunnel Thin-Film Transistor with Raised Source/Drain

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中華民國 一〇三 年 七 月

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摘要

穿隧式場效電晶體相較於傳統金氧半場效電晶體已知具有較高的開關電流比、陡峭的次臨界擺幅以及極低漏電流。在本篇碩士論文中，我們第一次提出利用奈米線結構和抬升式源汲極來製作多晶矽穿隧式薄膜電晶體。多晶矽奈米線穿隧式薄膜電晶體的特性卻展現了較高的次臨界擺幅和較低的開關電流比。為了釐清較劣表現的原因，我們研究了不同元件在不同條件下的電流特性，例如：閘極長度、奈米線的數目、奈米線的粗細以及變溫量測，並且利用 TCAD 模擬探討元件的摻雜分布。透過變溫量測萃取出的活化能，我們發現這種多晶矽奈米線穿隧式薄膜電晶體的穿隧電流是由陷阱輔助穿隧效應來主導，也驗證了元件特性會較差的原因。接著將元件進行氨電漿處理，發現適中的電漿處理時間會有效降低元件中的陷阱，因此增進了關電流和次臨界擺幅。經過一系列的結果分析，這種多晶矽奈米線穿隧式薄膜電晶體會因為摻雜濃度分布的關係，沒有看到優異的電流電壓特性，或許可以透過能夠自我對準離子佈值的方法來製作奈米線穿隧式薄膜電晶體，來獲得更好的表現。

A Study on Polycrystalline-Silicon Tunnel Thin-Film Transistor with Raised Source/Drain

Student: Po-Wei Fong **Advisor: Dr. Tien-Sheng Chao**

Department of Electrophysics

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Abstract

It has been known that tunnel field-effect transistors (TFETs) exhibit higher on/off current ratio, steep subthreshold swing, and ultralow off leakage current than conventional MOSFETs. In this study, we propose a tunnel TFT fabricated with nanowire structure and raised source/drain for the first time. The polycrystalline-silicon nanowire tunnel TFT with raised source/drain demonstrates a higher subthreshold swing, low on/off current ratio that is below our prediction. In order to clarify the cause of poor performance, we studied the I-V characteristics of devices with different conditions, such as, gate length, number of nanowires, diameter of nanowires and various temperature, and the doping profile by using the TCAD simulation. By various temperature measurements and the extracted activation energy, we found that the doping profile and the trap assisted tunneling (TAT) mainly impact the performance of poly-Si nanowire tunnel TFT. Additionally, devices were done with the NH_3 plasma treatment, the moderate plasma treatment time would eliminate traps in devices, and thus the off current and the subthreshold swing were improved. From these results and analysis, we found that this kind of nanowire tunnel TFTs would not have superior I-V characteristics due to doping profile problem. To obtain better performance, nanowire tunnel TFTs might be fabricated with self-aligned implantation.

誌謝

時光荏苒，歲月如梭，轉眼間碩士班兩年就這樣進入尾聲，在這期間遇到許多榜樣以及貴人惠我良多。首先要感謝的是我的指導老師—趙天生老師，從我大二的時候就有修趙老師的電子學，上課的過程覺得老師是個慈祥的學者，如沐春風，因此我也鑽入了半導體電子的領域，在大三的時候就到趙老師的實驗室做專題，接著升上碩士直到現在，除了課業上的指導外，老師也不時的教導我們做人的道理，時常帶著感恩的心、不浪費資源，才能讓人類生命平安地永續長存。

實驗室的學長姐中，最感謝的是我的指導學姊陳昱璇，身為學姊第一個指導的碩士生，從實驗機台的訓練一直到做研究的方法，都能感受到學姊鉅細靡遺的指導，在我有問題的時候能不厭其煩地解說；雖然最後實驗結果不盡滿意，學姊也告訴我說：「做研究不是一定要有好的結果，大家都只發表最好的實驗成果是沒有意義的，能從失敗的結果討論出前因後果，那才是對整個研究最有貢獻價值的。」也因此我的碩士班能順利畢業。接著要感謝郭柏儀學長、嚴立丞學長、張添舜學長、林哲毅學長和卓大鈞學長，不僅在課業及實驗上各種問題解惑，在聊天談心上也以過來人的身分經驗分享，讓我的碩士生涯能更順利度過。另外特別感謝陳昱璇學姊、張添舜學長和嚴立丞學長能陪我做重訓，培養堅強的體格和充沛的體力，而且越多人一起做比較才不會有怠惰的心，讓我這兩年不僅有優良的學業成績也有更強壯的體格。

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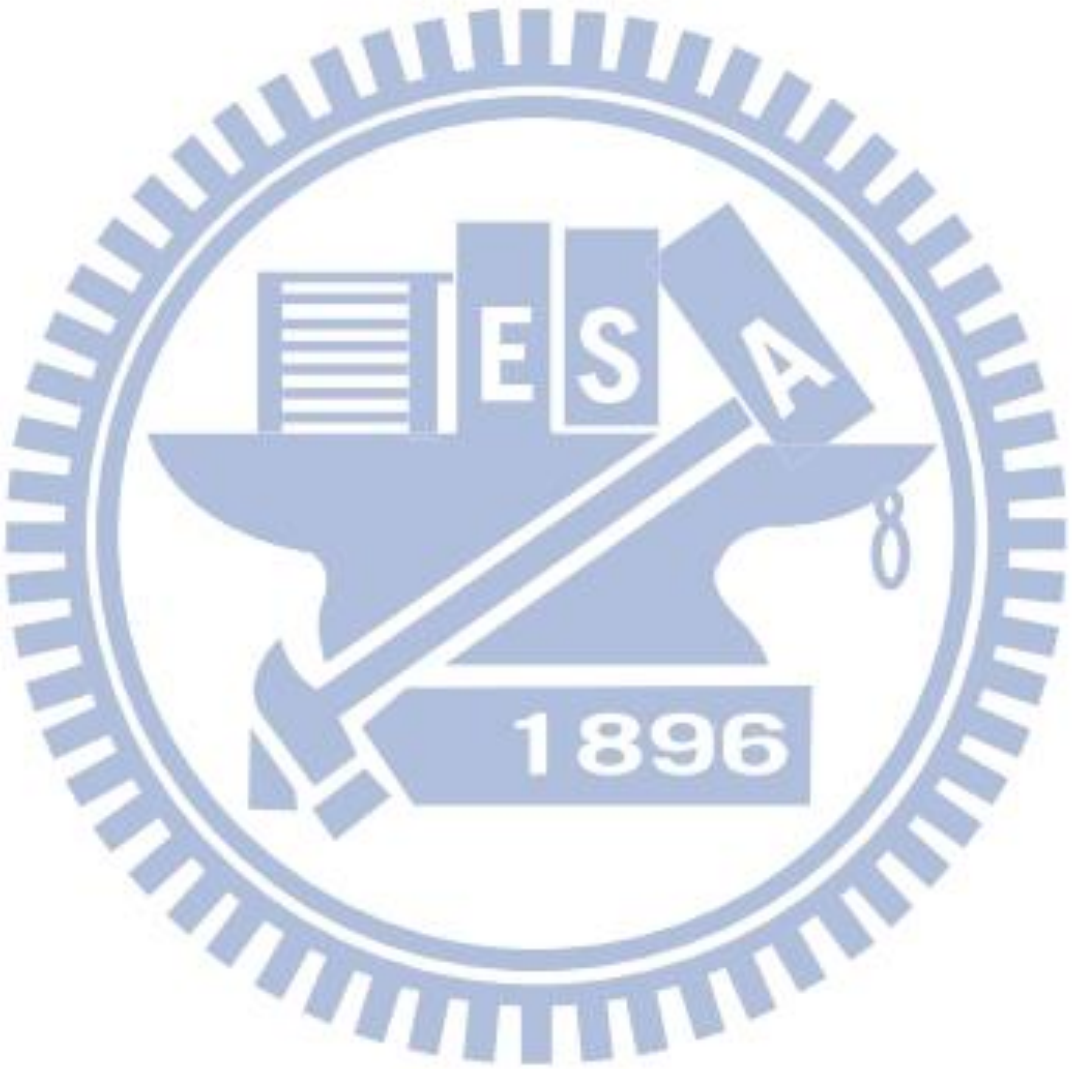
方柏崴 誌於交通大學



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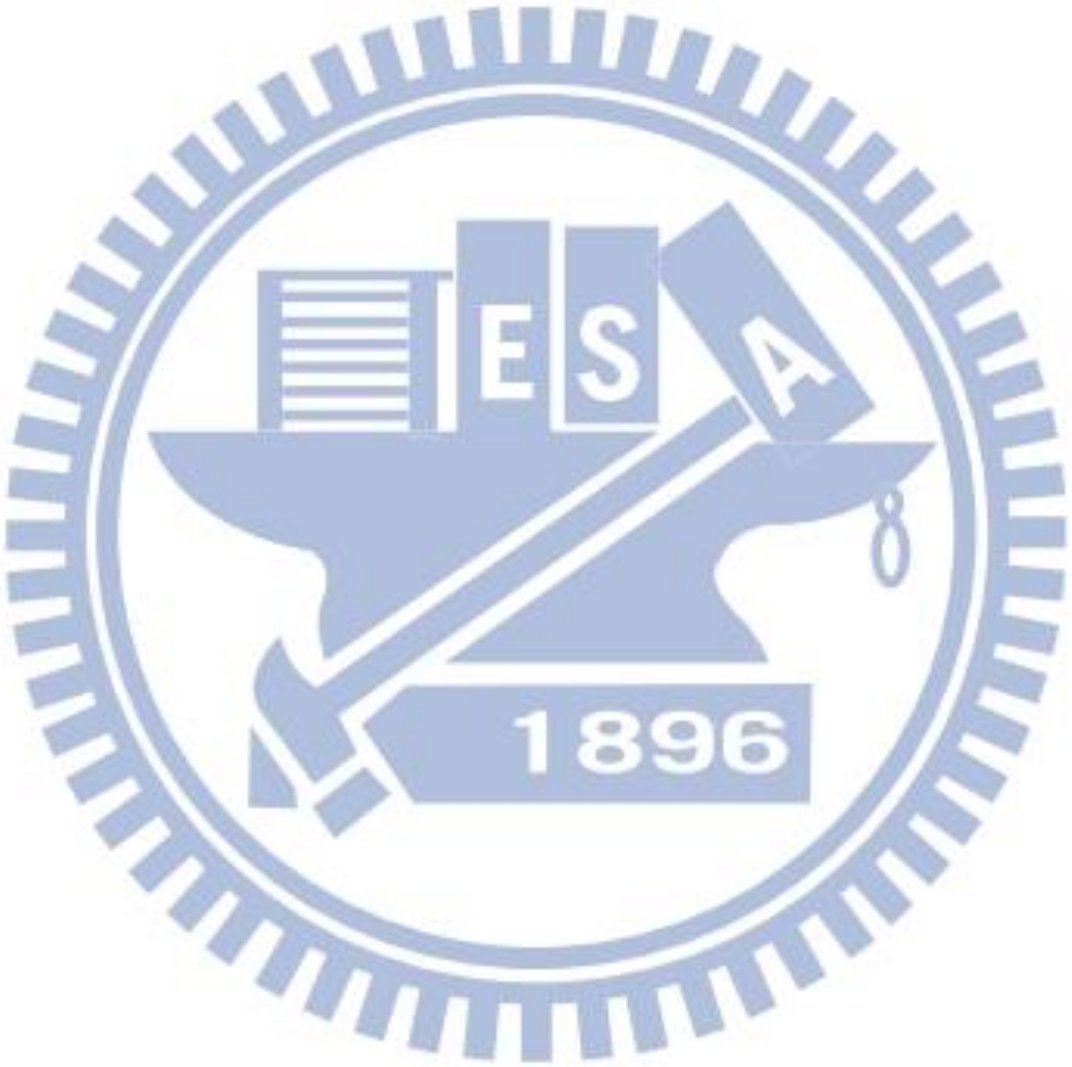

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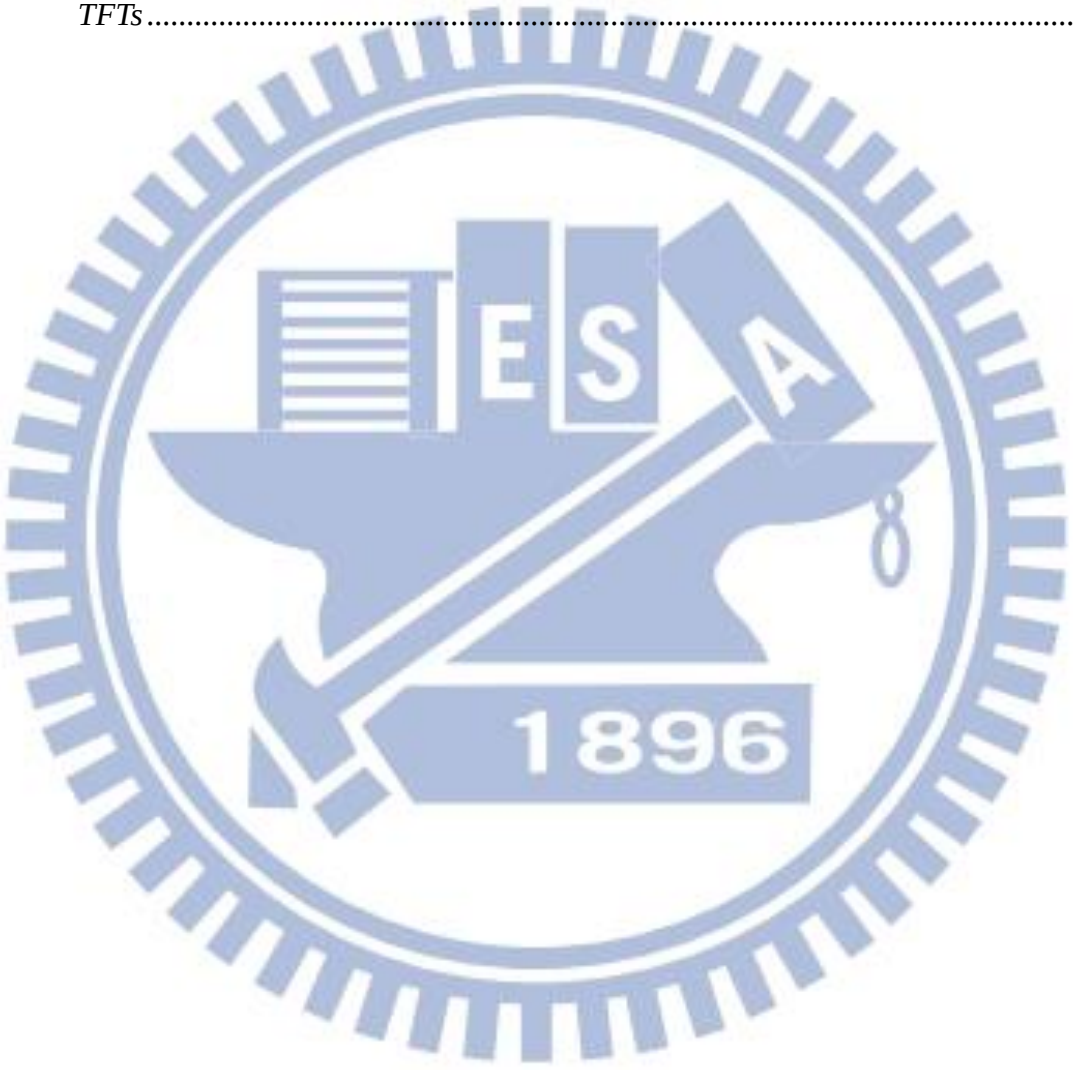


Chapter 1

Introduction

1.1 General Background

1.1.1 Polycrystalline silicon Thin Film Transistors

Since the first polycrystalline thin film transistors (Poly-Si TFTs) were fabricated in 1966 [1], enormous researches have been proposed and expanded the application of poly-Si TFTs. Initially, amorphous silicon TFTs (α-Si TFTs) were chosen to be switch devices in the industry applications. However, the low drive current of the α-Si TFT due to its low field effect carrier mobility μ_{EF} (about several $cm^2/V\text{-}s$) makes the α-Si TFT gradually be replaced by poly-Si TFTs. Poly-Si TFTs have been confirmed to have the higher carrier mobility resulting in the improvement of the drive current, the switching speed and the subthreshold swing. Therefore, poly-Si TFTs exhibit great potentials for the device scaling, enlarging open ratio, higher resolution, and lower power consumption.

With the coming of the digital times and the rise of the planar liquid crystal displays (LCD), polycrystalline silicon thin-film transistors (poly-Si TFTs) have been studied and widely used in active-matrix liquid crystal displays (AMLCDs) [2], image sensors, photo-detector amplifiers, and flat panels [3], due to its better performances compared to α-Si TFTs. Furthermore, poly-Si TFTs can be fabricated with low temperature process, which is called low temperature poly-silicon (LTPS), and make it more promising to apply to system on panel (SOP), system on chip (SOC) and three dimensional integrated circuits in the future.

However, it is important that the grain boundaries and defects in the poly-Si result in the

degradation of the device performance. The defects in grain boundaries would trap carriers and generate a potential barrier and this could degrade the on state current of poly-Si TFTs. There are several methods which have been proposed to improve the performance of poly-Si TFTs, for example, enlarging the grain size and reducing trap states in poly-Si films.

1.1.2 Nanowire Transistors

In recent years, for achieving the purpose of improving device characteristics and reducing manufacturing cost, the size of devices should be scaled down continuously. According to Moore's Law, the number of transistors in a dense integrated circuit doubles approximately every two years from 1964. In an effort to continue Moore's Law, the gate length of a transistor should be scaled down, as illustrated in Figure 1-1 [4].

With the shrinking of the MOSFET, the device behavior will be changed compared with the long channel devices, which is called the short channel effects (SCEs). The SCEs can be attributed to two physical phenomena: 1) the limitation imposed on electron drift characteristics in the channel, 2) the modification of the threshold voltage due to the shortening channel length [5]. When the channel length is scaled down below 0.3 μm, SCEs will obviously impact the device behavior which means that the gate length is not the only parameter to be scaled down. In order to improve the gate controllability, there are many parameters need to be accounted for, for example, the oxide thickness and the substrate doping, but that will increase the challenges in scaling the gate length in planar bulk MOSFETs more difficultly.

Non-planar devices, such as Double-gate FETs, Tri-gate FETs, FinFETs and Ω-gate FETs [6] have been developed as shown in Figure 1-2 [7], and FinFETs have been applied to the central processing unit (CPU) and produced by Intel in 2011 as illustrated in Figure 1-3. These multi-gate

devices have more directions of the gate field that provide better gate controllability, therefore, SCEs can be suppressed and they show a steep subthreshold swing and lower leakage current. Additionally, Nanowire transistors are considered to be one of the most promising device structures that can extend the scaling roadmap of the CMOS devices [8]. With the less dimensions of the channel and the limited body, the nanowire devices exhibit the best control of the channel potential.

1.1.3 Tunnel Field-Effect-Transistors

During the last several decades, semiconductor devices have been developed and improved noticeably due to achieving higher density, better performance and lower power consumption. With the scaling down of the transistor gate length, the supply voltage and the threshold voltage should be reduced to improve the performance and keep the overdrive factor [9], as shown in Figure 1-4. This results in the exponentially increasing of the off current for the subthreshold swing limit, which is 60 mV per decade at room temperature.

The Tunnel Field-Effect-Transistor (TFET) is one of the most promising candidate for the current CMOS technology node. Figure 1-5 illustrates the n-channel conventional MOSFET and the n-channel TFET and their operation band structure. The TFET operates by band-to-band tunneling (BTBT), which is different from the conventional transistor operating by thermal emission, so the TFET does not suffer from the subthreshold swing limit. This permits low standby leakage current and the scaling of the supply voltage, and thus it can achieve ultralow swing, lower off current, and higher on/off current ratio. Even though TFETs have been studied and experimented with superior performance, the low on current is the major issue that should be dealt with.

The on current of the TFET depends critically on the transmission probability, T_{WKB}, which is

calculated using the Wentzel-Kramer-Brillouin (WKB) approximation:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\,3}}}{3q\hbar(E_g+\Delta\Phi)}\right)$$

Where m* is the effective mass, E_g is the bandgap, λ is the screening tunneling length which depends on the device geometry, and ΔΦ is the energy difference between the valence band of the source (or channel) and the conduction band of the channel (or source). Observing from the approximation, m*, E_g and λ should be reduced to increase the barrier transparency (i.e., improve the tunneling rate). There are many approaches, such as using the heterostructure at the source side including the silicide source [10], strained silicon [11], using lower bandgap material (III-V compounds [12], Si-Ge [13, 14]), and the multi-gate structure, including the double gate [15] and the gate-all-around nanowire [16].

1.2 Motivation

LTPS TFTs have been widely used in consumer electronics in this era and are promising for future three dimensional integrated circuit (3D-IC) application. Compared with current planar circuits design, the device density of 3D-IC can be increased by vertical integration, which is a feasible way to extent the Moore's Law. Furthermore, the devices on second layer and more can be solely realized by LTPS TFTs because of the thermal budget issue and the lack of single crystalline silicon seed layer.

Considering the trend of the low power consumption and the low standby power, the importance and urgency of the steep swing device is revealed day by day. The tunnel FETs which operated by the band-to-band tunneling (BTBT) are the most promising devices that could lead to

ICs operating at a very low supply voltage, V_{DD} < 0.5 V. Here is an expression of the subthreshold swing of a tunnel FET [17]:

$$S = \ln 10 \left[\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_{GS}} + \frac{\xi + b}{\xi^2} \frac{d\xi}{dV_{GS}} \right]^{-1}$$

There are two terms in the denominator which should be maximized to obtain a low subthreshold swing. The first term suggests that a transistor geometry with a high-κ and an ultrathin body could obtain better electrostatic control, and the second term suggests that the swing would be improved if the applied gate field could align with the internal field of the tunnel junction.

Therefore, we use propose the nanowire TFET with raised source/drain, whose process can fabricate silicon nanowires and raised source/drain simultaneously without the use of advanced lithography tools [18], for the first time. With the nanowire structure with the superior gate electrostatic control and the raised source/drain which could reduce the resistance, we hope to achieve the desirable TFET performance, such as the steep subthreshold swing and the high on/off current ratio.

1.3 Organization of the Thesis

There are four chapters in this thesis. Chapter 1 depicts the background of the use of the polysilicon and the evolution of the multi-gate technique from planar device to gate all around nanowire. It also briefly describes advantages and the current situation of the tunnel field-effect transistor.

In chapter 2, we describe the operation principle of TFET and then present the process of the poly-Si nanowire tunnel TFTs with raised source/drain with different gate conditions: underlap or

overlap. Besides, the measurement tools and methods are also introduced and defined in this chapter.

In chapter 3, the device characteristics and measurement results are analyzed and discussed in detail, such as, the on/off current and subthreshold swing in relation to the length and numbers of nanowires. In order to confirm the tunneling mechanism of our devices, the activation was extracted. And the plasma treatment was done and discussed.

In chapter 4, the conclusion of this study is presented. Finally, the future work and the suggestion of device improvement are presented.

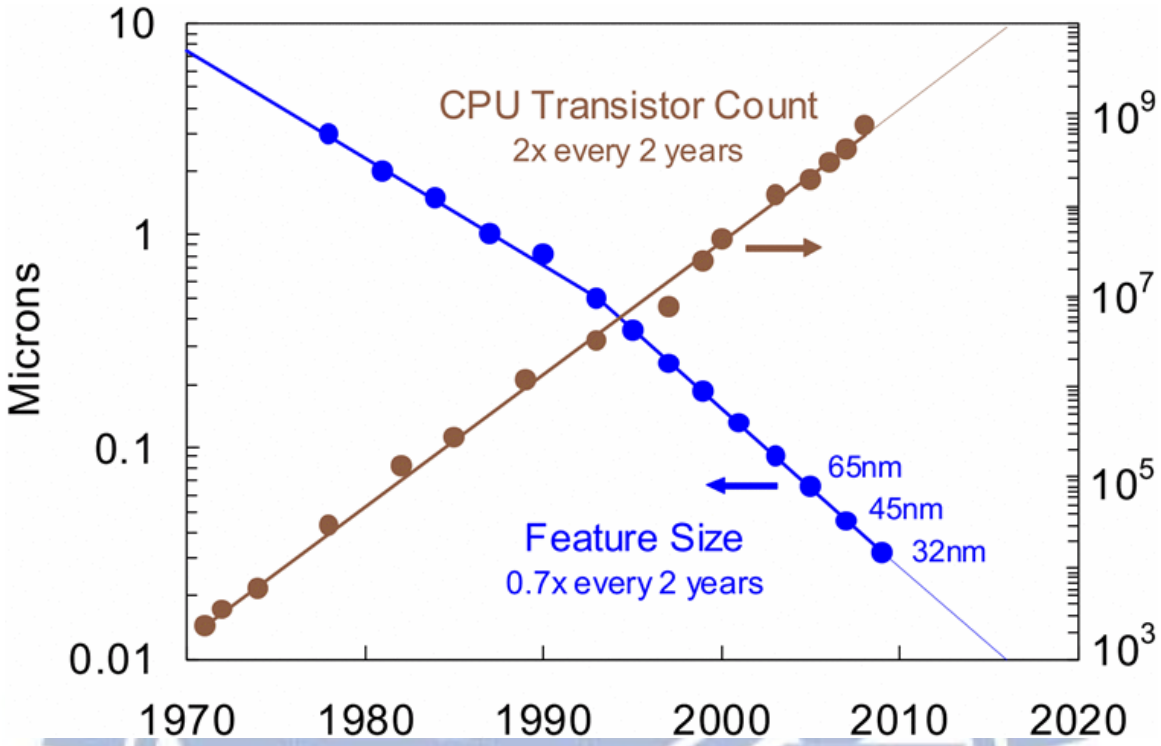


Figure 1-1 Moore's Law [4]

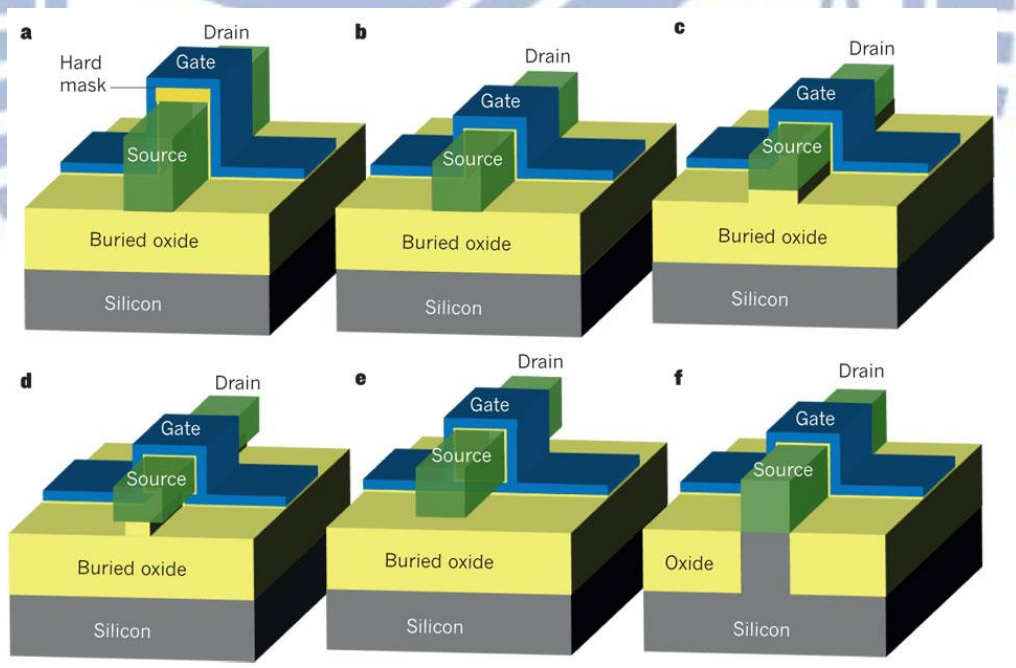


Figure 1-2 The different types of the gate electrode wrapping the channel [7]

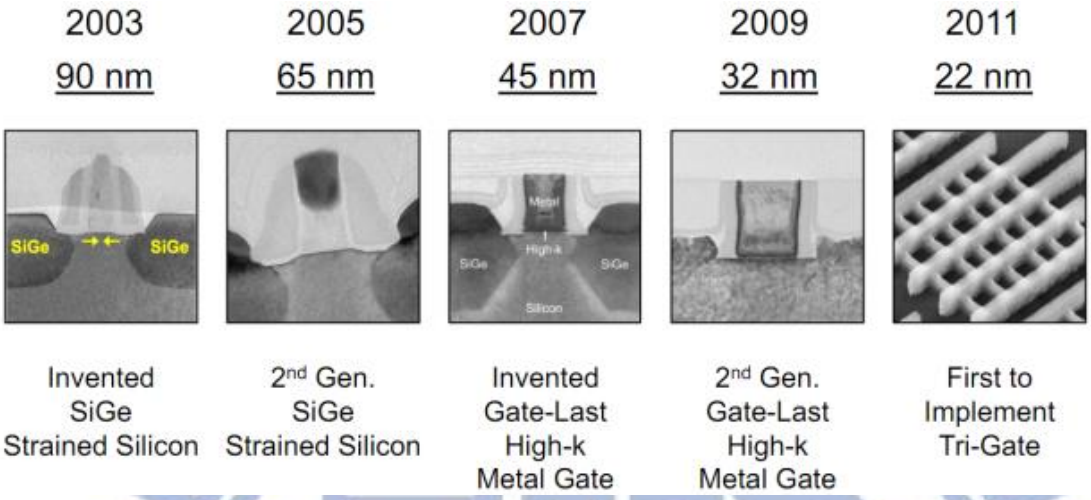


Figure 1-3 The evolution of the transistor generation introduced by Intel

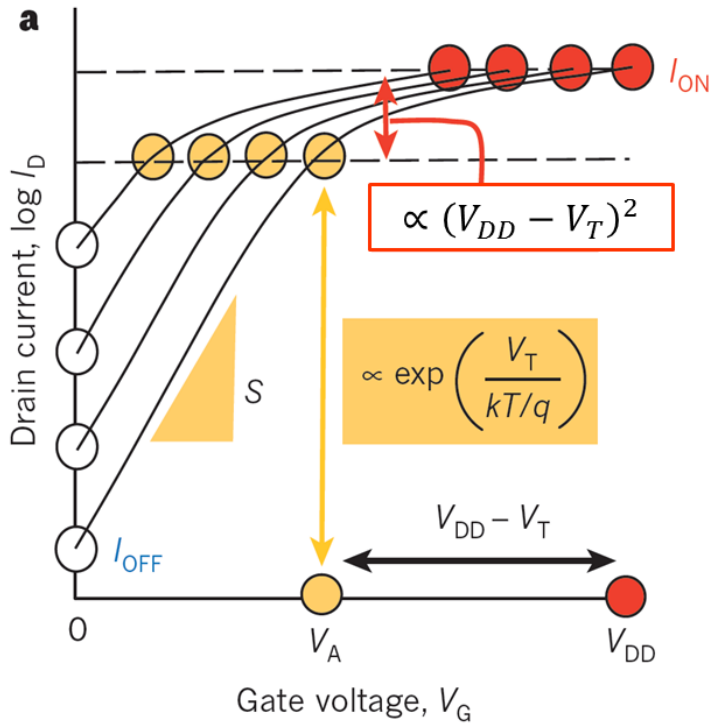


Figure 1-4 Transfer characteristics of a MOSFET shows that I_{OFF} increases exponentially because of the invariant subthreshold swing, S = 60 mV/dec. [9]

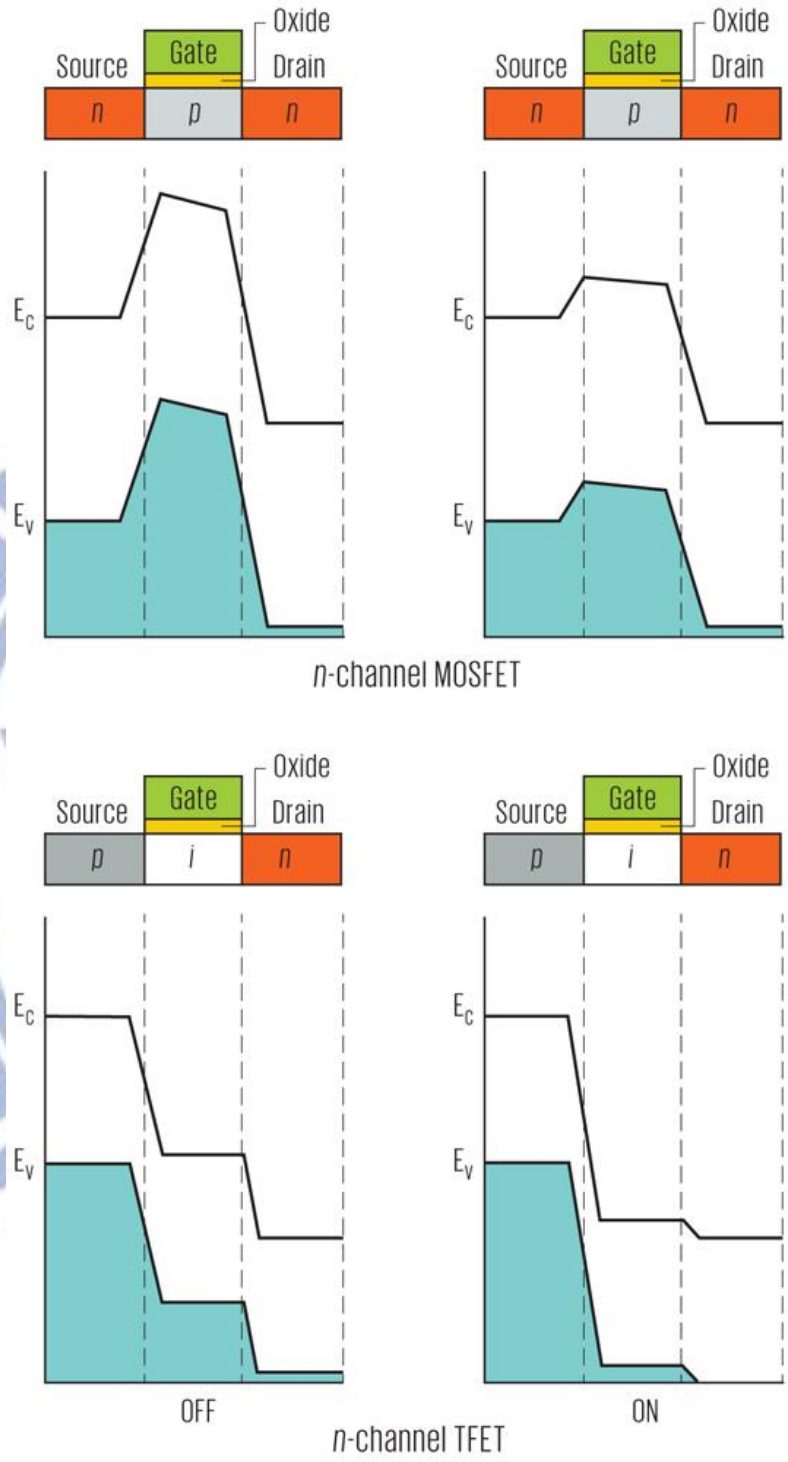


Figure 1-5 The n-channel conventional MOSFET and the n-channel TFET. The left side is in the off state and the right side is in the on state. [19]

Chapter 2

Device Fabrication and Experimental Setup

2.1 The Principle of Tunnel Field-Effect Transistors

The Tunnel Field-Effect Transistor consists of a gated p-i-n diode which is reverse biased to get an ultra-low leakage current. Figure 2-1a shows a typical planar p-type TFETs, which has an n+ source, a p+ drain and the intrinsic substrate. Figure 2-1b shows the energy band diagram of operation of a p-type TFET including the off state (dashed blue lines) and the on state (red lines). In the off state, the valence band edge of the channel is below the conduction band edge of the source, so there is no current flowing through the channel due to no empty states allowing holes tunneling into the channel which is the reason that the off current is quite low. In the on state, the energy band of the channel is pulled up, the valence band edge of the channel is higher than the conduction band edge of the source, so holes can tunnel from the source to the channel.

Only carriers in energy window, $\Delta\Phi$ (green shading), can tunnel into the channel, because the high and low energy part of the source Fermi distribution are cut off, as illustrated in Figure 2-1b, which is like the conventional MOSFET that is cooled down to a low temperature. Therefore, the subthreshold swing, S, could be below 60 mV/dec, as shown in Figure 2-1c. However, the channel valence band would be lifted up by the gate voltage, and the tunneling length would be reduced by the gate voltage simultaneously, so the subthreshold swing of a TFET is not a constant (Figure 2-1c).

2.2 Experimental Procedure

The process flow of the poly-Si thin-film tunnel field-effect transistors is shown in Figure 2-2 (a)-(j). First, we utilized a 6 inch (100) silicon wafer as a substrate and deposited wet oxidation. The dummy sandwich structure Si_3N_4 (30 nm) / SiO_2 (20 nm) / Si_3N_4 (30 nm) was deposited by low-pressure chemical vapor deposition (LPCVD). After the patterning and etching of the nanowire definition, the cavities of the oxide layer is etched laterally by the selective wet etching. The 100 nm amorphous Si (α-Si) layer was then deposited by LPCVD, which formed the Si nanowire channel and the raised S/D at the same time. The raised source region was implanted with BF_2^+, at 40 keV, at 5 x 10^{15} cm^{-2} and the drain was implanted with P^+, at 26 keV, at 5 x 10^{15} cm^{-2}, then the α-Si layer was crystallized by solid-phase crystallization (SPC) at 600ºC for 24 h in N_2 ambient. Then the raised source/drain and the nanowire region were patterned and dry etched. The dummy sandwich structure was removed by wet etching by using H_3PO_4 and diluted HF, and Si nanowires were suspended. Next, 7 nm oxide as the gate dielectric and 250 nm in-situ n^+ polysilicon as the gate electrode was deposited. Finally, we completed the fabrication after the lithography and the dry etching. The poly-Si gate was designed in two conditions: underlap gate and overlap gate shown in Figure 2-2 (j) and (k).

The underlap gate devices had additional processes to improve the device performance. After underlap gate devices was deposited TEOS oxide of 30 nm as the liner oxide, the source and drain was implanted and then annealed by microwave with 300 W for 600 sec.

2.3 Method of Device Parameter Extraction

2.3.1 Measurement Tool Setup

The measurement tool setup for the I-V characteristics of nanowire TFETs are presented in Figure 2-3, including the SCS Parameter Analyzer (Keithley 4200), the pulse pattern generator (Agilent 81110A), the low leakage current switch mainframe (Keithley 708A) and the probe station.

Keithley 4200 is equipped with programmable source-monitor units (SMU) and provides a high resolution to measure DC I-V and pulse characterization of semiconductor devices.

Agilent 81110A with two pulse channels supplies high timing resolution pulse. When a device is measured in the probe station, KEITHLEY 708A, which is configured a 10-input × 12-output switching matrix, switches the signal from KEITHLEY 4200 and Agilent 81110A.

2.3.2 Threshold Voltage

There are two physical definitions for the threshold voltage of a TFET: gate threshold voltage and drain threshold voltage, which are based on the saturation of the tunneling barrier length shortening with respect to V_G and V_D [20]. These two values can be extracted by (trans)conductance derivative. In this thesis, we will use the constant current method and the onset voltage to extract the threshold voltage. The constant current is defined as the gate voltage that yields a drain current of 10 nA which is widely used in industry because of its simplicity [21] and also utilized in most of the studies of TFTs. The onset voltage is defined as the gate voltage when the tunneling behavior begins which is also used in tunnel FETs [22].

2.3.3 Subthreshold Swing

The subthreshold swing (S.S.) is a widely used value to judge the gate controllability of a transistor. The typical transfer characteristics of a MOSFET, which is I_D-V_G curve, includes three regions: the subthreshold region, the linear region and the saturation. The subthreshold swing is defined as the inverse slope of the drain current (I_D) over the gate voltage (V_G) in the subthreshold region:

$$S.S. = \left[\frac{d log I_D}{dV_G}\right]^{-1}$$

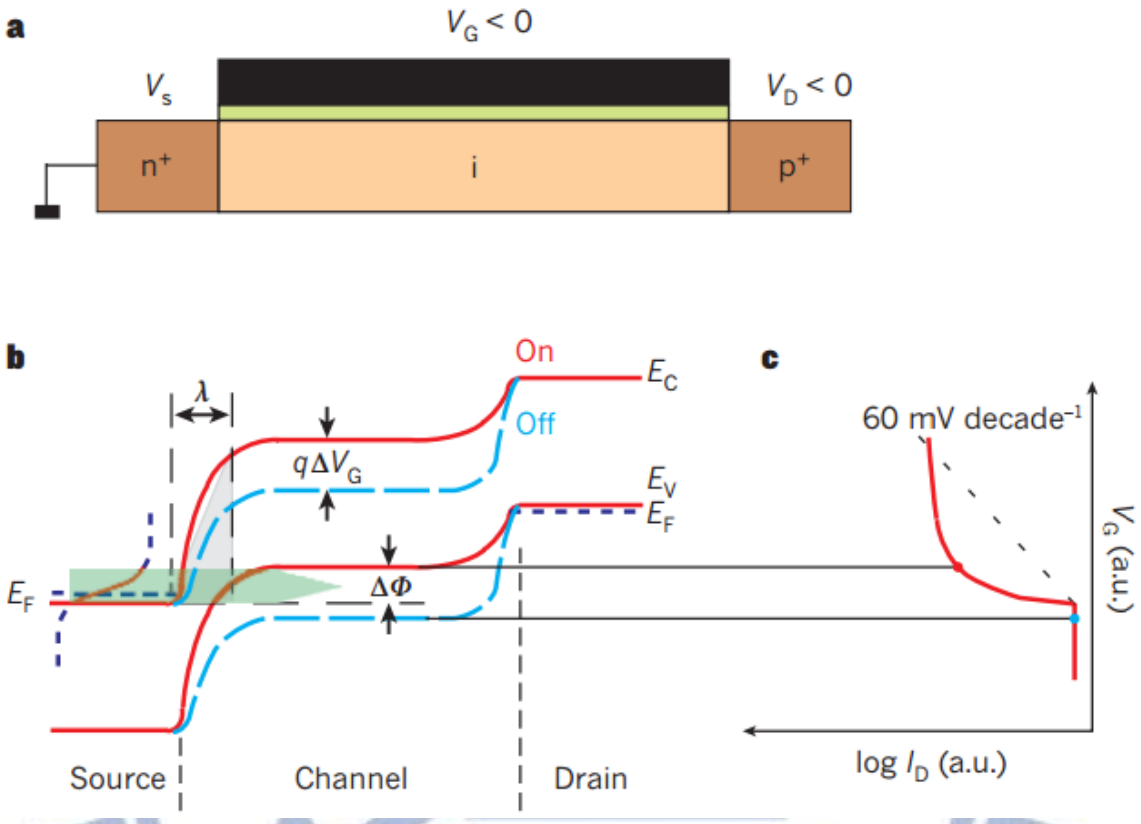
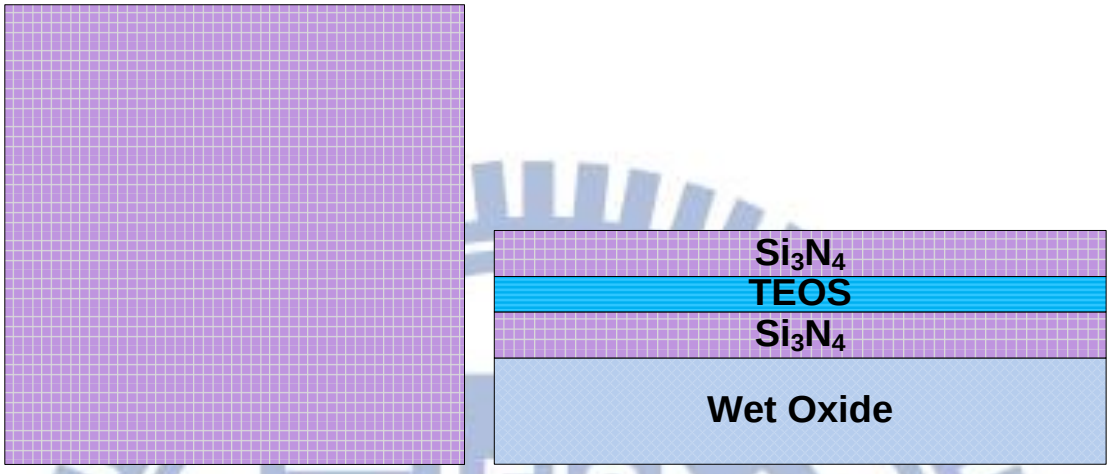
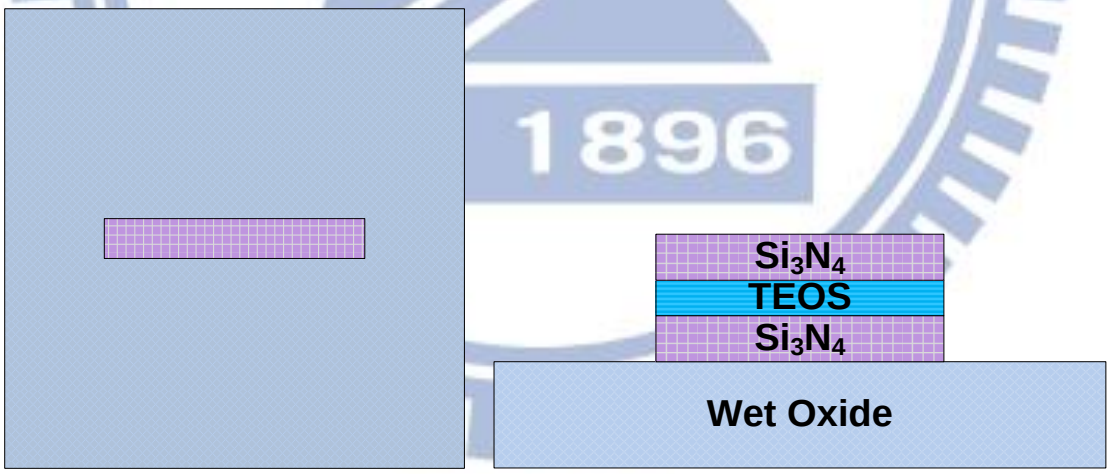


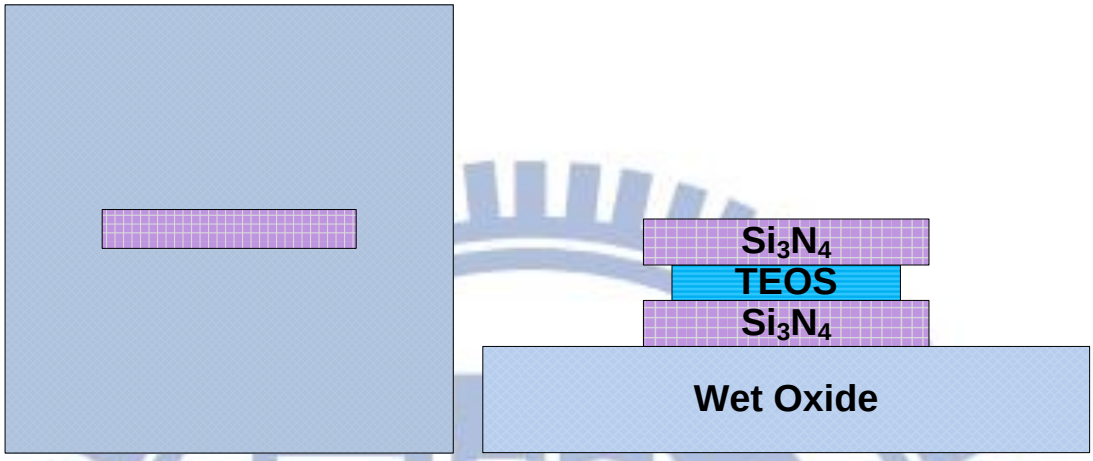
Figure 2-1 Principle of operation of a TFET. (a) Typical structure of planar p-type TFET (b) Schematic energy band profile for the off state and the on state in a p-type TFET (c) The ID-VG characteristics of a TFET compare with the limit of 60 mV/dec [9].



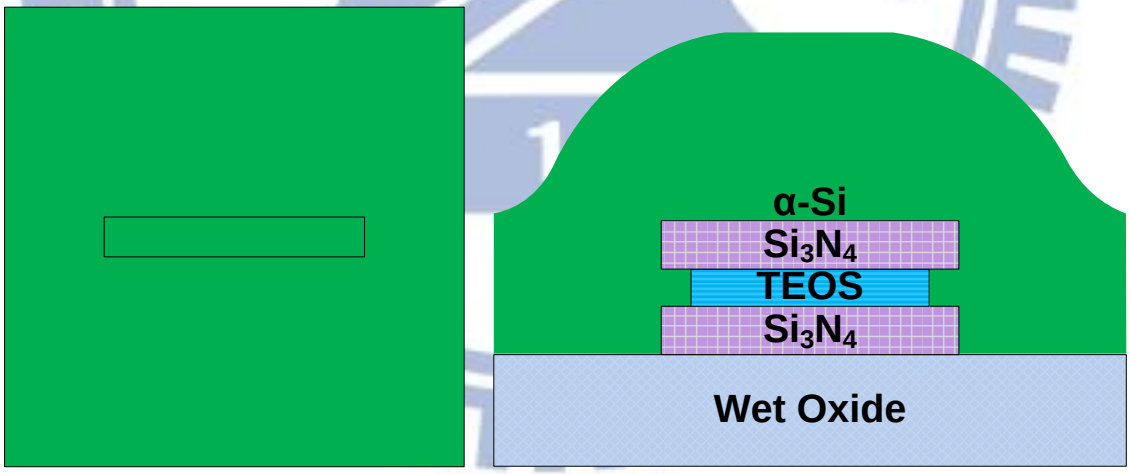
(a) wet oxide (500 nm) and Si_3N_4 (30 nm) / TEOS (20 nm) / Si_3N_4 (30 nm)



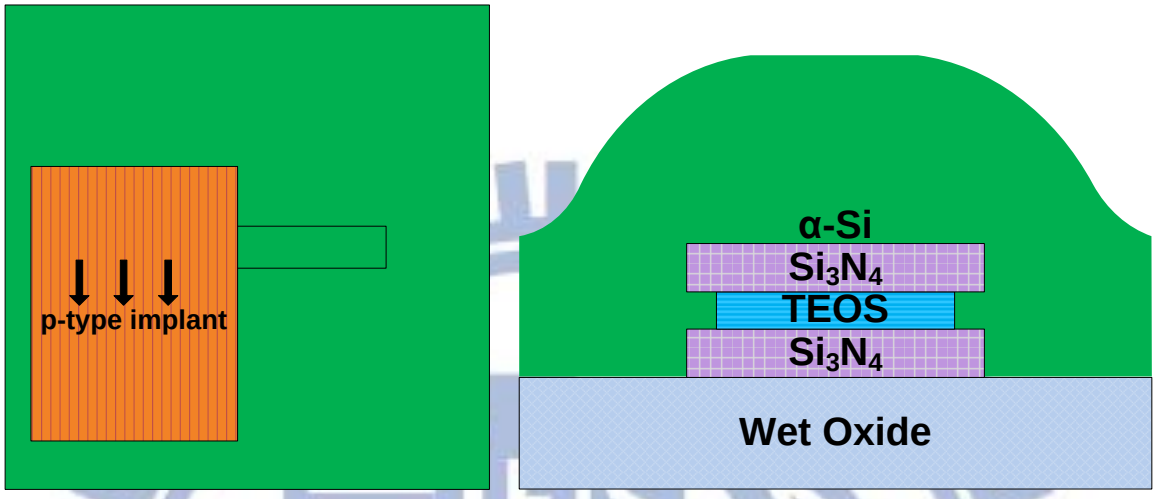
(b) nanowire region definition by lithography and dry etching



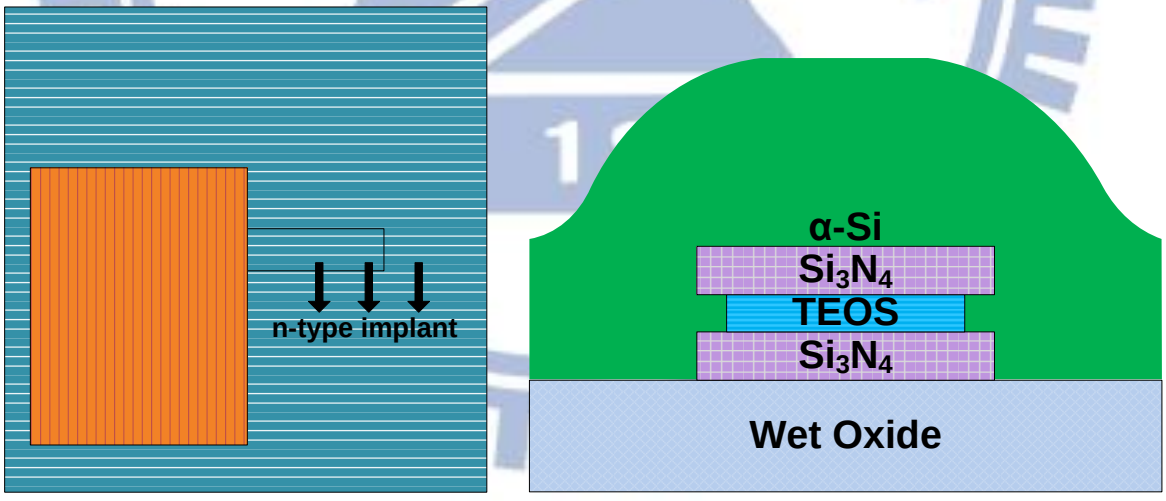
(c) cavities etching by HF wet selective etching



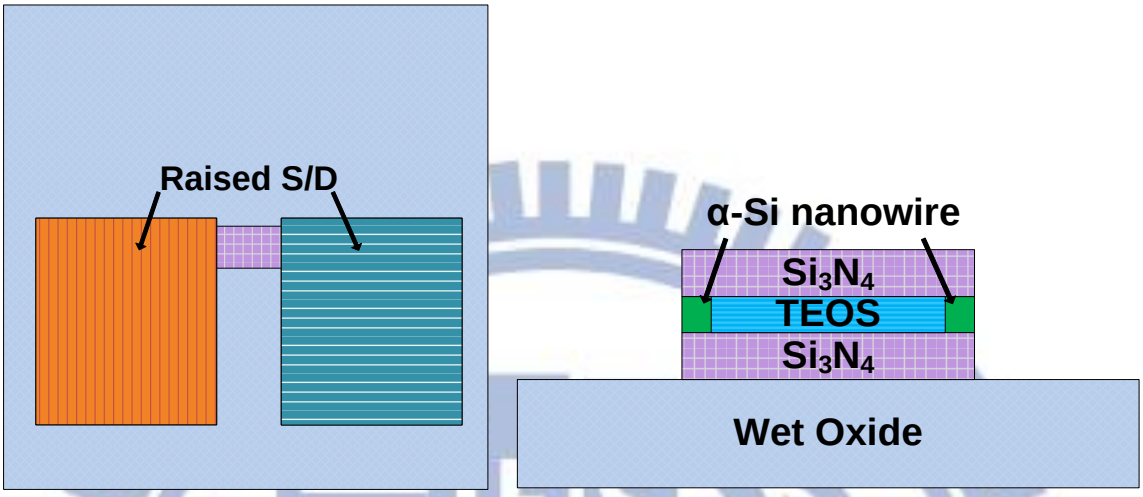
(d) amorphous Si (α-Si) (100 nm) deposition by LPCVD



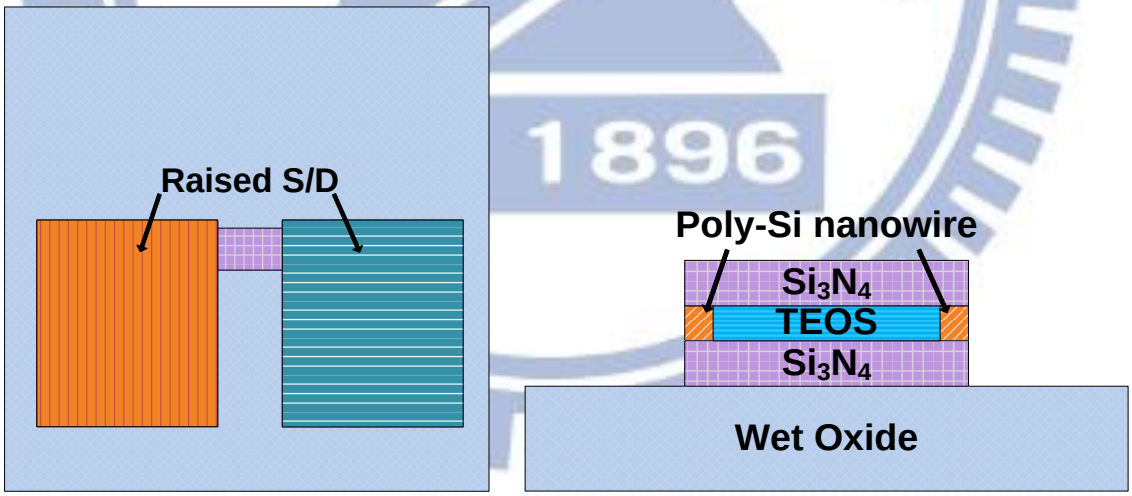
(e) p-type implantation



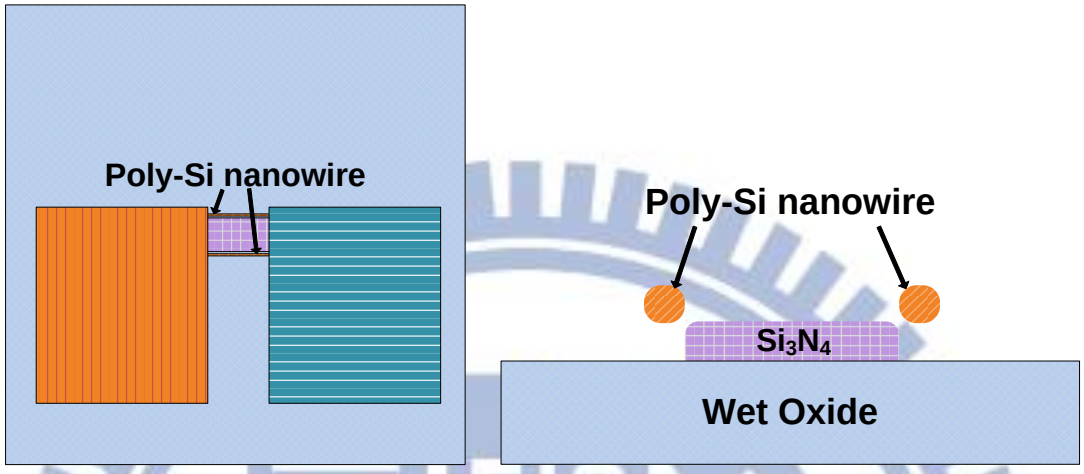
(f) n-type implantation



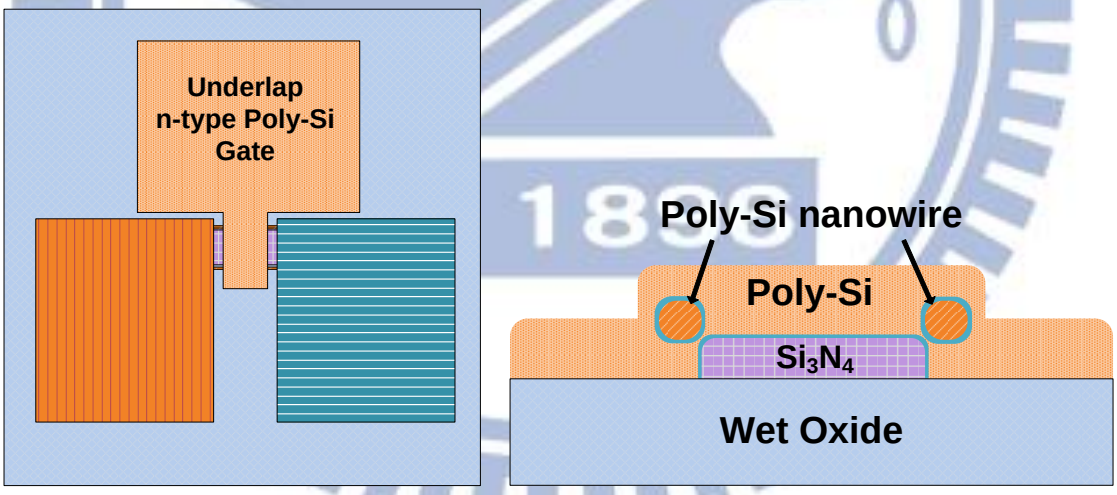
(g) nanowire region and raised S/D by dry etching



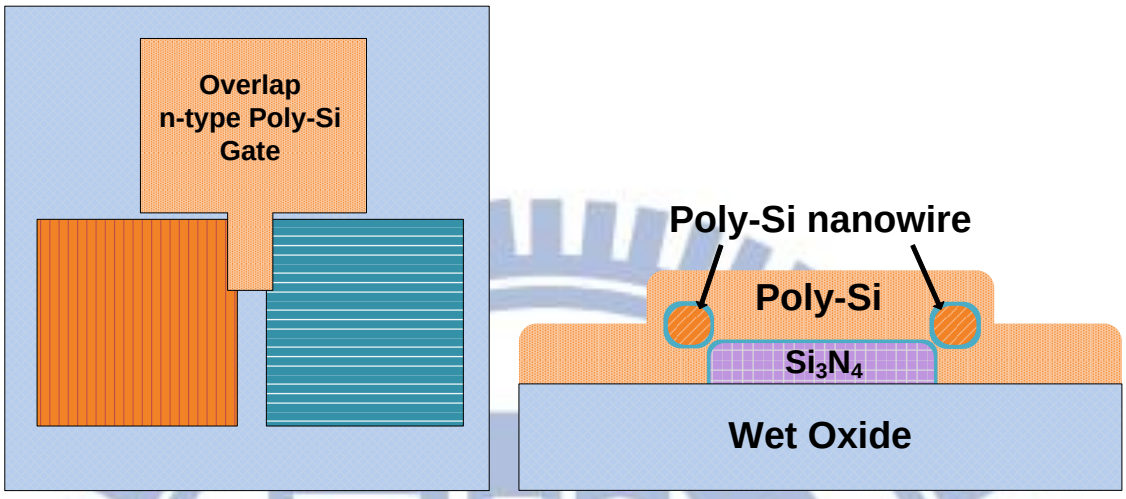
(h) solid phase crystallization (SPC) 600^{o}C 24 hr



(i) nanowire channels revealed by H_3PO_4 wet etching



(j) underlap gate: gate dielectric and in-situ n-gate deposition, and dry etching



(k) overlap gate: gate dielectric and in-situ n-gate deposition, and dry etching

Figure 2-2 (a)-(k) The process flow of the poly-Si nanowire thin-film TFET with raised source/drain

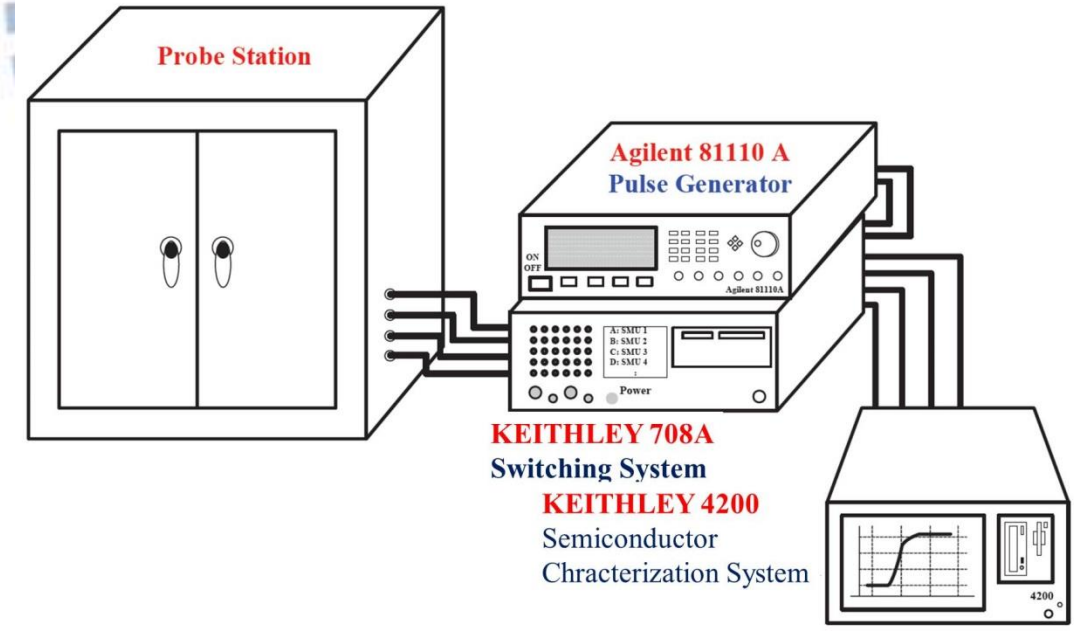


Figure 2-3 The experimental setup for the transfer characteristics of the poly-Si nanowire thin-film TFET with raised source/drain

Chapter 3

Poly-Si Nanowire Tunnel Thin-Film Transistors

3.1 Introduction

In this chapter, we will discuss the characteristics of the poly-Si thin-film transistors with underlap gate and overlap gate, respectively. With different conditions such as, length, numbers of nanowires and different diameter, the on/off current ratio, the subthreshold swing and the threshold voltage will be demonstrated.

3.2 Characteristics of Poly-Si Nanowire Tunnel Thin-Film Transistors with Underlap Gate

Figure 3-1 is the cross-sectional TEM image of a nanowire channel. The dummy sandwich NON stack was soaked in diluted HF to obtain a cavity of 20 nm height and of 25 nm / 35 nm / 45 nm depth. The diameter of NWs would be further reduced after the dry etching (Figure 2-2 (h)) and the H_3PO_4 wet etching (Figure 2-2 (i)). The final shape of a NW is elliptic cylindrical.

The I_D-V_G characteristics of a poly-Si nanowire tunnel TFT with underlap gate is shown in Figure 3-2. The behavior performs low ON current (I_{ON} ~ $8x10^{-12}$ A) and poor subthreshold swing (S > 1000 mV/dec). The low ON current can be attributed to large parasitic resistance and low doping concentration at source region. The S.S. degradation is due to the low doping concentration and the trap assisted tunneling (TAT). The low doping concentration makes the tunneling field lower and thus the tunneling distance is larger which results in poor S.S. Because

of additional implantation of underlap gate devices, there are traps appearing in the tunneling junction which enhances the TAT.

The on resistance of a poly-Si nanowire tunnel TFT with underlap gate is up to 50 MΩ as shown in Figure 3-3 (a), which confirms the very large resistance. Therefore, in order to improve the current drive of an underlap NW TFET, an overlap NW TFET was proposed. With a gate-to-source/drain-pad overlap structure, the on resistance could be successfully reduced from 50 MΩ to 150 kΩ as shown in Figure 3-3.

3.3 Characteristics of Poly-Si Nanowire Tunnel Thin-Film Transistors with Overlap Gate

The I_D-V_G characteristics of a poly-Si NW tunnel TFT with overlap gate in n-type and p-type are shown in Figure 3-5 (a) and (b). The curves exhibit higher ON current and better S.S which benefit from the overlap structure. However, the S.S. is still unacceptably large due to an occurrence of TAT and a less steep source-channel doping profile owing to long term annealing. We will discuss the TAT by using the temperature measurement and extracted activation energy later.

The source-gate-channel doping profile can be seen in Figure 3-6 (b) which is the cross-section image of the source pad in the simulation. Due to long term annealing, phosphorous diffused from the drain pad into nanowires and source pad as shown in Figure 3-7, and BF_2 was not implanted deep avoiding damage nanowires, there is an n^- region between the source and nanowires. When an n-type TFET is on (the applied gate voltage is positive), the distance between the inversed nanowire channel and p^+ region is so long that the tunneling length is large

as illustrated in Figure 3-8.

Figure 3-9 presents the on and off current versus the gate length of poly-Si nanowire TFET with diameter ~ 12 nm. The drive current and off-leakage current for single crystal are nearly independent of the gate length [23]. The invariant drive current is also found in tunnel TFTs because tunneling current dominates at on-state. On the other hand, the off current gets higher as the gate length is shorter due to the larger diffusion coefficient of phosphorus. When the gate length is short, phosphorus distribution would be near the p^+ source region, and it leads more current of the Schottky-Read-Hall (SRH) recombination. Thus, the leakage current is larger.

The threshold voltage by constant current versus gate length of n-type and p-type devices is presented in Figure 3-10. With the excellent gate control of nanowire structure, the threshold voltage roll-off is not seen, which means the immunity of SCE is good. The shift of the threshold voltage at different drain voltages is observed due to the trapped charges at gate dielectrics. Figure 3-11 illustrates the dual sweep I_D-V_G curve for n-type device. For n-type device, the reverse sweep shifts toward the left, that is, gate dielectrics would trap holes because of gate injection. Figure 3-12 shows the threshold voltage by onset voltage versus gate length of n-type and p-type devices. The onset voltage is defined as the gate voltage that charges start tunneling into channel. The onset voltages at larger drain voltage are higher than ones at lower drain voltage which is different from the trend illustrated in Figure 3-10, because the onset voltage is defined at the lowest drain current that strongly depends on the leakage current. When the drain voltage is larger, the bias of tunnel junction is larger, too, and thus reverse tunneling occurs easier.

Figure 3-13 illustrates the subthreshold swing as a function of the gate length of n-type and p-type devices. Because of the tunneling junction located in the sidewall of nanowires in the

source pad, the subthreshold swing is independent of the gate length.

Figure 3-14 shows the dependence of pairs of nanowires and the drain current for (a) n-type and (b) p-type. With number of nanowires increases, the effective width of channel increases. It is important to note that the SRH recombination current rises, too. As a consequence, the on and off current both increases.

Figure 3-15 illustrates the drain current versus the nanowire diameter for (a) n-type and (b) p-type. The on current is independent of the nanowire diameter because the tunneling junction is mainly at the sidewall of nanowires, and in this case, the oxide thickness of NON stack is all the same even in different diameter conditions.

The mechanism of tunnel FETs is illustrated in Figure 3-16. The first one is band-to-band tunneling, BTBT. The second one is trap assisted tunneling, TAT. The third one is field emission from traps which is also classified as TAT. Electrons from the valence band in the p^+ source region might tunnel through the bandgap into traps and then tunnel or thermally emit out of traps into the conduction band of n^+ region. In order to confirm operation of devices, the I-V measurement was carried out with various temperature and the extracted Arrhenius plot is shown in Figure 3-17. By using values of ln (I_D) at different gate voltage and different temperature, the slope was calculated which is known as the activation energy. The corresponding activation energy as a function of gate voltage is presented in Figure 3-18. At the off state (V_G ~ 0.5 V), the activation energy is about 0.5 eV, around half of the band gap of silicon, which means the SRH recombination dominates [24]. With the increase of the gate voltage, the activation energy decreases and is still larger than 0.1 eV until 3V which means that TAT occurs [25]. Because band-to-band tunneling (BTBT) shows weak dependence on temperature, an activation energy of BTBT should be below 0.1 eV. Therefore, poly-Si nanowire tunnel TFTs are mainly operated by

TAT.

In an effort to reduce traps that would cause TAT, overlap gate devices were done with the NH_3 plasma treatment. The on/off current and S.S. as a function of the plasma treatment time is shown in Figure 3-19 and 3-20. When the plasma treatment time is from 0 min to 3 min, the on/off current and S.S. all reduced due to the elimination of traps which also reduce the both TAT and SRH recombination. However, as the plasma treatment time is up to 5 min, the off current and S.S. all increased because overlong treatment time would lead to damage in devices. The degradation of the off current and S.S. are observed.

3-3 Summary

We demonstrated the poly-Si nanowire tunnel TFTs for the first time. Poly-Si nanowire tunnel TFTs with underlap gate performed high subthreshold swing and low on/off current ratio. Thus, we proposed overlap gate structure, but the characteristics is still poor. By the TCAD simulation of the doping profile, we found that phosphorus would diffuse into nanowires and even p+ pad. The gate could not control the tunneling junction leading to low tunneling efficiency. Thus, the drive current and subthreshold swing are degraded. Temperature-dependent I-V measurements and the extracted activation energy show that the tunneling current is mainly due to trap assisted tunneling rather than band-to-band tunneling, which is also the cause of poor performance. In addition, some overlap gate devices were exposed to NH_3 plasma. Consequently, traps would be eliminated in short plasma treatment time (~ 3 min), but nanowires would be damaged in overlong plasma treatment time (> 5 min) that degrade the performance.

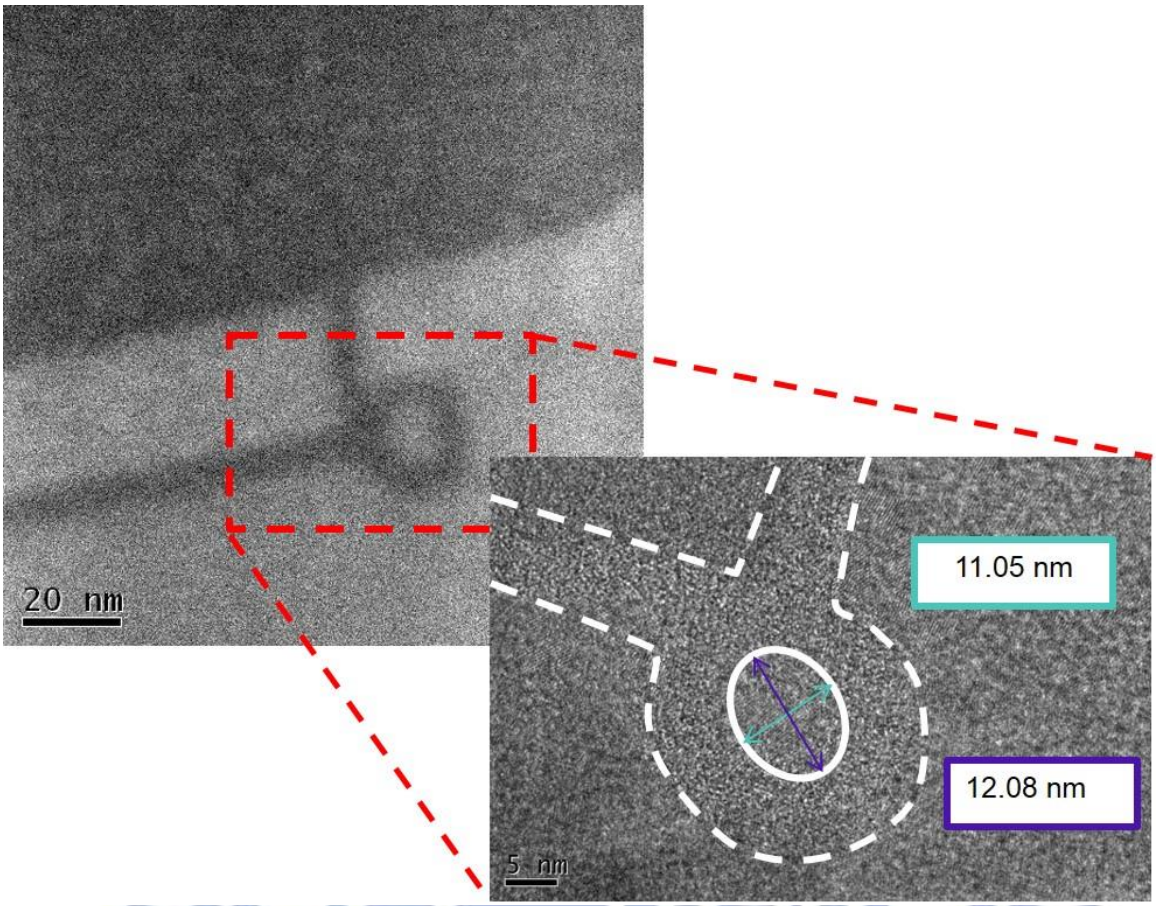


Figure 3-1 Cross-sectional transmission electron microscope (TEM) images of the poly-Si nanowire thin-film TFET

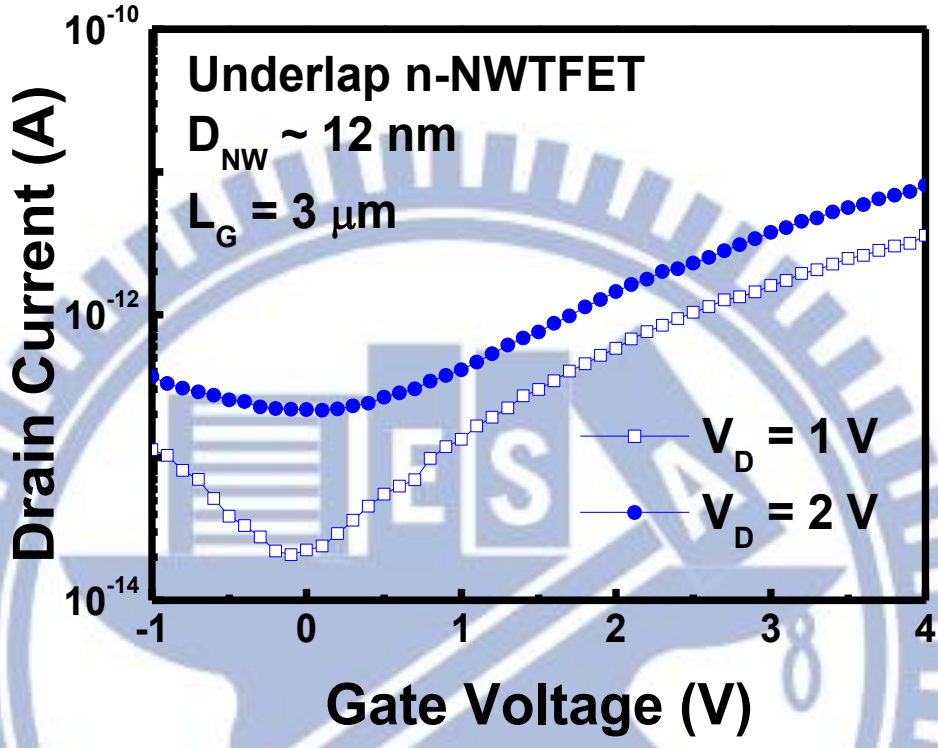
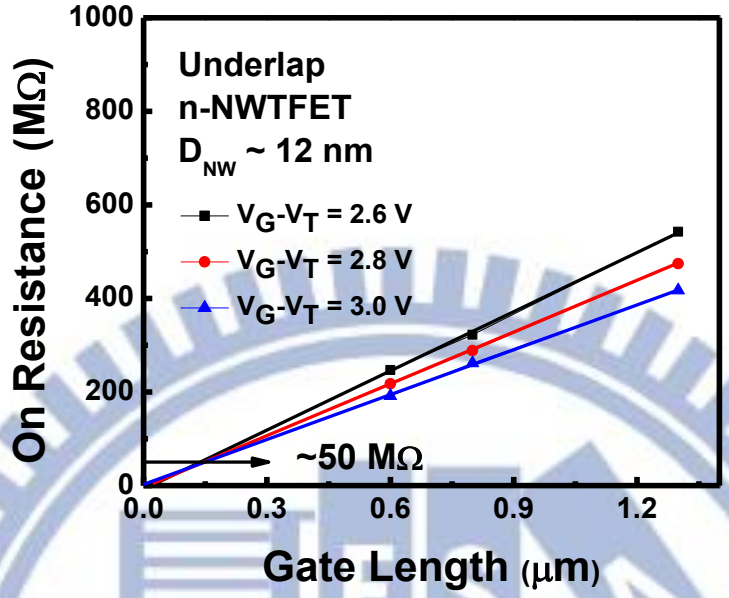
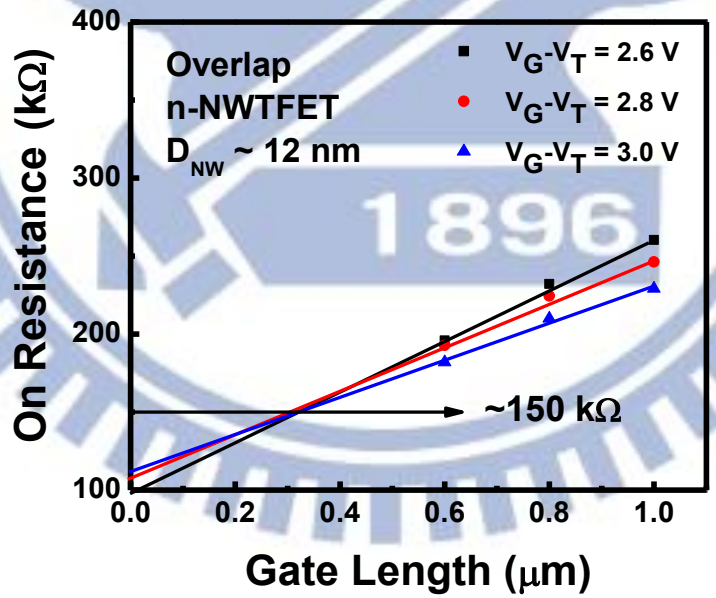


Figure 3-2 The I_D-V_G characteristics of the poly-Si nanowire thin-film TFET with Underlap gate

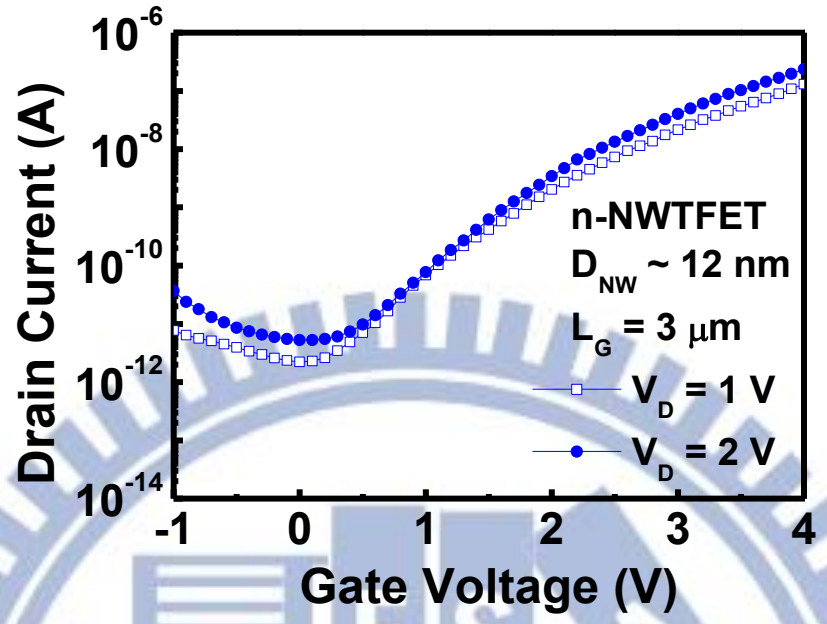


(a)

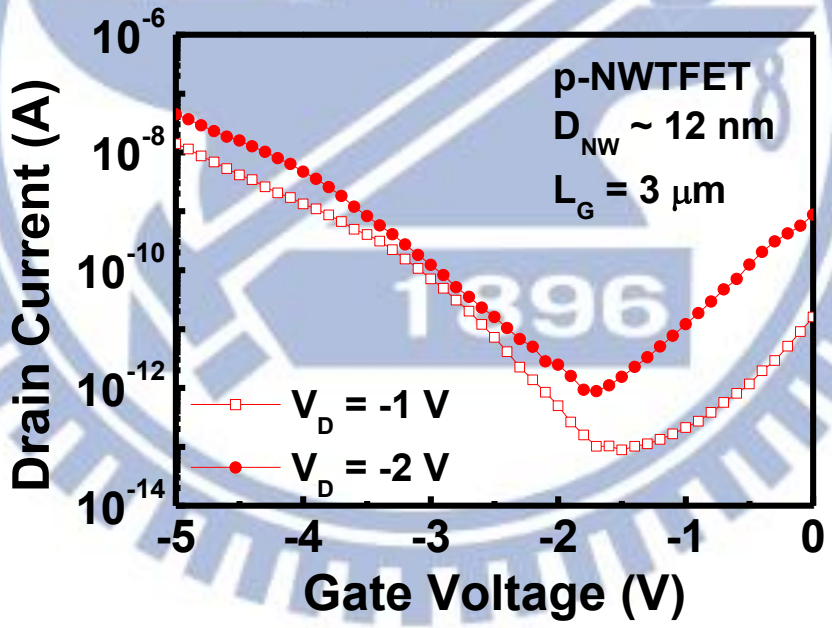


(b)

Figure 3-3 The on resistance of the poly-Si nanowire thin-film TFET (a) with underlap gate (b) overlap gate

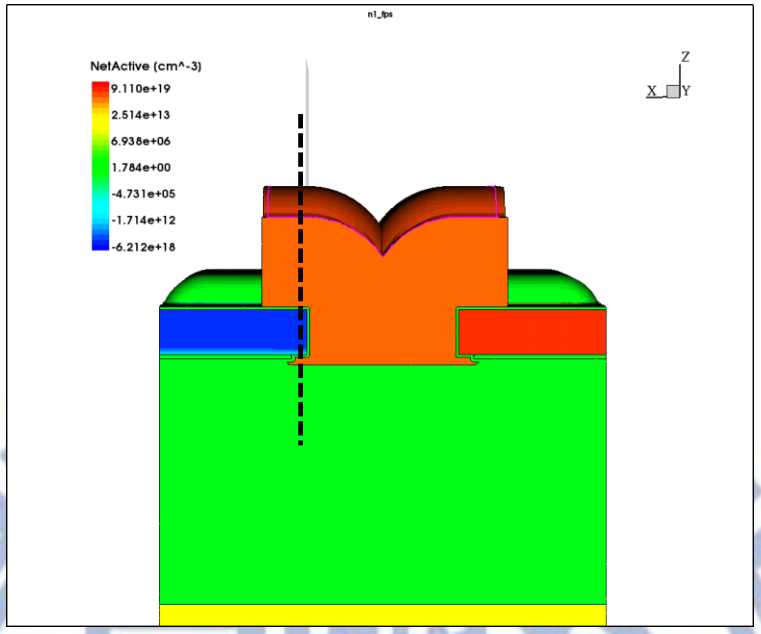


(a)

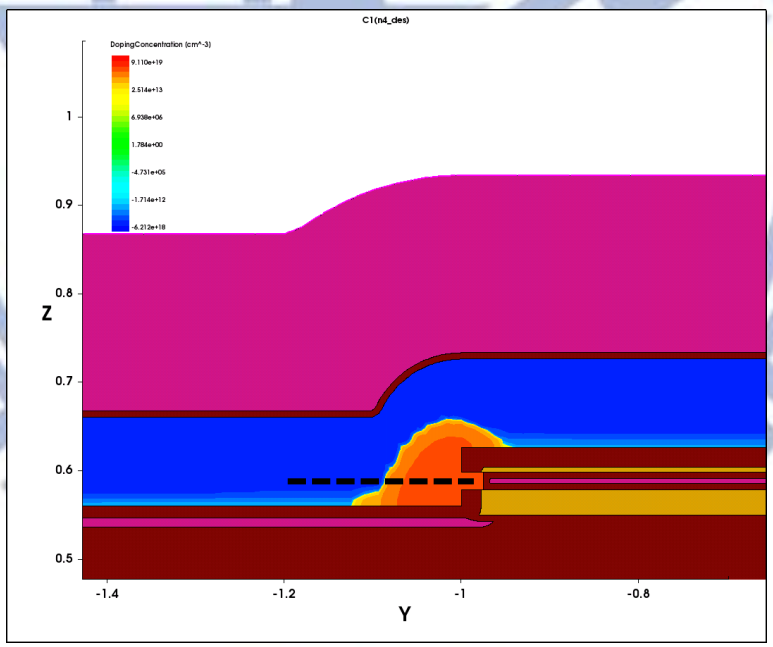


(b)

Figure 3-5 The I_D-V_G characteristics of the poly-Si nanowire tunnel TFT with Overlap gate (a) n-type (b) p-type



(a)



(b)

Figure 3-6 The dopant concentration simulation of a poly-Si nanowire thin-film TFET (a) the cross-sectional image of source-gate-drain (b) the dashed line cross-sectional image of (a)

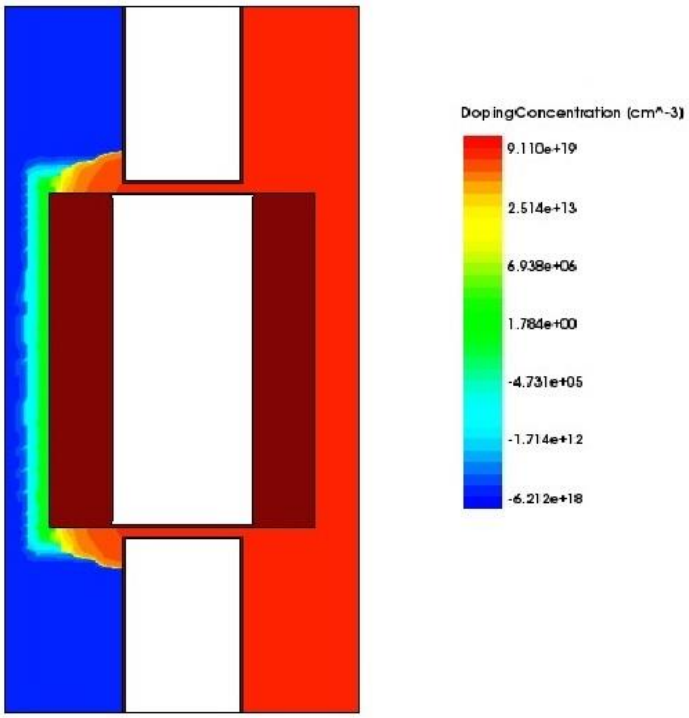


Figure 3-7 The top view of the dopant concentration simulation of a poly-Si nanowire thin-film TFET

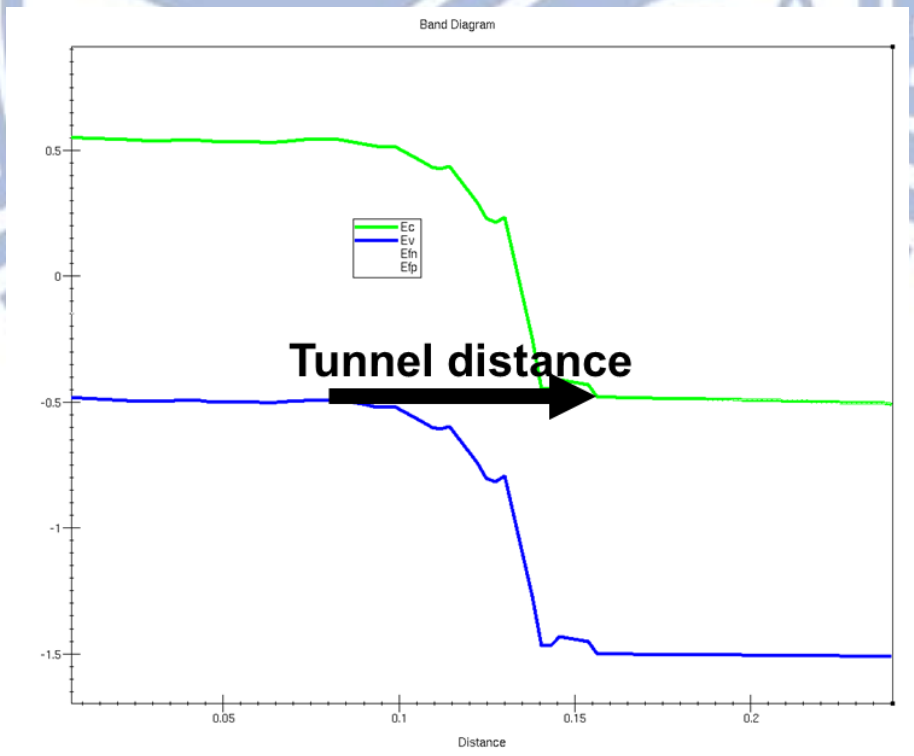
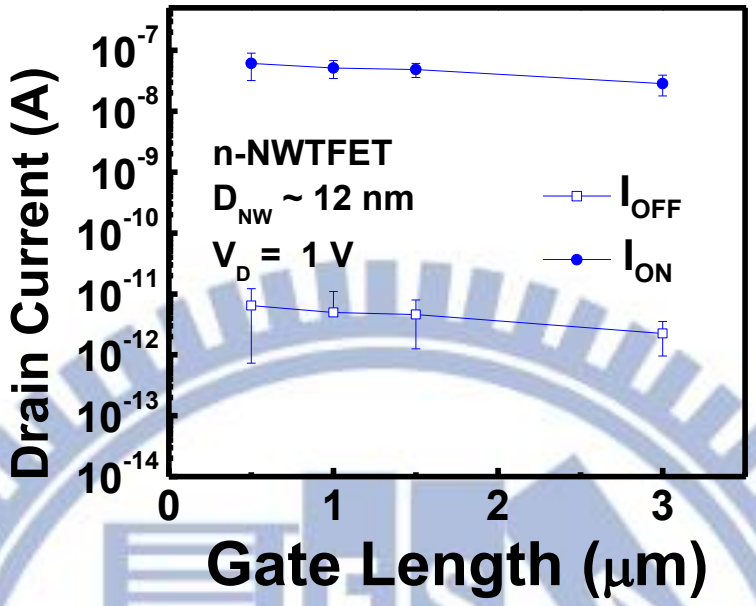
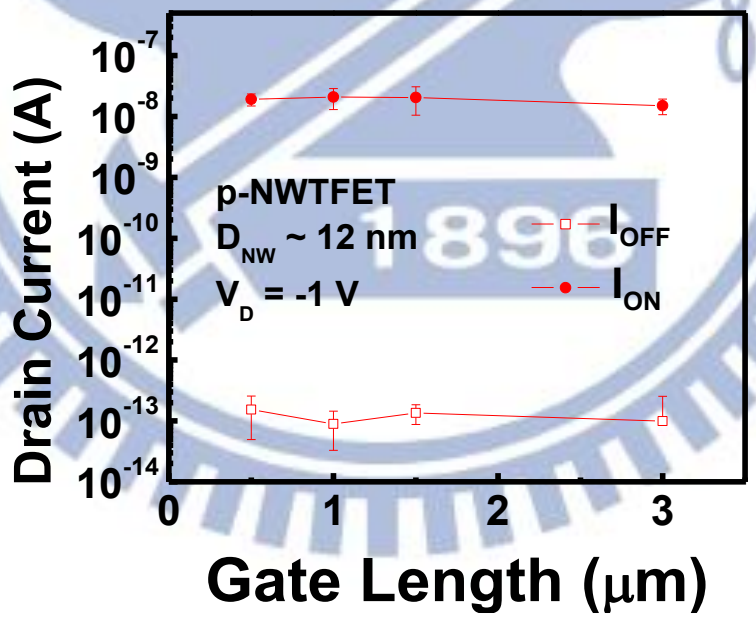


Figure 3-8 The energy band diagram of the dashed line in Figure 3-6(b)

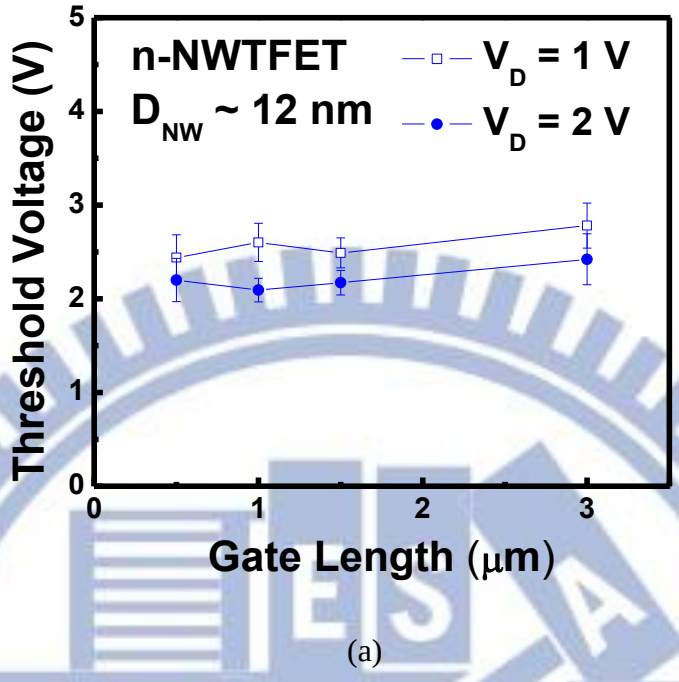


(a)

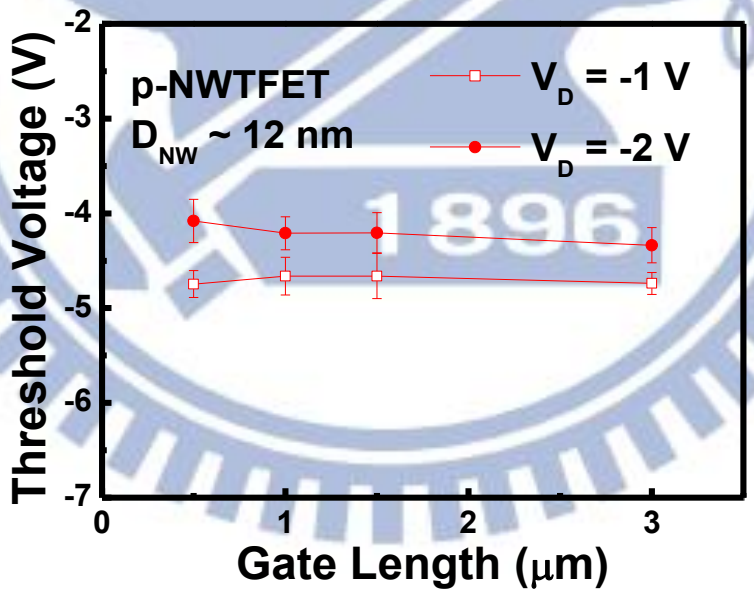


(b)

Figure 3-9 The on/off current as a function of the gate length with D_{NW} ~ 12 nm for poly-Si nanowire tunnel TFTs (a) n-type (b) p-type



(a)



(b)

Figure 3-10 The threshold voltage (constant current) as a function of the gate length for poly-Si nanowire tunnel TFTs with D_{NW} ~ 12 nm (a) n-type (b) p-type

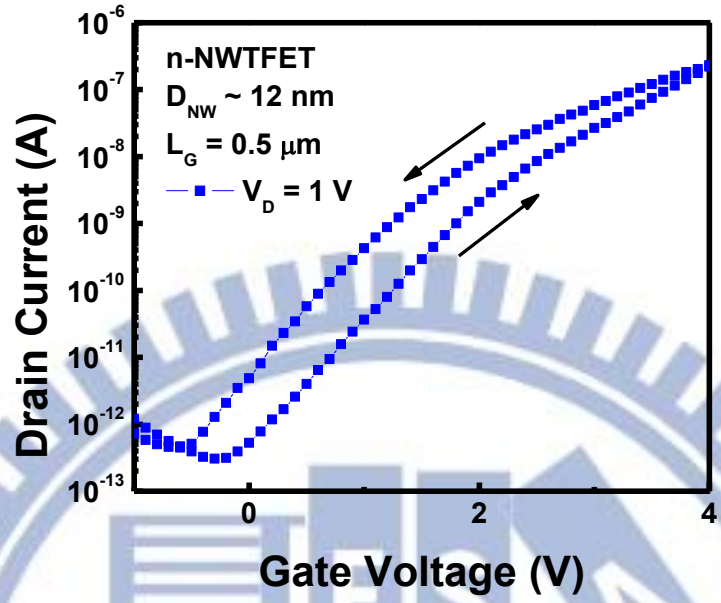
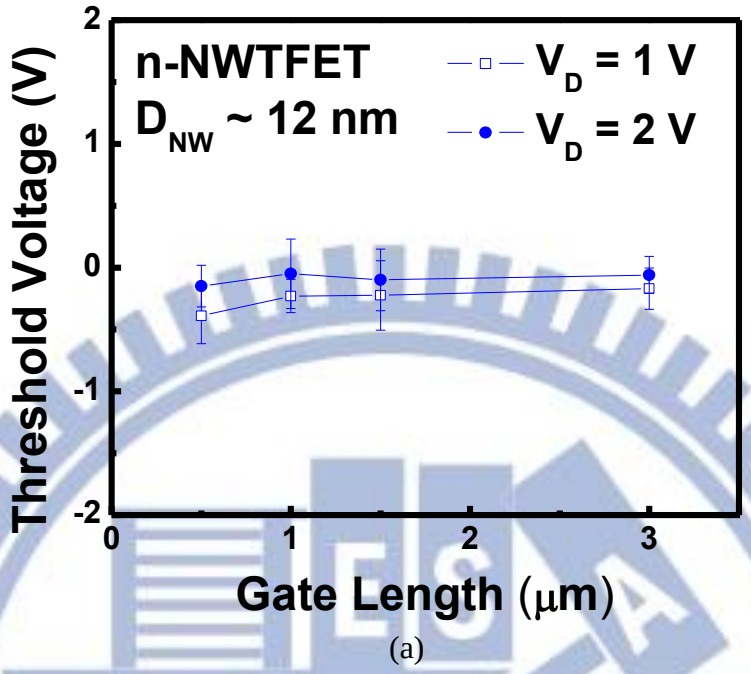
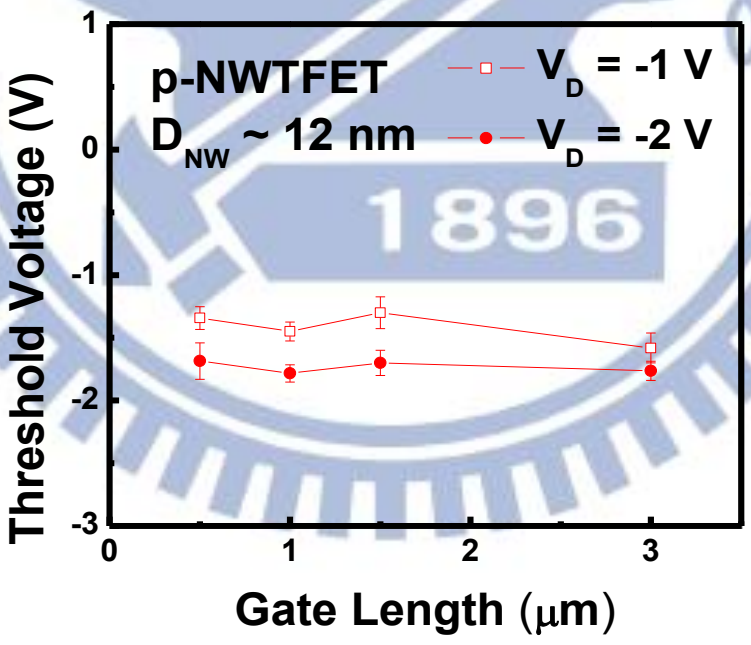


Figure 3-11 The dual sweep I_D-V_G curve of the n-type poly-Si nanowire tunnel TFT with D_{NW} ~ 12 nm and L_G = 0.5 μm at V_D = 1V

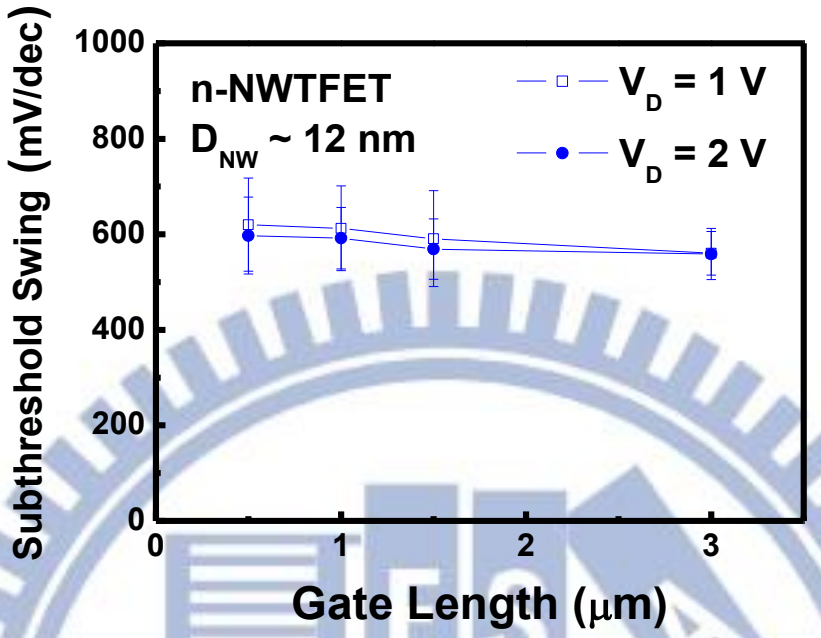


(a)

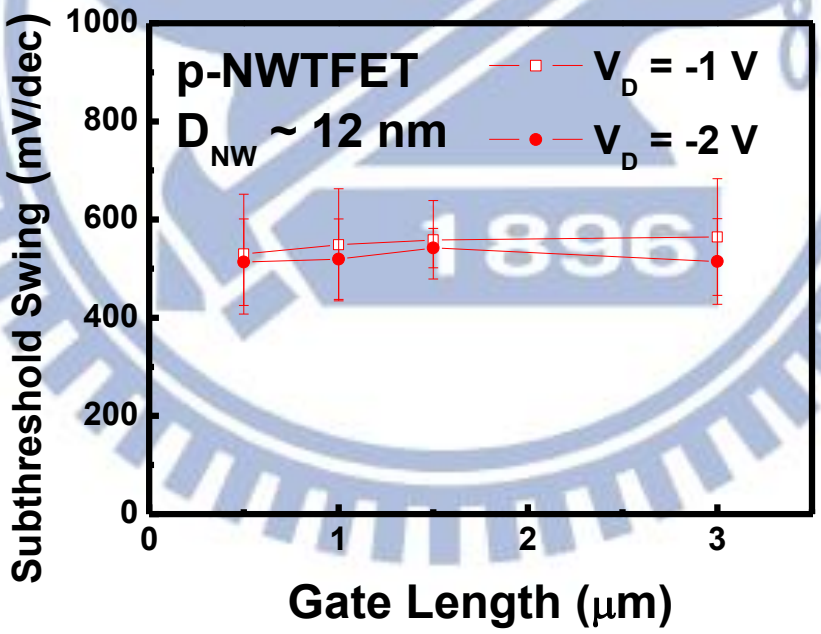


(b)

Figure 3-12 The threshold voltage (onset voltage) as a function of the gate length for poly-Si nanowire tunnel TFTs with D_{NW} ~ 12 nm (a) n-type (b) p-type

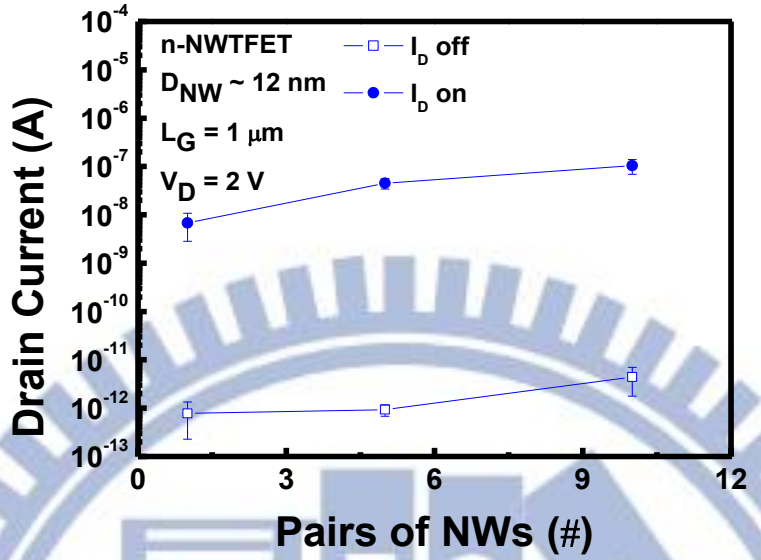


(a)

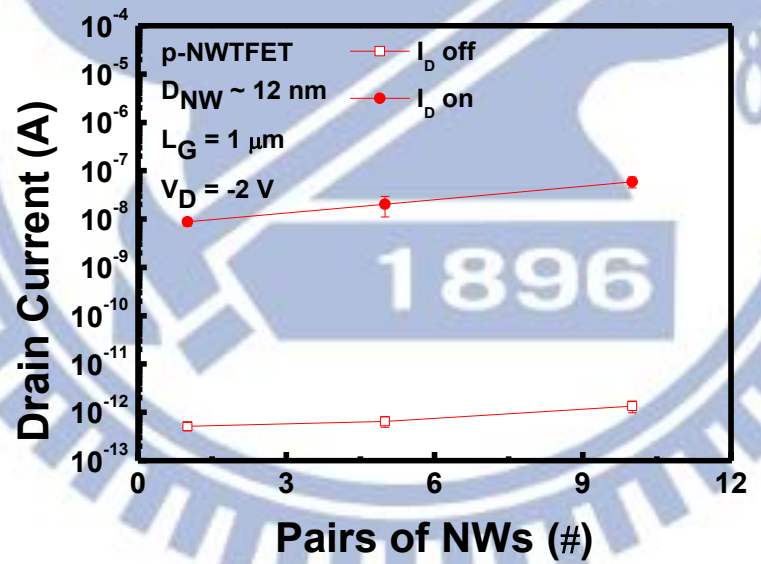


(b)

Figure 3-13 The subthreshold swing as a function of the gate length with D_{NW} ~ 12 nm for poly-Si nanowire tunnel TFTs (a) n-type (b) p-type

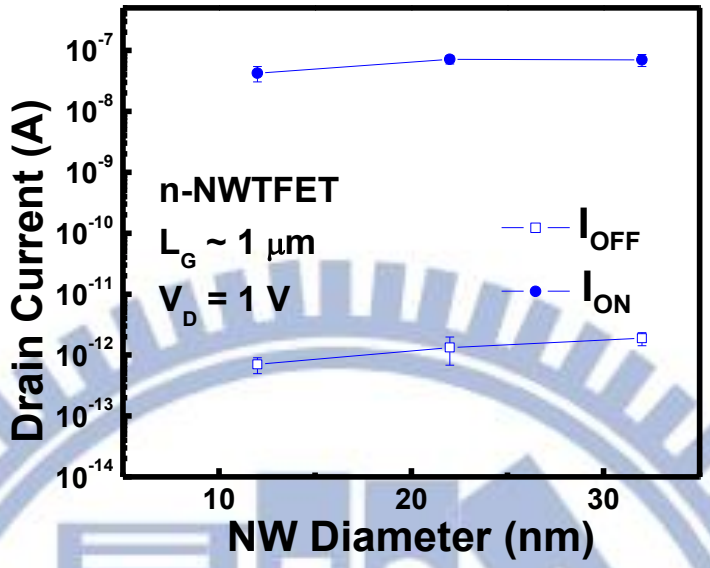


(a)

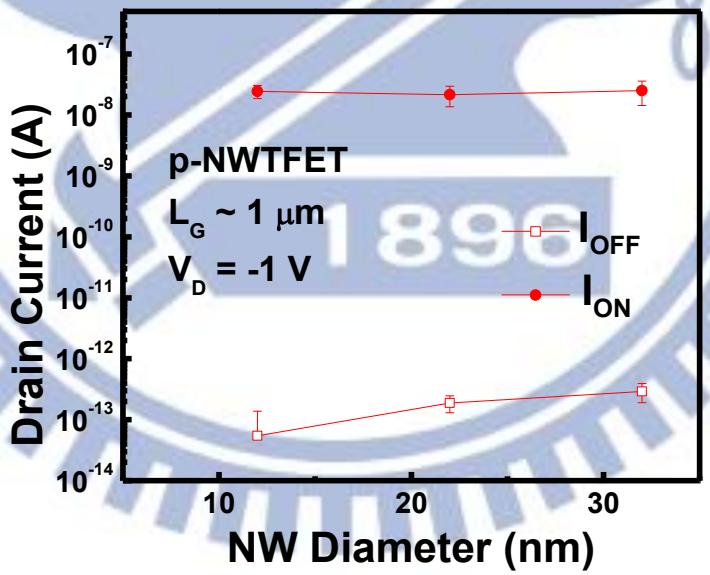


(b)

Figure 3-14 The drain current as a function of the pairs of NWs with D_{NW} ~ 12 nm and L_G = 1 μm for poly-Si nanowire tunnel TFTs (a) n-type (b) p-type



(a)



(b)

Figure 3-15 The drain current as a function of the pairs of NW Diameter with L_G = 1 μm for poly-Si nanowire tunnel TFTs (a) n-type (b) p-type

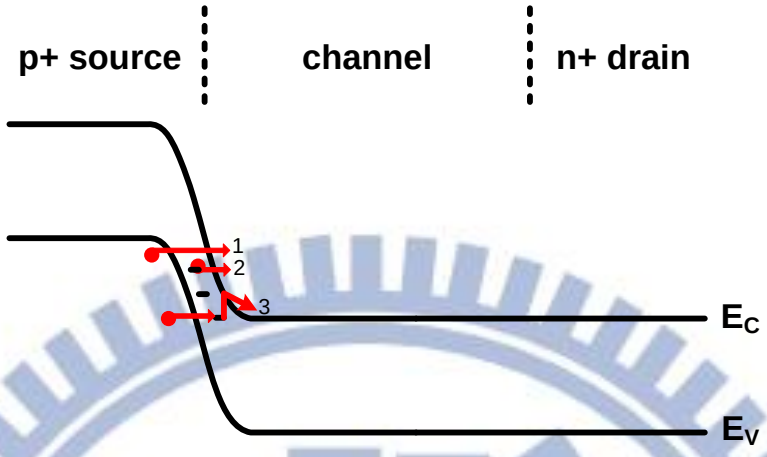


Figure 3-16 The mechanisms of tunneling current: 1: band-to-band tunneling, BTBT 2: trap assisted tunneling, TAT 3: field emission from traps

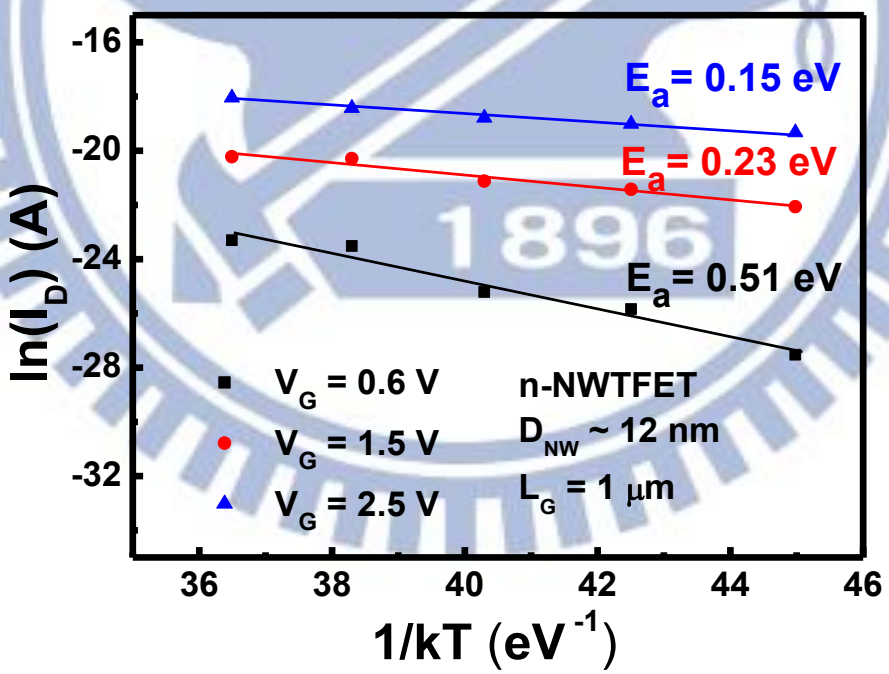


Figure 3-17 The Arrhenius plot at V_G = 0.6 V, 1.5 V and 2.5 V for n-type poly-Si nanowire tunnel TFTs

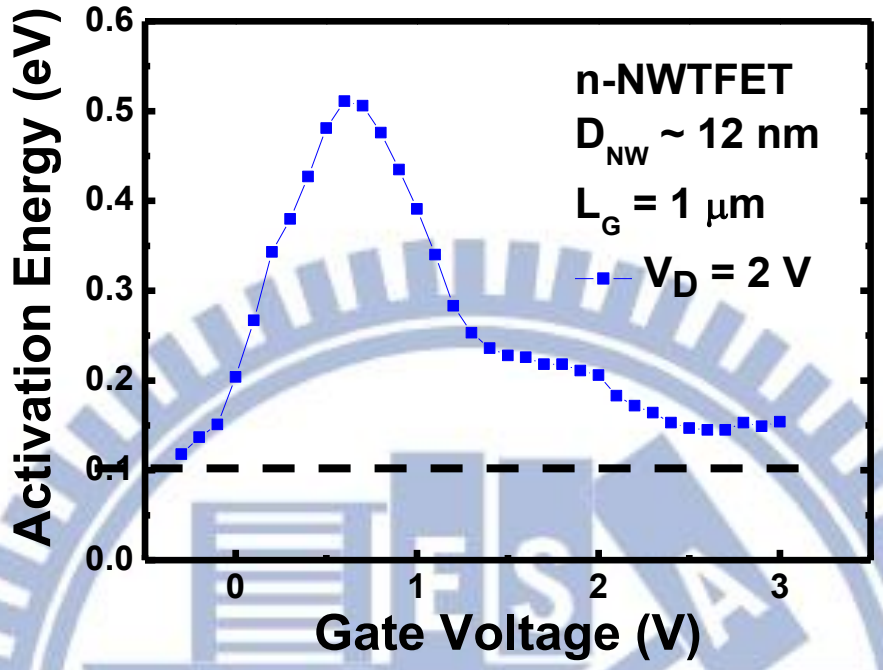


Figure 3-18 The corresponding activation energy versus gate voltage

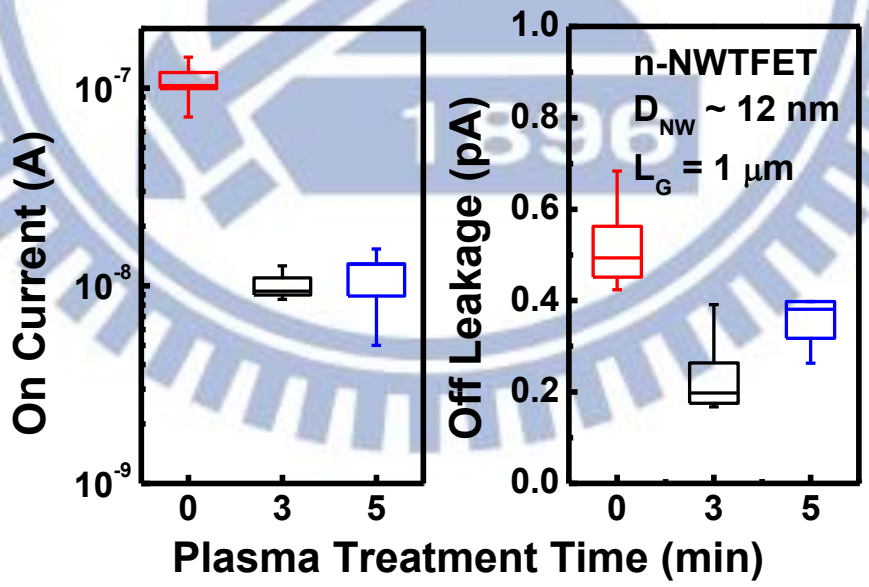


Figure 3-19 The on and off current error bar versus plasma treatment time for poly-Si nanowire tunnel TFTs

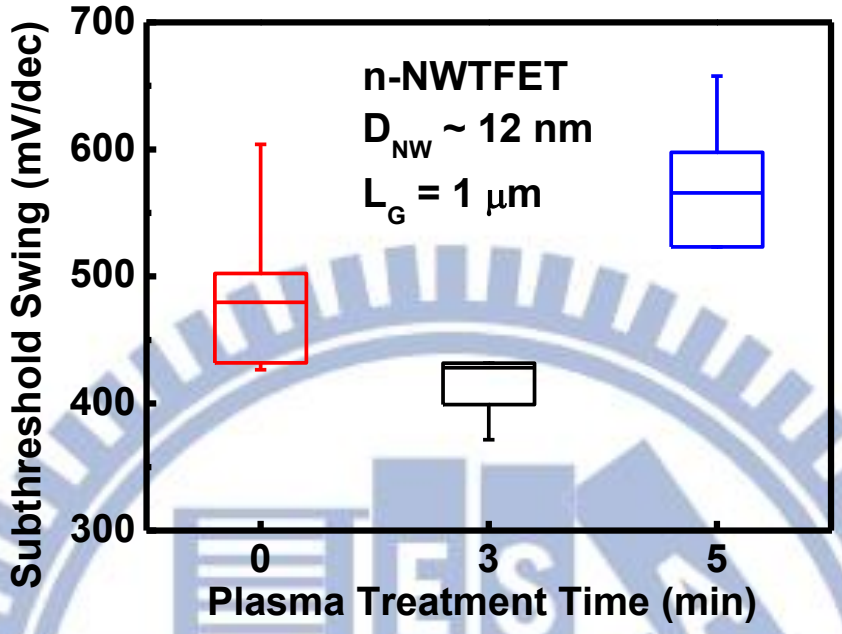


Figure 3-20 The subthreshold swing versus plasma treatment time for poly-Si nanowire tunnel TFTs

Chapter 4

Conclusions and Future Work

4.1 Conclusions

In this study, we demonstrate poly-Si nanowire tunnel TFTs with raised source/drain which was fabricated by dummy NON stack without using advanced lithography tools. Underlap gate devices have bad performance, such as, high subthreshold swing, low on current and low on/off current ratio. Thus, Overlap gate devices were fabricated and exhibit better subthreshold swing and on/off current ratio, but the result are still below our prediction. Even though the immunity of SCE is good which is observed from the invariance of threshold voltage and subthreshold swing with different gate length.

By the TCAD simulation of the doping profile, we found that phosphorus would diffuse into nanowires and even p+ pad. BF_2 didn't distribute well in the raised structure and was even far from nanowires. Poor doping profile and the gate which could not control the tunneling junction lead to large on resistance and tunneling distance which also degrades the behavior of TFETs. Temperature-dependent I-V measurements and the extracted activation energy show that the tunneling current is mainly due to trap assisted tunneling rather than band-to-band tunneling. Finally, some overlap gate devices was exposed to NH_3 plasma to reduce traps. The result show that the plasma treatment in short time (~ 3 min) is good to eliminate traps but the plasma treatment in long time (> 5 min) would damage devices and exhibit worse performance.

4.2 Future Work

In this work, we had clarified the cause of the poor performance for poly-Si nanowire tunnel TFTs with underlap and overlap gate. With different dopant diffusivity, we could not obtain the sharp doping profile which is important for TFETs. In addition, there are grain boundaries in poly-Si that would generate defect and degrade the performance of TFETs.

Future research is obviously required, but this is an exciting step. We still believe that nanowire structure with excellent gate control combined with TFET has large potential in the scaling of CMOS technology. There are many ways to fabricate nanowires in better ways such as sidewall spacer wire [26] and vertical nanowire [27]. Spacer wires should be fabricated with self-aligned implantation that could make the source/drain doped region align with gate edge to obtain the optimistic tunneling junction profile. In order to improve the doping profile, the diffusivity of dopants cannot differ large. Additionally, the plasma treatment is required to eliminate traps.

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