A Scalable Lossy Substrate Model for Nanoscale RF MOSFET Noise Extraction and Simulation Adapted to Various Pad Structures

J. C. Guo and Y. H. Tsai

Dept. of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
Tel: +886-3-5131368, Fax: +886-3-5724361, E-mail: jcguo@mail.nctu.edu.tw

Abstract — **A broadband and scalable lossy substrate model is developed and validated for nanoscale RF MOSFETs of different finger numbers and adopting various pad structures such as lossy, normal, and small pads. The broadband accuracy is justified by good match with S- and Y-parameters up to 40 GHz. The measured noise characteristics in terms of four noise parameters can be accurately simulated up to 18 GHz. The scalable lossy substrate model can consistently predict the abnormally strong finger number dependence and nonlinear frequency response of noise figure (NF_{min}) revealed by the devices with lossy pads. Furthermore, the scalable model can precisely distribute the substrate loss between the transmission line (TML) and pads of various metal topologies and the resulted excess noises. The enhanced model provides useful guideline for appropriate layout of pads and TML to effectively reduce the excess noises. The remarkably suppressed noise figure to ideally intrinsic performance can be approached by the small pad in this paper.**

Index Terms – **RF MOSFET, noise, lossy substrate, pad**

I. Introduction

Compact MOSFET model of broadband accuracy and scalability is recognized as a critical engine to facilitate the success of RF CMOS circuit design. The increasing demand on low power and low noise for wireless communication escalates the importance of noise characterization and modeling. However, a reliable noise de-embedding method to assure accurate extraction of intrinsic noise remains a difficult subject and is particularly challenging for nanoscale devices. A noise correlation matrix method [1] was frequently applied for noise de-embedding but the sophisticated matrices calculation sometimes suffers fluctuation at very low noise level and severe deviation in frequency dependence [2-3]. In our previous work, a lossy substrate model was developed to predict the measured noise and a lossy substrate de-embedding method can be easily performed through circuit simulation for precise extraction of intrinsic noise [4-6]. The accuracy has been proven by sub-100 nm nMOS of various finger numbers and operation under varying frequencies and biases. However, a scalable lossy substrate model is desirable to enable prediction for on-chip devices and circuits of sufficient freedom in TML and pad layouts as well as metal topologies. In this paper, an enhanced lossy substrate model has been developed to realize broadband accuracy and scalability. The enhanced model is composed of two substrate RLC networks in series with C_{pad} and C_{ox} to account for substrate losses through the pads and TML, respectively. The precise distribution of lossy substrate effect between that through the pads and the remaining portion through TML realizes accurate prediction of S-parameters and noise parameters for miniaturized devices over broadband regime. The scalability is justified by the fact that C_{pad} and C_{ox} introduced in the enhanced model consistently follow the scaling factors calculated by process and layout parameters corresponding to various GSG pad schemes such as lossy, normal, and small pads. The broadband and scalable lossy substrate model can be easily deployed in circuit simulators and is useful to improve RF circuit simulation accuracy for low noise design.

II. Device Technology and Characterization

n-MOSFETs of 100nm gate length were fabricated by 130nm 1.2V CMOS technology. Multi-finger structure was employed to reduced gate resistance and the induced excess noise. Various finger numbers of N=18, 36, 72 were designed to investigate the impact on high frequency and noise performance as well as model scalability to fit various device geometries. To study lossy substrate effect on high frequency noise and the excess noises introduced through pad and TML, GSG pads for RF measurement were implemented by Cu/FSG BEOL (Back-End-of-Line) process with 8 layers of Cu and FSG as IMD (Inter-Metal Dielectric). G-pads for grounding were constructed with stacked metal from bottom (M1) to top (M8) while S-pads for signal supply were built with different schemes to explore the impact on excess noise coupling.

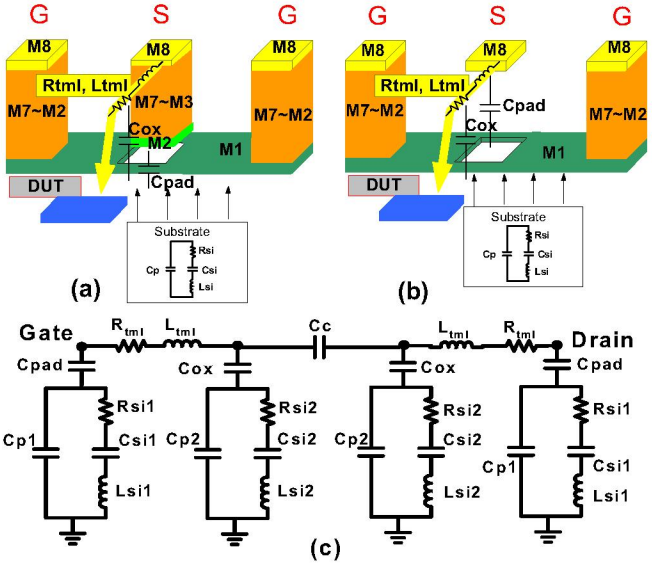
Two port S-parameters were measured by Agilent vector network analyzer up to 40 GHz. Y- and H-parameters can be derived from S-parameters for extraction of gate capacitances (C_{gg}, C_{gd}, C_{gs}) and current gain cut-off

frequency, f_T. Noise parameters (NF_{min}, R_n, Γ_{opt} or Y_{opt}) were measured by ATN-NP5B under V_{gs} at maximum g_m, 0.8V or minimum NF_{min}, 0.5V (not shown for brevity) and sweeping frequency to 18 GHz. Two step de-embedding (open and short) was carried out to extract parallel and series parasitic RLC elements. The incorporation of accurately extracted R and L associated with MOSFET's terminals is crucial to determine the accuracy for high frequency and noise simulation.

III. Scalable Lossy Substrate Model for Various Pad Structures

The original lossy substrate model proved the mechanism of excess noises caused by substrate loss coupled through lossy pads [4-6]. In this paper, an enhanced lossy substrate model is developed to accurately simulate RF noise for on-chip devices of freedom in pad and TML layouts. Three GSG pad structures such as lossy, normal, and small pads with different metal topologies or pad sizes were fabricated by 0.13μm Cu/FSG BEOL process to investigate resulted lossy substrate effect. Fig. 1(a) and (b) illustrate the 3D schematics for lossy and normal pads in which the ground pads (G) were constructed with stacked metal from bottom (M1) to top (M8) while the signal pads (S) were built with two different schemes. For lossy pad scheme in Fig.1(a), the S pads are composed of stacked metal from M2 to M8 whereas for normal pad scheme in Fig.1(b), they are consisted of top metal (M8) only and excluding all lower metals. As for small pad scheme, its signal pads just follow that of normal pad scheme but with smaller size of 50μm× 35μm w.r.t. 50μm×50μm for normal and lossy ones. All three pad structures adopt exactly the same G pad scheme.

Fig.1(c) depicts the equivalent circuit schematics of the enhanced lossy substrate model to incorporate varying pad structures. The primary enhancement to the original model is a modification on the substrate RLC network in conjunction with TML by adopting a C_{ox} representing the TML to substrate coupling capacitance. The resulted enhanced model is composed of two substrate RLC networks in series with C_{pad} and C_{ox} to simulate substrate loss through the pads and TML, respectively. Regarding the lossy substrate model parameters, a complete extraction flow assisted by equivalent circuit analysis can be referred to our original work [4-5]. Note that the initial values of C_{pad} and C_{ox} were calculated based on layout and BEOL process parameters (metal thicknesses, IMD thicknesses and dielectric constants) rather than extraction. The table attached with Fig.1(c) lists full set of model parameters through optimization for lossy, normal, and small pads respectively. The category of lossy pad reveals apparently larger capacitances for all three elements (C_{pad}, C_{p1}, C_{Si1}) in the first RLC network under pad and C_{Si2} in the second RLC network under TML. C_{ox} is kept at similar value for all three kinds of pad due to the same metal layout and topology for TML from the pads to intrinsic device. On the other hand, C_{pad} presents significant difference among the three pad structures in which the scaling factors of around 3.9~4.0 for lossy versus normal and 0.82~0.85 for small versus normal just approach the theoretical values of 4.04 and 0.75 calculated by layout and process parameters.



Gate Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	**77.87**	**74.97**	**200**	**170.7**	**159.9**	50	0.2
Normal	20	28.55	32.68	425.3	511.7		
Small	13.89	24.43	33.4	425.3	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)	C_c (fF)	
Lossy	10.78	1.629	**45.98**	**515.4**	**328.8**	1.103	
Normal	9.932	2.553	9.316	874.3	638.3		
Small	9.913	2.635	8.741	874.3	638.3		

Drain Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	**80.99**	**62**	**200**	**83.72**	**164.3**	50	0.2
Normal	20.17	24.05	30	671.3	511.7		
Small	12.84	19.72	30	671.3	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)		
Lossy	11.07	2	**54.15**	**590.6**	**270.9**		
Normal	10.21	2.887	11.73	1059	540.3		
Small	9.932	2.635	10.29	1059	540.3		

Fig.1 3D schematics of GSG pads (a) lossy pad scheme : S-pads of stacked metals from M2 to M8 (b) normal pad : S pads of top metal (M8) only (c) The equivalent circuit schematics of enhanced lossy substrate model applicable to lossy, normal, and small pad schemes. All RLC model parameters are listed in the attached table.

The accuracy of optimized lossy substrate model was verified and justified by good match with measured S_{11} and S_{22} (mag. and phase) for lossy, normal, and small pads together in Fig. 2. Good prediction was achieved for Y-parameters simultaneously (not shown for brevity). Interestingly, the lossy pad reveals remarkably smaller magnitudes and more negative phase for both S_{11} and S_{22}, i.e. extraordinary shift in magnitude and phase away from 1.0 and 0° under increasing frequency. The difference between normal and small pads is much smaller. As a result, the enhanced lossy substrate model can accurately simulate the pad structure effects in terms of layout and metal topologies with predictable scaling factors.

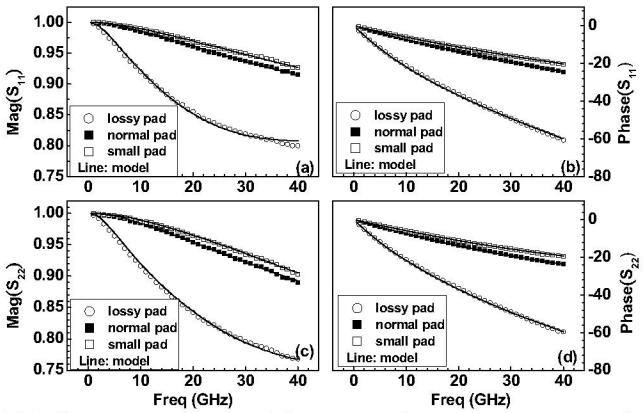


Fig.2 Comparison of open pad S-parameters between measurement and lossy substrate model for three pad schemes, lossy, normal, and small (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase (S_{22})

IV. Lossy Substrate Model to Predict Pad Structure Effect on RF Noise– Broadband Accuracy & Scalability

The enhanced lossy substrate model was further verified by integration with the intrinsic devices for full circuit simulation to identify the impact on high frequency and noise characteristics. The particularly interesting and useful application is an accurate and simple noise extraction method to ensure noise simulation accuracy for nanoscale devices. Firstly, extensive calibration was done on the intrinsic device's I-V and C-V models (BSIM3). Afterward, 4 terminal parasitic R and L (R_g, R_s, R_d, R_b, L_g, L_s, L_d) were correctly extracted and deployed in Intrinsic MOSFET. Consequently, good match in terms of g_m, C_{gg}, C_{gd} (Y-parameters), and f_T (H-parameters) over wide range of biases or currents was realized for 100 nm nMOS of various finger numbers (N=18, 36, 72). The full circuit model accuracy can then be verified in terms S-parameters and noise parameters. Note that short channel effects have been adequately implemented in the model to yield accurate noise simulation for nanoscale MOSFETs [4].

Figs. 3 exhibit good match in S_{11} (magnitude and phase) between model and measurement for full circuits adopting various pad schemes and intrinsic ones after pad de-embedding. The phase sign change from negative to positive revealed by full circuits of larger devices (N=36,72) in Figs.3(a)-(c) at sufficiently high frequency accounts for the parasitic inductance effect. This effect can be eliminated for intrinsic devices in Fig.3(d) subject to pad and lossy substrate de-embedding. Besides S_{11}, good agreement is simultaneously realized for S_{22}, S_{12}, and S_{21} and Y-parameters (not shown).

Fig. 4(a)-(c) indicate the simulated extrinsic NF_{min} and good agreement with measurement for full circuits adopting various pad schemes such as lossy, normal, and small pads respectively. Very interestingly, the devices adopting lossy pads reveal abnormally large finger number dependence and nonlinear frequency response (Fig. 4(a)) while the finger number dependence is much relieved and frequency dependence is recovered to be linear for normal and small pads. (Fig.4(b),(c)). The larger NF_{min} revealed by the smaller finger number (N) in the category of lossy pads suggests the amplification effect through larger noise resistance R_n for smaller N. The extrinsic NF_{min} is effectively reduced for devices using normal or small pads and the enhanced lossy substrate model can accurately predict the measured features. The intrinsic NF_{min} simulated by the calibrated model as shown in Fig.4(d) presents near constant free from finger number dependence over wide range of frequency up to 18 GHz. The intrinsic NF_{min} at V_{gs}=0.8V corresponding to maximum g_m is as low as 0.75 dB at 10 GHz and can be further suppressed to around 0.55 dB under V_{gs}=0.5V corresponding to minimum NF_{min} (not shown).

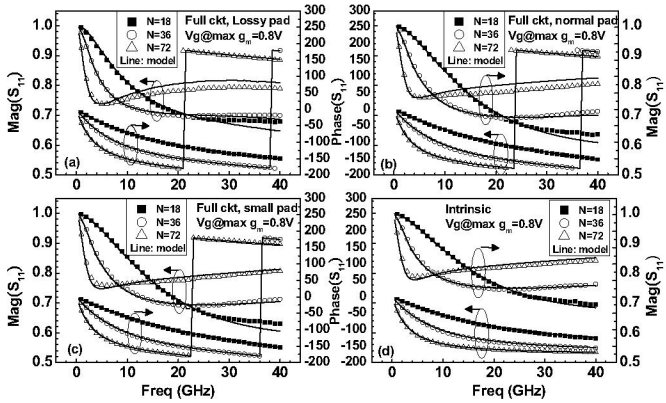


Fig.3 Comparison of measured and simulated S_{11}(mag., phase) by full circuit model for 100nm nMOS (N=18, 36, 72) adopting 3 different pads, (a) lossy pad (b) normal pad (c) small pad (d) intrinsic S_{11} by pad or lossy substrate de-embedding

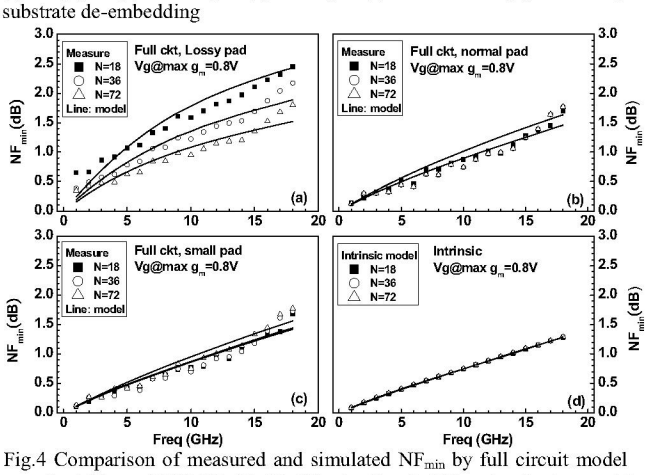


Fig.4 Comparison of measured and simulated NF_{min} by full circuit model for 100nm nMOS (N=18, 36, 72) adopting 3 different pad schemes (a) lossy pad (b) normal pad (c) small pad (d) intrinsic NF_{min} by lossy substrate de-embedding

Pad structure effect on four noise parameters NF_{min}, R_n, $Re(Y_{opt})$ and $Im(Y_{opt})$ are illustrated in Figs. 5 for N=18 and 72 to investigate finger number dependence of excess

noises coupled through different pads. The smallest device (N=18) in Fig.5(a)-(d) reveals the largest sensitivity to pad structures with substantial increase in NF_{min}, $Re(Y_{opt})$ and $Im(Y_{opt})$ for lossy pad. The sensitivity is obviously suppressed by increasing finger numbers. The increase of mentioned noise parameters becomes much smaller for N=72 in Fig.5(e)-(h). Note that R_n is effectively reduced by increasing N attributed to smaller R_g and larger g_m but keeps nearly constant for different pads. The scalability and broadband accuracy of the lossy substrate model is proven by good agreement with measured noise parameters corresponding to various pads as well as finger numbers and over wide range of frequencies to 18 GHz. The intrinsic noise parameters extracted through lossy substrate de-embedding indicates effective reduction and recovery to linear frequency dependence in NF_{min}, $Re(Y_{opt})$ and $Im(Y_{opt})$. NF_{min} of small pads are effectively suppressed to approach the intrinsic values.

As a result, the enhanced lossy substrate model of two RLC networks introduced via pad and TML justify themselves scalable through the physical parameters C_{pad} and C_{ox} , which consistently follow the pad and TML layout as well as metal topology parameters. The extreme conditions of fully open or fully short along pad and TML can be simulated by the scalable model to explore the optimized layout to approach the intrinsic noise characteristics. The simulation subject to extreme conditions suggests that elimination of C_{pad}, i.e. fully open along pad can minimize substrate loss induced excess noise and attain the intrinsic characteristics. On the other hand, elimination of C_{ox}, i.e. full isolation along TML makes minor contribution provided that C_{pad} stays not reduced. The proven scalable model is useful to guide pad and TML layout to minimize noise for miniaturized devices.

V. Conclusion

A broadband and scalable lossy substrate model has been developed and validated by 100 nm RF MOSFET of various finger numbers and adopting different GSG pads. The broadband accuracy is justified by good match with measured S-parameters to 40 GHz as well as noise parameters to 18 GHz. The scalability is proven by accurate prediction for various finger numbers in conjunction with lossy, normal, and lossy pads. The enhanced model can be easily deployed in circuit simulator and is useful to improve RF circuit simulation accuracy for low noise design.

Acknowledgement

This work is supported in part by National Science Council under Grant No. 95-2221-E009-289. Besides, the authors would like to acknowledge the support from NDL RF Lab. and CiC for RF measurement and simulation.

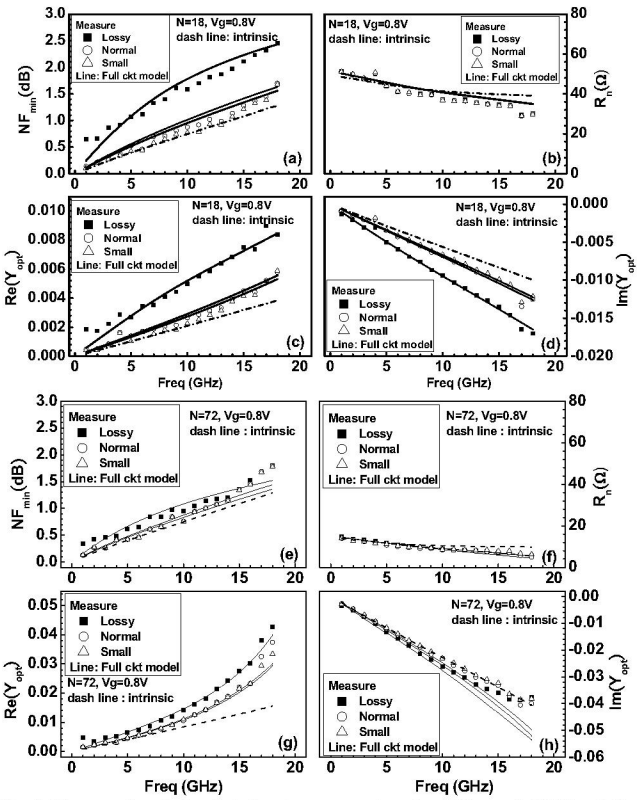


Fig.5 Measured and simulated noise parameters for 100nm nMOS by full circuit model of lossy, normal, small pads and comparison with intrinsic ones after lossy substrate de-embedding, N=18 (a)NF_{min} (b)R_n (c) $Re(Y_{opt})$ (d) $Im(Y_{opt})$, N=72 (e) NF_{min} (f)R_n (g) $Re(Y_{opt})$ (h) $Im(Y_{opt})$

References

[1] H. Hillbrand et al.,"An Efficient Method for Compact Aided Noise Analysis of Linear Amplifier Networks," IEEE T-CAS 23,pp.235-238, 1976

[2] C.E. Bilber, et al., "Technology independent degradation of minimum noise figure due to pad parasitics," *in 1998 IEEE MTT-S Proc.*, Vol. 1, pp.145-148

[3] C. H. Chen, et al., "A general Noise and S-parameter deembedding procedure for on-wafer high-frequency noise measurements of MOSFETs," *IEEE T-MTT*, vol. 49, pp. 1004-1005, May 2001.

[4] Jyh-Chyurn Guo, et al., "A New Lossy Substrate Model for Accurate RF CMOS Noise Extraction and Simulation with Frequency and Bias Dependence," IEEE T-MTT, vol.54, pp.3975-3985 Nov. 2006

[5] Jyh-Chyurn Guo, et al., "A Lossy Substrate De-embedding Method for Sub-100nm RF CMOS Noise Extraction and Modeling," IEEE T-ED, vol. 53, pp.339-347, Feb. 2006

[6] J. C. Guo, et al., "65-nm 160-GHz f_T RF n-MOSFET Intrinsic Noise Extraction and Modeling using Lossy Substrate De-embedding Method," in 2006 RFIC Tech. Digest, pp.349-352