Poly-Si Thin-Film Transistor Nonvolatile Memory Using Ge Nanocrystals as a Charge Trapping Layer Deposited by the Low-Pressure Chemical Vapor Deposition

Po-Yi Kuo, Tien-Sheng Chao, *Senior Member, IEEE*, Jyun-Siang Huang, and Tan-Fu Lei

***Abstract*—We have successfully developed and fabricated a poly-Si thin-film transistor (poly-Si TFT) nonvolatile memory using Ge nanocrystals (Ge-NCs) as a charge trapping layer. Process compatibility and memory operation of the device were investigated. The Ge-NC trapping layer was directly deposited by low-pressure chemical vapor deposition at 370 °C. Results show that the new poly-Si TFT nonvolatile Ge-NC memory has good programming/erasing efficiency, long charge retention time, and good endurance characteristics. These results show that poly-Si TFT nonvolatile Ge-NC memory is the promising nonvolatile memory candidate for system-on-panel application in the future.**

***Index Terms*—Charge retention, endurance, Ge nanocrystals (Ge-NCs), nonvolatile memory, polycrystalline silicon thin-film transistors (poly-Si TFTs), programming/erasing.**

I. INTRODUCTION

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) are very attractive for system on panel (SOP) as device performance improves further [1]. The entire system will include memories, solar cells, and touch sensors as well as driver circuits for active-matrix liquid crystal displays [2]–[4].

Nanocrystal (NC) floating-gate (FG) memories offer a number of potential advantages over FG Flash devices, including improved scalability, retention, and cyclability, as well as lower voltage operation [5]. Recently, nonvolatile memory devices using Ge or Si NCs (Ge-NCs or Si-NCs) as FG have been widely studied because of its excellent memory performance and high scalability. Ge has smaller bandgap and similar electron affinity compared with Si. Nonvolatile memory devices using Ge-NCs instead of Si-NCs have superior retention properties [6]–[11]. Most of the Ge-NC fabrication methods, including the thermal annealing of Ge and dielectric mixture, the oxidation of SiGe, and Ge ion implantation, all require annealing at high temperature [6], [9], [11]. In this letter, a poly-Si TFT nonvolatile memory using Ge-NCs as a charge trapping layer (poly-Si TFT nonvolatile Ge-NC memory) was proposed. The Ge-NCs embedded in oxide were directly deposited by low-pressure chemical vapor deposition (LPCVD) at 370 °C, and therefore, it was easy to control the real thickness of tunneling oxide. The size of Ge-NCs can be easily modified by changing the deposition time and flow rate of GeH_4 [10].

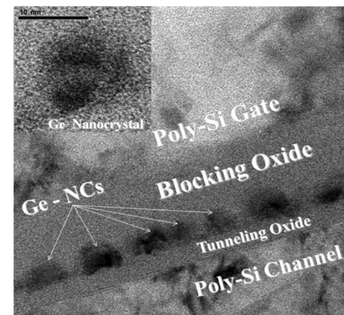

Fig. 1. Cross-sectional TEM microphotographs of poly-Si TFT nonvolatile Ge-NC memory. The blocking oxide and tunneling oxide thicknesses are about 40 and 10 nm, respectively. The sizes of the Ge-NCs are about 9–11 nm, and the density of the Ge-NCs is about $2-4 \times 10^{11}$ cm^{-2}.

II. EXPERIMENT

Fig. 1 shows the cross-sectional transmission electron microscope (TEM) microphotographs of poly-Si TFT nonvolatile Ge-NC memory. First, a 100-nm amorphous silicon (a-Si) active region layer was deposited by LPCVD at 550 °C on wet oxide and then was crystallized by solid phase crystallization at 600 °C for 24 h. After the active region patterning, a 10-nm tetraethoxysilane (TEOS) tunneling oxide layer was deposited by LPCVD. After deposition of a-Si nuclei, the Ge-NCs were directly deposited by LPCVD at 370 °C. The a-Si nuclei were deposited by using SiH_4 as a gaseous precursor at 550 °C on tunneling SiO_2 surface. This way, we were able to adjust the a-Si nuclei density, and hence, the density of the Ge-NCs can be between 10^9 cm^{-2} and slightly less than 10^{12} cm^{-2}. Once the a-Si nuclei were deposited, we stopped the SiH_4 gas

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flow. After cooling down CVD chamber temperature to 370 °C, GeH_4 was introduced to selectively grow Ge-NCs on the a-Si nuclei. This way, the a-Si nuclei were not oxidized because they were never exposed to oxygen. Indeed, no Ge-NCs would grow on oxidized a-Si nuclei [10]. The size of Ge-NCs can be easily controlled by changing the deposition time and flow rate of GeH_4. The low deposition temperature of Ge-NCs is suitable for low-temperature poly-Si TFT applications. A high-resolution image of one typical Ge-NC is shown in Fig. 1 for revealing the geometrical and crystal characteristics of the Ge-NC. In NC nonvolatile memories, the size of NC is an important factor that affects electrical characteristics. The size of Ge-NC embedded in oxide should not be scaled below 5 nm, because the quantum confinement effect becomes very significant for such small Ge-NC [12], [13]. Large quantum confinement leads to the conduction band in the NC being much higher than that of the Si substrate, resulting in enhanced leakage from NC and shorter retention time [6].

Next, a 40-nm TEOS blocking oxide layer and a 200-nm a-Si gate layer were deposited in sequence. After gate implantation and defining gate electrode, a self-aligned implantation was used to form the n^+ S/D. After passivation process, dopants were activated by furnace at 600 °C for 12 h. After contact and metallization processes, NH_3 plasma treatments were implemented after sintering at 400 °C for 30 min.

III. Results and Discussion

Fig. 2 shows the measured (a) programming and (b) erasing characteristics of poly-Si TFT nonvolatile Ge-NC memory with $W/L = 0.8$ μm/0.8 μm. We employ channel hot electron injection to program and also band-to-band tunneling induced hot-hole injection (BTBHHI) to erase. The program conditions are as follows: $V_G = 12$ V and $V_D = 9$, 10 V. The erase conditions are as follows: $V_G = -10$ V and $V_D = 9$, 10 V. We can read the threshold voltage (V_{TH}) shift ($= V_{\mathrm{TH}}$ of program state–V_{TH} of erase state) from Fig. 2. We think that V_{TH} shift is due to the electron trapping in the Ge-NC trapping layer. With increasing the V_D, the V_{TH} shift also increases and the programming/erasing speeds become faster. In the floating-body poly-Si TFTs, we apply appropriate drain voltages before strong drain avalanche. These drain voltages are used to achieve good channel hot electron injection efficiency in the programming and good BTBHHI efficiency in the erasing. The applied drain voltage can be reduced with decreasing gate length [14], [15].

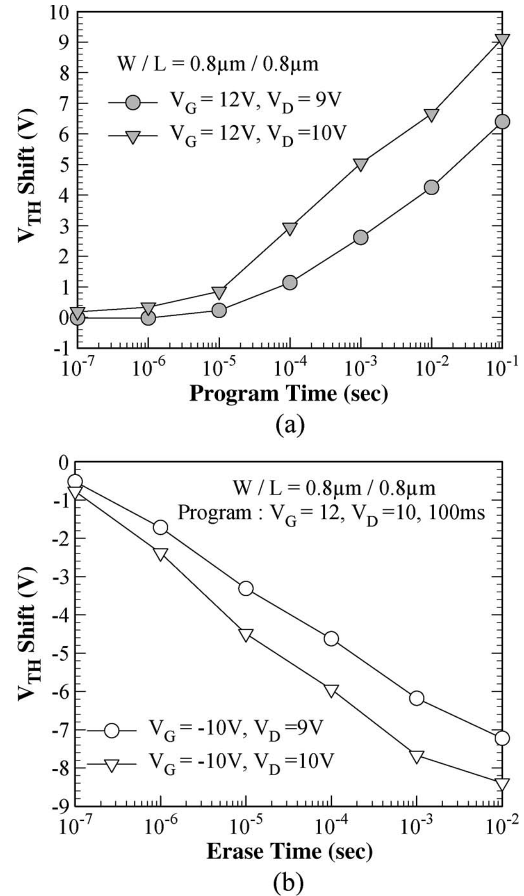

Fig. 2. Measured (a) programming and (b) erasing characteristics of poly-Si TFT nonvolatile Ge-NC memory with $W/L = 0.8$ μm/0.8 μm.

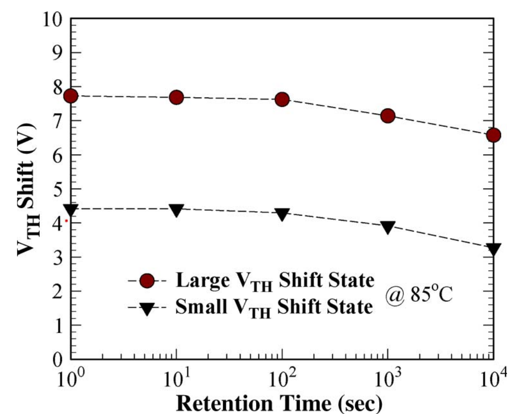

Fig. 3. Measured retention characteristics at 85 °C. The poly-Si TFT nonvolatile Ge-NC memory was programmed to two V_{TH} shift states at 0 s.

Fig. 3 shows the measured retention characteristics at 85 °C. The poly-Si TFT nonvolatile Ge-NC memory exhibits good retention characteristics at high temperature due to the sufficiently deep trapping level of Ge-NCs. Compared with Si, Ge has a narrower bandgap and a similar electron affinity. Nonvolatile memory devices using Ge-NCs instead of Si-NCs have superior retention properties. Here, we display real V_{TH} shift instead of normalized V_{TH} shift. The normalized V_{TH} shift will change with different V_{TH} shift at 0 s. For example, the normalized V_{TH} shift of large V_{TH} shift state ($\sim$7.8 V) at 0 s is about 15%, but the normalized V_{TH} shift of small V_{TH} shift state ($\sim$4.4 V) at 0 s is about 25%.

The measured endurance characteristics are shown in Fig. 4. We find that the memory window narrowing rate slightly increases after 2×10^3 P/E cycles for the memory with 10-nm tunneling oxide. It may be due to the stress-induced electron traps generated in the tunneling oxide during P/E cycles. Thick tunnel oxide has more serious memory window closure. Thus, the tradeoff between retention and endurance characteristics shall be carefully conducted [16]. We believe that retention and endurance characteristics can be significantly improved

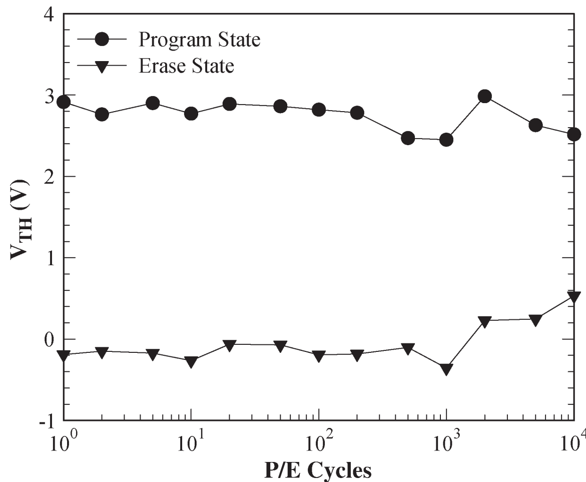

Fig. 4. Measured endurance characteristics. The memory window narrows to about 2.1 V after 10^4 P/E cycles.

by using high-quality tunneling oxide and blocking oxide. Furthermore, it is important to effectively reduce the amount of grain boundaries in the channel for achieving high-performance poly-Si TFT nonvolatile memory.

IV. Conclusion

In this letter, poly-Si TFT nonvolatile Ge-NC memory has been reported and demonstrated. The Ge-NCs embedded in oxide were directly deposited by LPCVD at 370 °C, and therefore, it was easy to control the real thickness of tunneling oxide. The low deposition temperature of Ge-NCs is suitable for low-temperature poly-Si TFT applications. Experimental results show that the poly-Si TFT nonvolatile Ge-NC memory has good P/E efficiency, long charge retention time, and good endurance characteristics. The poly-Si TFT nonvolatile Ge-NC memory has high potential in realizing the nonvolatile memory for SOP application in the future.

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