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# Threshold-Voltage Fluctuation of Double-Gated Poly-Si Nanowire Field-Effect Transistor

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***Abstract*—In this letter, the fluctuation characteristics of polycrystalline silicon (poly-Si) nanowire (NW) thin-film transistors (TFTs) with independently controlled double-gate configuration were studied. The defects existing in the NW channels are identified as one of the major sources for the fluctuation. The passivation of these defects by plasma treatment is shown to be effective for reducing the fluctuation. We have also found that the fluctuation is closely related to the operation modes. When only one of the gates is employed as the driving gate to control the switching behavior of the device, an optimum bias for the other gate can be found for minimizing the fluctuation.**

***Index Terms*—Double gate, fluctuation, nanowire (NW), polycrystalline silicon (poly-Si).**

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) have become an important building block for large-area [1] and 3-D [2] electronic products, owing to the low-temperature and mature fabrication technology. In conventional poly-Si TFTs, however, the large amount of defect contained in the poly-Si film leads to high subthreshold slope ($SS$) and OFF-state leakage current. Recently, poly-Si devices built with nanowire (NW) channels have been reported [3]–[6]. Owing to the tiny volume, the total defects in the NW channel are dramatically reduced. This feature, together with the implementation of a multiple-gated scheme, facilitates the realization of poly-Si devices with steep SSs (< 100 mV/dec) [3], [6].

For practical applications, it is important to understand the properties associated with poly-Si NW devices, particularly the fluctuation of device characteristics. However, few works were devoted to this topic [7]. In this letter, we address this issue and study the impacts of process treatment, channel length, and operation mode on the characteristics of a novel poly-Si NW TFT. The device channels which are formed by the sidewall spacer etching technique are surrounded by an inverse-T gate and a top gate. The structure and cross-sectional image of the NW channel by transmission electron microscopy (TEM) are shown in Fig. 1. Details about the device fabrication can be found in our previous report [6]. Fig. 1 also shows the bias conditions of the two independent gates for the three operation modes studied in this letter.

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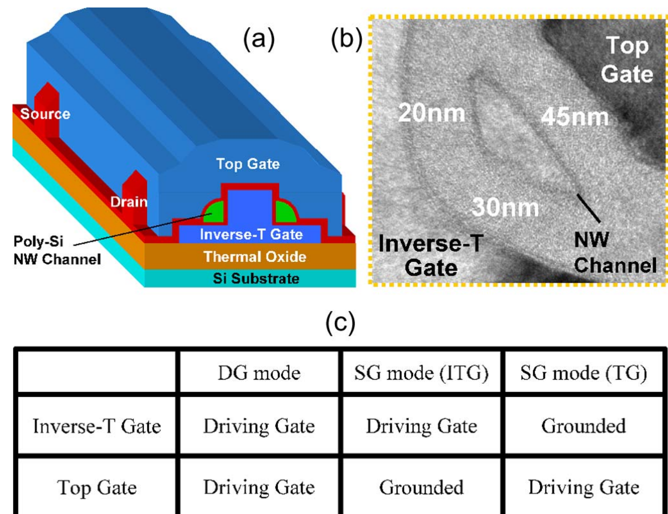


| | DG mode | SG mode (ITG) | SG mode (TG) |
|---|---|---|---|
| Inverse-T Gate | Driving Gate | Driving Gate | Grounded |
| Top Gate | Driving Gate | Grounded | Driving Gate |

Fig. 1. (a) Schematic illustration of the double-gated poly-Si NW device. (b) TEM picture of the cross-sectional image of an NW channel. (c) Definition of three operation modes.

Fig. 2 shows the transfer characteristics operating under DG operation mode for devices both with and without the plasma treatment [7]. The optional plasma treatment was performed in an $NH_3$ discharge after the device fabrication. The $NH_3$ plasma was generated in a diode reactor configured with a pair of parallel electrode plates powered by an RF power supply with a frequency of 13.56 MHz [8]. As can be seen in the figures, owing to the effective passivation of defects in the NW channels, both threshold voltage and $SS$ are significantly reduced with the plasma treatment. Several trends are also identified. First, the plasma passivation treatment is also effective in reducing the fluctuation, as shown in Fig. 2. Second, the fluctuation reduces with increasing channel length, as shown in Fig. 3(a). Moreover, the DG mode of operation depicts the smallest variation among the three operation modes, as shown in Fig. 3(b). To more deeply understand the experimental results, an analytical expression is used to describe the standard deviation of $V_{\mathrm{TH}}$

$$\sigma V_{\mathrm{TH}} = \frac{q}{C_{\mathrm{OX}}}\sqrt{\frac{N_{\mathrm{Trap}}W_d}{3LW}} \tag{1}$$

where $q$ is the charge of an electron, $C_{\mathrm{OX}}$ is the gate oxide capacitance per unit area, $N_{\mathrm{Trap}}$ is the effective trap concentration (in $\mathrm{cm}^{-3}$) in the poly-Si channel, $W_d$ is the channel depletion width, $L$ is the channel length, and $W$ is the channel

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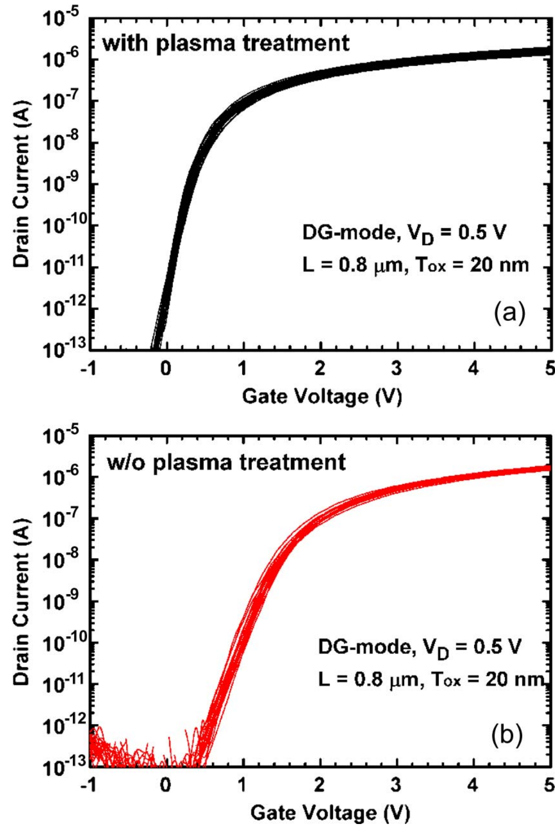


Fig. 2. Transfer characteristics of poly-Si NW devices under DG mode of operation (a) with and (b) without receiving $NH_3$ plasma treatment at 300 °C for 3 h. In each split, 20 devices were characterized.

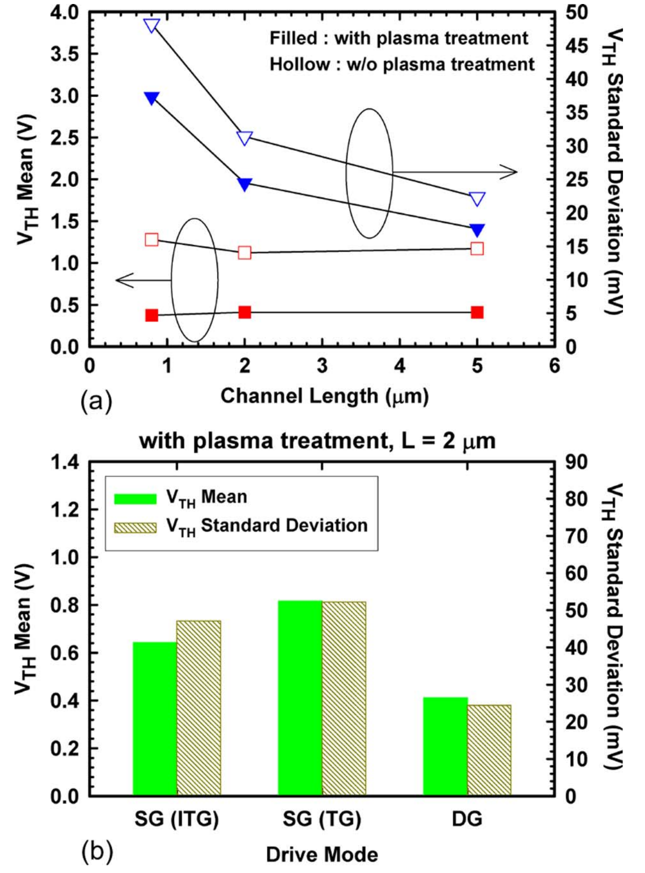


Fig. 3. (a) Mean value and standard deviation of $V_{\mathrm{TH}}$ as a function of channel length for devices operated under DG mode of operation. (b) Mean value and standard deviation of $V_{\mathrm{TH}}$ for plasma-treated devices with channel length of 2 $\mu$m under different operation modes.

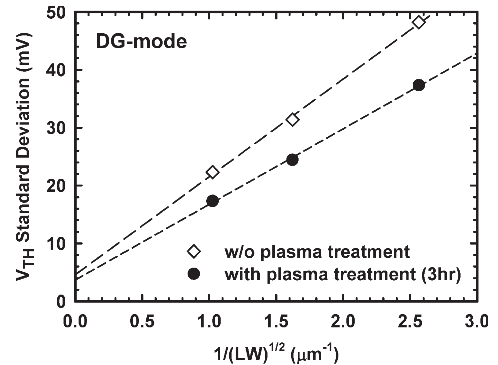


Fig. 4. Standard deviations of $V_{\mathrm{TH}}$ as functions of $(LW)^{-1/2}$ for devices with and without plasma treatment under DG mode of operation.

width. Equation (1) is based on a theory modified from the random-dopant-fluctuation (RDF) model [9]. It should be noted that the RDF model considers the dopant fluctuation effect in bulk CMOS devices. In the present case, no intentional channel doping was performed. However, defects contained in the grain boundaries of poly-Si NW act as trapping centers and may affect the $SS$ and threshold voltage [10]. The role played by these defects is thus similar to the dopant in the bulk CMOS. In reality, defects are located mainly in the grain boundaries of poly-Si films. In (1), it is assumed that defects are distributed uniformly in the film and $N_{\mathrm{Trap}}$ is the effective trap concentration. This assumption is reasonable in the present case as the characteristic grain size of the poly-Si film ($< 50$ nm) is much smaller than the channel length.

Fig. 4 shows the standard deviations of $V_{\mathrm{TH}}$ as a function of $(LW)^{-1/2}$ for the devices under the DG mode of operation. The slope of linear fitting line for the devices not receiving the plasma treatment is obviously larger than that for the treated devices. This is attributed to the passivation of defects by the plasma treatment and illustrates the importance of defect reduction in improving the fluctuation. From the mean $SS$ values shown in Fig. 2, we can estimate the effective trap density $T_{\mathrm{Trap}}$ (in cm$^{-2}$) in the channel based on the following [10]:

$$SS = \ln 10 \times \left(\frac{kT}{q}\right) \times \left(1 + \frac{C_{\mathrm{dm}}}{C_{\mathrm{ox}}}\right), \quad \text{where} \quad C_{\mathrm{dm}} = q \times T_{\mathrm{Trap}}. \quad (2)$$

The mean $SS$ is 188 and 105 mV/dec for the devices without and with plasma treatment, respectively, and the corresponding $T_{\mathrm{Trap}}$ is estimated to be around $2.3 \times 10^{12}$ and $8.1 \times 10^{11}$ cm$^{-2}$, respectively. Since the poly-Si NW channel is fully depleted, the product $N_{\mathrm{Trap}} W_d$ in (1) is actually equal to $T_{\mathrm{Trap}}$. Thus, we can calculate the contribution of channel defects to the device fluctuation based on the extracted $T_{\mathrm{Trap}}$ and (1). Nevertheless, the slopes calculated by (1) are smaller than the experimental data. This indicates that other fluctuation sources, such as gate oxide thickness, channel length, and width, also

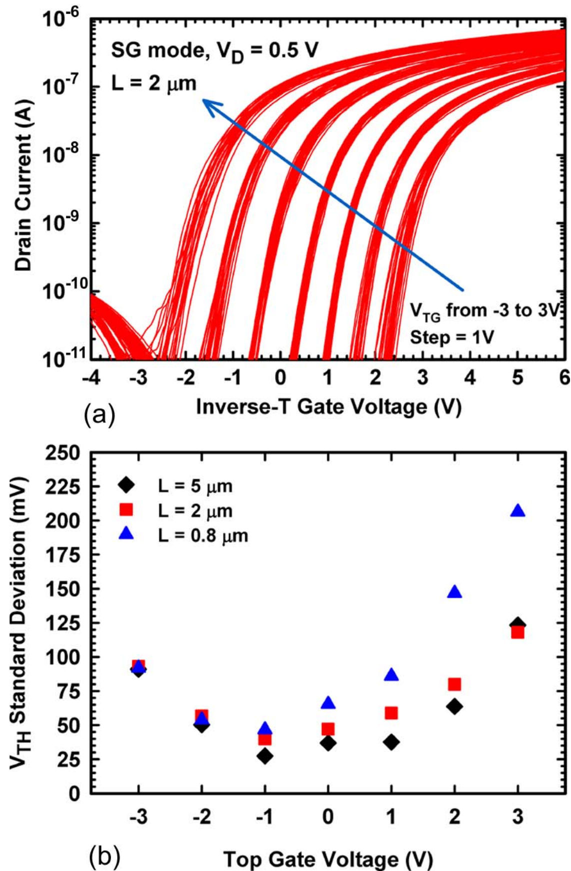


Fig. 5. (a) Transfer characteristics of devices with channel length of 2 $\mu$m measured by sweeping inverse-T gate voltage and fixed top-gate bias ranging from $-3$ to 3 V. (b) $V_{\mathrm{TH}}$ standard deviation as a function of top-gate bias for devices with different channel length. Twenty-five samples were characterized in each datum point.

affect the characteristics of poly-Si NW devices. Works for a detailed understanding of these factors are still in progress.

The independent gate configuration also provides more flexibility in device operation. For example, transfer characteristics obtained by driving one of the gates can be effectively modulated by the bias applied to the other gate (denoted as $V_{\mathrm{TH}}$-control gate here) [11]. In this letter, we also address the $V_{\mathrm{TH}}$ fluctuation issues under these operation conditions. Fig. 5(a) shows $I$–$V$ curves of 20 devices $(L = 2\ \mu\mathrm{m})$ measured with the inverse-T gate acting as the driving gate, while the top gate is serving as the $V_{\mathrm{TH}}$-control gate. Fig. 5(b) shows the standard deviation of $V_{\mathrm{TH}}$ as a function of top-gate bias for devices with channel lengths ranging from 0.8 to 5 $\mu$m. We can see that the smallest fluctuation is achieved when the top-gate voltage is in the range between 0 and $-1$ V, and the fluctuation worsens as the top-gate voltage shifts toward either a more negative or positive direction. This is because, when the top-gate voltage is shifted away from the optimum bias condition, it causes an increase in the transverse electric field in the NW channel which may enhance the impact of channel film-thickness variation on the modulation of the channel potential, thus leading to a larger $V_{\mathrm{TH}}$ variation [12]. In Fig. 5(b), the fluctuation under large top-gate bias worsens as the channel length is scaled down. This is because, when the top-gate bias is positive and sufficiently high, an inversion layer would be formed at the channel surface adjacent to the top gate; therefore, the device becomes a "normally on" type. In other words, a highly negative bias must be applied to the inverse-T gate to turn the device off [e.g., see Fig. 5(a)]. Under this situation, the effective gate dielectric consists of the gate oxide adjacent to the inverse-T gate and the fully depleted body and is thicker than the nominal gate oxide. Therefore, the aggravated short-channel effects lead to a larger $V_{\mathrm{TH}}$ fluctuation in short-channel devices.

In short, our study confirms that defects contained in the channel are the dominant source for the fluctuation observed in NW DG-TFTs. Our results also show that these defects can be effectively passivated with the plasma treatment, therefore effectively reducing the device fluctuation. Finally, reducing the $V_{\mathrm{TH}}$ fluctuation by optimizing the bias to the $V_{\mathrm{TH}}$-control gate under single-gate mode is also demonstrated in this letter.

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