Low-Dropout Regulators With Adaptive Reference Control and Dynamic Push–Pull Techniques for Enhancing Transient Performance

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***Abstract*—An adaptive reference control (ARC) technique is proposed for minimizing overshoot/undershoot voltage and settling time of low-dropout regulators. Linear operation provided by the ARC technique can dynamically and smoothly adjust the reference voltage so as to increase the slew rate of error amplifier thus forcing the output voltage back to its steady-state value rapidly. The amount of transient revision is proportional to transient state output voltage variation and load condition. In addition, a dynamic push–pull technique is used to enhance transient response. Experimental results demonstrate that the undershoot voltage, settling time, and load regulation are improved by 31%, 68.5%, and 70%, respectively, when load current changes between 1 and 100 mA.**

***Index Terms*—Analog ICs, CMOS analog ICs, dc–dc power conversion, MOSFET ICs .**

I. Introduction

LOW-DROPOUT (LDO) regulators are widely used in portable electronic devices as they occupy only small chip area and can convert battery voltages to low-noise, accurate voltages for noise-sensitive system-on-chip (SoC) applications. However, large parasitic capacitance at the gate of a power transistor degrades the slew rate of an error amplifier in case of load variations. Thus, several techniques are proposed for improving transient response time and transient voltage variations in order to maintain a reliable supply voltage for SoC applications. Especially, in the designs of an RF circuit, a stable and regulated supply voltage is the most important requirement for ensuring optimum performance. As we know, the transient response is limited by the bandwidth of the LDO regulators and the internal slew rate associated with the parasitic capacitance of the power MOSFET. Several fast transient techniques are proposed to extend the bandwidth of the LDO regulators and improve the slew rate at the gate of the power MOSFET [1]–[7].

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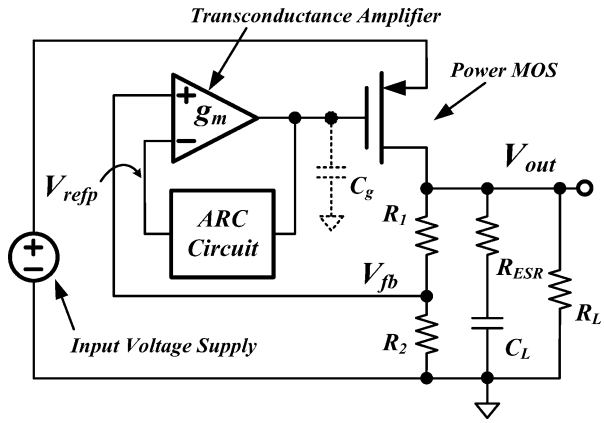

Fig. 1. LDO with ARC technique.

The first fast transient technique named as nonlinear control [1]–[3] speeds up the time of charging/discharging the large parasitic capacitor (C_g) at the gate of a power transistor, as shown in Fig. 1. This technique has the ability to provide large quiescent current for driving a large parasitic capacitor at the output of an error amplifier in case of load variations. However, it may suffer from oscillation problems. Thus, a tradeoff between system stability and speed exists in this fast transient technique. Generally speaking, temperature, process, and voltage variations are needed to be taken into consideration when the LDO regulator uses this fast transient technique.

Prediction control is an important fast transient technique to reduce transient voltage ripple. The most famous prediction technique is the adaptive voltage position (AVP) technique [3], [4], which continuously maintains constant output impedance of the converter. This technique improves dynamic performance like transient response time and transient voltage at the sacrifice of static performance like load regulation. Recently, one popular technique, the end-point prediction (EPP) technique, was proposed to improve the reference tracking speed [6]. However, the EPP technique, which is suitable only for reference tracking, still suffers from large overshoot/undershoot output voltage and slow response time in case of large load variations. The EPP technique cannot predict the variation of load current, thereby resulting in slow response.

According to the analysis of literatures, the fast transient technique must contain three important characteristics for providing a reliable supplying voltage. These are system stability at full loads, small overshoot/undershoot output voltage, and good line/load regulation. In order to satisfy the aforementioned

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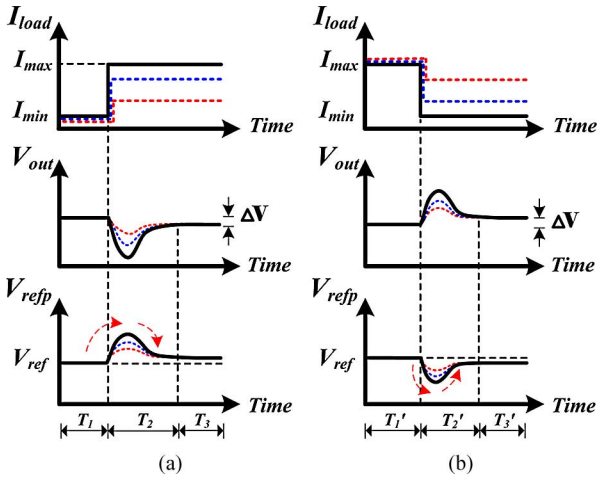


Fig. 2. Concept of ARC. (a) Load current changes from light to heavy. (b) Load current changes from heavy to light.

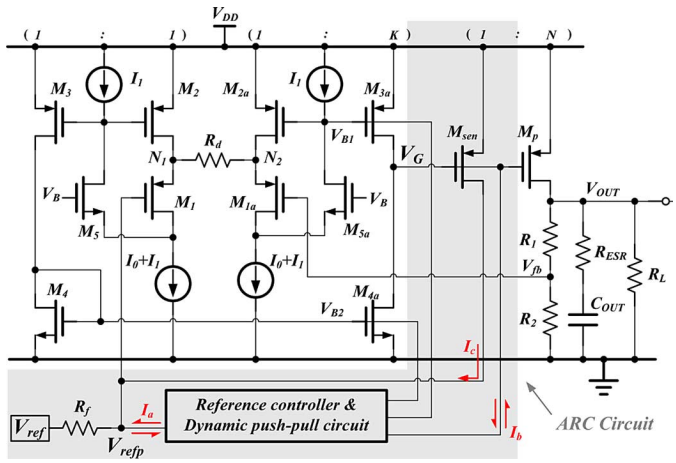


Fig. 3. Schematic of LDO with ARC circuit.

demands, the adaptive reference control and dynamic push–pull techniques are proposed to provide these three fast-transient characteristics at the same time for getting a regulated power supply.

Section II describes the analysis of the ARC technique for LDO regulators. Section III introduces the architecture of the ARC technique. Experimental results are illustrated in Section IV. Finally, conclusions are presented in Section V.

II. Concept of ARC Operation for an LDO Regulator

The block diagram of the proposed LDO with ARC technique is shown in Fig. 1 . This LDO is composed of a transconductance amplifier, an ARC circuit, a power transistor, an output capacitor C_L with equivalent series resistance (ESR) $R_{\rm ESR}$, and resistors R_1 and R_2.

In this design, ESR frequency compensation is used to introduce a pole-zero cancellation to ensure closed-loop stability. It is a simple and popular method to compensate the phase margin of the system. However, ESR degenerates the overshoot/undershoot voltage and limits the performance of the regulator in case of load variations. In order to overcome this issue, an ARC technique is proposed.

The concept of the proposed ARC technique is shown in Fig. 2(a) and (b). Reference voltage ($V_{{\rm ref}p}$), which is close to voltage $V_{\rm ref}$, can be adaptively and smoothly adjusted according to the error voltage ($V_{\rm err}$) between voltage $V_{{\rm ref}p}$ and scaled output voltage V_{fb}. During load transient period, the reference voltage $V_{{\rm ref}p}$ is increased when load current changes from low to high. The quantity of $V_{\rm err}$ is increased when V_{fb} is smaller than $V_{\rm ref}$. Therefore, the discharging current of the gate capacitor of the power transistor M_p and the falling rate of the gate voltage are increased to reach the appropriate voltage level. Oppositely, the reference voltage $V_{{\rm ref}p}$ is decreased when load current changes from high to low. The value of $V_{\rm err}$ and the charging current are also increased so as to fast charge the gate capacitor. Hence, the output voltage during the transient period can rapidly return back to the regulated voltage. It means that this scheme responds to undershoot (or overshoot) of the output voltage instantly and creates an adaptive adjustment of the reference voltage to achieve fast transient response.

With the ARC technique, waveforms of $V_{\rm out}$ and $V_{{\rm ref}p}$ are shown in Fig. 2 (a) and (b) when load current changes from light to heavy load, or vice versa. The main concept is that reference voltage $V_{{\rm ref}p}$ changes only during load transient period (T_2 and T_2'). At steady state, $V_{{\rm ref}p}$ is close to $V_{\rm ref}$ and the value of output voltage is not affected. That is the reason why the performance of the ARC technique is better than that of the AVP technique. Besides, load regulation can be enhanced if $V_{{\rm ref}p}$ is directly proportional to the load condition [7], i.e., voltage variation ΔV can be reduced. Hence, the value of voltage $V_{{\rm ref}p}$ in T_3 region is larger than that in T_1 region. Similarly, the value of voltage $V_{{\rm ref}p}$ in T_3' region is less than that in T_1' region when load current changes from heavy to light. Based on the aforementioned description, the ARC technique can use the error voltage $V_{\rm err}$ and load condition to control $V_{{\rm ref}p}$ signal for dynamically determining the reference voltage. The implementation of the ARC circuit is described in the following section.

III. Design of the Proposed Circuits

The schematic of an LDO with adaptive reference control circuit is shown in Fig. 3 . M_p is the power transistor and $M_{\rm sen}$ is the sensing transistor for sensing load condition, i.e., I_c is a load sensing current. I_a is generated by a reference controller and its value is proportional to the error voltage $V_{\rm err}$. In order to achieve the ARC technique, an additional resistor R_f is serial to a fixed voltage $V_{\rm ref}$. By using two revised currents I_a and I_c to flow through the resistor R_f, the reference voltage $V_{{\rm ref}p}$ can be dynamically adjusted for the LDO regulator according to the output voltage variation and load condition.

A. Transconductance Amplifier

Transconductance amplifier is composed of transistors M_1–M_5 and M_{1a}–M_{5a}. Two cascaded flipped voltage followers (CASFVF) [8]–[10] composed of (M_1, M_2, and M_5) and (M_{1a}, M_{2a}, and M_{5a}) have small output impedances to improve the linearity of level shifters. Therefore, the voltage difference between $V_{{\rm ref}p}$ and V_{fb} is equal to the voltage difference between nodes N_1 and N_2. Using three current mirror

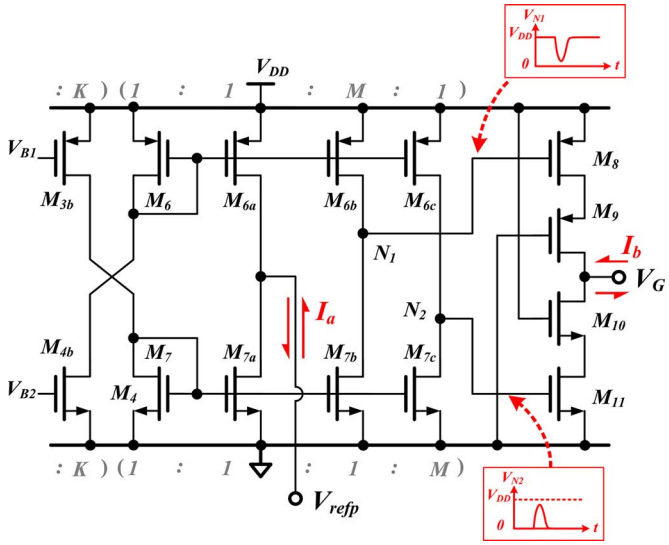


Fig. 4. Schematic of reference controller and dynamic push–pull circuit ($M > 1$).

pairs, which are (M_2, M_3), (M_{2a}, M_{3a}), and (M_4, M_{4a}), the transconductance can be determined as

$$g_m = \frac{2K}{R_d} \tag{1}$$

where K is the ratio of current mirror. Here, the transconductance amplifier has a broad bandwidth about megahertz, thus contributing to enhance the transient response time. However, the dc gain is slightly lower and not enough to support an excellent performance for load regulation. Hence, the load regulation compensator is used to retrieve it.

B. Reference Controller and Dynamic Push–Pull Circuit

The reference controller, as shown in Fig. 4, uses the transistors M_{3b} and M_{4b} to mirror the small-signal current from M_{2a} and M_4, respectively. Based on current mirror pairs (M_6, M_{6a}) and (M_7, M_{7a}), the revised current I_a can be generated and derived as

$$I_a = (V_{\text{refp}} - V_{fb})\frac{2K}{R_d}. \tag{2}$$

According to (2), the revised current that is proportional to the output error voltage can be used to adjust the reference voltage in case of large load variations.

The dynamic push–pull circuit is composed of transistors $M_{6b}, M_{6c}, M_{7b}, M_{7c}$, and M_8–M_{11} . Based on the appropriate design for the ratio of current mirror ($M > 1$), voltages of node N_1 and N_2 are set to "1" and "0" to force transistors M_8 and M_{11} to be turned off at steady state. Assuming that i_1 and i_2 are the sum of small-signal current of $M_{6b,7b}$ and $M_{6c,7c}$, respectively, they can be determined as

$$i_1 = i_2 = \frac{1}{2}g_m(V_{\text{refp}} - V_{fb})(1+M). \tag{3}$$

Once the load current changes and causes large output variations, the small-signal current i_1 (or i_2) is generated to pull the voltage of node N_1 (or N_2) down (or up). And then, transistor M_8 (or M_{11}) is turned on to charge (or discharge) the voltage V_G . Hence, this dynamic push–pull scheme can effectively enhance the transient response time for regulating the output voltage of LDO regulator back to a stable voltage level, i.e., the circuit is used to enhance the slew rate of the error amplifier during the transient period. In addition, transistors M_9 and M_{10} are used to prevent the noise of N_1 and N_2 from coupling to the gate of the power transistor when transistors M_8 and M_{11} are turned on.

Once load current rapidly changes from light to heavy, the gate–source voltage of the power transistor cannot be adjusted immediately owing to the slew rate of the transconductance amplifier. Hence, the output capacitor C_L supplies the insufficient charge between load current and input supplying source. There is an undershoot voltage at the output node. Thus, the reference controller converts the error voltage V_{err} to a revised current I_a, and increases the value of reference voltage $V_{\text{ref}p}$. Consequently, the slew rate of the transconductance amplifier can be enhanced during the transient period. Moreover, the dynamic push–pull circuit pulls up the voltage of node N_2 to discharge the node V_G through transistor M_{11}. The gate–source voltage of power transistor is rapidly increased, and thus, more energy is delivered to the load. When the output voltage is regulated back to its expected voltage, i.e., V_{err} is small, the revised current becomes trickle current and is not large enough to affect the reference voltage. Besides, the voltage of node N_2 is smoothly reset to "0" to turn transistor M_{11} off. Finally, the voltage $V_{\text{ref}p}$ becomes constant again at steady state.

C. Load Regulation Compensator

According to [7], the output voltage of LDO regulator can be derived as

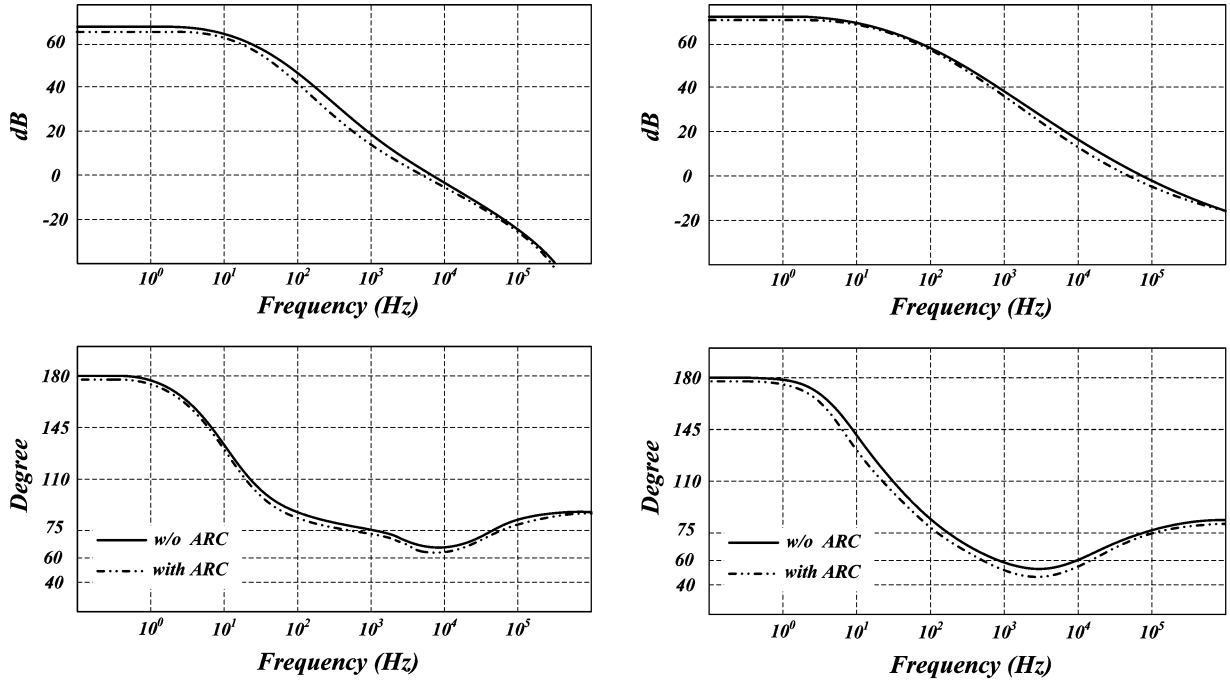
$$V_{\text{out}} = V_{\text{ref}p}\left(1 + \frac{R_1}{R_2}\right) - I_L R_{\text{load\_reg}}, \quad \text{where}$$
$$R_{\text{load\_reg}} = \frac{R_o}{1 + A_{\text{EA}}\beta} \tag{4}$$

where $R_{\text{load\_reg}}$ is the load regulation, A_{EA} is the open-loop gain of the error amplifier, β is the feedback factor, and R_o is the output resistance of the power transistor. In order to reduce the voltage variation ΔV due to load variations, the ARC circuit uses a load sensing current I_c to solve this issue, and we can obtain the following condition:

$$\frac{R_f}{N}\left(1 + \frac{R_1}{R_2}\right) = R'_{\text{load\_reg}}. \tag{5}$$

Hence, the sizes of R_f and the value of N are carefully designed to get a minimum voltage variation ΔV.

Based on the reference controller and load regulation compensator, the adaptive reference voltage $V_{\text{ref}p}$ can be derived as



(a) (b)

Fig. 5. Simulation results of loop gain and phase of the proposed LDO regulator. (a) Load current is 1 mA. (b) Load current is 100 mA.

in the following equation to satisfy the demands of different load conditions during transient and steady periods:

$$V_{\mathrm{ref}p} = V_{\mathrm{ref}} + \left((V_{\mathrm{ref}p} - V_{fb}) \frac{2K}{R_d} + \frac{I_L}{N} \right) R_f. \quad (6)$$

Substituting the results of (5) and (6) in (4), the output voltage of LDO regulator is derived as

$$V_{\mathrm{out}} = V_{\mathrm{ref}} R_f \left(1 + \frac{R_1}{R_2}\right) + (V_{\mathrm{ref}p} - V_{fb}) \frac{2K}{R_d} R_f \left(1 + \frac{R_1}{R_2}\right) + I_L (R'_{\mathrm{load\_reg}} - R_{\mathrm{load\_reg}}). \quad (7)$$

Referring to (7), the output voltage variation of LDO regulator in case of load variation is reduced by minimizing the difference between $R_{\mathrm{load\_reg}}$ and $R'_{\mathrm{load\_reg}}$. Owing to the variation of temperature and process, there is a little error between the value of $R'_{\mathrm{load\_reg}}$ and $R_{\mathrm{load\_reg}}$. However, the insertion of $R'_{\mathrm{load\_reg}}$ still has the ability to improve load regulation compared to the original design.

D. Stability Analysis

In order to demonstrate the stability in steady state, the analysis of positive/negative feedback loop should be considered carefully for designing the circuit. The dynamic push–pull circuit will be shut down when the output voltage is close to V_{ref}, i.e., M_8 and M_{11} are OFF; hence, we only need to analyze the ARC technique.

The feedback signal produced by LDO returns to both inputs of the transconductance amplifier. To improve the stability of the ARC technique, the quantity of both inputs is discussed. At the noninverting input terminal of transconductance amplifier, the negative feedback factor β_N is given by

$$\beta_N = \frac{R_2}{R_1 + R_2}. \quad (8)$$

At the inverting input terminal of transconductance amplifier, the positive feedback factor β_P is given by

$$\beta_P = 2K \frac{R_2}{R_1 + R_2} \times \frac{R_f}{R_d}. \quad (9)$$

Thus, the condition $\beta_N > \beta_P$ is essential for stability, i.e., the quantity of negative feedback is larger than that of positive feedback, and it assures that the proposed LDO is operating under stable condition. In our design, the parameters and components are shown in Table I.

TABLE I
PARAMETER AND COMPONENT VALUES

$\mathbf{R_f}$	10 kΩ	$\mathbf{R_1}$	100 kΩ
$\mathbf{R_d}$	50 kΩ	$\mathbf{R_2}$	100 kΩ
K	1	**M**	2

Fig. 5 shows the gain and frequency response of the proposed LDO with ARC technique under load currents of 1 and 100 mA. The gain of the LDO regulator is about 60 dB and the phase margin is larger than 60°, i.e., the structure of the ARC does not deteriorate the stability of the original design. The stability of the proposed LDO is guaranteed in our design.

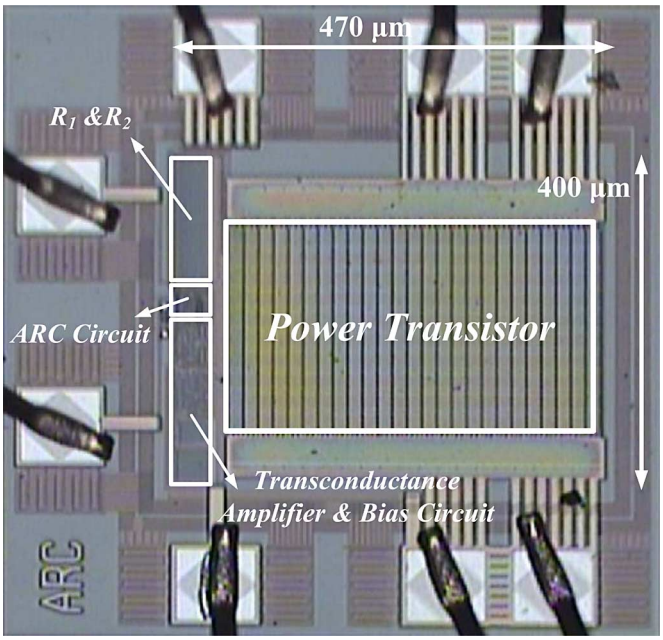


Fig. 6. Chip micrograph.

TABLE II
SUMMARY OF THE LDO PERFORMANCE

Technology	0.35-µm CMOS
Supply Voltage	2.1 V to 5 V
Output Voltage	2 V
Maximum Load Current	100 mA
Line Regulation	5 mV/V
Load Regulation	w/o ARC: 0.2 mV/mA with ARC: 60 µV/mA
Quiescent Current	40 µA
Dropout Voltage (I_{out}=100 mA)	60 mV
Settling Time (C_L=4.7 µF, R_{ESR}=0.3 Ω)	
1mA→100 mA)	w/o ARC: 20 µs with ARC: 10 µs
100 mA→1 mA	w/o ARC: 35 µs with ARC: 11 µs
(C_L=10 µF, R_{ESR}=0.5 Ω)	
1mA→100 mA	with ARC: 11 µs
100 mA→1 mA	with ARC: 10 µs
Undershoot Voltage	w/o ARC: 58 mV with ARC: 40 mV
Overshoot Voltage	w/o ARC: 55 mV with ARC: 54 mV

IV. EXPERIMENTAL RESULTS

The proposed LDO regulator with ARC technique was implemented in Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 and 0.65 V, respectively. The chip micrograph is shown in Fig. 6 and chip area is 400 μm $\times$ 470 μ m. A summary of the LDO performance is shown in Table II. Fig. 7 shows the experimental setup of the proposed LDO with ARC and dynamic push–pull techniques. Two output filter capacitors 4.7 and 10 μF, which have ESRs of 0.3 and 0.5 Ω, respectively, are used to demonstrate the performance of the

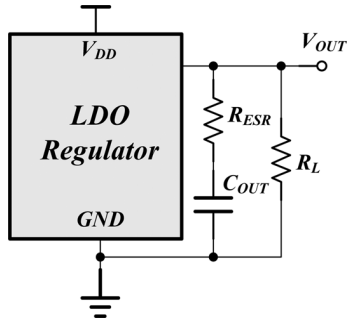
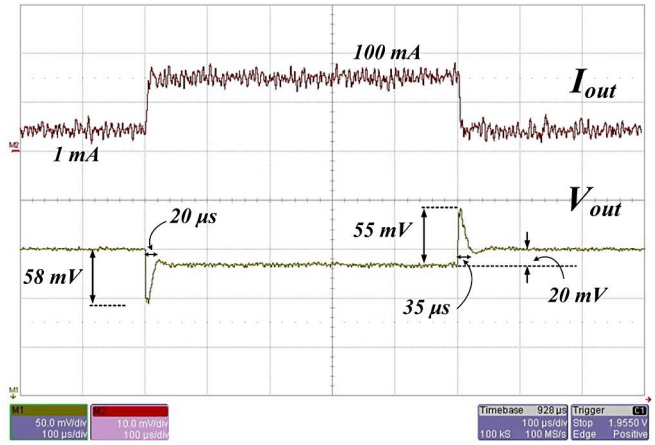
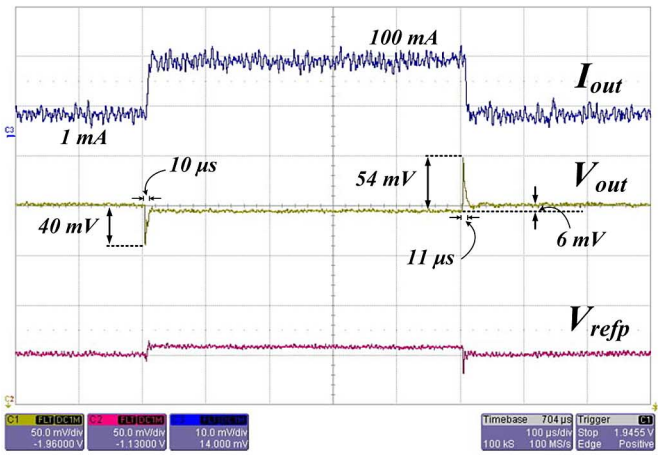


Fig. 7. Experimental setup of the proposed LDO regulator.



(a)



(b)

Fig. 8. Transient response of an LDO regulator with load current step from 1 to 100 mA, or vice versa. (a) Without ARC technique. (b) With ARC technique ($V_{\rm out}$ = 2 V, C_L = 4.7 μF, $R_{\rm ESR}$ = 0.3 Ω).

LDO regulator with ARC technique. The value of load resistor R_L is used to decide the load current.

The dropout voltage is about 60 mV at $I_{\rm out}$ = 100 mA. The load current with rising time and falling time of 0.1 μs changes from 1 to 100 mA, or vice versa. Fig. 8(a) and (b) shows the waveforms of LDO regulator without and with ARC technique, respectively. Obviously, the undershoot voltage and settling time are improved about 31% and 68.5%, respectively. Load regulation is improved about 70%. The enlarged waveforms

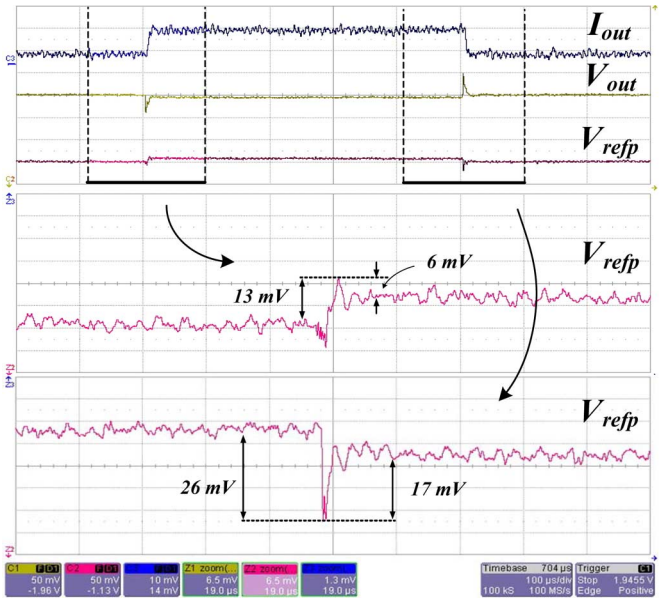


Fig. 9. Enlarged waveforms of an LDO regulator with ARC technique when load current changes from 1 to 100 mA, or vice versa.

shown in Fig. 9 demonstrate that the ARC technique can smoothly adjust reference voltage to stabilize output voltage in case of load variations. As the output capacitor C_L equals 10 μF, the measured results are shown in Fig. 10. Certainly, owing to the large output capacitor, the overshoot/undershoot voltage is smaller than that with a small output capacitor. Meanwhile, stability is also guaranteed in the proposed LDO regulator with ARC technique. Besides, Fig. 11 is the statistical representation of measured output voltage with different supply voltages. It is obvious that the LDO regulator with ARC technique has good line regulation. Table III shows the important performance parameters of the proposed circuit compared to previous designs. Referring to Table III, it is clear that the quiescent current of the proposed LDO regulator with ARC technique is much less than those of the previous designs. It causes the recovery time to be a little larger than those of other designs. However, the voltage drop is about 60 mV, which is much better than those of the prior arts. Besides, the performance of load regulation is enhanced by the load regulation compensator. Thus, the load regulation is about 60 μ V/mA. Compared to other LDO regulators, the performance is improved a lot. The figure of merit (FOM) of the proposed LDO regulator with ARC technique is 0.0048 μs and close to the values of the previous designs.

V. Conclusion

An LDO regulator with ARC technique is presented in this paper. The ARC technique can dynamically and smoothly adjust the reference voltage, which is proportional to the output error voltage and load condition, to enhance the slew rate of the error amplifier. Not only the undershoot/overshoot voltage can be improved but also the settling time and load regulation can be enhanced significantly.

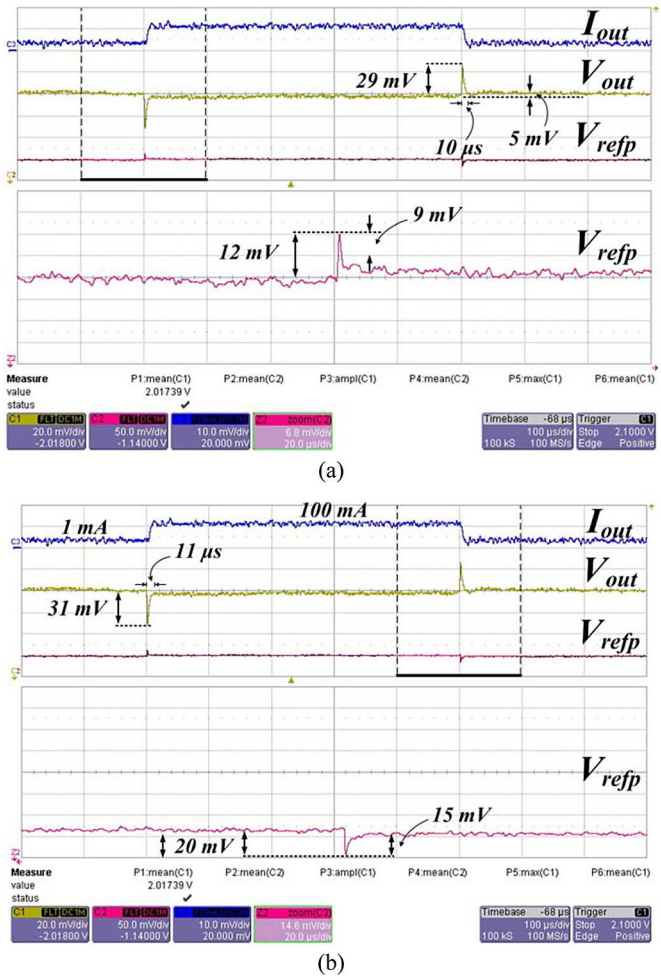


Fig. 10. Waveforms of an LDO regulator with ARC technique. (a) Load current changes from 1 to 100 mA. (b) Load current changes from 100 to 1 mA (C_L = 10 μF, $R_{\rm ESR}$ = 0.5 Ω).

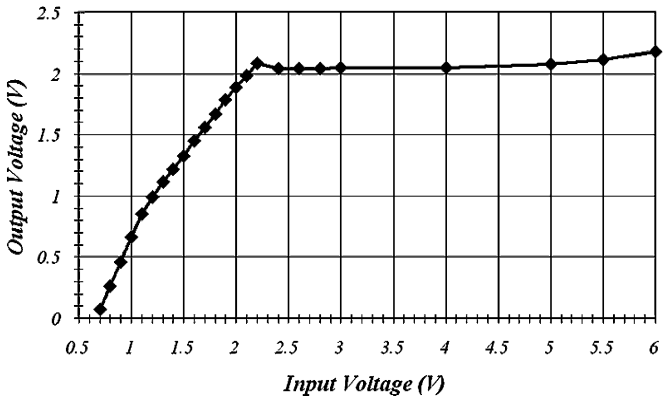


Fig. 11. Measured output voltage with different supply voltages.

Acknowledgment

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TABLE III
COMPARISONS OF THE PRIOR ART AND THE PROPOSED CIRCUIT

	[11]. 1998	[12]. 2004	[13]. 2006	[14]. 2007	[15]. 2008	**This work**
Technology (μm)	2	0.5	0.35	0.35μm	0.35μm	**0.35μm**
I_Q *(μA)*	23	23	53	65	95	40
V_{IN} *(V)*	≥1	3.3	2-5	3	1.2-1.5	2.1-5
I_{OUT} *(mA)*	50	160	150	50	50	100
Line Regulation	4mV/3.8V	N/A	0.143%/V	N/A	18mV/V	5mV/V
Load Regulation	19mV/50mA	0.2V/160mA	92.8ppm/mA	N/A	280μV/mA	60μV/mA
Area(mm^2)	1.375	N/A	0.2842	0.12	0.0448	0.188
Recovery time (T_r)	N/A	≤30μs	≤3.5μs	~15μs	2μs	≤12μs
Voltage Drop	232mV	100mV	110mV	200mV	160mV	60mV
FOM[*]	N/A	0.0043	0.00124	0.0195	0.0038	0.0048

[*] FOM = $(T_r I_Q)/I_{OUT}$ (μs).

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