國　立　交　通　大　學

電子物理學系　電子物理研究所碩士班

碩 士 論 文

完全鎳自我對準矽化源/汲與閘極之薄膜電晶體研究

An Investigation of the Fully Ni-salicided S/D and Gate in Poly-Si TFTs

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完全鎳自我對準矽化源/汲與閘極之薄膜電晶體研究

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摘　要

超薄的絕緣層上矽金氧半場效電晶體的大的源/汲極寄生電阻會使得元件性能變差。相同的問題也會發生在多晶矽薄膜電晶體。超薄的多晶矽薄膜電晶體限制了元件的驅動電流。為了減少多晶矽薄膜電晶體的寄生電阻，我們採用完全鎳自我對準矽化反應去解決這個問題。最近，關於矽化鎳的研究被廣泛地探討。片電阻方面，矽化鎳(NiSi)的片電阻是跟二矽化鈦($TiSi_2$)和二矽化鈷($CoSi_2$)差不多的。而且鎳金屬矽化物可以在低溫(400~600℃)時形成，而不會有結塊效應(agglomeration effect)。在矽化鎳的形成過程當中，它消耗較少的矽，所以它可以形成較淺的接面。

在本論文中，完全鎳自我對準矽化源/汲與閘極多晶矽薄膜電晶體(FSA-TFTs)

已經被成功地製造出來。和傳統的多晶矽薄膜電晶體比較的話，完全鎳自我對準矽化多晶矽薄膜電晶體有較小的源/汲極與閘極片電阻，而且它可以有效地抑制浮接基體效應(floating body effect)和寄生雙極性接面電晶體效應(parasitic bipolar junction transistor action)。實驗結果顯示完全鎳自我對準矽化多晶矽薄膜電晶體有較低的漏電流、較好的次臨界特性、較少的臨界電壓變化量和較大的場效遷移率。所以完全鎳自我對準矽化多晶矽薄膜電晶體的特性適合用在需要穩定的臨界電壓和大的崩潰電壓。

An Investigation of the Fully Ni-salicide S/D and Gate in Poly-Si TFTs

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ABSTRACT

Large source/drain parasitic resistance degrades device performance in the ultrathin-film silicon on insulator metal oxide field effect transistors (SOI MOSFETs). Similar problem also happens in the poly-Si TFT. Large parasitic resistance results in the limitation of the ON current in the thin-channel poly-Si TFTs. To decrease the parasitic resistance of the poly-Si TFTs, the fully Ni-salicidation is a technology to solve this problem. Recently, many researches have been studied about NiSi. The sheet resistivity of NiSi is comparable with that of $TiSi_2$ and $CoSi_2$. And Ni-silicidation can be accomplished at low temperature (400~600℃) without agglomeration effect. During the formation of NiSi, it is the less silicon consumption. So it can form shallower junction.

In this thesis, a fully Ni self-aligned silicided (fully Ni-salicided) source/drain and gate poly-Si thin-film transistors (FSA-TFTs) have been successfully fabricated

on 40-nm-thick channel layer. The FSA-TFTs exhibit small S/D and gate sheet resistance and can effectively suppress the floating-body effect and parasitic bipolar junction transistor action, compared to control TFTs. Experimental results show that the FSA-TFTs give lower off-state leakage, improved subthreshold characteristics, less threshold voltage variation, and larger field-effect mobility compared with control TFTs. The characteristics of the FSA-TFTs are suitable for high performance driving TFTs with a stable threshold voltage and large breakdown voltage.

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Chapter 1

Introduction

1.1 Brief introduction of poly-Si TFTs

At the beginning, the pixel switching device of active matrix liquid crystal displays (AMLCDs) rely upon a-S:H TFTs. However, the low field effect mobility (below 1 cm^2/V-s generally) of the a-Si:H TFTs limit its application. In order to integrate peripheral driving circuits on the same glass substrate, the device with high mobility by a simple and low temperature process should be developed. The mobility of poly-Si can reach 10 to 300 cm^2/V-s [1-2]. Polycrystalline-silicon (poly-Si) thin film transistors (TFTs) are used in a wide variety of application fields, including linear image sensors, photo-detector amplifiers, thermal printer heads, and scanners. Poly-Si TFTs can also be used in DRAM, SRAM, EPROMs, and EEPROMs.

The performance of poly-Si TFTs is strongly influenced by the size of grain and the trap states within the grain boundaries. In order to obtain large grain size, there are many methods, including Solid Phase Crystallization (SPC), Excimer laser annealing (ELA), Metal Induced Crystallization (MIC), Metal Induced Lateral Crystallization (MILC). About the trap states within the grain boundaries, they can be passivated with H_2 [3], NH_3 [4], N_2O [5], O_2 [6] plasma.

1.1.1 Solid Phase Crystallization (SPC)

Because the a-Si is deposited at temperature below 600°C, the thermal crystallization for several hours (~24 hours) at 600°C is required to convert them into final polycrystalline form. This method is called Solid Phase Crystallization (SPC).

Thin Films deposited in the amorphous state and then crystallized into poly-Si by a furnace have been shown to have higher carrier mobility compared to thin films deposited in the polycrystalline state directly. The main advantages of SPC include good uniformity, smooth surface, compatible with the silicon technology, and without extra cost. But, low throughout and still high defect were its main disadvantages.

1.1.2 Excimer Laser Annealing (ELA)

The basic principle of laser crystallization is the transformation from amorphous to crystalline silicon by melting the silicon for a very short time. Strictly speaking, the ELA process is not a low temperature process. With the excimer laser annealing, the silicon is heated above 1200°C. However, the high temperatures are only sustained for a very short time. Because a very short time of the laser annealing, the thermal energy will not propagate to damage the glass substrate. The throughput of the ELA process is higher than that of the SPC process and the large grain size translates to fewer defects.

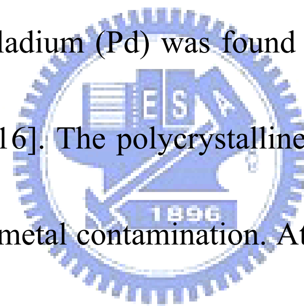
But the disadvantages of the ELA process include narrow laser process window,

high initial facility cost and high process complexity [7].

1.1.3 Metal Induced Crystallization (MIC)

The metal induced crystallization is a technology of transferring the a-Si into poly-Si with large grain size [8]. When a certain metal, for example Al [8]、Cu [9]、Ag [10]、Au [11]、Pd [12]、or Ni [13], is deposited on a-Si, the a-Si crystallizes to poly-Si at a lower temperature than its SPC temperature. But MIC has a disadvantage of the metal contamination.

Metal induced lateral crystallization (MILC) is also a technology to enlarge the grain size. Nickel (Ni) or Palladium (Pd) was found to induce crystallization of a-Si outside its coverage area [14-16]. The polycrystalline silicon thin films, produced by the MILC, are largely free of metal contamination. At the same time, they have better crystallinity than those produced by SPC.



1.2 Introduction of some material for salicide process

In the ultrathin-film silicon on insulator metal oxide field effect transistors (SOI MOSFETs), large parasitic resistance degrades device performance. This problem has been solved by using self-aligned silicide (salicide). Similar problem also happens in the poly-Si TFT. To decrease the parasitic resistance of the poly-Si TFT, the salicide is a technology to solve this problem.

Recently, the material of the fully silicide gate include $TiSi_2$ [17], $CoSi_2$ [18- 19],

NiSi [20], HfSi [21], PdSi [22], $Co_{(1-x)}Ni_{(x)}Si_2$ [22] and so on. Among silicides as mentioned above, $TiSi_2$, $CoSi_2$, and NiSi were widely used in the silicide process. The fully silicide gate has many benefits: First, compared with the poly-Si gate, the fully silicide gate does not have poly depletion effect (PDE). Second, when metals are deposited on gate dielectrics, sputtering damage may occur. Third, the work function of the silicide gate can be tuned by doping the poly-Si with different dopants and dosages.

Because $TiSi_2$ has a low sheet resistance (13~15Ω/□) and better thermal stability, it is widely used in the IC industry. But $TiSi_2$ has the narrow lines effect, and Ti can react with the oxide at the elevated temperature. $CoSi_2$ is an attractive replacement of $TiSi_2$ due to its relatively linewidth-independent sheet resistance [23-25]. The formation of $CoSi_2$ does not need phase transformation, so it can be extensively used in the narrow line. In addition, Co does not react with oxide. However, the formation of the $CoSi_2$ will consume more Si than the formation of the $TiSi_2$. It will result in a deeply junction and also a large junction leakage current.

NiSi is also a kind of material for silicide application [26-27]. Regarding the sheet resistance, NiSi is comparable with that of $TiSi_2$ and $CoSi_2$. Like $CoSi_2$, NiSi also does not have narrow line effect. Then NiSi process offers a number of merits : First, silicidation can be formed at low temperature (400~600°C) without

agglomeration. Second, the work function of NiSi can be tuned by doping different dopants, such as arsenic, phosphorous, and antimony [28-29]. Third, nickel is not reacted with oxide. Fourth, during the silicidation process, NiSi has the less silicon consumption compared with $TiSi_2$ and $CoSi_2$. Hence, NiSi can form the shallower junction.

1.3 Motivation

In the ultrathin-film poly-Si TFTs, large parasitic resistance degrades device performance. To decrease the parasitic resistance of the poly-Si TFTs, the Ni-salicidation is a technology to solve this problem.

In this thesis, for the first time, we carried out the fully Ni-salicided source/drain (S/D) and gate with different gate implant dosages, including in-situ doped gate and un-doped gate. We want to increase the driving current of device and decrease the gate and S/D parasitic resistance. Salicidation is a technology to suppress the floating body effect because the silicide near the source/body junction act as a sink for holes [30]. Accumulation of holes was decreased, which results in a less activated parasitic bipolar junction transistor. So, the performance of fully Ni-salicided poly-Si TFTs (FSA-TFTs) is expected to have a better performance than that of control TFTs.

1.4 Organization of the Thesis

In this thesis, experimental process and electrical parameters extraction are shown in chapter 2. In chapter 3, the performance of FSA-TFTs (in-situ doped gate) and that of control TFT are compared. At the same time, the performance of FSA-TFTs (un-doped gate) and that of control TFTs are compared. Some more detailed electrical characteristics of FSA-TFTs are discussed. In chapter 4, the conclusions of this thesis and the future works are given.

Chapter 2

Experimental process and electrical parameters extraction

2.1 Fabrication of poly-Si thin-film transistors (poly-Si TFTs)

In this section, the process flow of poly-Si thin-film transistor is described, including the process flows of the FSA-TFTs and the control TFTs.

2.1.1 Fabrication of the FSA-TFTs

The process flows of devices are showed in Fig.2-1. First, a 550-nm thick oxide was deposited on the 6-in wafers. Then, a 40-nm thick a-Si layer was deposited as the active layer in a LPCVD system using SiH_4 as source at 550°C. The a-Si was crystallized to poly-Si by solid phase crystallization (SPC) process at 600°C for 24 hours. Then the wafers were subjected to photolithography for active region definition. A 50-nm thick TEOS oxide layer and a 50-nm a-Si layer were deposited. A 150-nm nitride was deposited by LPCVD as hard mask. Then the nitride layer and the a-Si layer were etched by the oxide dry etcher (TEL-5000) and poly-Si dry etcher (TCP-9400), respectively. The wafers were ion implanted by phosphorous. The energy and the dose of implantation were 45 keV and 5×10^{15} cm^{-2}, respectively. A 300-nm thick TEOS oxide was deposited, then the spacer was formed by TEL5000 to avoid bridge

effect between gate and S/D. The 150-nm thick nitride layer was stripped by H_3PO_4. After a HF-dip for 10-sec, a 40-nm thick Ni and a 10-nm thick TiN were deposited on the wafer by Metal-PVD. NiSi was formed in the gate and S/D region by rapid-thermal annealing (RTA) at 550°C for 30 seconds. The unreacted TiN and Ni were selectively removed by H_2SO_4.

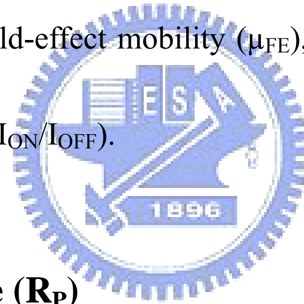
2.1.2 Fabrication of control TFTs

Besides the fabrication of FSA-TFTs, control TFTs were also fabricated for comparison. In fast, the process flow of the control TFTs is nearly the same as that of FSA-TFTs. So, the process flow of the control TFTs is described briefly. First, a 550-nm thick oxide was deposited on the 6-in wafers. Then, a 40-nm thick a-Si layer was deposited as active layer in a LPCVD system. The a-Si was crystallized to poly-Si by SPC process at 600°C for 24 hours. Then the wafers were subjected to photolithography for active region definition. A 50-nm thick TEOS oxide layer and a 50-nm in-situ doped a-Si layer were deposited in a vertical furnance. A 150-nm nitride was deposited by LPCVD as the hard mask. Then the nitride layer and the in-situ doped a-Si layer were etched by the TEL-5000 and TCP-9400, respectively. The wafers were ion implanted by phosphorous. The energy and the dose of implantation were 45 keV and 5×10^{15} cm^{-2}, respectively. A 300-nm thick TEOS oxide was

deposited, then the spacer is formed by TEL5000. The 150-nm thick nitride layer was etched by H_3PO_4. Next, 300-nm passivation oxide was deposited by PECVD and patterned for contact holes opening. A 500-nm thick Al was immediately thermal evaporated, followed by lithography for Al pad pattern definition.

2.2 Electrical parameters extraction

In this section, the methods of parameter extraction used in this study are described. These parameters include parasitic resistance (R_P), threshold voltage (V_{TH}), subthreshold swing (S.S.), field-effect mobility (μ_{FE}), ON current (I_{ON}), OFF current (I_{OFF}), ON/OFF current ratio (I_{ON}/I_{OFF}).



2.2.1 Parasitic resistance (R_P)

The device parasitic resistances are extracted from their output characteristics. It is known that when devices are operated under low drain voltage and high gate voltage their measured resistance (R_m) can be expressed as

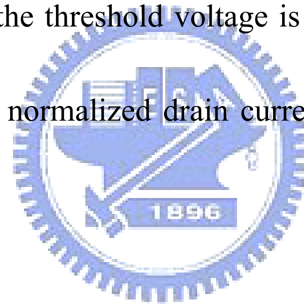
$$R_m = R_{ch} + R_P = \frac{L - \Delta L}{W_{eff}\mu_{eff}C_{OX}(V_{GS} - V_T)} + R_P \text{ ------------------------ (Eq. 2.1)}$$

where R_{ch} and R_p represent channel resistance and parasitic resistance. C_{OX} is the gate dielectric capacitance per unit area and W, L, V_{TH} are device channel width, length and threshold voltage, respectively. The parasitic resistance R_p can be extracted by plotting R_m versus L for varying gate voltages.

2.2.2 Threshold voltage (V_{TH})

The threshold voltage V_{TH} is an important parameter required for the channel length-width and series resistance measurements. However, V_{TH} is not unique defined. Various definitions exist and the reason for this can be found in the I_D-V_G curves. One of the most common threshold voltage measurement technique is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100 mV typically to ensure operation in the linear MOSFET region.

However, in this thesis, the threshold voltage is defined at a fixed drain current $I_D=I_{DN}\times(W/L)$ where I_{DN} is a normalized drain current. Here, I_{DN} is 100 nA and the same for all devices.



2.2.3 Subthreshold swing (S.S.)

The drain current in the saturation region($V_D>V_G-V_{TH}$) is expressed as the following equation:

$$I_{DS}=\frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2 \quad \text{(Eq. 2.2)}$$

It appears that the current abruptly vanishes while V_G is reduced to zero from the equation. In reality, there is still some drain conduction current below threshold, and this is known as the subthreshold conduction. This current is due to the weak inversion in the channel between flat-band and threshold, which leads to a diffusion

current from source to drain.

The subthreshold swing (S.S.) is defined as the reciprocal of slope of the I_D-V_G curve in weak inversion region. It is the amount of gate voltage required to increase/ decrease drain current by one order of magnitude. It is a typical parameter to describe the control ability of gate toward channel.

In this thesis, the subthreshold swing is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.2.4 Field effect mobility (μ_{FE})

The field effect mobility (μ_{FE}) is extracted from the maximum value of transconductance (g_m) at low drain voltage. The drain current in linear region ($V_D < V_G - V_{TH}$) can be approximated as the following equation:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^{2} \right] \text{ ------------------------ (Eq. 2.3)}$$

where

W is the channel width,

L is the channel length,

V_{TH} is the threshold voltage,

C_{ox} is the gate oxide capacitance per unit area.

Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_{DS} \quad \text{-- (Eq. 2.4)}$$

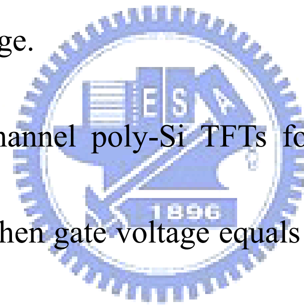
Therefore, the field-effect mobility is

$$\mu_{FE} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{-- (Eq.2.5)}$$

2.2.5 ON/OFF current ratio

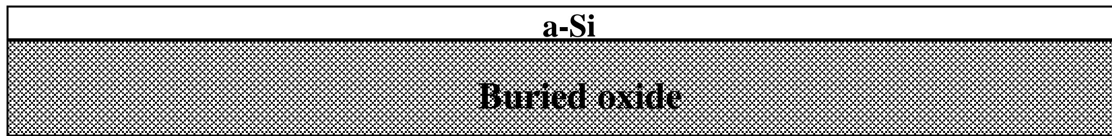
A poly-Si TFT with good characteristics should have not only high ON state driving current but also low OFF state leakage current. For pixel transistors, the OFF state is frequently encountered in normal operation. Therefore, ON/OFF current ratio is obviously a better evaluation parameter compared with ON state current alone. The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly crystalline Si. A large amount of trap densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than that in MOSFET. Considering large negative gate bias V_G is applied, a hole channel forms under the gate. In principle, little current flows because the junction between the hole

channel and the drain is reverse-biased. However, due to the existing numerous trap states in the polysilicon film and the large electric field, electron and hole emission from trap states becomes a strongly increasing function of electric field. Here, a trap could be modeled by a potential well. For large electric fields, it is possible for electrons to escape the potential well by quantum mechanical tunneling. The tunneling rate increases strongly with electric field because the barrier thickness decreases. The effect is a rapid increase in leakage current. The tunneling rate depends upon the total electric field, and consequently the leakage current is highest when both drain and gate voltages are large.

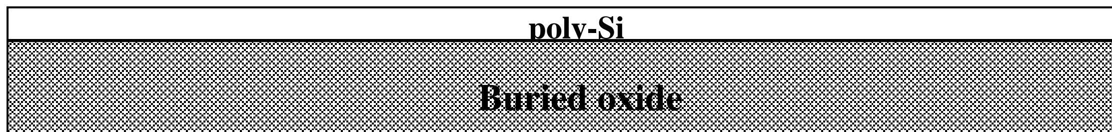


In this thesis, take n-channel poly-Si TFTs for examples, the ON current is defined as the drain current when gate voltage equals to 15 V and drain voltage is 0.5 V. The OFF current is specified as the minimum current when drain voltage equals to 0.5 V.

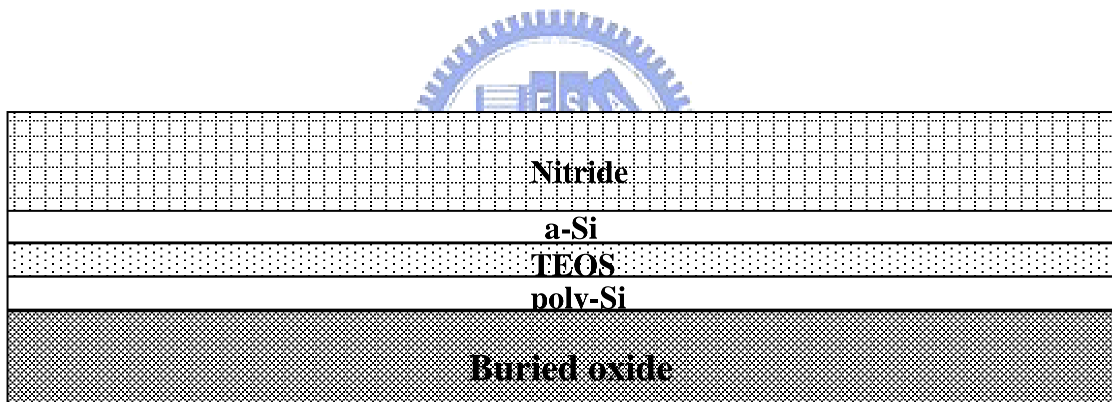
$$\frac{I_{ON}}{I_{OFF}} = \frac{Current\ \ of\ \ I_{DS} - V_{GS}\ \ Plot\ \ at\ \ V_{DS} = 0.5V, V_{GS} = 15V}{Minimum\ \ Current\ \ of\ \ I_{DS} - V_{GS}\ \ Plot\ \ at\ \ V_{DS} = 0.5V} \text{--------------(Eq. 2.6)}$$



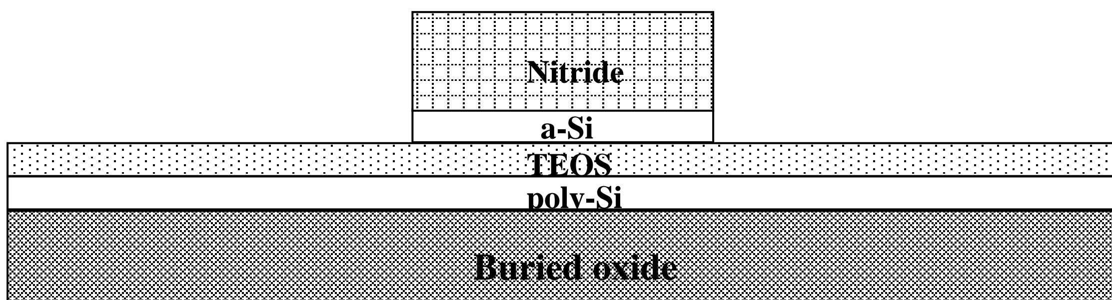
(1) 550-nm thick buried oxide and 40-nm thick a-Si were deposited.



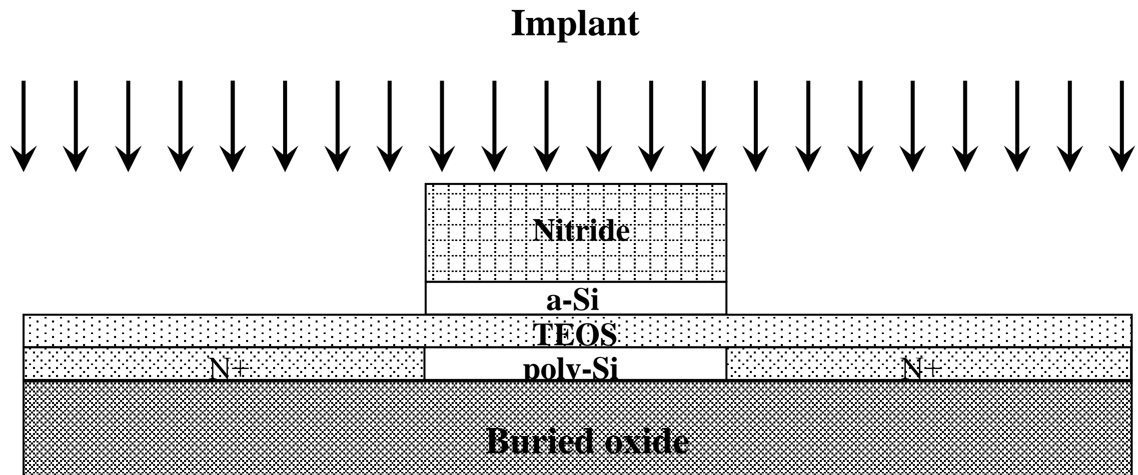
(2) 600°C annealing for 24-hr and active region definition.



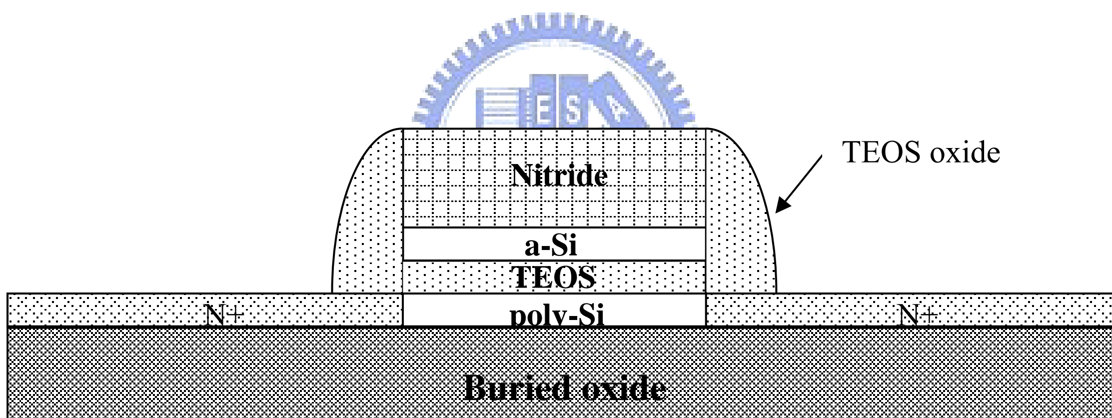
(3) 50-nm thick TEOS oxide , 50-nm thick a-Si and 150-nm thick nitride layer.



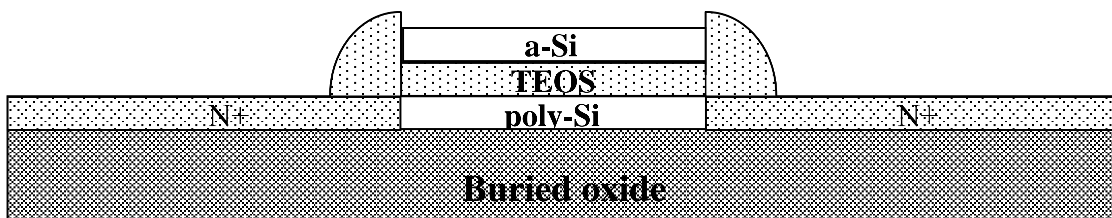
(4) Gate definition.



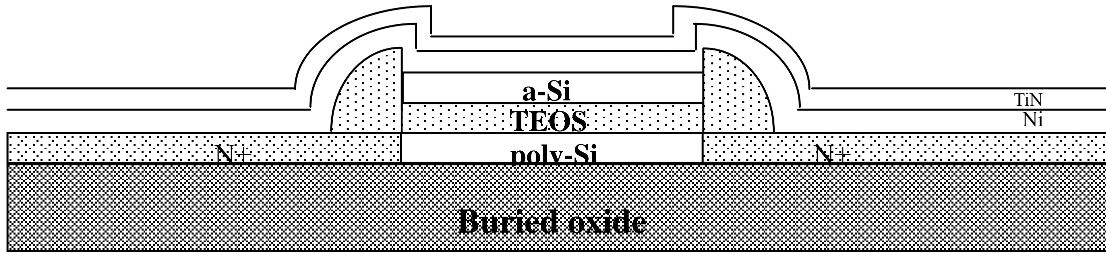
(5) Phosphorous implantation.



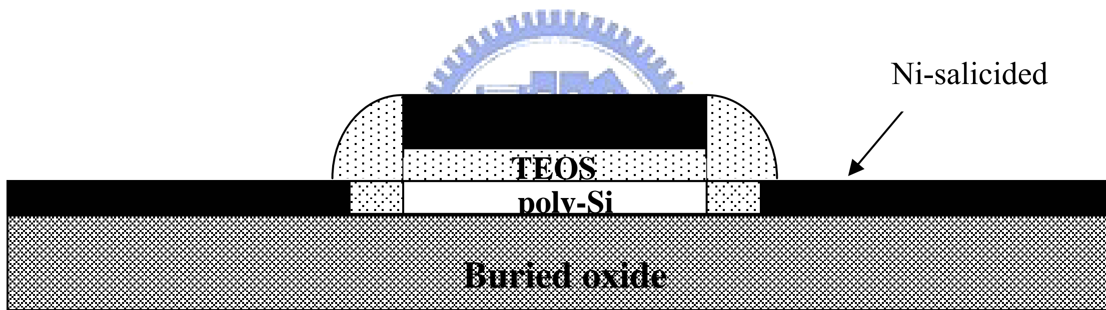
(6) TEOS spacer formation.



(7) Nitride layer was etched by H_3PO_4.



(8) Ni and TiN deposition.



(9) NiSi formation by RTA 550°C.

Fig. 2-1 Process flows of fully Ni-salicidation TFTs.

Chapter 3

Electrical Characteristics of the Fully Ni-Salicided TFTs

At first, the cross-section TEM of FSA-TFTs (un-doped gate RTA 550°C 30-sec) is shown in Fig.3-1. Thicknesses of channel film, TEOS oxide and gate are shown in Fig.3-2. In this chapter, the electrical characteristics of control TFTs and FSA-TFTs (in-situ doped gate) with RTA 550°C 30-sec are compared at first in 3.1. Then the electrical characteristics of control TFTs and FSA-TFTs (un-doped gate) with RTA 550°C 30-sec are compared in 3.2. Device parameters including parasitic resistance (R_P), threshold voltage (V_{TH}), subthreshold swing (S.S.), field-effect mobility (μ_{FE}), ON current (I_{ON}), OFF current (I_{OFF}), and ON/OFF current ratio are all extracted. Next step, we will explain the electrical characteristics of control TFTs and FSA-TFTs. We found that S/D fully salicidation resulted in the reduction of V_{TH}、kink effect、threshold voltage roll off、subthreshold swing roll off and Gate-Induced-Drain-Leakage (GIDL) enhancement current.

3.1 Basic electrical characteristics of FSA-TFTs (in-situ doped gate)

Figure 3-3 shows the parasitic resistance (R_P) of the control TFTs. The extracted

value of R_P is 7.521 kΩ. Figure 3-4 shows the parasitic resistance (R_P) of the FSA-TFTs. The extracted value of R_P is 0.7965 kΩ. Obviously, the R_P of the FSA-TFTs is significantly lower than that of the control TFTs.

Figure 3-5 exhibits I_D-V_G and field-effect mobility characteristics of control TFTs with W/L=10 μm/10 μm and T_{ox}=500 Å. The drain bias is 0.5 V and 5.0 V. The ON current (I_{ON}) at V_D=0.5 V and V_G=15 V of control TFTs is 12.68 μA. The OFF current (I_{OFF}，the minimum value of drain current) of control TFTs is 1.25 pA. So, the ON/OFF current ratio (I_{ON}/I_{OFF}) is 1.01×10^7. The maximum mobility of control TFTs is 29.58 cm^2/V-s.

Figure 3-6 exhibits I_D-V_G and field-effect mobility characteristics of the FSA-TFTs with W/L=10 μm/10 μm and T_{ox}=500 Å. The drain bias is 0.5 V and 5.0 V. The ON current at V_D=0.5 V and V_G=15 V of FSA-TFTs is 14.44 μA. The OFF current of FSA-TFTs is 0.1 pA. So, the ON/OFF current ratio is 1.444×10^8. The maximum mobility of the FSA-TFTs is 33.96 cm^2/V-s. Based on the above electrical results, significant improvements can be found for the FSA-TFTs. All devices' parameters of the control TFTs and the FSA-TFTs are listed in the Table 3-1.

Figure 3-7 shows the comparison of I_D-V_G characteristics at V_D=0.5 V between control TFTs and FSA-TFTs with W/L=10 μm/10 μm. Figure 3-8 shows the comparison of mobility between control TFTs and FSA-TFTs with W/L =10 μm/10

μm. Fully Ni-salicidation remarkably improves the mobility of TFTs. From Table 3-1, FSA-TFTs give smaller threshold voltage, higher mobility, higher ON current and higher ON/OFF current ratio.

Figure 3-9 show I_D-V_D characteristics of control TFTs and FSA-TFTs with W/L =10 μm/10 μm (V_G-V_{TH}=3.0 V, 4.0 V, 5.0 V, 6.0 V). The output current of FSA-TFTs is obviously larger than that of control TFTs. The low parasitic resistance by fully Ni-salicidation greatly boosts the output current.

Figure 3-10 shows I_D-V_D output characteristics of control TFTs and FSA-TFTs with W/L=10 μm/0.8 μm. The output characteristics exhibit in fact an anomalous current increase in the saturation region. The kink effect [31-32] is observed. The detailed explanation about the kink effect is shown in 3.3.2.

Figure 3-11 exhibits V_{TH} roll off characteristics of control TFTs and FSA-TFTs. All threshold voltages of control TFTs and FSA-TFTs are summarized in Table 3-2. The threshold voltage roll off from 10 μm to 0.8 μm of control TFTs at V_D=0.5 V is 1.402 V. The threshold voltage roll off from 10 μm to 0.8 μm of FSA-TFTs at V_D=0.5 V is 0.37 V. Obviously, threshold voltage roll off phenomenon of control TFTs is more severe than that of FSA-TFTs. Because the floating body effect of control TFTs is more severe than that of FSA-TFTs. So, V_{TH} roll off phenomenon of control TFTs is more severe.

Figure 3-12 exhibits subthreshold swing (S.S.) roll off characteristics of control TFTs and FSA-TFTs. The drain bias is 5 V. The channel width is 10 μm. The S.S. roll off from 10 μm to 0.8 μm of control TFTs at V_D=5 V is 295.84 mV/dec. The S.S. roll off from 10 μm to 0.8 μm of FSA-TFTs at V_D=5 V is 148.04 mV/dec. Table 3-3 shows detailed data about subthreshold swing from 10 μm to 0.8 μm. Obviously, S.S. roll off phenomenon of control TFTs is more severe than that of FSA-TFTs.

Figure 3-13 shows the mobility of control TFTs and FSA-TFTs when the channel length is 10 μm and 0.8 μm. The channel width is 10 μm. Table 3-4 shows detailed data about maximum mobility. The maximum mobility of FSA-TFTs are 33.96 cm^2/V-s and 32.01 cm^2/V-s when the channel length is 10 μm and 0.8 μm. The degradation of mobility from 10 μm and 0.8 μm is 1.95 cm^2/V-s. The maximum mobility of control TFTs is 29.58 cm^2/V-s and 23.03 cm^2/V-s when the channel length is 10 μm and 0.8 μm. The degradation of mobility from 10 μm and 0.8 μm is 6.55 cm^2/V-s. Clearly, the mobility degradation of control TFTs is more severe than that of FSA-TFTs. This can be explained from Fig. 3-14. Where A is the channel length, B is the S/D regions. When channel length is decreased, the serious S/D resistance becomes prominent. This will result in the across voltage of the channel region becomes smaller. When the lateral electrical field becomes smaller, the mobility becomes smaller. But fully Ni-salicidation can result in the decrease of parasitic resistance. So,

the mobility roll off of FSA-TFTs from 10 μm to 0.8 μm is not severe.

The off-state leakage currents in n-type device are measured for channel length of 10 μm and 0.8 μm at V_G=-5 V as shown in Fig. 3-15. Obviously, the leakage current of FSA-TFTs from 10 μm to 0.8 μm has little variation. However, the leakage current of control TFTs from 10 μm to 0.8 μm increases very quickly at V_D=8 V. This is because the fully Ni-salicidation can suppress parasitic BJT effect, the FSA-TFTs do not have severe GIDL enhancement current. About GIDL enhancement current is explained clearly in section 3.3.3.

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3.2 Basic electrical characteristics of FSA-TFTs (un-doped gate)

In this section, the electrical characteristics of control TFTs and FSA-TFTs (un-doped gate) with RTA 550°C 30-sec are compared.

The parasitic resistance (R_P) of the control TFTs is 7.521 kΩ. Figure 3-16 shows the parasitic resistance (R_P) of the FSA-TFTs. The value of R_P is 0.7224 kΩ. Obviously, the R_P of the FSA-TFTs with un-doped gate is much lower than that of the control TFTs.

Figure 3-17 exhibits I_D-V_G and field-effect mobility characteristics of the FSA-TFTs with W/L=10 μm/10 μm and Tox=500 Å. The drain bias is 0.5 V and 5.0 V.

The ON current at V_D=0.5 V and V_G=15 V of FSA-TFTs is 13 μA. The OFF current of FSA-TFTs is 0.1 pA. So, the ON/OFF current ratio is 1.3×10^8. The maximum mobility of the FSA-TFTs is 32.36 cm^2/V-s. All devices' parameters of the control TFTs and the FSA-TFTs are listed in the Table 3-5. Similar to the results of device with doped gate, ON current, ON/OFF current ratio, the maximum mobility of FSA-TFTs with un-doped gate is higher than those of control TFTs.

Figure 3-18 shows the comparison of I_D-V_G characteristics at V_D=0.5 V between control TFTs and FSA-TFTs with W/L=10 μm/10 μm. Figure 3-19 shows the comparison of mobility between control TFTs and FSA-TFTs with W/L =10 μm/10 μm. The fully Ni-salicidation remarkably improves the mobility of TFTs.

Figure 3-20 show I_D-V_D characteristics of control TFTs and FSA-TFTs with W/L= 10 μm/10 μm (V_G-V_{TH}=3.0 V, 4.0 V, 5.0 V, 6.0 V). The output current of FSA-TFTs is obviously larger than that of control TFTs.

Figure 3-21 shows I_D-V_D output characteristics of control TFTs and FSA-TFTs with W/L=10 μm/0.8 μm. The kink effect is observed.

Figure 3-22 exhibits V_{TH} roll off characteristics of control TFTs and FSA-TFTs. All threshold voltages of control TFTs and FSA-TFTs are summarized in Table 3-6. The threshold voltage roll off from 10 μm to 0.8 μm of control TFTs at V_D=0.5 V is 1.402 V. The threshold voltage roll off from 10 μm to 0.8 μm of FSA-TFTs at V_D= 0.5

V is 0.48 V. Obviously, threshold voltage roll off phenomenon of control TFTs is more severe than that of FSA-TFTs.

Figure 3-23 shows subthreshold swing (S.S.) roll off characteristics of control TFTs and FSA-TFTs. The drain bias is 5 V. The channel width is 10 μm. Table 3-7 shows detailed data about subthreshold swing from 10 μm to 0.8 μm. The S.S. roll off from 10 μm to 0.8 μm of control TFTs at V_D=5 V is 295.84 mV/dec. The S.S. roll off from 10 μm to 0.8 μm of FSA-TFTs at V_D=5 V is 172.17 mV/dec. Obviously, S.S. roll off phenomenon of control TFTs is more severe than that of FSA-TFTs.

Figure 3-24 shows the mobility of control TFTs and FSA-TFTs when the channel length is 10 μm and 0.8 μm. The channel width is 10 μm. Table 3-8 shows detailed data about maximum mobility. The maximum mobility of FSA-TFTs is 32.36 cm^2/V-s and 29.46 cm^2/V-s in the channel length of 10 μm and 0.8 μm. The degradation of mobility from 10 μm and 0.8 μm is 2.9 cm^2/V-s. The degradation of mobility from 10 μm and 0.8 μm is 6.55 cm^2/V-s in the control TFTs. Clearly, the mobility degradation of control TFTs is more severe than that of FSA-TFTs.

The off-state leakage currents in n-type device are measured for channel length of 10 μm and 0.8 μm at V_G=-5 V as shown in Fig. 3-25. Obviously, the leakage current of FSA-TFTs from 10 μm to 0.8 μm has much less variation. However, the leakage current of control TFTs from 10 μm to 0.8 μm increases significantly at V_D=8

V. So, the FSA-TFTs does not have severe GIDL enhancement current.

Figure 3-26 shows the GIDL enhancement current for in-situ doped gate and un-doped gate FSA-TFTs with W/L=10 μm/10 μm. The gate voltage is -5 V. The GIDL enhancement current of FSA-TFTs (un-doped gate) is higher than that of FSA -TFTs (in-situ doped gate). The doping of the poly-Si gate prior to complete gate silicidation affects the NiSi workfunction. The different dopant's amount can tune the work function of NiSi [29]. Different work function of NiSi results in the larger leakage for FSA-TFTs with un-doped gate.

3.3 Analysis of the poly-Si TFT's electrical characteristics

In this section, some electrical characteristics of devices will be discussed, including the reduction of V_{TH} using the S/D fully salicidation processes, kink effect, Gate-Induced-Drain-Leakage (GIDL) enhancement current.

3.3.1 The reduction of V_{TH} using the S/D fully salicidation processes

Fully Ni-salicidation in the S/D region can result in the reduction of the threshold voltage. In the following, a equivalent circuit model is used to explain this phenomenon in Fig.3-27 [33]. A source resistance R_S and a drain resistance R_D are assumed to connect an intrinsic TFT to the external terminals where V_{DS} and V_G are applied. The internal voltages are V'_{DS} and V'_G for the intrinsic TFT. The following

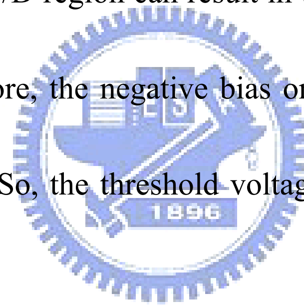
relations are :

$$V'_{DS}=V_{DS}-(R_S+R_D)I_{DS} \text{ ---------------------------------- (Eq. 3.1)}$$

$$V'_{G}=V_{G}-R_S \times I_{DS} \text{ -- (Eq. 3.2)}$$

As shown in Fig. 3-27, an actual device with parasitic resistance is equivalent to an intrinsic TFT with a grounded source, with V'_G and V'_{DS} at the gate and the drain terminals, and with a negative bias $-R_S I_{DS}$ on the substrate. A negative bias on the substrate leads to the body effect. This phenomenon results in the higher threshold voltage.

Fully Ni-salicide in the S/D region can result in the drastic decrease of the series resistance R_S and R_D. Therefore, the negative bias on the substrate is decreased and the body effect is alleviated. So, the threshold voltage of TFTs could be reduced by the Ni-salicidation process.



3.3.2 Kink effect

The output characteristics exhibit an anomalous current increase in the saturation region. The kink effect is observed. The kink effect in TFTs is showed in Fig. 3-28. The short gate length and high drain bias result in the lateral electric field becomes stronger. The stronger lateral electric field causes impact ionization near the drain, generating more electron-hole pairs. Due to impact ionization occurring at the drain end of the channel, holes are injected into the floating body. The presence of these holes raises the body potential, which may become large enough to forward bias the

body-source. The hole current flowing into the source forces the electron injection from the source into the body. These electrons flow along the electric field into the drain region. This added drain current augments impact ionization which forward biases the floating body harder. The entire process is like a positive feedback to make the problem serious.

Because FSA-TFT's source region can be used as a sink for holes [30], holes in the floating body do not accumulate. So, FSA-TFT's kink effect is not more severe than that of control TFTs.

3.3.3 Gate-Induced-Drain-Leakage (GIDL) enhancement current

GIDL is the off-state leakage current, which occurs when the gate potential is very low or negative and a high drain potential is applied [34]. The leakage current is the tunneling current in the deep depletion region due to the high vertical electric field. Fig. 3-29 shows the energy band diagram about the tunneling current. The tunneling theory predicts that

$$I_D = A E_S \exp(-B/E_S) \quad \text{(Eq. 3.3)}$$

Where A is a pre-exponential constant and B has a theoretical value of 21.3MV/cm. E_S is the surface electric field.

In the n-type TFTs, holes generated on the surface of drain by band-to-band tunneling mechanism are swept into the floating body. The floating body potential

rises and becomes forward biased with respect to source (i.e. as emitter). The parasitic npn bipolar therefore enters into forward active mode. The GIDL current, thus, serves as the base current for the lateral bipolar transistor as shown in Fig. 3-30. The resultant current near the drain junction is thus given by

$$I_D=\beta I_{GIDL}+I_{GIDL}=(\beta+1)I_{GIDL} \qquad \text{(Eq. 3.4)}$$

Where β is the gain of the lateral BJT.

The current gain of the lateral BJT increases as the base width decreases. Therefore, for short channel devices, β is significant, which is not the case with long channel devices. In our above result, we have shown that control TFT's GIDL current from 10 μm to 0.8 μm is more severe than that of FSA-TFTs. Hence, Ni-salicidation has demonstrated as a very promising technology to eliminate this lateral bipolar transistor effect.

Table 3-1 Summary of parameters of control TFTs and FSA-TFTs (in-situ doped gate, RTA 550°C 30-sec) with W/L=10 μm/10 μm and V_D=0.5 V.

	V_{TH} (V)	**S.S. (mV/dec)**	**μ_{FE} (cm^2/V-s)**	**I_{ON} (μA)**	**I_{OFF} (pA)**	**I_{ON}/I_{OFF} ratio**
Control TFTs	**1.61**	**746.28**	**29.58**	**12.68**	**1.25**	**1.01×10^7**
FSA-TFTs	**1.05**	**371.71**	**33.96**	**14.44**	**0.1**	**1.44×10^8**

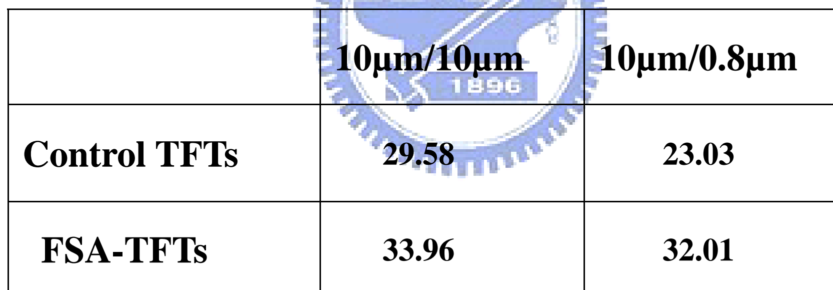
Table 3-2 V_{TH} (V) roll off of control TFTs and FSA-TFTs (in-situ doped gate, RTA 550°C 30-sec).

	10μm/ 10μm	**10μm/ 5μm**	**10μm/ 3μm**	**10μm/ 2μm**	**10μm/ 1μm**	**10μm/ 0.8μm**
Control TFTs V_D=0.5V	**1.61**	**1.18**	**0.618**	**0.557**	**0.217**	**0.208**
Control TFTs V_D=5V	**1.41**	**0.979**	**0.375**	**0.184**	**-0.79**	**-1.1**
FSA-TFTs V_D=0.5V	**1.05**	**0.993**	**0.987**	**0.932**	**0.779**	**0.68**
FSA-TFTs V_D=5V	**0.982**	**0.89**	**0.887**	**0.737**	**0.173**	**-0.04**

Table 3-3 Subthreshold swing (mV/dec) roll off of control TFTs and FSA -TFTs (in-situ doped gate, RTA 550°C 30-sec) with V_D=**5 V**.

	10μm/ 10μm	**10μm/ 8μm**	**10μm/ 5μm**	**10μm/ 3μm**	**10μm/ 2μm**	**10μm/ 1μm**	**10μm/ 0.8μm**
Control TFTs	**727.82**	**724.12**	**700**	**685.79**	**614.57**	**495.59**	**431.98**
FSA-TFTs	**340.5**	**333**	**328.57**	**328**	**290**	**203.4**	**192.46**

Table 3-4 Maximum mobility (cm^2/V-s) of control TFTs and FSA-TFTs (in-situ doped gate, RTA 550°C 30-sec).



	10μm/10μm	10μm/0.8μm
Control TFTs	**29.58**	**23.03**
FSA-TFTs	**33.96**	**32.01**

Table 3-5 Summary of parameters of control TFTs and FSA-TFTs (un-doped gate, RTA 550°C 30-sec) with W/L=10 μm/10 μm and V_D=0.5 V.

	V_{TH} (V)	S.S. (mV/dec)	μ_{FE} (cm^2/V-s)	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF} ratio
Control TFTs	**1.61**	**746.28**	**29.58**	**12.68**	**1.25**	**1.01×10^7**
FSA-TFTs	**1.69**	**396**	**32.36**	**13**	**0.1**	**1.3×10^8**

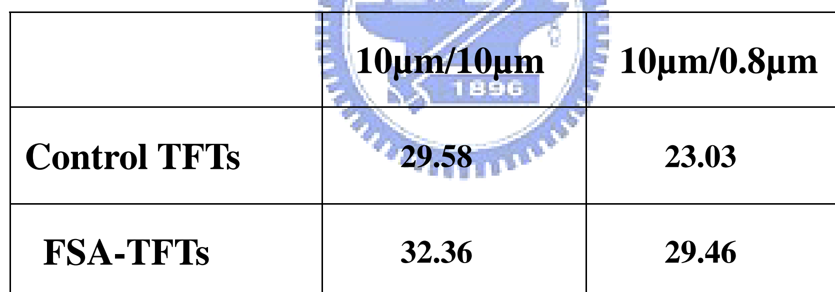
Table 3-6 V_{TH} (V) roll off of control TFTs and FSA-TFTs (un-doped gate, RTA 550°C 30-sec).

	10μm/ 10μm	10μm/ 5μm	10μm/ 3μm	10μm/ 2μm	10μm/ 1μm	10μm/ 0.8μm
Control TFTs V_D=0.5V	1.61	1.18	0.618	0.557	0.217	0.208
Control TFTs V_D=5V	1.41	0.979	0.375	0.184	-0.79	-1.1
FSA-TFTs V_D=0.5V	1.69	1.68	1.62	1.56	1.36	1.21
FSA-TFTs V_D=5V	1.57	1.52	1.35	1.17	0.784	0.51

Table 3-7 Subthreshold swing (mV/dec) roll off of control TFTs and FSA-TFTs (un-doped gate, RTA 550°C 30-sec) with V_D=**5 V**.

	10µm/ 10µm	**10µm/ 8µm**	**10µm/ 5µm**	**10µm/ 3µm**	**10µm/ 2µm**	**10µm/ 1µm**	**10µm/ 0.8µm**
Control TFTs	**727.82**	**724.12**	**700**	**685.79**	**614.57**	**495.59**	**431.98**
FSA-TFTs	**376.5**	**375.13**	**372.2**	**350**	**301**	**228.1**	**204.33**

Table 3-8 Maximum mobility ($cm^2/V\text{-}s$) of control TFTs and FSA-TFTs (un-doped gate, RTA 550°C 30-sec).



	10μm/10μm	10μm/0.8μm
Control TFTs	**29.58**	**23.03**
FSA-TFTs	**32.36**	**29.46**

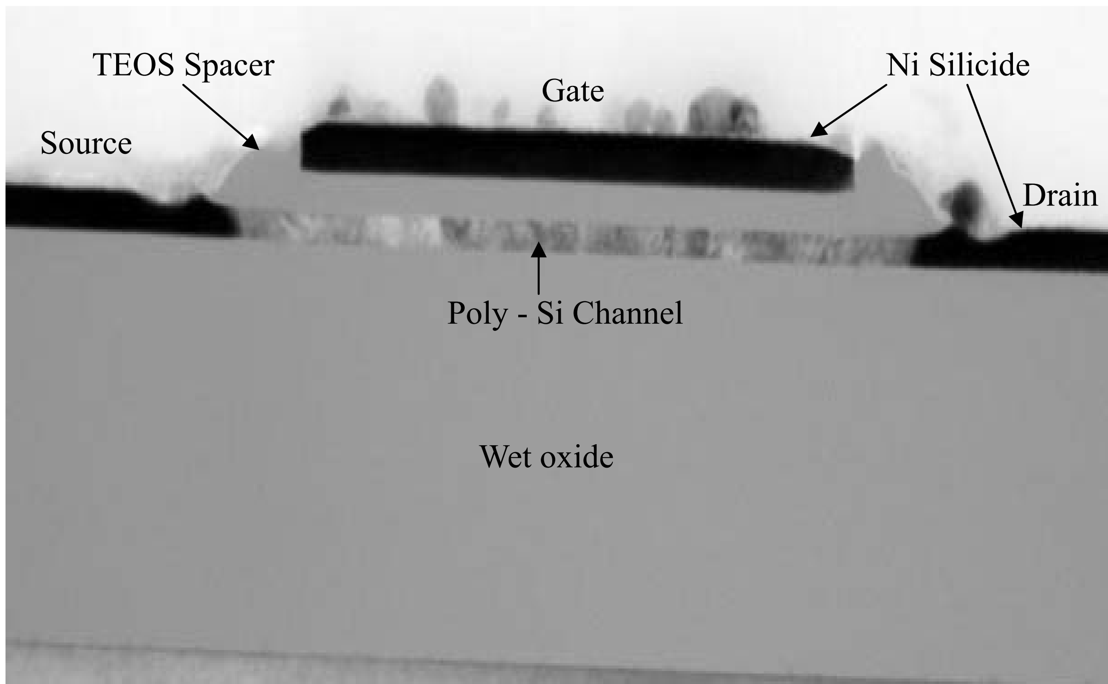
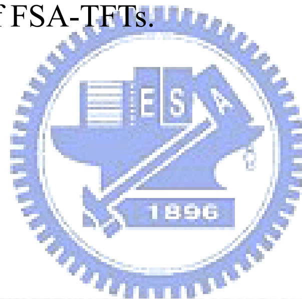


Fig. 3-1 Cross-section TEM of FSA-TFTs.



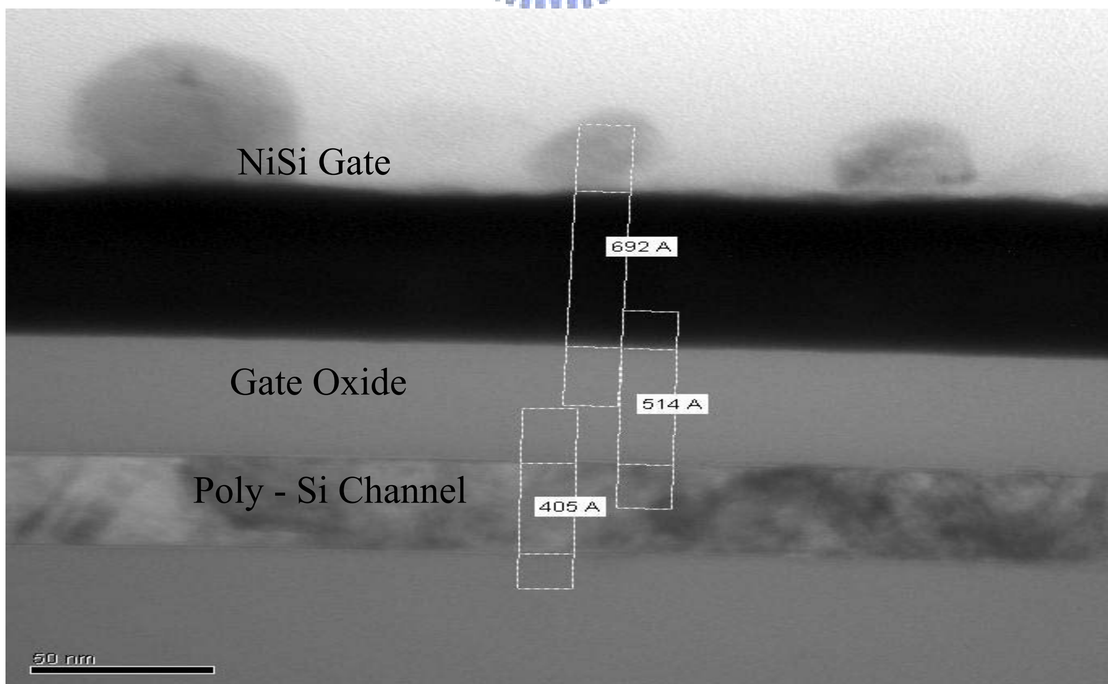


Fig. 3-2 Thickness of Poly-Si channel film, Gate oxide and NiSi gate.

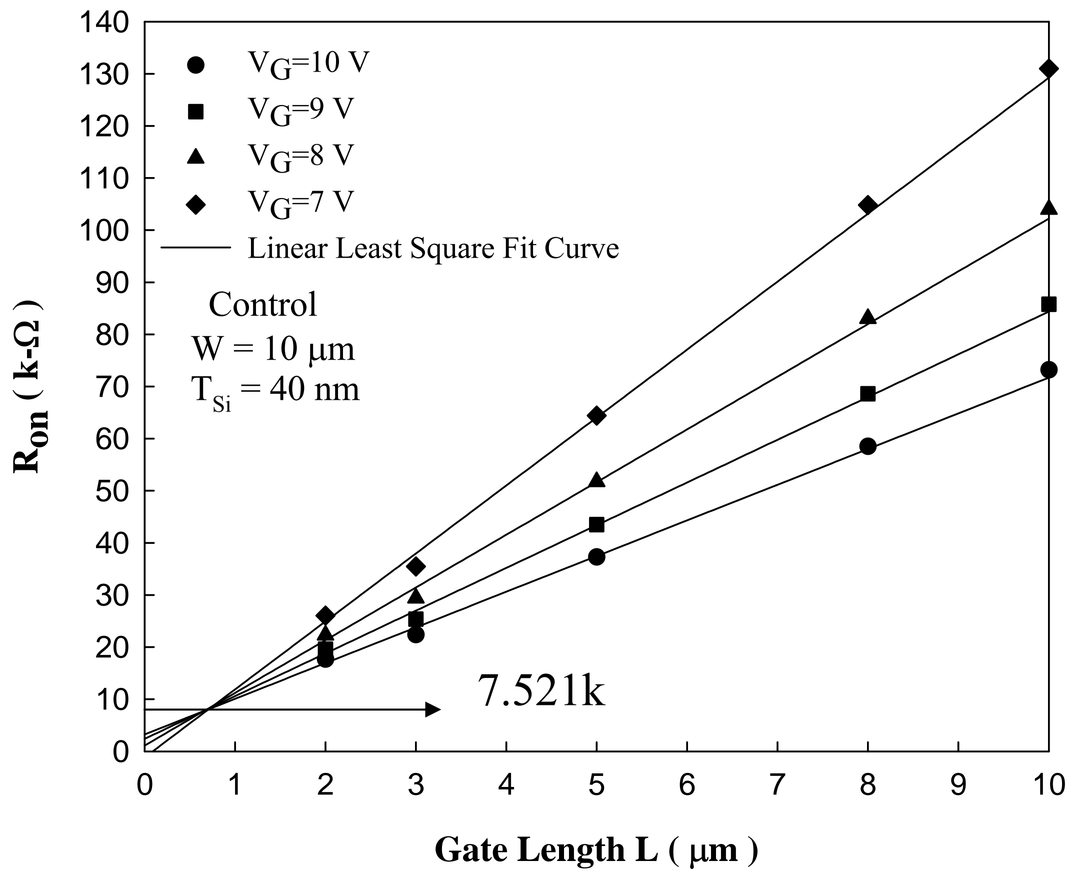


Fig. 3-3 Parasitic resistance Rp is extracted from the I_D-V_G of control TFTs

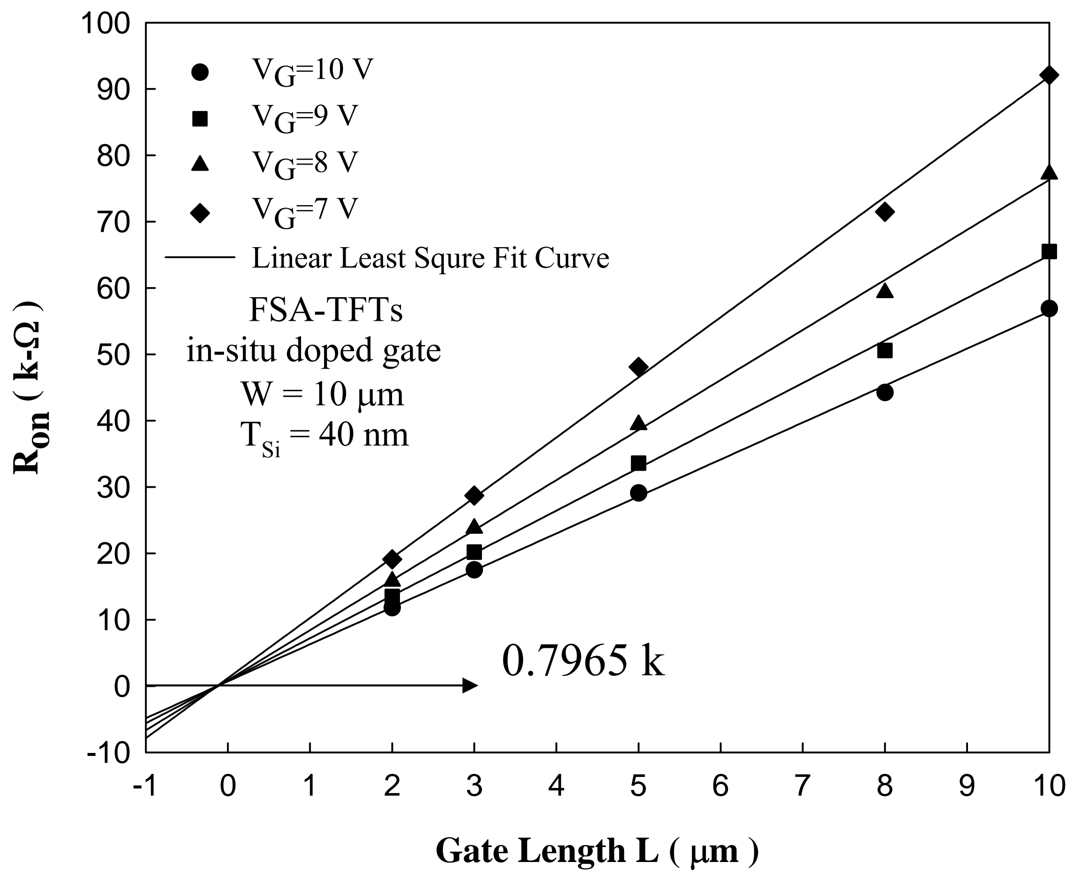


Fig. 3-4 Parasitic resistance R_P is extracted from the I_D-V_G of FSA-TFTs (in-situ doped gate).

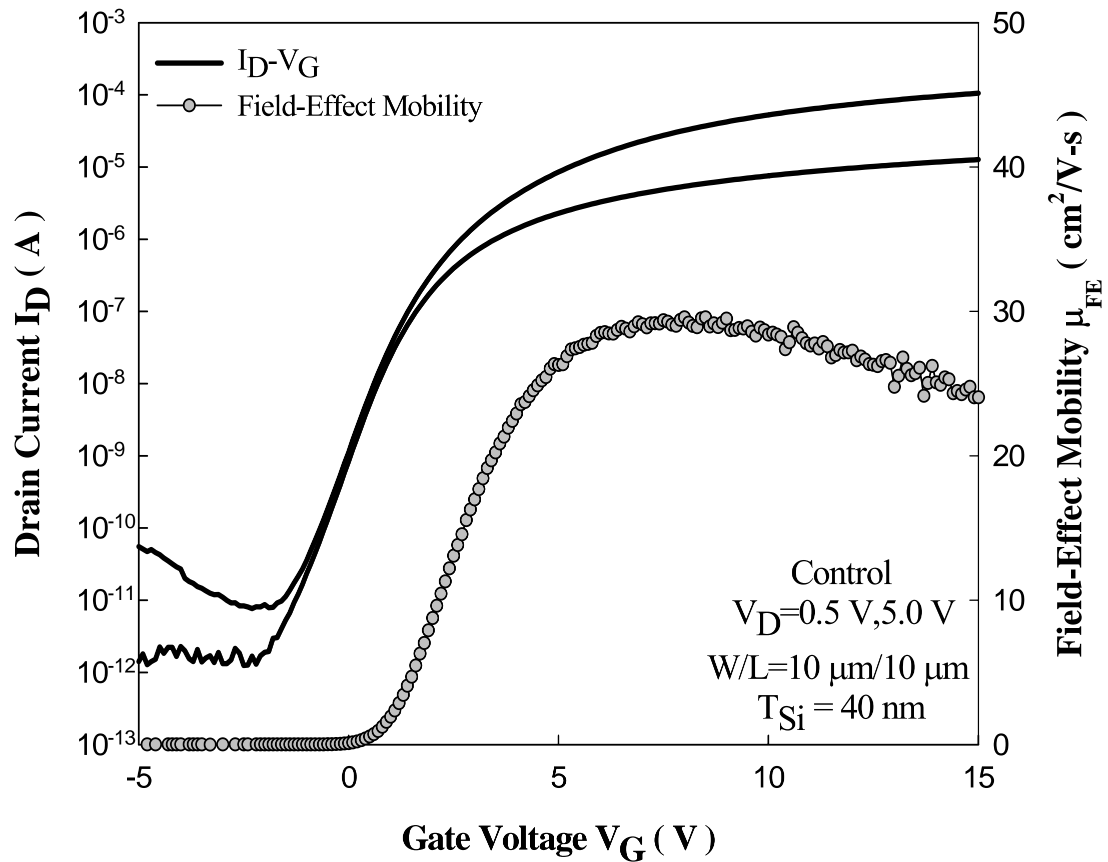


Fig. 3-5 I_D-V_G and field-effect mobility characteristics of control TFTs with W/L=10 μm/10 μm and T_{OX}=500 Å.

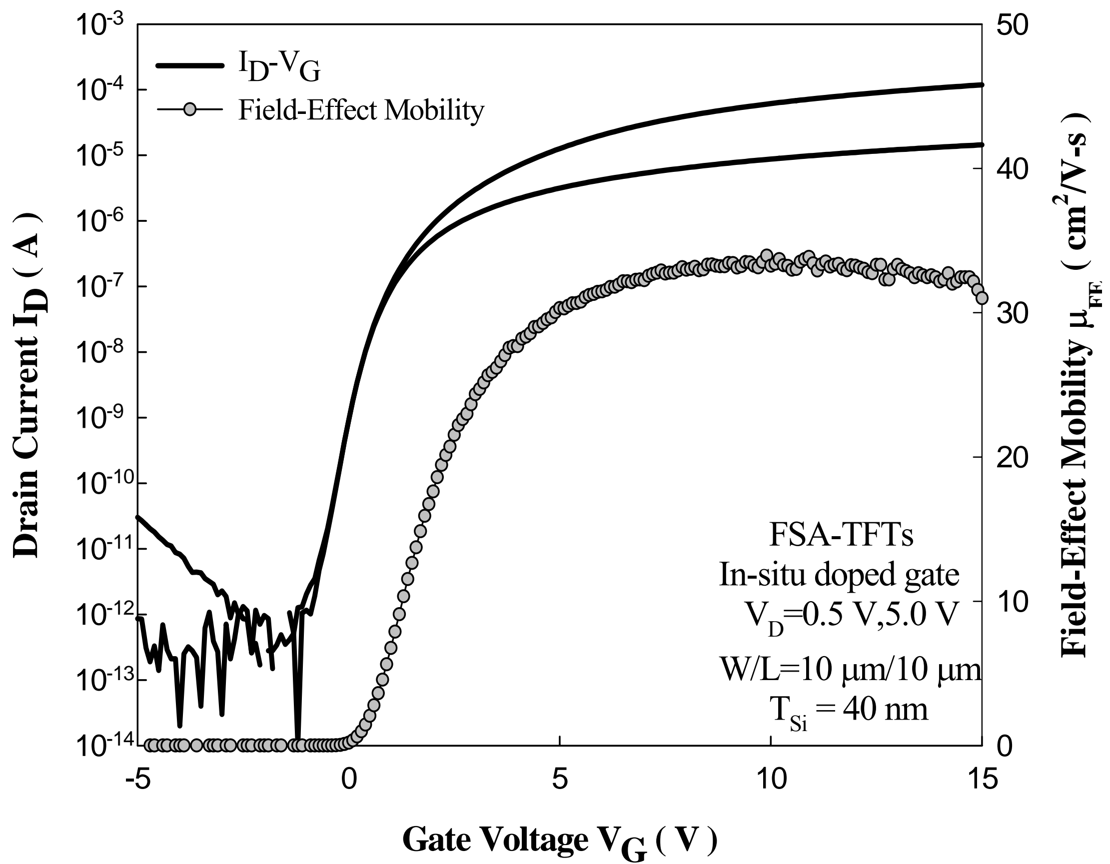


Fig. 3-6 I_D-V_G and field-effect mobility characteristics of FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm and T_{OX}=500 Å.

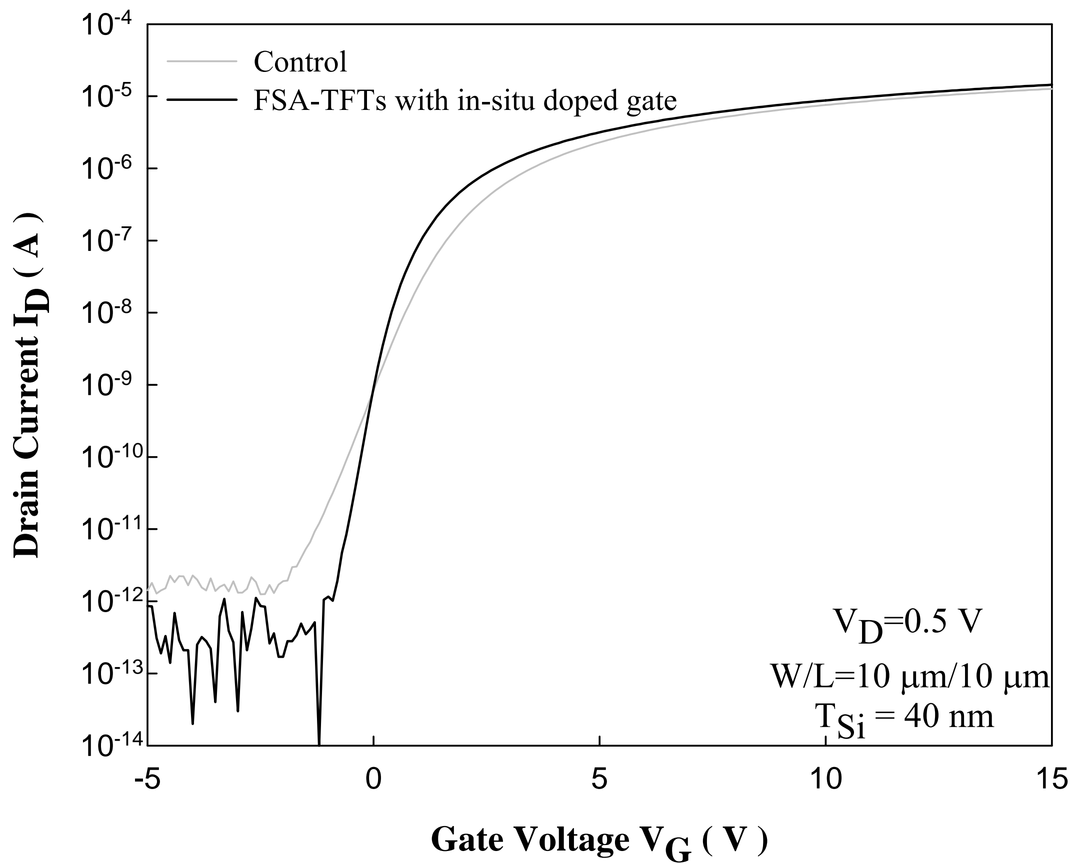


Fig. 3-7 Comparison of I_D-V_G characteristics between control TFTs and FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm and V_D=0.5 V.

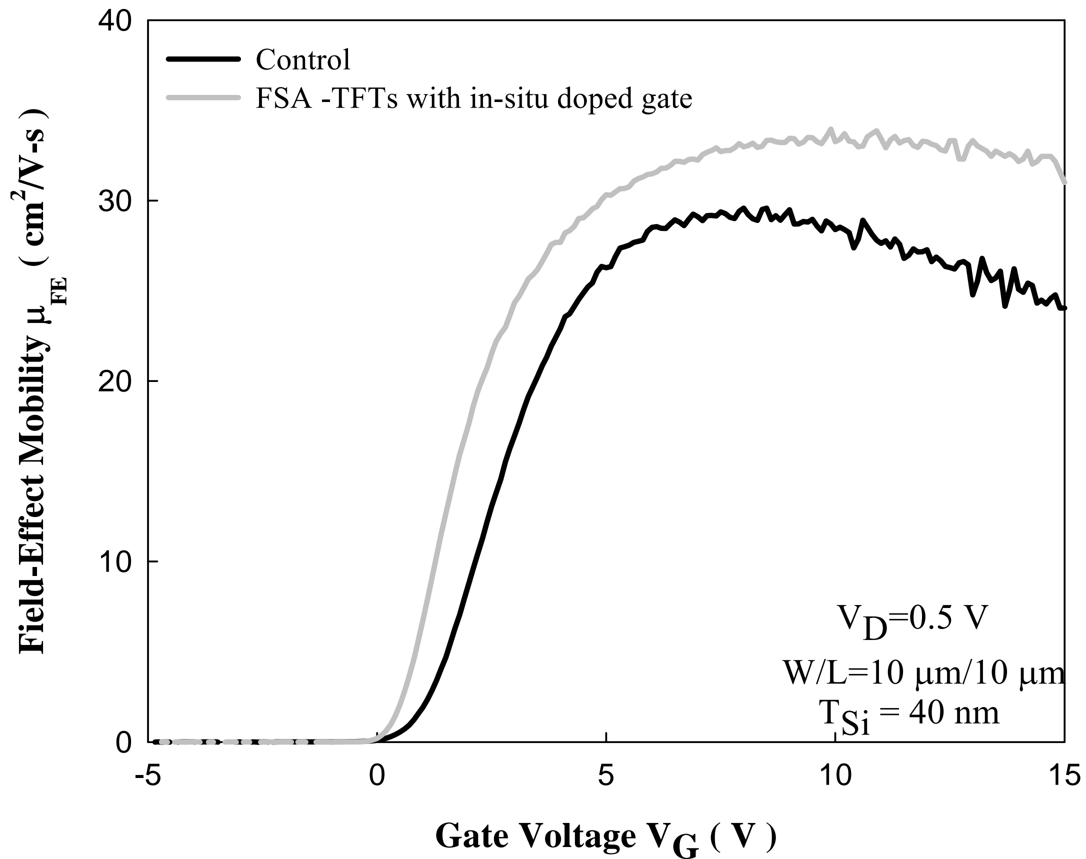


Fig.3-8 The mobility is plotted versus gate voltage at V_D=0.5V for both control TFTs and FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm. The peak mobility is 29.58 cm^2/V-s for control TFTs and 33.96 cm^2/V-s for FSA-TFTs.

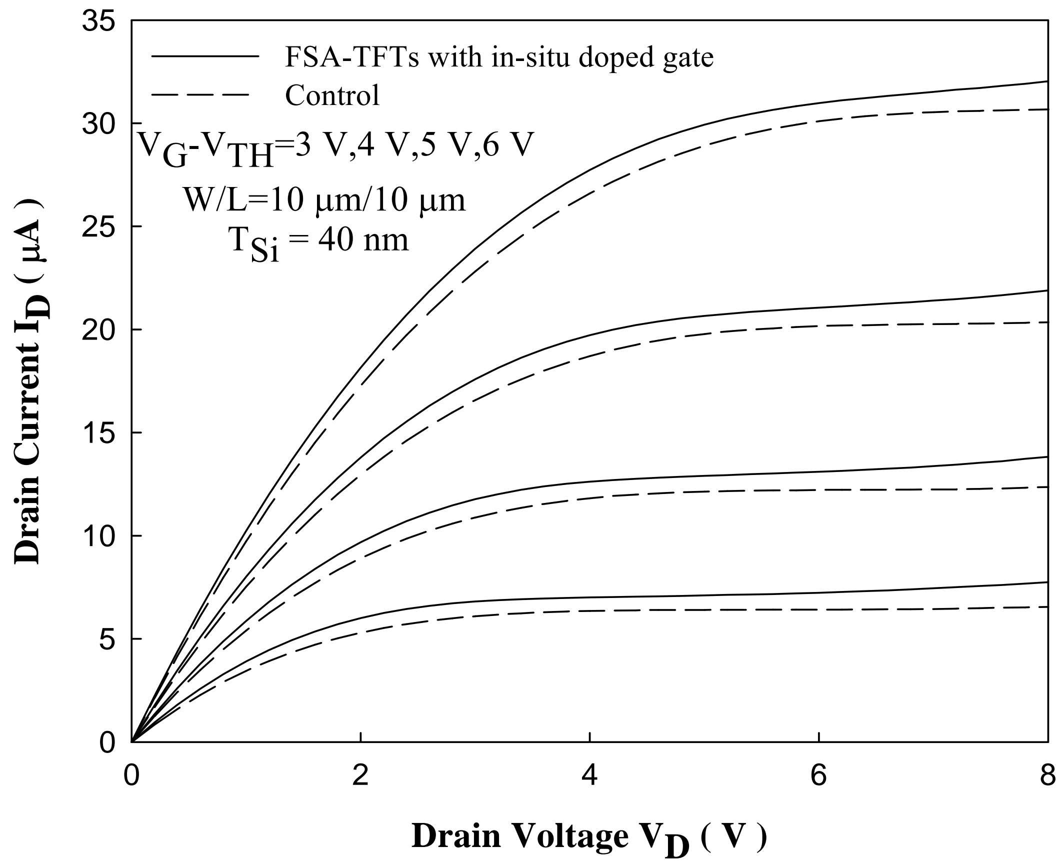


Fig. 3-9 I_D-V_D characteristics of control TFTs and FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm. V_G-V_{TH}=3.0 V, 4.0 V, 5.0 V, 6.0 V.

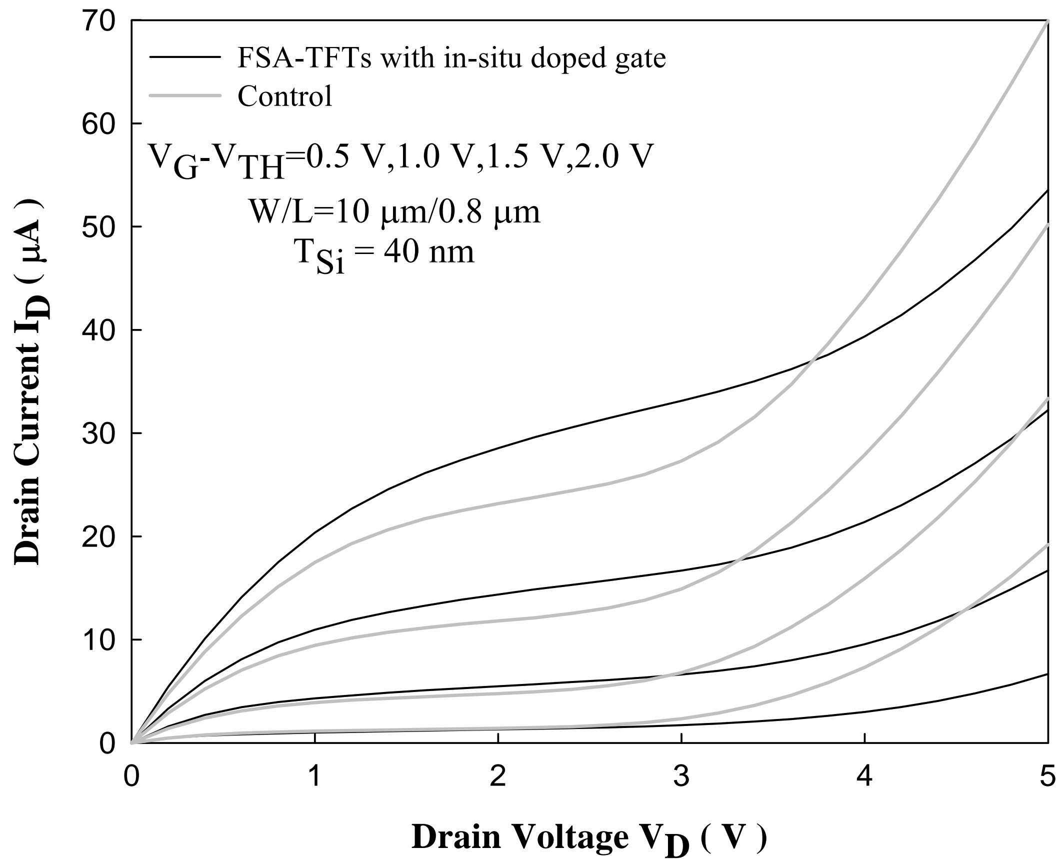


Fig. 3-10 I_D-V_D output characteristics of control TFTs and FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm. V_G-V_{TH}=0.5 V, 1.0 V, 1.5 V, 2.0 V. Note that kink effect is observed at high drain bias.

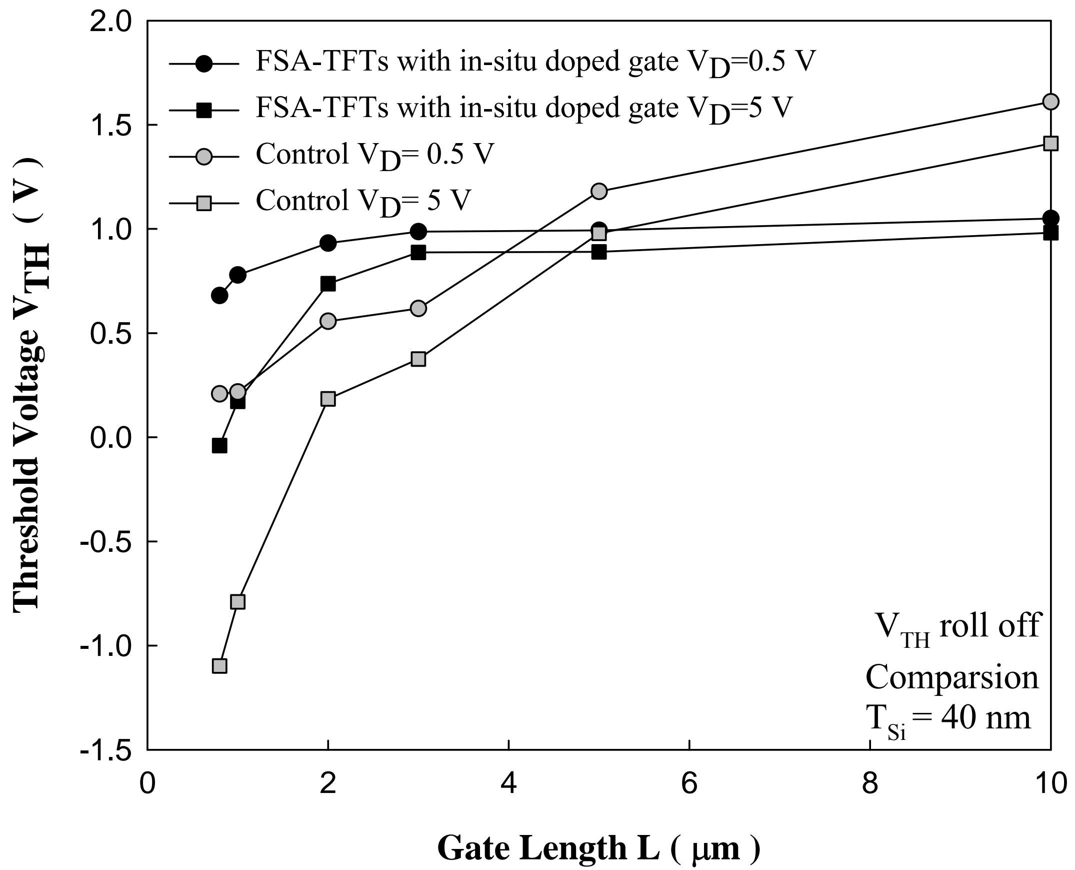


Fig. 3-11 Threshold voltage roll off vs. channel length. The channel width is 10 μm. The drain voltage is 0.5 V and 5 V.

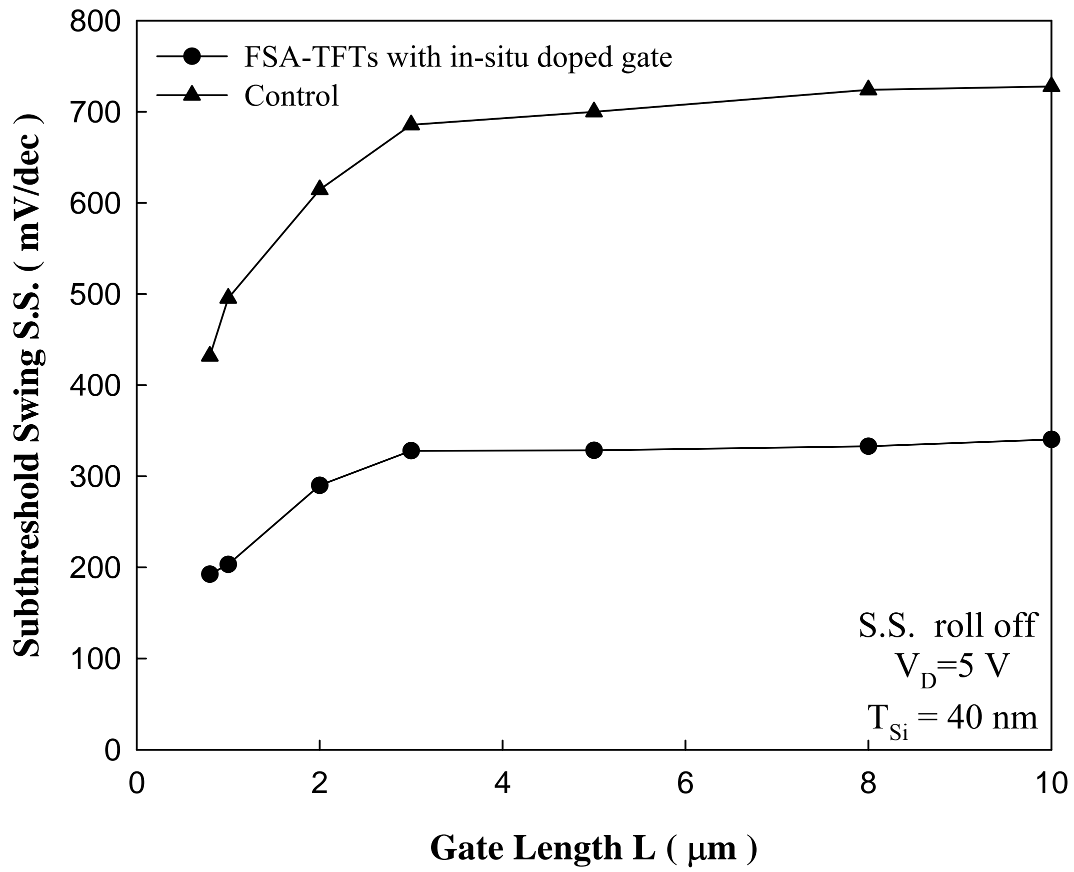


Fig. 3-12 Subthreshold Swing roll off vs. channel length. The channel width is 10 μm. The drain voltage is 5 V.

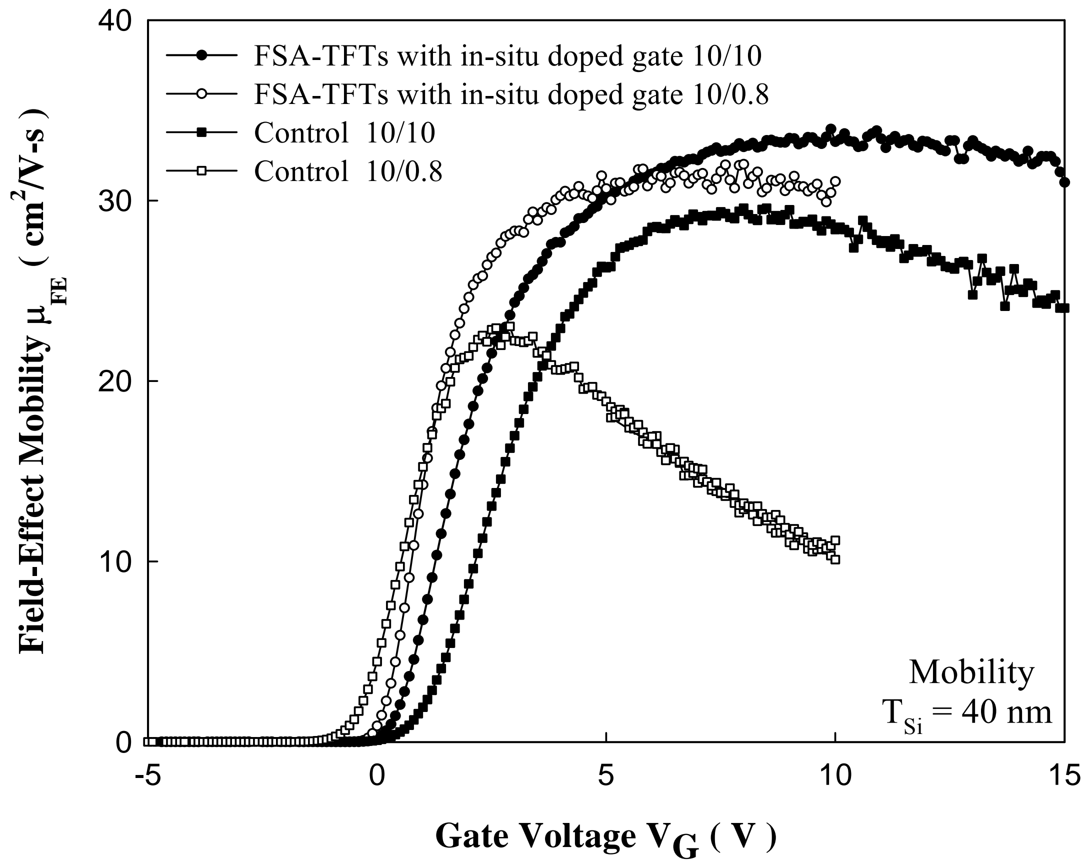


Fig.3-13 The mobility is plotted versus gate voltage for both control TFTs and FSA -TFTs (in-situ doped gate) with W/L=10 μm/10 μm and W/L=10 μm/0.8 μm.

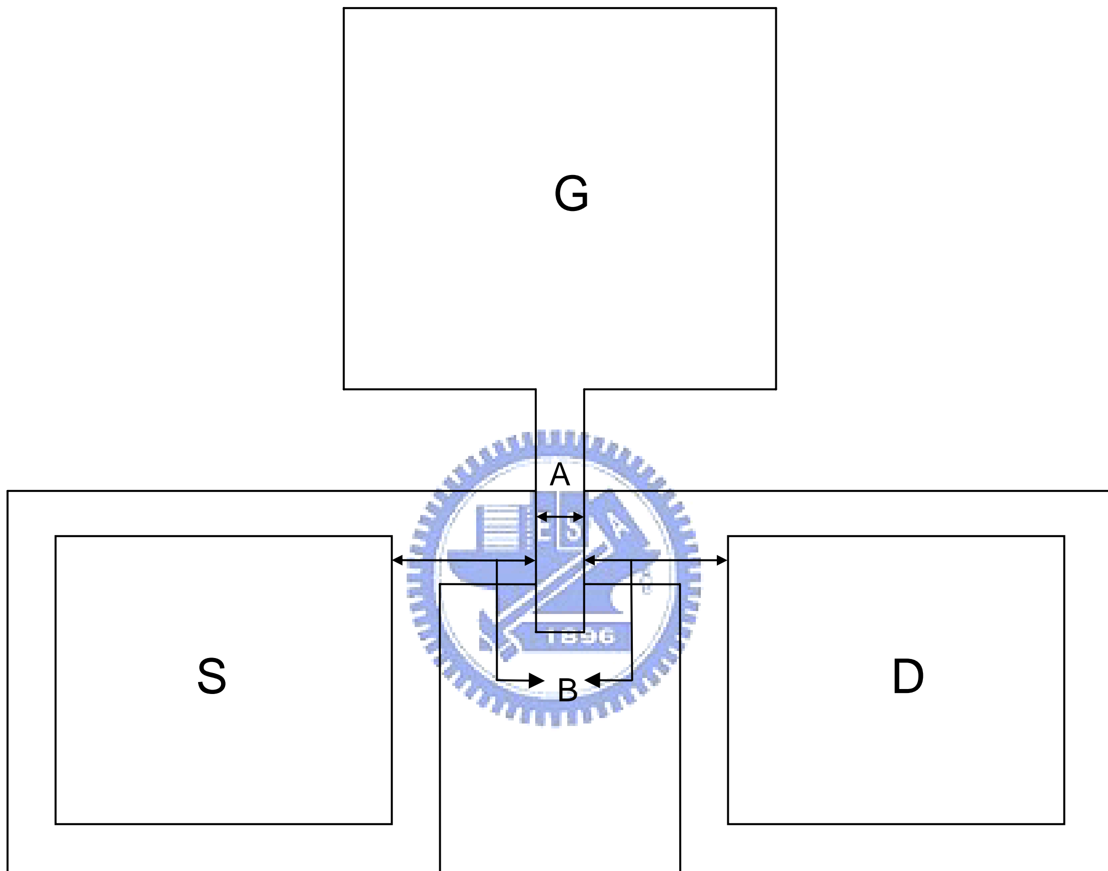


Fig.3-14 Schematic structure of device layout

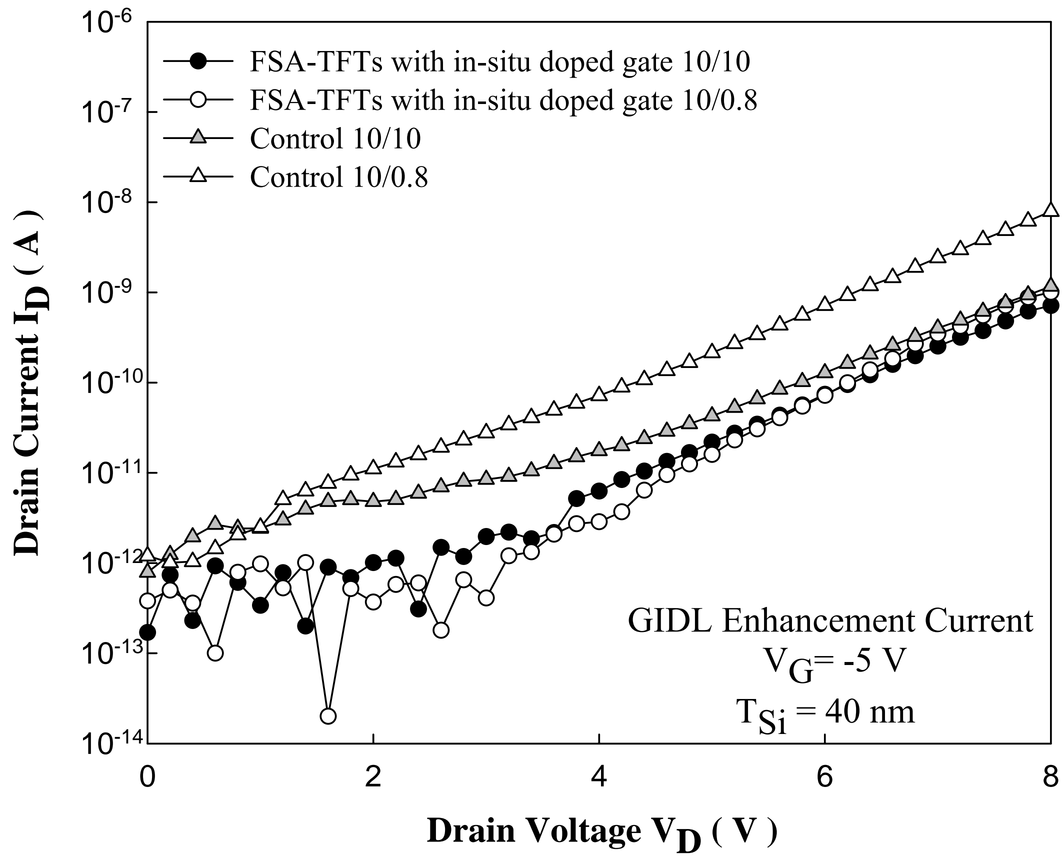


Fig.3-15 The GIDL enhancement current for both control TFTs and FSA-TFTs (in-situ doped gate) with W/L=10 μm/10 μm and W/L=10 μm/0.8 μm.

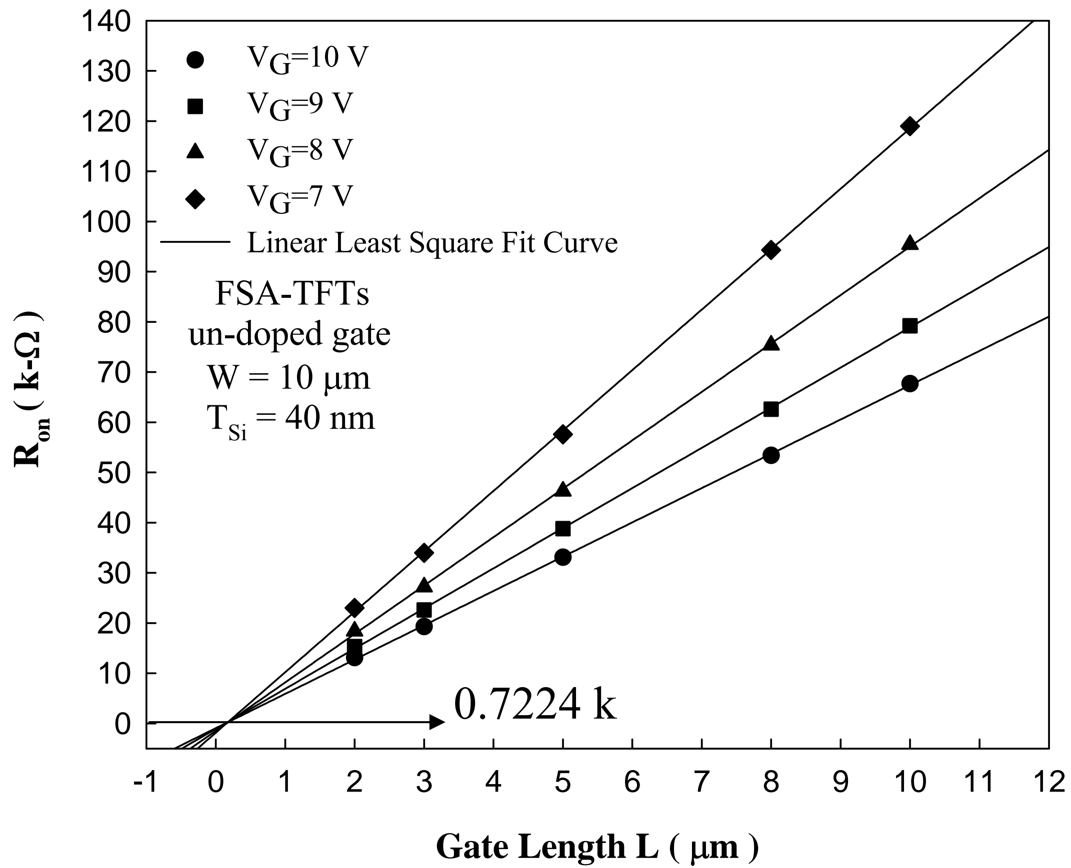


Fig. 3-16 Parasitic resistance Rp is extracted from the I_D-V_G of FSA-TFTs (un-doped gate).

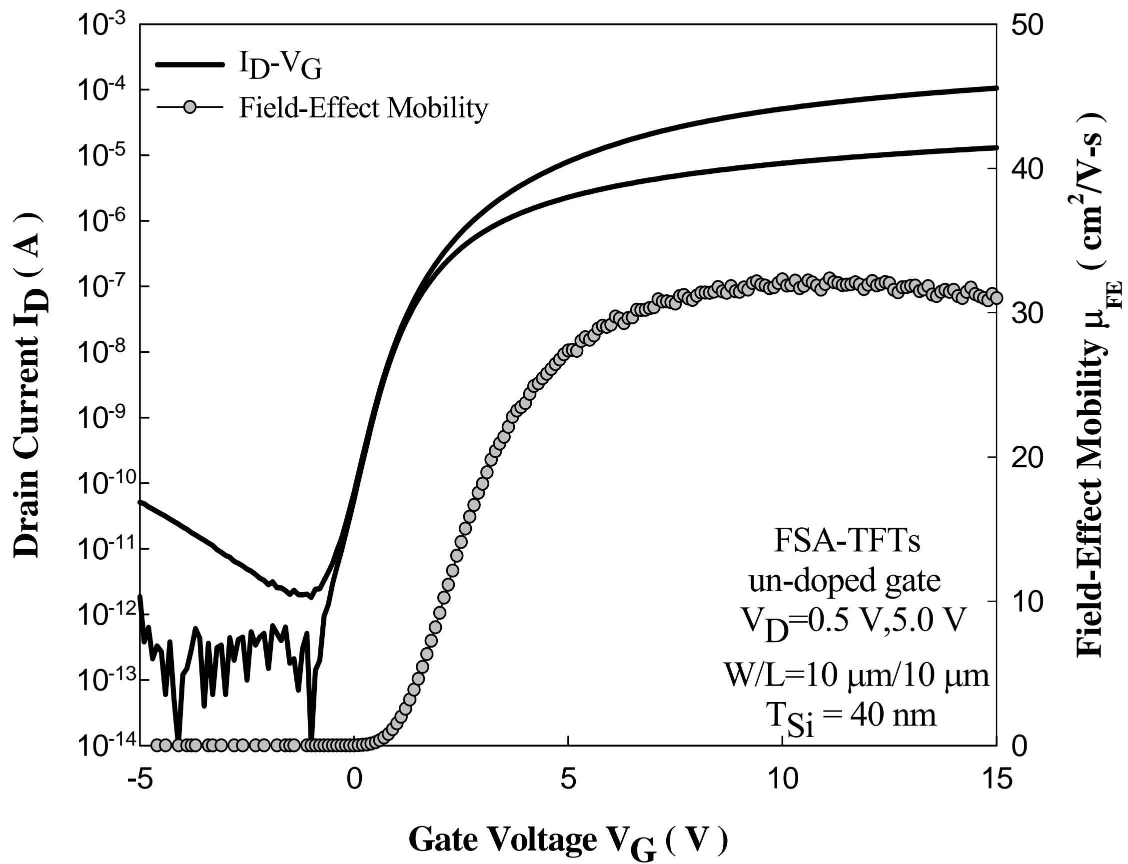


Fig. 3-17 I_D-V_G and field-effect mobility characteristics of FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm and T_{OX}=500 Å.

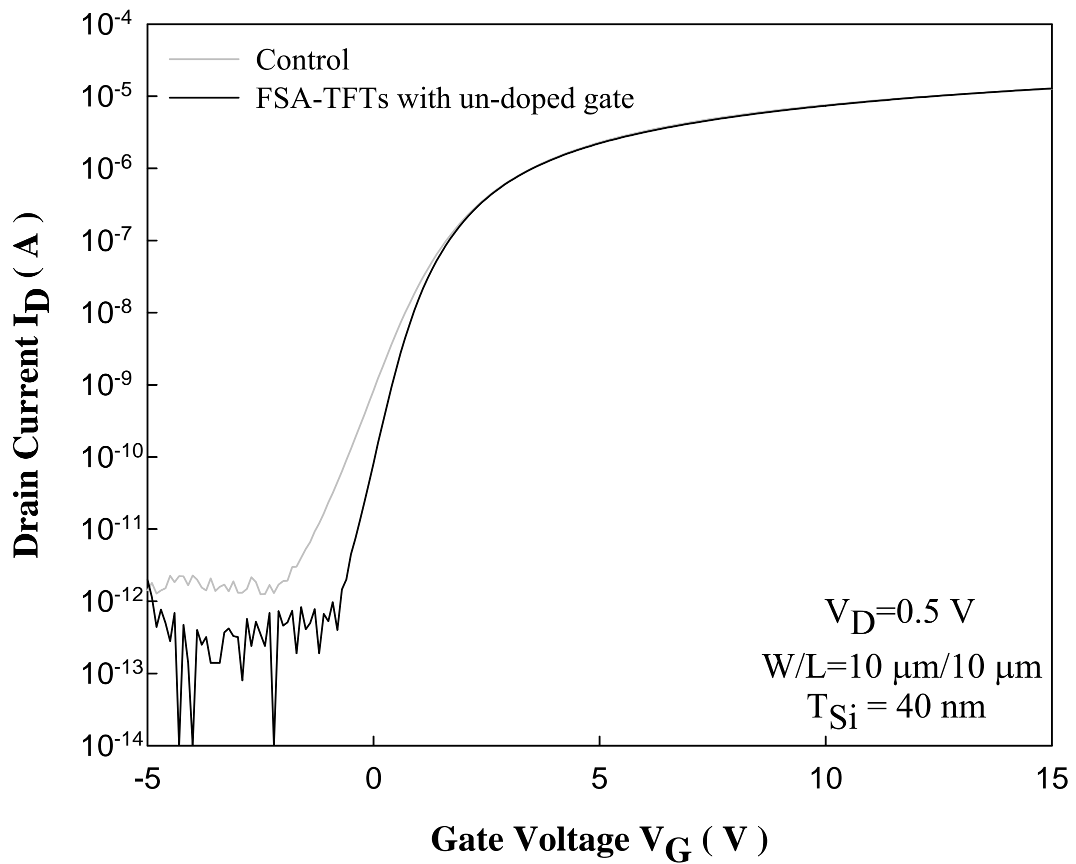


Fig. 3-18 Comparison of I_D-V_G characteristics between control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm and at V_D=0.5 V.

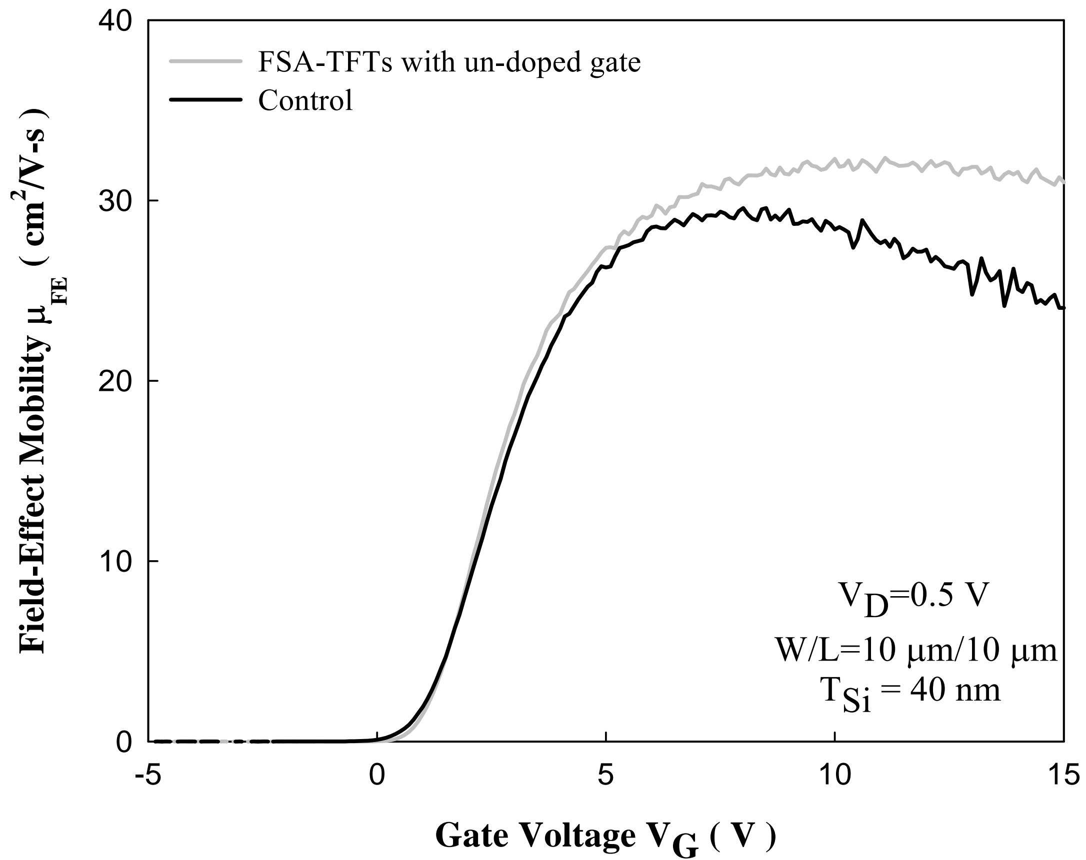


Fig.3-19 The mobility is plotted versus gate voltage at V_D=0.5 V for both control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm. The peak mobility is 29.58 cm^2/V-s for control TFTs and 32.36 cm^2/V-s for FSA-TFTs.

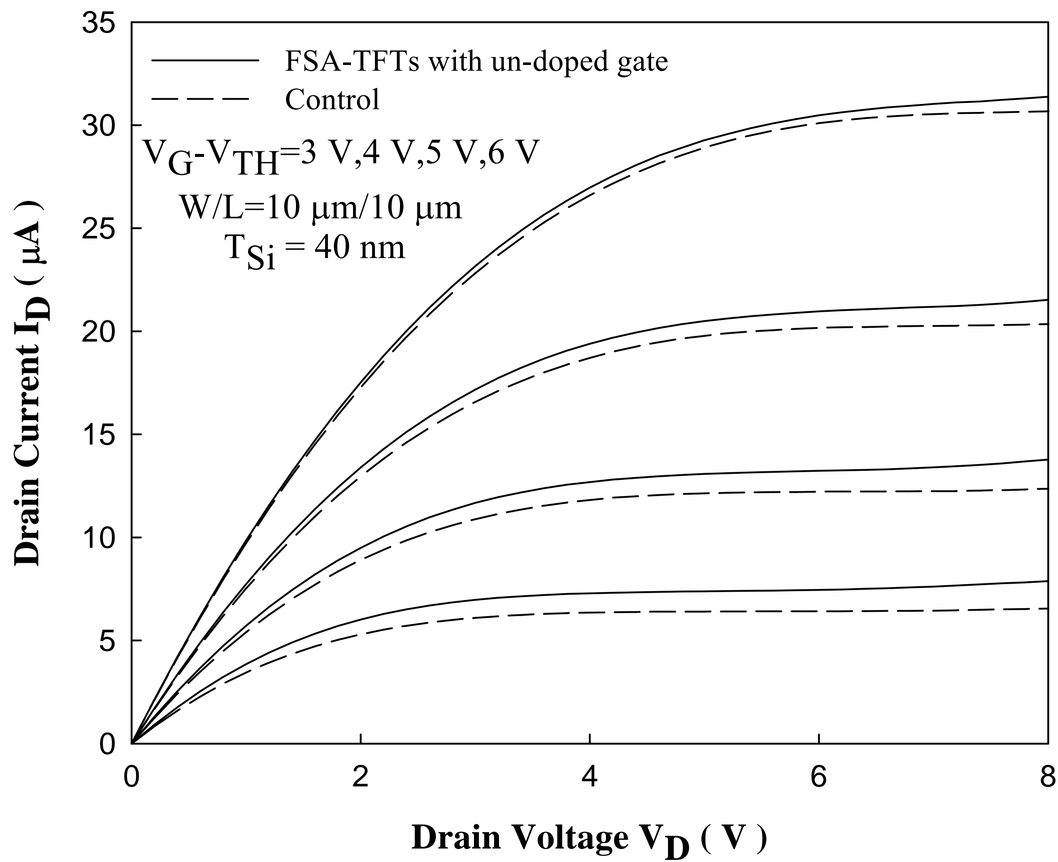


Fig. 3-20 I_D-V_D characteristics of control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm. V_G-V_{TH}=3.0 V, 4.0 V, 5.0 V, 6.0 V.

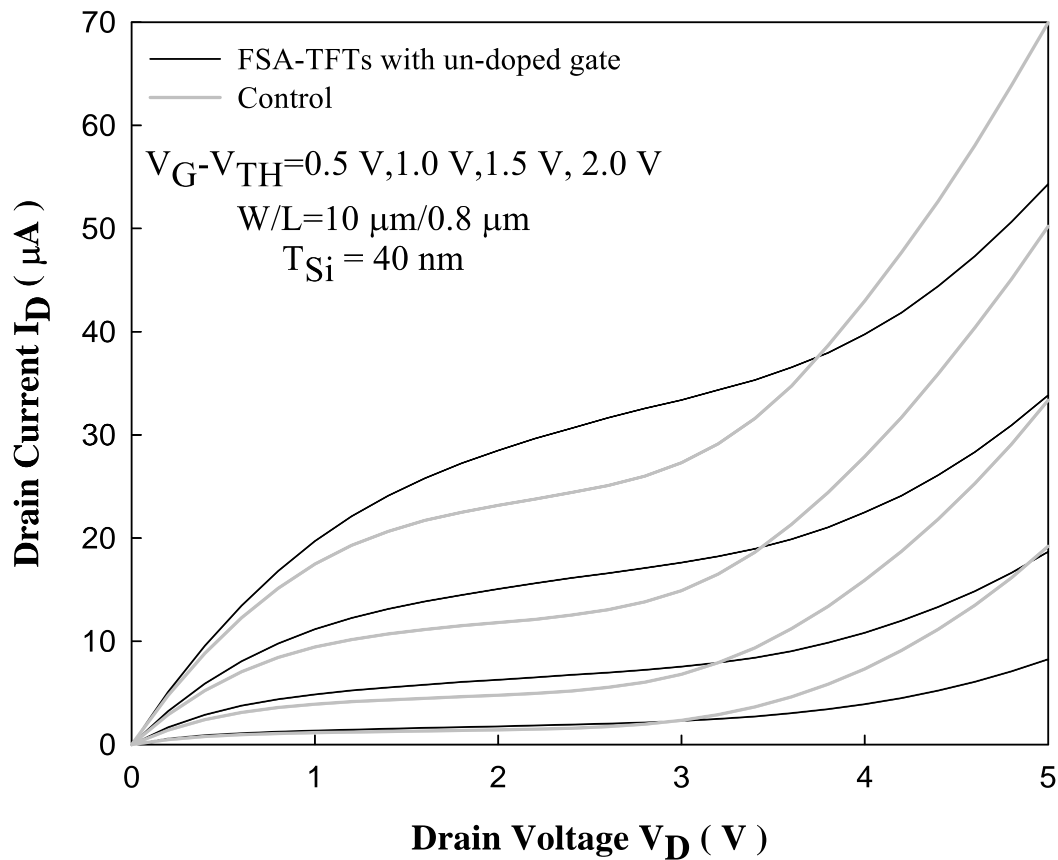


Fig. 3-21 I_D-V_D output characteristics of control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm. V_G-V_{TH}=0.5 V, 1.0 V, 1.5 V, 2.0 V. Note that kink effect is observed at high drain bias.

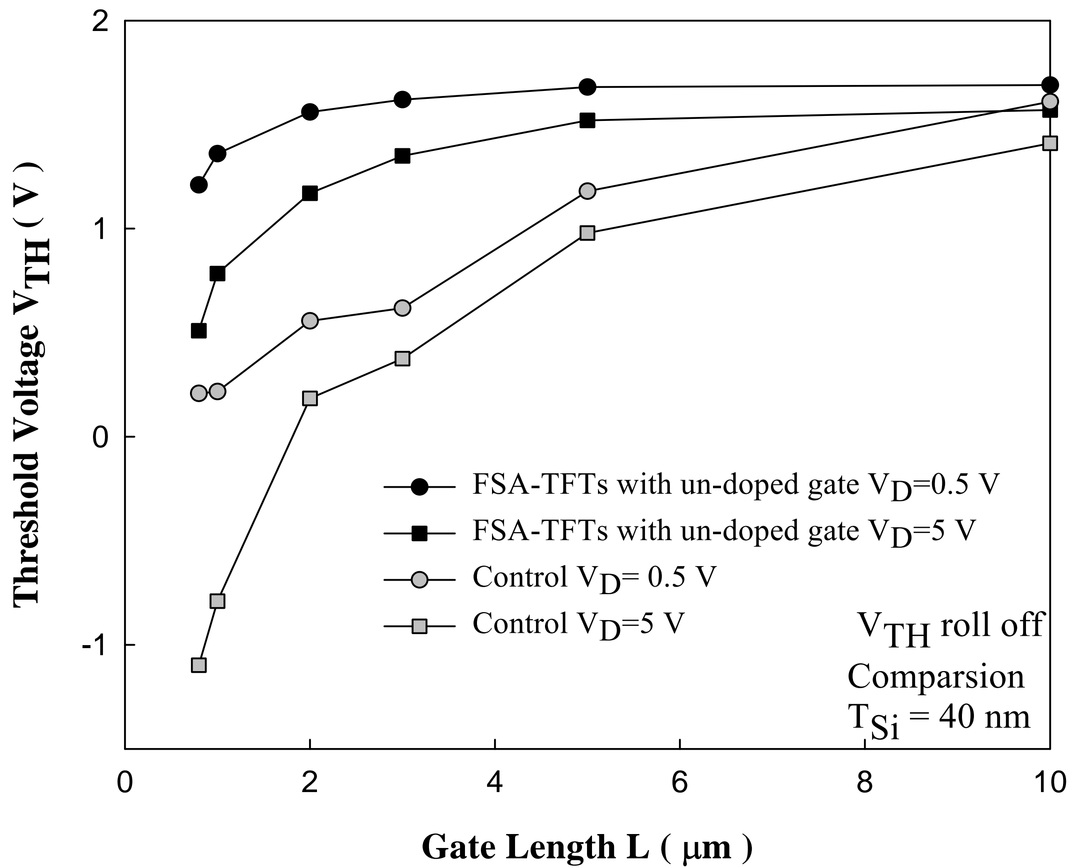


Fig. 3-22 Threshold voltage roll off vs. channel length. The channel width is 10 μm. The drain voltage is 0.5 V and 5 V.

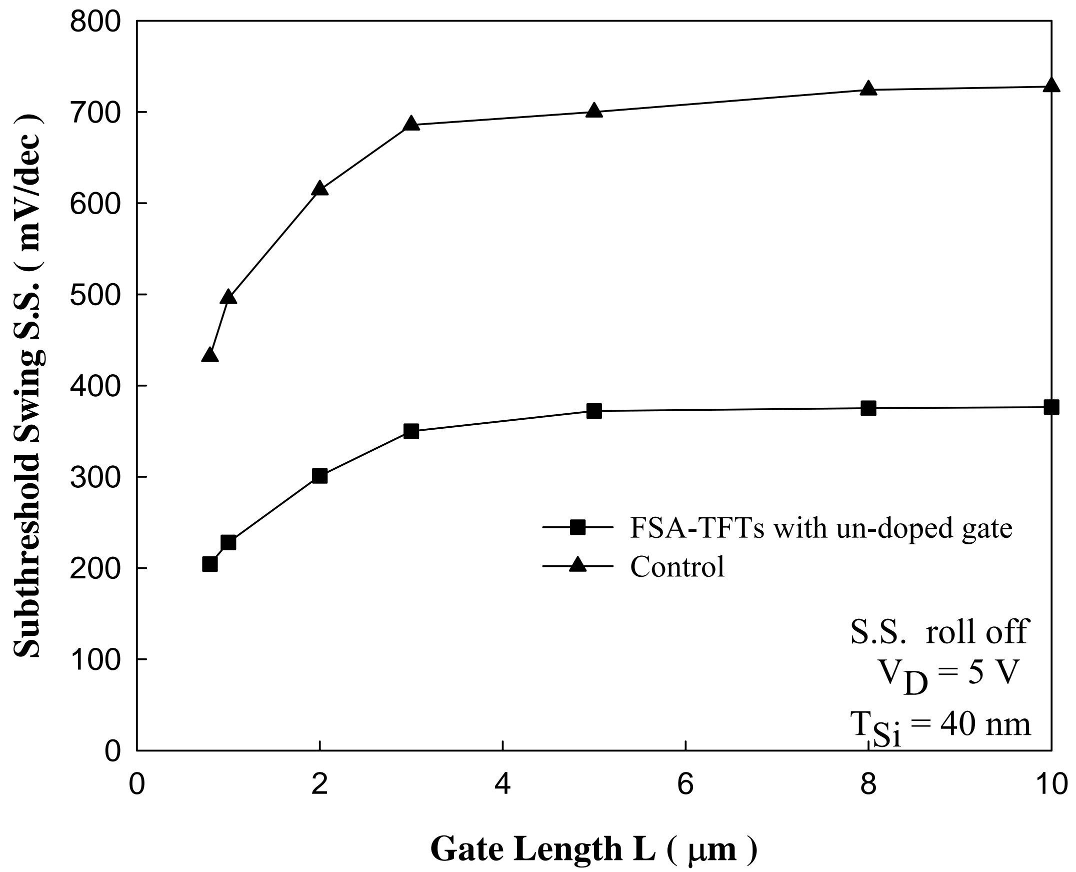


Fig. 3-23 Subthreshold swing roll off vs. channel length. The channel width is 10 μm. The drain voltage is 5 V.

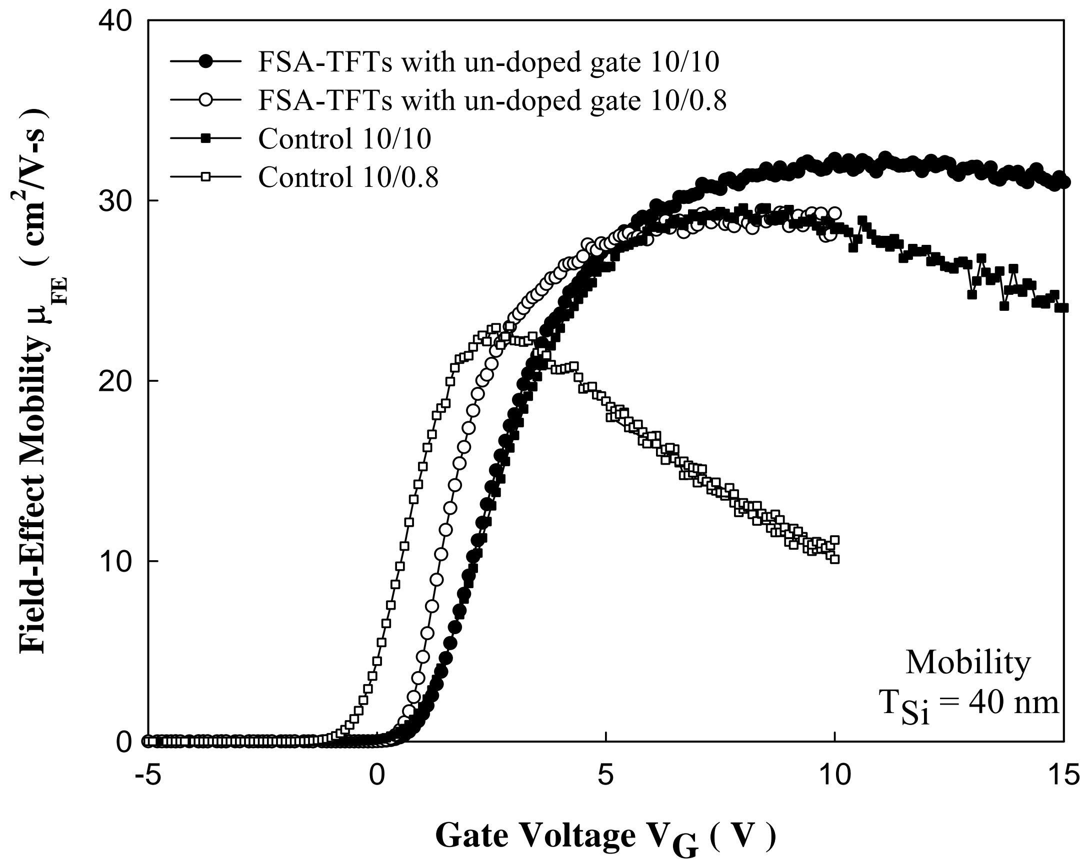


Fig.3-24 The mobility is plotted versus gate voltage for both control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm and W/L=10 μm/0.8 μm.

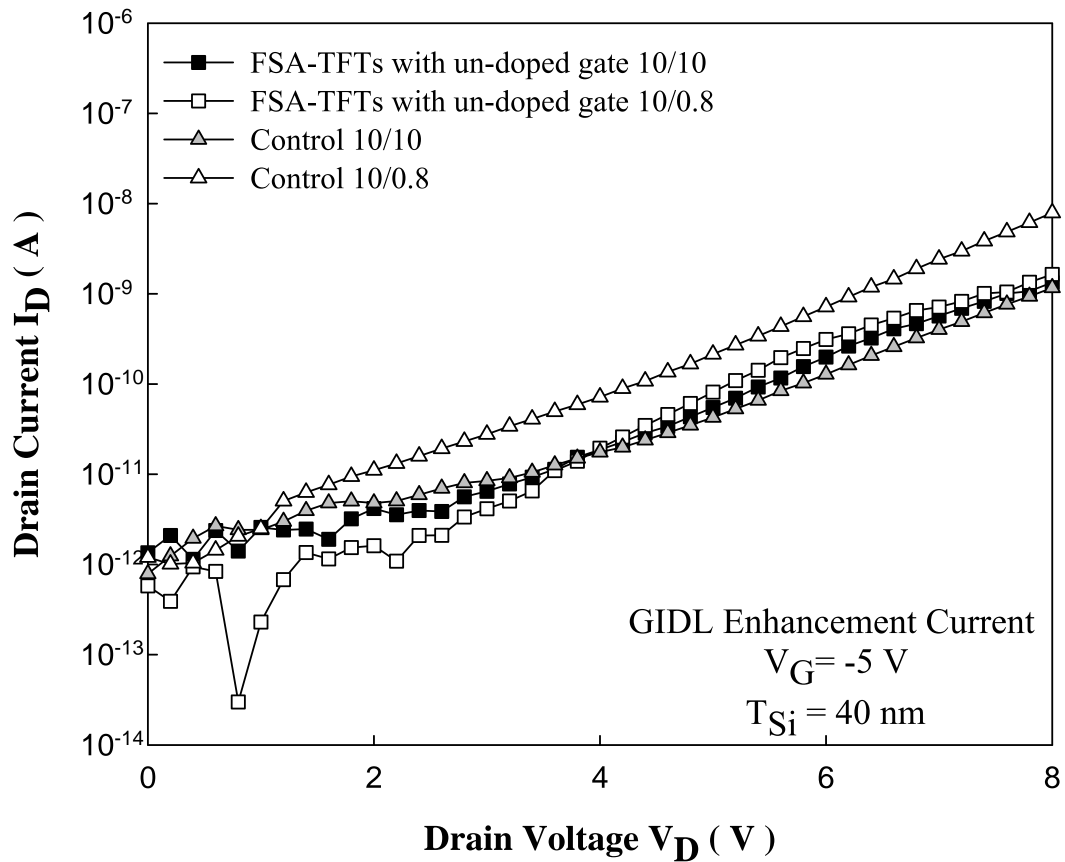


Fig.3-25 The GIDL enhancement current for both control TFTs and FSA-TFTs (un-doped gate) with W/L=10 μm/10 μm and W/L=10 μm/0.8 μm.

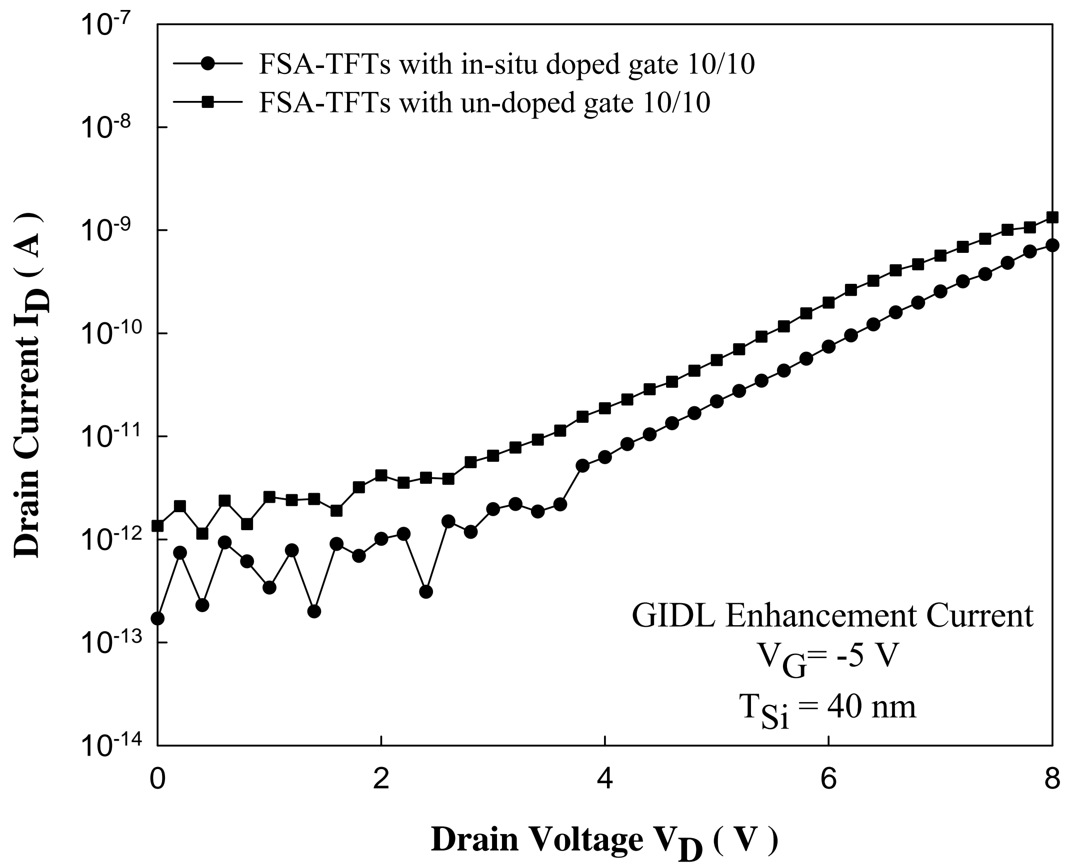


Fig. 3-26 The GIDL enhancement current for in-situ doped gate and un-doped gate FSA-TFTs with W/L=10 μm/10 μm.

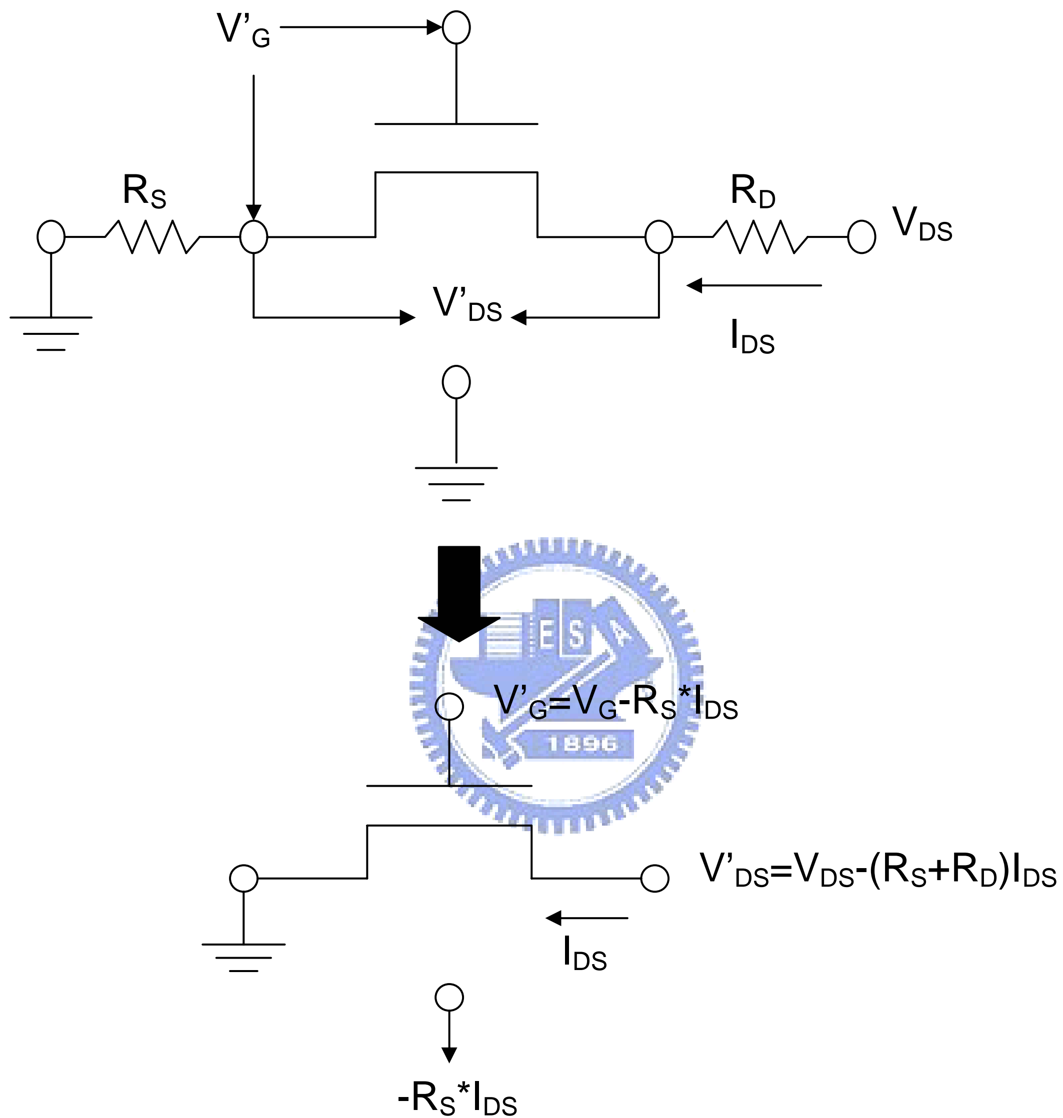


Fig.3-27 Equivalent circuit model with S/D series resistance is shown. The intrinsic part of the top circuit is equivalent to the bottom circuit with redefined terminal voltages [33].

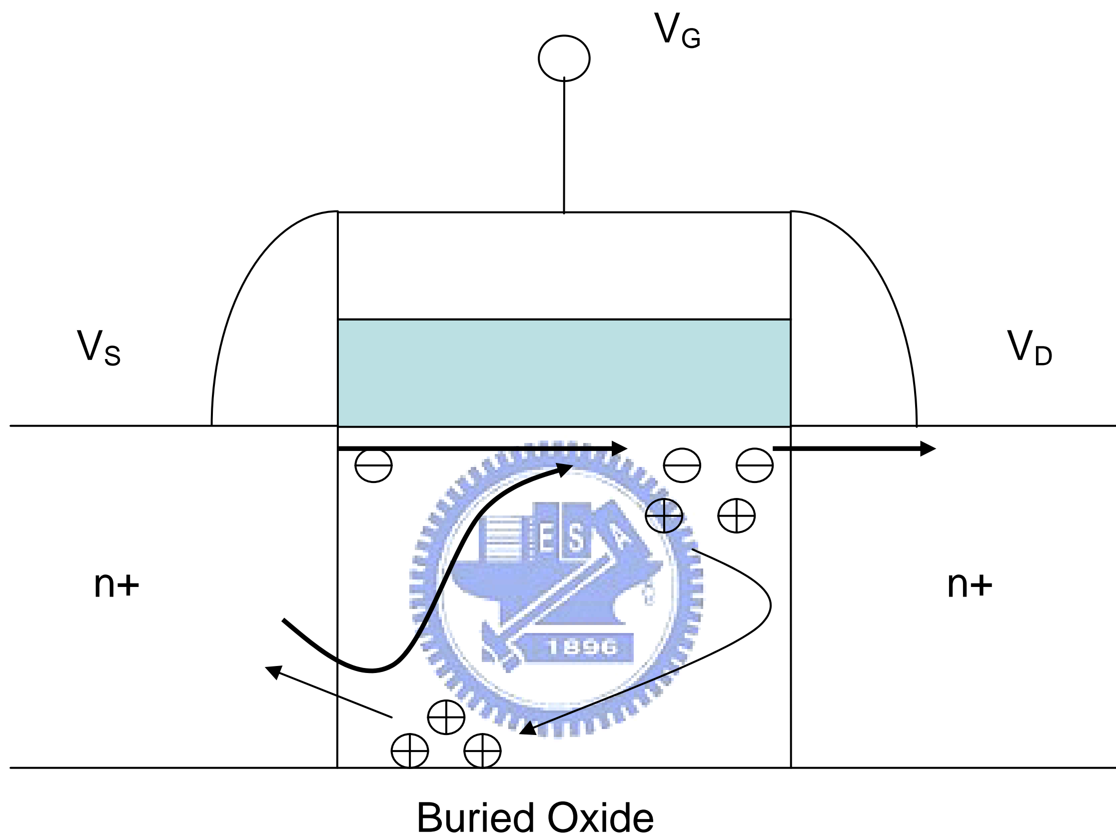


Fig. 3-28 The kink effect in Poly-Si TFTs.

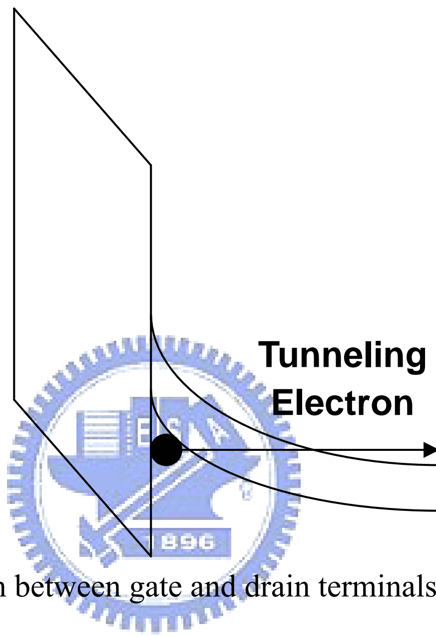


Fig. 3-29 Energy band diagram between gate and drain terminals.

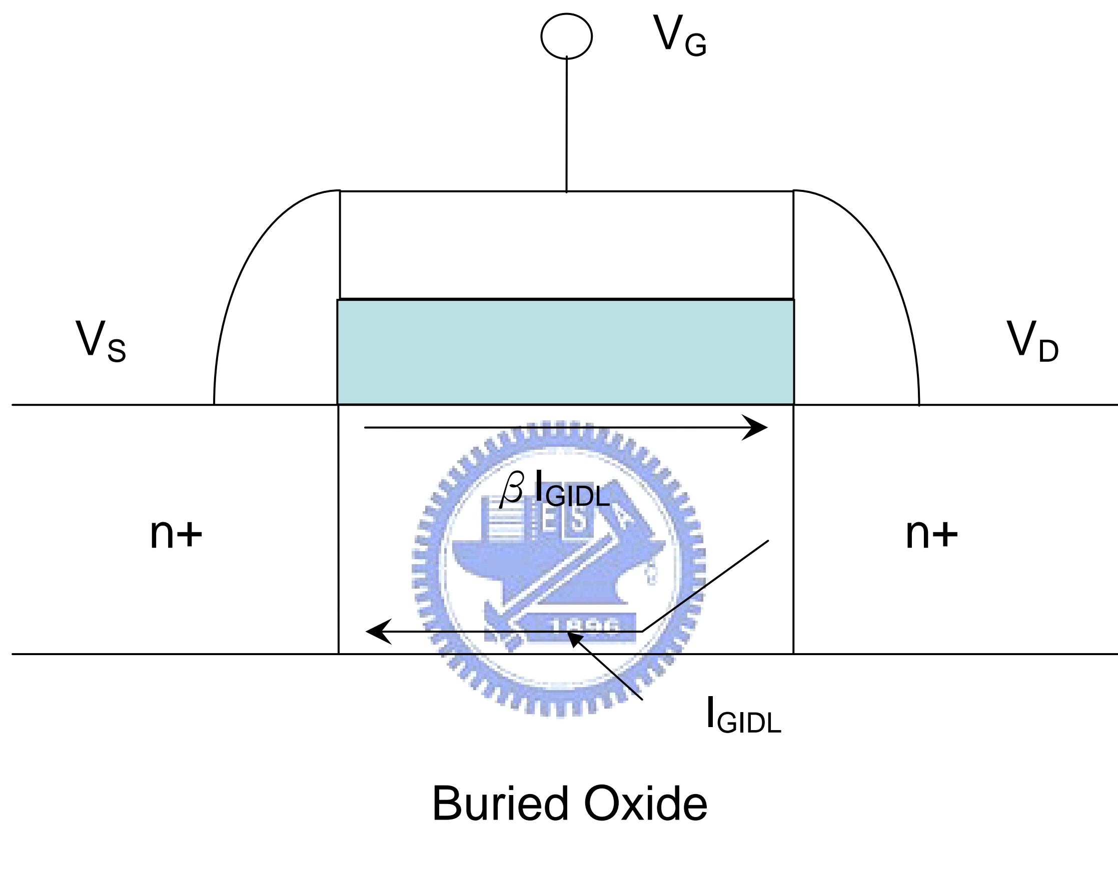


Fig. 3-30 Schematic of n-type poly-Si TFTs current flow in GIDL mode when the channel is turned off.

Chapter 4

Conclusions and Future works

4.1 Conclusions

In this thesis, we have investigated, for the first time, the fully Ni-salicided S/D and Gate in poly-Si TFTs. For fully Ni-salicidation technique, the parasitic resistance is drastically decreased. Besides its low resistivity, NiSi also possesses some inherent properties: (1)NiSi does not have narrow line effect. (2)Nickel is not reacted with oxide. (3)NiSi has the less silicon consumption compared with $TiSi_2$ and $CoSi_2$. (4)Silicidation can be formed at low temperature (400~600°C) without agglomeration.

In this thesis, fully Ni-salicided S/D and Gate can be achieved by one step RTA 550°C for 30-sec. The FSA-TFTs have excellent performance. Take in-situ doped gate for example, the ON current of FSA-TFTs is 14.44 μA. The OFF current of FSA-TFTs is 0.1 pA. So, the ON/OFF current ratio can be reached as high as 1.444×10^{8} which is one order of magnitude higher than control ones. The maximum mobility of the FSA-TFTs can also be achieved as high as 33.96 cm^2/V-s.

It is demonstrated that fully Ni-salicidation is a technology to solve some problems in this thesis. FSA-TFTs can effectively suppress the floating-body effect and parasitic bipolar junction transistor action, compared to control TFTs.

Experimental results show that the FSA-TFTs give lower off-state leakage, improved subthreshold characteristics, less threshold voltage variation, and larger field-effect mobility compared with control TFTs. The characteristics of the FSA-TFTs are suitable for high performance driving TFTs with a stable threshold voltage and large breakdown voltage.

4.2 Future works

There are some interesting and important topics that are valuable for the future works. First of all, SPC process is used to crystallize a-Si layer in this thesis. Low mobility and high trap state density are the two major disadvantages. With excimer laser crystallization (ELC), better device performance can be expected. Besides active layer crystallization, there are many different process conditions which are our future works.

Different S/D implant dosage is an interesting topic. In this thesis, the S/D implant dosage is 5×10^{15} cm^{-2}. Different S/D implant dosage include $1\times10^{15} cm^{-2}$, 5×10^{14} cm^{-2}, 1×10^{14} cm^{-2} can be executed. We expect that fewer S/D implant dosages will not have severe kink effect, compared to control TFTs.

In-situ doped gate and un-doped gate FSA-TFTs have been successfully fabricated. Different gate implant dosage is also an interesting topic that we want to accomplish.

We hope that the different threshold voltage in the different gate implant dosage can be observed. Different RTA temperature, different RTA time, different TEOS oxide spacer thickness and 300 Å of channel film thickness are also our future research topics.

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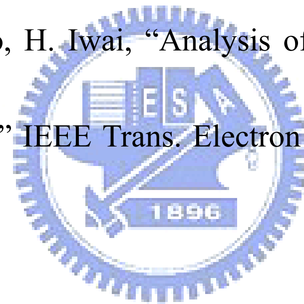

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