國 立 交 通 大 學

電子物理學系電子物理研究所

碩 士 論 文

金氧半場效應電晶體上佈植不同氮、氟離子劑量
之可靠性分析

Study on the reliability of pMOSFETs with different nitrogen and fluorine implantation dosages

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中華民國 九 十 四 年 六 月

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誌　謝

碩士班兩年辛苦的生涯，最後以一本論文做為連接另一個階段的橋梁，邁向人生另一個旅程。在這兩年中，受到許多人的幫忙，此論文才得以完成。首先，感謝趙天生博士在學生研究的歲月裡，提供了相當多的寶貴意見；老師獨特的為人處事態度，更讓我值得學習，令我獲益良多。

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金氧半場效應電晶體上佈植不同氮、氟離子劑量之可靠性分析

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摘要

隨著金氧半場效應電晶體尺寸持續的縮小，超薄氧化層在半導體發展的過程上，扮演著重要的角色。此論文研究不同位置和不同劑量的氮、氟離子佈植在 pMOSETs 上之電特性及因負偏壓溫度的不穩定性造成元件可靠性的下降。

首先，發現了一個重要的現象，當在汲極／源極延伸區域上佈植氮離子時，在退火過程期間，氮會阻止硼往通道介面的擴散，使得介面變的更陡峭，減小短通道效應。若將氟離子佈離進入矽基板上，能夠增加通道的轉移電導。其原因是氟離子造成汲極／源極上的片電阻值變小，使得轉移電導變大。

在可靠性方面，我們著重在氮佈植對於起始電壓漂移的影響。其結果表示氮離子在矽／矽氧化層的介面上，會降低活化能，減小元件對於負偏壓溫度不穩定性應力的抵抗力。為了改善此情況，我們在閘極上佈植適當劑量的氮、氟離子。根據結果顯示，這個方法的確可以的改善元件的可靠性。綜合上述，雖然在電性上有些佈植對於元件有好處，但在可靠性上反而造成不好的影響，因此，在元件製造過程中必需最佳化，使元件能發揮最大的效能。

Study on the reliability of pMOSFETs with different nitrogen and fluorine implantation dosages

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Abstract

With the dimensions of MOSFET devices continue to shrink, the reliability of ultra-thin oxide plays an important role in the development of semiconductor devices. In this thesis, we have investigated the electrical characteristics and degradation of device reliability due to Negative Bias Temperature Instability (NBTI) of pMOSFETs with different dosages of nitrogen and fluorine implanting into different regions of devices.

We found that when nitrogens were implanted into source/drain extension regions, nitrogen will retard boron diffusion into channel surface during annealing process, let interface become more steep lateral abruptness and reduce short channel effect. On the other hand, fluorine implanted into silicon substrate will enhance channel transconductance. This is because nitrogen reduces the sheet resistance in source/drain regions and has large transconductance.

Regarding reliability issues of devices, we focus on the effect of nitrogen implantation on the shift of threshold voltage. The result indicates that nitrogen on Si/SiO_2 interface

reduces active energy and decreases the immunity for NBTI stress. In order to improve this situation, we implanted applicable dosages of nitrogen and fluorine into the gate. In according to the result, this method improves devices' reliability indeed. We found that although implantations such as nitrogen would benefit for devices' performance, it may cause degradation of reliability such as NBTI for pMOSFETs. Therefore, ion implantations for pMOSFETs need to trade-off for obtaining the optimized devices' performance.

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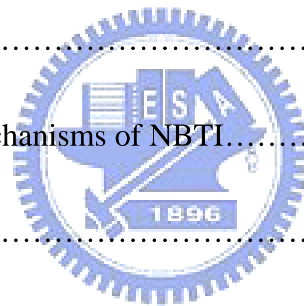

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Chap1

Introduction

1.1 General Background

For the recent 20 years, the semiconductor industry has been witnessing exceptional growth and achievements in integrated circuit (IC) manufacturing. In order to achieve high-performanced and low-powered devices, thinner gate insulators are required for deep submicrometer MOSFETs, but as the thickness of gate oxide is reduced, boron penetration occurs easily and the problem becomes severe.

With the continuous shrinking of the transistor dimensions, there are more and more issues to be solved. As MOSFET device dimensions are reduced below 1-μm gate lengths, the channel hot-carrier effect will be a major barrier to continued scaling and VLSI reliability [1],[2]. However, shifts in threshold voltage and changes in transconductance, subthreshold slope, or substrate current only secondhand reflect the physical damage at the interface. It is well known that hot-carrier effect in nMOSFETs is more serious than in pMOSFETs. In nMOSFETs, many studies has been done on the construction of the behavior and essential mechanisms , and it is generally accepted that hot-carrier stress damage is due both to the creation of interface states and the trapping of charge carriers in the oxide [3]-[5].

Owing to operation voltage is continually reduced, hot carrier issue becomes less critical as before. When the MOS devices are scaled down to sub-100nm node, gate-dielectric thickness decreases approaching to the direct tunneling regime [6]-[8]. The gate-leakage current of the ultrathin gate-dielectric significantly increases, and this current increases the standby power consumption and causes an insufficient on–off current ratio in static circuits. Therefore, some papers proposed oxynitride, SiON, which with a high concentration of nitrogen will be the gate dielectrics for the short term technology node. The SiON gate-dielectric with high nitrogen concentration is one of the key techniques to achieve low-leakage gate-dielectrics and to prevent boron penetration. However, it is difficult to form the ultrathin SiON with high nitrogen concentration without degrading devices' performance. Reliability is another issue while using the ultrathin SiON gate-dielectric [9]-[11].

High-k insulating metal oxides provide the required specific capacitance at a considerably larger physical thickness than SiO_2, they are currently under consideration as alternative gate dielectric materials for MOS devices. High-k dielectrics required to reduce the gate leakage current by suppression of direct tunneling for equivalent oxide thickness (EOT) are expected to replace SiO_2 around the 65 nm node [12]-[14]. In the original stage of the research, several high-k dielectric materials were considered, such as Al_2O_3, ZrO_2, HfO_2, and mixed layers. In fact while keeping the EOT constant, high-K dielectrics allow to increase the physical thickness of the gate stack. Hence the gate leakage is found to be reduced by 2 to 3

orders of magnitude. The use of high-K dielectrics has brought on serious additional problems to be solved, including unable to scale down EOT, reduction of channel mobility, thermal instability, increase of fixed charge, Fermi level pinning of the effective gate work function and reliability degradations.

1.2 Reliability issues on pMOSFETs

The reliability issues of ultrathin gate dielectrics is one of the most serious challenges in the scaling of ULSI devices. It has been reported that negative-bias-temperature instability (NBTI) is an important reliability problem in p-channel metal-oxide-silicon (MOS) field-effect transistors and complementary MOS (CMOS) inverter circuits when the oxide thickness is less than 3.5 nm [15]-[22]. Although much effort has been dedicated to reduce NBTI, the mechanisms of the degradation process are not fully clarified yet. This instability is seen as an increase with time of both interface-trap density and positive-oxide-fixed charge density during the operation of these devices.

NBTI is anticipated to be enhanced by scaling down of gate length [16] and also by incorporation of nitrogen into gate oxide [17]. This is because that nitrogen will pile-up at the Si/SiO_2 interface leads to some inferior as-grown characteristics such as Gm peak degradation, threshold voltage shift, and mobility degradation in inversion-layer. The enhancement of the NBTI degradation by nitrogen becomes stronger when the number of neighboring N atom

increases with increasing the N_{int}. On the other hand, it is known that nitrogen incorporation in the gate oxide suppresses boron penetration [18], [19], improves the hot-carrier resistance. The location of nitrogen in the film impacts the boron penetration and interface properties of the gate oxide [20]–[22]. Nitrogen implantation is also used to retard gate oxide growth and changes the oxide thickness with different implantation dosages.

Device characteristics instability in MOSFET's is also strongly associated with fluorine incorporation in the p^+-gate. The addition of fluorine into gate oxide is known to have a number of significant effects. Some benefits to device reliability have been reported, including improved p-type field-effect transistor (PFET) and n-type FET (NFET) hot-carrier immunity [23]–[28], improved dielectric integrity [29], and improved negative bias threshold instability (NBTI) [30]. A potentially adverse effect is fluorine's enhancement of boron diffusion in oxide, which may lead to large threshold shifts and poor dielectric quality [31]–[36]. Changes in oxide thickness and flatband voltage have also previously been reported [37-38].

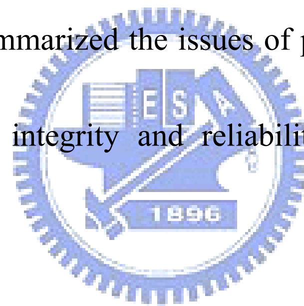
Some papers investigated that the effects of fluorine and nitrogen co-implantation into poly-Si gate. It is found that nitrogen in poly-silicon suppresses the boron penetration through the gate oxide [39]-[41]. On the contrary, the fluorine incorporated in polysilicon enhances boron penetration through the gate oxide into the Si substrate [42], [43]. However, leakage current induced by charging damage can be reduced significantly by fluorine or nitrogen

implantation. As a result, it is very interesting to investigate the mechanisms of incorporation of fluorine and nitrogen on the different positions in MOSFETs. In this thesis, we focus on implantation of fluorine and nitrogen at the substrate, poly-gate and/or source/drain extension with different implantation dosages. By this scheme, we obtain some interesting results and will clarify the role of fluorine and nitrogen on pMOSFETs.

1.3 Organization of this thesis

This thesis is divided into six chapters.

In Chapter 1, we have summarized the issues of pMOSFETs such as hot-carrier effects, boron penetrations, dielectric integrity and reliability issues etc. Then we compare the motivation of our studies.



In Chapter 2, we will describe the device structure and fabricating steps of pMOSFETs and list the process flow and split table.

In Chapter 3, we demonstrate the characteristics of fluorine and nitrogen on pMOSFETs. The result indicates that implantation of fluorine on substrate enhances channel transconductance and the nitrogen in source/drain reduces short channel effect.

In Chapter 4, negative-bias-temperature instability will be discussed with different nitrogen and fluorine implantation dosages. As we expected, the nitrogen in source/drain will aggravate the threshold voltage shifts.

In Chapter 5, we investigate dynamic NBTI (DNBTI) on p-channel MOSFETs with different conditions. The results show the similar trend as those in Chapter 4.

In Chapter 6, we give a brief conclusion to this study, dissertation and suggest with future work on this topic.

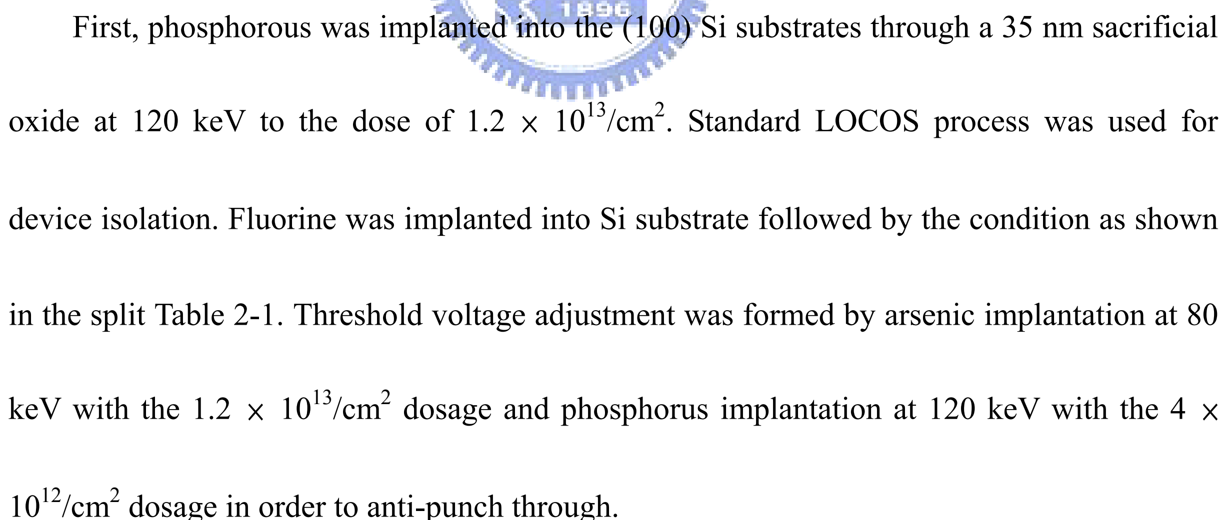
Chap 2

Device fabrication

2.1 Introduction

In this chapter, we will introduce the fabrication process of p-channel MOSFETs briefly. The p-channel MOSFETs were fabricated on 6-inch p type (100) silicon substrate with 2.5nm gate oxide in the Nation Nano Device Laboratories (NDL). The fundamental conditions were illustrated in Fig. 2-1 and Table 2-1

2.2 The sketch of device fabrication



First, phosphorous was implanted into the (100) Si substrates through a 35 nm sacrificial oxide at 120 keV to the dose of $1.2 \times 10^{13}/cm^2$. Standard LOCOS process was used for device isolation. Fluorine was implanted into Si substrate followed by the condition as shown in the split Table 2-1. Threshold voltage adjustment was formed by arsenic implantation at 80 keV with the $1.2 \times 10^{13}/cm^2$ dosage and phosphorus implantation at 120 keV with the $4 \times 10^{12}/cm^2$ dosage in order to anti-punch through.

After the RCA cleaning process, 2.5 nm gate oxide was grown in a vertical furnace with O_2 at 800 °C. A 200 nm poly-Silicon was deposited at 600 °C after gate oxidation. Fluorine and/or nitrogen was implanted into the poly-silicon gate followed the condition as shown in

the split table. Dry etcher, TCP-9400 Lam Research, was used to etching poly-silicon gate after behind gate patterning process. The sidewall spacer was formed by a conformal deposition of 200 nm TEOS oxide and a subsequent reactive ion etching (RIE). Then, Fluorine and/or nitrogen was implanted again under the split conditions as shown in the split table before S/D extension implantation. The self-alignment process was used to form source and drain electrode by implanting BF_2 at 10 keV with the dose of $5 \times 10^{12}/cm^2$.

Substrate etching and substrate implantation were executed continuously. Rapid thermal annealing (RTA) was performed at 1000 °C for 10 seconds to activate the dopants and annealed out the damage from ion-implantation. The passivation layer was deposited by TEOS at 700 °C for 550 nm. After contact etching, four-layer metal (Ti / TiN / Al / TiN) were carried out in a PVD system. Finally, wafers were annealed in forming gas (H_2 / N_2) ambient at 400 ℃ for 30 minutes.

2.3 Device fabrication process flow

【1】N-Well implantation

1. HF dip for 1 minute
2. Deposition of sacrificial oxides with the thickness of 35nm at 925 °C
3. N-Well Implantation with the dose of $1.2 \times 10^{13}/cm^2$ at 120 keV
4. Well drive-in at 1100 °C

5. BOE for 3 minutes

【2】LOCOS Definition

1. Deposition of pad oxide with the thickness of 35nm at 925 °C
2. Deposition of Si_3N_4 with the thickness of 150nm at 780 °C
3. LOCOS alignment (Mask 2 AA-I)
4. Use RIE (TEL5000) to etch Si_3N_4
5. N-field implantation with the dose of 2×10^{13} /cm^2 at 120 keV
6. P.R. stripping
7. Formation of field oxide with the thickness of 550nm at 980 °C
8. BOE dip for 15 seconds
9. Remove Si_3N_4 layer

【3】V_{th} adjustment Implantation:

1. HF for 8 minutes
2. Formation of sacrificial oxide with the thickness of 30nm at 925 °C
3. HF dip for 8 minutes
4. Formation of sacrificial oxide with the thickness of 30nm at 925 °C
5. Implantation conditions were followed by split table

6. As^+ ion implantation with the dose of 1.2×10^{13} /cm^2 at 80 keV
7. P-APT implantation with the dose of 4×10^{12} /cm^2 at 120 keV

【4】Gate pattern definition:

1. HF for 8 minutes
2. RCA Clean
3. HF dip for 1 minute
4. 25nm O_2 oxidation in vertical furnace
5. 200nm poly-Si deposition at 625 °C
6. Implantation conditions were followed by split table
7. Gate Alignment (Mask 3 POLY-I)
8. Poly-Silicon etching by TCP-9400
9. P.R. stripping

【5】S/D formation:

1. Implantation conditions were followed by split table
2. BF_2 implantation with the dose of 1×10^{15} /cm^2 at 5 keV for S/D extension
3. Growth of 200nm TEOS oxides at 700 °C
4. Dry etching of TEOS oxides by TEL5000

5. BF_2 implantation with the dose of 5 × 10^{15}/cm^2 at 10 keV for S/D implantation

6. N^+ substrate alignment (MASK 5 SUBSTRATE OPENING-I)

7. Sub-etching by TEL5000

8. N^+ substrate implantation with the dose of 5 × 10^{15}/cm^2 at 40 keV

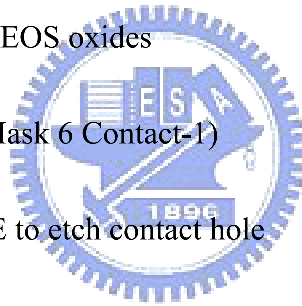
9. P.R. Stripping

10. Activation at 1000 °C for 10 seconds.

【6】Contact holes formation:

1. Deposition of 550nm TEOS oxides

2. Contact alignment (Mask 6 Contact-I)



3. Use TEL5000 and BOE to etch contact hole

4. Remove P.R.

【7】Metallization:

1. HF dip for 2 minutes

2. Sputter 40 / 100nm Ti / TiN films

3. Sputter 900nm Al-Si-Cu films

4. Metal alignment (Mask 7 PAD-I)

5. Metal etching by ILD-4100

6. P.R. Stripping

7. Post-metal annealing (PMA) at 400 °C for 30 minutes in H_2 / N_2 ambient

Chap 3

Device Measurement and Characteristics

3.1 Introduction

In this chapter, I-V characteristics of pMOSFETs with 2.5-nm gate oxide thickness were characterized in detail. The methods of measurement are briefly also described. Transistor characteristics depend on the location of fluorine and nitrogen. We will explain the resultant difference in pMOSFETs with fluorine and nitrogen incorporation.

3.2 Methods of Device Parameter Extraction

The transistor performance and I-V characteristics of the pMOSFETs were measured using a KEITHLEY 4200 semiconductor parameter analyzer with source and bulk grounded. In the nonsaturation region, we will obtain the ideal drain current for p-channel MOSFET

$$I_D = \frac{W \mu_p C_{OX}}{2L}[2(V_{SG} + V_T)V_{SD} - V_{SD}^2] \qquad (3.1)$$

and, in the saturation region, we will have

$$I_D = \frac{W \mu_p C_{OX}}{2L}(V_{SG} + V_T)^2 \qquad (3.2)$$

where L is the channel length, W is the channel width, μ_p is the mobility of the holes in the inversion layer, C_{OX} is the oxide capacitance per unit area, V_{SG} is the source-to-gate voltage, and V_{SD} is the source-to-drain voltage.

The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage for linear region：

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \frac{W\,\mu_n\,C_{OX} V_{SD}}{L} \qquad (3.3)$$

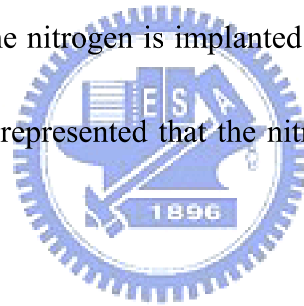
The I_D-V_{GS} curve deviates from a straight line at gate voltages below V_T due to subthreshold currents and above V_T due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope on the I_D-V_{GS} curve by a maximum in the transconductance, $g_m \equiv \frac{\partial I_D}{\partial V_{GS}}$, fit a straight line to the I_D-V_{GS} curve at that point and extrapolate.

We use a charge pumping technique to investigate interface-state densities in pMOSFETs. This method is suitable for interface trap measurements on small-geometry MOSFETs instead of large-diameter MOS capacitors. Figure 3-1 illustrates a basic setup for charge-pumping measurements. The MOSFET source and drain are tied together and reverse-biased with a voltage V_R. The time-varying gate voltage is of sufficient amplitude for the surface under the gate to be driven into inversion and accumulation. The pulse train can be square, triangular etc. Here we use square and triangular waveforms generated by an Agilent 81110 pulse generator. The charge pumping currents are measured at the substrate, with source and drain tied together. When a p-MOSFET channel is pulsed into inversion, hole currents from source/drain can flow into the channel, where some of the holes will be captured by the surface states. When the gate pulse is driving the surface back to accumulation, the hole charges drift back to

the source and drain, but those hole charges trapped in the surface states will recombine with the electrons from the substrate and give rise to a net flow of negative charges into the substrate. This substrate current can be directly related to the surface-state density.

3.3 Results and Discussion

First, we determined some notations to represent our spilt conditions. "B" is represented "Bulk", "S/D" is represented "source and drain", "G" is represented "Gate", "B(F)" means that the fluorine is implanted into bulk Si at 15 keV with the $1 \times 10^{14}/cm^2$ dosage, and "S/D(N)" is represented that the nitrogen is implanted into source/drain at 15 keV with the $1 \times 10^{14}/cm^2$, and "S/D(N*)" is represented that the nitrogen is implanted into source/drain at 15 keV with the $1 \times 10^{15}/cm^2$.



In this section, we would introduce the nitrogen and fluorine effects on different positions of pMOSFETs with different dosages. In Fig. 3-2, we measured different dimensions of devices. We found that incorporation of nitrogen into poly-Si gate with the dose of $1 \times 10^{15}/cm^2$ have large threshold voltage. On the contrary, gate implanted fluorine reduced threshold voltage. This is because that fluorine in the poly-Si gate will enhance boron diffusion through gate oxide into substrate and nitrogen will retard boron diffusion into bulk silicon. Figure 3-3 illustrate the effect of nitrogen incorporation into source/drain junction. In the annealing process, nitrogen will decrease boron out-diffusion from source/drain extension

region. Therefore, this implantation condition reduced threshold voltage roll off effects.

We measured ten devices for each split condition to extract the average transconductance and threshold voltage. Figure 3-4 and Figure 3-5 depict that fluorine in the substrate will enhance the transconductance at the same condition. As a result, this may be due to the improvement at the interface when F is incorporated. The charge-pumping current is measured for these devices. We found it is not the case as we expected. In Figure 3-6, the Icp of device with fluorine implanted substrate exhibits a larger Icp current. Figure 3-7 illustrates source/drain sheet resistance for different implantations at poly-silicon gate and bulk-Si. We found that sheet resistance in source/drain region dominate transconductance degradation phenomenon. Nitrogen incorporation into gate with the dose of $1 \times 10^{14}/cm^2$ will also enhance the transconductance. But large nitrogen concentration reduces the transconductance. This is due to the combination of N-B in the gate, causing the poly-depletion effect. This makes the effective oxide capacitance decrease. Threshold voltage characteristics with different poly-gate and bulk-Si implantation of pMOSFETs characteristics are shown in Fig. 3-8 and Fig 3-9. Fluorine in the substrate results in a small threshold voltage and nitrogen in the gate has large threshold voltage. Because fluorine was implantated all over the active region including source/drain junction, the following annealing process will let fluorine enhance boron diffusion into the channel region. Implanting nitrogen with the dose of $1 \times 10^{15}/cm^2$ increased the threshold voltage due to poly depletion effect, which causes the

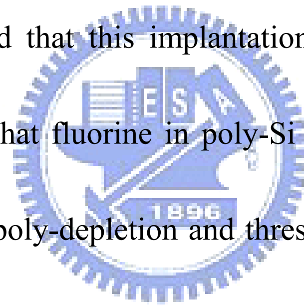
decrease of oxide capacitances.

Figure 3-10 and Figure 3-11 shows the transconductance with different source/drain and bulk-Si implantation. We found that nitrogen implantation into source/drain decreased transconductance. Devices with fluorine in source/drain has large transconductance than nitrogen ones. This may be due to the diffusion of nitrogen toward silicon/oxide interface during annealing process and cause interface state as shown in Fig.3-12. Moreover, sheet resistance in source/drain region also affects the transconductance. In Fig 3-13, we found that fluorine in source/drain has large sheet resistance than nitrogen in source/drain. In Fig. 3-14 and Fig. 3-15, nitrogen in source/drain has large threshold voltage due to prevention of boron diffusion by nitrogens. Fluorine incorporation into source/drain has small threshold voltage than nitrogen incorporation into source/drain. Since fluorine enhance boron diffusion to bring small threshold voltage.

To compare fluorine incorporation into poly-silicon gate with silicon substrate, we have some results as shown in Fig. 3-16 and Fig. 3-17. Fluorine in poly-silicon gate reduce transconductance. Figure 3-18 and Figure 3-19 show that fluorine implantation into gate results the reduction of threshold voltage. It is known that pile-up of fluorine from the fluorine and/or BF_2 gate implant at the poly-silicon/gate oxide interface is responsible for the enhanced boron penetration.

3.4 Summary

In this chapter, electrical characteristics of fluorine and nitrogen effects on pMOSFETs were measured in detail. First, we find that large nitrogen concentration in poly-silicon gate results in poly-depletion effect and possess larger threshold voltage. Second, nitrogen in source/drain extension region has a better immunity to threshold voltage roll-off phenomenon. On the other hand, fluorine incorporation into silicon substrate enhances the transconductance, which is similar to nitrogen incorporation into poly-silicon gate. The implantation of nitrogen into poly-Si gate can effectively suppress the boron penetration deleterious to pMOSFET with thin gate oxide. But we found that this implantation will increase interface state density. Finally, we have also shown that fluorine in poly-Si gate can reduce the transconductance. Therefore, boron penetration, poly-depletion and threshold voltage effects are combinational issue while we try to enhance devices' performance by incorporating nitrogen and fluorine into pMOSFETs.



Chap4

Negative bias temperature instability of pMOSFETs with different nitrogen and fluorine implantation dosages

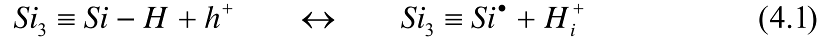
4.1 Introduction

Generation of interface traps during negative bias temperature instability (NBTI) stress in p+-gate pMOSFETs has been the most critical issue for the reliability as continuous scaling down of ULSI devices. Moreover, it has been reported that NBT degradation of oxynitride dielectrics (SiON) is remarkably enhanced. On the contrary, the addition of fluorine into gate oxide improved negative bias threshold instability. In this chapter, we investigated the NBTI effects on pMOSFETs with the different dosages of nitrogen and fluorine incorporation. The devices were applied to the gate electrode of pMOSFET at high temperatures with source/drain grounded and the stress condition is under Vg = -3.5 V at 150°C shown in Fig. 4-1.

4.2 Researches about the mechanisms of NBTI

During negative bias temperature instability stress, the interface states N_{it}, trivalent silicon dangling bonds $Si_3 \equiv Si^{\bullet}$, and fixed oxide charges ($O_3 \equiv Si^{-}$) are generated by the impact of hot holes on the hydrogen-terminated Si bonds and contribute to the negative

threshold voltage shift [44],[45]. The electrochemical reactions are expressed as follows:



$$Si_3 \equiv Si - H + h^+ \quad \leftrightarrow \quad Si_3 \equiv Si^\bullet + H_i^+ \qquad (4.1)$$

$$Si_3 \equiv Si - H \quad \xleftrightarrow{h^+} \quad Si_3 \equiv Si^\bullet + H_i \qquad (4.2)$$

$$O_3 \equiv Si - H + h^+ \quad \leftrightarrow \quad O_3 \equiv Si^+ + H_i \qquad (4.3)$$

The holes are activated thermally and gain enough energy to dissociate the interface/oxide defects by the vertical electrical field near the LDD regions because of higher hole concentrations near the gate edge. Initially, the reaction favors the generation of interface states and produces hydrogen atoms and ions at the interface. And this process is limited by the dissociation rate of hydrogen-terminated Si bonds. After some stress time, however, the transport of hydrogen ions in the oxide dominates and its diffusion rate is controlled by two factors: (a) the modified oxide field due to the existing hole trapping in the oxide and the formation of positive fixed oxide charges. (b) the gradually increasing interface states $Si_3 \equiv Si^\bullet$. Hence, further diffusion of protons or the generation of interface states will be discouraged. When reaction (4.1) reaches the balanced condition, the main electrochemical reaction becomes the diffusion of neutral hydrogen atoms in (4.2) and (4.3).

4.3 Results and Discussion

In this section, we employ charge pumping methods to extract interface-trap density [46]. At high frequencies, the Icp current is given by

$$I_{cp} = q \cdot f \cdot A_G \cdot N_{it} \tag{4.4}$$

$$\Rightarrow \quad N_{it} = \frac{I_{cp}}{q \cdot f \cdot A_G} \tag{4.5}$$

where N_{it} is interface-trap densities per area unit, A_G (cm^2) is the gate area and *f* (Hz) is the frequency.

We use two kinds of pulse train as square and triangular. The first form obtain interface-trap densities near conduction band and valance band, the latter form obtain interface-trap densities close to deeper level. By using this method, we can realize different levels of interface-trap density.

Figure 4.2 shows threshold voltage shift under NBTI stress with different source/drain and bulk-Si implantation. The BT stress condition is Vg = - 3.8 V at 150°C. We found an interesting result. Although higher nitrogen implantation at source/drain extension region reduces short channel effect, it decreases device reliability under NBTI stress. It can be explained by the locally enhanced degradation reactions between holes and oxide near the source/drain extension region, and the nitrogen may diffuse toward the silicon/oxide interface during RTA processing step or lateral scattering of ion implantation. In Fig. 4-3, interface-trap density of nitrogen implantation at source/drain extension region has the maximal N_{it} than others. Triangle wave has the same trend as shown in Fig. 4-4. There is another reason for nitrogen reduce reliability phenomenon. Fig. 4-5 shows temperature dependence of NBTI stress. In the figure, slope is proportional to active energy. So, nitrogen cause lower Ea let

device owning poor reliability.

Figure 4-6 shows threshold voltage shift under NBTI stress for pMOSFETs with different source/drain implantation. Fluorine incorporation into source/drain extension region has a better reliability than nitrogen does. Figure 4-7 and Figure 4-8 exhibit the account for this result. In the annealing process, nitrogen diffusion to Si/SiO_2 interface causes an increase of interface-trap density than fluorine influence does. The result is corresponding to Fig. 3-12 as we expected. Threshold voltage shift under NBTI stress for different poly-silicon gate and bulk-Si implantation as shown in Fig. 4-9. In chapter 3, we have known that fluorine implantation into silicon substrate has more interface-trap density opposite to control wafer (compare to Fig. 3-6). This figure suggests fluorine and nitrogen incorporation into poly-silicon gate enhance device reliability and nitrogen implantation has the better efficiency than fluorine. Maybe it is related to fluorine enhances boron diffusion through gate insulator into silicon substrate. We also found the similar result as shown in Fig 4-10. Besides, we investigate difference poly-silicon gate implantation without substrate implantation. In Fig. 4-11, nitrogen and fluorine implantation into gate can also increase reliability issues. Nitrogen incorporation into poly-silicon gate with the $1 \times 10^{15}/cm^2$ dosage has the better immunity for NBTI stress than fluorine incorporation into poly-silicon gate with the $1 \times 10^{14}/cm^2$ dosage. Figure 4-12 illustrates interface state for the same condition as that in Fig. 4-10. Moreover, it shows the similar result as before.

4.4 Summary

NBTI effects on pMOSFETs with the different dosages of nitrogen and fluorine incorporation were investigated in this chapter. Although nitrogen at the source/drain extension region can reduce threshold voltage roll-off effects, however, nitrogen diffusion from source/drain extension region into channel interface during RTA processing step makes the NBTI of pMOSFETs more serious. Therefore, the implantation must be trade-off for devices' fabrication. We found that the method of nitrogen and fluorine implantation into poly-silicon gate can be used to enhance device reliability performance.

Chap 5

Dynamic Negative bias temperature instability of pMOSFETs with different nitrogen and fluorine implantation dosages

5.1 Introduction

In conventional NBTI study, a constant negative bias is applied to the gate electrode as the "high" output state in a CMOS inverter. However, the applied gate bias is switching between "high" and "low" voltage during the operation of pMOSFETs in CMOS inverters, while the drain bias is alternating between "low" and "high" voltage correspondingly. During low output phase of an inverter, the electric passivation (EP) effect reduces the interface traps generated during high output phase effectively and recovers the degradations of device parameters for a certain degree. This "Dynamic" negative bias temperature instability (DNBTI) operating in a CMOS inverter circuit prolongs the device lifetime significantly. Therefore, it is important to investigate dynamic stress conditions. In this chapter, we clarified the DNBTI effects to our splits. The positive gate voltages were stressed under Vg = 0 V at 150°C.

5.2 Researches about the mechanisms of DNBTI

The passivation effect or dynamic NBIT can be explained by extending the previous Hydrogen diffusion–reaction model [47]–[50]. The interface trap generation is ascribed to hydrogen release from a hydrogen terminated silicon-dangling bond ($Si \equiv Si - H$), first proposed by Balk in 1965. Under high-temperature and negative gate bias stress conditions, the holes from the induced inversion layer react with the interface trap precursors ($Si \equiv Si - H$), breaking the H–Si bond and resulting in interface traps N_{it} (Si dangling bonds). The produced hydrogen-related species, denoted as X in Fig. 5-1(a), diffuse/drift to the gate electrode. During this stress period, the interface acts as a hydrogen source. The electric passivation (EP) effect can be readily interpreted by the reverse reaction between N_{it} and X species, as shown in Fig. 5-1(b). The interface trap passivation by hydrogen-related in SiO_2 was first explained in a comprehensive study by Sah et al. in 1984. When the bias polarity is reversed (positive or zero gate bias), the channel inversion layer disappears. The breaking of Si–H bond is interrupted due to a lack of holes, and at the same time, move back to the SiO_2 /Si interface under the influence of positive gate voltage and passivates the Si dangling bond, resulting in N_{it} reduction. In this period, the interface acts as a hydrogen sink. Further investigation of this interface trap generation/passivation mechanism in DNBTI is in progress and will be reported elsewhere.

5.3 Results and Discussion

Figure 5-2 shows threshold voltage shift under stress-passivation-stress for pMOSFETs with different source/drain and bulk-silicon implantation. The BT stress condition is Vg = -3.8 V for NBT stress, and Vg = 0 V for PBT stress. It is obvious that the threshold voltage shift increases during negative gate voltage applied with source/drain ground. When reversing the gate-to-source/drain electric field to the opposite polarity (positive) during DNBTI stressing, a reduction (passivation) of ΔN_{it} and thus ΔV_{th} is observed. In Fig. 5-3 and Fig. 5-4, nitrogen implantation into the source/drain extension region has large ΔN_{it} than control device. This is because nitrogen causes interface-trap density enhancement during annealing process and have the lower active energy.

Threshold voltage shift under stress-passivation-stress for pMOSFETs with different source/drain implantation is shown in Fig. 5-5. We found the same trend as shown in chap 4. The ΔV_{th} of nitrogen implantation into source/drain extension region is lower than that by fluorine implantation into source/drain extension region. In Fig. 5-6 and 5-7, we found nitrogen implantation has a lower interface state under the square wave plus. But under the triangle wave plus, two curves are almost the same.

Figure 5-8 shows DNBTI curves between control and fluorine implantation condition. The device of fluorine implantation has a better performance of reliability than that of control one. On the other hand, the variation of charge pumping current by fluorine implantation has

lower values as shown in Fig. 5-9 and Fig. 5-10. Finally, we compare the DNBTI effect by fluorine implantation or nitrogen implantation into poly-silicon gate. Obviously,. ΔV_{th} of devices with fluorine implantation into poly-silicon gate is worse than that with nitrogen does, as shown in Fig. 5-11. This indicates that ΔN_{it} of device with nitrogen implantation into the gate is less than that with fluorine implantation. The result is shown in Fig. 5-12.

5.4 Summary

In this chapter, we have investigated the dynamic NBTI effects of pMOSFETs with different nitrogen and fluorine implantation dosages. The result indicates the identical trend as those in chapter 4. Nitrogen implanted at source/drain extension regions has poor reliability performance. But fluorine at source/drain extension region can improve the performance. We also found that nitrogen or fluorine in implanted at poly-silicon gate can enhance devices' reliability. Moreover, the immunity of DNBTI effects by nitrogen implantation is better than fluorine implantation.

Chap 6

Conclusion

In this thesis, the effects of nitrogen and fluorine incorporation into different regions of pMOSFETs have been investigated in detail for the first time. We implant nitrogen and/or fluorine with different dosages into silicon substrate, poly-silicon gate and source/drain extension regions.

The electrical characteristics of pMOSFETs with 2.5-nm gate oxide thickness were first characterized. Nitrogen dosage of 1×10^{14} /cm^2 in poly-silicon gate will enhance channel transconductance and suppress the boron penetration effect. But large nitrogen dosage in poly-silicon gate will result in poly-depletion effect and reduce transconductance. Therefore, the dosage of nitrogen implantation needs optimization. We found that devices with nitrogen in source/drain extension region have a better immunity to threshold voltage roll-off. We have also shown that fluorine in poly-silicon gate can reduce the transconductance.

The reliability of surface channel p^+-gate pMOSFETs have been evaluated from the viewpoint of BT instability. We found that devices with nitrogen at source/drain extension regions enhance threshold voltage shift due to nitrogen diffuse into channel region during RTA process, which decreases the active energy (Ea) of NBTI. Moreover, nitrogen and fluorine incorporation into poly-gate were discussed. This method can reduce interface-trap

density and is useful for NBTI immunity.

The dynamic NBTI effect for all devices is investigated for a real operation of pMOSFETs in CMOS. We found the threshold voltage shift decreased at the same condition. This is because that the dangling bond will be repaired by hydrogen-related species during positive voltage applying. Under this operation, it significantly prolongs the pMOSFETs lifetime as compared to traditional static NBTI. The resultant DNBTI for pMOSFETs is similar to NBTI for different nitrogen and/or fluorine implantations.

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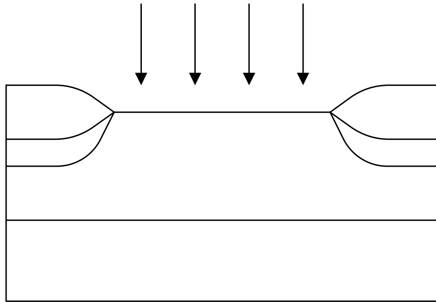
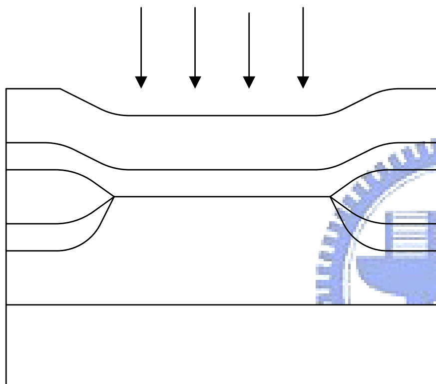


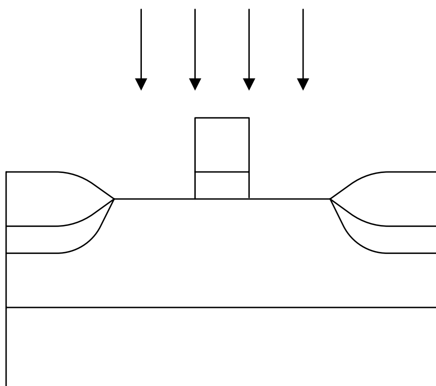
Bulk silicon implantation：

F^+, 1 × 10^{14}/cm^2, 15 keV



Gate implantation：

F^+, 1 × 10^{14}/cm^2, 15 keV
N_2, 1 × 10^{14}/cm^2, 15 keV
N_2, 1 × 10^{15}/cm^2, 15 keV



S/D implantation：

F^+, 1 × 10^{14}/cm^2, 15 keV
N_2, 1 × 10^{14}/cm^2, 15 keV
N_2, 1 × 10^{15}/cm^2, 15 keV

Fig. 2-1 the sketch of conditions

Gate split / Bulk and S/D split	W/O	**Bulk** F^+ 1E14 /cm^2 15 keV	**Gate** F^+ 1E14 /cm^2 15 keV	**Gate** N_2 1E14 /cm^2 15 keV	**Gate** N_2 1E15 /cm^2 15 keV
W/O	★		★		★
Bulk F^+ 1E14 /cm^2 15 keV		★	★	★	★
S/D extension F^+ 1E14 /cm^2 15 keV	★				
S/D extension N_2 1E14 /cm^2 15 keV		★			
S/D extension N_2 1E15 /cm^2 15 keV	★	★			

Table 2-1 Split conditions

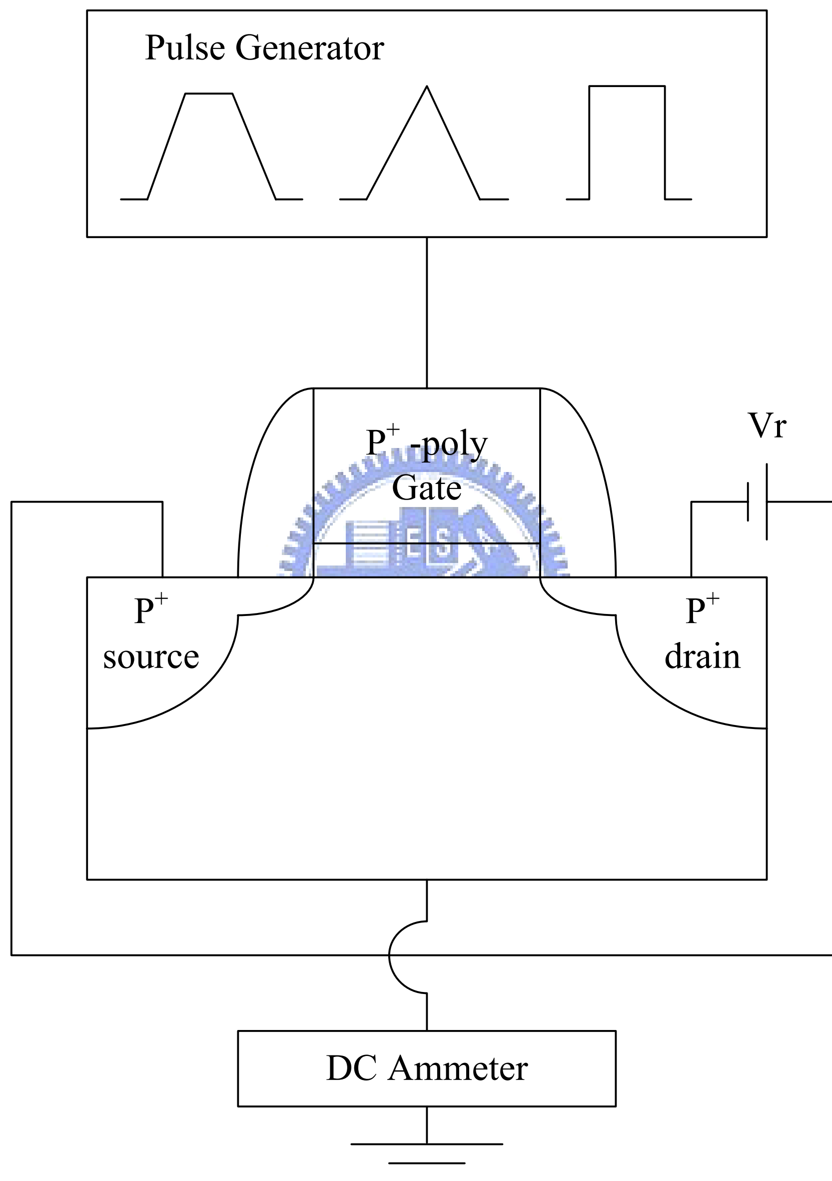


Fig. 3-1 Basic experimental setup of charge pumping measurement

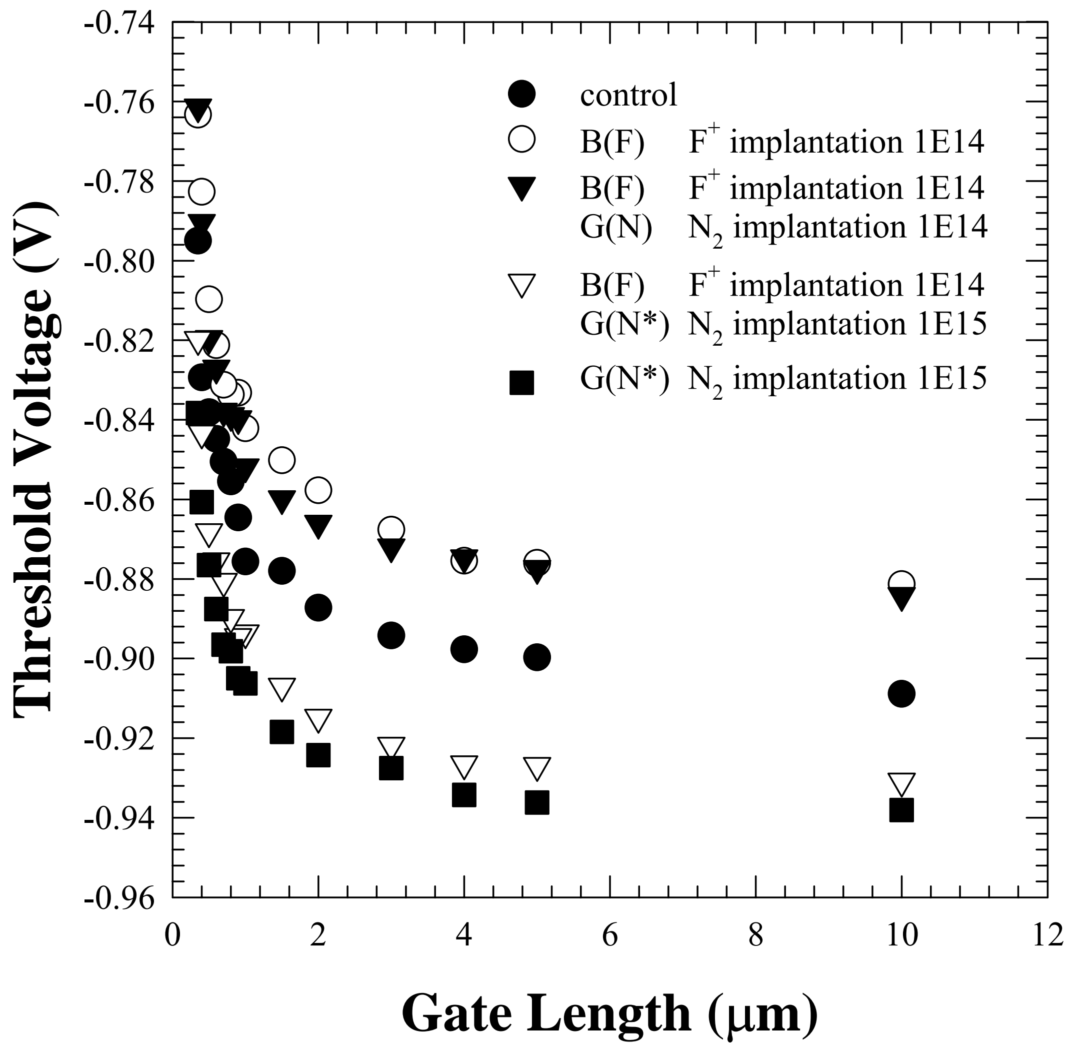


Fig. 3-2 Threshold voltage roll off with different poly-silicon gate and bulk-Si implantation

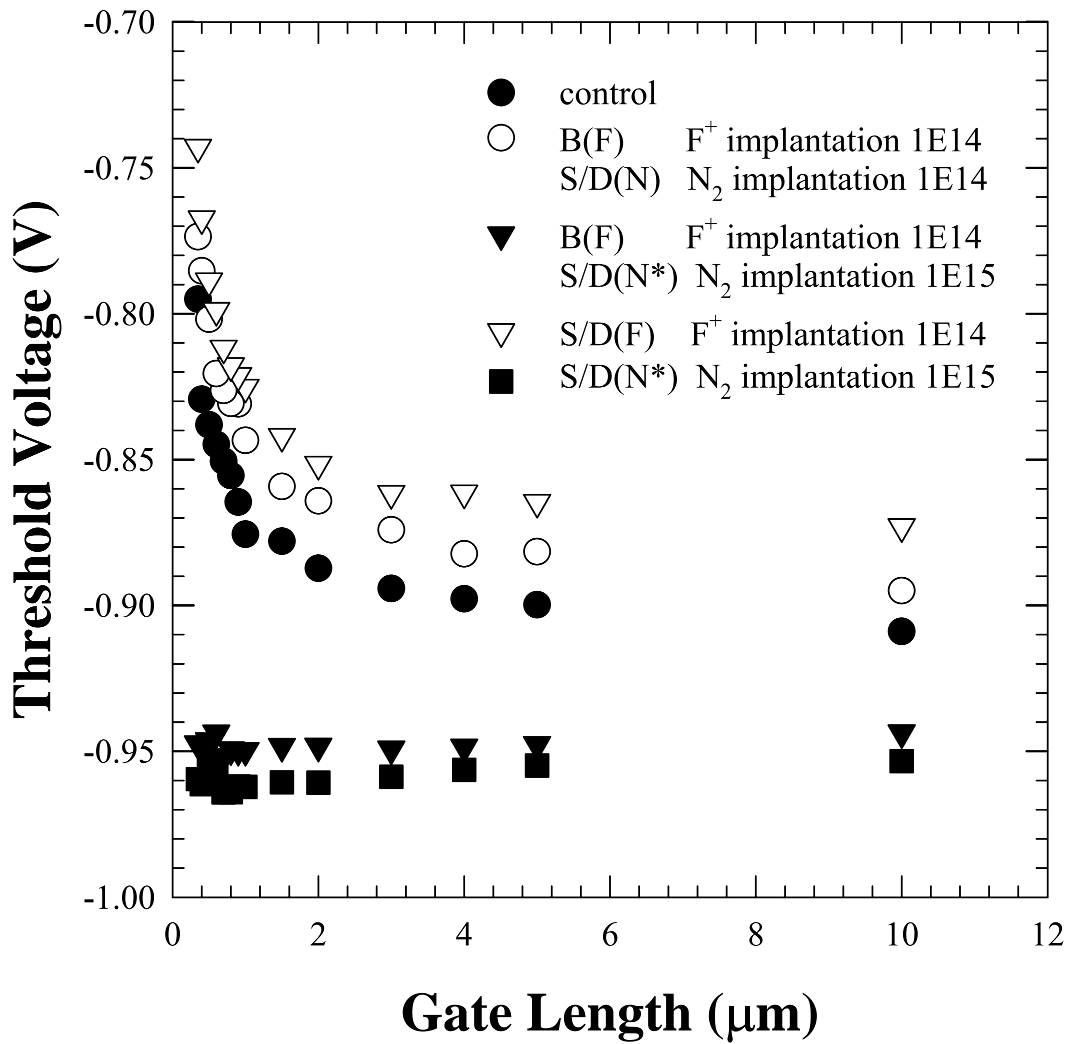


Fig. 3-3 Threshold voltage roll off with different source/drain and bulk-Si implantation

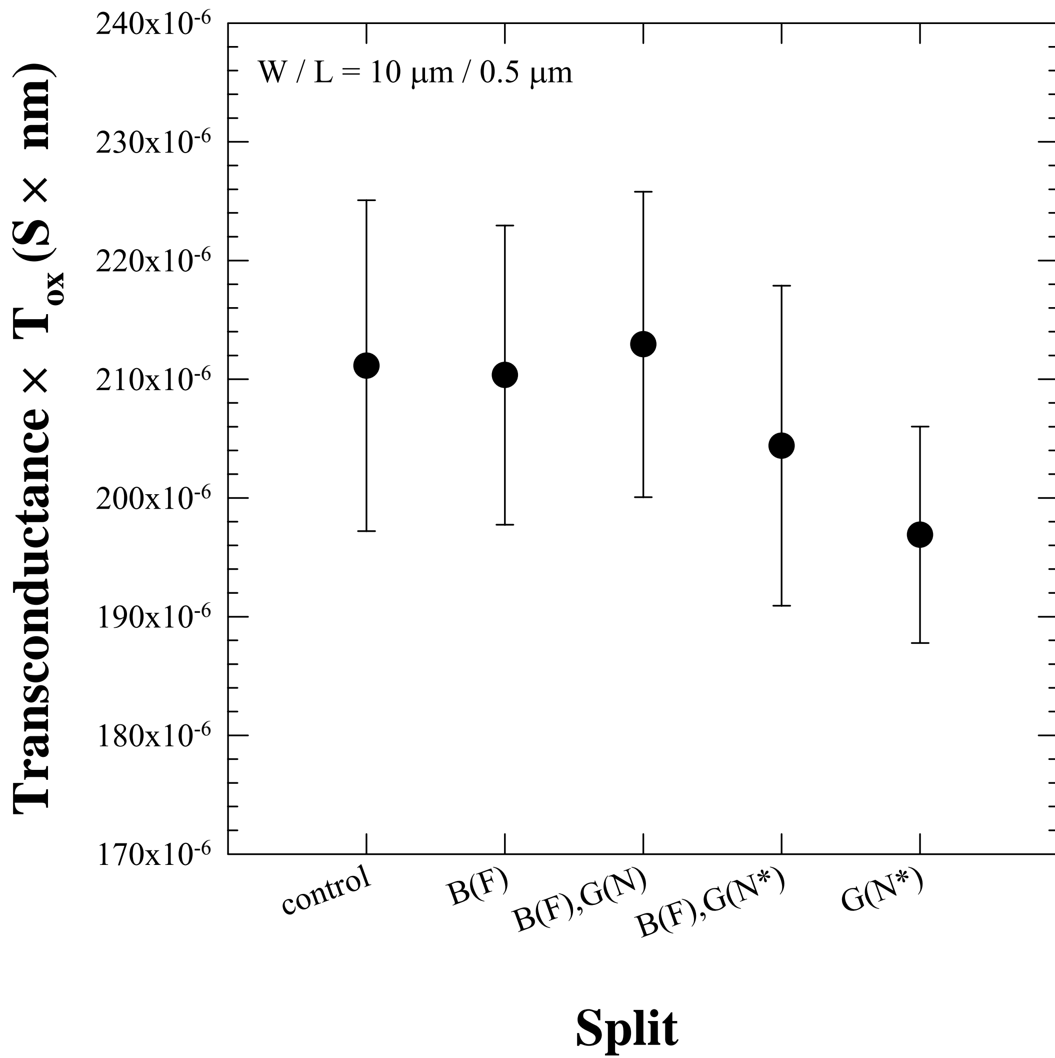


Fig. 3-4 Transconductance with different poly-silicon gate and bulk-Si implantation for 0.5 µm channel length

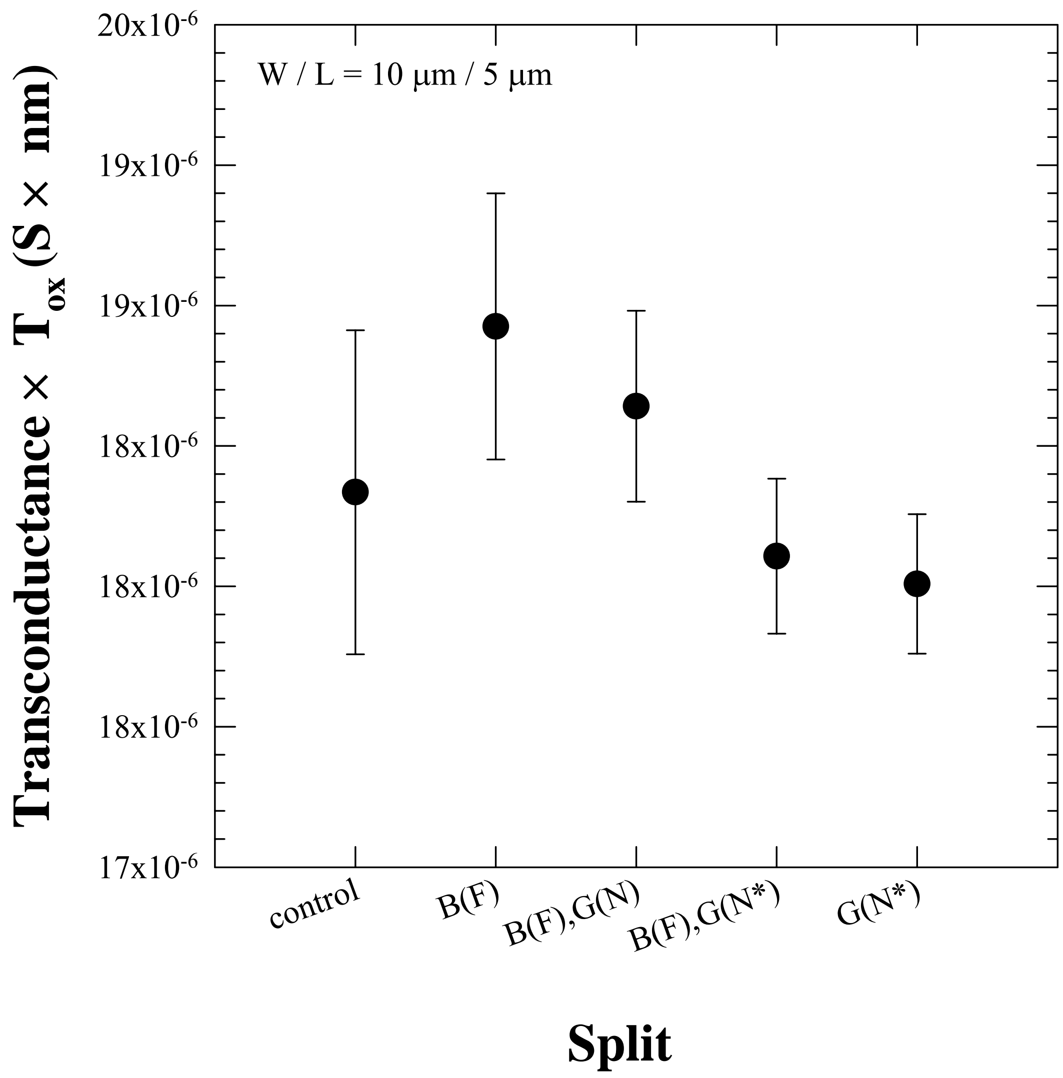


Fig. 3-5 Transconductance with different poly-silicon gate and bulk-Si implantation for 5 μm channel length

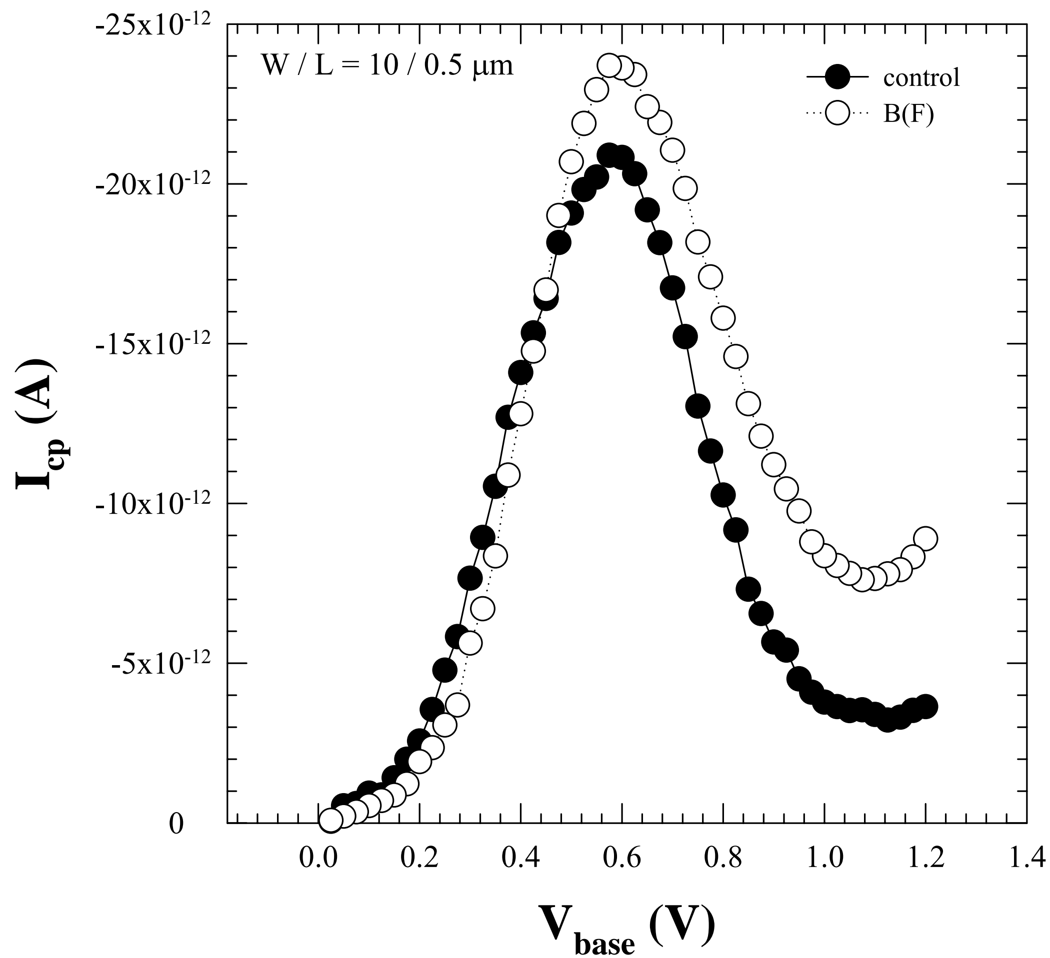


Fig. 3-6 Charge pumping current with control and bulk fluorine implantation for 0.5 μm channel length

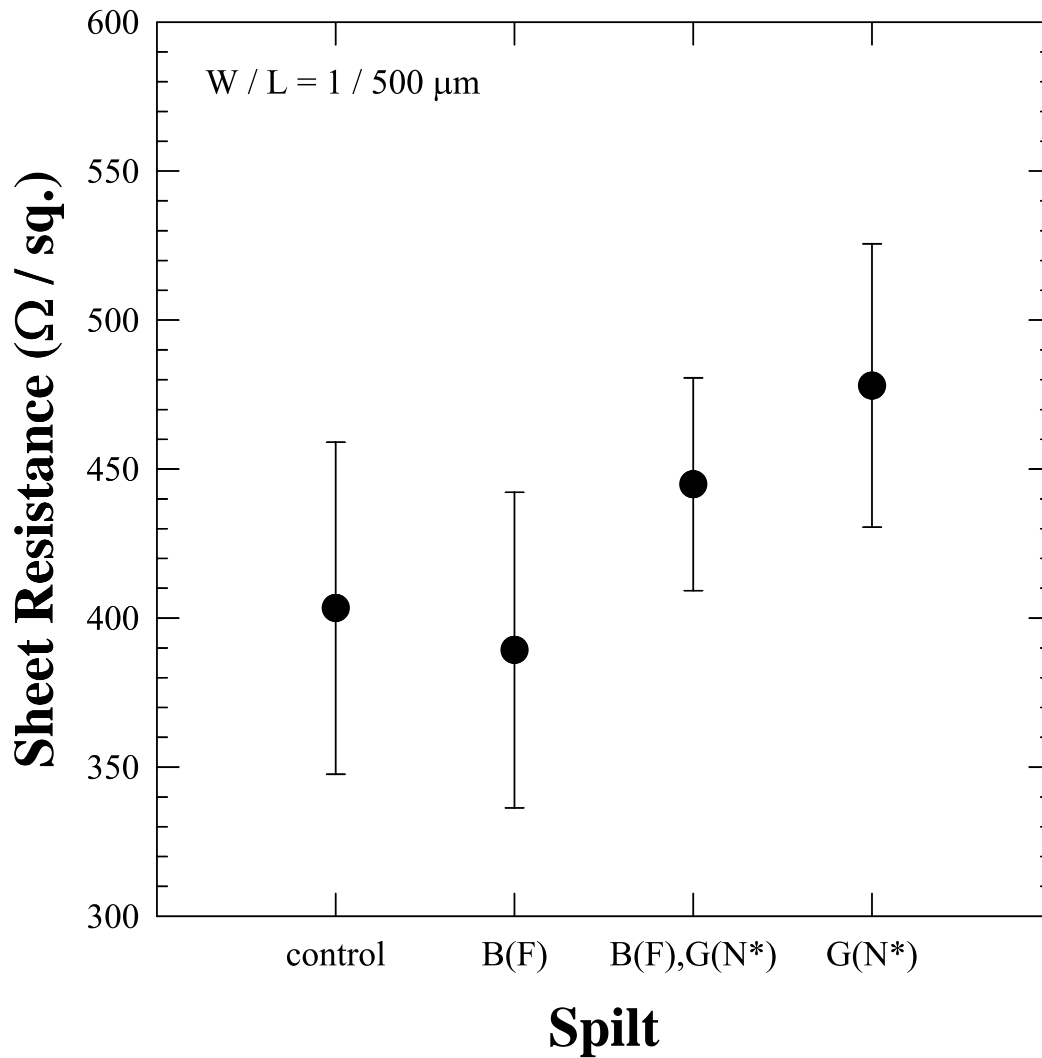


Fig. 3-7 Source/drain sheet resistance with different poly-silicon gate and bulk-Si implantation

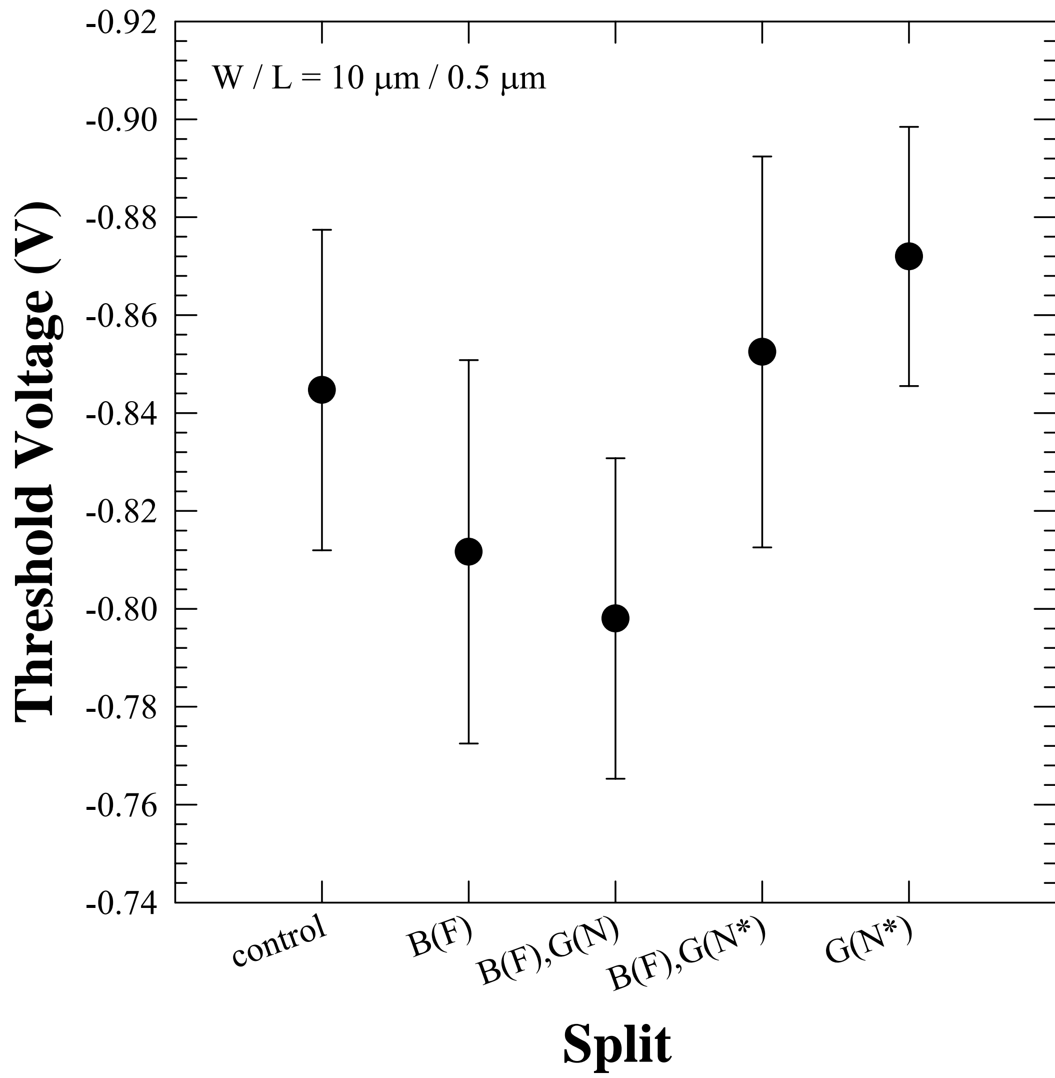


Fig. 3-8 Threshold voltage with different poly-silicon gate and bulk-Si implantation for 0.5 μm channel length

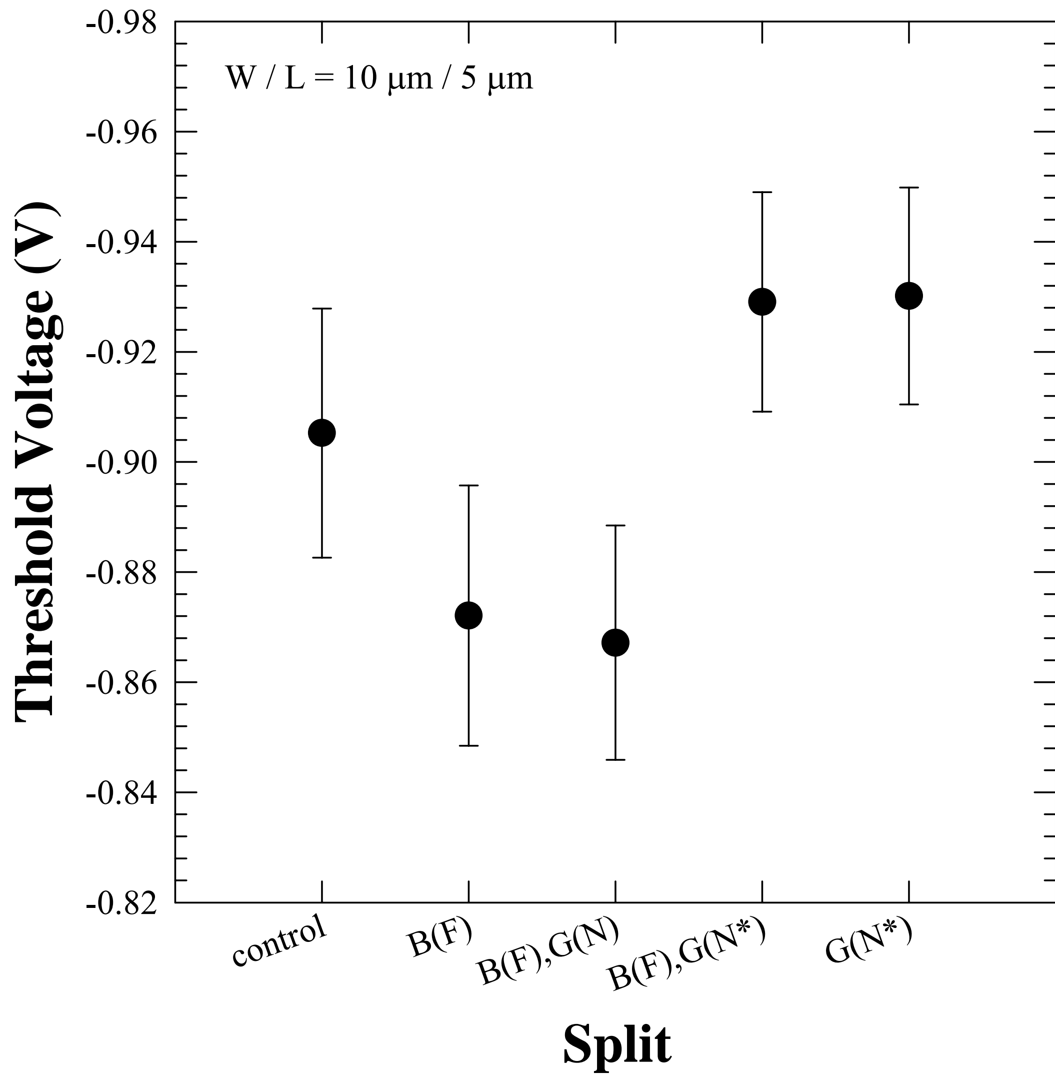


Fig. 3-9 Threshold voltage with different poly-silicon gate and bulk-Si implantation for 5 μm channel length

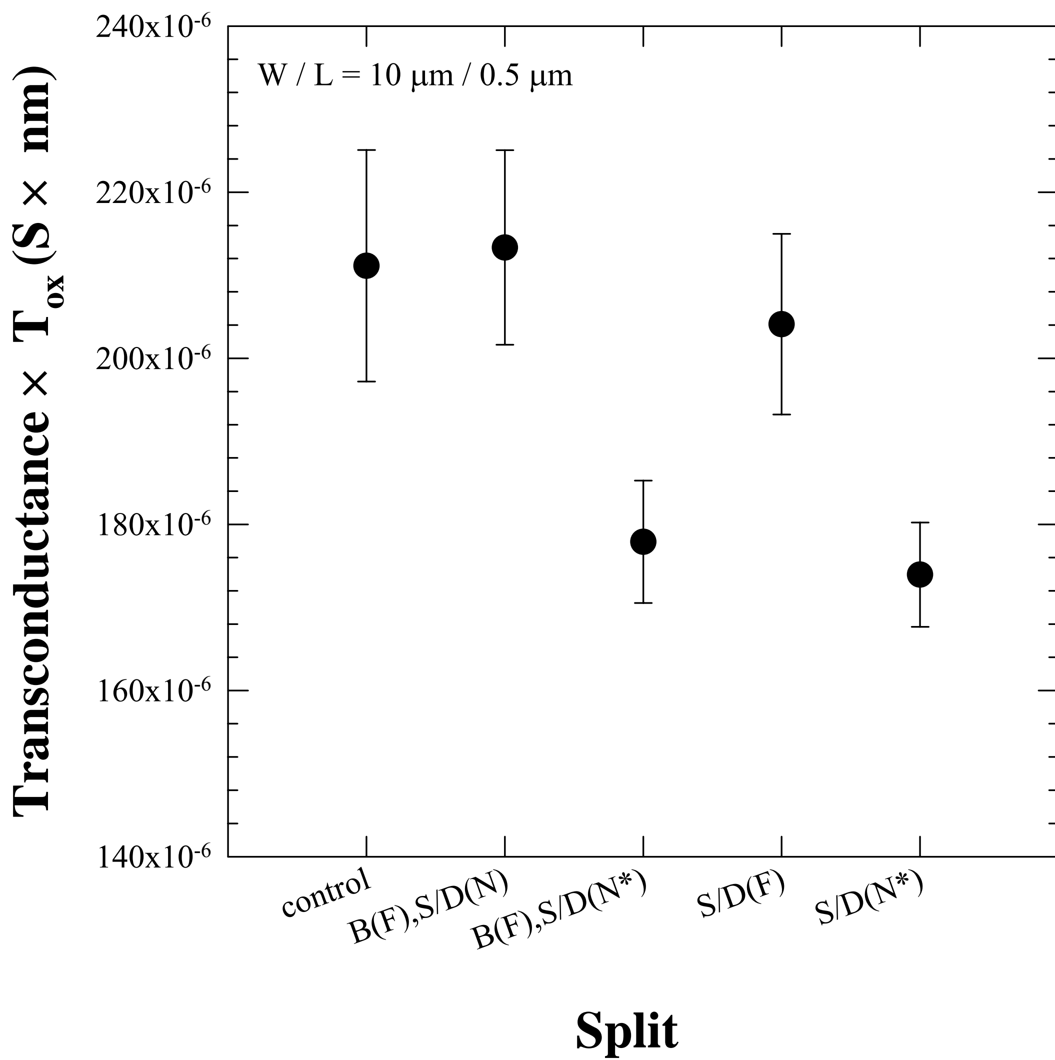


Fig. 3-10 Transconductance with different source/drain and bulk-Si implantation for 0.5 μm channel length

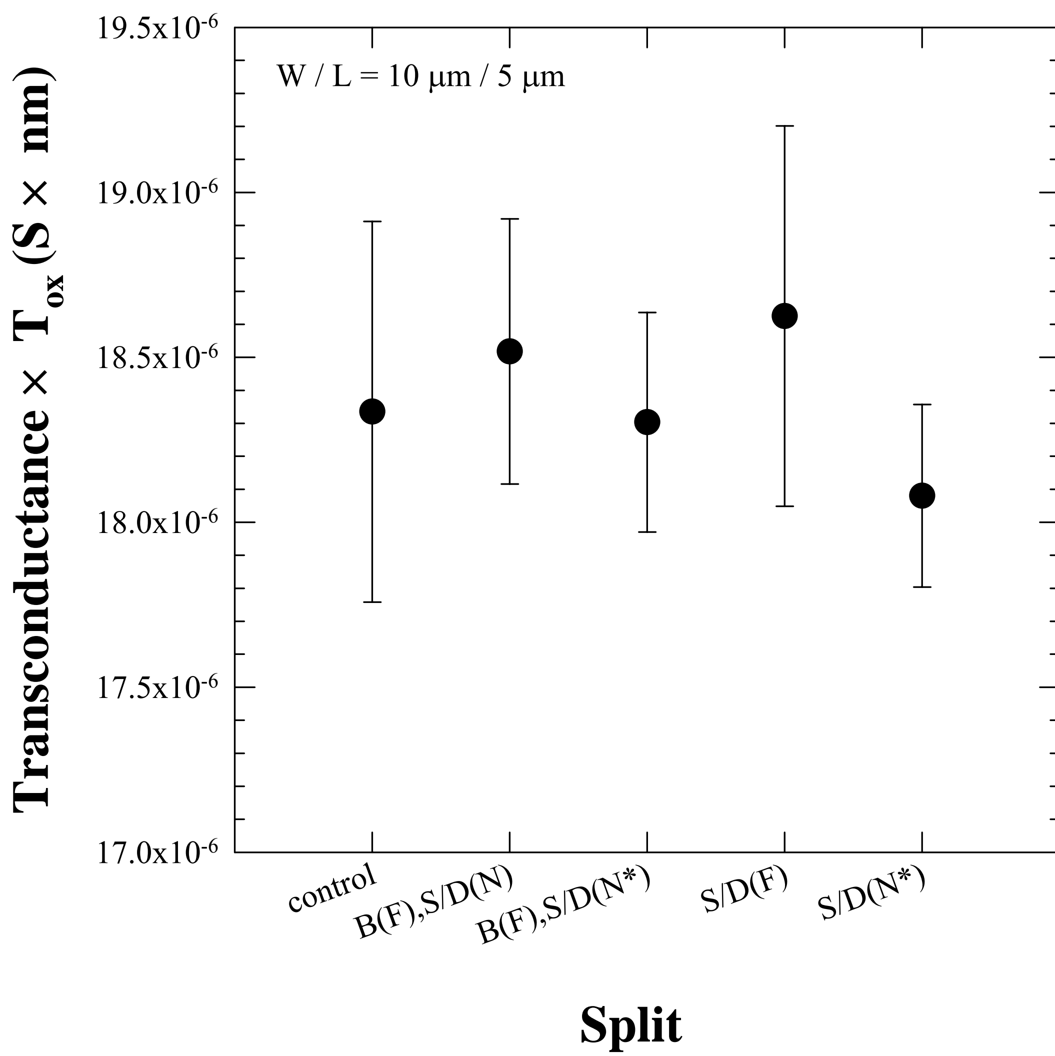


Fig. 3-11 Transconductance with different source/drain and bulk-Si implantation for 5 μm channel length

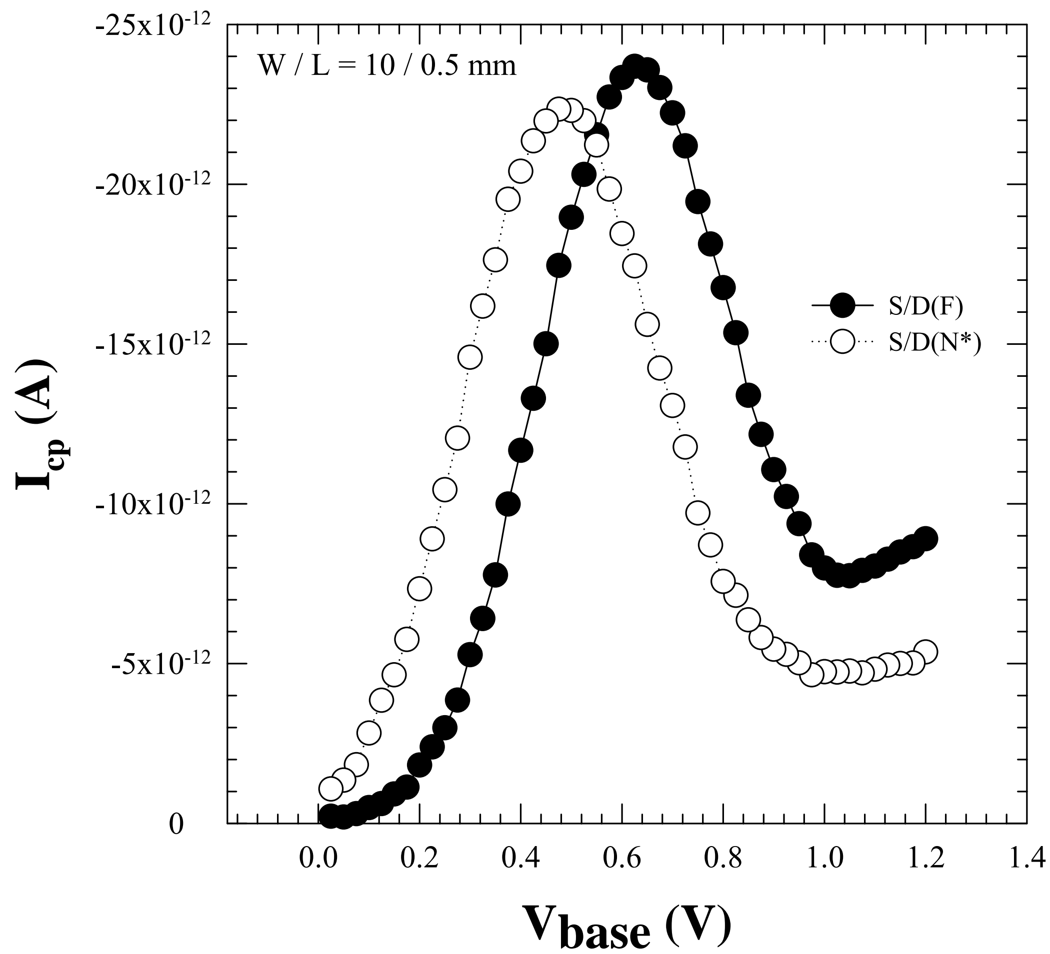


Fig. 3-12 Charge pumping current with different source/drain implantation for 0.5 µm channel length

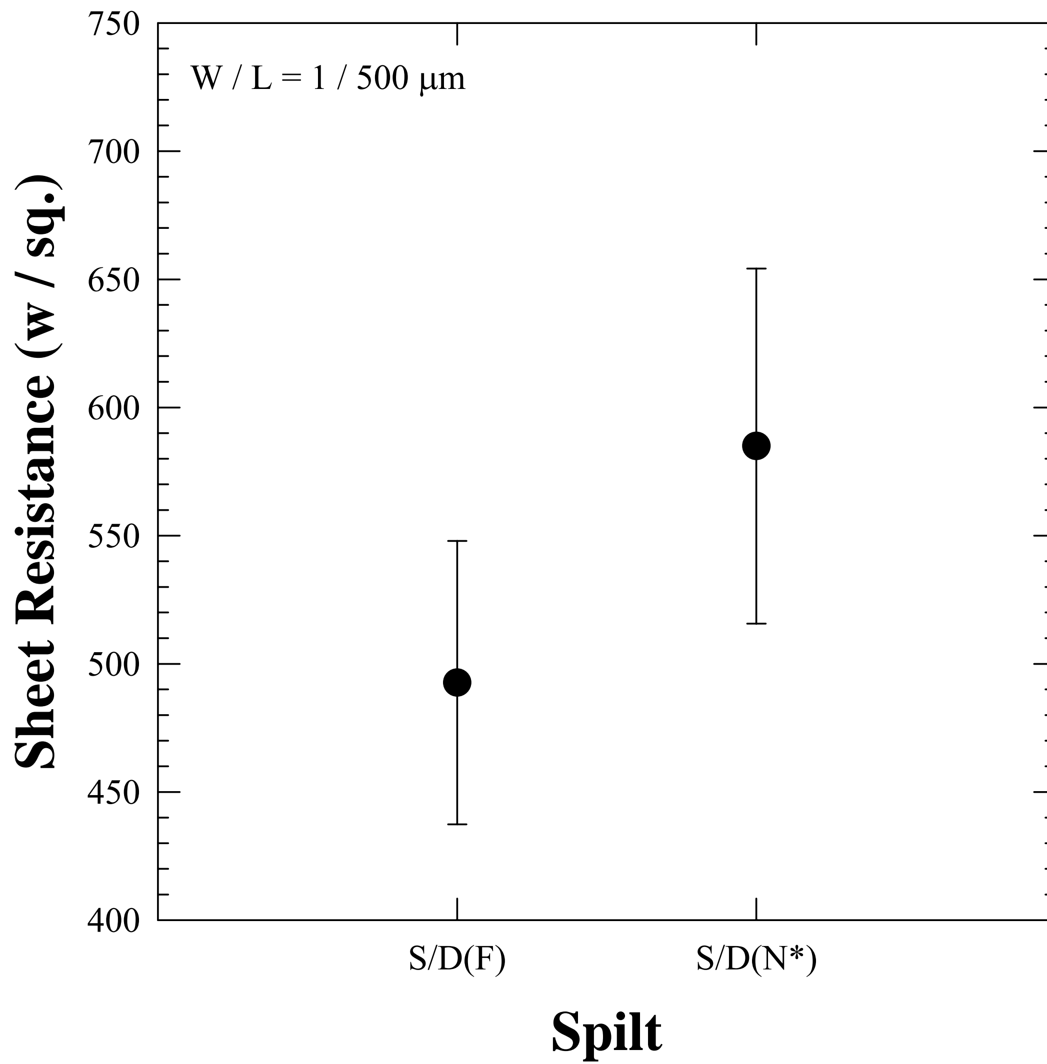


Fig. 3-13 Source/drain sheet resistance with different source/drain implantation

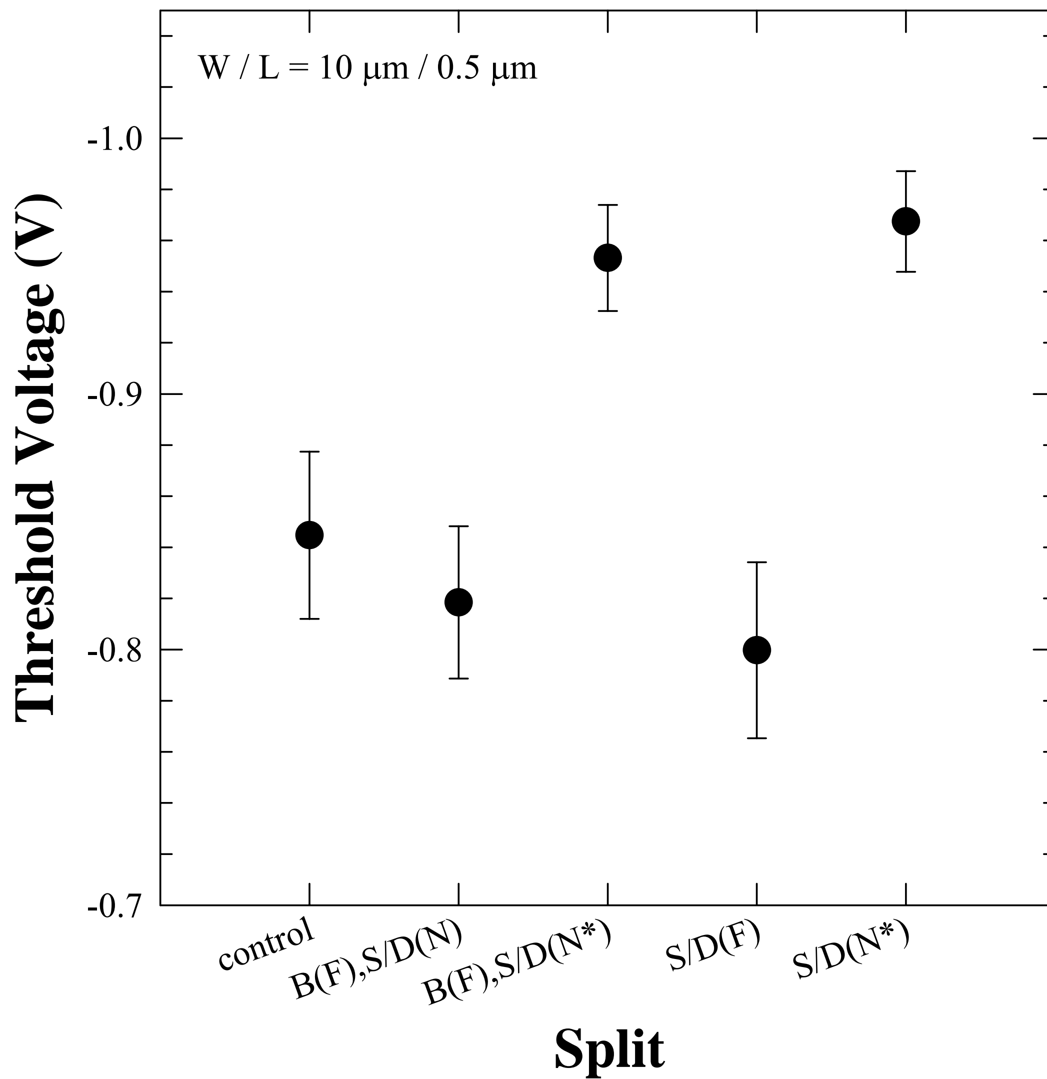


Fig. 3-14 Threshold voltage with different source/drain and bulk-Si implantation for 0.5 μm channel length

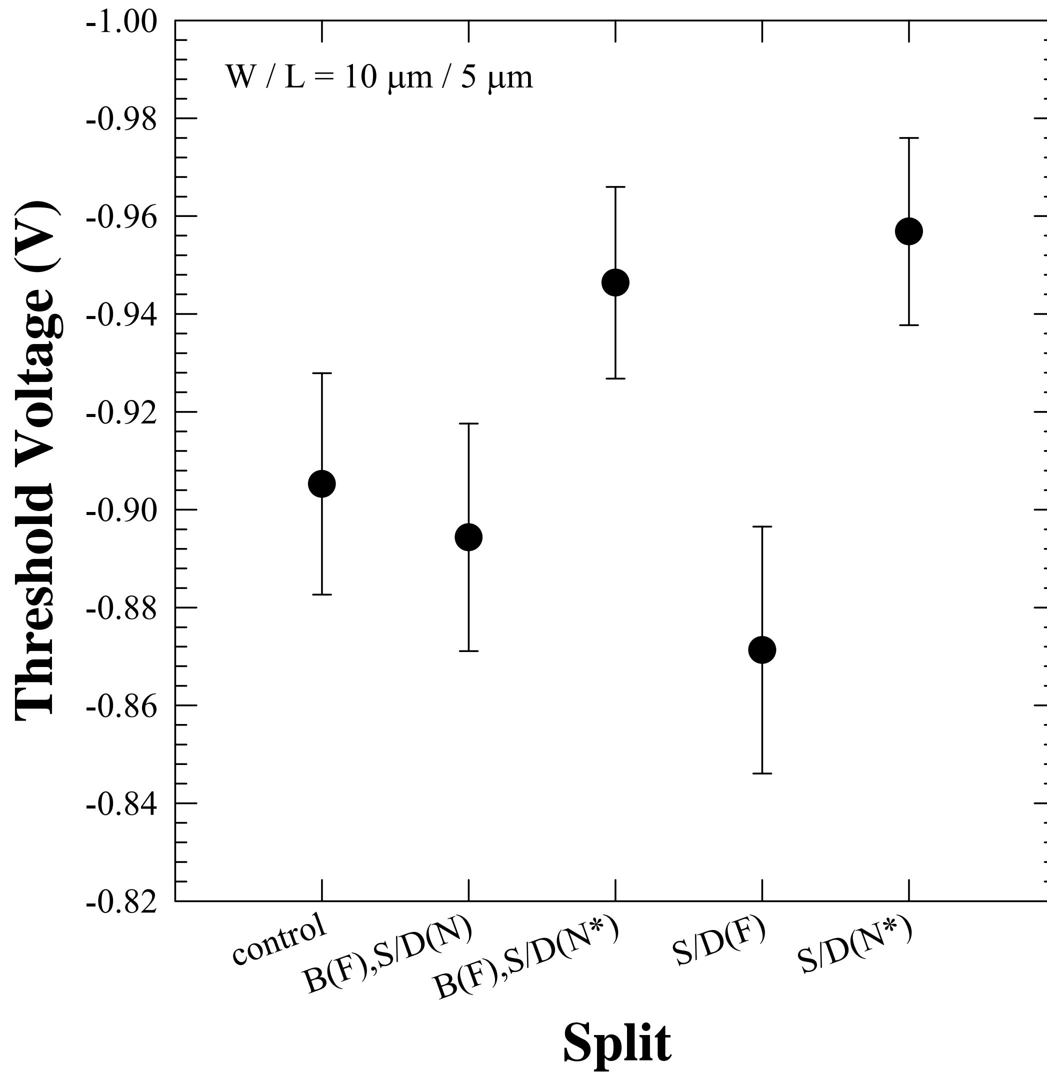


Fig. 3-15 Threshold voltage with different source/drain and bulk-Si implantation for 5 μm channel length

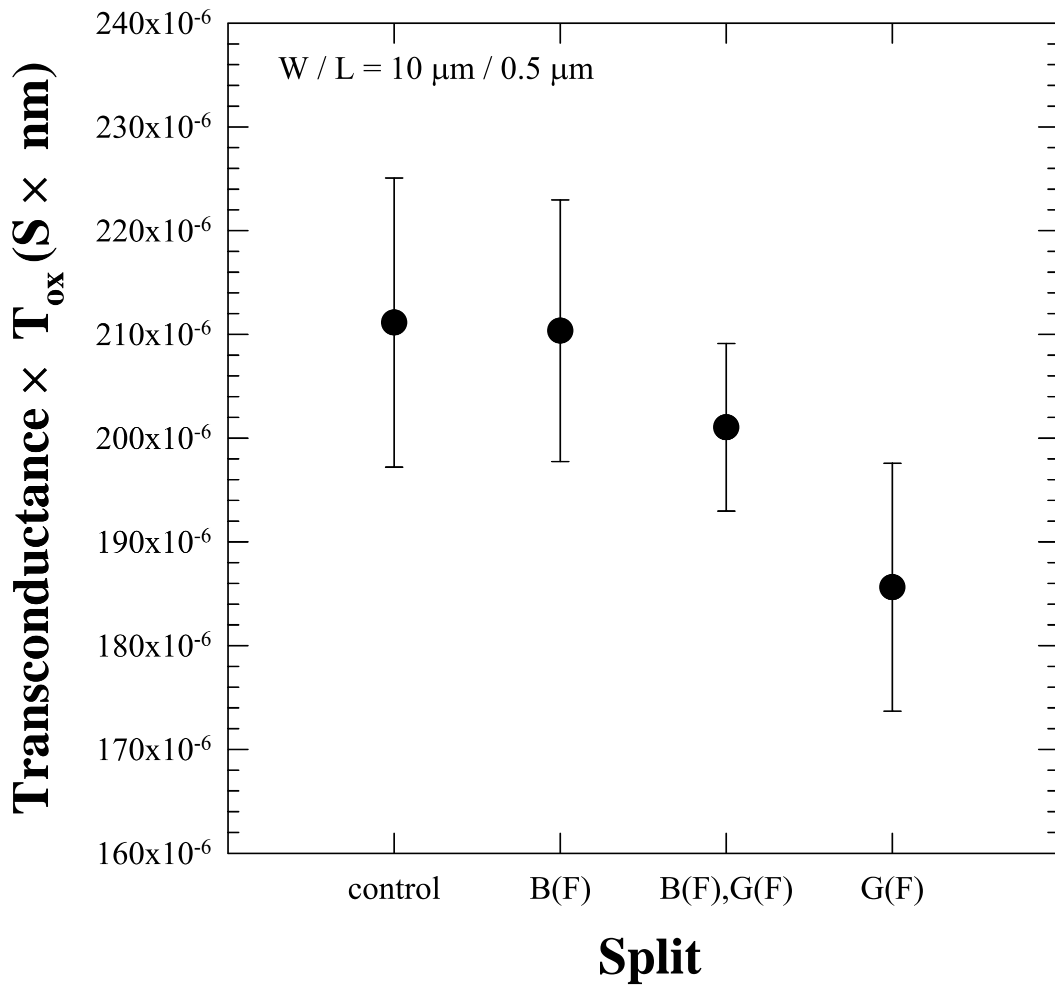


Fig. 3-16 Transconductance with different poly-silicon gate and bulk-Si implantation for 0.5 μm channel length

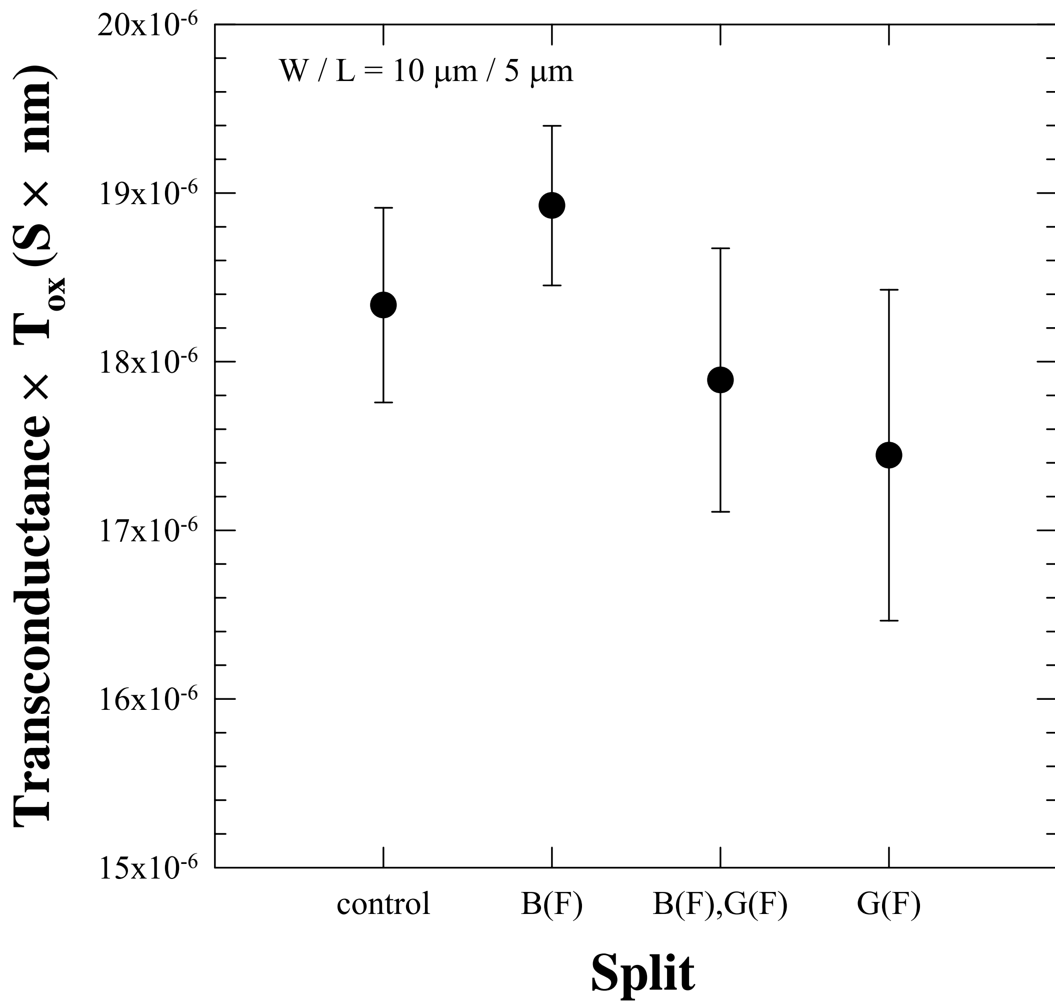


Fig. 3-17 Transconductance with different poly-silicon gate and bulk-Si implantation for 5 μm channel length

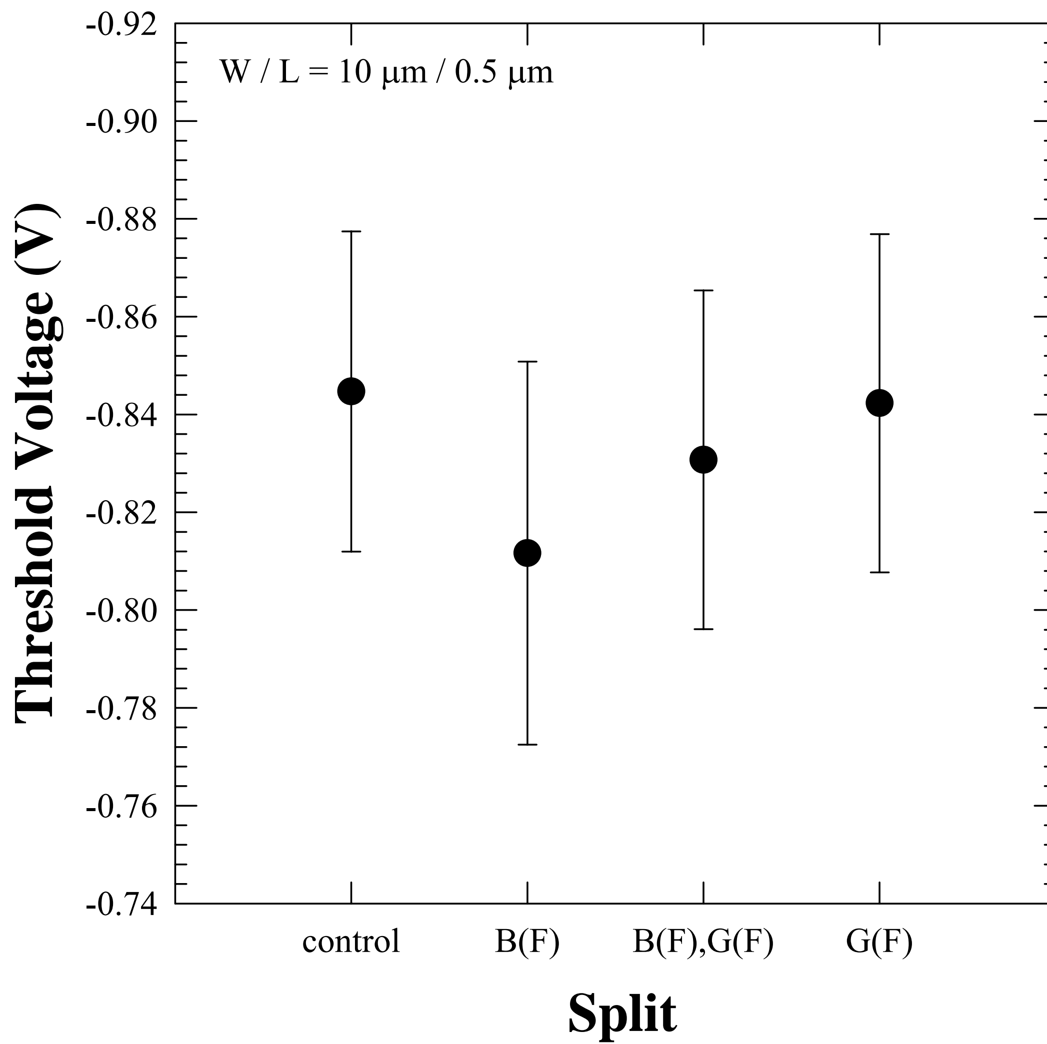


Fig. 3-18 Threshold voltage with different poly-silicon gate and bulk-Si implantation for 0.5 μm channel length

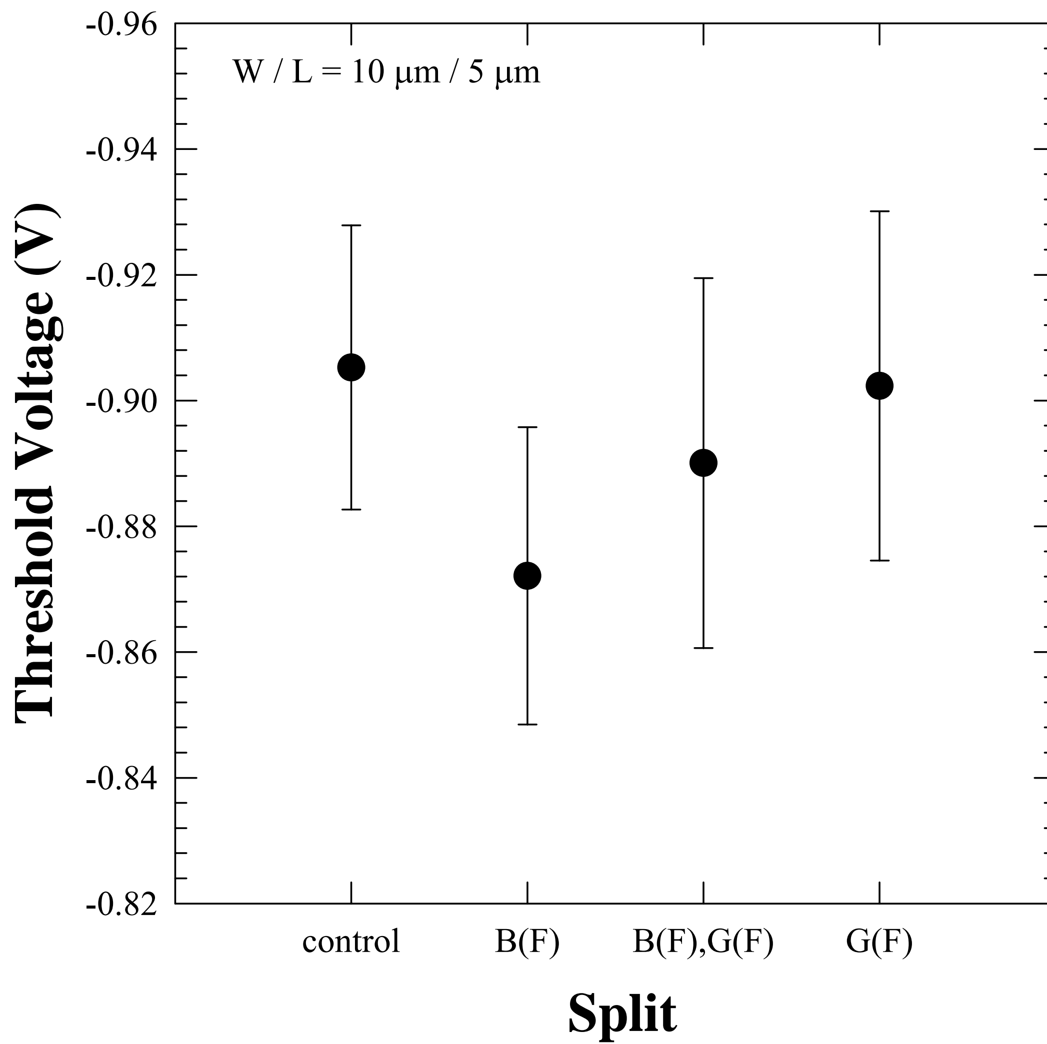


Fig. 3-19 Threshold voltage with different poly-silicon gate and bulk-Si implantation for 5 μm channel length

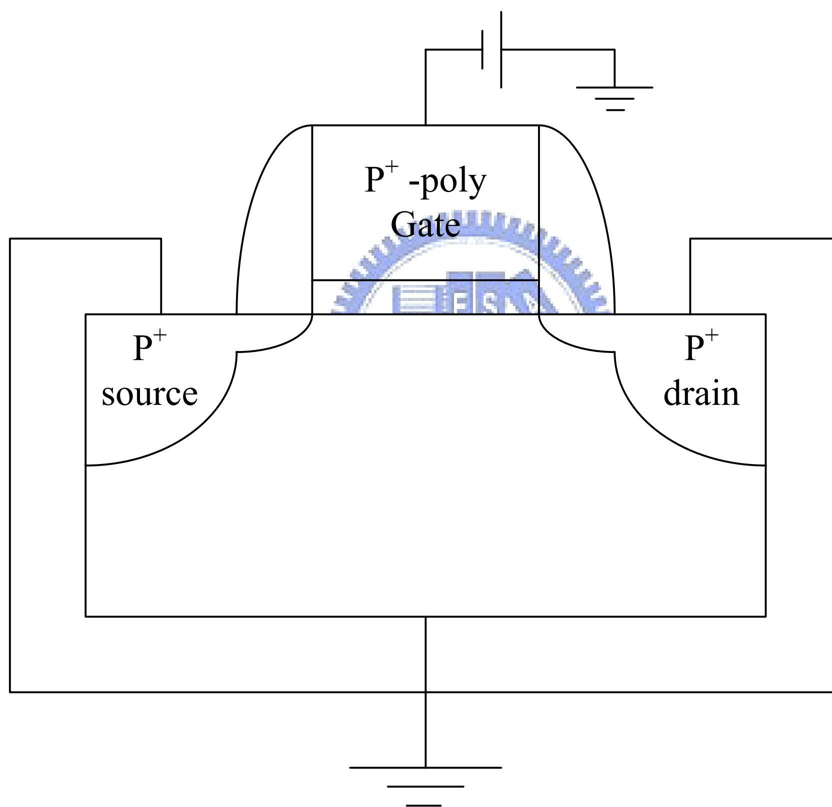


Fig. 4-1 A schematic illustration for NBTI stress setup.

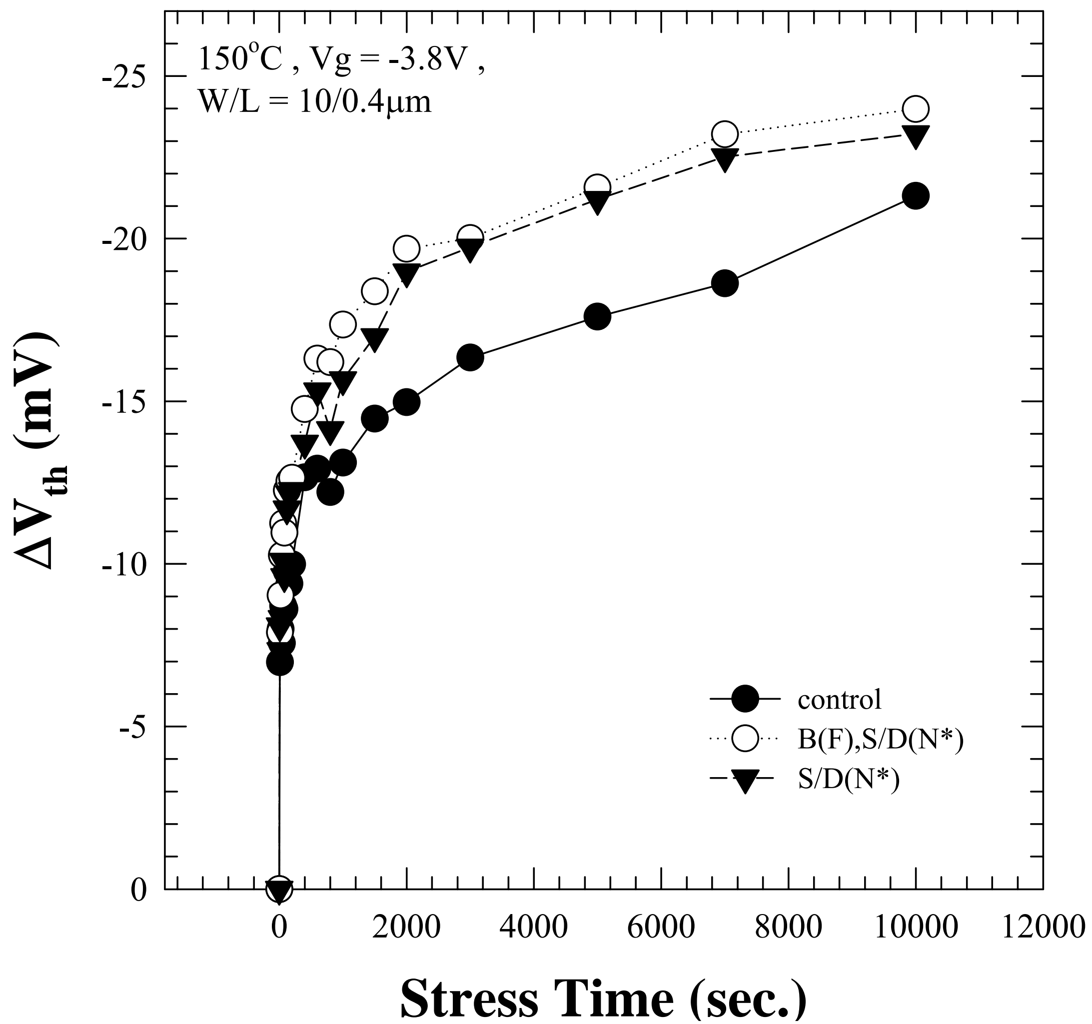


Fig. 4-2 ΔV_{th} versus stress time under NBTI stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length.

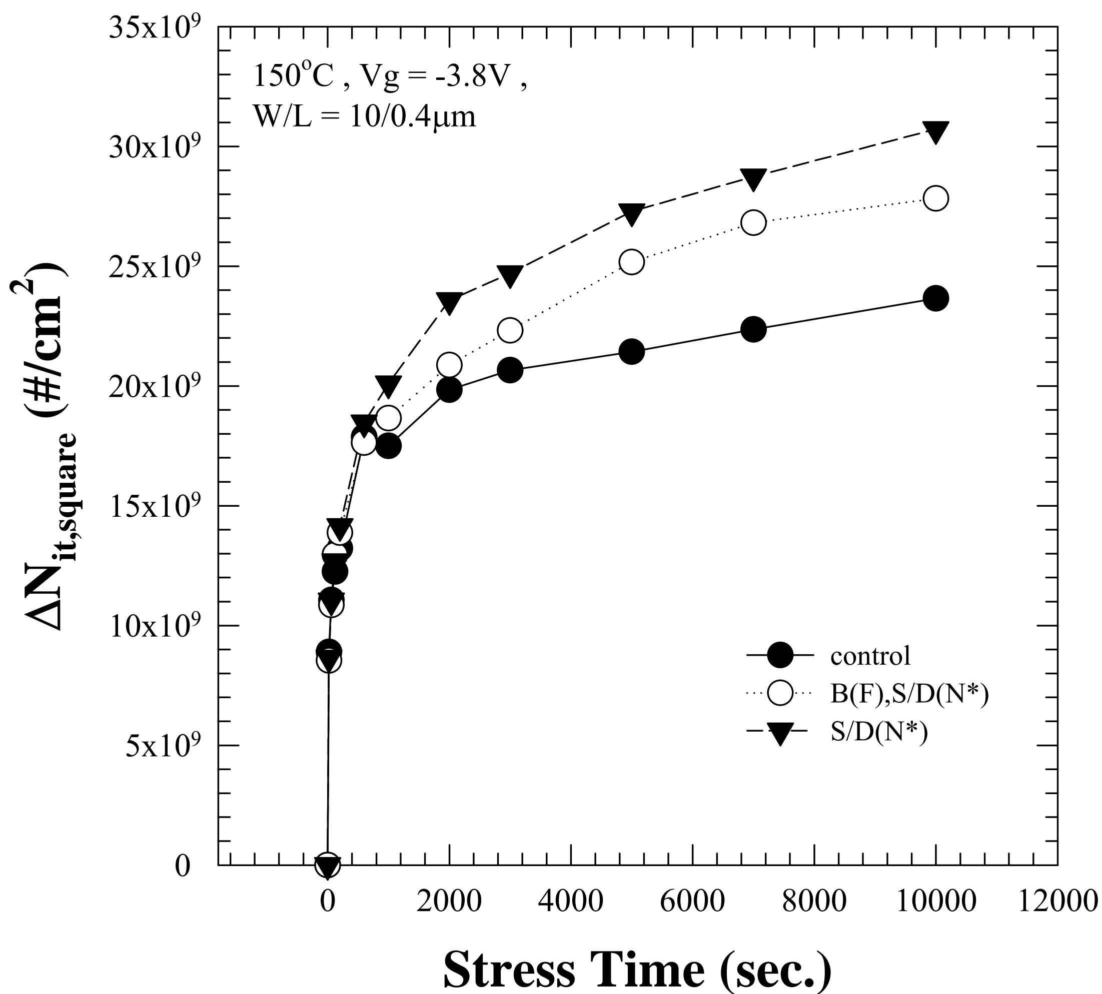


Fig. 4-3 Interface state versus stress time under NBTI stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length. (square wave)

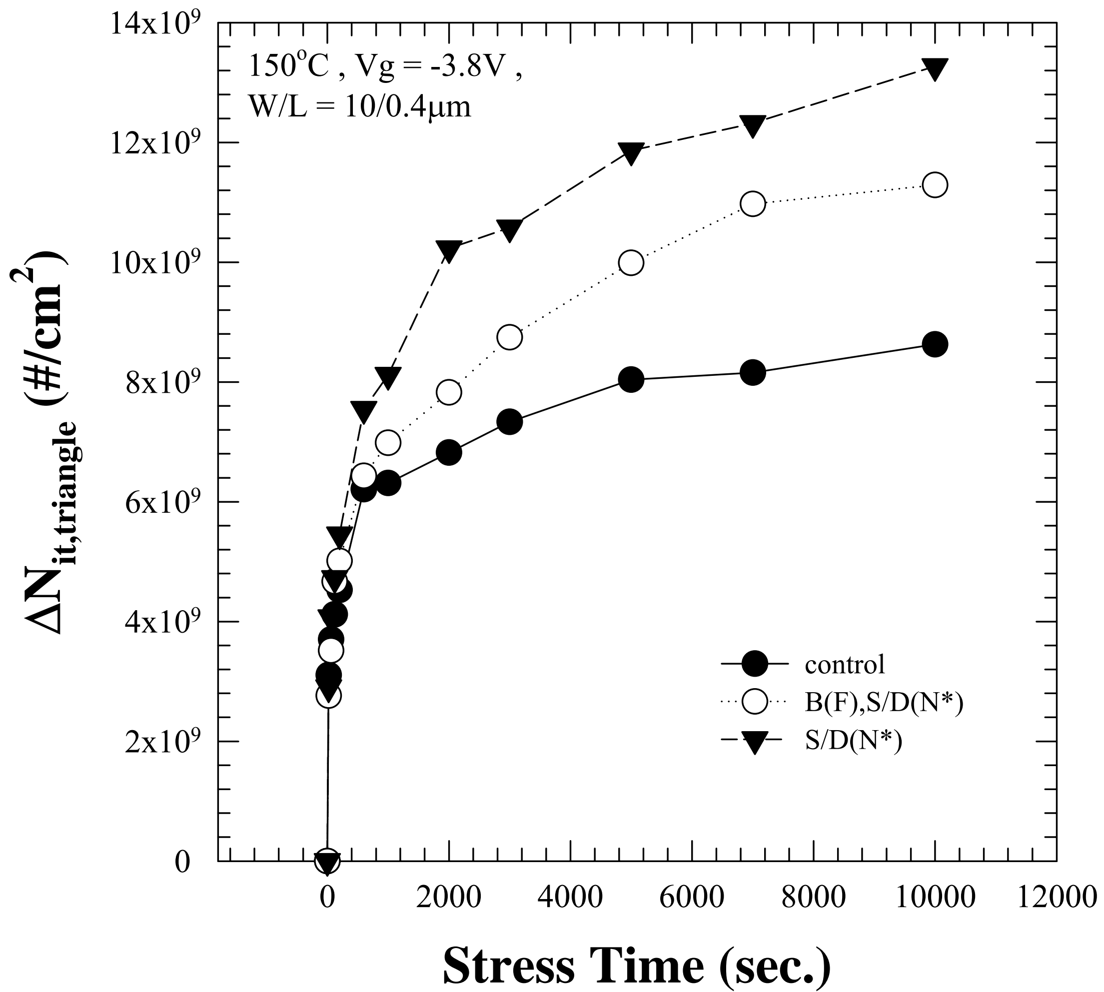


Fig. 4-4 Interface state versus stress time under NBTI stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length. (triangle wave)

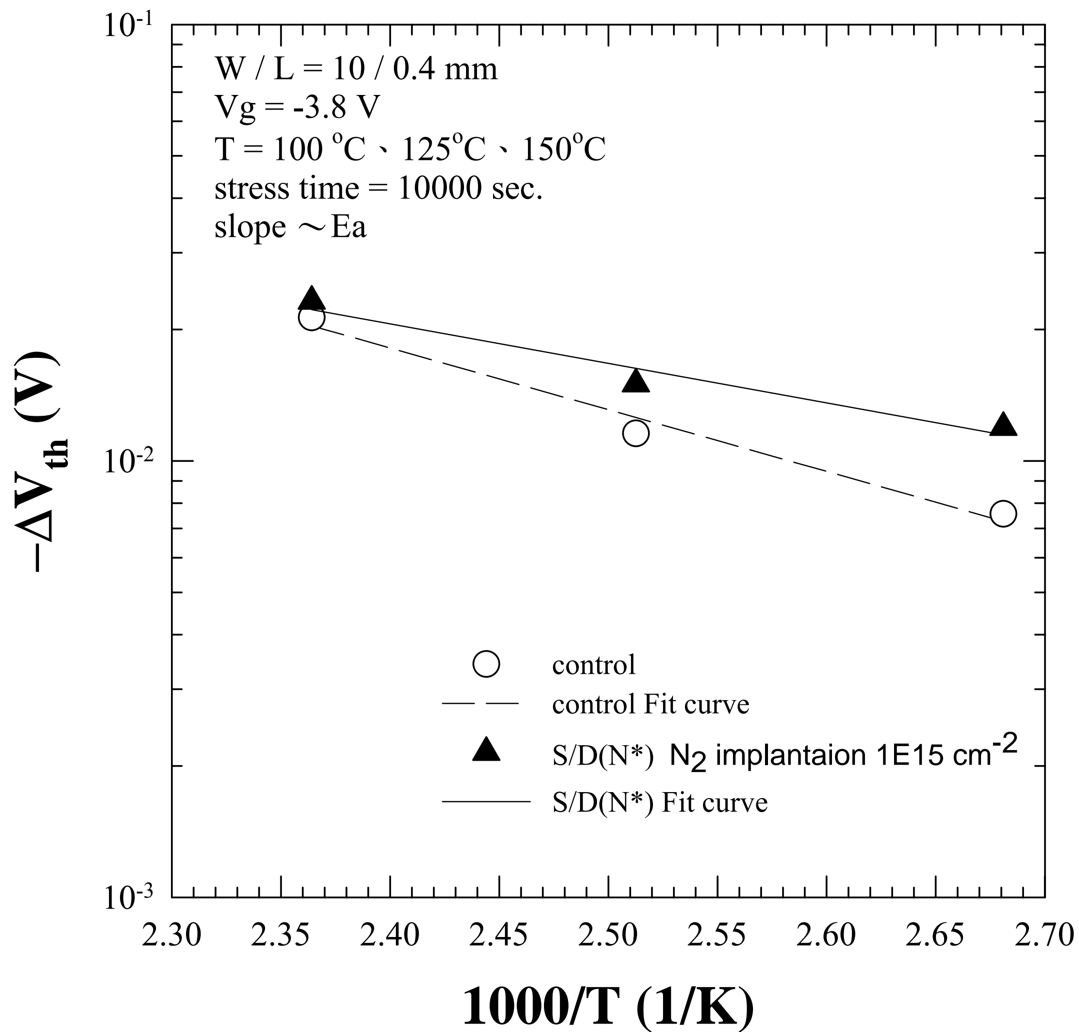


Fig. 4-5 Temperature dependence of NBTI stress for pMOSFETs with control and source/drain implantation for 0.4 μm channel length.

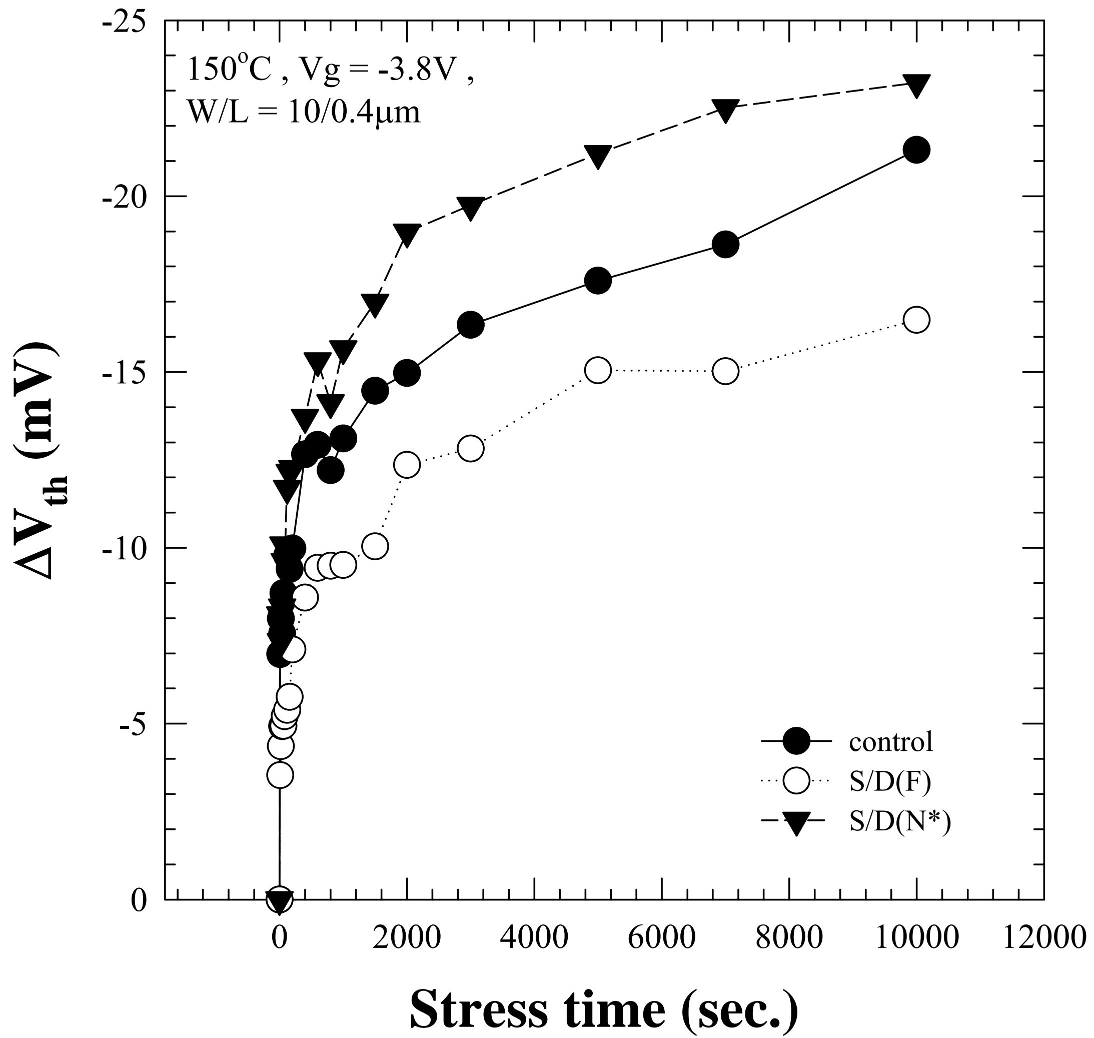


Fig. 4-6 ΔV_{th} versus stress time under NBTI stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length.

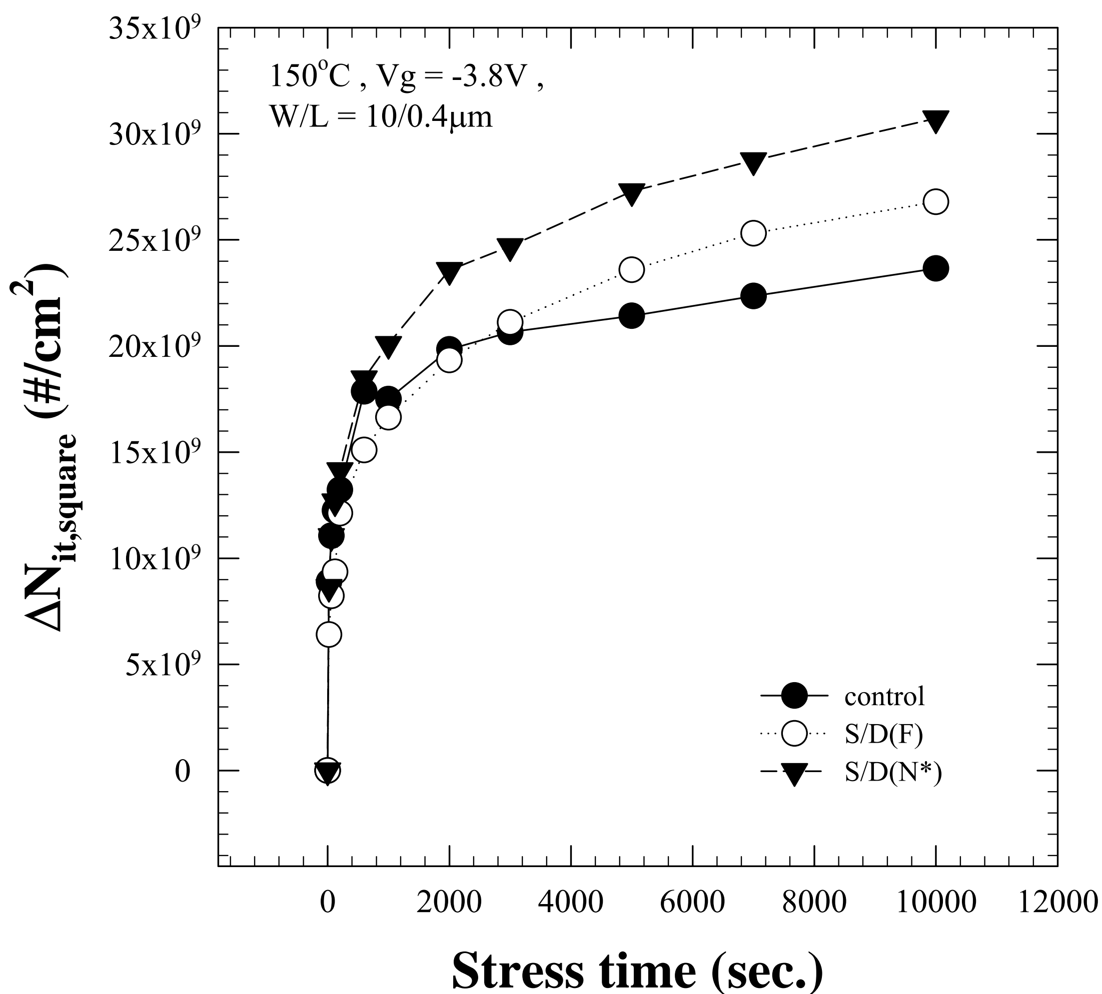


Fig. 4-7 Interface state versus stress time under NBTI stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length. (square wave)

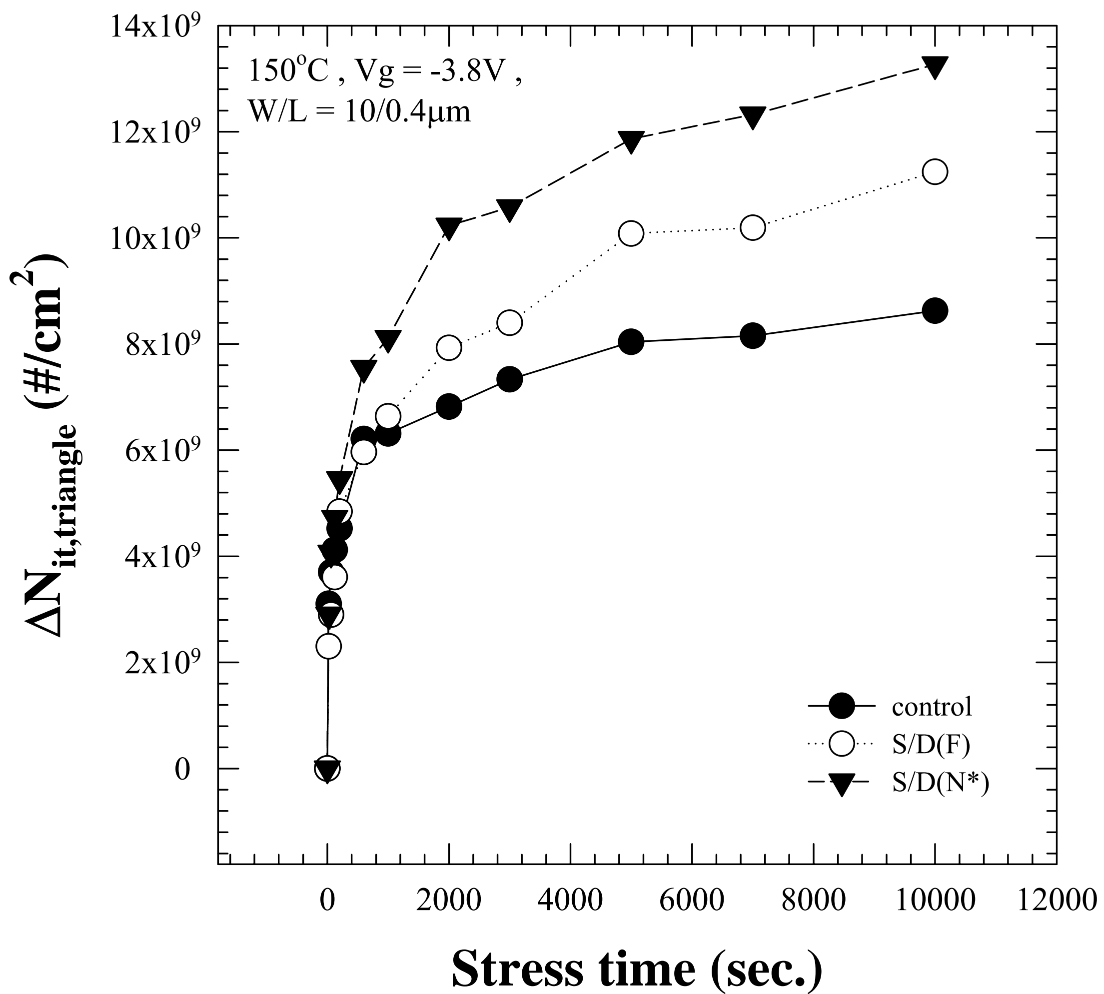


Fig. 4-8 Interface state versus stress time under NBTI stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length. (triangle wave)

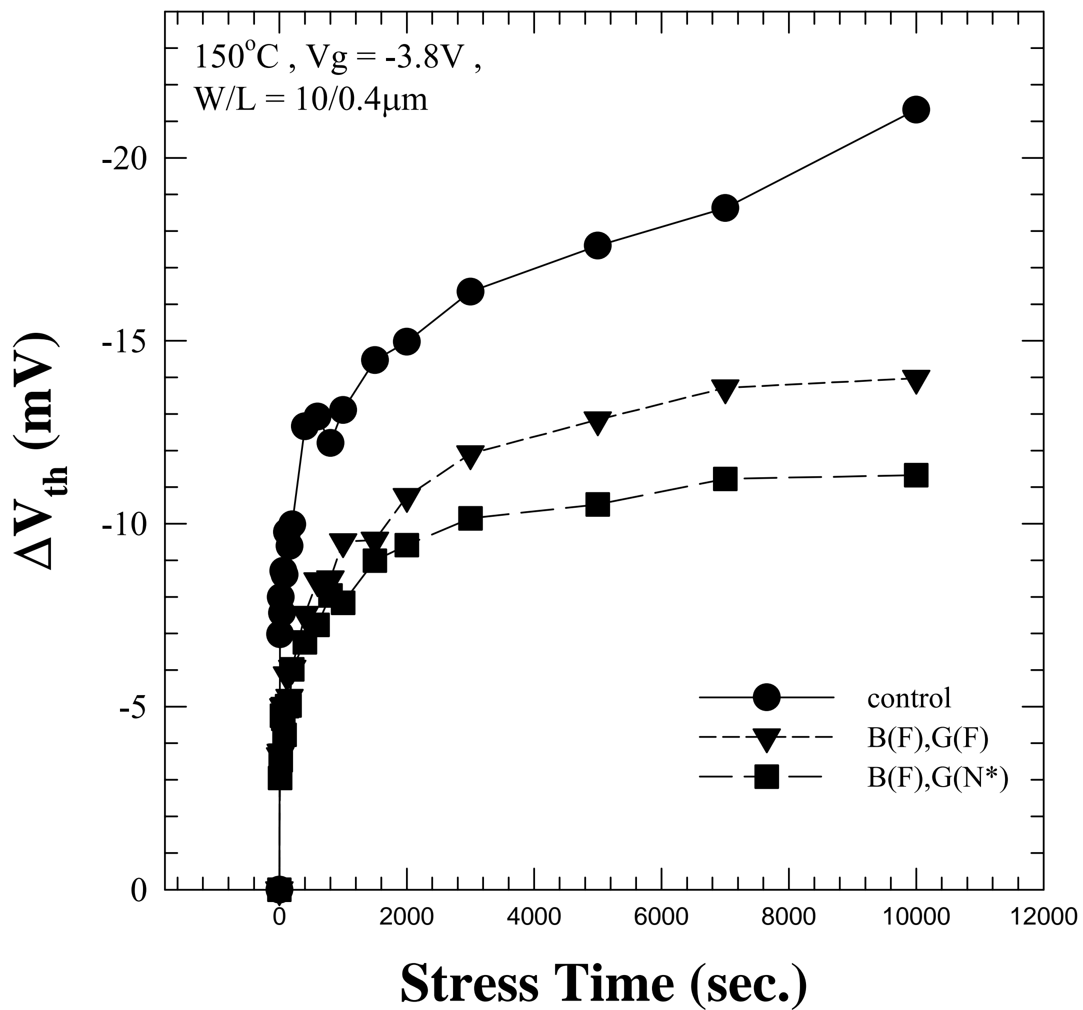


Fig. 4-9 ΔV_{th} versus stress time under NBTI stress for pMOSFETs with different poly-silicon gate and bulk-Si implantation for 0.4 μm channel length.

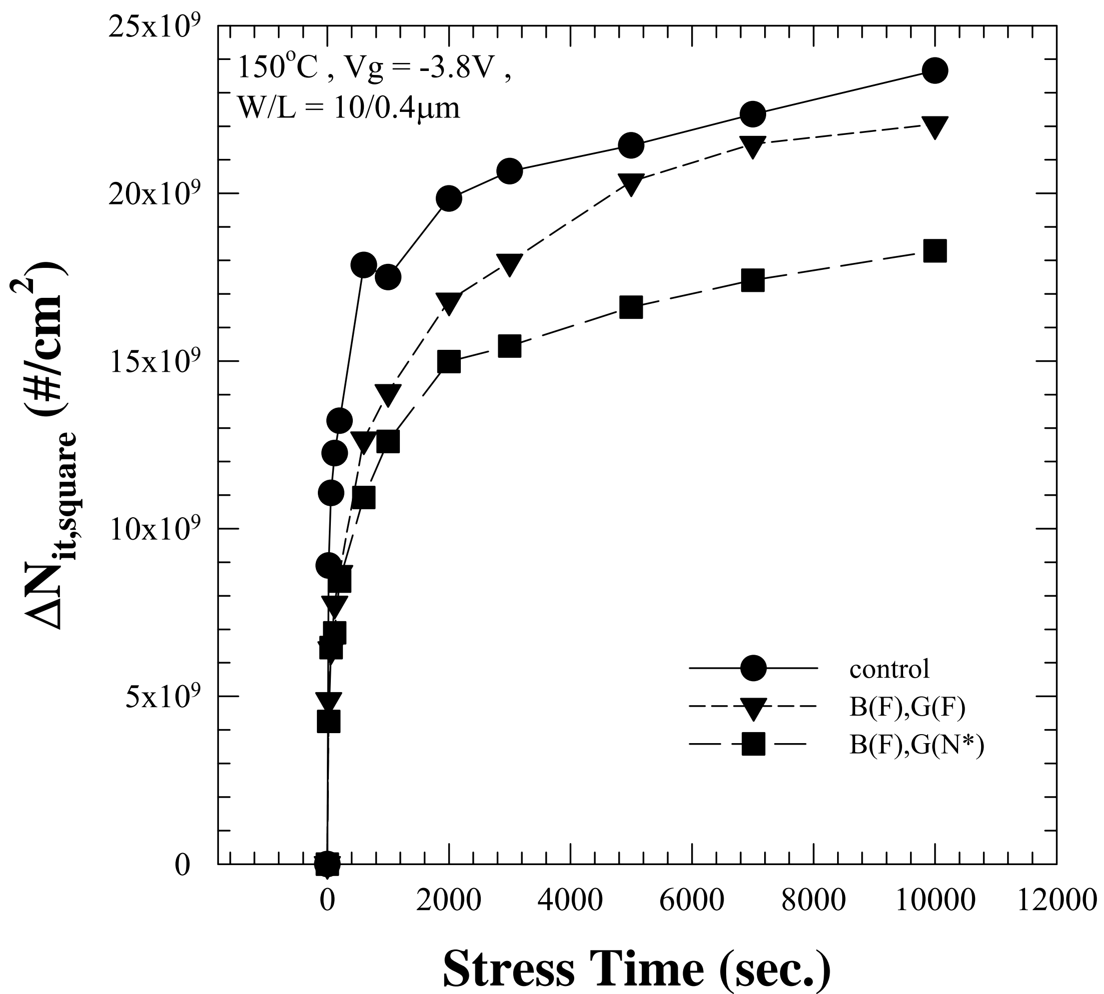


Fig. 4-10 Interface state versus stress time under NBTI stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length. (square wave)

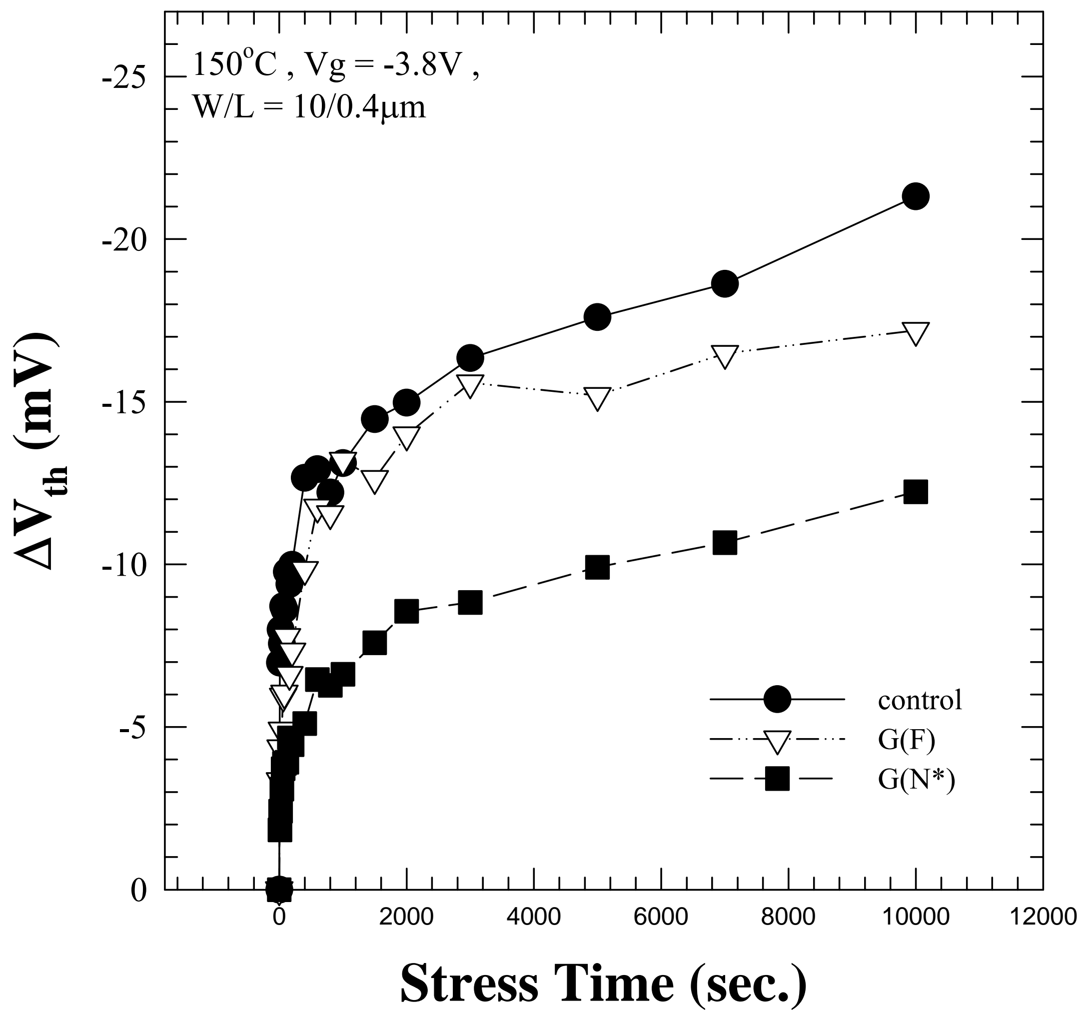


Fig. 4-11 ΔV_{th} versus stress time under NBTI stress for pMOSFETs with different poly-silicon gate implantation for 0.4 μm channel length.

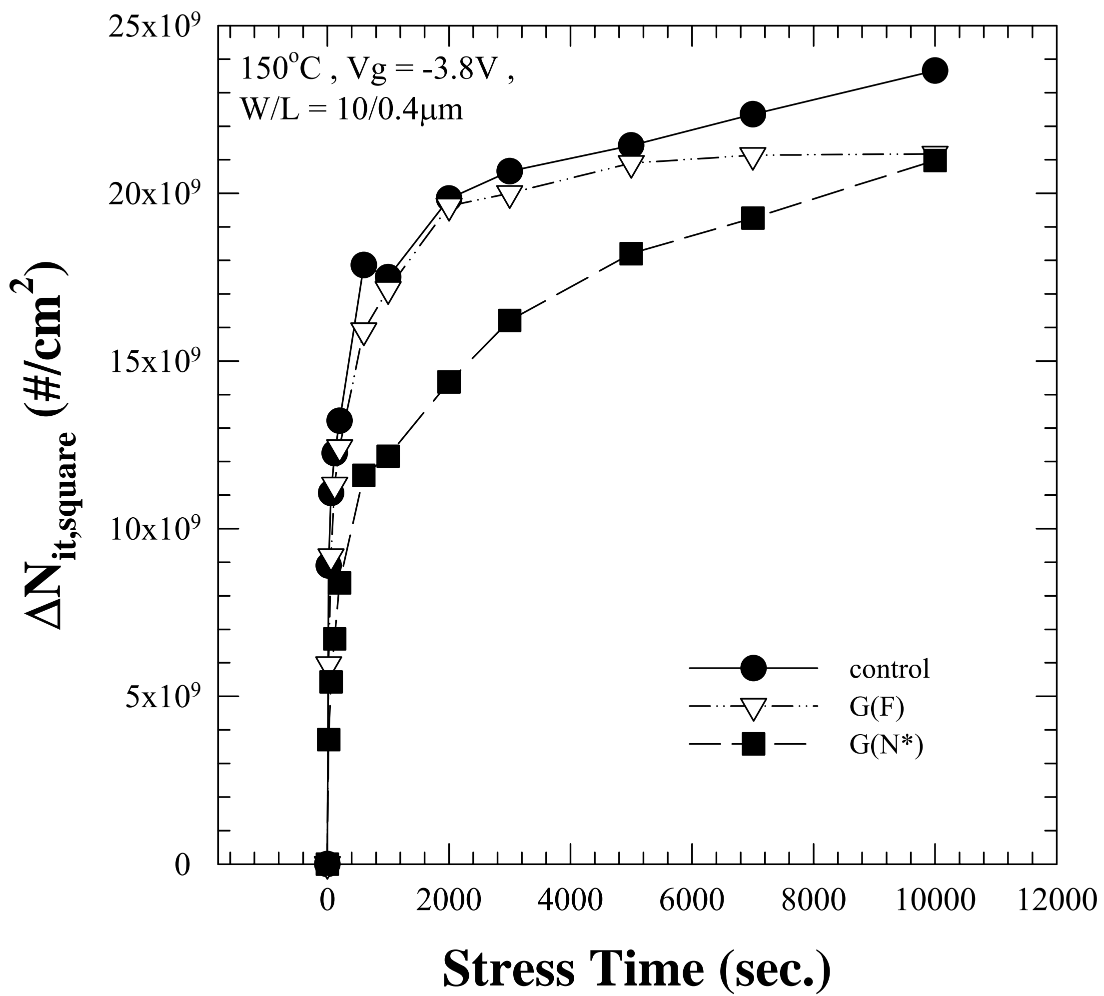


Fig. 4-12 Interface state versus stress time under NBTI stress for pMOSFETs with different poly-silicon gate implantation for 0.4 μm channel length. (square wave)

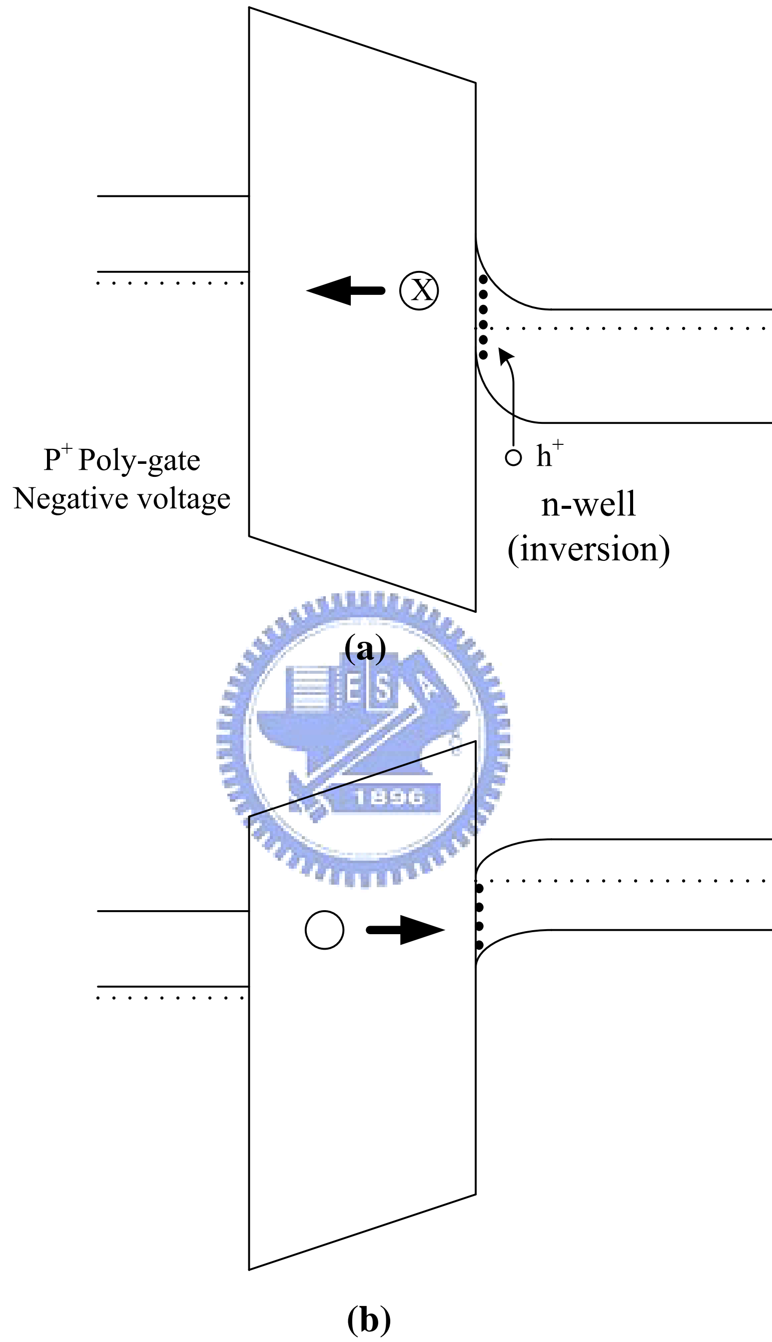


Fig. 5-1 (a) Nit generation. (b) Nit passivation. X stands for hydrogen-related species.

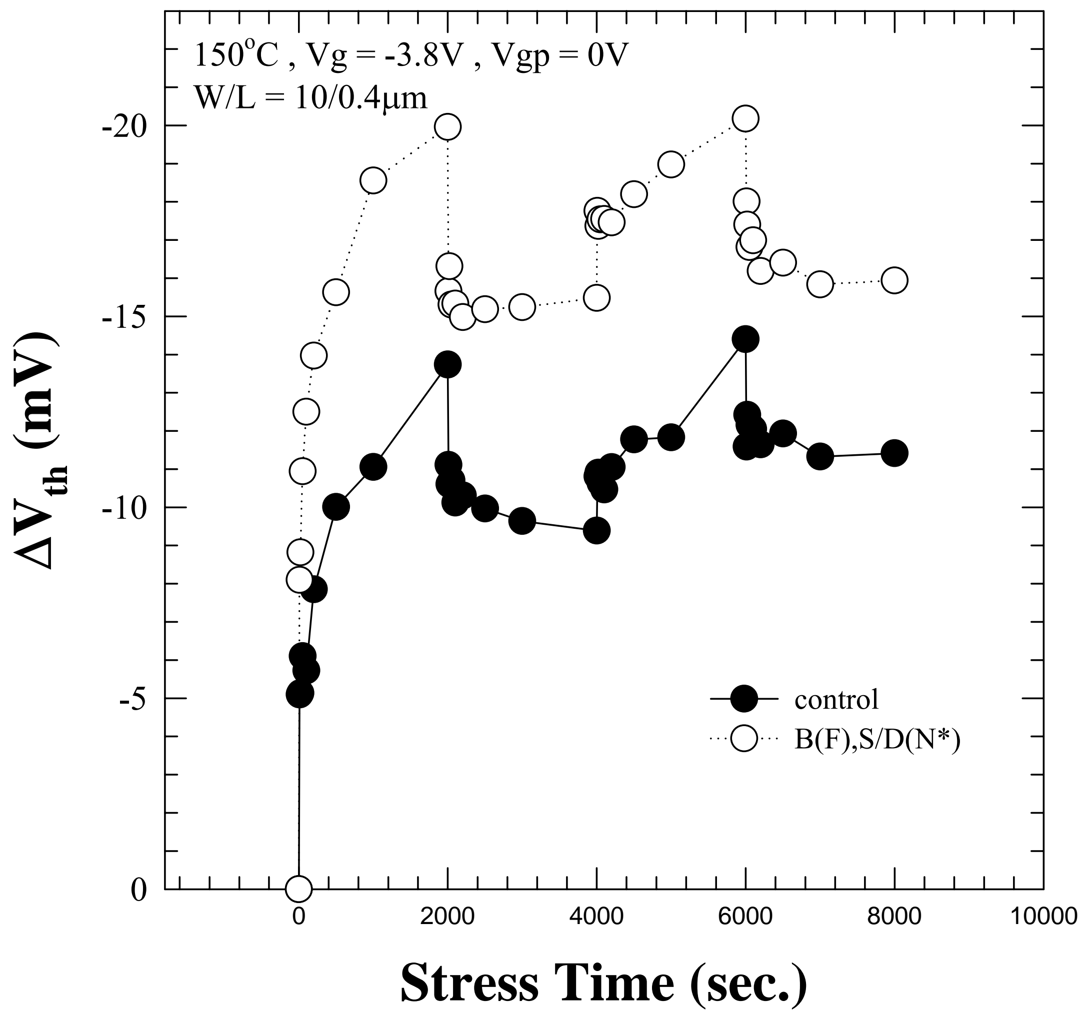


Fig. 5-2 ΔV_{th} versus stress time under stress-passivation-stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length

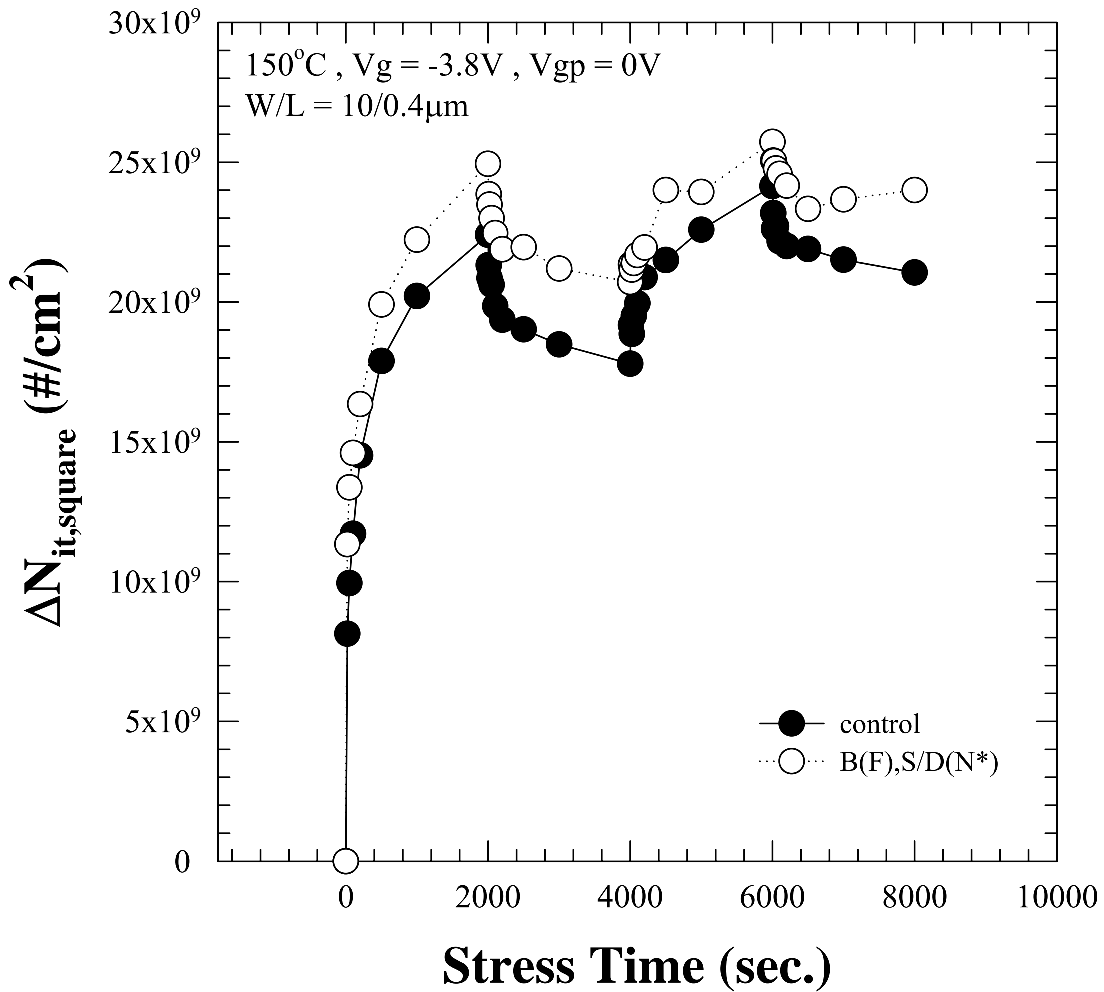


Fig. 5-3 Interface state versus stress time under stress-passivation-stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length(square wave)

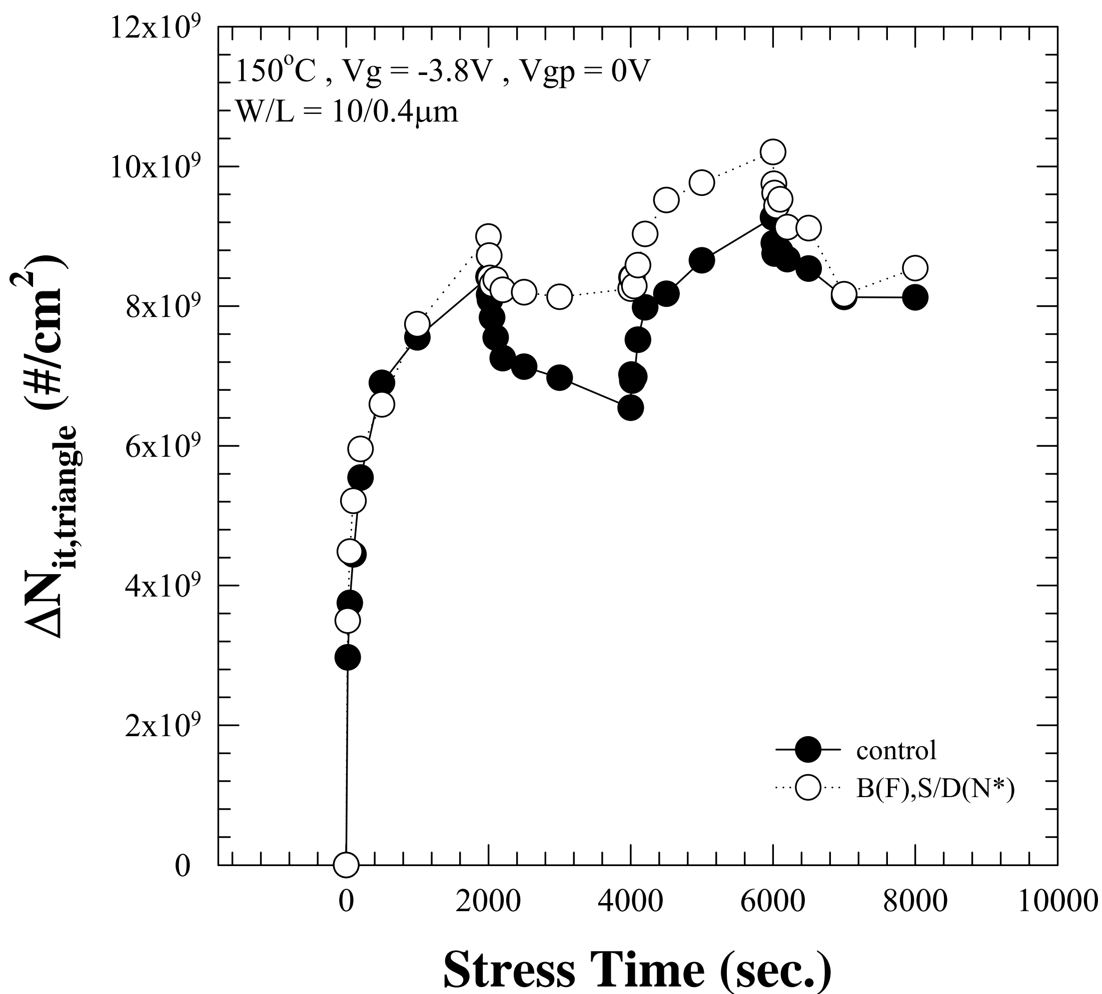


Fig. 5-4 Interface state versus stress time under stress-passivation-stress for pMOSFETs with different source/drain and bulk-Si implantation for 0.4 μm channel length (triangle wave)

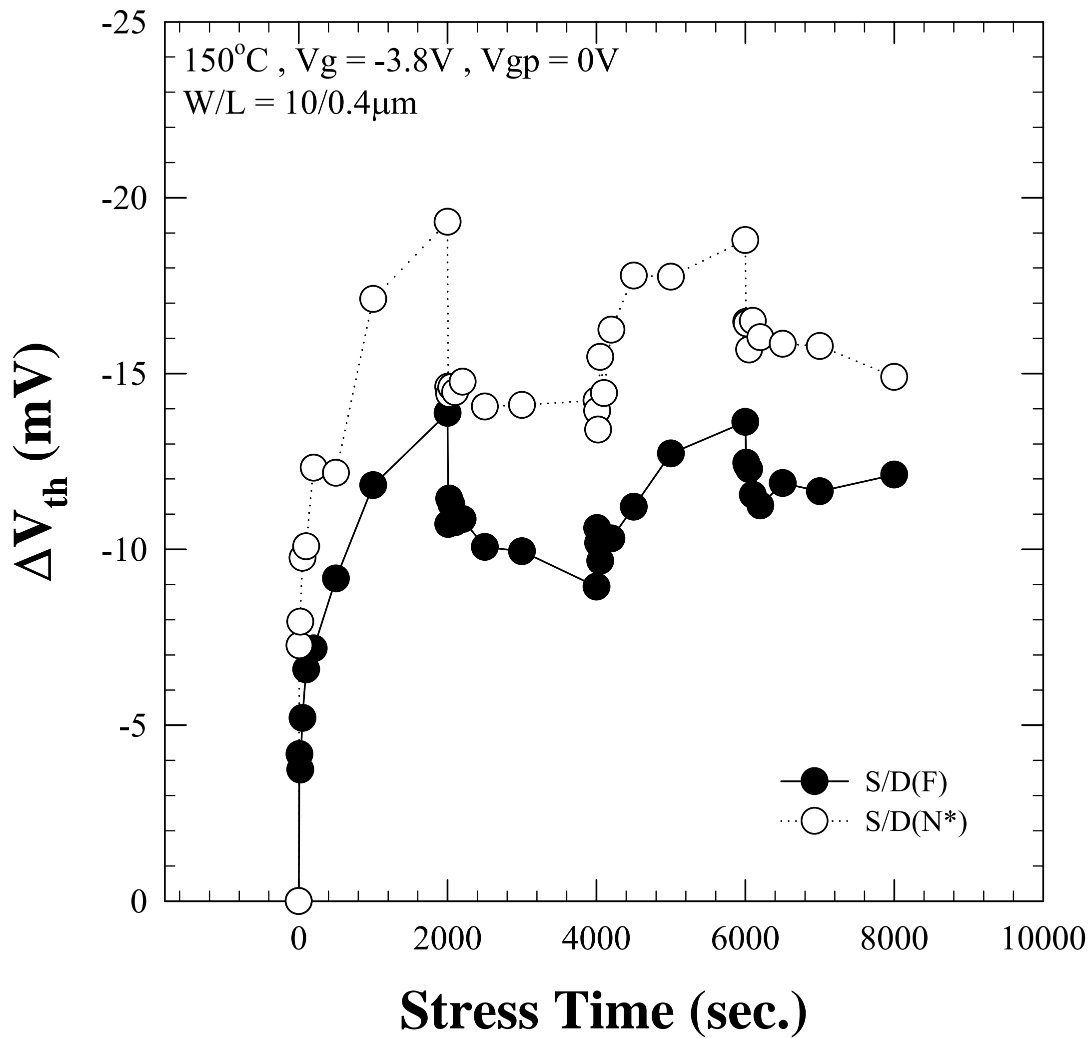


Fig. 5-5 ΔV_{th} versus stress time under stress-passivation-stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length

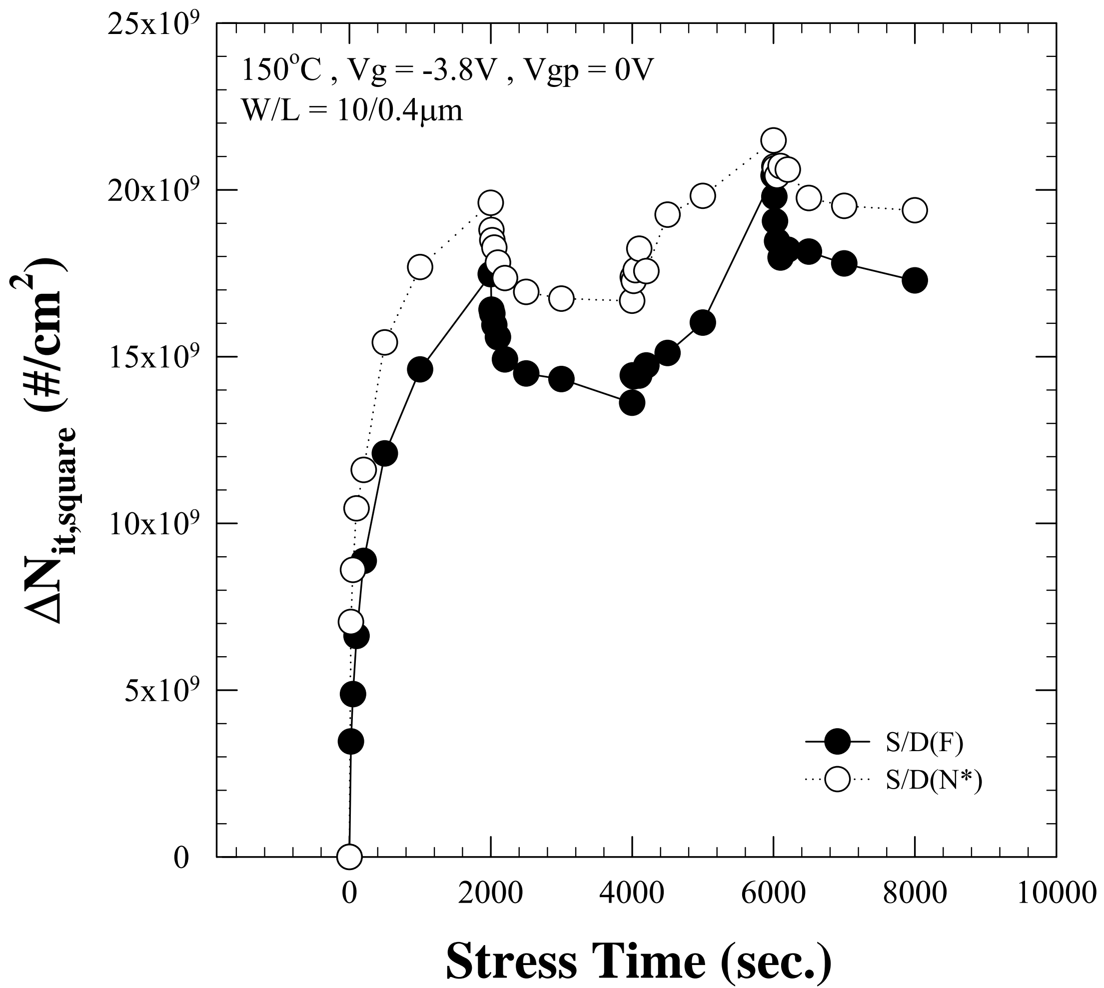


Fig. 5-6 Interface state versus stress time under stress-passivation-stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length(square wave)

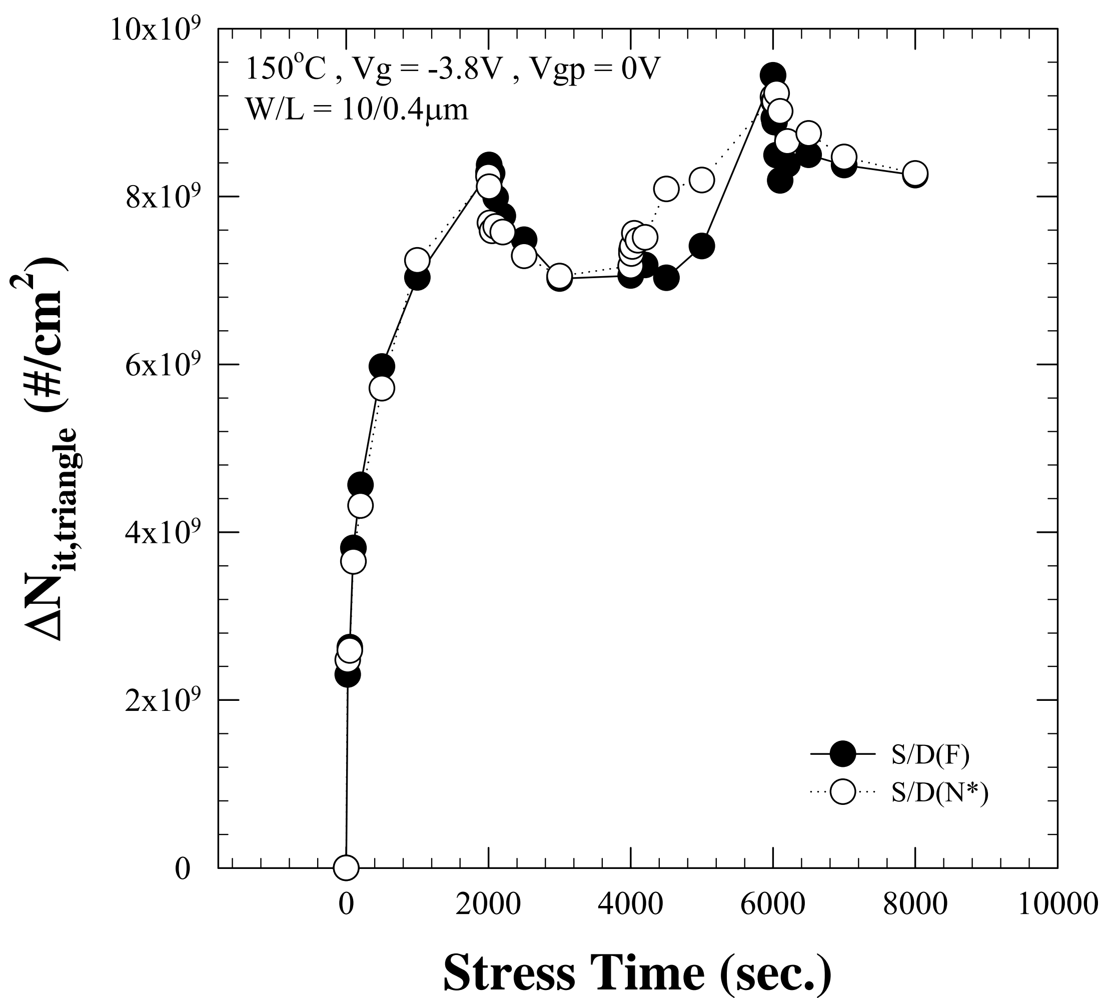


Fig. 5-7 Interface state versus stress time under stress-passivation-stress for pMOSFETs with different source/drain implantation for 0.4 μm channel length (triangle wave)

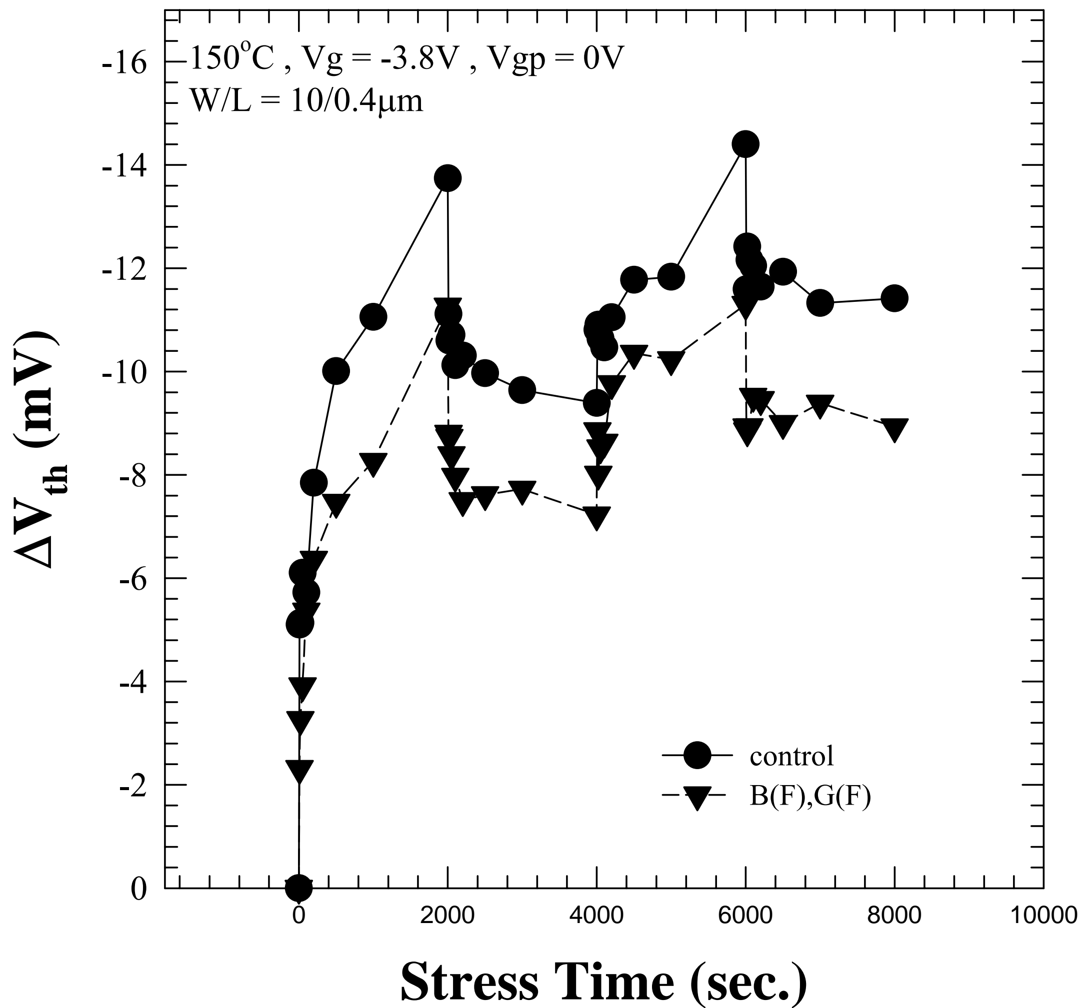


Fig. 5-8 ΔV_{th} versus stress time under stress-passivation-stress for pMOSFETs with control and source/drain implantation for 0.4 μm channel length

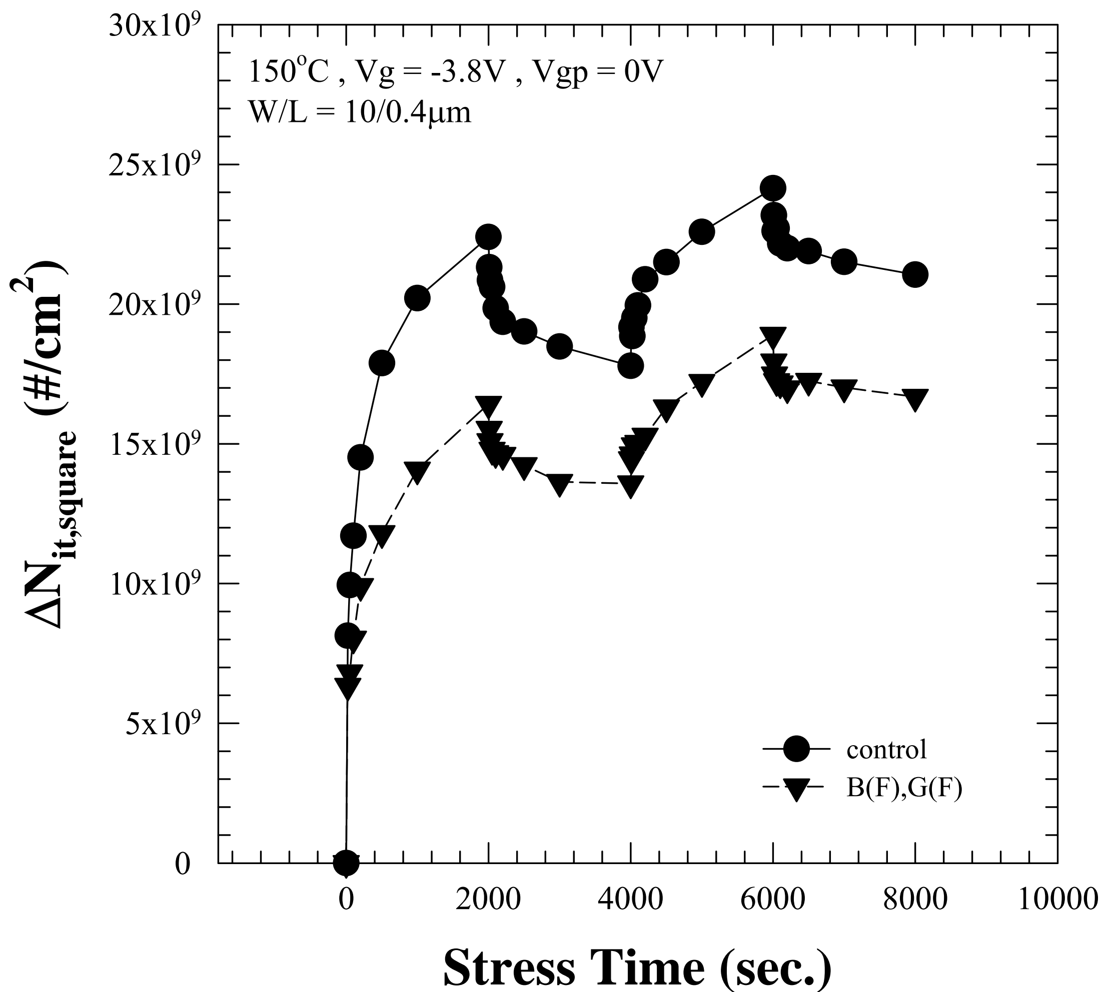


Fig. 5-9 Interface state versus stress time under stress-passivation-stress for pMOSFETs with control and source/drain implantation for 0.4 μm channel length(square wave)

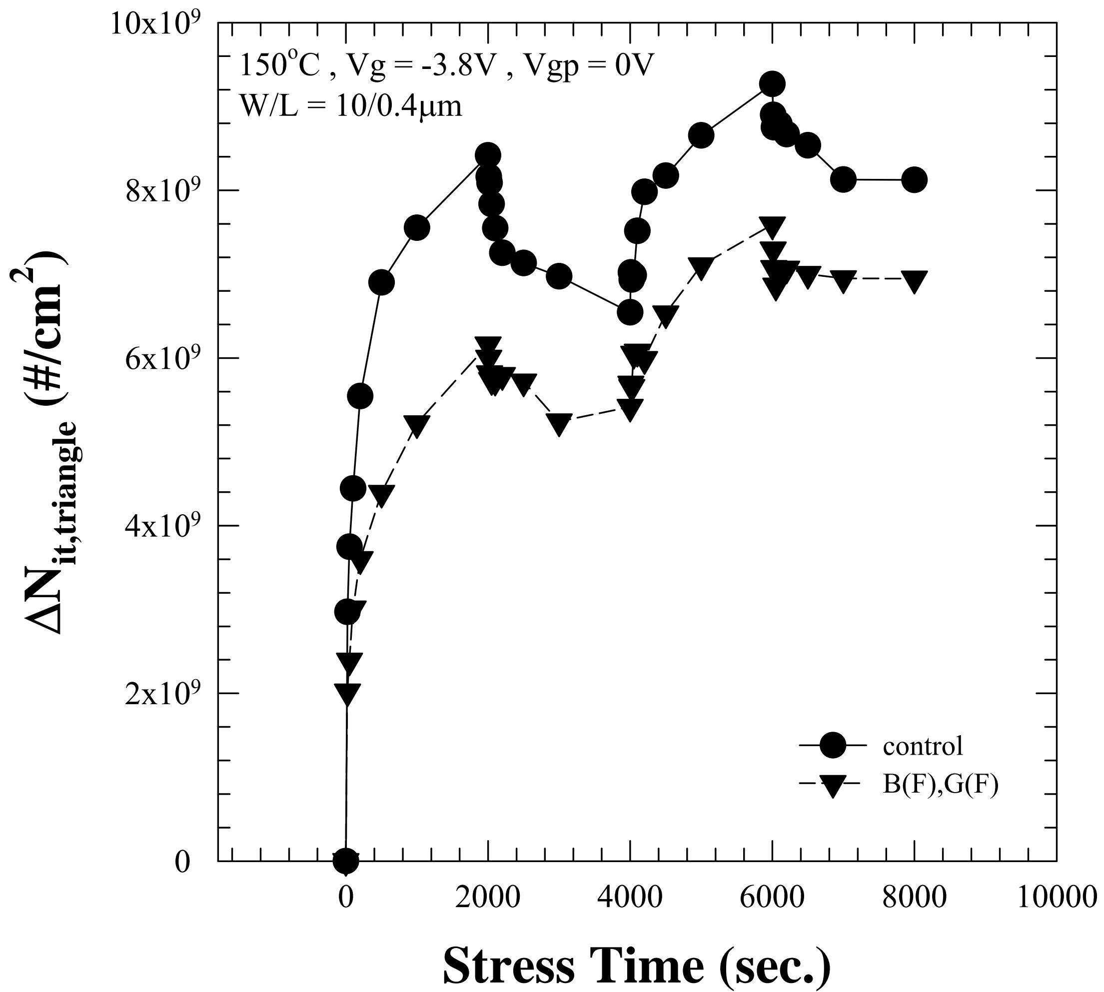


Fig. 5-10 Interface state versus stress time under stress-passivation-stress for pMOSFETs with control and source/drain implantation for 0.4 μm channel length (triangle wave)

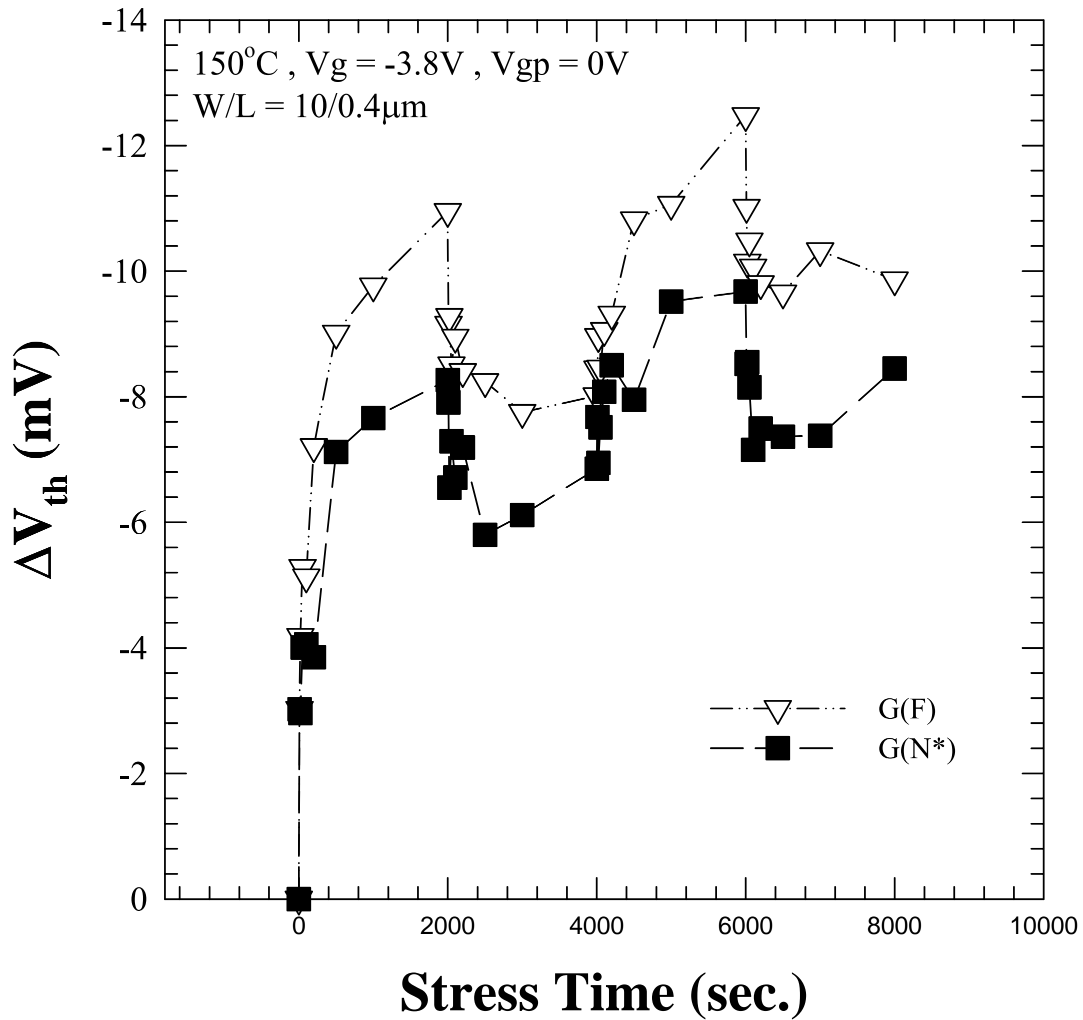


Fig. 5-11 ΔV_{th} versus stress time under stress-passivation-stress for pMOSFETs with different poly-silicon gate implantation for 0.4 μm channel length

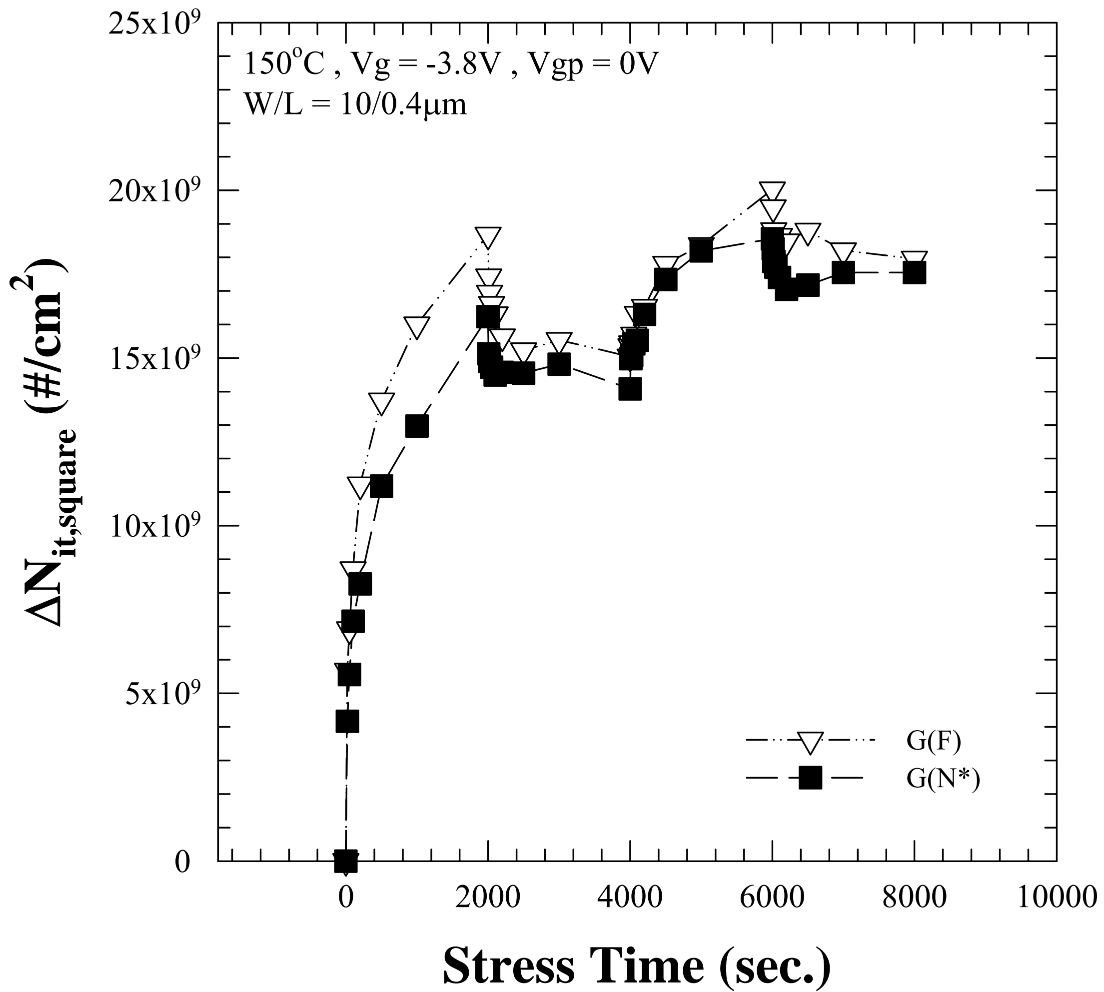


Fig. 5-12 Interface state versus stress time under stress-passivation-stress for pMOSFETs with different poly-silicon gate implantation for 0.4 μm channel length (square wave)