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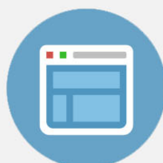

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# Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors

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In this work we report the observation and characterization of a hysteresis phenomenon in the transfer characteristics of *n*-channel polycrystalline silicon (poly-Si) thin-film transistors (TFTs). Such phenomenon is observed in devices with fully depleted channel and not treated with hydrogen-related anneal. The origin of the hysteresis is identified to be related to the electron trapping and detrapping processes associated with the deep-level traps in the grain boundaries of the poly-Si channel. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3086271]

## I. INTRODUCTION

Thin-film transistors (TFTs) built on an insulating substrate are fundamental building blocks for large-area electronics. During operation, a sheet of carriers induced in the thin film by the gate voltage transport along the channel. Amorphous silicon (*a*-Si) and polycrystalline silicon (poly-Si) are the two most commonly used channel materials for practical manufacturing. Owing to much better crystallinity in poly-Si than in *a*-Si, poly-Si TFTs typically exhibit higher carrier mobility and faster switching speed than the *a*-Si counterparts. However, the presence of grain boundaries (GBs) and a huge amount of defects contained may seriously affect the device characteristics.[1,2] For example, a significant portion of these defects acts as trapping center for carriers and thus degrades the device performance in terms of increased threshold voltage and decreased carrier mobility. To address the issue, hydrogenation treatment used for passivation of defects is usually employed.[1]

In this work we study a hysteresis phenomenon observed in the transfer characteristics of poly-Si TFTs. Occurrence of such phenomenon is closely related to a number of structural and process factors. Based on the measurement results obtained in this work, a model that considers the carrier trapping/detrapping processes at the GBs is proposed.

## II. TESTER STRUCTURE AND EXPERIMENT

Planer poly-Si TFT devices with poly-Si thickness ranging from 30 to 100 nm were fabricated and characterized. Those devices were built on 6 in. Si wafers capped with a 200-nm-thick thermal oxide. The Si channel is originally an amorphous layer deposited with a low-pressure chemical vapor deposition system. A thermal treatment performed at 600 °C in $N_2$ ambient for 24 h was employed to transform the layer into poly-Si. The grain size was found to be in the range from 20 to 40 nm through transmission electron microscopy inspection. After gate oxide and gate electrode ($n^+$ poly-Si) formation, source and drain doping was done with a self-aligned ion implantation step. After normal procedure to form the metal pads, a portion of the devices received a $NH_3$ plasma treatment or a forming gas anneal at 400 °C for 30 min. Device characteristics were characterized using an Agilent 4156 A parameter analyzer.

## III. EFFECTS OF POLY-SI THICKNESS AND PLASMA TREATMENTS

Figures 1(a)–1(c) show the transfer characteristics of poly-Si devices, in which the samples characterized are with poly-Si film thicknesses of 30, 50, and 100 nm, respectively, and receive no hydrogen-related treatment during and after device fabrication. In the measurements the gate voltage was swept forward from −3 to 6 V, and then backward from 6 to −3 V. Clearly in Figs. 1(a) and 1(b) the threshold voltage ($V_{th}$) of the backward sweeping (BS) curve shifts to a smaller value than that of the forward sweeping (FS), resulting in a hysteresis. Moreover, the BS curve shows improved subthreshold swing (SS) as compared with the FS curve. The reductions in both $V_{th}$ and SS strongly imply that a portion of the defects contained in the channel or at the channel/oxide interface becomes inactive in the BS measurements. Interestingly, as shown in Fig. 1(c), such phenomenon disappears as the poly-Si film thickness is increased to 100 nm, indicating that the film thickness plays an important role in the occurrence of the hysteresis.

Another factor that may eliminate the hysteresis is to perform a hydrogen-related treatment on the devices. An example is shown in Fig. 2, in which the transfer characteristics of a device treated with 2 h $NH_3$ plasma treatment are shown. The poly-Si film thickness is 50 nm in this case and the results are in strong contrast with that shown in Fig. 1(b). In addition to the plasma treatment, a forming gas anneal has the same effect (data not shown).

## IV. HYSTERESIS MECHANISM

Although the above results are interesting, we surveyed the literature but found no papers reporting similar phenom-

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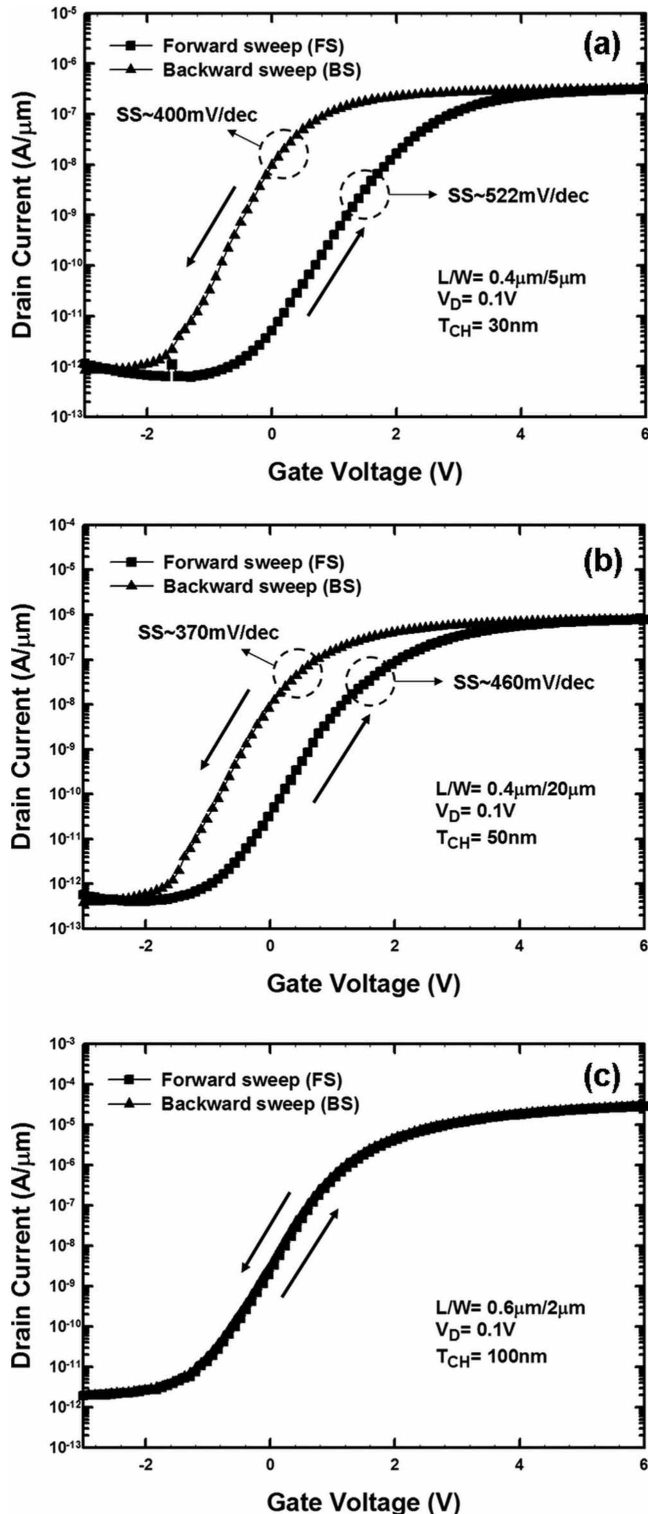


FIG. 1. Subthreshold characteristics of a poly-Si TFT with channel thickness of (a) 30, (b) 50, and (c) 100 nm.

enon in poly-Si TFTs. This is reasonable based on the above observations. First, most of the previous papers studied poly-Si TFTs with channel thickness around or thicker than 100 nm.[3] In some papers the channel thickness is indeed around or thinner than 50 nm, but the hysteresis phenomenon is still lacking.[4] This is attributed to the implementation of plasma treatments in order to obtain high-performance poly-Si TFTs, but the treatments also eliminate the hysteresis.

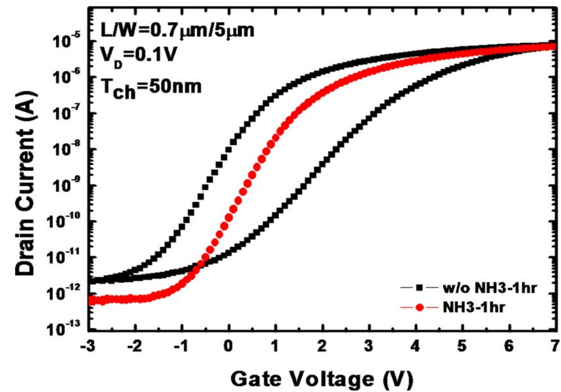


FIG. 2. (Color online) Subthreshold characteristics of a poly-Si TFT with channel thickness of 50 nm before and after plasma treatment in $NH_3$ for 1 h.

Actually, hysteresis phenomena have been observed and reported on several types of field-effect transistors other than poly-Si TFTs, such as silicon-on-insulator (SOI) devices[5,6] and metal-oxide-semiconductor transistors with high-$k$ gate dielectric.[7] In the former case it replies on impact ionization[5] to generate excess holes accumulating in the floating body of the SOI channel. This is obviously not the cases in Fig. 1, in which a small drain voltage of 0.1 V is applied. In this situation, the excess holes generated by impact ionization are not feasible. In the later one the mechanism for hysteresis has been identified to be due to electron trapping and detrapping events occurring in the high-$k$ gate dielectrics.[7] However electron trapping causes a positive shift in $V_{th}$ which is opposite to that shown in Fig. 1.

Here we propose a model based on the trapping/detrapping of electrons in the poly-Si channel to explain the occurrence of the hysteresis phenomenon. According to one of our previous publications,[8] the depletion width ($W_{dep}$) was estimated to be around 60 nm for poly-Si layers formed with a scheme identical to this work (e.g., solid phase crystallization at 600 °C in $N_2$ ambient for 24 h). Correlating this with results shown in Fig. 1, it is clear that $W_{dep}$ plays a key role in the occurrence of hysteresis.

The energy band diagrams perpendicular to the channel for fully depleted (FD) and partially depleted (PD) conditions at on-state modes under FS and BS are illustrated in Figs. 3 and 4, respectively. Figure 5 shows the energy band diagrams of the depletion region parallel to the channel. In the PD case, under the process of FS, the energy bands near the semiconductor surface (the depletion region) are bent downward [Fig. 3(a)]. In the neutral region ($x > W_{dep}$), there are many empty trap states at or near the GBs with levels distributed in the energy band gap. Nevertheless, in the depletion region ($x < W_{dep}$), most of the trap sites under the Fermi level are filled with the induced electrons. Subsequently, when the BS operation is executed and the bending of the energy band in the depletion region gradually recovers and shifts back to the flat-band condition. In the meantime, the trapped electrons tend to detrap from the trap sites. Three possible detrapping paths are identified in the figures. The first path [path 1 in Fig. 3(b)] pertains to the trapped electrons at the GBs being released from the trap site to the

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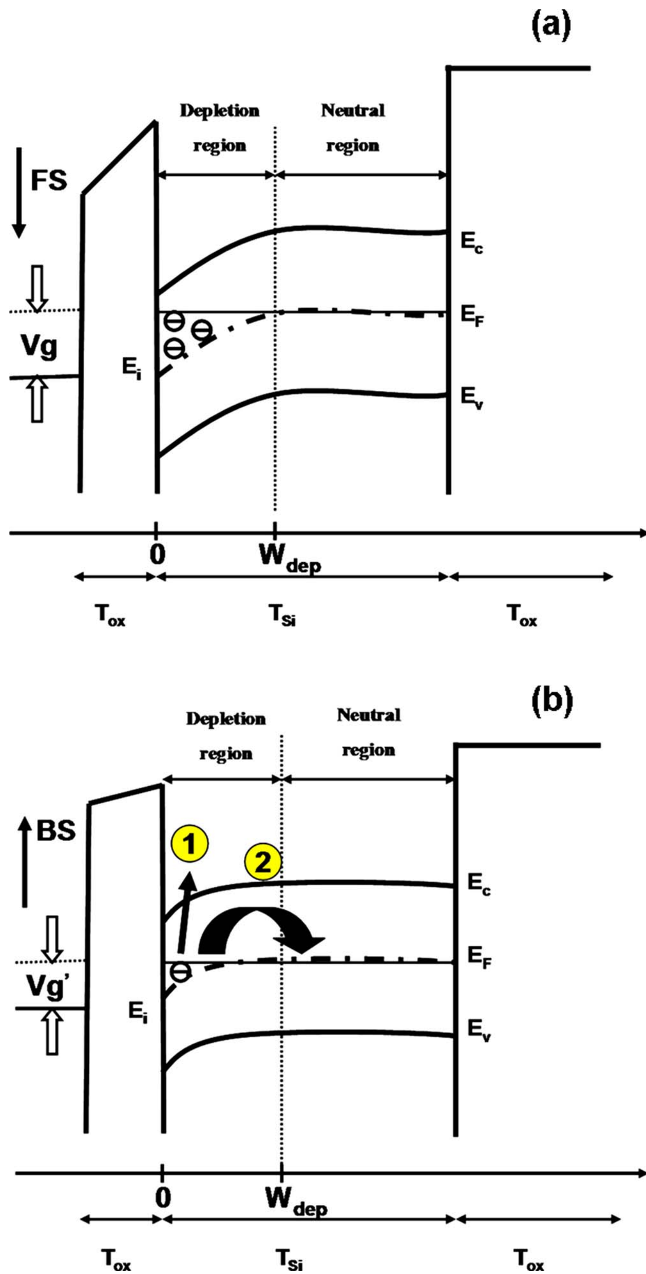


FIG. 3. (Color online) Band diagrams of poly-Si TFTs with a thick poly-Si channel. (a) The FS results in electron trapping in the depletion regions. (b) In the BS period the trapped electrons are released mainly through the empty traps located in the neutral region (path 2).

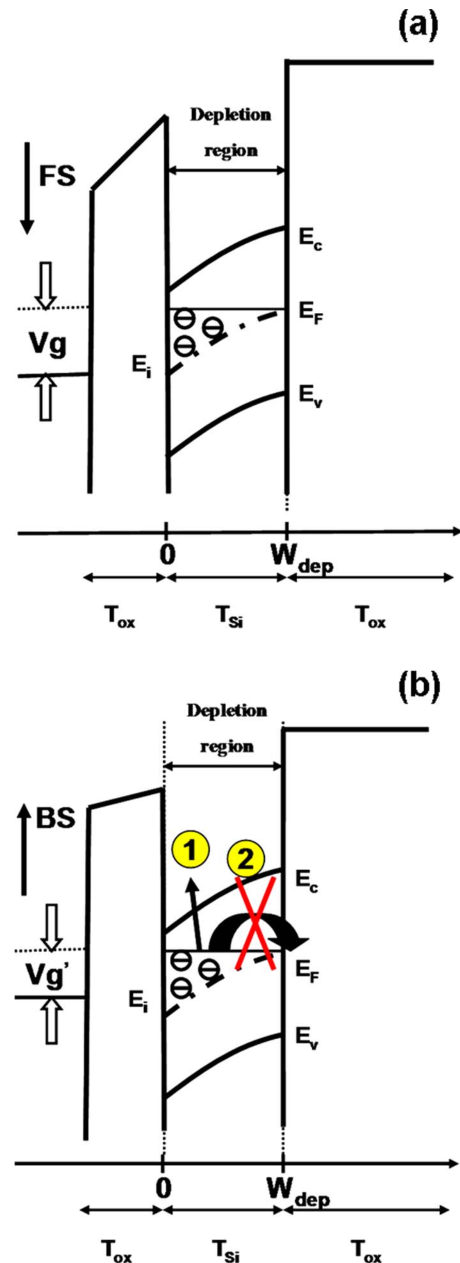


FIG. 4. (Color online) Band diagrams of poly-Si TFTs with a FD poly-Si channel. (a) The FS results in electron trapping in the depletion regions. (b) In the BS period, path 2 is blocked while path 1 is not efficient as the temperature is low. As a result the stored electrons remain in the channel until the gate voltage is sufficiently low to expel them.

conduction band by thermionic emission. The second path [path 2 in Fig. 3(b)] pertains to the trap-to-trap conduction via the traps located in the neutral region of GBs, with the electrons moving to the neutral region and recombining with holes there. The third path (denoted in Fig. 5 as path 3) pertains to the detrapping of electrons to the intragrain region. Considering the energy barrier for the paths, we find that the energy needed for Paths 1 and 3 is bigger than that for Path 2, thus Path 2 is more favorable. Path 2 is thus the major detrapping path in the devices with a thick poly-Si channel [e.g., Fig. 1(c)] and the transfer curve under BS operation can promptly follow the FS curve without depicting any hysteresis.

In the case of the FD mode ($T_{ch} < W_{dep}$), however, path 2 is hindered by the buried oxide as indicated in Fig. 4, so the available detrapping paths are paths 1 and 3, both requiring sufficient energy (or longer time to acquire the energy) to occur for electrons trapped in a deep level. Hysteresis phenomenon is thus resulted [Figs. 1(a) and 1(b)]. In other words, as the hysteresis occurs, an amount of electrons are stored in the deep-level states in the channel, resulting in a reduction in $V_{th}$ as well as the SS.

Based on the proposed model, the origin of the hysteresis is related to the electron trapping events occurring at the GBs. In other words, the difference in the FS and BS transfer characteristics originating from the mechanism. The amount of trapped electrons stored in the channel ($\Delta N_t$) can be estimated from either the difference in $V_{th}$ or SS using the following equations:[8]

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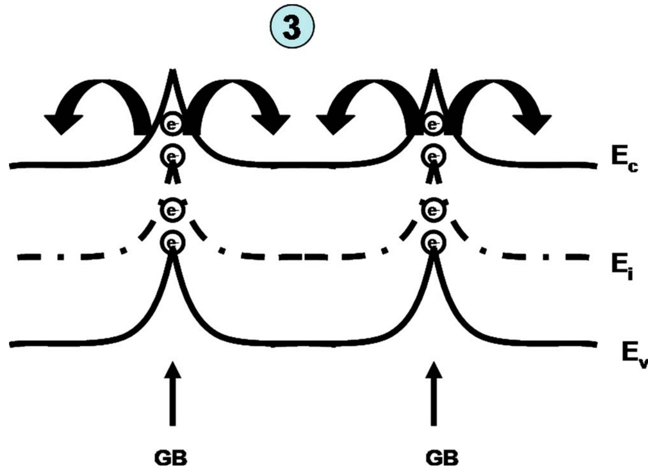


FIG. 5. (Color online) Band diagram in the depletion region parallel to the channel direction. Path 3 represents the release paths efficient only for electrons trapped in the tail states at the GBs.

$$V_{\text{th}}(\text{FS}) - V_{\text{th}}(\text{BS}) = \Delta V_{\text{th}} = \frac{q\Delta N_t}{C_{\text{ox}}}, \quad (1)$$

$$\text{SS}(\text{FS}) - \text{SS}(\text{BS}) = \Delta \text{SS} = \frac{kT}{q} \ln 10 \times \left(\frac{q\Delta N_t}{C_{\text{ox}}}\right), \quad (2)$$

in which $C_{\text{ox}}$ is the gate oxide capacitance per unit area. The results of calculation are summarized in Table I. It is seen that the estimated $\Delta N_t$ values are consistent in the two calculations. Moreover, it is well known that a hydrogenation step can effectively passivate the deep-level states. As a result, the amount of trapping/detrapping centers is dramatically reduced after the treatment, and the hysteresis becomes negligible (see Fig. 2).

The above model can well explain the effects of channel thickness and plasma treatment shown in Figs. 1 and 2. To further examine the accuracy of the proposed model, we investigate the impact of applied gate voltage. Figures 6 and 7 show the transfer characteristics of a poly-Si TFT with channel thickness of 50 nm with various $V_g$ sweeping range. In Fig. 6 the gate voltage is swept from −3 V to various highest voltages ($V_{gh}$) ranging from 3 to 8 V. It is seen that the FS curves basically follow the same trajectory, while BS curves show dependence on $V_{gh}$ applied in the previous FS measurement, and the hysteresis window (the shift in $V_{\text{th}}$) increases with increasing $V_{gh}$. This is reasonable considering the band diagram shown in Fig. 4(a). As the device is turned on, the largest band bending is determined by $V_{gh}$. As a result a

TABLE I. Trapped electron density in the channel estimated from the difference in $V_{\text{th}}$ and SS between the FS and BS transfer curves.

| Channel thickness | 30 nm [Fig. 1(a)] | 50 nm [Fig. 2(b)] |
|---|---|---|
| SS (FS) (mV/dec) | 522 | 460 |
| SS (BS) (mV/dec) | 400 | 370 |
| $V_{\text{th}}$ (FS) (V) | 2.02 | 1.83 |
| $V_{\text{th}}$ (BS) (V) | 0.02 | 0.29 |
| $\triangle Nt$ (cm$^{-2}$) [Eq. (1)] | $2.15 \times 10^{12}$ | $1.66 \times 10^{12}$ |
| $\triangle Nt$ (cm$^{-2}$) [Eq. (2)] | $2.19 \times 10^{12}$ | $1.61 \times 10^{12}$ |

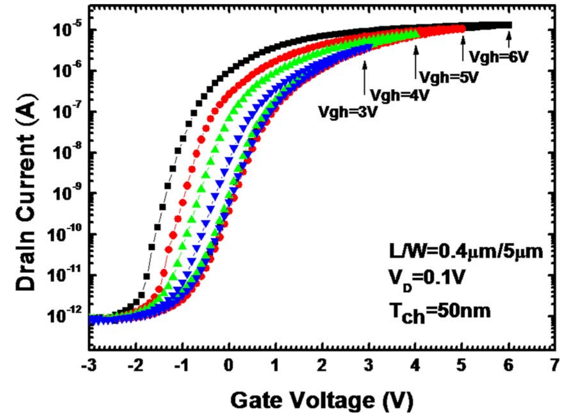


FIG. 6. (Color online) Transfer curves measured by applying gate voltages from −3 V to various maximum voltages ($V_{gh}$) ranging from 3 to 6 V. The BS curve depends on the maximum voltage applied in the FS curve.

larger amount of trapped electrons is stored in the channel as the $V_{gh}$ is increased and thus leads to a larger hysteresis window. As the gate voltage is swept back to −3 V, the potential level at channel/gate oxide interface is raised to a level sufficiently high to release all the stored electrons in the channel. Therefore the $I$-$V$ curve executed in the next FS measurement coincides with the previous FS curve.

The measurements conducted in Fig. 7 are with gate voltage swept from various lowest voltages ($V_{gl}$) ranging from −6 to −1 V and end at 8 V. Under the situation, the results indicate the FS curves depend on $V_{gl}$ applied in the BS curve, while the difference among the BS curves is obviously much smaller. As mentioned above, the $V_{gl}$ is a key factor that determines the detrapping process of trapped electrons. As $V_{gl}$ is not sufficiently low, an amount of trapped electrons will remain in the channel and result in a lowering in $V_{\text{th}}$ of the following FS $I$-$V$ curve.

## V. EFFECTS OF TEMPERATURE

Figure 8 depicts the transfer characteristics of a device measured at temperatures of 25, 50, 75, and 100 °C, respec-

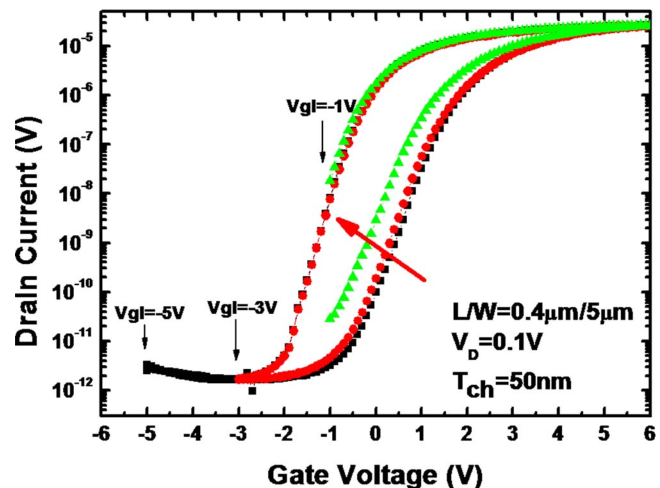


FIG. 7. (Color online) Transfer curves measured by applying gate voltages with various minimum voltages ($V_{gl}$) ranging from −5 to −1 V and maximum voltage of 6 V. The FS curve depends on the minimum voltage applied in the FS curve.

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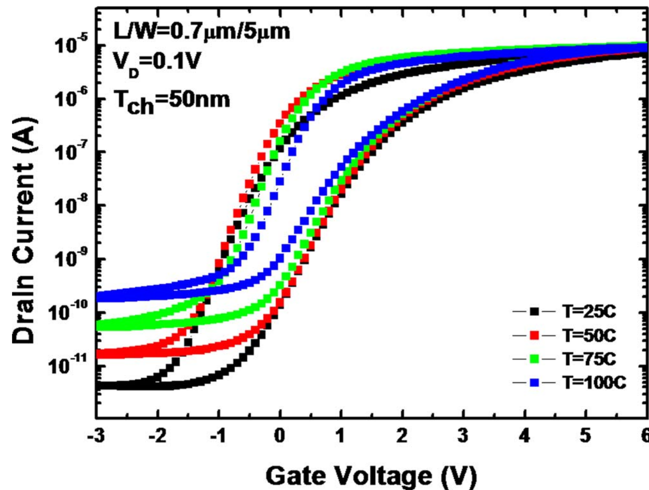


FIG. 8. (Color online) Transfer curves measured at various temperatures.

tively. As the gate voltage is smaller than −2 V, it is seen that FS curve coincides with the RS one while the current increases with increasing temperature. In this regime the extracted activation energy, as shown in Fig. 9, is around 0.5 eV, which is close to one-half of the bandgap of Si, indicating that thermionic emission is the major conduction mechanism.[9] On the other hand, the subthreshold current measured under FS mode increases with increasing temperature as expected. However, the situation becomes complicated in the RS measurements and the current may decrease with increasing temperature in the gate voltage region ranging from −1 to 0.5 V. As a result, the hysteresis window shrinks as the temperature increases. This is attributed to the enhanced thermal detrapping probability as the temperature increases, as shown in Fig. 5, and thus more trapped electrons resulted in the FS measurement are released. This mechanism is also responsible for the negative activation energy shown in Fig. 9.

The field-effect conduction (FEC) method[10–12] was employed to extract the density-of-state (DOS) of the FS and

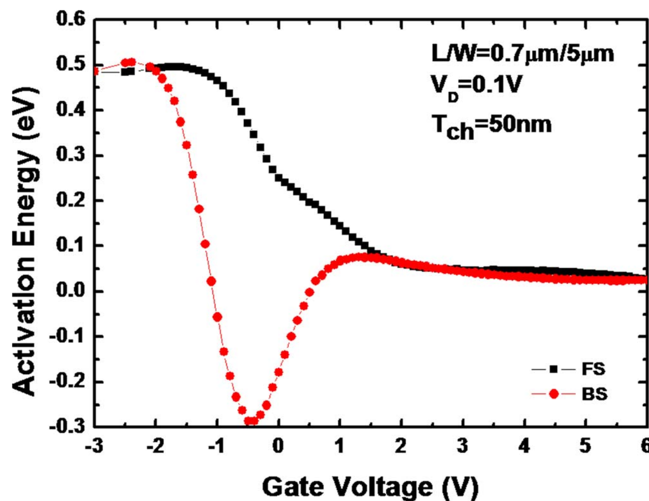


FIG. 9. (Color online) Activation energy extracted from the results shown in Fig. 8.

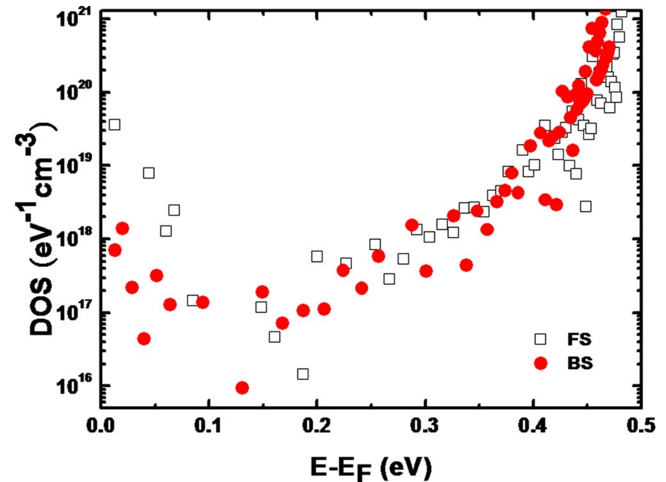


FIG. 10. (Color online) DOS extracted using the FEC method. Major difference exists in the midgap region.

BS curves and the results are shown in Fig. 10. In this method, based on the transfer characteristics measured at different temperatures under FS mode, as shown in Fig. 8, the flat-band voltage could be determined.[13] Once the flat-band voltage is determined, the DOS could be extracted as a function of energy level inside the gap using the FEC approach. As can be seen in the figure, the major difference between the FS and BS comes from the midgap (deep-level) regime, supporting the inference given in the proposed model.

## VI. CONCLUSIONS

The origin of the hysteresis characteristics observed in *n*-channel poly-Si TFTs is thoroughly studied in this work. The occurrence of the hysteresis is found to be related to a number of factors, including channel film thickness, hydrogenation treatment, range of sweeping gate voltage, and temperature. A model considering the electron trapping and detrapping processes in the channel region is proposed to explain our findings. The model indicates that detrapping of electrons stored in the deep-level traps located in the GBs will be hindered as the channel thickness becomes FD and lead to the occurrence of the hysteresis. However, the hysteresis becomes negligible as the amount of deep-level traps is significantly reduced with hydrogen passivation treatment.

## ACKNOWLEDGMENTS

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