Chapter 3

Experiments

In this chapter, we presented the fabrication processes of planar ion-implanted VCSELs. It main goal is establishing electrical contacts to anode and cathode of a laser diode and defining the transverse region of current aperture or optical cavity. Our 850 nm GaAs/AlGaAs VCSEL device was grown by MOCVD on the Si-doped GaAs substrate. It contains 20.5 pairs of alternating p-doped (C) $Al_{0.12}Ga_{0.88}As/AlAs$ stacks with quarter-wavelength-thick layer as the top DBR, three GaAs quantum wells as the active region and a 30.5 pairs of alternating n-doped (Si) $Al_{0.12}Ga_{0.88}As/AlAs$ stacks with quarter-wavelength-thick layer as the bottom DBR. The composition grading of the DBRs and the spacer was also implemented. The detailed specification of VCSEL structure is listed in Table 2.2 in chapter 2.

3.1 Fabrication Procedures

The fabrication process was performed with four photolithographic procedures. First, we deposited SiO_2 on the wafer for device passivation using plasma enhanced chemical vapor deposition (PECVD). Then, a lithographic process was performed to define the pattern and the SiO_2 was etched by reactive ion etching (RIE). Second, we defined the pattern of the top p-metal contact, evaporating Ti/Pt/Au on the wafer surface, and then lifting off the unwanted metal.

After evaporating p-metal, the n-metal evaporation on the back side of the wafer was followed by the general lapping and polishing procedures. The third lithographic process was performed to define the un-implanted region ready for ion implantation to form the transverse extent of the optical cavity. It is advantage to deposit the top contact prior to the ion

implantation to avoid surface damage, such as unintentional removal of a GaAs cap layer protecting underlying AlGaAs DBR layers, which may degrade the ohmic contact.

The final step was performed to evaporate the bonding pad metal. Bonding pad and p-contact metals are both on the same side of the wafer. They must be connected to each other, so it seems that they could be formed at the same time. However, if we fabricate the p-contact and bonding pad at the same time, the contact metal would be too thick for implantation ions to penetrate through. To avoid this condition, we should form the p-contact and bonding pad separately. A sketch of the whole process is shown in Figure 3.1. The top view sketch of the device is shown in Figure 3.2. More detailed process parameters and steps are listed as follow:

1. Figure 3.1(a)

Wafer Clean : Immersing in ACE, IPA, B.O.E 5'; dipping in D.I water ; blowing with N_2.

SiO_2 Deposition : PECVD 3000 Å .

Lithography : Baking 120℃ 5'
PR 500 rpm 5", 4000 rpm 2"
Baking 120 ℃ 2'
Exposure 32"
Develop 62"
Baking 120 ℃ 10'

SiO_2 Etching : RIE 250"

Remove PR : Immersing in ACE 10', IPA 2' ; dipping in D.I water ; blowing with N_2.

2. Figure 3.1(b)

Lithography : Baking 120℃ 5'
PR 500 rpm 5", 3500 rpm 30"

Baking 120 ℃ 5'
Exposure 41"
Develop 1'20"
Baking 120 ℃ 10'

Evaporation : P-contact ~ Ti(300 Å)/Pt(600 Å)/Au(3000 Å).

Lift off : Immersing in ACE 10', IPA 5' ; dipping in D.I water ; blowing with N_2.

Alloying : Furnace 420 ℃ 5'

PR Protection : PR 1000 rpm 3" , 4000 rpm 50"
Baking 120 ℃ 10'

Lapping / Polishing

Remove PR : Immersing in ACE 10', IPA 2' ; dipping in D.I water ; blowing with N_2.

PR Protection : PR 1000 rpm 3" , 4000 rpm 35"
Baking 120 ℃ 10'

Clean : NH_3/H_2O_2/D.I water 1' ; dipping in D.I water ; blowing with N_2.

Evaporation : N-contact ~ AuGe(700 Å)/Ni(200 Å)/Au(3500 Å).

Remove PR : Immersing in ACE 10', IPA 2' ; dipping in D.I water ; blowing with N_2.

Alloying : Furnace 420 ℃ 5'

3. Figure 3.1(c)

Lithography : Baking 120℃ 5'
PR 1000 rpm 3", 4000 rpm 45"
Baking 120 ℃ 5'
Exposure 30"
Develop 4'30"
Baking 120 ℃ 10'

Ion implantation : H^{+}, $5\times10^{14}cm^{-2}$, 300 keV

Remove PR : Immersing in ACE 10' , IPA 2' , H_2SO_4 3' (40 ℃).

Annealing : Furnace 420 ℃ 10'

4. Figure 3.1(d)

Lithography : Baking 120℃ 5'
PR 500 rpm 5", 3500 rpm 45"
Baking 120 ℃ 2'
Exposure 35"
Develop 1'40"
Baking 120 ℃ 10'

Clean : CH_3COOH / NH_4F/H_2O 1' ; dipping in D.I water ; blowing with N_2.

Evaporation : Bonding pad ~ Ti(5000 Å)/Au(10000 Å).

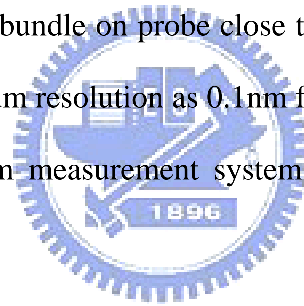
Lift off : Immersing in ACE 10', IPA 5' ; dipping in D.I water ; blowing with N_2.

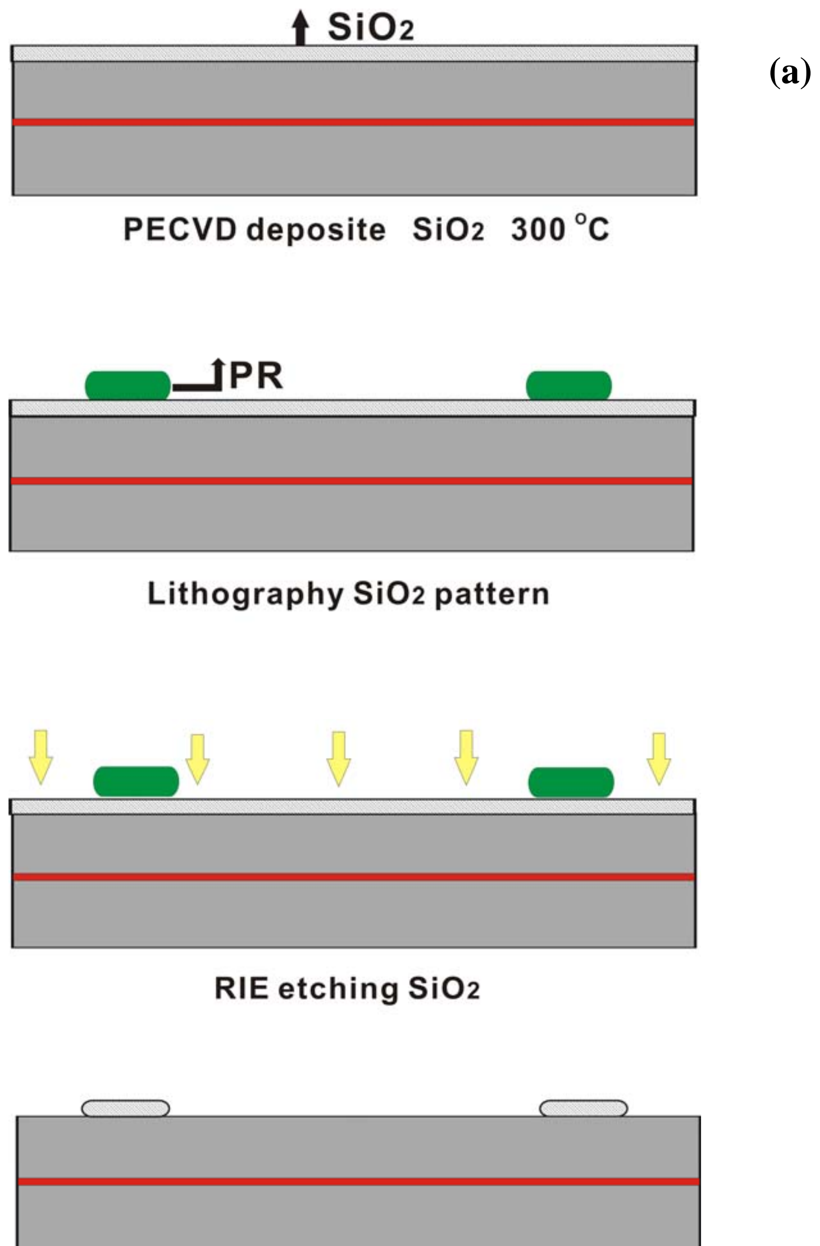
Alloying : Furnace 420 ℃ 5'

3.2 Measurement Setup

One of the advantages for VCSELs is that they are compatible with wafer-level test, and we can utilize a probe station system for basic characteristics measurement such as L-I-V characteristics. Scheme of probe station system, illustrated in Figure 3.3, contained probe station, current source, and power-meter module. Keithley 238 as current source supplies DC current for diode laser and receives relative voltage synchronously. Laser output power is measured by power-meter module (Newport, Model 1835C). For accuracy power measurement, an integration sphere was used to pick up whole light output from VCSELs. With these data information, we could acquire the L-I-V curves from the computer.

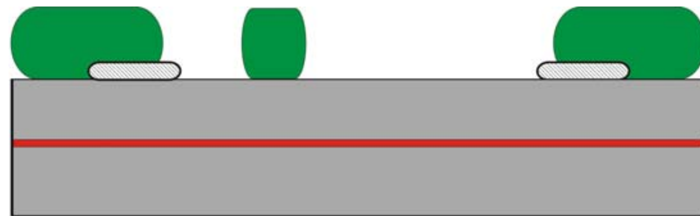
In addition, emission spectrum was measured by an optical spectrum analyzer (OSA). We served a multi-mode fiber bundle on probe close to emission aperture in focus for taking spectra. OSA had small spectrum resolution as 0.1nm for accurately measuring VCSEL lasing spectrum. Scheme of spectrum measurement system was combined with probe station as Figure 3.3.



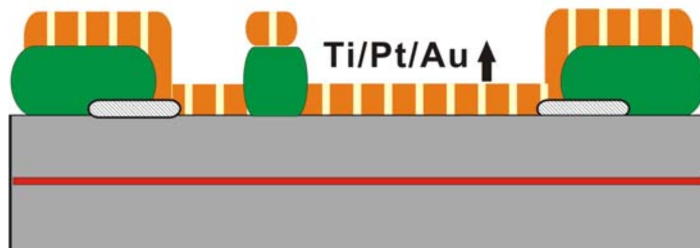


(a)

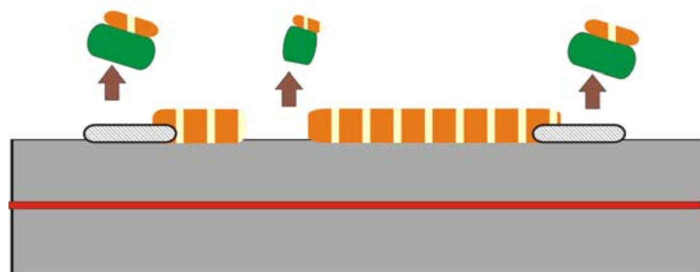
(b)



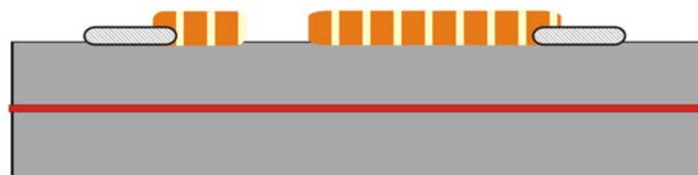
Lithography p-metal pattern

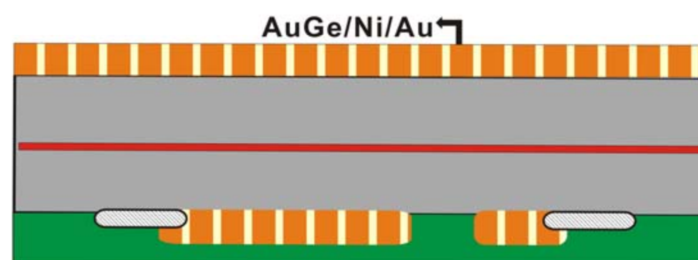


E-gun:p-metal evaporation



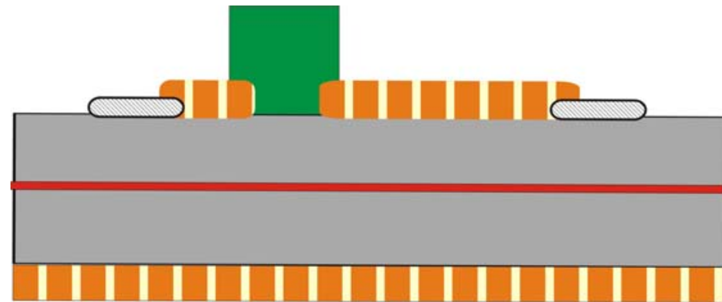
Unwanted metal lift off



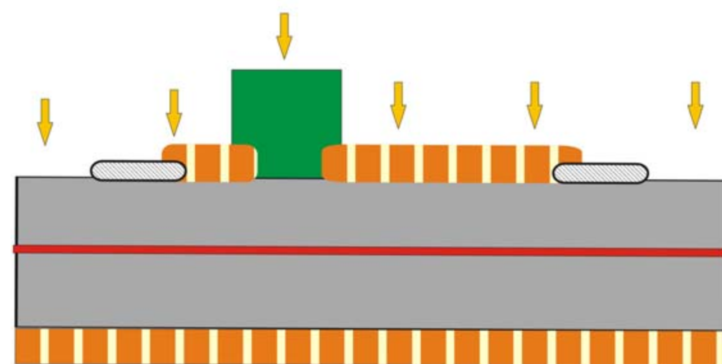


n-metal evaporation

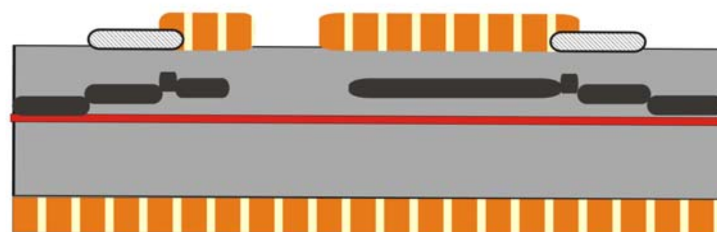
(c)



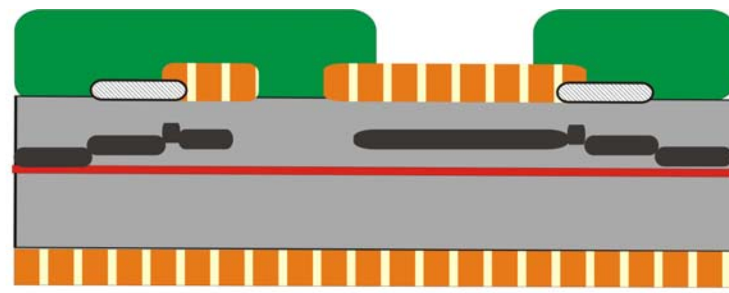
Lithography pattern Ion implanted PR mask

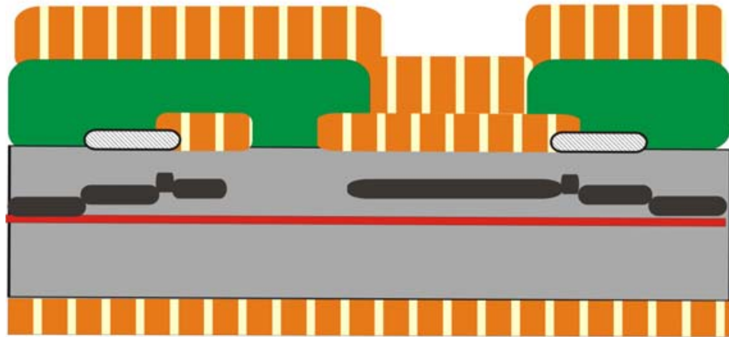


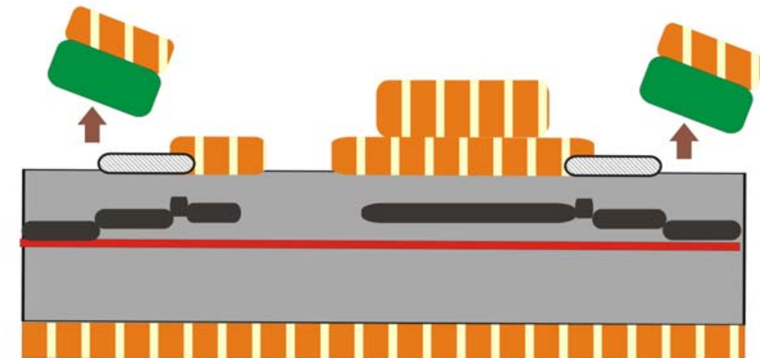
Ion implantation: H^{+} $5*10^{14}$ cm^{-2} 300keV



(d)







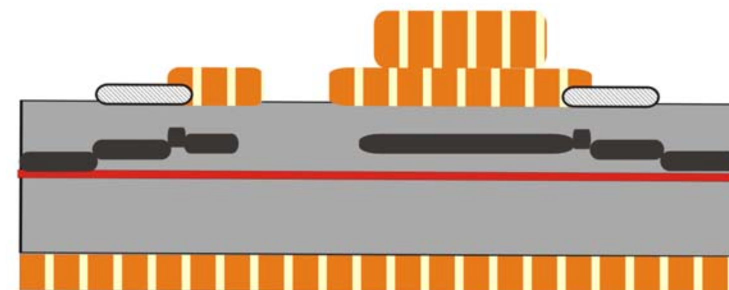


Figure 3.1 The process procedures of the device with (a) SiO_2 deposition, (b) top and bottom metal evaporation, (c) ion implantation, and (d) bonding pad metal evaporation.

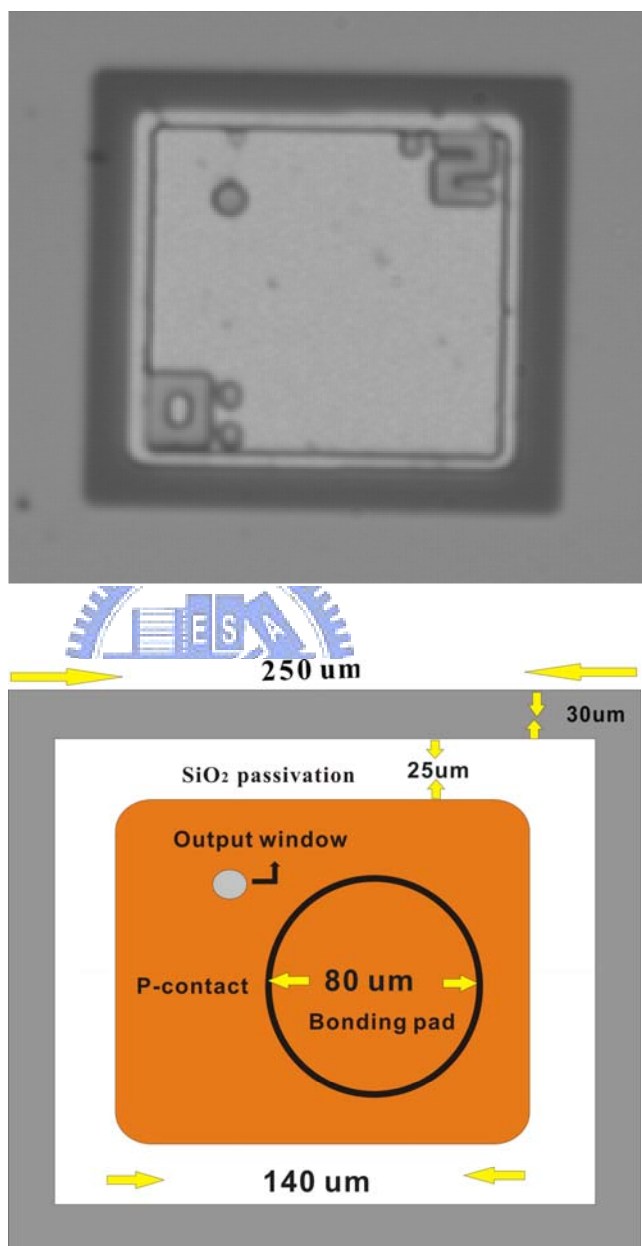


Figure 3.2 Top view sketch of the device.

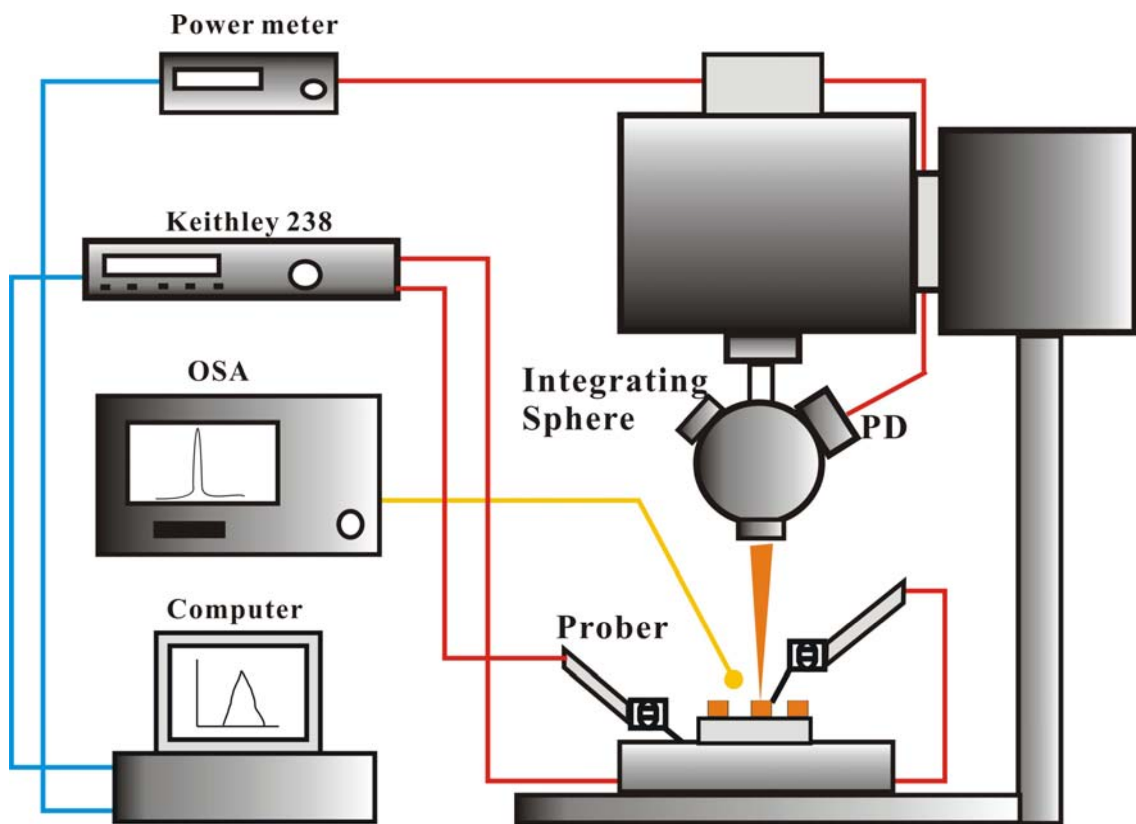


Figure 3.3 Probe station measurement setup.