

國立交通大學
電子物理研究所碩士班
碩士論文

一種具有奈米線通道的新穎多晶矽薄膜電晶體
製作與特性之研究

Fabrication and Characterization of a Novel
Polycrystalline Silicon Thin Film Transistor with
Nanowire Channels



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中華民國九十四年六月

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摘 要

在本篇論文中，我們製作了一種具有奈米線通道的新穎多晶矽薄膜電晶體，並測量了它的特性。一般來說，製作奈米線結構需要昂貴的設備或運用複雜的過程。我們提出一種簡單快速製備奈米線之方法。利用一般製作氧化層邊襯 (oxide spacer) 之方法概念，以底閘極薄膜電晶體結構來形成多晶矽邊襯奈米線通道 (poly-Si sidewall spacer nano-wire channel)。可藉由調整閘極高度、非晶矽沉積厚度和蝕刻時間，來控制此邊襯之直徑至 30nm 以下。此製作程序與傳統製程設備相容，且不需要其它困難的技術。元件完成總共只需要四道光罩，是低成本的製程。

在研究中，我們測量了不同條件的奈米線通道之元件特性。為了更進一步改善元件特性，我們對元件分別做了 N_2/H_2 退火及 NH_3 電漿處理。我們發現 NH_3 電漿處理比 N_2/H_2 退火能更有效改善元件特性，例如：鈍化缺陷、降低漏電流、提升載子遷移率、增強開啟電流等。 NH_3 電漿處理對於

元件輸出特性也有所改善，在高汲極偏壓下能有效抑制 kink effect。在文中，我們也分析並討論了有關漏電流的造成因素，並提出了兩個造成漏電流的機制和其他影響漏電流的可能原因。

在未來，為了改善原件特性，有效減少多晶矽薄膜的缺陷是很重要的。而使用金屬誘發側向結晶法和準分子雷射結晶法，可以達到增大多晶矽結晶的目的，相信可以大大提升元件特性。只要元件特性夠好，此元件技術可以應用在各種先進應用方面。



Fabrication and Characterization of a Novel Polycrystalline Silicon Thin Film Transistor with Nanowire Channels

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Abstract

In this thesis, we fabricated a novel poly-Si TFT with nanowire channels and measured its characteristics. Generally, the traditional method is expensive and complicated to obtain the nano-wire structure. We proposed a simple and fast approach to manufacture the nano-wire. Using the method of forming oxide spacer, we form the poly-Si sidewall spacer nano-wire channels for the bottom-gate TFT. Thus, we can control the sidewall spacer nano-wire thickness under 30 nm by controlling the gate height, α -Si layer thickness, and etching time. The process is compatible to conventional process equipment, and doesn't need any difficult technique. The total mask number to complete the device is only four, so it is a low-cost process.

In this study, we characterized the performance of poly-Si NW TFTs for various nano-wire conditions. In order to improve the device performance, we executed the N_2/H_2 gas annealing and NH_3 plasma treatment. However, the NH_3 plasma treatment can improve the device performance more effectively than N_2/H_2 gas annealing, such as passivate the defects, reduce leakage current, enhance carrier mobility, increase on-current, and decrease

subthreshold slope. The NH₃ plasma treatment also can improve the device output property, and suppress the kink effect at high drain bias effectively. We also analyzed and discussed the origins of the off-state current, and proposed two mechanisms to explain the origins of leakage current and the other probable reasons for our device.

In the future, to further improve the device performance, it is important to reduce the defects and trap-states in poly-Si film for the poly-Si NW TFT. This could be achieved by using the metal induce lateral crystallization (MILC) or excimer laser crystallization (ELC) to enlarge the grain size of the poly-Si films. We believe that can greatly improve the device performance. As long as the performance reaches good enough, it can be applied to a variety of novel applications in the future.



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Chapter 1

Introduction

1-1 Background and motivation

1-1-1 Overview of polycrystalline silicon thin film transistors

Thin film transistors (TFTs), which employ a thin semiconductor film on an insulating substrate as the active device channel, was first demonstrated in 1961 by Dr. P. K. Wenimer in RCA. With its simplicity in structure and fabrication, the applications of thin film transistors in image sensors and displays become more and more popular. Polycrystalline silicon deposited by low-pressure chemical vapor deposition (LPCVD) technique is widely used in modern very large scale integrated (VLSI) circuit [1-3]. The first polycrystalline silicon thin film transistors (poly-Si TFTs) were fabricated by Fa et al [4] in 1966. Since then, electrical properties, conduction mechanism and fabrication process of polysilicon films were widely and extensively studied [5][6].

Active matrix-addressed flat-panel liquid crystal displays (AMLCDs) are one of the most promising candidates for realizing high-quality large-area flat-panel displays [7]. The traditional AMLCDs were fabricated using α -Si:H TFTs for the pixel switching device. Amorphous silicon thin film transistors, among many types of active elements, have been intensively studied because of their many advantages, particularly their compatibility with large glass substrate with low processing temperature [8]. However, the low electron field-effect mobility attainable ($< 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) with these devices limits their applications for the switching elements. To integrate the switching elements with the driver circuits together

on the same substrate is very desirable not only to reduce the cost but also to improve the circuit and system reliability. Recently, poly-Si has been proposed as a very attractive alternative material for the active element of LCDs. During the past decade there has been a rapid growth of interest in polycrystalline silicon (poly-Si) for the active device layer in thin film transistors (TFTs) for AMLCDs [9][10][11]. This is due to the much higher mobility and the drive current of poly-Si TFTs, compared to amorphous silicon counterparts, which enables the integration of peripheral circuit on the same panel in active matrix liquid crystal displays [1]. The superior field effect mobility ($>100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) achieved with poly-Si thin film transistors seems to be essential for the successful integration of row and column drive circuits on the active plate.

The performance of poly-Si TFTs is strongly influenced by grain boundaries and intragranular defects [12]. In order to enhance TFTs characteristics, several techniques used to increase the grain size of poly-Si films have been proposed and developed [13][14][15], such as direct deposition of poly-Si at a reduced pressure (e.g., $<10 \text{ mTorr}$), as well as conversion from an amorphous precursor state. The latter approaches include:

1. Solid-Phase Crystallization (SPC):

Although solid-phase crystallization of the amorphous silicon films had been studied by Koster in 1978 in the context of solar cell work, the interest in the technique for TFT work was stimulated by the work of other people. This method is the crystallization of amorphous silicon (α -Si) films deposited by low-pressure chemical vapor deposition (LPCVD) [16]. For α -Si films deposited at temperature below 600°C , thermal crystallization for 20 hours at 600°C was required to convert them into their final polycrystalline form. The grain size obtained by solid-phase crystallization (SPC) of α -Si films is larger by several times and has smoother surface morphology than that of as-deposited poly-Si films. Grain size dimensions in excess of $1 \mu\text{m}$ have been obtained by this technique.

2. Metal-Induced Lateral Crystallization (MILC):

MILC employs metal as precursor to lead amorphous Si to re-crystallize at lower temperatures because of lower energy barrier of re-crystallization resulting from the reaction between metal and Si [17].

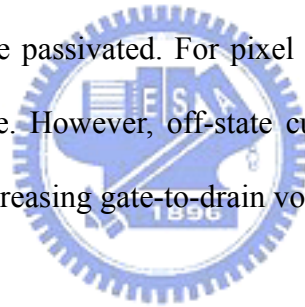
3. Excimer Laser Crystallization (ELC):

The conventional approach for producing low-defect-density polysilicon films is the solid-phase crystallization (SPC) of thin amorphous-silicon films on glass substrate by furnace annealing near 600°C. Pulsed UV-excimer laser annealing is also being investigated as an alternative crystallization technique to replace furnace annealing [18]. The standard gas mixtures and output wavelengths are ArF(193nm), KrF(248nm) and XeCl(308nm). For fabricating high performance poly-Si TFTs on a glass substrate, excimer laser crystallization method is very promising for the following reasons. First, it is a low-temperature process that introduces no serious thermal shrinkage of the glass substrate caused by the effects of the short pulse and large absorption coefficient of silicon in the UV light regime. Secondly, it can crystallize the film selectively by partially irradiating the film surface, so both poly-Si TFTs and amorphous Si TFTs can be formed on the same substrate. The laser process heats the thin silicon film to melting point on a short time scale (10ns~30ns) the allows the film to melt and recrystallize without significantly heating the glass substrate. Since this process achieves higher annealing temperature than a conventional furnace annealing, significantly higher quality polysilicon film can be obtained.

While there is a high-temperature technology based on the use of quartz substrate, people focus on the film processing at a sufficiently low temperature (< 630°C) to permit the use of inexpensive glass substrates.

The operation principles of poly-silicon TFTs are complicated compared to their

single-crystal counterparts because of the presence of grain boundaries in the channel. Polycrystalline silicon is rich in grain boundary defects as well as intragrain defects, and the electrical activity of these charge-trapping centers profoundly affects the thin film transistor characteristics. Due to the high density of defect states at grain boundaries and interior of grains, poly-Si TFTs exhibit poor performance such as low mobility, large subthreshold swing, large threshold voltage, and large leakage current, as compared to single-crystal counterparts. The electrical properties of polycrystalline semiconductor devices are strongly affected by the defects such as dangling bonds and strained bonds located at or near the grain boundaries [19][20]. To reduce the impact of the existing defects, a good way is to passivate them with hydrogen. This has actually become a key process in the fabrication of poly-Si TFTs. Hydrogen diffusion in this highly defected material was found to be significantly retarded by the presence of the states to be passivated. For pixel TFTs, it is essential to maintain a low leakage current in the off-state. However, off-state current in poly-Si devices have usually been found to increase with increasing gate-to-drain voltage difference.



1-1-2 Overview of nanowire

Minimization of silicon electronics is being actively pursued. One-dimensional structures, such as nanowires (NWs) have great potential for testing and understanding fundamental concepts about the roles of dimensionality and size in electrical properties, and could be the ideal building block for nanoelectronics, because they can function both as devices and as the interconnect wires that access them. Owing to the inherent high surface-to-volume ratio feature, NWs can suppress short-channel effects encountered in nano-scale MOSFETs [21] and provide high surface sensitivity for sensing devices. Many possible applications of Si NWs have been exploited, including nano CMOS , memory devices [22], NW TFTs [23], and

biosensors [24].

Preparation of Si NWs could be categorized into two types, namely, top-down and bottom-up, described as follows:

(I) Top-down

This approach uses advanced lithography techniques, such as deep UV, e-beam or nanoimprint, to generate the NW patterns, followed by an etching step to obtain the NW structures. These techniques are well developed and mature for mass-production purpose. Nevertheless, very expensive equipments and cutting-edge techniques are required. Conventional photolithography processes (e.g., G-line and I-line steppers), though relatively cheap for manufacturing, are not capable of patterning NWs directly. Some special skills such as thermal flow, chemical shrink, and spacer patterning have been proposed to help generate the nano-scale patterns using these conventional lithography tools.



(II) Bottom-up

This approach typically utilizes deposition methods to prepare the NWs, and synthesize the NWs on a substrate. Afterwards, these NWs were harvested and dispersed into a solution. Depositing the harvested NWs onto another oxidized substrate and making electrical contacts to the NWs, will complete the device structure. Many deposition methods have been developed nowadays which include laser ablation catalyst growth [25], chemical deposition catalyst growth [26] and oxide-assisted catalyst-free method [27]. The first two methods are carried out with metal nanocluster catalyst as the energetically favored sites for absorption of gas-phase reactants, and then the cluster supersaturates and grows a wire-like structure of the materials. The process is based on vapor-liquid-solid (VLS) mechanism. Nanometer-diameter catalyst clusters define the size of wires produced by VLS growth, in which bulk quantities of single crystalline NWs can be obtained. The approach can also be applied to prepare NWs of

other materials in addition to Si, such as III-V compounds and II-VI compounds. However, metal contamination is a potential concern in this approach. Oxide-assisted catalyst-free method is conducted without metal nanocluster catalyst, and thus is free from metal contamination. Nevertheless, there could be plenty of defects in the wires, and hence it is not applicable to electronic devices. In addition, these aforementioned methods usually suffer from the poor control of structural parameters such as NW's diameter, length, and orientation.

Methods used to assemble and align the NWs prepared by “bottom-up” approach include electric-field-directed assembly [28], microfluidic channel [29] and Langmuir-Blodgett (LB) technique. Electric field method is via interaction between electric field of two parallel electrodes and polarity of NWs, and therefore directs the wires. Although electric fields enable more control over assembly, this method is limited by electrostatic interference between nearby electrodes as separations below micrometer level and requirement of extensive lithography to fabricate the electrodes. Fluidic channel method is to align wires by flowing NWs suspension inside a poly(dimethylsiloxane) (PDMS) mold, and could obtain layer-by-layer assembly of multiple crossed NW arrays. However, the size of fluidic channels may limit alignment of NWs. LB method could assemble a large-area anisotropic NWs by compression process, but it is restricted to preparation of one monolayer. Overall, for practical applications, more refinement is needed to improve the reproducibility and controllability of the above methods.

In a brief, most of the proposed schemes for device fabrication based on “bottom-up” nanostructures are plagued by complex integration that lacks reproducible transfer and positioning of NWs and reliable ohmic contacts. Moreover, the control of doping concentrations in self-assembled semiconducting NWs remains a challenge, and it's difficult for high-density integration. On the other hand, the top-down approaches usually require

expensive lithography apparatus and materials that dramatically increase the fabrication cost. To circumvent these shortcomings, we propose to develop a new method for preparation and fabrication of Si NWs TFT devices in this thesis.

1-2 Thesis organization

There are four chapters in this thesis. This thesis is organized as follows:

In Chapter 1, we introduce the development of thin-film transistors and the comparison between poly-Si TFTs and α -Si TFTs. Some basic processes of the manufacture are described in this chapter. Moreover, we also introduce the fabrication of the nano-wire.

In Chapter 2, we describe the structure and the process of our poly-Si NW TFTs. We also show some analysis of the sidewall spacer nano-wire for different conditions by SEM and TEM. We introduce the operation principles in the end of this chapter.

In Chapter 3, we discuss the performance of the poly-Si NW TFTs and the effect of post treatment. Then, we discuss the origins of off-state leakage current.

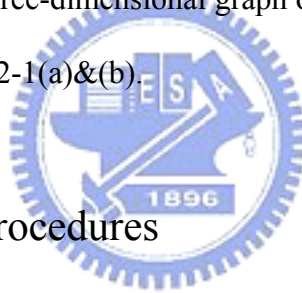
Finally, we summarize our conclusions and the future work in Chapter 4.

Chapter 2

Device Fabrication and Operation Principles

2-1 Device structure and fabrication

In this chapter, we describe the fabrication of poly-Si TFT with nano-wire channels on the oxidized silicon wafer. We propose a new approach that could potentially resolve the shortcomings mentioned in last chapter. Our approach, albeit based on “top-down” approach, involves only mature and low-cost process skills. Since it could be easily realized using state-of-the-art IC processing, this new scheme is thus very suitable and promising for future practical manufacturing. The three-dimensional graph of the device structure and the top-view layout graph are shown in Fig. 2-1(a)&(b).



2-1-1 Experimental procedures

The schematic illustration of key processes is illustrated in Fig. 2-2. The detailed process flow of poly-Si nano-wire TFT is described as follows:

(1) Zero layer fabrication:

Mark the number on silicon wafers and define the zero-layer alignment key.

1. Use laser marking to define number marks.
2. Perform SC-1 (NH_4OH) cleaning to remove the particles.
3. Use stepper (ASM) to define Zero Mark.
4. Use RIE (TEL5000) to etch silicon.
5. P.R. stripping.

(2) Substrate oxide:

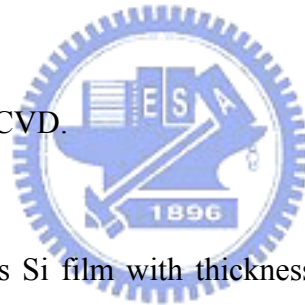
1. Perform STD (SC-1,SC-2) cleaning.
2. Grow thermal oxide (wet oxide) as to simulate the “glass” substrate.

(3) Define poly-Si gate:

1. Perform STD (SC-1, SC-2) cleaning.
2. Deposit the *in-situ* doped poly-Si film with thickness of 100 nm(or 200 nm) in an LPCVD system at 625°C.
3. Use a g-line stepper to define gate pattern (Mask 1).
4. Dry-etch of poly-Si by TCP-9400.
5. P.R. stripping.

(4) Gate oxide:

1. Perform standard RCA cleaning.
2. Dip in HF. (HF:H₂O=1:50)
3. Deposit 35 nm TEOS by LPCVD.



(5) Channel layer deposition:

1. Deposit undoped-amorphous Si film with thickness of 100 nm (or 70 nm, 50 nm) in an LPCVD system at 550°C.

(6) Solid state crystallization (SPC):

1. Before source, drain, and channel defining, some wafers were re-crystallized at 600°C in N₂ ambient for 24 hours in the furnace.

(7) Ion implantation:

1. Ion implantation(no mask): n-channel TFT: P⁺, 1×10¹⁵ cm⁻², 10 or 15 keV, tilt=0

p-channel TFT: BF₂⁺, 1×10¹⁵ cm⁻², 10 or 20 keV, tilt=0

(8) Source, drain, and channel define:

1. Use a g-line stepper to define source, drain, and channel regions (Mask 2).
2. Dry-etch to form sidewall spacer channels by TCP-9400.

3. Use In-line SEM to check the sidewall spacer width.

4. Strip P.R.

(9) Solid state crystallization (SPC):

1. After source, drain, and channel definition, the rest of wafers (not re-crystallized before dry etching) are re-crystallized at 600°C in N₂ ambient for 24 hours in the furnace.

(10) Contact hole formation:

1. Perform STD cleaning.

2. Deposit 200 nm TEOS by LPCVD.

3. Contact hole alignment mask (Mask 3).

4. Wet-etch TEOS by B.O.E.

5. Strip P.R.

(11) Metallization:

1. Dip in HF for 3 seconds.

2. Sputter-deposit 500 nm Al-Si-Cu film.

3. Metal alignment mask (Mask 4).

4. Etch metal by ILD-4100.

5. Strip P.R.

6. Post metal annealing (PMA) at 400°C in N₂ ambient for 30 minutes.

(12) Post treatment:

1. Forming gas annealing. (at 400°C in 95%N₂ and 5%H₂ ambient in the furnace for 30 minutes)

2. NH₃ plasma treatment for 1 hour and 2 hours.

-End of process-

Note that, in step (7) of the above process flow, source/drain (S/D) implant was performed with low implant-energy, so that most implanted dopants are located near the top surface of the Si layer. S/D P.R. patterns were then formed on the substrate using the G-line

stepper. Table 2-1 shows the etching recipe of the high-density plasma and etching selectivity of poly-Si to SiO₂. The etching selectivity in both main etch and over etch steps are larger than 100, which is suitable for nano-scale patterning. The sidewall Si nano-wire channels were formed in this step in a self-aligned manner. Note that the implanted dopants in places other than S/D regions will be removed during the etching step because of the very shallow projected range just mentioned. The tetraethylorthosilicate (TEOS) layer deposited by LPCVD process has been applied to integrated circuit device fabrication as an inter-metal isolation layer and a passivation layer. The deposition of TEOS by LPCVD is at 720°C in the furnace for about 2 hours and the dopants can be activated at this step and the SPC process. After sintering at 400°C in N₂/H₂ ambient for 30 minutes, the device process was completed. Some fabricated wafers were subjected to the plasma treatment with condition is shown in Table 2-2. Detailed sputter conditions are summarized in Table 2-3. The total mask number of the conventional bottom-gate TFTs is five, which is identical to that of conventional etch-stopper TFTs. Comparing to the conventional bottom gate TFTs, the total mask number of our poly-Si NW TFTs is only four.

2-1-2 Experimental results

The electrical performance of poly-Si TFTs strongly depends on the width, thickness, and quality of the channel layer. The width and thickness of the sidewall spacer channel both depend on the gate height, thickness of the α -Si channel layer deposition, and etching time for our poly-Si NW TFTs. The definition of the width and thickness of the sidewall spacer channel is shown in Fig. 2-3. Sample(1) was fabricated with 200 nm gate, 100 nm channel layer and 20 seconds over etching. Figures 2-4(a) and (b) shows TEM and SEM pictures of Sample(1), respectively. From Fig. 2-4(a), the thickness and width of the sidewall spacer

nano-wire channel are around 105 nm and 174 nm, respectively, which seem to be too large for the fabrication of nano-wire TFTs. To reduce the nanowire dimensions, gate height as well as the as-deposited channel thickness are reduced. Moreover, over etching time is used as a parameter for the control of the nanowire structure. Figures 2-5~2-11 show the cross-sectional TEM pictures of samples with various gate heights, as-deposited channel layer thickness, and the etching times. The summary of TEM results is listed in Table 2-4. Note in Fig. 2-7 that the sidewall spacer nano-wire channel has been etched off. Figure 2-12 shows that the thickness and width of sidewall spacer nano-wire channel decrease with increasing over etching time as characterized by TEM.

2-2 Operation of poly-Si NW TFT

The operation principles of our new poly-Si NW TFTs are similar to those of the conventional bottom-gate TFTs. For n-channel poly-Si NW TFTs, when the gate and drain are positively biased with respect to the source, and the gate bias is higher than the threshold voltage, the device is turned on. On the other hand, when the gate bias is smaller than the threshold voltage, the device is turned off. In contrast to conventional poly-Si TFTs in term of structural arrangement, our nano-wire channels are aligned along the sidewall of the gate.

The parameters of the transistors and I-V characteristics, including threshold voltage (V_{th}), linear maximum transconductance (G_M), and subthreshold swing (SS), were measured and extracted. All data were characterized by an HP4156 analyzer.

The on-current can be expressed as,

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_G - V_{th}) V_D - \frac{1}{2} V_D^2 \right] \quad (2-1)$$

in linear region (for $V_G > V_{th}$, $V_G - V_{th} > V_D$), where L is the channel length, W is the channel

width, μ is the mobility, and C_{OX} is the gate capacitance per unit area. The on-current in saturation region (for $V_G > V_{th}$, $V_G - V_{th} < V_D$), can also be expressed as,

$$I_D = \frac{1}{2} \mu C_{OX} \frac{W}{L} \left[(V_G - V_{th})^2 \right] \quad (2-2)$$

Then, G_M is extracted by the differentiation of equation (2-1),

$$G_M = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D=const} = \left(\frac{W}{L} \right) \mu C_{OX} V_D \quad (2-3)$$

Subthreshold swing (SS) can be calculated from the subthreshold current increase in the weak inversion region,

$$SS = \frac{\partial V_G}{\partial (\log I_D)} = (\ln 10) \frac{\partial V_G}{\partial (\ln I_D)} = 2.3 \frac{\partial V_G}{\partial (\ln I_D)} \quad (2-4)$$

These electrical parameters could be extracted from the curve of I_D versus V_G under a constant drain voltage of 0.5V.

In this thesis, we use $G_{M(max)}$ (the maximum value of G_M) to find V_{th} . This method is simple and straight-forward. ON/OFF current ratio is one of the most important performance indicators. In this thesis, we measured the ‘‘ON’’ current at $V_G=10V$, $V_D=0.5V$ and $V_G=-10V$, $V_D=-0.5V$, for n- and p-channel operation, respectively. The ‘‘OFF’’ current was measured at $V_G=-3V$, $V_D=0.5V$, and $V_G=3V$, $V_D=-0.5V$, for n- and p-channel operation, respectively.

Chapter 3

Characteristics and Discussion of NW TFT

3-1 Device performance

Recently, the poly-Si thin film transistors fabricated by low-temperature process have received extensive study for their important applications to the active matrix liquid crystal display (AMLCD)[30][31]. To optimize the design of the poly-Si NW TFTs with high performance, it is important to develop a reliable analytical methodology based on the physical mechanisms that correlates the electrical characteristics with the fabrication condition. The performance of poly-Si TFTs is dominated by trapping states at grain boundaries and within the grains themselves [32][33]. Although the electron and hole field-effect mobility of poly-Si are considerably higher than those of α -Si, the values are still much lower than those of single-crystal silicon. Fig.3-1 shows the comparison of transfer property between sample(1) and sample(2). Sample(2) has smaller off-state leakage current, larger on-current, and better subthreshold swing than Sample(1). Figure 3-2 shows the comparison of transfer characteristics between devices with 30 and 40 seconds over-etching time, both with the same gate height (100nm) and channel layer deposition thickness (100nm). However, the device with 40 seconds over-etching time depicts larger off-state leakage current, smaller threshold voltage, and better subthreshold swing than the device with 30 seconds over-etching time. It is worthy to note that the off-state leakage current of the device with 40s over-etching is larger than that with 30s over-etching. We believe this is because the nano-wire channel with longer-etching time suffered from more plasma damage during the channel-etching step. The mechanisms of off-state leakage current will be discussed in section

3-3. In addition, we also observed that both thinner channel layer and shorter over etching-time affect the characteristics of devices. The comparison on characteristics between the device with 20s over-etching and the device with 25s over-etching, both having the same gate height (100 nm) and channel layer thickness (50 nm), is shown in Fig. 3-3. The comparison on characteristics between the device with 20s over-etching and the device with 25s over-etching, both having the same gate height (100nm) and channel layer thickness (50nm) is shown in Fig. 3-3. The comparison on characteristics between devices with 54nm and 30nm nano-wire thickness is shown in Fig. 3-4. It shows the device with thinner nanowire has smaller threshold voltage and higher drain current, indicating better gate control ability. Detailed summary of characteristic parameters ($V_D=0.5V$) with various channel layer thickness and etching times is shown in Table 3-1.

The transfer characteristics of SPC-before-etching and SPC-after-etching nano-wire devices are shown and compared in Figs. 3-5(a) and (b). The two figures indicate that the devices with SPC-before-etching nano-wire have better electrical properties. For the device with SPC-after-channel-etching, α -Si was re-crystallized in a confined space, and the grain growth would be easily impeded. As a result, the grain size is smaller than that in the device with SPC before channel etching. The comparison between n-channel and p-channel devices is shown in Fig. 3-6. The characteristics of the n-channel devices are better than that of the p-channel devices, owing to higher electron mobility. The results also indicate that more attentions need to be paid to optimize p-channel devices. Fig. 3-7 shows the threshold voltage of the devices with measurement deviation versus channel length. We can see the process uniformity of poly-Si NW TFTs is less than optimum, and is worse with shorter channel. This is owing to the difficulty in grain size and nanowire dimension control. Fig. 3-8 shows the on-current versus channel length at $V_G=10V$, $V_D=0.5V$. The results in Fig.3-8 basically agree with equation (2-1).

Another very important electrical characteristic of poly-Si TFTs is I_D - V_D output characteristic. The kink effect observed in the drain current of poly-Si TFT operating in the high drain bias regime has been investigated by several works [35-39]. With the aid of two-dimensional (2-D) numerical simulation, the nature of the kink effect had been identified to be due to the impact-ionization mechanism in the high field regime near the drain for the intrinsic poly-Si TFT [35-38]. Along the channel, the formation of the potential barrier of the grain boundary and defects cause the low transconductance and high threshold voltage of poly-Si TFTs. The barrier height is expressed in terms of channel doping, gate oxide thickness, grain size, and external gate as well as drain biases. Drain bias will result in an asymmetric potential barrier and introduce more carrier injection from the lowered barrier side. It is shown that this consideration is very important to characterize the saturation region under high drain bias condition.

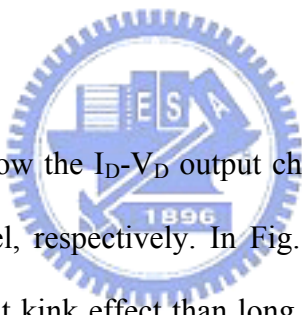


Fig. 3-9 and Fig. 3-10 show the I_D - V_D output characteristics of n-channel devices with short channel and long channel, respectively. In Fig. 3-9 and Fig. 3-10, the short channel devices exhibit more significant kink effect than long channel devices in the high drain bias region. When the drain bias is applied, the grain barrier heights for both sides of the grain boundary become asymmetric and the grain barrier height of the side near the source junction will be lower than that of the side near the drain junction. Fig. 3-11 shows the energy band diagram along the channel under high drain bias. As a consequence, there will be extra carriers injecting from the source junction through the side with lower grain barrier into the channel, resulting in the increased current. This phenomenon is so called the “drain induced grain barrier lowering” (DIGBL) effect [38]. It is more significant for short channel poly-Si TFTs [39], because the electrons drifting from source to drain is easier for short channel. Impact-ionization effect initiated by DIGBL current is another cause responsible for the kink effect of poly-Si TFTs [40]. When the intrinsic poly-Si TFT operates in the kink regime, the

impact-ionization of carriers occurs in the saturation region in which the lateral electric field is higher than the critical electric field. The impact-ionization mechanism in the saturation region is illustrated in Fig.3-12(a). Fig. 3-12(a) illustrates the multiplication process of the impact-ionization mechanism initiated by the DIGBL current, where \odot represents the Si atom-site; the arrow with dashed line shows the path of the generated electron-hole pair. The drain-source current includes DIGBL current and impact-ionization current initiated by the electrons. Fig. 3-12(b) illustrates the continuity for the mechanism of the impact-ionization initiated by the DIGBL current. Initially, electrons injecting from the source junction move toward the drain through the transport mechanisms in tandem, by surmounting the grain barriers, diffusing across the depletion regions near the grain boundaries, and drifting through the inversion regions between the depletion regions. This is the transport mechanism described by the interfacial-layer thermionic-diffusion model [41]. The generated electrons and holes, being separated by the high electric field, move toward the drain and source junctions, respectively. When reaching the drain junction, the electron flows originating both from the DIGBL and the impact-ionizations constitute the total drain-source current.

Fig. 3-13 shows the output characteristics of SPC-before-etching and SPC-after-etching samples. The drain current of the devices with SPC-before-etching nano-wire channels are larger than that of the devices with SPC-after-etching nano-wire channels. Figures 3-14(a) and (b) show I_D - V_D output characteristics of p-channel devices with short channel and long channel, respectively. It is noted that the drain current of the p-channel device is smaller than that of the n-channel device, both biased at the same absolute values of V_G , V_D , and channel length, owing to the lower hole mobility. According to the results above, we summarize that Samples with split conditions (3), (7), and (8) have better transfer properties, and the characteristics of devices with SPC-before-etching channel are better than those of devices with SPC-after-etching channel. In the next section, we will discuss how to improve the

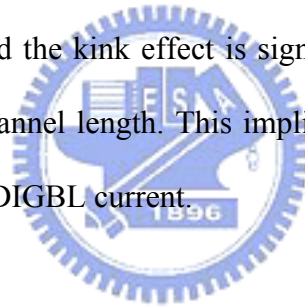
device characteristics.

3-2 Effects of post treatment

It is well known that the grain boundaries exert a profound influence on device characteristics, because electronic charges trapped within grain boundaries form potential barriers. Due to the high density of defect states at grain boundaries and interior of grains, poly-Si TFTs exhibit poor performance such as low mobility, large subthreshold swing, large threshold voltage, and large leakage current, compared to single-crystal counterparts. Therefore, to minimize the defect density in polysilicon film is essential to realizing high performance TFTs.

Hydrogen plasma passivation of polysilicon films to reduce defect states in the grains and the grain boundaries has been widely investigated for improving the electrical characteristics of polysilicon thin film transistors [42-45]. The hydrogen plasma treatments can improve the performance of poly-Si TFTs by lowering the grain boundary potential barriers [44][45]. It is well-known that hydrogenation tends to tie up the grain boundary dangling bonds and intra-grain strain bonds with hydrogen, thereby remarkably improving the characteristics of the poly-Si TFTs [44][45]. After plasma passivation, better performance including higher on/off current ratio, higher field-effect mobility, higher drive current, lower leakage current, lower threshold voltage, and lower subthreshold swing can be achieved. The effects of forming gas annealing and NH_3 plasma treatment on the subthreshold characteristics are shown in Fig.3-15 and Table 3-2. After forming gas annealing 30 mins, the characteristics of device can be improved, including higher on-current, lower off-state current, higher mobility, larger On/Off current ratio, lower subthreshold voltage, and better subthreshold swing. After NH_3 plasma treatment, the characteristics of the device are much

improved over the as-fabricated and forming-gas-annealed devices. We have also extended the NH_3 plasma treatment time, and observed the effect on electrical characteristics. Figures 3-16 and 3-17 show the device characteristics of as-fabricated sample and samples after either 1-hour or 2-hour NH_3 plasma treatments. In Fig.3-17, it can be seen that longer NH_3 plasma treatment time results in further improvement of the device characteristics. It is ascribed to more defect passivation in the films by longer NH_3 plasma treatment time. Detail device characteristics of as-fabricated sample and samples with either 1-hour or 2-hour NH_3 plasma treatment are shown in Table 3-3. In Fig.3-18, it can be seen that, after NH_3 plasma treatment, the device characteristics are similar for devices with channel layer SPC either before or after plasma, indicating that extra defects are efficiently passivated by NH_3 plasma treatment. In Figs. 3-19(a) and (b), drain current of the device after NH_3 plasma treatment is larger than that of the as-fabricated device, and the kink effect is significantly suppressed after NH_3 plasma treatment, regardless of the channel length. This implies that the passivation of defect states could effectively suppress the DIGBL current.



3-3 Origins of leakage current

Polysilicon thin-film transistors have been actively investigated for use in peripheral and active-matrix circuits in large-area liquid crystal display because of their high field-effect mobility and reliability. However, compared to amorphous silicon TFTs, poly-Si TFTs suffer from larger off-state leakage current, which could render them unacceptable for pixel driver application. In order to hold the signal at levels for acceptable image quality, the off-state current must be reduced to well below $1 \text{ pA}/\mu\text{m}$. Considerable effort has been devoted to clarifying the conduction mechanisms of off-state leakage current in poly-Si TFTs since the 1980's, such as field emission, field-enhanced thermal emission, resistive current and Frenkel-Poole emission, etc. In the earlier studies, it has generally been assumed that the

conduction mechanism of off-state leakage current is dominated by one of those proposed mechanisms. Recently, it has been found that the mechanisms of off-state current are dependent on gate bias, drain bias, device size, device structure, and fabrication conditions such as process temperature, annealing condition, hydrogenation, thickness of active poly-Si layer, and deposition method of gate insulator. In short, the leakage current is not due to a simple mechanism. In addition to the mechanisms referred to above, there are other contributions to the off-state leakage current depending upon the overall trap density and the extent to which it has been passivated as well as the film thickness and grain size effects. When a negative gate bias (V_G) is applied to an n-channel TFT, there will be considerable off-state leakage current which results from two basic mechanisms [46].

1. Resistive current: in this case the applied V_G is not negative enough to induce a p-layer in the channel surface region, so the off-state leakage current can be assumed to be an ohmic current through the poly-Si layer.
2. Junction leakage current: when V_G is more negative, a significantly reverse-biased pn junction is formed near the channel interface between the drain and channel. The junction leakage current is carried by the holes generated via grain boundary traps in the depletion region.

First, we consider the effect of plasma damage on the off-state leakage current for our poly-Si NW TFTs. In Fig.3-20, the device with longer plasma etching time exhibits higher off-state leakage for devices with SPC before etching. It is presumably due to plasma etching-induced damage on the nano-wire channel. On the other hand, reduction in the off-state leakage current with longer etching time is observed for devices with SPC after etching. It is ascribed to the fact that the SPC after etching can remove part of the plasma damage during nano-wire channel etching step. In this case, the longer etching time results in smaller cross-sectional area of the nanowire, and thus lower leakage current. It is important to

note that the off-state leakage current of the SPC-after-etching device is still higher than the SPC-before-etching device. Moreover, the transfer characteristics of the SPC-after-etching device are not better over those of the SPC-before-etching device. It may be due to the smaller grain size of the channel layer for the device with SPC-after-etching, as mentioned in previous section. The off-state leakage current as a function of V_G and V_D is shown in Figs. 3-21(a) and (b). Higher drain bias results in higher off-state leakage current. Furthermore, the more negative the gate bias, the higher the off-state leakage current. In order to further discuss the reason of off-state leakage current, we have to understand the activation energy in the off-state region. The activation energy of the off-state can be obtained from the temperature dependence of the drain current. The governing equation of off-state current, activation energy, and temperature is given by

$$I_{\text{off}} = I_0 e^{-\frac{E_a}{kT}} \quad (3-1),$$

where I_0 = constant independent of temperature, and E_a = drain current activation energy.

The equation also can be expressed as

$$\log(I_{\text{off}}) = \log(I_0) + \left(\frac{-E_a}{kT} \right) \quad (3-2).$$

The off-state currents with various temperatures (25°C, 50°C, 75°C, 100°C, and 125°C) are shown in Fig. 3-22(a). Next, we use equation (3-2) to plot the Arrhenius plot, which is shown in Fig. 3-22(b). The activation energy (E_a) can be extracted from the slope of the data lines [47]. Figure 3-23(a) shows the dependence of E_a on gate and drain voltages. Either more negative gate bias or higher drain bias can reduce the activation energy, and results in larger off-state leakage current. In Fig. 3-23(b), the activation energy of the device with NH_3 plasma treatment is higher than that of as-fabricated device at high gate and drain voltages. It is suggested to be due to the fact that NH_3 plasma can effectively passivate the defects and trap states in the poly-Si film [48]. In the off-state, E_a decreases with increasing drain voltage at a

given constant gate voltage. Under lower drain bias, E_a keeps roughly a constant value about $0.5eV$ ($\sim E_g/2$). Two possible mechanisms are proposed to account for the off-state leakage current for our devices.

Mechanism 1:

This mechanism considers the trap-assisted conduction processes occurring laterally from channel to the drain. There are three related cases illustrated in (a), (b), and (c) of Fig. 3-24.

- (a) Pure thermal emission or thermal generation: this is due to thermal excitation of an electron from valence band into trap-state, and the trapped electron is emitted to the conduction band by the same way.
- (b) Thermionic field emission: this is due to the field-enhanced emission under a medium electric-field strength. This case comprises two steps in tandem: the first step is the thermal activation of an electron from the valence band to a trap state, and the second step is electron tunneling through the reduced barrier to the conduction band as shown in Fig. 3-24(b).
- (c) Field emission or tunneling: under a strong electric field, the band gap is pulled more severely. It causes the electrons to tunnel from the valence band to the conduction band via the trap states.

All the processes stated above are common to poly-Si thin film transistors with top-gate self-aligned structure, and the presence of trap state in the band-gap plays an important role. The trap-assisted field emission current has the strongest dependence on the applied bias, but is essentially independent of temperature, thus it is dominant under low-temperature and/or high-field conditions. The thermal emission current is proportional to the intrinsic carrier concentration of silicon (n_i) which is proportional to $\exp[-E_g/2kT]$ (where E_g is the energy

band gap of silicon, k is the Boltzmann constant, and T is temperature in Kelvin). For this reason, the activation energy of the pure thermal emission current should be approximately equal to $E_g/2$. In addition, the pure thermal generation current is nearly independent of gate voltage.

Mechanism 2:

In Fig. 3-25, it highlights the unique gate-drain overlap region that defines the top gate width of our device. The off-state current for different gate widths is shown in Figs. 3-26(a) and (b). As can be seen in the figures, the off-state current is actually proportional to the gate width, implying that the conduction path is located in the gate-drain overlap regions illustrated in Fig.3-25. We also extracted the activation energy for devices with gate width of 5 and 1 μm , respectively. The results are shown in Fig. 3-27. It can be seen that the activation energy is essentially independent of the gate width at both $V_D=0.5\text{V}$ and $V_D=5\text{V}$, indicating the same conduction mechanism is responsible for the samples, and it occurs in the gate-drain overlap region. Fig. 3-28 illustrates the band diagrams of three cases in the gate-drain overlap region for mechanism 2 proposed to explain the leakage current conduction:

- (a) Low electric field: in this situation, both gate and drain bias are low. Therefore, the off-state current is dominated by thermal emission.
- (b) Medium electric field: the electrons in the valence band are thermally activated to the trap states, and then tunnel to the conduction band. This is known as the thermionic field emission.
- (c) High electric field: under this situation, quasi Fermi level at the channel/oxide interface shifts nearer to valence band edge, and band-to-band tunneling takes place easier with the aid of trap states, which may lead to a high leakage current in the off-state region.

Those processes well explain the dependence of activation energy on V_G and V_D shown

in Fig.3-27, and the resulted current is proportional to the gate-to-drain overlap width indicated in Fig.3-26. This conduction mechanism is thus believed to be responsible for the off-state leakage characterized in this work.



Chapter 4

Conclusions and Future Works

4-1 Conclusions

In this work, a novel poly-Si NW TFT device and its fabrication method are proposed. The overall process of this device is very simple, fast, and cheap. In this approach, we can obtain the sidewall spacer nano-wire by channel layer etching. Critical dimensions of the nano-wires can be adjusted by setting appropriate gate height, channel layer thickness, and etching time.

In this work, the novel NW device is successfully demonstrated. Reasonable performance of the fabricated device is obtained, and could be dramatically improved using NH_3 plasma treatment. For example, high On/Off current ratio of near 10^7 is obtained. In addition, we analyzed and discussed the origins of the off-state leakage current. It is also identified that the gate-to-drain overlap region determines the off-state leakage. Based on this finding, further improvement on reducing the leakage current is possible by appropriately modifying the device's structural parameters and the process conditions.

Table 4-1 highlights the major advantages of the proposed scheme. This technique is manufacturable and economic, and is capable of providing a reliable high-performance poly-Si NW TFTs which are not only useful for biosensors but also for investigating nano-scale semiconductor physics. It is also compatible with the low-temperature poly-Si (LTSP) technologies, and could be integrated on low-cost and flexible substrates (such as glass or plastic), making the fabrication of system-on-panel (SOP) for biologic sensing and regulating purpose products possible.

4-2 Future works

Polycrystalline silicon is rich in grain boundary defects as well as intragrain defects, and the electrical activity of these charge-trapping centers profoundly affects the TFT characteristics. To further improve the device performance, it is important to reduce the defects and trap-states in poly-Si film for the poly-Si NW TFT. This could be achieved by using the MILC or ELC to enlarge the grain size of the poly-Si films.

Another important work is to reduce the off-state current with optimized device layout and structure. Furthermore, we may use other materials like the poly-Ge film to potentially enhance the carrier mobility, and the silicide material for S/D to reduce the parasitic resistance. With suitable optimization, we believe that the performance of poly-Si NW TFTs can be improved significantly. As long as decent performance is achieved, the new NW device can be readily applied to a variety of novel applications in the future.

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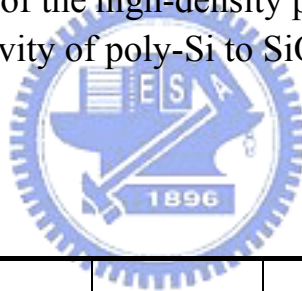
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	Pressure (mtorr)	RF Top power (W)	RF Bottom Power (W)	Gas Flow (sccm)	Etching Selectivity (Si/SiO ₂)	Time (second)
Break Through Step	5	250	200	Cl ₂ : 80	10.4	4
Main Etch Step	17	160	33	Cl ₂ : 22 O ₂ : 1.5 HBr : 165	157	End point
Over Etch Step	25	250	33	O ₂ : 2 HBr : 150	368	20,25,30,40

Table 2-1 Etching recipe of the high-density plasma and the corresponding etching selectivity of poly-Si to SiO₂.



Plasma	RF power (watt)	Pressure (mtorr)	Flow rate (sccm)	Temperature (°C)
NH ₃	200	300	700	300

Table 2-2 NH₃ plasma treatment conditions.

Split condition	Gate deposition (nm)	Channel layer deposition (nm)	Ion implantation	Etching time (sec)
1	200	100	Dopant: P ⁺ E=15keV, dose=1E15	Main etching +OE 60s
2	100	100	Dopant: P ⁺ E=15keV, dose=1E15	Main etching +OE 30s
3	100	100	Dopant: P ⁺ E=15keV, dose=1E15	Main etching +OE 40s
4	100	100	Dopant: P ⁺ E=15keV, dose=1E15	Main etching +OE 50s
5	100	100	Dopant: BF ₂ ⁺ E=15keV, dose=1E15	Main etching +OE 40s
6	100	50	Dopant: P ⁺ E=10keV, dose=1E15	OE 20s
7	100	50	Dopant: P ⁺ E=10keV, dose=1E15	OE 25s
8	100	70	Dopant: P ⁺ E=10keV, dose=1E15	Main etching +OE 20s
9	100	70	Dopant: P ⁺ E=10keV, dose=1E15	Main etching +OE 30s

Table 2-3 Split conditions

Split conditions	Thickness	Width
Gate 200nm Channel layer 100nm Main etch + OE 20s	174 nm	105 nm
Gate 100nm Channel layer 100nm Main etch + OE 30s	47.0 nm	35.1 nm
Gate 100nm Channel layer 100nm Main etch + OE 40s	22.9 nm	21.0 nm
Gate 100nm Channel layer 100nm Main etch + OE 50s	0 nm	0 nm
Gate 100nm Channel layer 50nm OE 20s	53.8 nm	53.6 nm
Gate 100nm Channel layer 50nm OE 25s	33.8 nm	34.7 nm
Gate 100nm Channel layer 70nm Main etch + OE 20s	30.0 nm	27.9 nm
Gate 100nm Channel layer 70nm Main etch + OE 30s	0 nm	0 nm

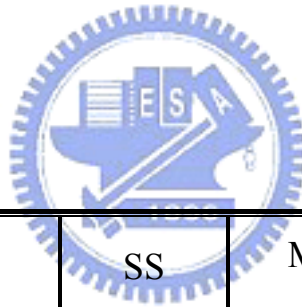
Table 2-4 Summary of the feature size of nano-wire with 100nm gate by TEM.

Split conditions	V_{th} (V)	SS (V/dec)	Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	On/Off ratio
Gate 100nm Channel layer 100nm Main etch + OE 30s	6.36	0.96	19	1.47×10^5
Gate 100nm Channel layer 100nm Main etch + OE 40s	5.97	0.88	24	1.38×10^5
Gate 100nm Channel layer 50nm OE 20s	3.55	0.60	21	2.91×10^5
Gate 100nm Channel layer 50nm OE 25s	3.90	0.67	24	7.20×10^4
Gate 100nm Channel layer 70nm Main etch + OE 20s	3.49	0.50	29	6.94×10^5

Table 3-1 The summary of characteristic parameters with various channel layer thickness and etching time at $V_D=0.5\text{V}$. (SPC before etching)

	V_{th} (V)	SS (V/dec)	Mobility ($cm^2V^{-1}s^{-1}$)	On/Off ratio
As-fabricated	6.36	0.96	19	1.47×10^5
Forming Gas annealing-30ms	5.13	0.80	20	1.92×10^5
NH ₃ plasma treatment-1hr	1.66	0.31	34	3.35×10^6

Table 3-2 Comparison of characteristic parameters among as-fabricated FG-annealed, and NH₃ plasma-treated n-channel devices, all at $V_D=0.5V$.



	V_{th} (V)	SS (V/dec)	Mobility ($cm^2V^{-1}s^{-1}$)	ON/OFF ratio
As-fabricated	5.97	0.88	24	1.38×10^5
NH ₃ -1hr	2.67	0.35	48	2.33×10^6
NH ₃ -2hrs	1.87	0.29	50	8.90×10^6

Table 3-3 Comparison of n-channel device characteristics among as-fabricated, NH₃ plasma treatment 1hr, and 2hrs.

	Size of NWs	Alignment of NWs	Sensitivity	Cost & Process
Top-down	Good control	Good control	Can be high	Expensive, high techniques and complicated
Bottom-up	Rely on nanocluster and growth time	Not easy to control	Can be high	Medium, but complex integration
<i>Our Approach</i>	<i>Good control</i>	<i>Good control</i>	<i>Can be improved by re-crystallization and V_{th}-set to modify</i>	<i>Cheap and simplified, reliable and reproducible</i>

Table 4-1 Summary of major features of conventional top-down, and bottom-up approaches, and our approach.

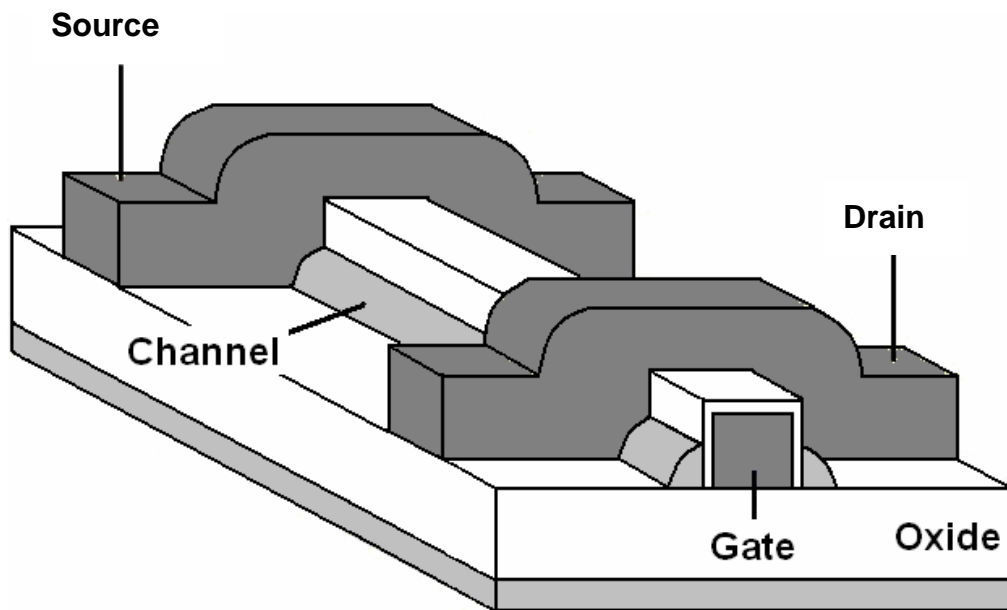


Figure 2-1 (a) Device structure of the proposed poly-Si NW TFT.

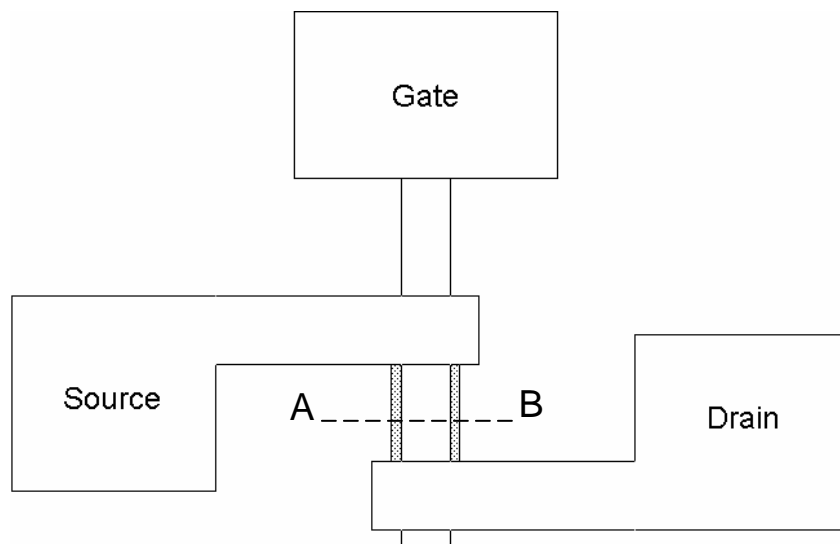
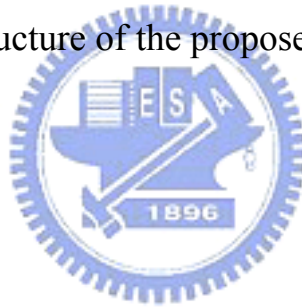
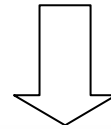
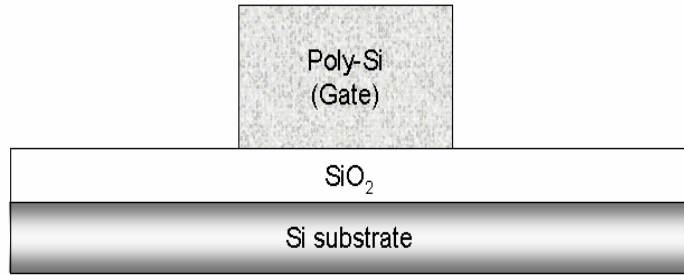
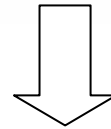
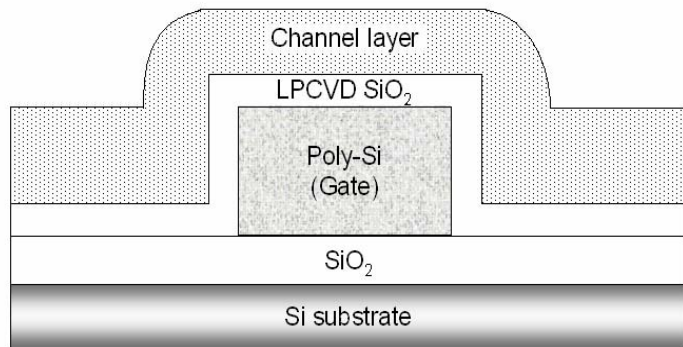


Figure 2-1 (b) Top-view layout of the poly-Si NW TFT.

- Wet oxidation (glass substrate)
- LPCVD in-situ doped poly-Si
- Define gate



- LPCVD TEOS (gate insulator)
- LPCVD a-Si channel layer



- Ion implantation

Dopant atoms →

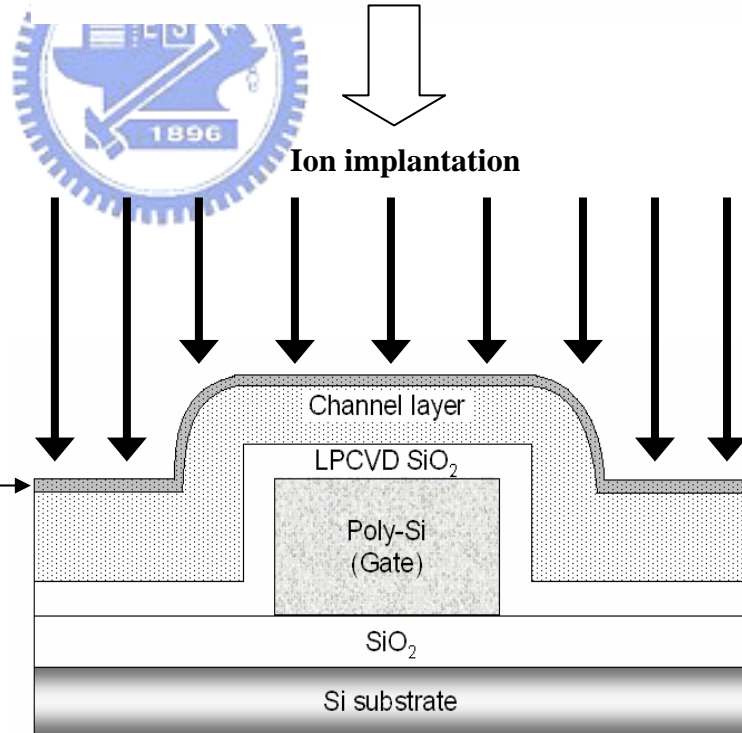


Figure 2- 1 The key process flow of poly-Si NW TFT.

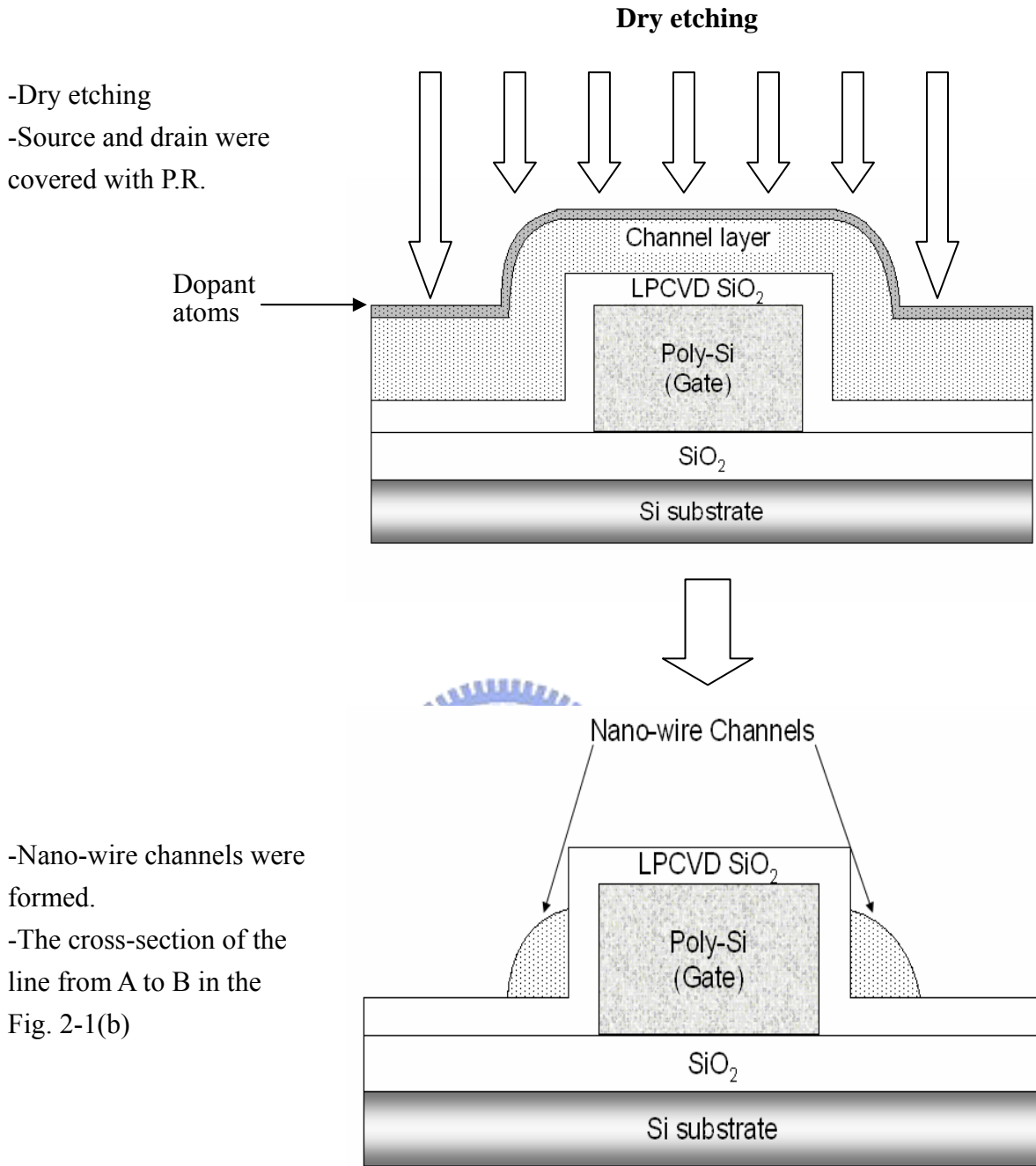


Figure 2-2 Key process flow of poly-Si NW TFT.

Nano-wire Channel

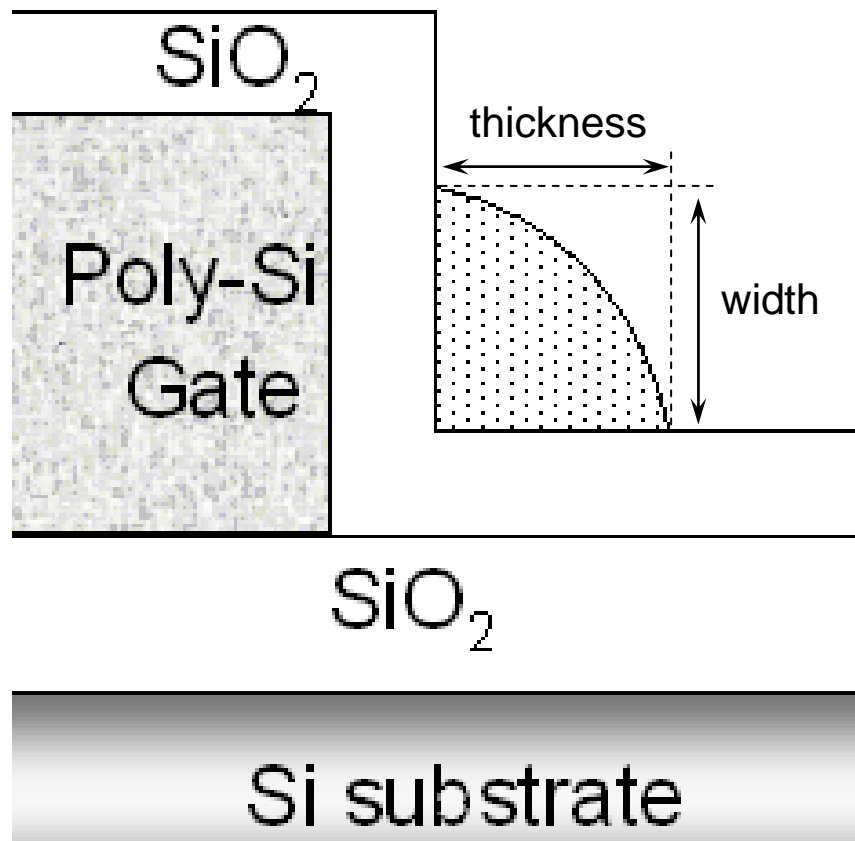


Figure 2-3 Definition of the nanowire width and thickness.

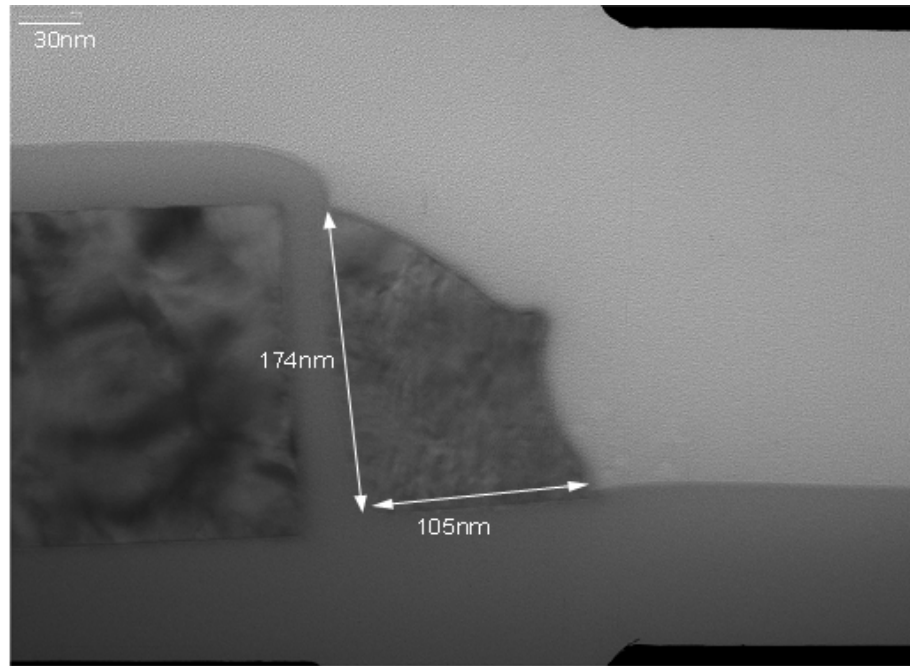


Figure 2-4 (a) Cross-sectional TEM picture of the sample(1).

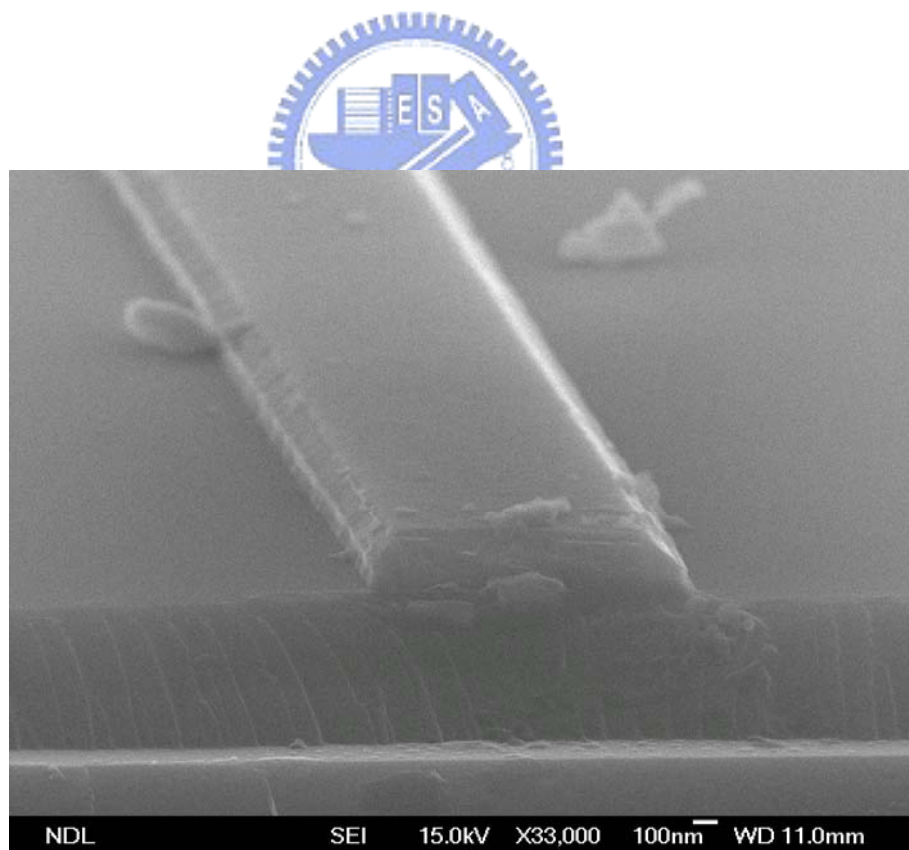


Figure 2-4(b) SEM picture of the sample(1).

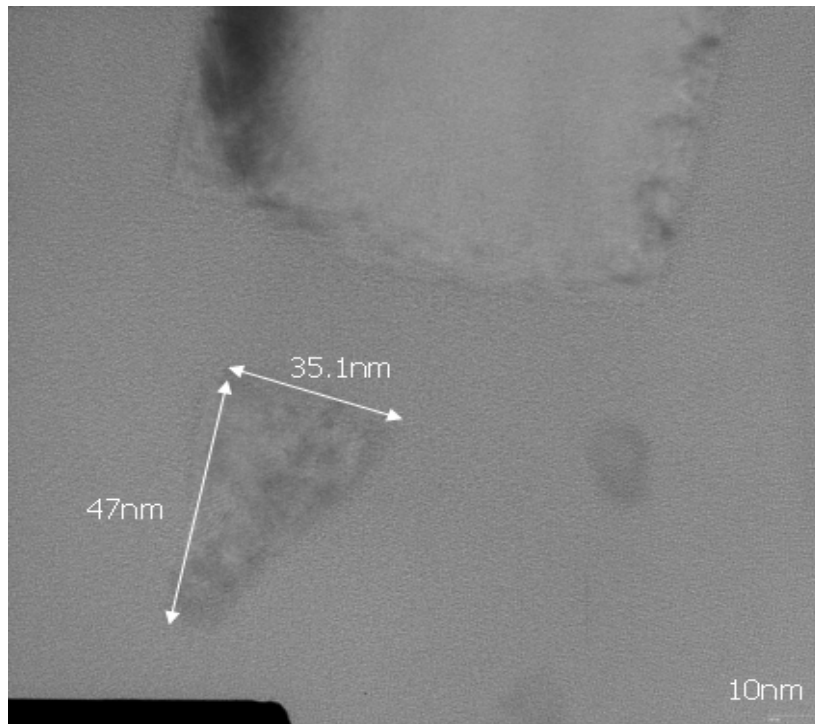


Figure 2-5 Cross-sectional picture of sidewall spacer nano-wire channel of sample(2) by TEM.

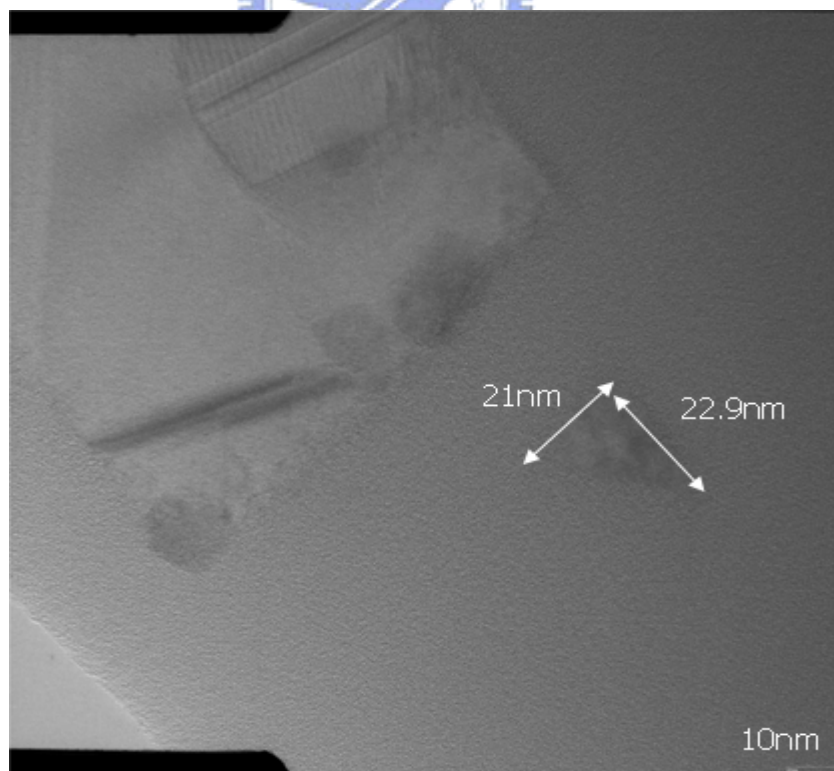


Figure 2-6 Cross-sectional picture of sidewall spacer nano-wire channel of sample(3) by TEM.

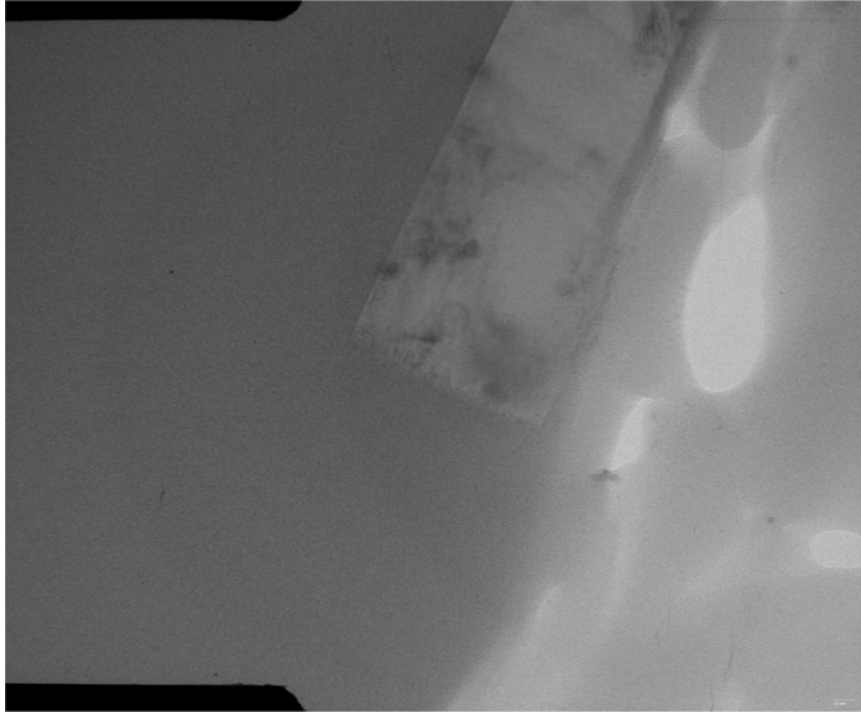


Figure 2-7 Cross-sectional picture of sidewall spacer nano-wire channel of sample(4) by TEM.

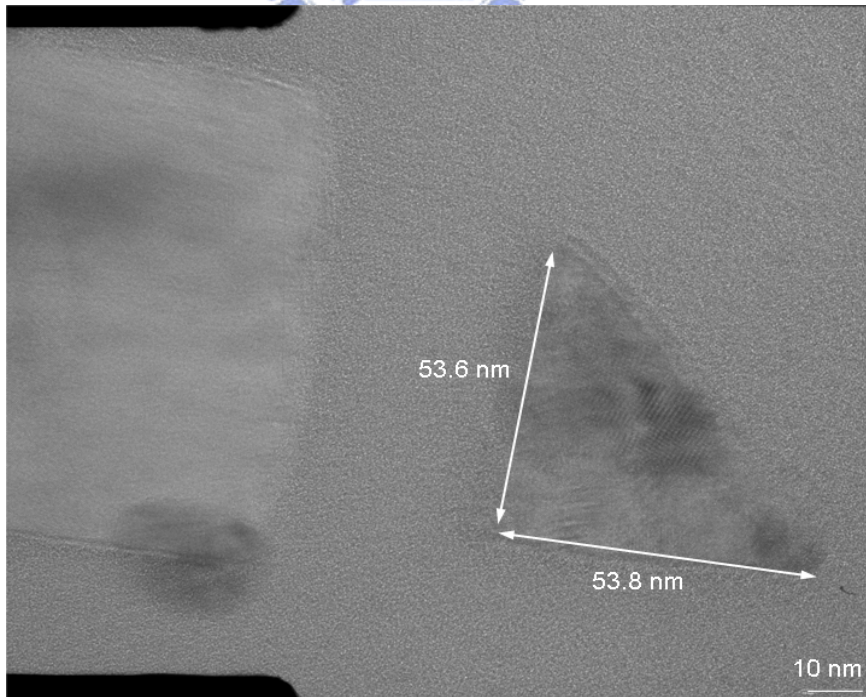


Figure 2-8 Cross-sectional picture of sidewall spacer nano-wire channel of sample(6) by TEM.

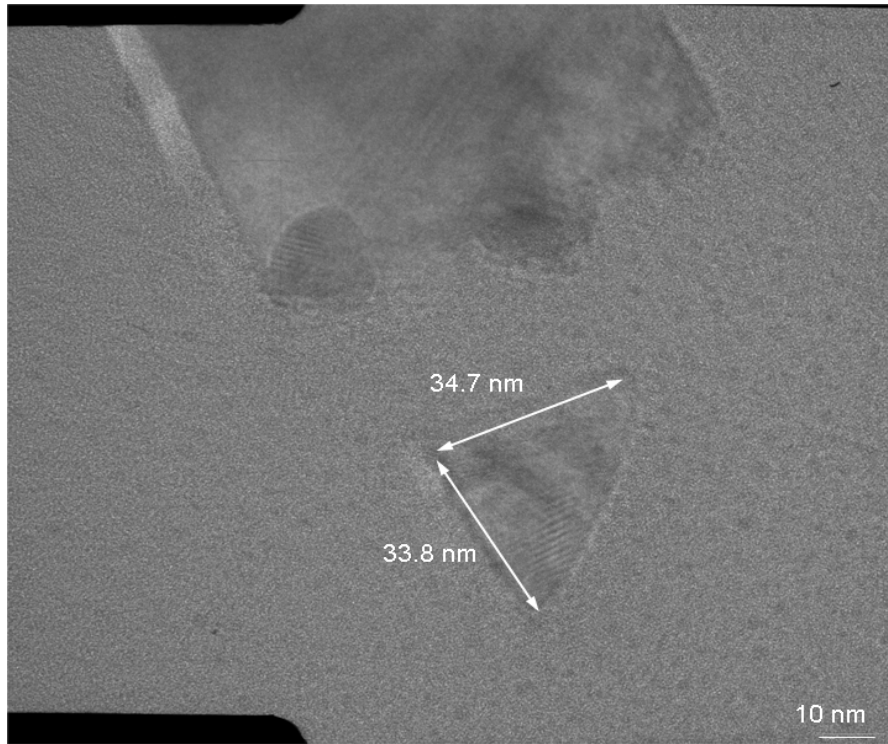


Figure 2-9 The cross-sectional picture of sidewall spacer nano-wire channel of sample(7) by TEM.

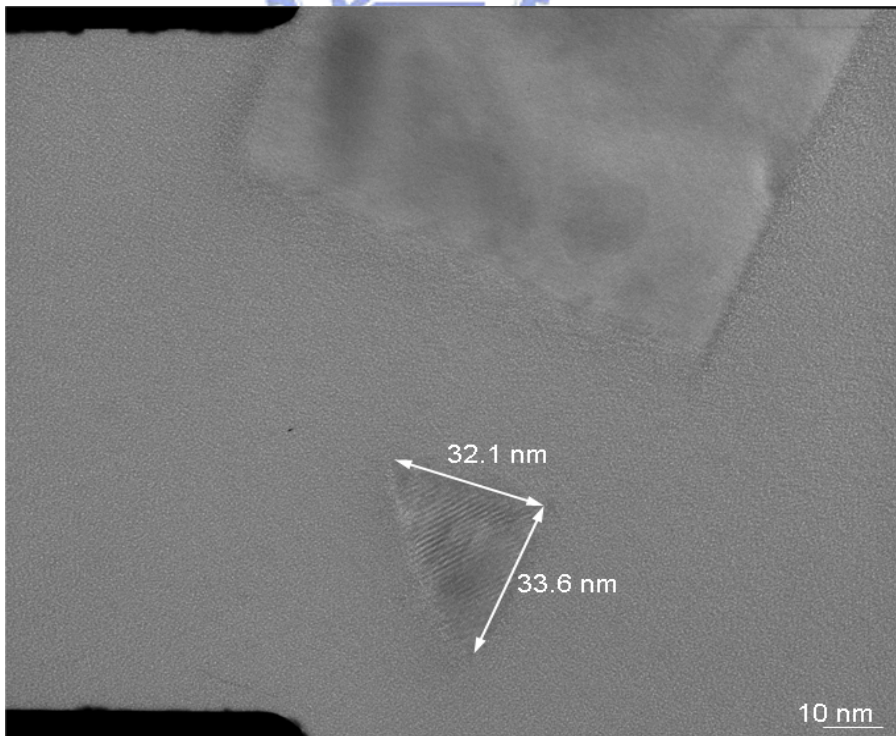


Figure 2-10 Cross-sectional picture of sidewall spacer nano-wire channel of sample(8) by TEM.

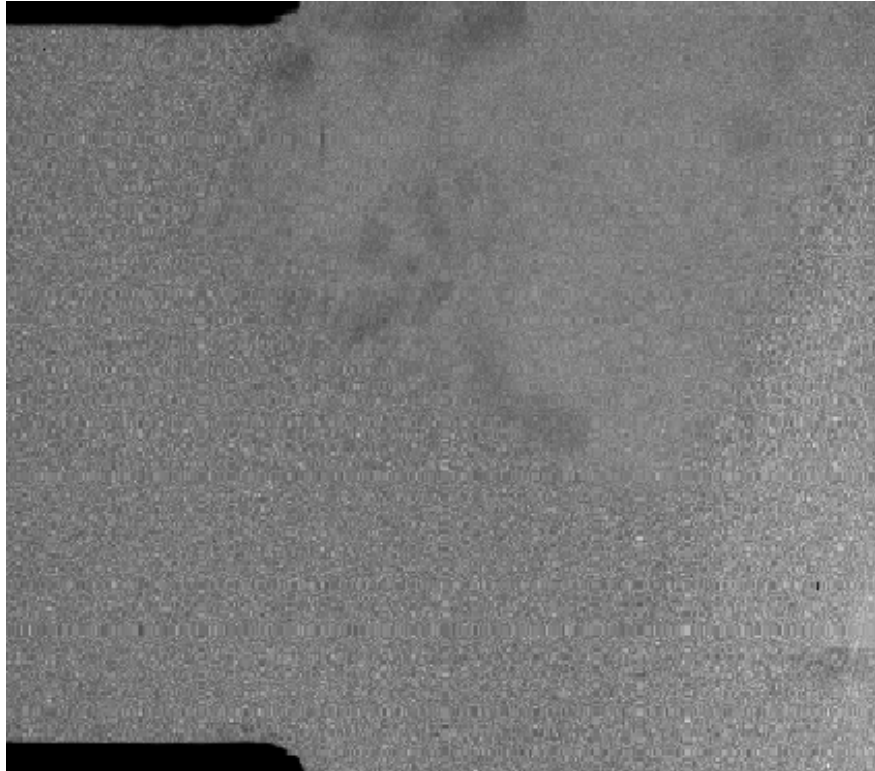


Figure 2-11 Cross-sectional picture of sidewall spacer nano-wire channel of sample(9) by TEM.

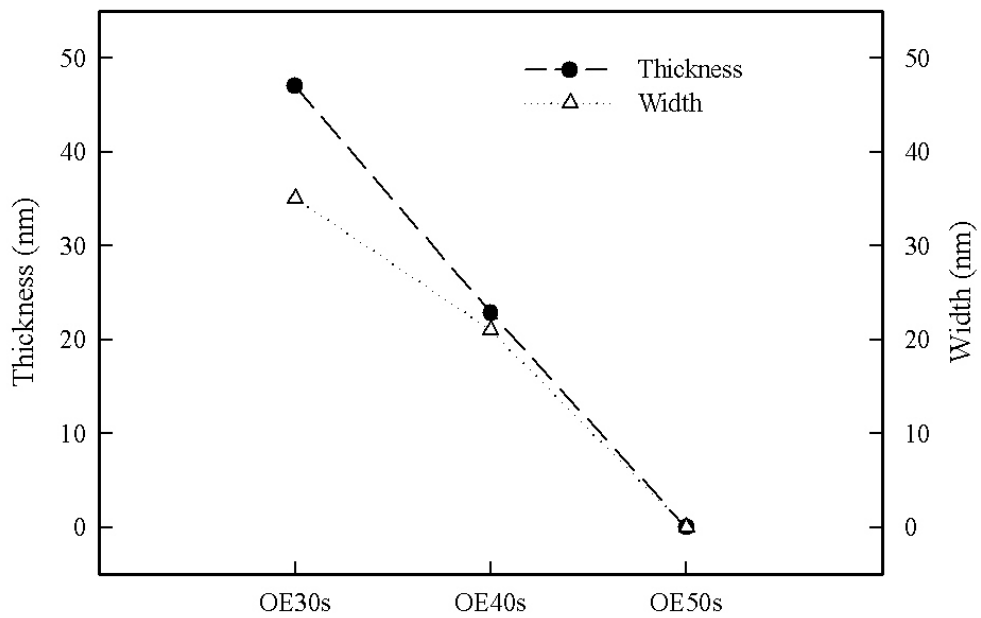


Figure 2-12 Cross-sectional nanowire width and thickness as a function of over etching time by TEM for samples(2), (3), and (4).

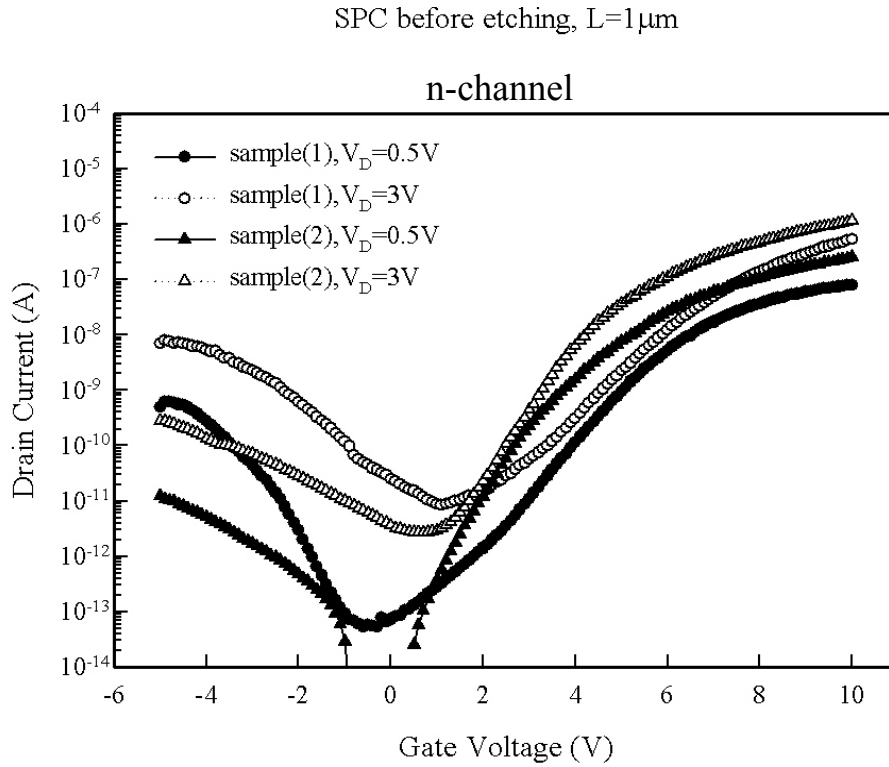


Figure 3-1 Typical transfer characteristics of sample(1) and sample(2).

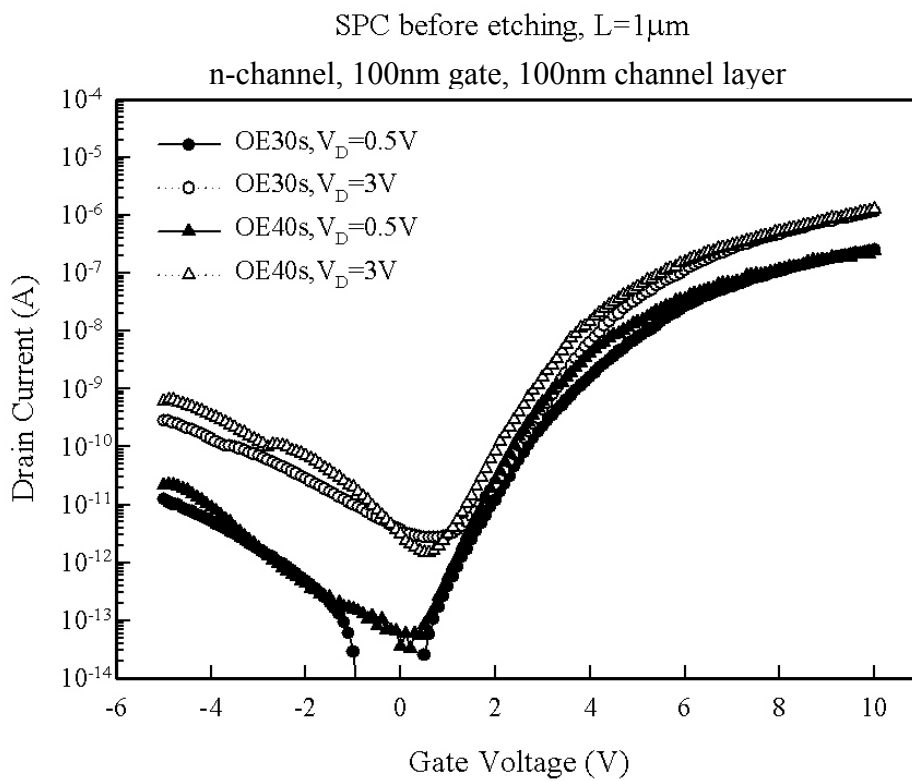


Figure 3-2 Typical transfer characteristics of devices with over etching of 30s and over etching 40s.

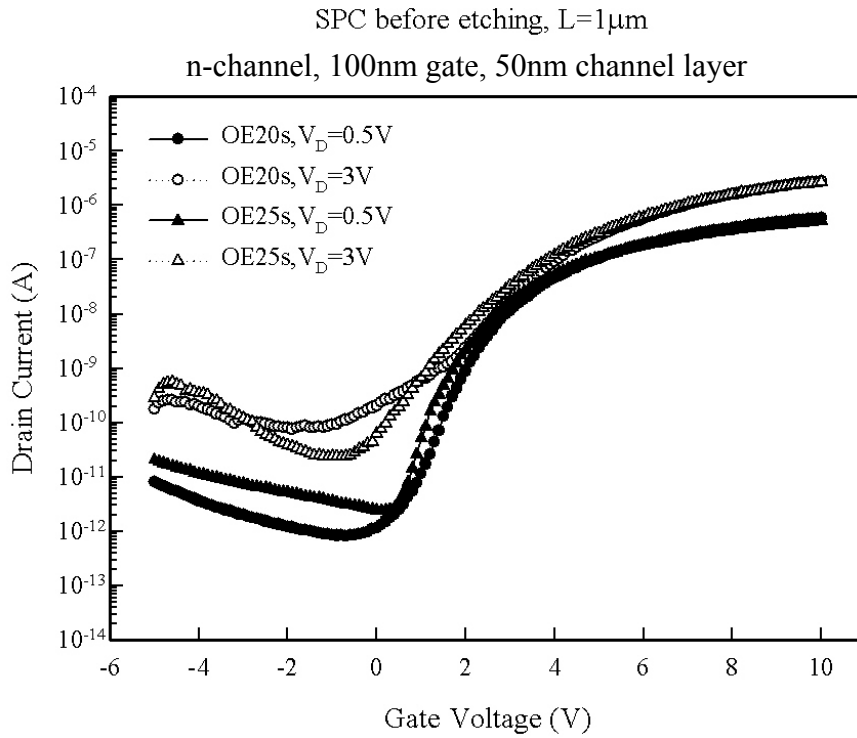


Figure 3-3 Typical transfer characteristics of devices with over etching of 20s and over etching 25s.

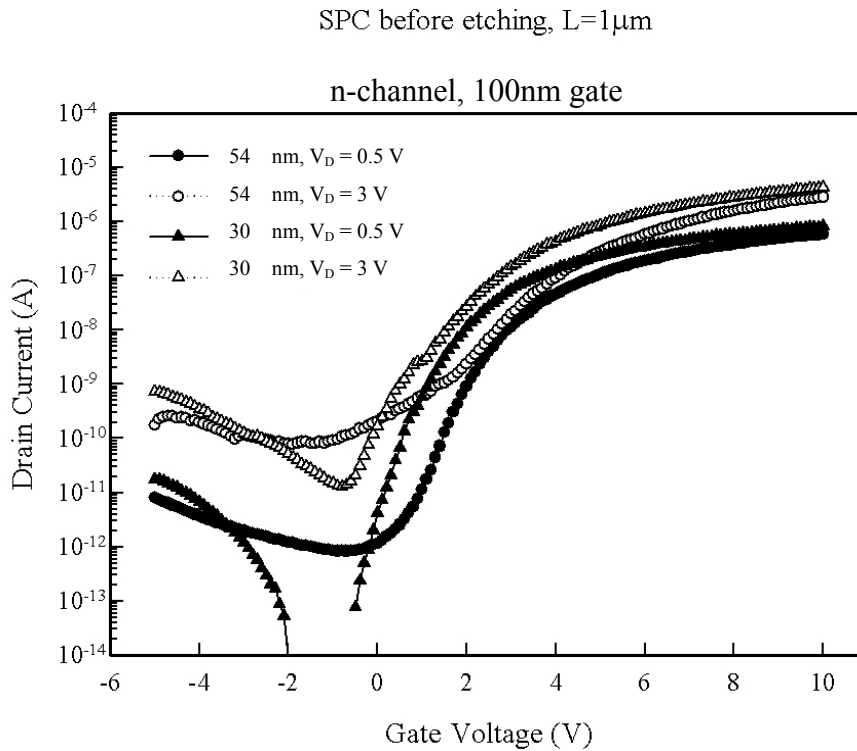


Figure 3-4 Typical transfer characteristics of devices with nanowire thickness of 54 and 30 nm.

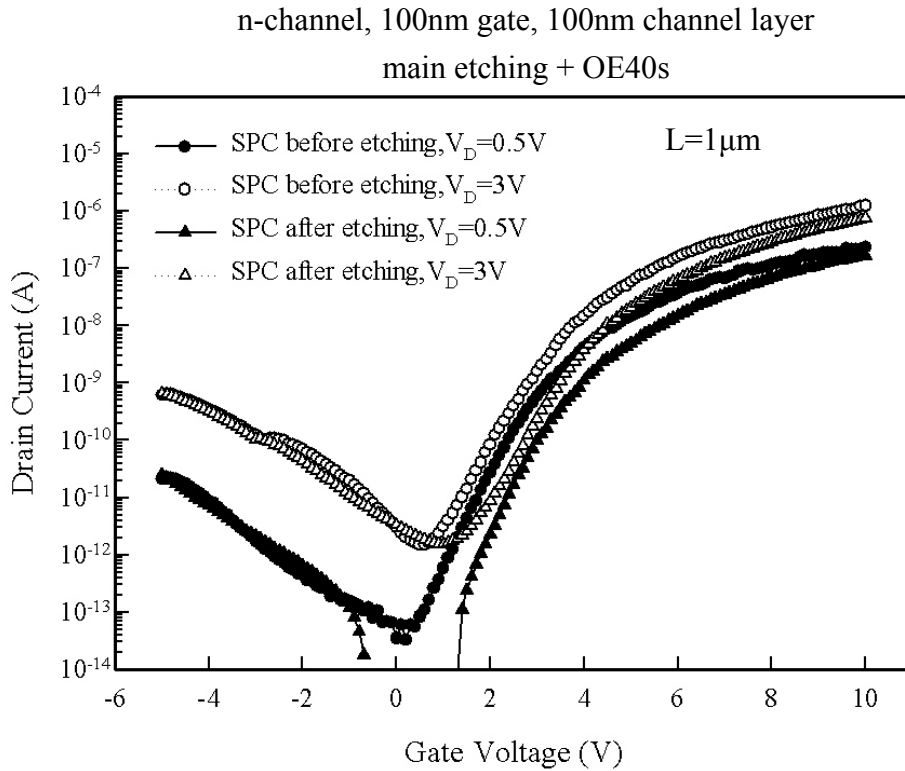


Figure 3-5 (a) Typical transfer characteristics of devices with channel layer SPC before plasma etching and SPC after plasma etching (OE40s).

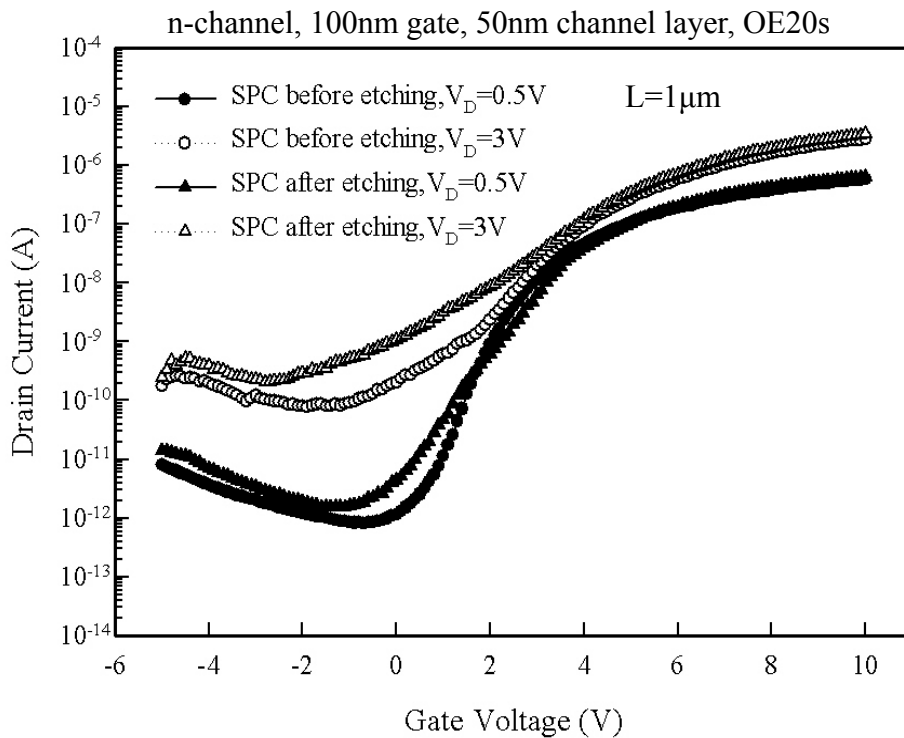


Figure 3-5(b) Typical transfer characteristics of devices with channel layer SPC before plasma etching and SPC after plasma etching (OE20s).

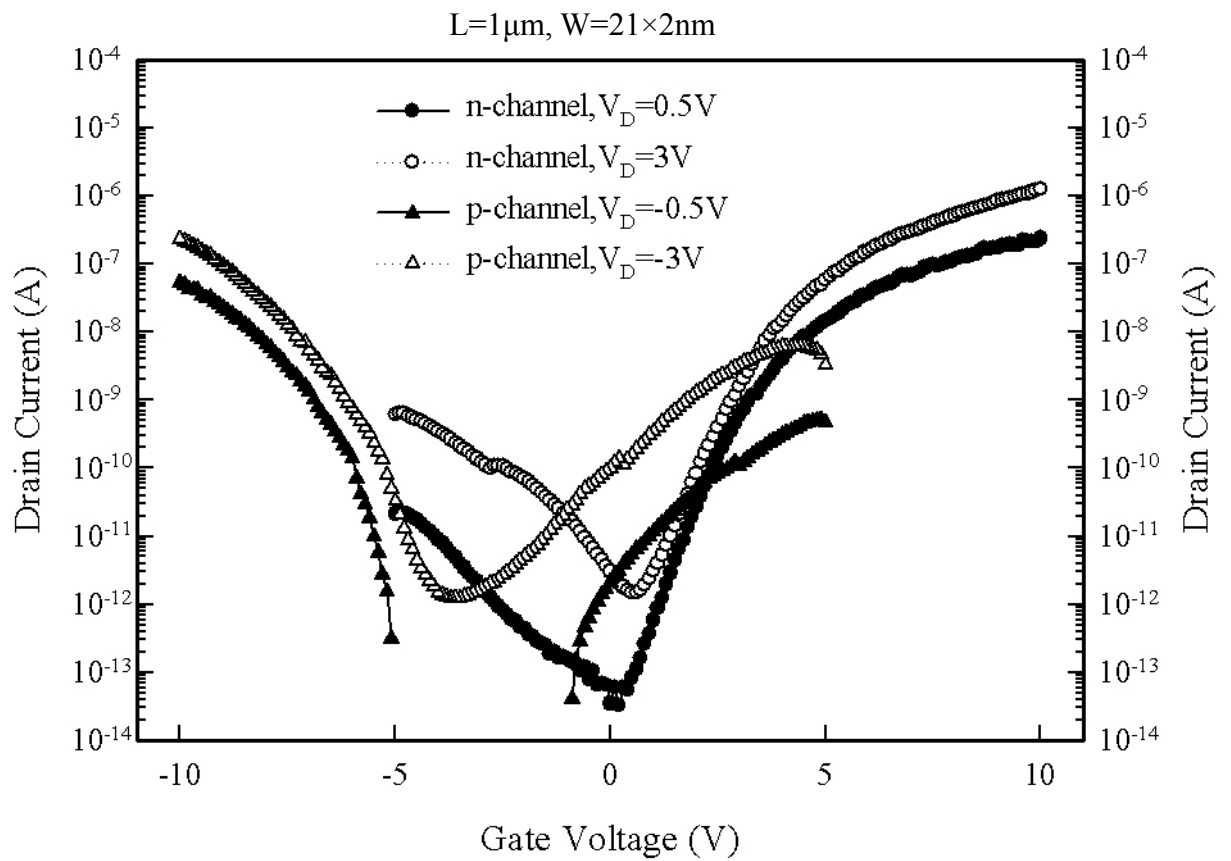


Figure 3-6 Typical transfer characteristics of n-channel and p-channel devices.

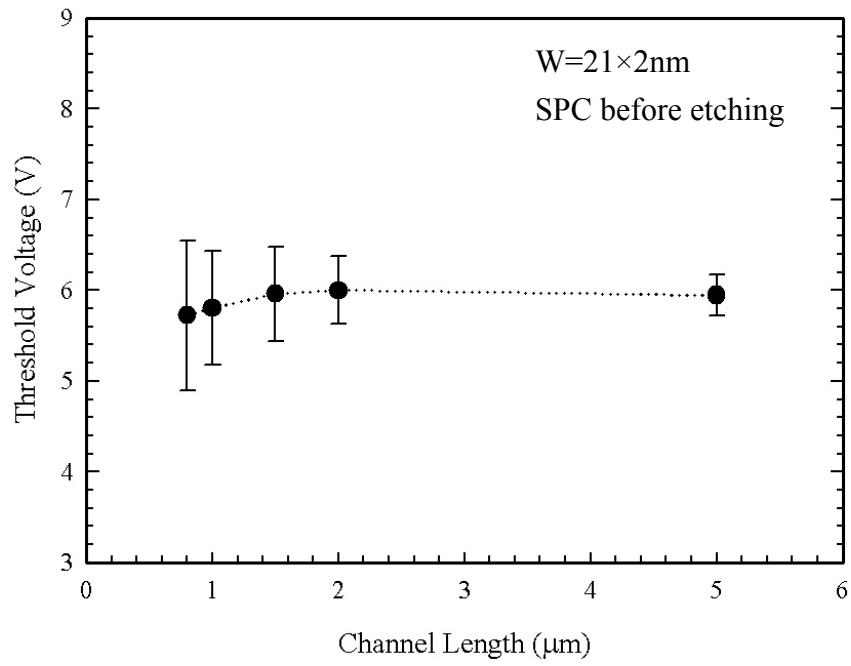


Figure 3-7 V_{th} and its deviation as a function of channel length.

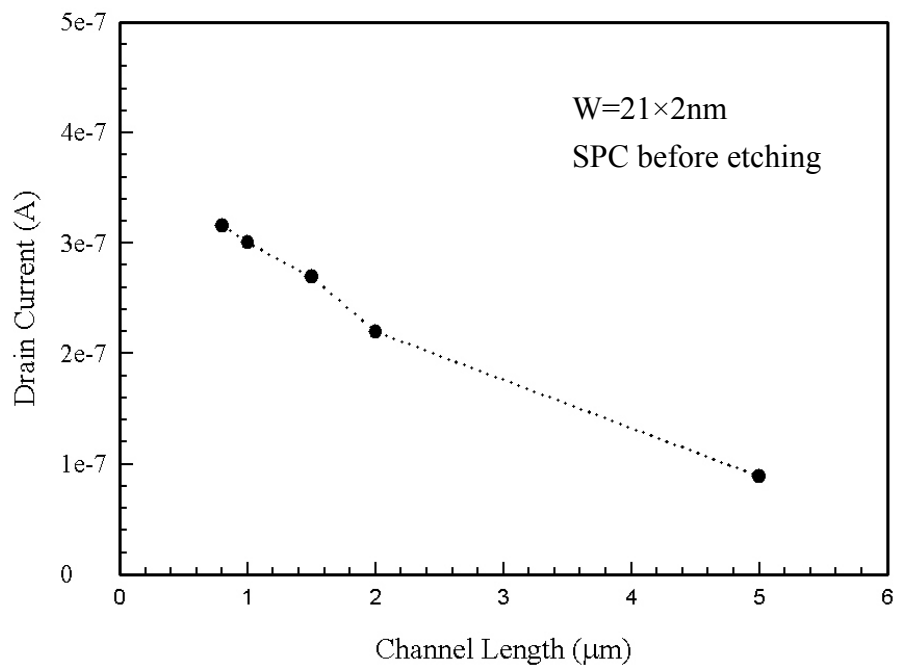


Figure 3-8 On-state drain current versus channel length at $V_G=10V$ and $V_D=0.5V$.

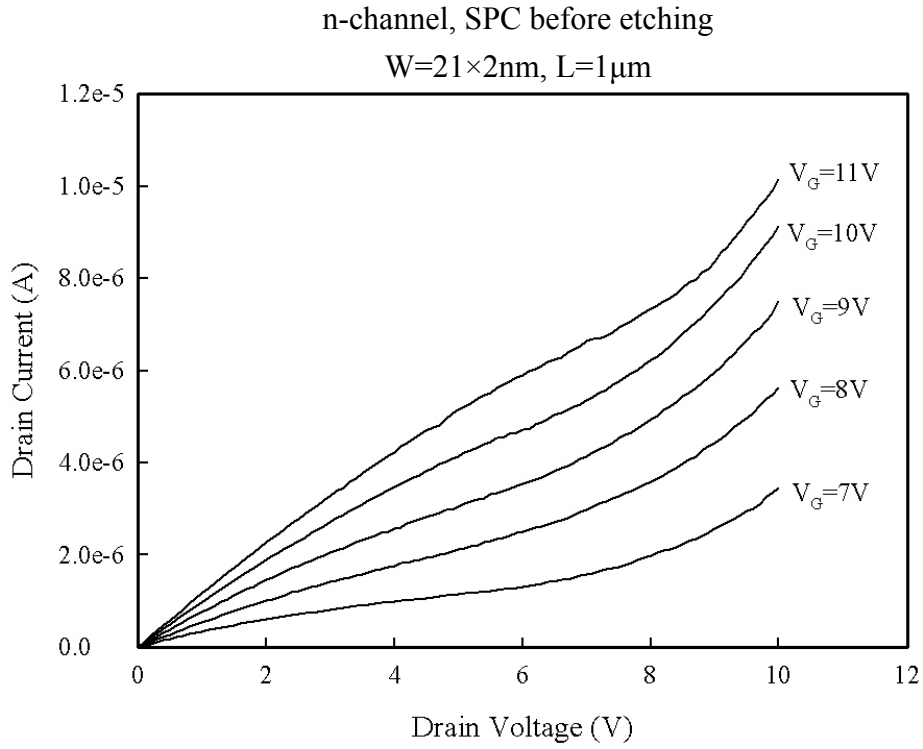


Figure 3-9 (a) I_D - V_D output characteristics of a short channel device ($L = 1\mu\text{m}$).

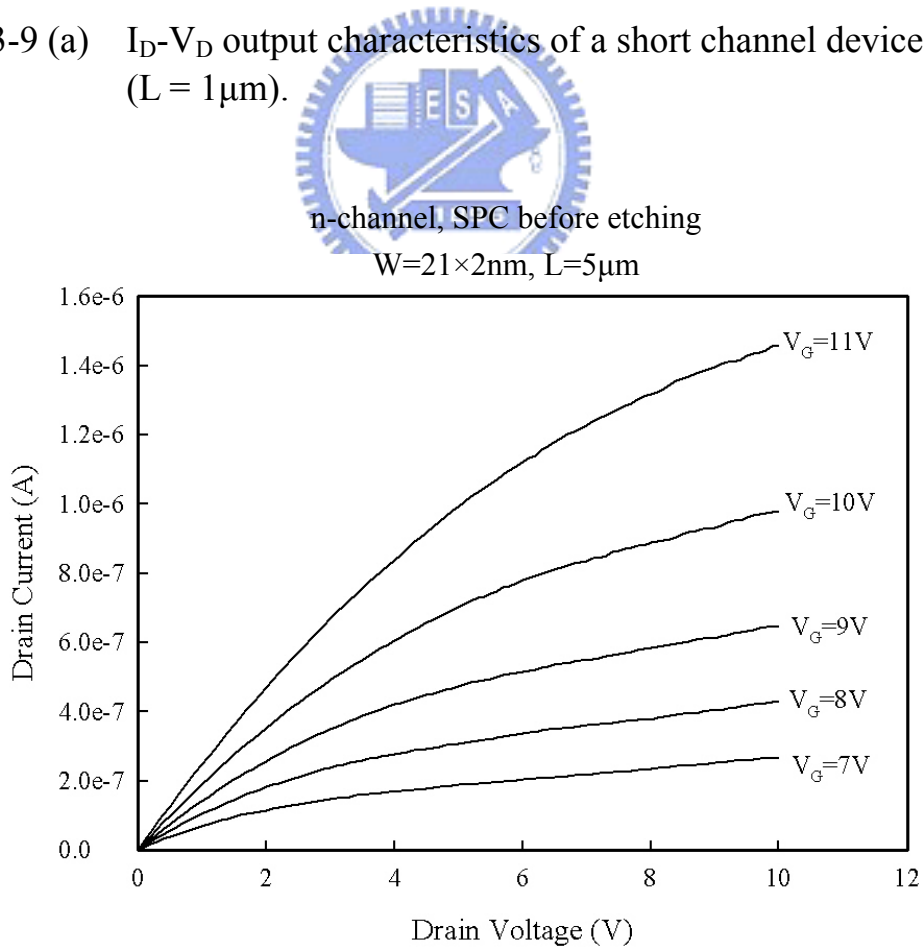


Figure 3-9 (b) I_D - V_D output characteristics of a long channel device ($L = 5\mu\text{m}$).

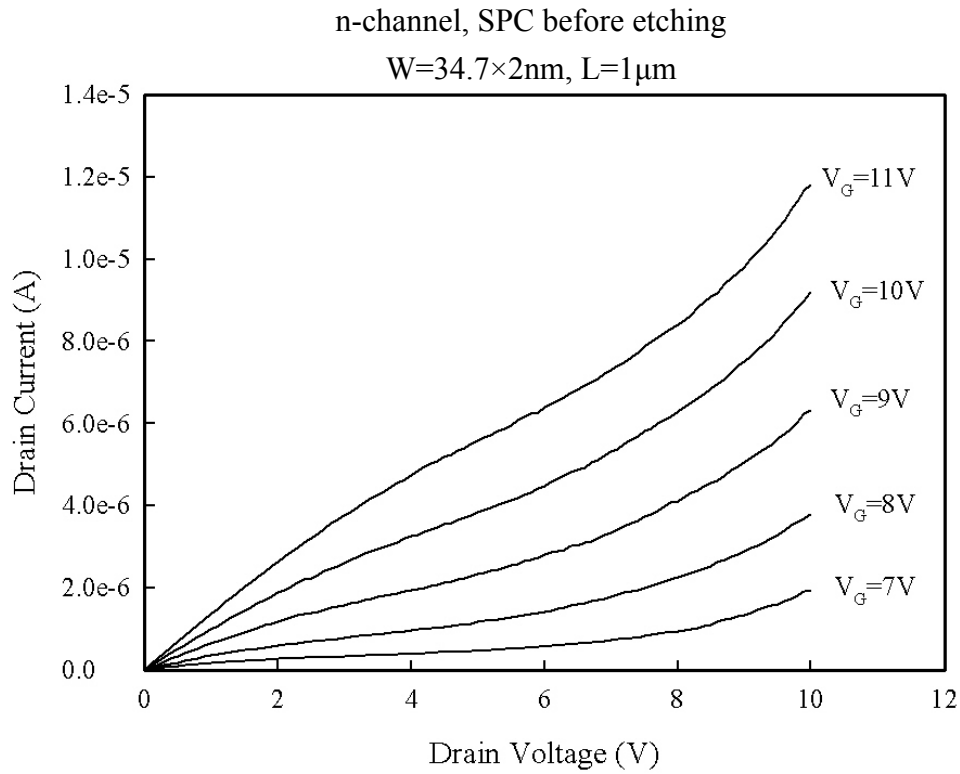


Figure 3-10 (a) I_D - V_D output characteristics of a short channel device ($L=1\mu\text{m}$).

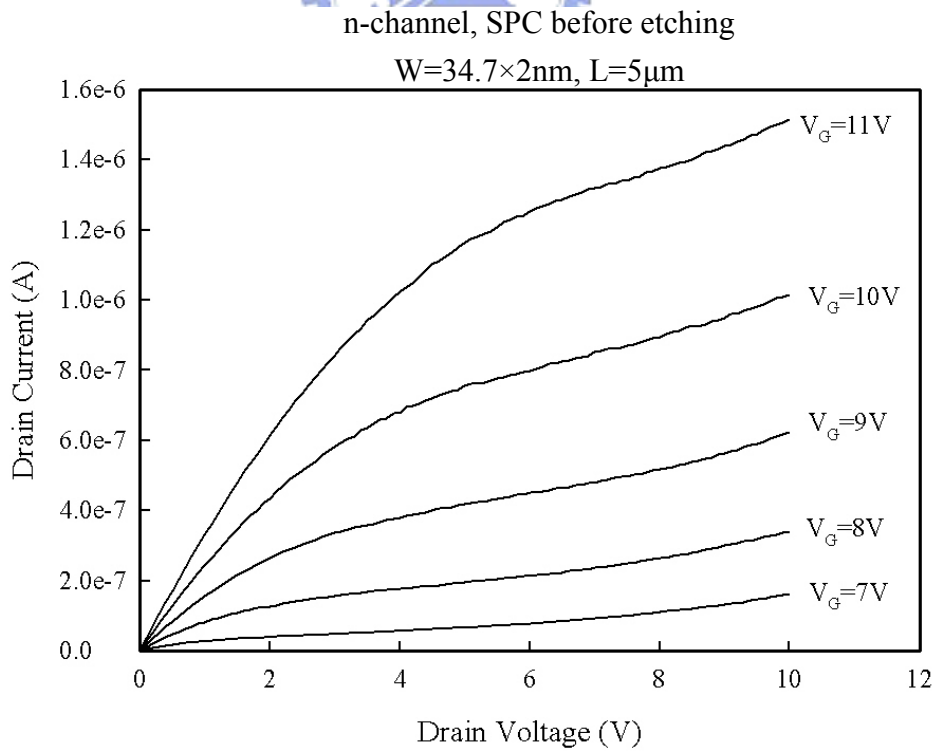


Figure 3-10 (b) I_D - V_D output characteristics of a long channel device ($L=5\mu\text{m}$).

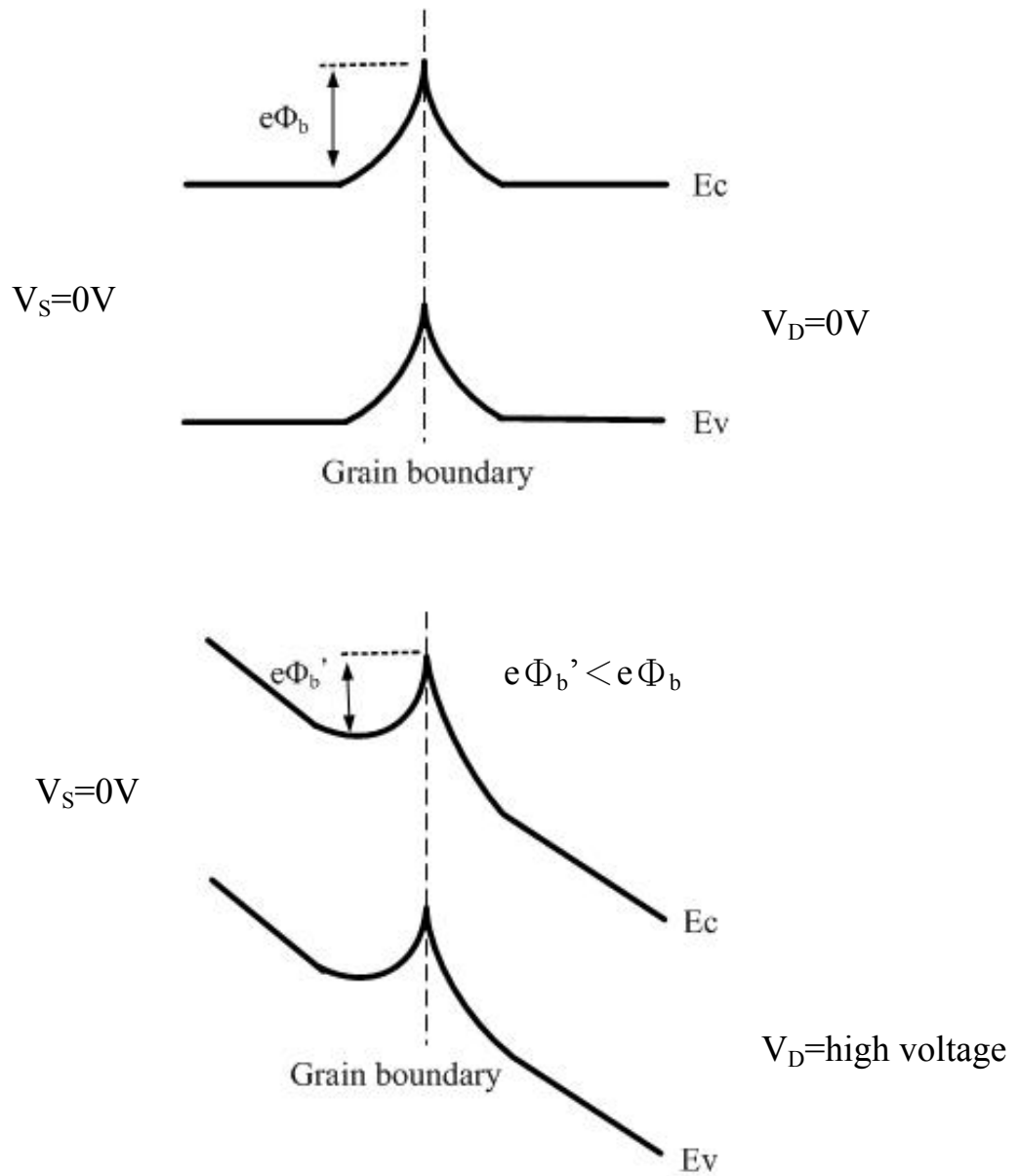


Figure 3-11 Energy band diagram along the channel at $V_D = 0V$ and $V_D = \text{high voltage}$.

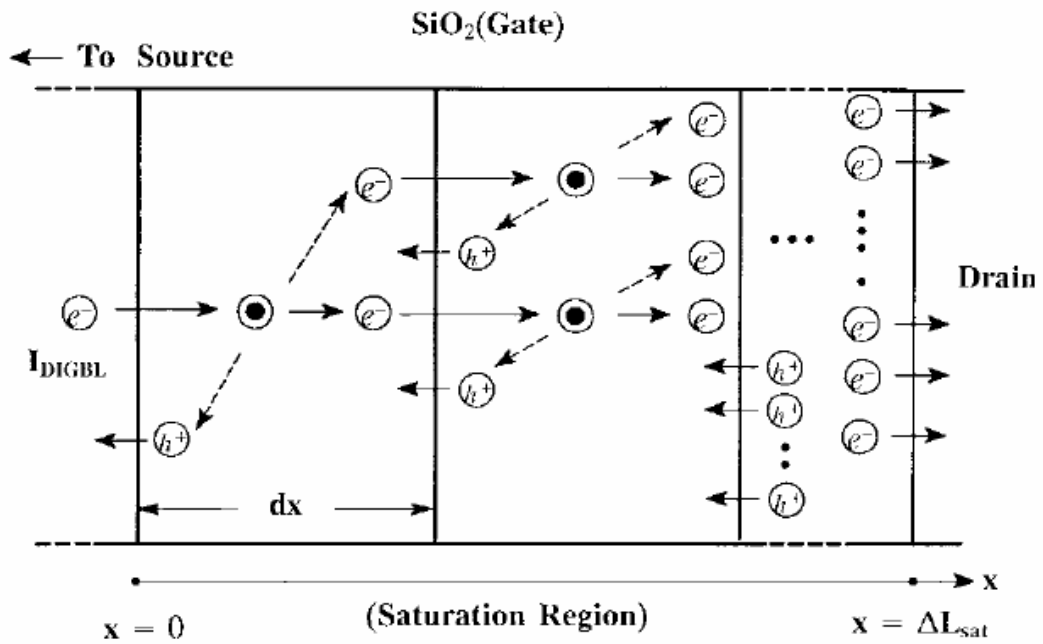


Figure 3-12 (a) Cross-sectional view of the saturation region in the intrinsic n-channel poly-Si TFT.

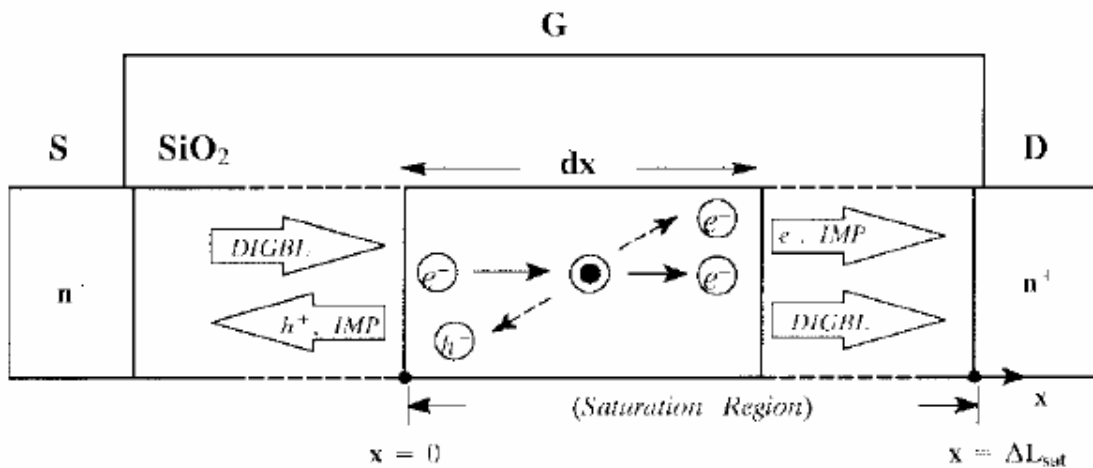


Figure 3-12 (b) Diagram illustrating the current continuity for the impact-ionization mechanism initiated by the DIGBL current in the intrinsic n-channel poly-Si TFT.

(Reference: Hsin-Li Chen, Ching-Yuan Wu, "A New I-V Model Considering the Impact-Ionization Effect Initiated by the DIGBL Current for the Intrinsic n-Channel Poly-Si TFT's", IEEE Trans. Electron Devices, vol.46, no.4, pp.722-728, 1999.)

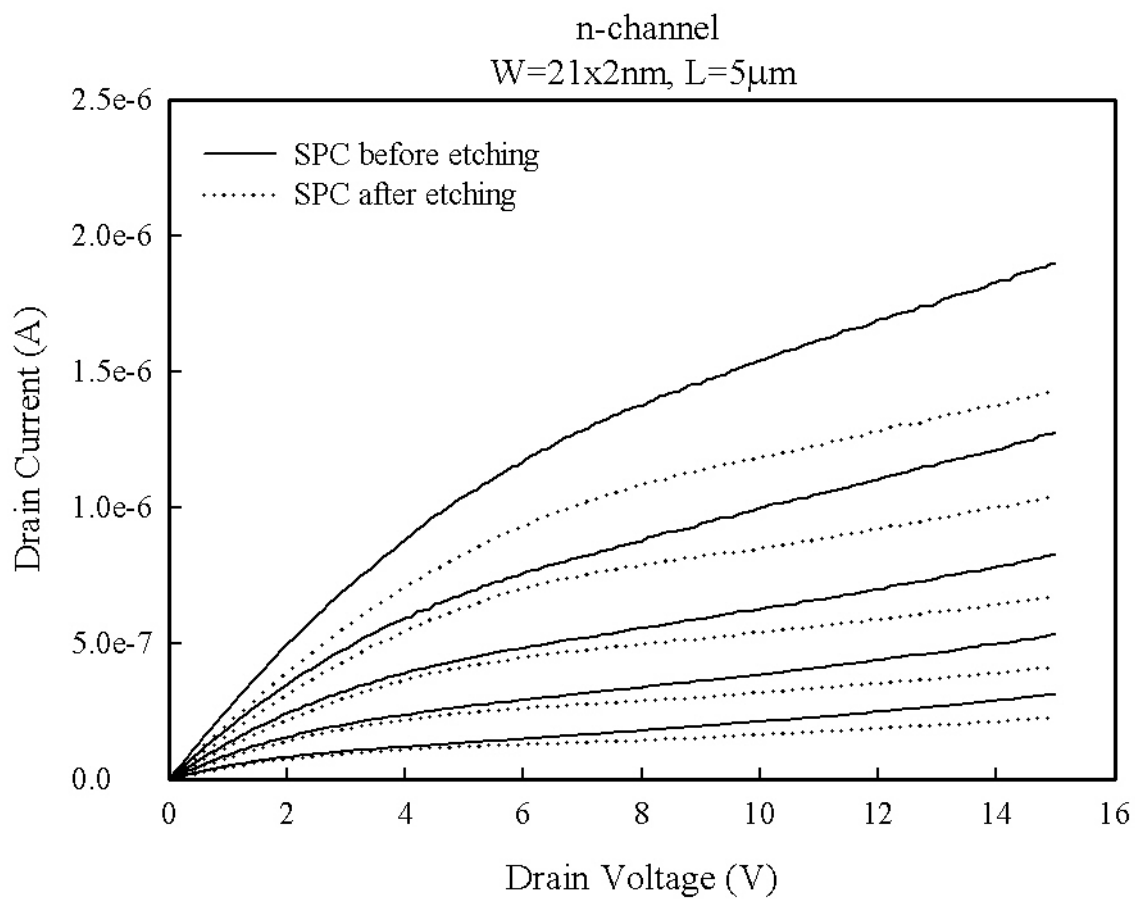


Figure 3-13 The I_D - V_D output characteristics of devices with SPC before and after etching.

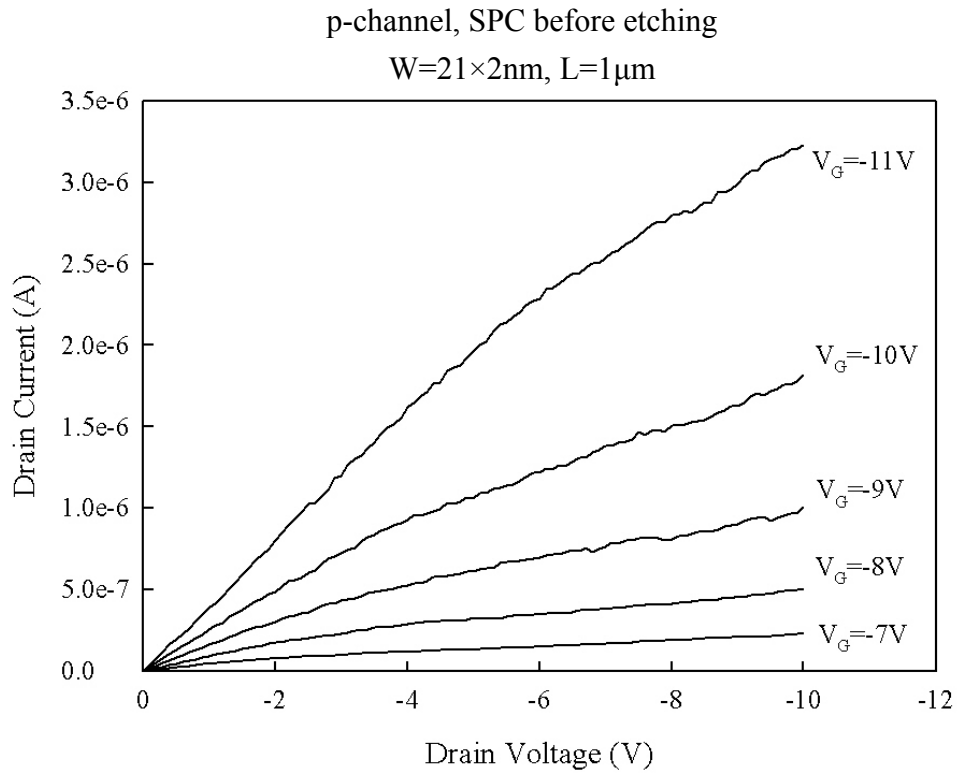


Figure 3-14 (a) I_D - V_D output characteristics of a short p-channel device ($L = 1\mu\text{m}$).

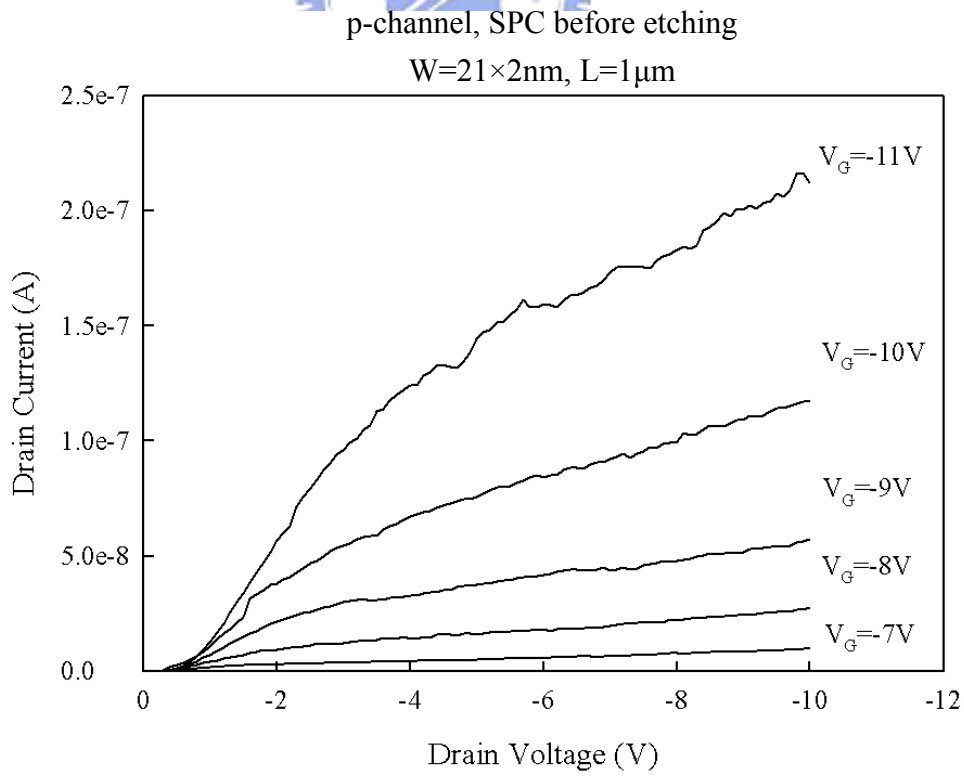


Figure 3-14(b) I_D - V_D output characteristics of a p-channel device ($L = 5\mu\text{m}$).

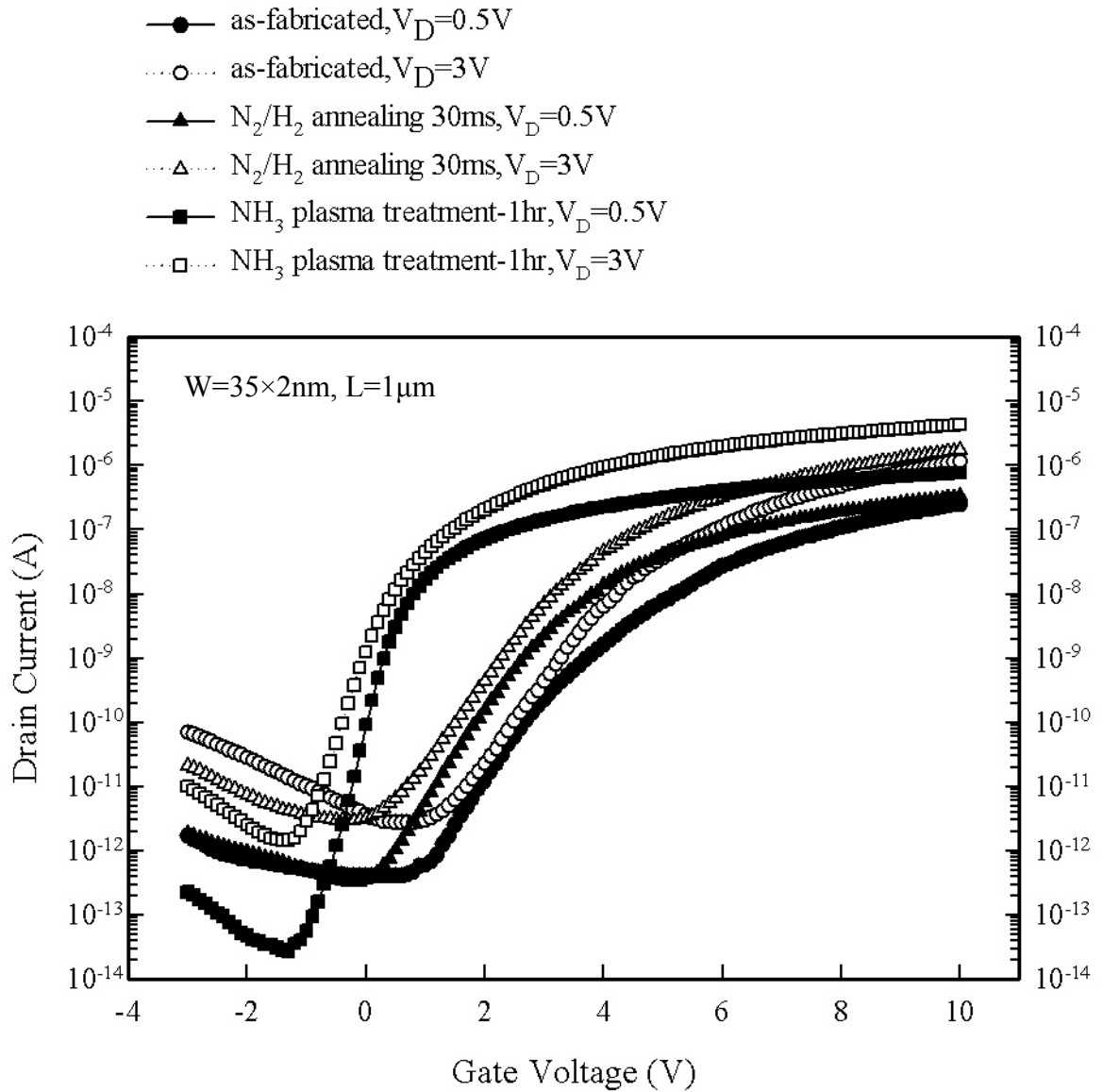


Figure 3-15 Subthreshold characteristics of as-fabricated device and devices with N_2/H_2 gas annealing 0.5hr, and NH_3 plasma treatment-1hr.

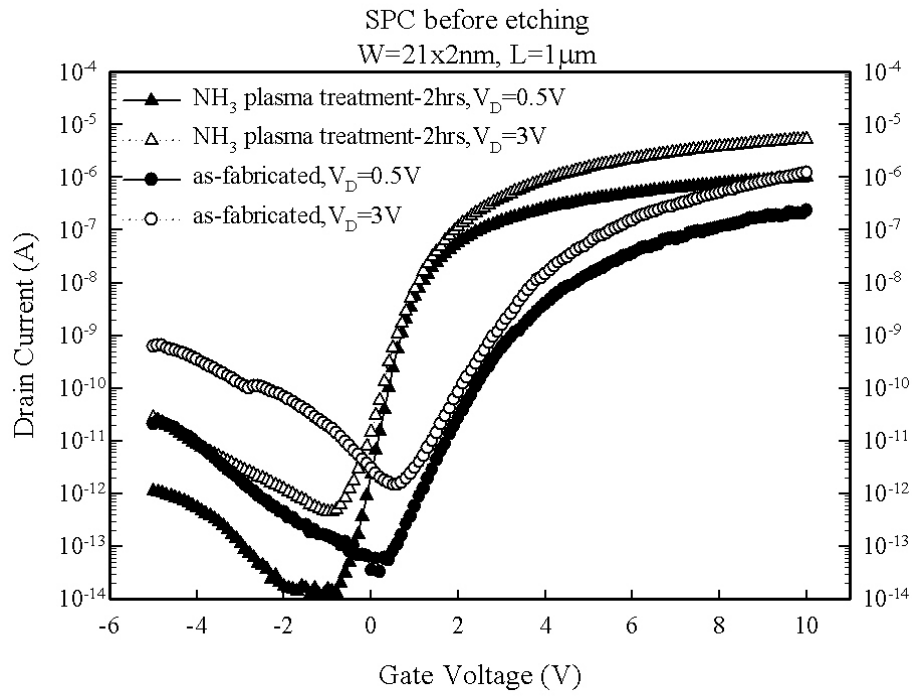


Figure 3-16 Transfer characteristics of as-fabricated device and device with 2-hour NH_3 plasma treatment at $V_D=0.5\text{V}$ and $V_D=3\text{V}$.

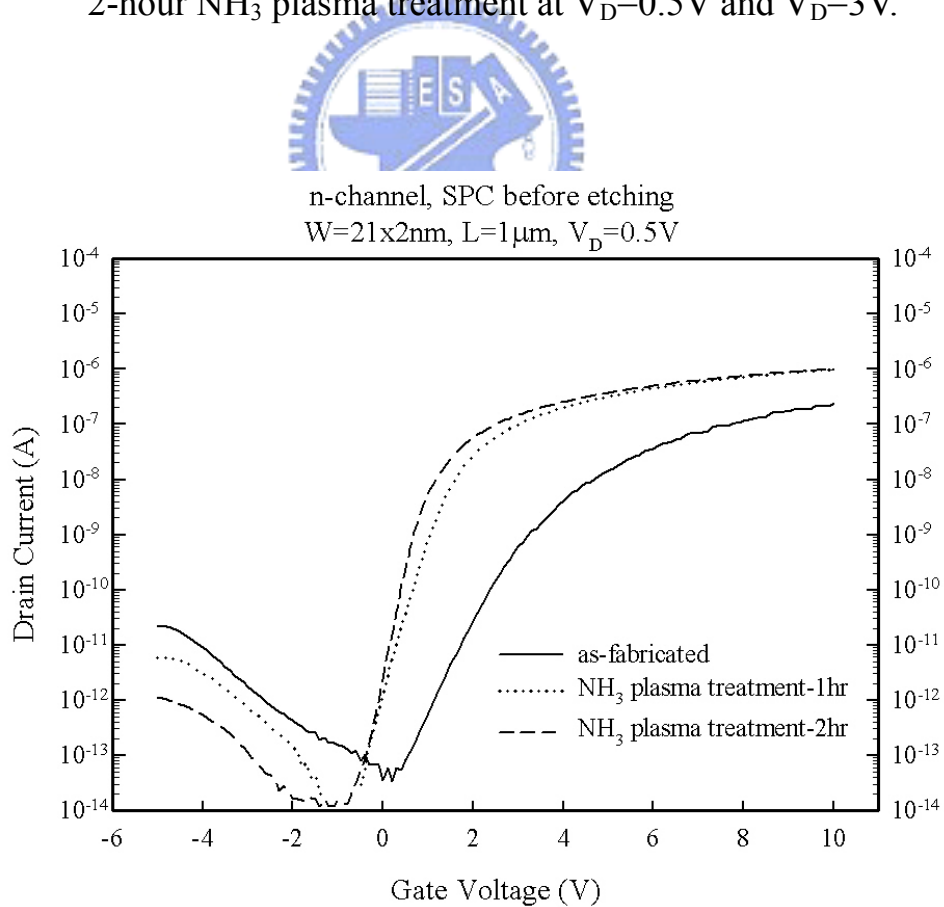


Figure 3-17 Subthreshold characteristics of as-fabricated device and devices that received 1- and 2-hour NH_3 plasma treatment at $V_D=0.5\text{V}$.

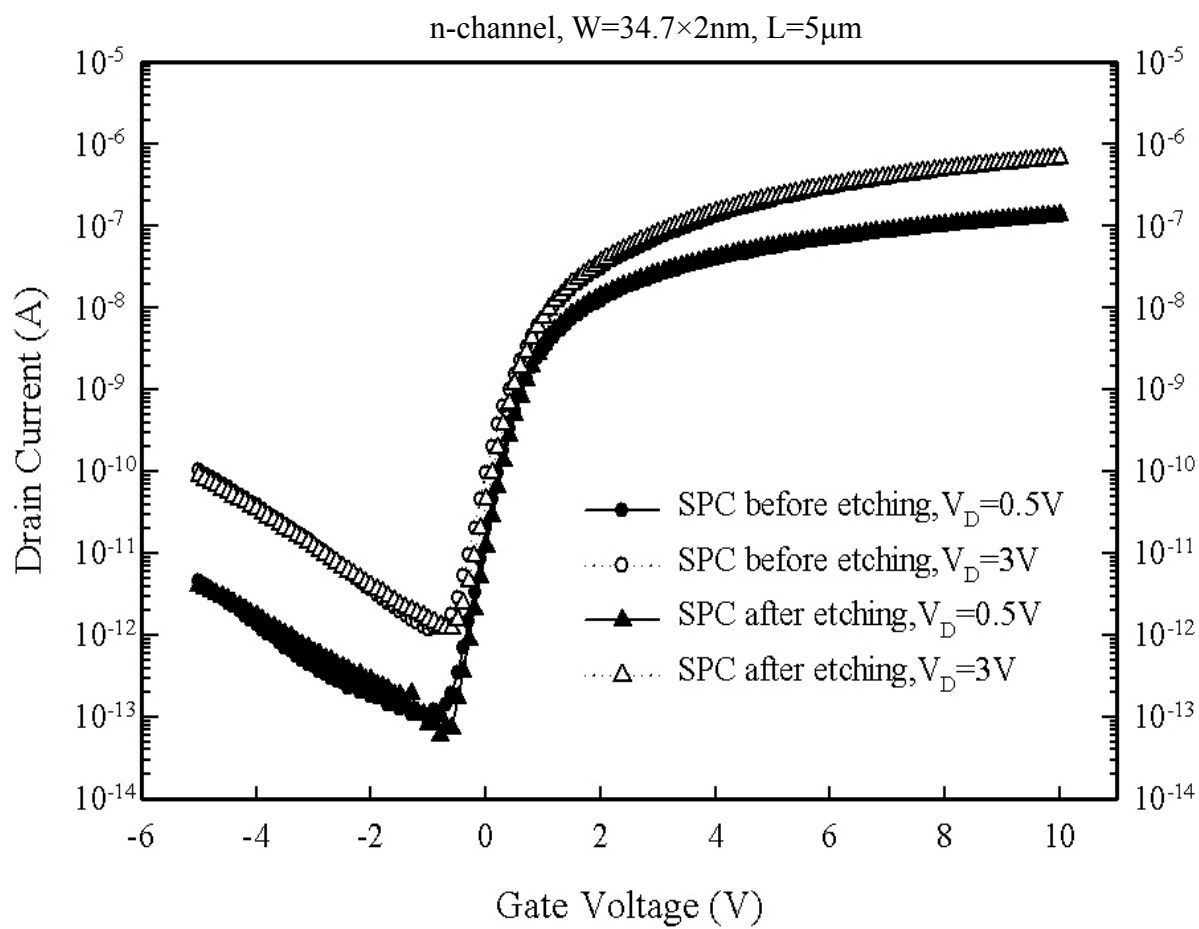


Figure 3-18 I_D - V_G characteristics of devices with SPC before and after etching and received NH_3 plasma treatment 1 hour.

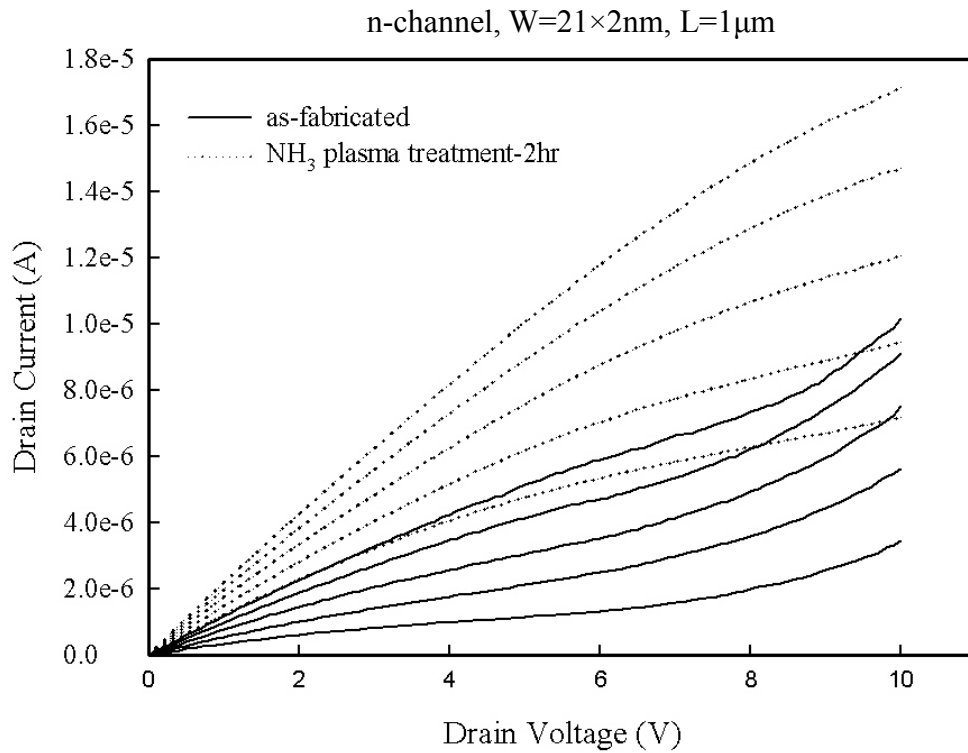


Figure 3-19 (a) I_D - V_D output characteristics of as-fabricated device and device with NH_3 plasma treatment for 2 hours. ($L = 1\mu\text{m}$)

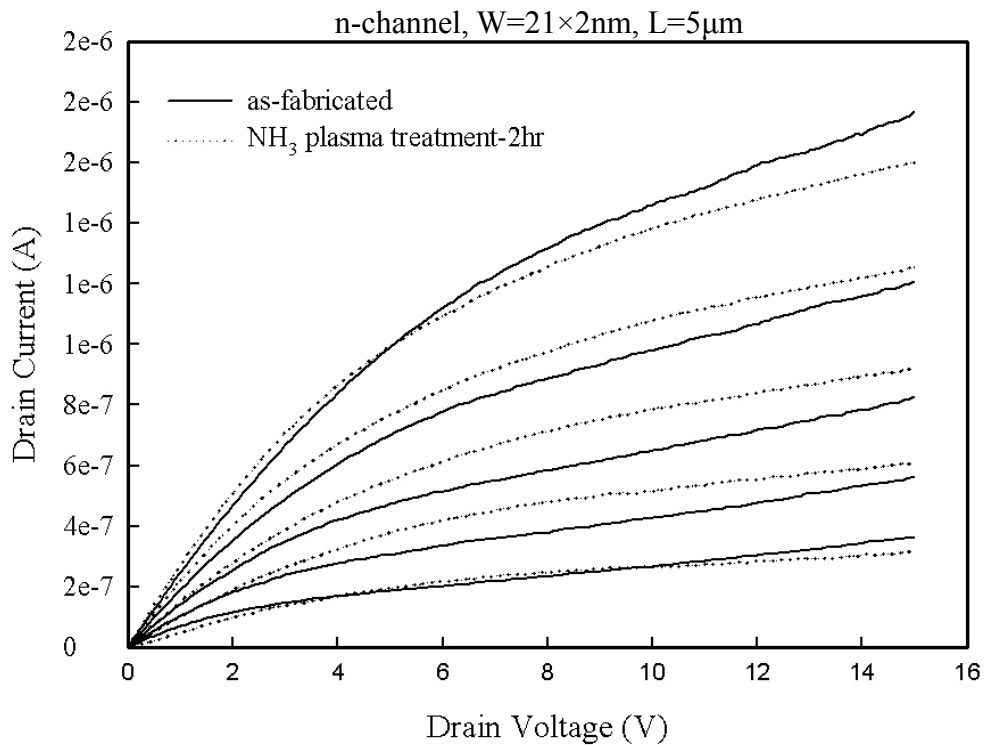


Figure 3-19 (b) I_D - V_D output characteristics of as-fabricated device and device with NH_3 plasma treatment for 2 hours. ($L = 5\mu\text{m}$)

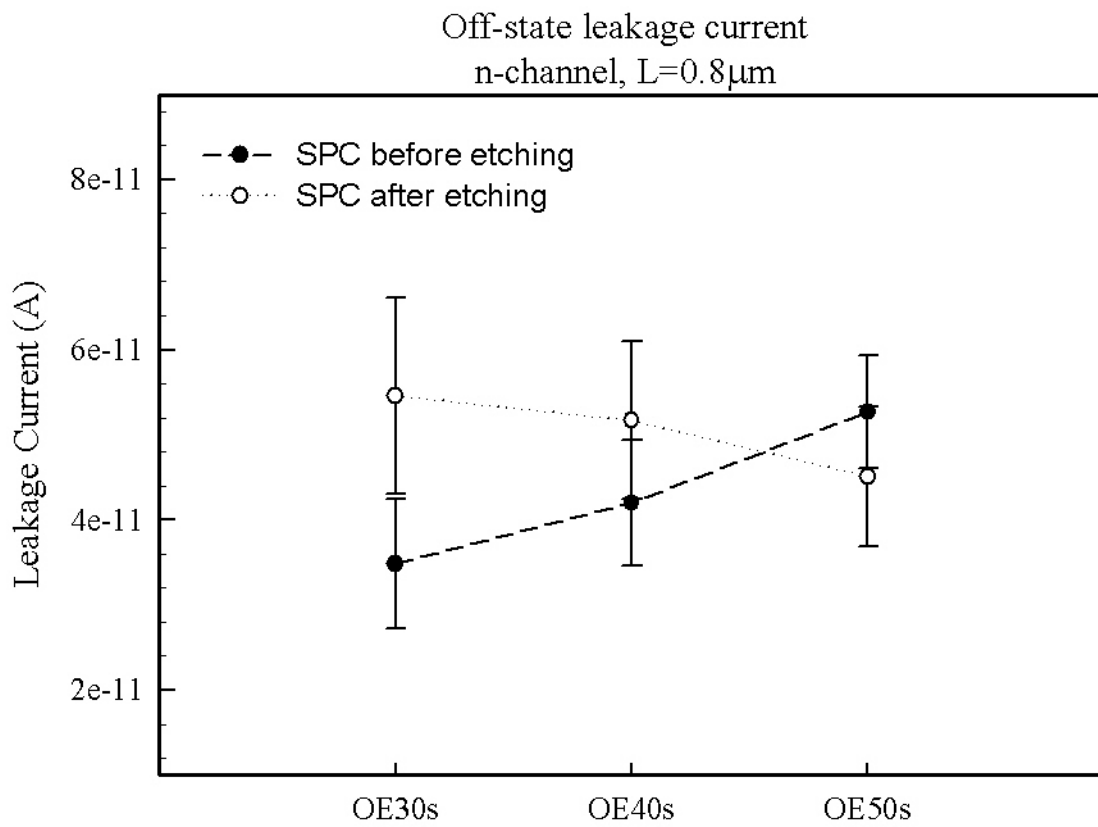


Figure 3-20 Leakage current as a function of overetch time for samples with SPC before and after channel etching.

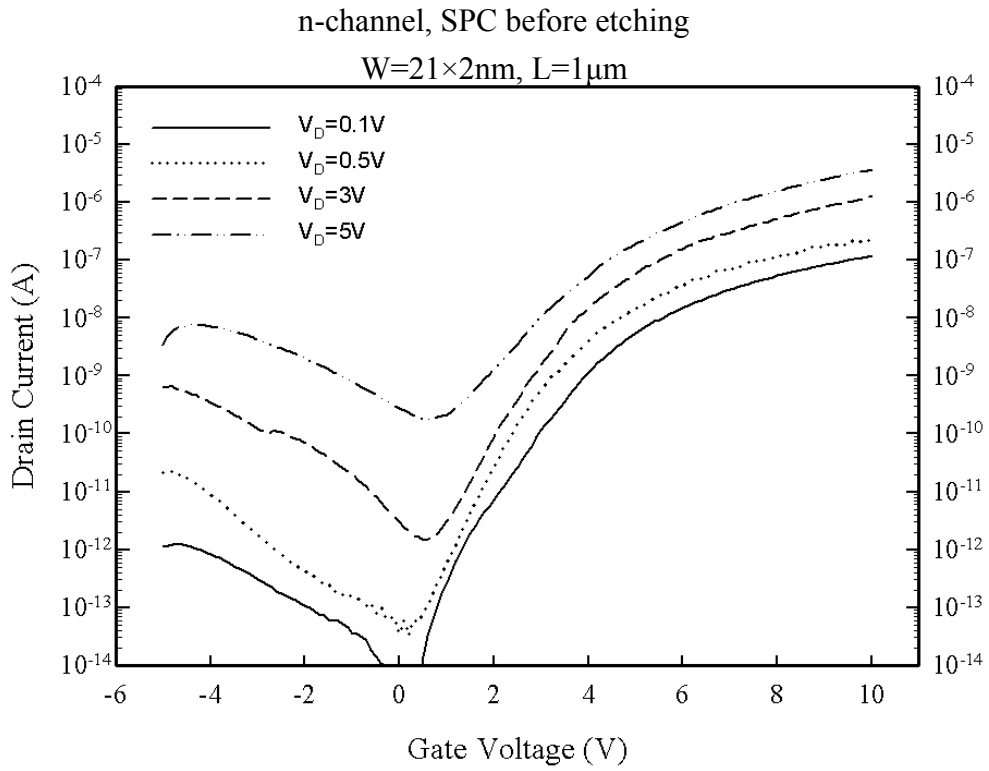


Figure 3-21 (a) I_D - V_G characteristics of the as-fabricated device with various V_D .

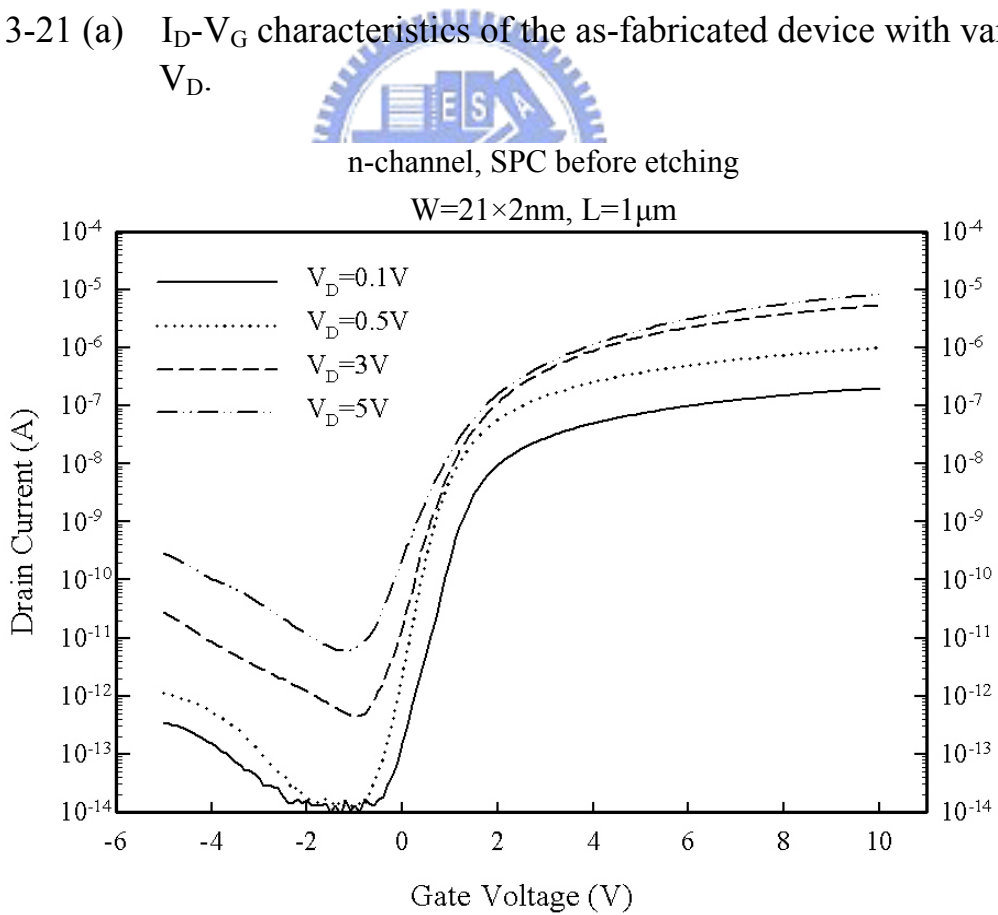


Figure 3-21(b) I_D - V_G characteristics of the device received 2-hour NH_3 plasma treatment with various V_D .

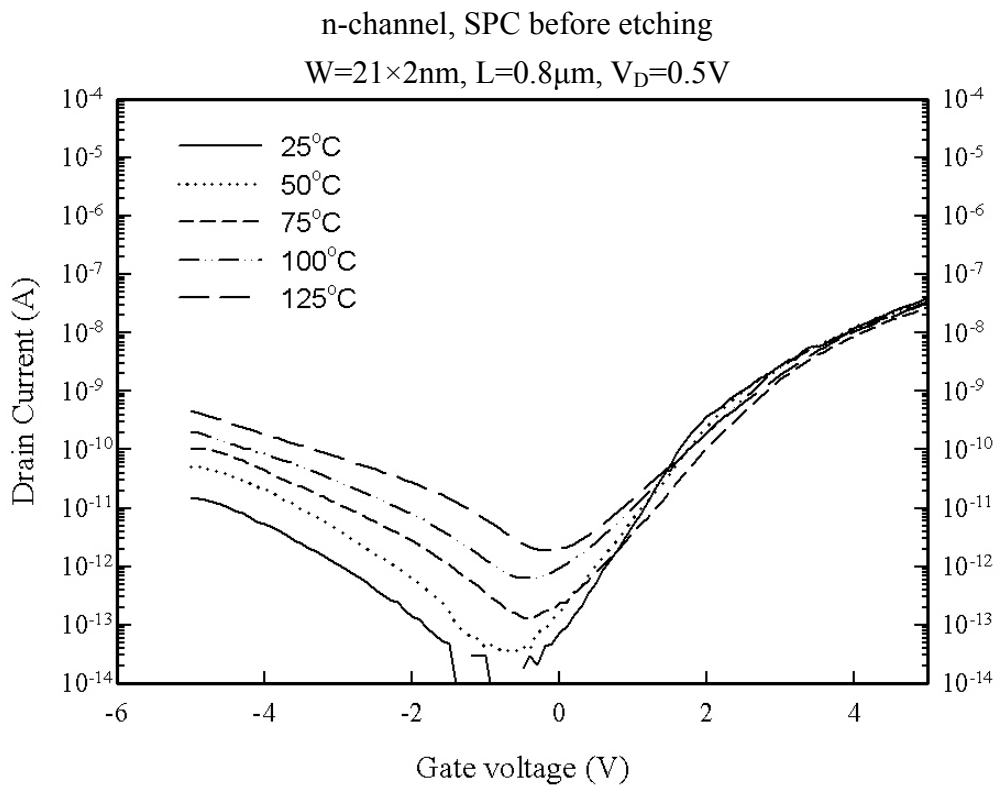


Figure 3-22 (a) Off-state leakage characteristics characterized at various temperatures.

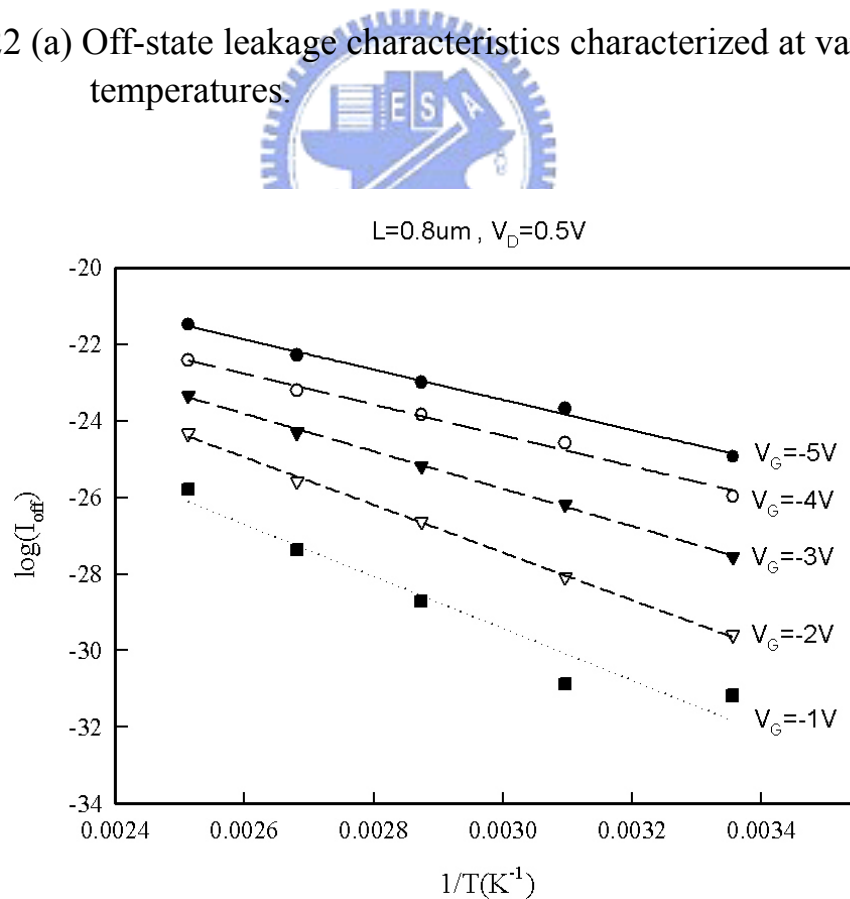


Figure 3-22 (b) Arrhenius plots of the off-state current of $0.8\mu\text{m}$ n-channel device at different gate voltages. The slope of each line determines the activation energy (E_a).

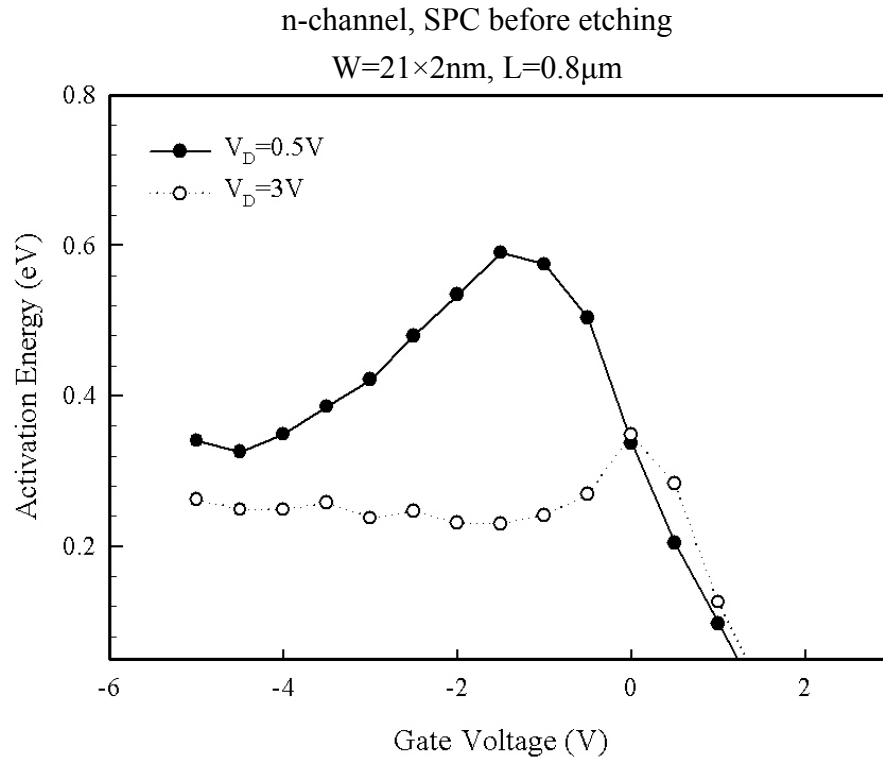


Figure 3-23 (a) Dependency of activation energy on gate and drain voltages for an as-fabricated device.

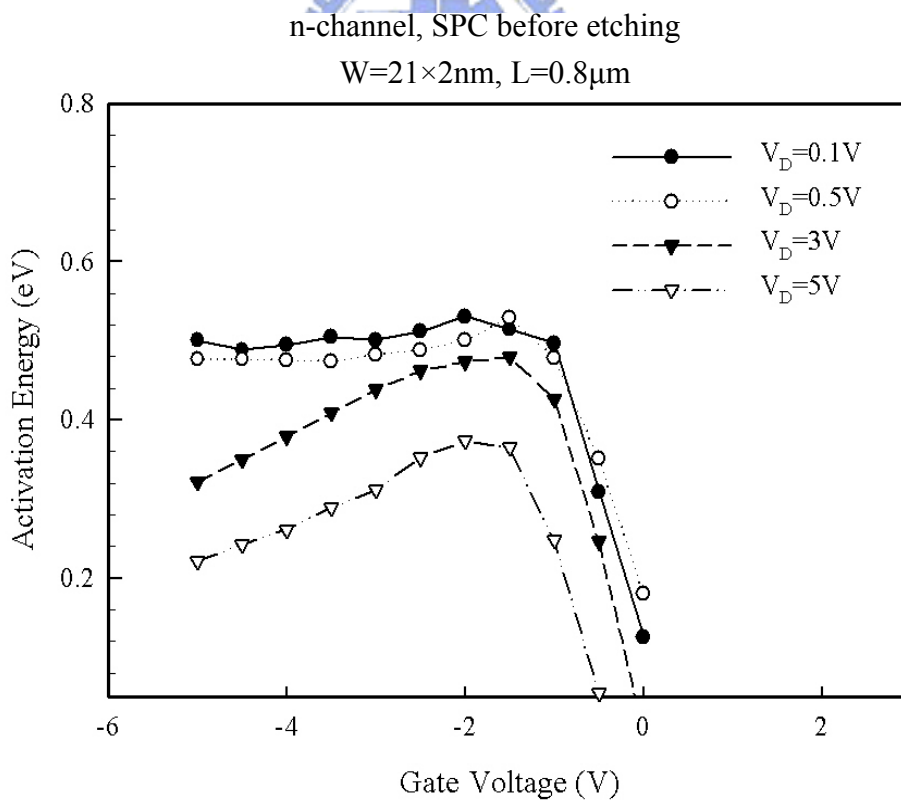
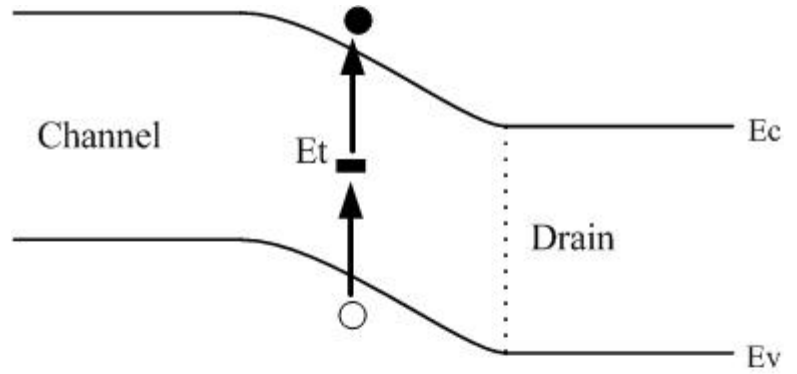
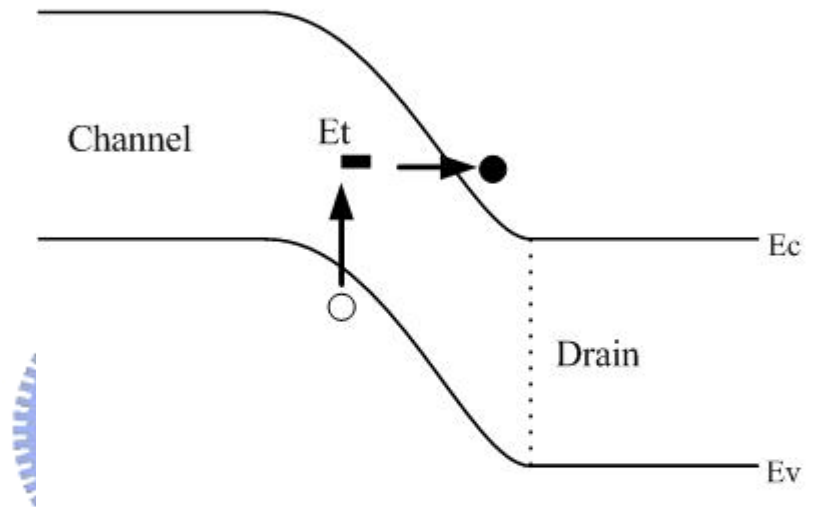


Figure 3-23 (b) Dependency of activation energy on gate and drain voltage for a device received 2-hour NH_3 plasma treatment.

(a) The case of weak electric field.



(b) The case of medium electric field.



(c) The case of strong electric field.

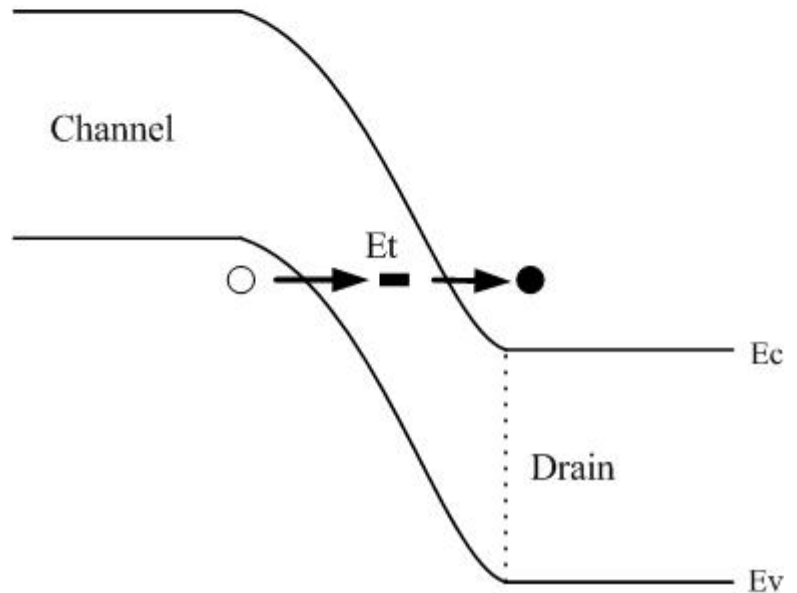


Figure 3-24 The band diagrams for mechanism 1.

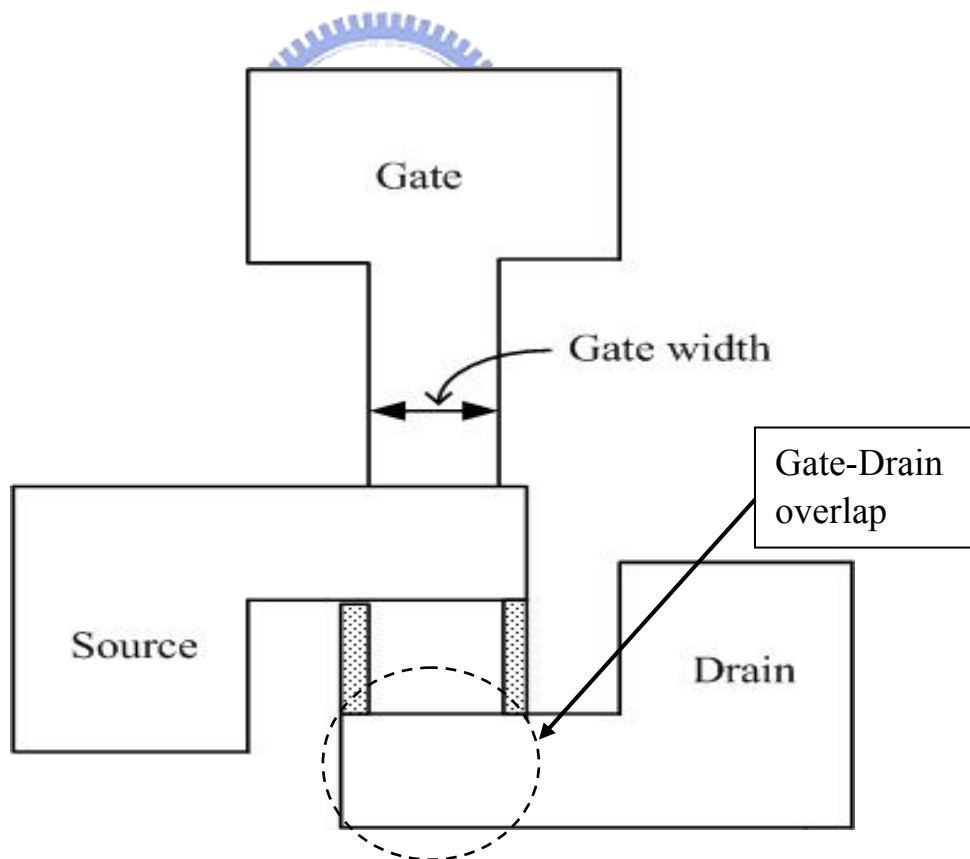
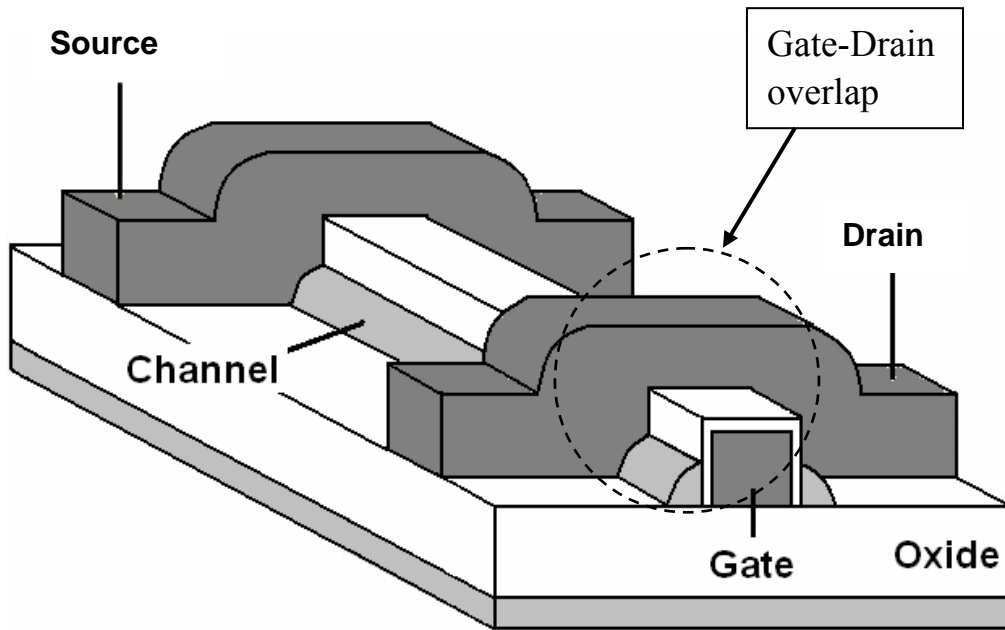


Figure 3-25 The gate-drain overlap region and the definition of gate width.

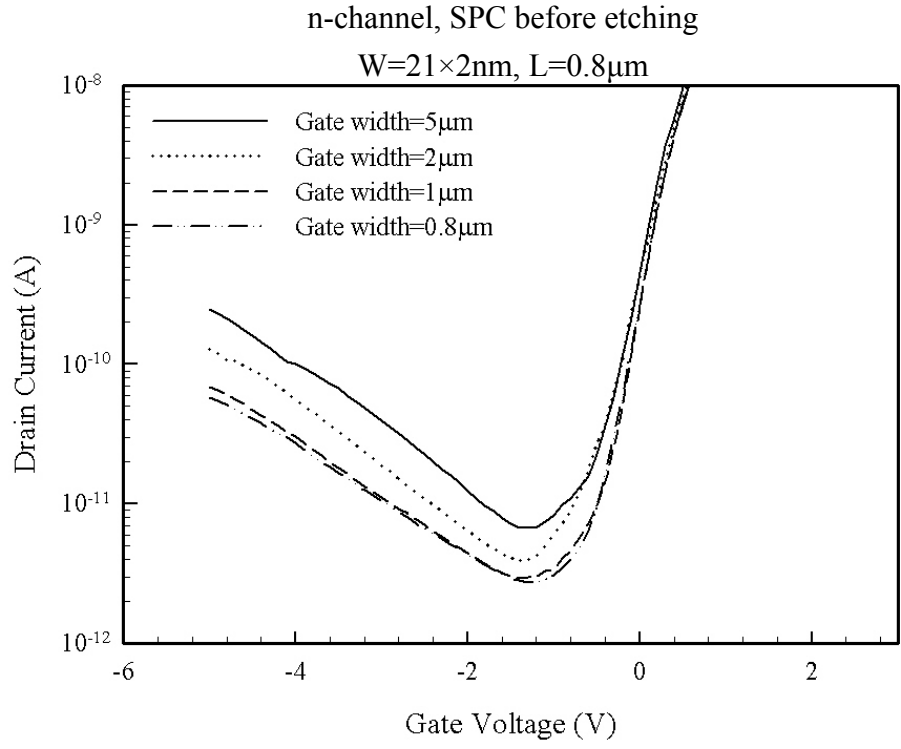


Figure 3-26 (a) The off-state current with various gate widths at $V_D=5V$.

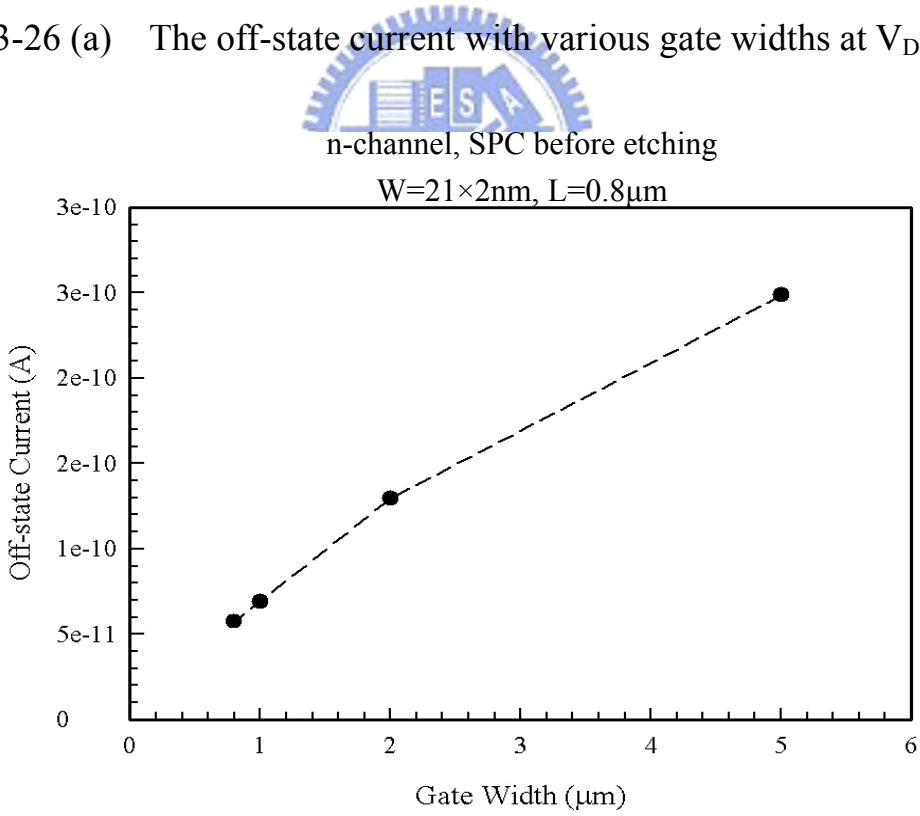


Figure 3-26 (b) Off-state current with various gate widths at $V_G=-5V$ and $V_D=5V$.

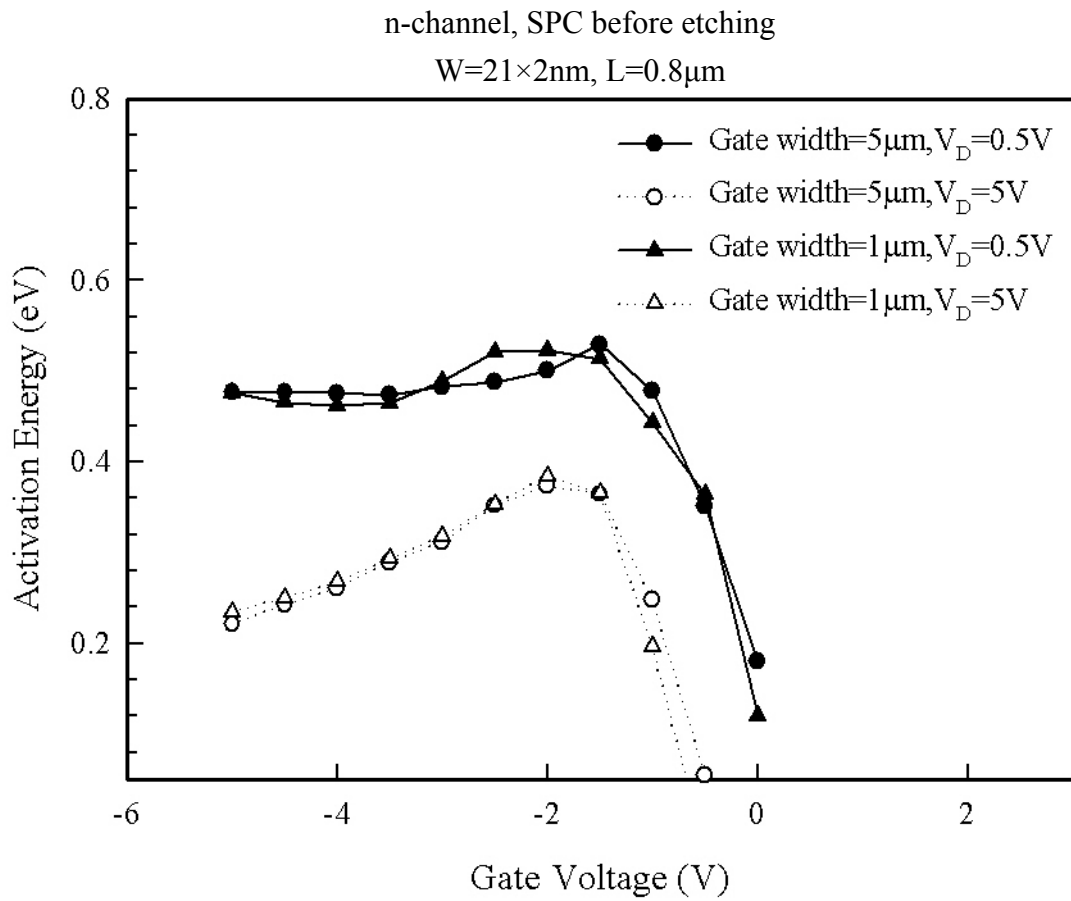
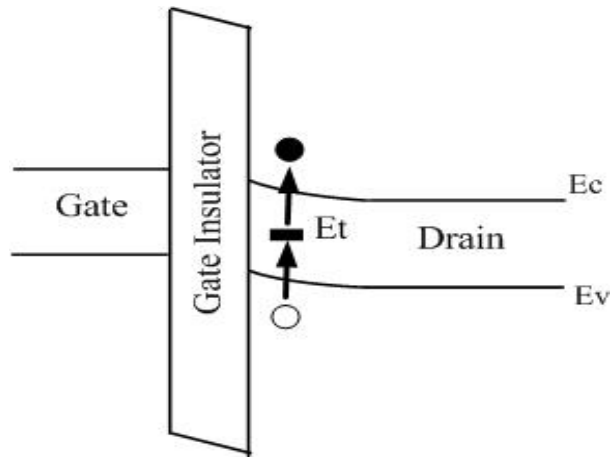
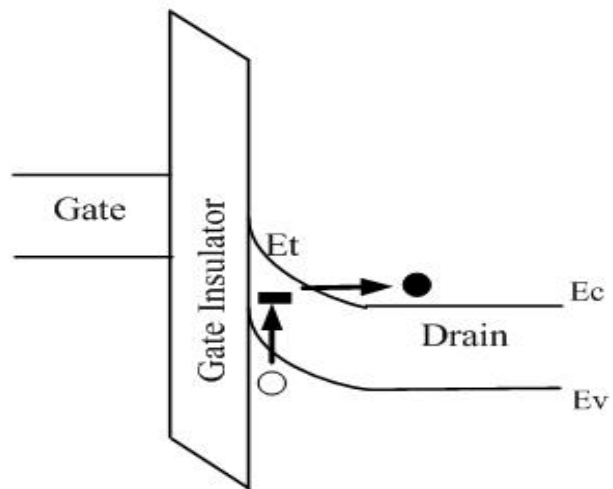


Figure 3-27 Dependency of activation energy on gate and drain voltages for a device received 2 hour NH₃ plasma treatment.

(a) Low electric field.



(b) Medium electric field.



(c) High electric field.

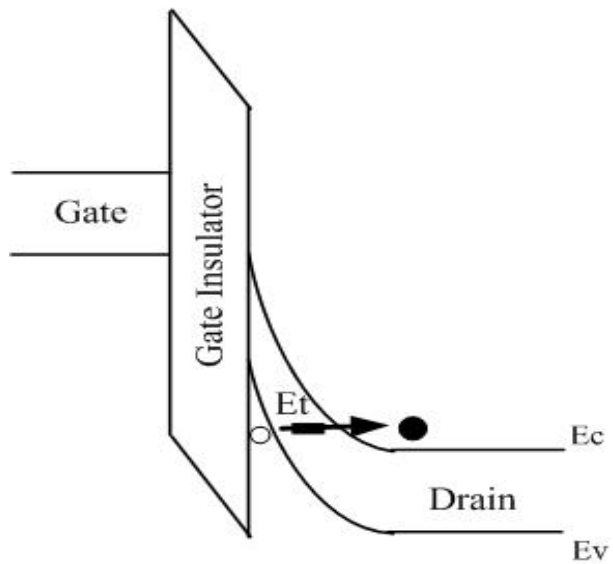


Figure 3-28 The band diagrams for mechanism 2.

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