Vertical n-Channel Poly-Si Thin-Film Transistors With Symmetric S/D Fabricated by Ni-Silicide-Induced Lateral-Crystallization Technology

Po-Yi Kuo, Tien-Sheng Chao, *Senior Member, IEEE*, Jiou-Teng Lai, and Tan-Fu Lei

***Abstract*—We have successfully developed and fabricated the vertical n-channel polycrystalline silicon thin-film transistors with symmetric S/D fabricated by Ni-silicide-induced lateral-crystallization technology (NSILC-VTFTs). The NSILC-VTFTs are S/D symmetric devices and equivalent to dual-gate devices. The dual-gate structure of NSILC-VTFTs can moderate the lateral electrical field in the drain depletion region, significantly reducing the leakage current. In NSILC-VTFTs, the Ni accumulation and grain boundaries induced from S/D sides can be centralized in the n^+ floating region. The effects of Ni accumulation in symmetric VTFTs crystallized by NSILC and metal-induced lateral crystallization are studied. In addition, a two-step lateral crystallization has been introduced to improve the crystal integrity through secondary crystallization. The NSILC-VTFTs crystallized by two-step lateral crystallization show a steep subthreshold swing of 180 mV/dec and field effect mobility $\mu = 553\ cm^2/V \cdot s$ without NH_3 plasma treatment.**

***Index Terms*—Dual gate, n^+ floating region, Ni-silicide-induced lateral crystallization (NSILC), polycrystalline silicon thin-film transistors (poly-Si TFTs), symmetric S/D, vertical channel.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) have the potential advantages of silicon-on-insulator MOSFETs. Recently, poly-Si TFT technology has been receiving more attention because it is a promising means of achieving 3-D integration, which has been utilized in various 3-D circuits [1]–[3].

It is believed that electrical characteristics of poly-Si TFTs can be improved if the poly-Si grain size can be enhanced and the number of grain boundaries in the channel can be reduced. Metal-induced lateral-crystallization (MILC) technology has been studied in the past to achieve large and regular poly-Si grain [4]–[6]. In addition, vertical thin-film transistors (VTFTs) are suitable for high-density 3-D integration, since their channel lengths are determined by the thicknesses of SiO_2 or poly-Si films instead of the photolithographic limitation. Many works had been devoted to developing and studying VTFTs [7], [8].

In this letter, we have successfully developed and fabricated the vertical n-channel poly-Si TFTs with symmetric S/D fabricated by Ni-silicide-induced lateral-crystallization technology (NSILC-VTFTs). The NSILC-VTFTs were fabricated by combining NSILC process and vertical channel. The NSILC-VTFTs are S/D symmetric devices and equivalent to dual-gate devices. The dual-gate structure is employed to eliminate the grain boundaries perpendicular to the current flow in the channel [9], [10]. Furthermore, a two-step lateral crystallization has been introduced to improve the crystal integrity through secondary crystallization, and device characteristics can be further improved [11]–[13].

II. Experiment

First, bare silicon covered with 5500-Å-thick SiO_2 was used as the glass substrate. An *in situ* n^+-doped 2500-Å-thick poly-Si thin film was deposited for gate by low-pressure chemical vapor deposition (LPCVD). After gate patterning, a 1000-Å depth of oxide undercut was etched to form a gate offset region. A 500-Å-thick TEOS gate oxide thin film was deposited by LPCVD, and then, a 500-Å-thick a-Si was deposited by LPCVD to form S/D and channel active region. After the active region patterning, a 4000-Å low-temperature oxide was deposited by high-density plasma chemical vapor deposition (HDPCVD) at 350 °C. Next, Ni-seeding window mask pattern was formed in the contact hole region. A stacked 100-Å/100-Å TiN/Ni thin film was deposited on the contact hole of the devices. We used two methods to complete the channel poly-Si crystallization: MILC and NSILC. The MILC-VTFTs were fabricated without rapid thermal annealing (RTA) Ni-silicidation processes. In the NSILC-VTFTs, the Ni silicidation was achieved by RTA at 450 °C for 20 s, and then, the residue Ni was removed by $H_2SO_4 : H_2O_2$ solution before lateral crystallization. The key process difference between NSILC-VTFTs and MILC-VTFTs is shown in Fig. 1. Next, both devices were crystallized by one-step lateral crystallization at 500 °C for 12 h. Furthermore, the NSILC-VTFTs (RTA) were

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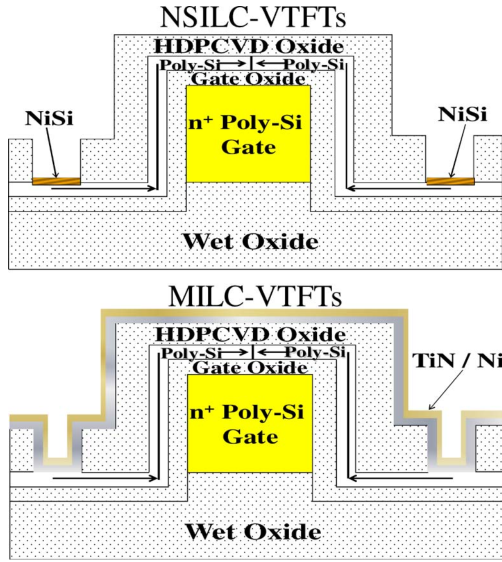

Fig. 1. Key process difference between NSILC-VTFTs and MILC-VTFTs. Compared with MILC processes, the NSILC processes provided a limited Ni source in Ni-silicided seeding window arranged on source and drain contact holes.

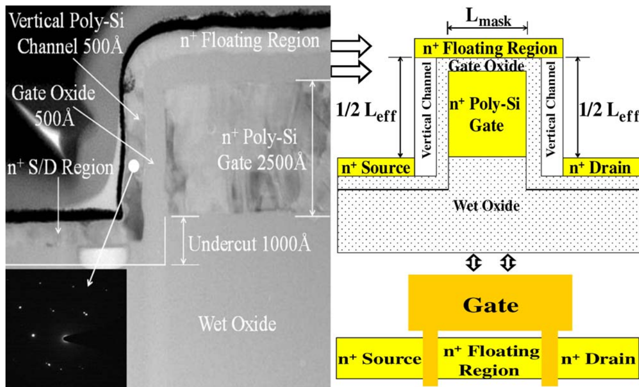

Fig. 2. Cross-sectional TEM microphotograph and the schematic cross-sectional structure of NSILC-VTFTs. The effective channel length (L_{eff}) of VTFTs with symmetric S/D is defined by 2 × total thickness of poly-Si gate and gate oxide. The length of n^+ floating region is defined by mask channel length (L_{mask}), and the mask channel width (W_{mask}) is equal to effective channel width.

crystallized by two-step lateral crystallization: first step lateral crystallization (500 °C for 12 h) and second step RTA (700 °C for 60 s). The channel active region of conventional TFTs was crystallized by solid-phase crystallization at 600 °C for 24 h.

After removing the low-temperature HDPCVD oxide, a 100-Å pad-oxide was deposited and 15-keV 5×10^{15}-cm^{-2} As^+ ion implantations were performed vertically to form self-aligned n^+ S/D and n^+ floating region [8]. Dopants were activated by RTA at 600 °C for 60 s for short-channel VTFTs. After passivation, contact, and metallization processes, all the devices were fabricated without NH_3 plasma treatment for studying influences of grain boundaries and Ni accumulation in the vertical channel and n^+ floating region.

III. Results and Discussion

Fig. 2 shows the cross-sectional transmission electron microscope (TEM) microphotograph and the schematic cross-sectional structure of NSILC-VTFTs. The depth of undercut is designed by the total thickness of gate oxide and channel for the purpose of n^+ S/D top edge and poly-Si gate bottom edge in the same horizontal level. The integrity of the vertical poly-Si channel is verified by the transmission electron diffraction (TED) pattern inserted in TEM microphotograph. The dots in TED pattern confirm that good crystallization is achieved. In Fig. 2, the equivalent dual-gate structure can moderate the lateral electrical field in the drain depletion region, significantly reducing the leakage current and increasing the $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio [9], [14].

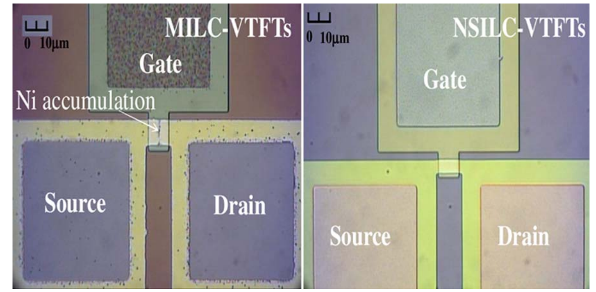

Fig. 3. Plan view optical microscope microphotographs of MILC-VTFTs and NSILC-VTFTs after one-step lateral crystallization.

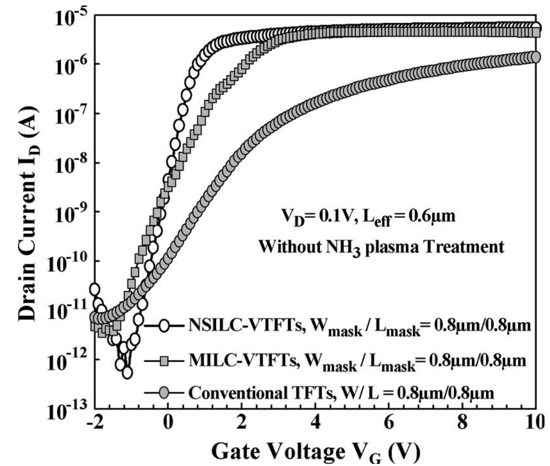

Fig. 4. Transfer characteristics of NSILC-VTFTs, MILC-VTFTs, and conventional TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 0.8$ μm/0.8 μm. The L_{eff} of VTFTs is 0.6 μm.

Fig. 3 shows the plan view optical microscope microphotographs of MILC-VTFTs and NSILC- VTFTs after one-step lateral crystallization. The excess Ni accumulation of the n^+ floating region is found in the MILC-VTFTs, but it is not found in the NSILC-VTFTs. Compared with MILC-VTFTs, the NSILC-VTFTs can eliminate metal contaminations due to the limited Ni source from Ni-silicided seeding window arranged on source and drain contact holes.

In narrow W_{mask}, there is a higher probability that only one of those grains will grow and occupy the entire channel region [15], [16]. Fig. 4 shows the transfer characteristics of NSILC-VTFTs, MILC-VTFTs, and conventional TFTs with $W_{\mathrm{mask}}/L_{\mathrm{mask}} = 0.8$ μm/0.8 μm. The NSILC-VTFTs have smaller subthreshold swing (S.S.) and larger $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio compared with MILC-VTFTs and conventional TFTs. It is believed that improved electrical characteristics of

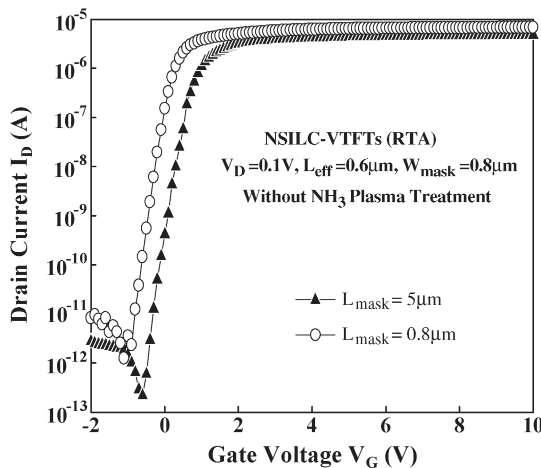

Fig. 5. Transfer characteristics of NSILC-VTFTs (RTA) with $W_{\rm mask} = 0.8\ \mu$m and different $L_{\rm mask}$. The $L_{\rm eff}$ is 0.6 μm.

NSILC-VTFTs are due to larger poly-Si grain size and less number of grain boundaries in the channel compared with conventional TFTs. In the VTFTs, the OFF-state leakage current can be reduced by the self-aligned gate offset without additional masking step [8]. The poor electrical characteristics of MILC-VTFTs are due to the excess Ni accumulation in the n^+ floating region, and this phenomenon can be eliminated in NSILC-VTFTs.

Fig. 5 shows the transfer characteristics of NSILC-VTFTs (RTA) with $W_{\rm mask} = 0.8\ \mu$m and different $L_{\rm mask}$. The NSILC-VTFTs (RTA) have steeper S.S. and larger field effect mobility compared with NSILC-VTFTs. Secondary grain crystallization by the second step RTA is the process responsible for the crystal integrity improvement [11]–[13]. The NSILC-VTFTs (RTA) with $L_{\rm mask} = 0.8\ \mu$m have the smallest $S.S. = 180$ mV/dec and maximum field effect mobility $\mu = 553\ {\rm cm}^2/{\rm V}\cdot{\rm s}$. Moreover, the NSILC-VTFTs (RTA) with $L_{\rm mask} = 5\ \mu$m have the largest $I_{\rm on}/I_{\rm off}$ current ratio ($\sim$2.2 $\times$ 10^7). The NSILC-VTFTs (RTA) with appropriate $L_{\rm mask}$ can moderate the OFF-state peak lateral electrical field in the drain depletion region, significantly reducing the OFF-state leakage and increasing the $I_{\rm on}/I_{\rm off}$ current ratio [9], [14]. The lower ON-state current of NSILC-VTFTs (RTA) with $L_{\rm mask} = 5\ \mu$m is due to the larger series resistance in the n^+ floating region.

IV. Conclusion

The vertical n-channel poly-Si TFTs with symmetric S/D fabricated by NSILC technology have been proposed to fabricate the high-performance TFTs. The metal contaminations can be reduced by NSILC processes, resulting in improved poly-Si TFT characteristics. Two-step lateral crystallization has been introduced to improve the crystal integrity through secondary recrystallization. The OFF-state leakage of the NSILC-VTFTs can be improved by increasing appropriate $L_{\rm mask}$ and depth of undercut without additional masking steps.

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