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碩士論文

高介電常數材料之低溫複晶矽快閃記憶體的研究

Low Temperature Polycrystalline Silicon Thin-Film Flash Memory with High-k Material

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摘　　要

在本論文中，我們提出在低溫複晶矽薄膜上製作非揮發性快閃記憶體。首先，改變不同高介電常數材料當作記憶體元件的電荷補陷層(Trapping layer)，在此我們所使用的高介電常數材料分別是二氧化鉿(HfO_2)、鉿矽酸鹽(Hf-silicate)以及鋯矽酸鹽(Zr-silicate)，對快閃記憶體元件做特性及可靠度分析，我們可以發現我們所製作的低溫複晶矽薄膜快閃記憶體具有以下幾個特點：(1)三種不同的電荷補陷層製作出的記憶體元件，都具有記憶視窗大的特性；(2)在資料寫入/抹除(Program/Erase)的速度表現上，三種材料的記憶體元件都可以達到毫秒級以上的資料寫入/抹除速度；(3)在資料保存能力(Data retention)上的表現，三種材料的記憶體元件在室溫量測下，推測十年後的電荷保存能力都可以維持在 70%以上，鉿矽酸鹽的記憶體元件甚至可以達到保存 90%以上的電荷；(4)在元件耐久度(endurance)測試下，三種材料的記憶體元件經過資料反覆寫入/抹除十萬次，記憶視窗的大小都維持的很好，沒有因為反覆寫入/抹除而造成記憶視窗關閉的情形；(5)記憶體具有單一元件二位元(2bits/cell)操作特性。

本篇論文另外探討改變不同穿隧氧化層(Tunneling oxide)厚度對元件特性的影響，其中穿隧氧化層較厚的在資料保存能力上有較好的特性，然而兩種不同厚度的穿隧氧化

層在資料寫入/抹除速度上分別不大，但是在抗閘極干擾(Gate disturbance)及抗汲極干擾(Drain disturbance)特性上，對低溫複晶矽薄膜快閃記憶體仍然是一個問題。我們將製作好的元件利用氨電漿(NH_3 plasma)處理後，可以大幅改善元件在資料保存能力、抗閘極干擾及抗汲極干擾的特性，不過氨電漿修補介面懸鍵及複晶矽通道中的載子補獲態(Trap states)仍然有限，如果可以找到更好的方法排除介面懸鍵及複晶矽通道中的載子補獲態對元件造成的影響，未來低溫複晶矽快閃記憶體在應用上就能更有發展空間。

Low Temperature Polycrystalline Silicon Thin-Film Flash Memory with High-k Material

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ABSTRACT

In this thesis, we proposed the fabrication of low temperature polycrystallize silicon thin film with nonvolatile flash memory as named the SONOS-type poly-Si-TFT memories. In addition, the different high-k materials of trapping layer were used in this experiment, including the HfO_2, Hf-silicate and Zr-silicate. We also analyze the electrical properties and the reliability of the SONOS-type poly-Si-TFT memories. It was demonstrated that the fabricated memories exhibit good performance. First, the large memory window was shown in the device with three different trapping layers. Second, these samples would have the high program/erase speed (1ms/10ms). Third, all the three samples can be operated up to 10^8 s with only 30% charge loss for the data retention performance under room temperature operation. However, the data retention for the sample with Hf-silicate trapping layer can be operated up

to 10^8 s with only 10% charge loss. Fourth, our devices also have long retention time (>10^6s for 20% charge loss) and negligible read/write disturbances. Fifth, the 2-bit operation has been successfully demonstrated in these devices with different trapping layers.

We also discuss the electrical characteristics of SONOS-type poly-Si-TFT memories with different tunneling oxide thickness. The device with thicker tunneling oxide thickness would have better data retention performance than the sample with thinner tunneling oxide thickness. In addition, our device with thicker tunneling oxide thickness would have good program/erase speed as well as the device with thinner tunneling oxide thickness. However the gate and drain disturbance are still problems in low temperature poly-crystallize silicon thin film flash memories. After NH_3 plasma treatment, the performances of data retention and disturbance would be improved for our SONOS-type poly-Si-TFT memories. This is because the hydrogen atoms of NH_3 can terminate dangling bonds and replace the weak bonds in the grain boundaries and SiO_2/poly-Si interface and thus reduce the trap states in the poly-Si channel. Thus, both the performance and reliability of poly-Si TFTs were also improved. As long as the drain and gate disturbance can be reduced, this TFT flash memories are very promising for the future flash memory application.

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Chapter1

Introduction

1-1 General Background

Polycrystalline silicon thin-film transistors (Poly-Si TFT) have been widely used to integrate driver circuits for the application of AMLCD's [1]-[4]. With progressive manufacturing technologies, the complexity of circuit integration will continue to increase. Currently, the feasibility of integrating an entire system on top of the panel (SOP) is being actively pursued [5]. Since a system shall include the functionality of memory, efforts shall be paid in order to successfully integrate the memories, such as SRAM and flash memory, on the panel [6]. SONOS-type nonvolatile memory based on discrete storage nodes possesses great potential for achieving large memory windows, high program/erase speed, low programming voltage, low-power performance, excellent retention and good disturb characteristics [7]. In this thesis, we used three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate for the trapping layer of the poly-Si TFT memory. By employing low thermal cycle (600℃, 24hrs) for post high-k deposition annealing, the proposed nonvolatile memory fabrication is fully compatible with the conventional TFT processing.

1-2 Thesis Organization

This thesis is divided into five chapters. In Chapter 2, show the TFT flash memory fabrication and experimental measurement. The experimental measurement include program operation, erase operation, and all kinds of disturb. In Chapter 3, we demonstrated a nonvolatile memory on low temperature polycrystalline silicon thin-film, and show the electrical characteristics of TFT flash memory. In Chapter 4, we will discuss the electrical characteristics with different tunneling oxide thickness and improvement of NH_3 plasma treatment. In the last Chapter, the conclusions of this thesis will be given.

Chapter 2

The TFT flash memory fabrication and experimental measurement

2-1 Device fabrication

The schematic diagram of the fabrication process is illustrated in Fig. 2.1. First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to substitute for the glass substrate and all the experimental devices in this study were fabricated on thermally-oxidized Si wafers. Then, a 100-nm-thick amorphous-silicon layer was deposited on thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 hours in N_2 ambient for the phase transformation. Individual active regions were then patterned and defined. After a standard RCA cleaning, two kinds of tunneling oxide thickness was deposited, one is 90-nm-thick TEOS oxide, the other is 200-nm-thick TEOS oxide. The followed by the depositions of three different kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate thin films by co-sputtering method. A blocking oxide of about 33nm was then deposited by PECVD at 350°C. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-3} and 40keV, respectively. After

S/D formation, which was activated at 600°C for 24-hr, passivation, metallization and NH_3 plasma sintering were performed to complete the fabrication of the poly-Si TFT memories.

2-2 Program and erase mechanisms

In this thesis, the programming scheme is executed by using channel hot electron injection (CHEI) to move charge into the trapping layer, thus threshold voltage can be changed. Figure 2-2 shows the hot electron injection scheme in an n-channel TFT flash memory. The hot electrons are “hot” because they are heated to a high-energy state by the high field near the drain. Some of them with energy higher than the barrier height of SiO_2/Si conduction band, so they can surmount the barrier and are injected into the trapping layer. The erasing scheme is executed by using band to band hot hole injection to combine negative charge in the trapping layer.

2-3 The disturbance

The first failure phenomenon, “program disturbance,” often takes place under the electrical stress applied to those neighboring un-programmed cells during programming a specific cell in the array. Two types of program disturbances, gate (word-line) disturbance and drain (bit-line) disturbance need be considered. In Fig. 2-3, shows the schematic circuitry of the memory array. During programming cell A, gate disturbance occurs in the cell B and same for those cells connected with the same word-line because the gate stress is applied to the

same word-line (WL). This is called gate disturbance. During programming cell A, drain disturbance occurs in the cell C and same for those cells connected with the same bit-line because the drain stress is applied to the same bit-line (BL). This is call drain disturbance. For the cell reading, the unwanted electron injection would happen while the word-line voltage and bit-line voltage are under read operation. This phenomenon would result in a significant threshold voltage shift of our selected reading cell. This is call read disturbance.

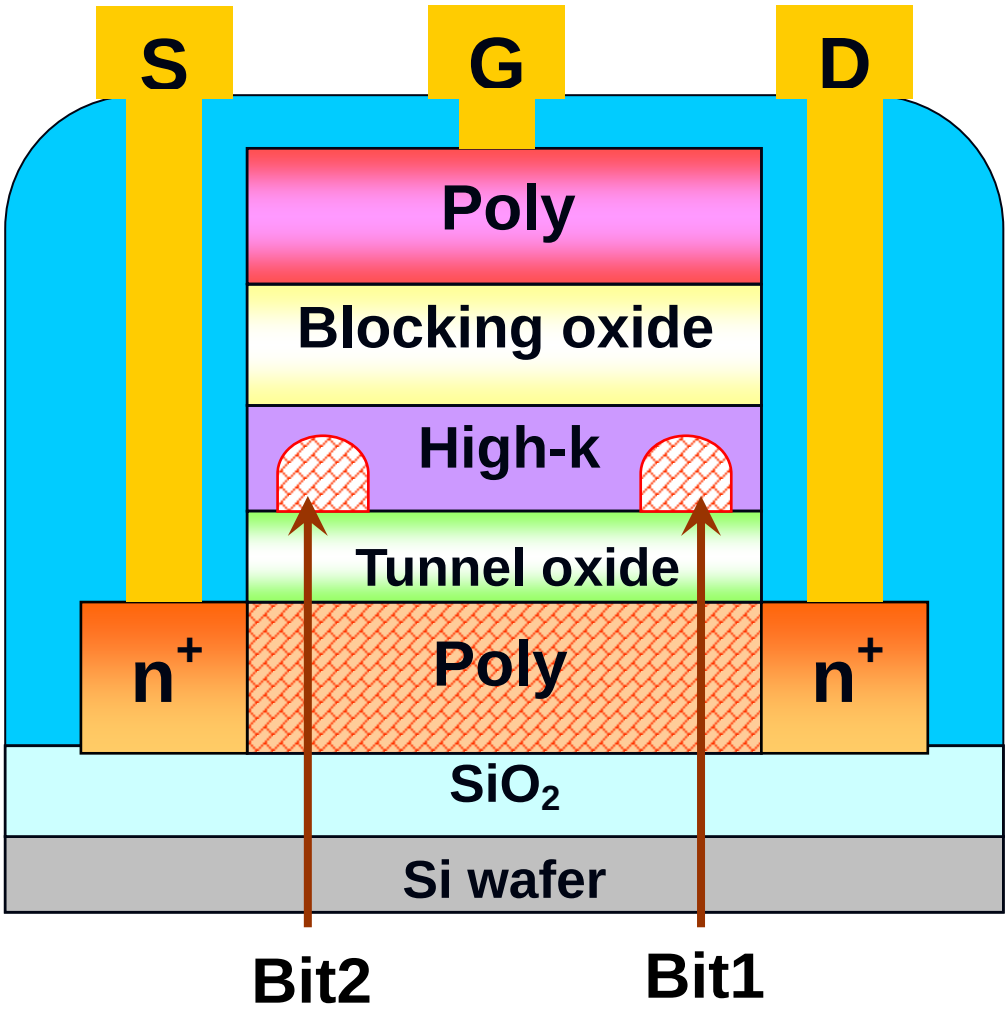

Fig. 2-1 Schematic cross section of the TFT flash memory.

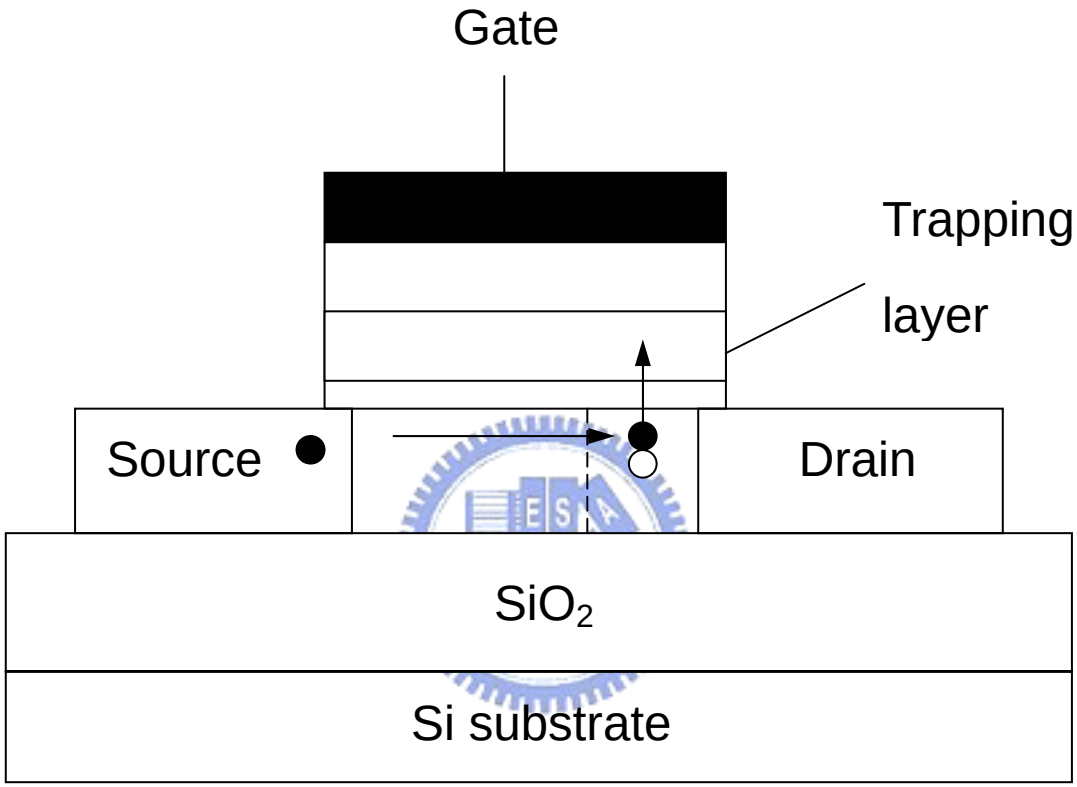

Fig. 2-2 Illustration of hot electron injection in a TFT memory.

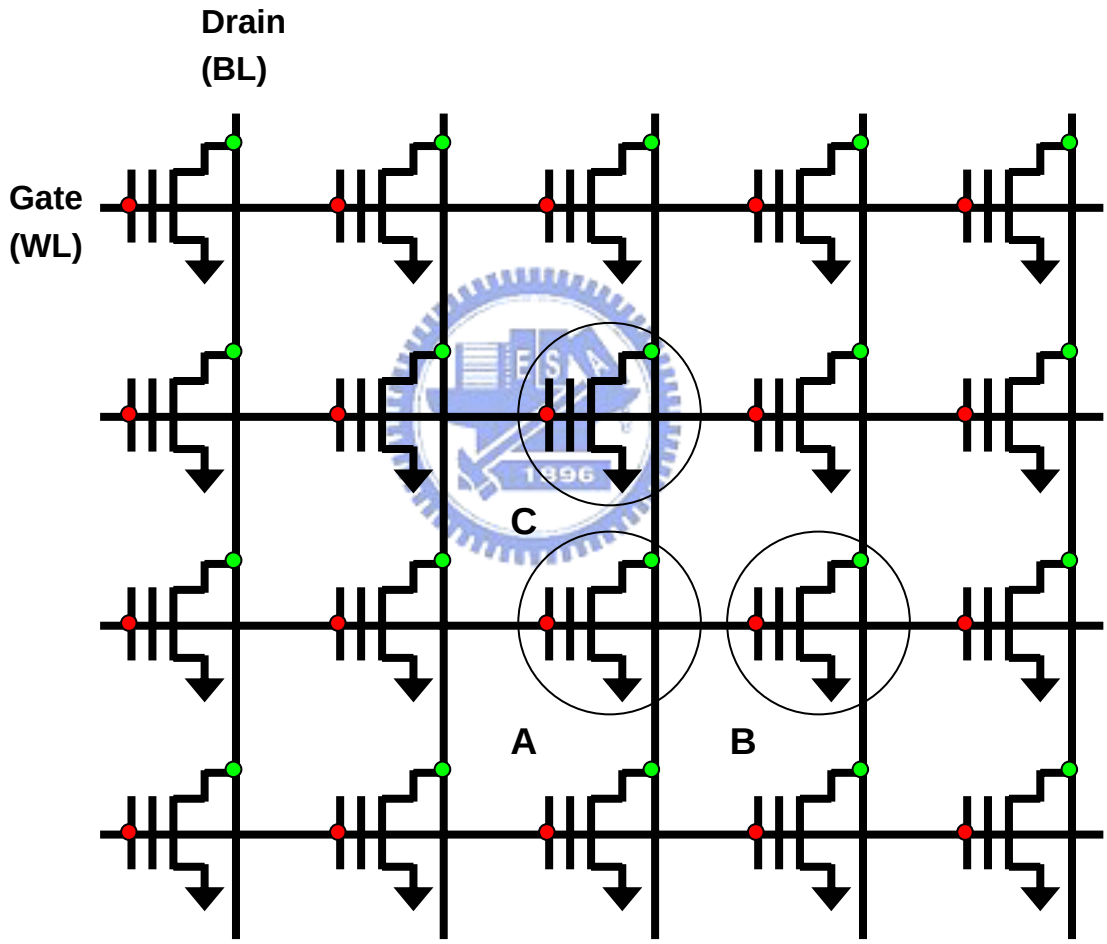

Fig. 2-3 The schematic illustration of disturb condition. Cell A is the programming cell. Cell B and Cell C are the gate disturb and drain disturb, respectively.

Chapter 3

The electrical characteristics of TFT flash memory

3-1 TFT Flash Memory Characteristics

Fig. 3-1 shows the cross-sectional HRTEM images of the gate stacks of poly-Si TFT memories. For all samples, the thicknesses of the tunnel oxide and blocking oxide layer are 9nm and 33nm, respectively. The trapping layer thicknesses are 9.8nm, 20.1nm and 13.9nm for the memories with HfO_2, Hf silicate, and Zr silicate, respectively. Fig. 3-2 illustrates the corresponding diffraction patterns taken from the three high-k dielectric trapping layers. It is found that HfO_2 and Hf silicate samples depict less degree of crystallization than Zr silicate after 600°C, 24hrs dopant activation.

Fig. 3-3 (a)-(c) show the Ids-Vgs curves of the poly-Si TFT memories with HfO_2, Hf-silicate and Zr-silicate trapping layers under fresh, programmed and erased states. Channel hot-electron injection and band-to-band hot-hole injection were employed for programming and erasing, respectively, and the programming/erasing times are 1s. It is clearly observed that the memory windows are quite large. For Vg=Vd=12V, a memory window larger than 5V can be easily achieved for Hf-silicate and Zr-silicate memories. Program/erase characteristics of the poly-Si TFT memories with HfO_2, Hf-silicate and Zr-silicate trapping layers are shown in Figs 3-4 (a)-(c), respectively. We can see that the program time can be as short as 1ms for a window close to 1V with the operation condition of Vg=Vd=10V, and the erase time is about 1ms with Vg=-10V and Vd=10V for all cases. Data retention is an important reliability issue of TFT flash memory devices. Figs.3-5 (a)-(c) show the retention behavior of TFT flash memory device with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) in programmed state, at room temperature (25℃) and high temperature (85℃), respectively. The charge loss behavior under the high temperature condition is accelerated

seriously than that under the room temperature condition. Their charge loss may be resulted from possible detrapping processes. This detrapping process means that the trapped electrons near the oxide-trapping layer interface would escape into the substrate or the gate due to the trap-assisted tunneling[8]. Meanwhile, the endurance characteristics after 10^5 P/E cycles for the memories with HfO_2, Hf- silicate and Zr-silicate trapping layers are shown in Figs 3-6 (a)-(c). The programming and erasing conditions are Vg=Vd=12V for 1ms and Vg=-10V, Vd=10V for 10ms for both samples, respectively. Despite the occurrence of significant memory window narrowing, a memory window of about 2V is sustained even after 10^5 P/E cycles. The origin of the narrowing over cycling, mainly coming from the increase of Vt in erased state, might be due to two factors: The first is the mismatch between the localized spatial distributions for injected electrons and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electrons will then cause the Vt to increase gradually over P/E cycling. The other is the stress-induced electron traps generated in the tunnel oxide during cycling. Therefore, in pursuing superior performance in charge storage capability of these new TFT memories, nano-dots formation [9], if feasible, and higher quality tunnel oxide are highly recommended. The cycling retention was an important issue for the TFT flash memory device. Therefore, we studied the retention loss behavior of TFT flash memory device with Hf-silicate trapping layer before and after 10k cycling. Fig.3-7 and 3-8 show the cycling retention behavior of TFT flash memory device with different tunneling oxide thickness (20 nm & 9 nm) in programmed state, at room temperature (25℃) and high temperature (85℃), respectively. As we can see in Fig.3-7, the charge loss behavior of the sample with 10k cycling is accelerated seriously than the sample without 10k cycling under the room temperature condition. Besides, the samples with thinner tunneling oxide have shown the same tendency in cycling retention performance under the room temperature condition as illustrated in Fig.3-8. However, the sample with thicker tunneling oxide (20 nm) shown the better cycling retention performance than the sample with

thinner tunneling oxide (9 nm) as shown in both Fig.3-7 and 3-8. The threshold voltage of the TFT flash memory device with 20 nm tunneling oxide has only shown 20 % shift as indicated in Fig.3-7. Fig. 3-9 demonstrates the feasibility of 2-bit operation with a reverse read scheme in a single cell for our poly-Si TFT memories. From the Ids-Vgs curves, we can employ forward/reverse reads for detecting the information stored in programmed bit1/bit2, respectively. Table1 is the scheme of the bias conditions for the 2-bits/cell memory operation.

3-2 Disturb Characteristics

The first failure phenomenon, program disturbance, often takes place under the electrical stress applied to those neighboring un-programmed cells during programming a specific cell in the array. Two types of program disturbances, gate (word-line) disturbance and drain/source (bit-line) disturbance need to be considered. Fig. 2-3 shows the schematic circuitry of the memory array. During programming cell A, gate disturbance occurs in the cell B and those connected with the same word-line because the gate stress is applied to the same word-line (WL). Fig. 3-10 (a)-(c) show the gate disturb characteristics. After 1000s at 25°C, small extent of gate disturbance was found. During programming cell A, drain disturbance occurs in the cell C and those connected with the same bit-line because the drain stress is applied to the same bit-line (BL). Fig. 3-11 (a)-(c) show the drain disturb characteristics. After constant Vd stress1000s at 25°C and 85°C, we can find high voltage and high temperature stress resulting in a more terrible drain disturbance than low voltage and temperature stress. This phenomenon is believed due to the presence of the localized traps along the grain boundaries in the channel, which can significantly affect the Vt shift through drain and gate bias stressing [10-11]. Therefore, to eliminate the traps along the grain boundaries in the channel is another key for achieving better performance. In addition, the read disturb characteristic is shown in Figs. 3-12 (a)-(c). For the cell reading, the unwanted electron injection would happen while the word-line voltage and bit-line voltage are under read operation. This phenomenon would result in a significant threshold voltage shift of our selected reading cell. However, the threshold voltage shift of the read disturbance was only 0.1V for all three samples after 1000s at 25°C as shown in Figs. 3-12 (a)-(c). This result means that the apparent read disturbance was not observed in our device. Because the gate voltage and drain voltage were different while the device was operated in program state and read state, respectively. The gate voltage and drain voltage for the reading operation are smaller than that in the program state. The gate voltage of the reading operation would not

induce in the serious grain boundaries trap and interface state trap. And so the read disturbance was not degraded as shown in Fig. 3-12 (a)-(c).

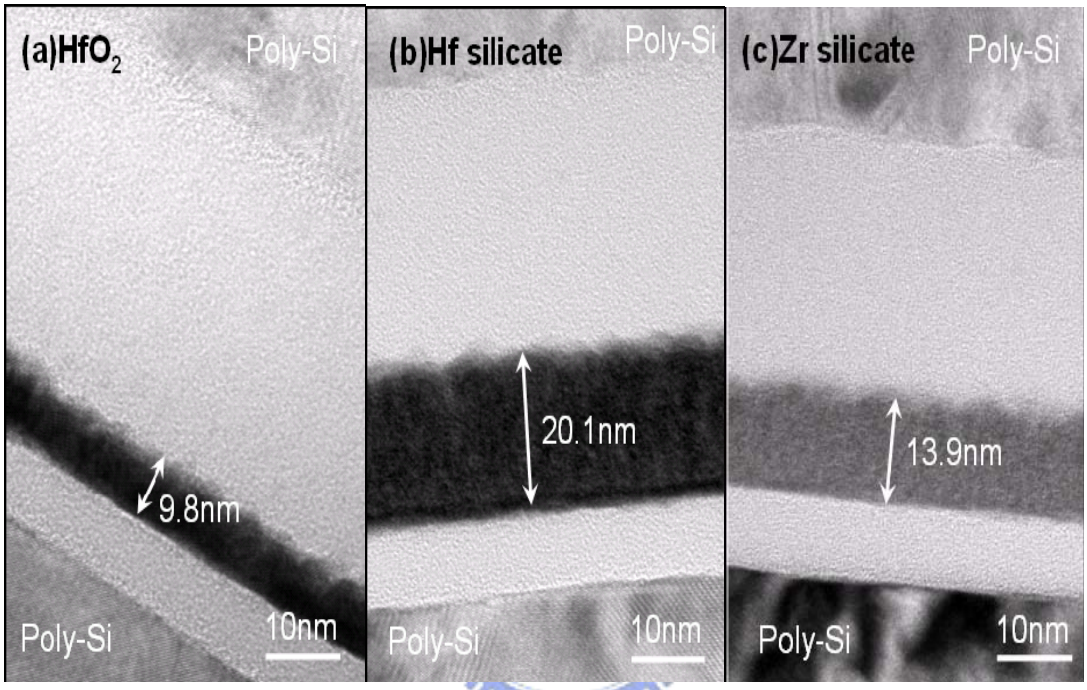

Fig. 3-1 Cross-sectional HRTEM images of the gate stacks for the poly-Si TFT memories with (a) HfO_2, (b) Hf silicate, and (c) Zr silicate trapping layers.

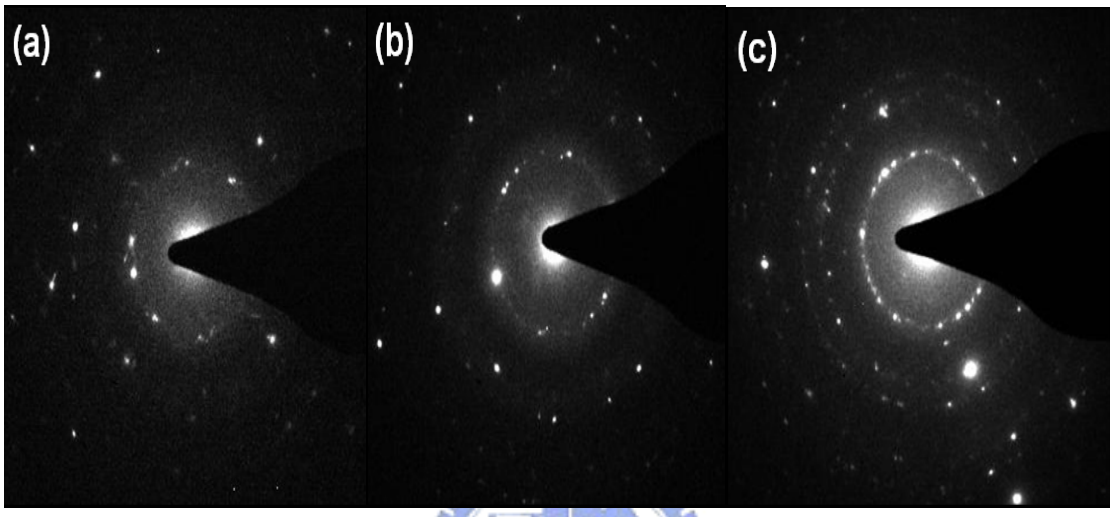

Fig. 3-2 Diffraction patterns of (a)HfO_2, (b)Hf silicate, and (c)Zr silicate trapping layers. HfO_2 and Hf silicate samples depict less degree of crystallization than Zr silicate.

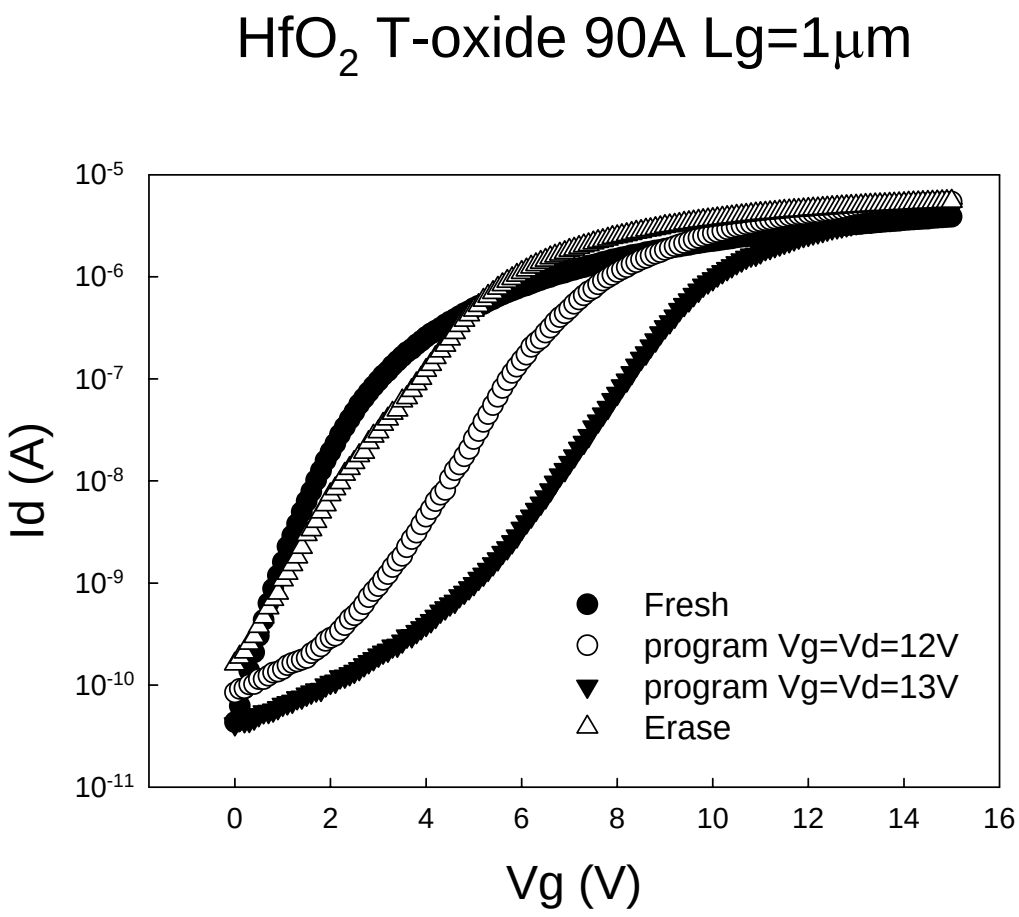

Fig. 3-3 (a) Ids-Vgs curves of the memory in the programmed/erased states for different programming conditions. The trapping layer is HfO_2. The programming and erasing times are 1s. A memory window of larger than 5V can be achieved with Vg= Vd=13V programming condition.

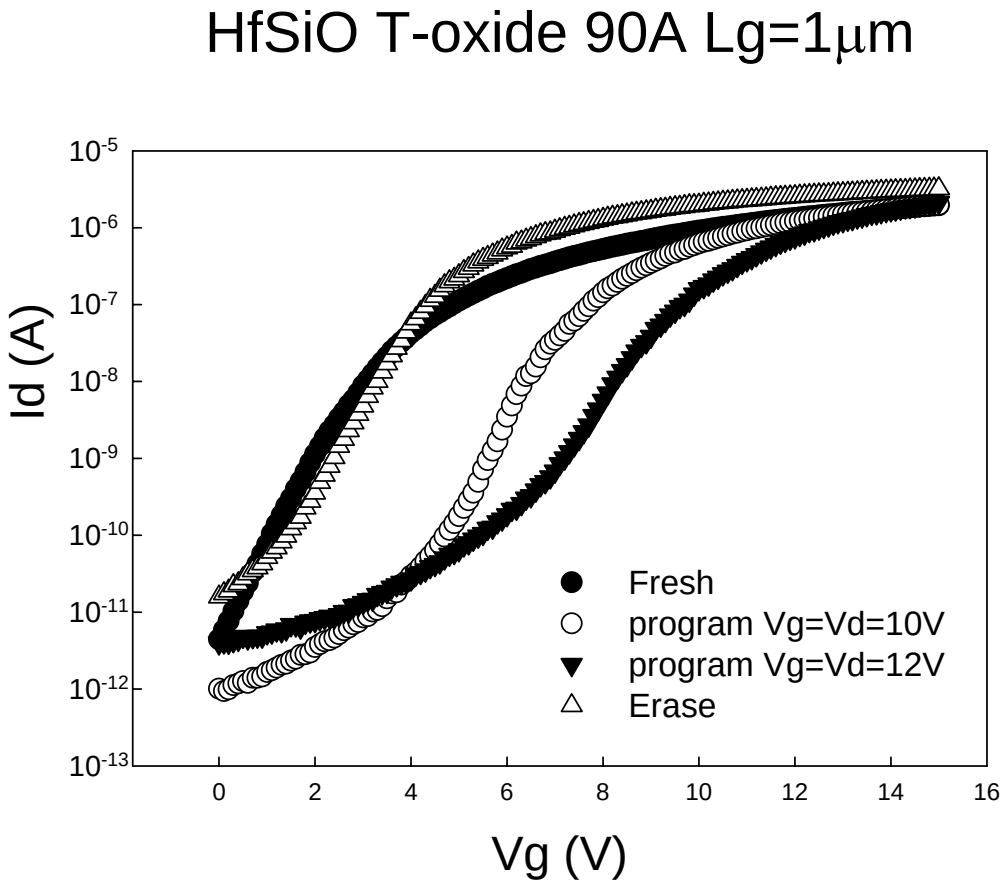

Fig. 3-3 (b) Ids-Vgs curves of the memory in the programmed/erased states for different programming conditions. The trapping layer is Hf-silicate. The programming and erasing times are 1s. A memory window of larger than 5V can be achieved with Vg= Vd=12V programming condition.

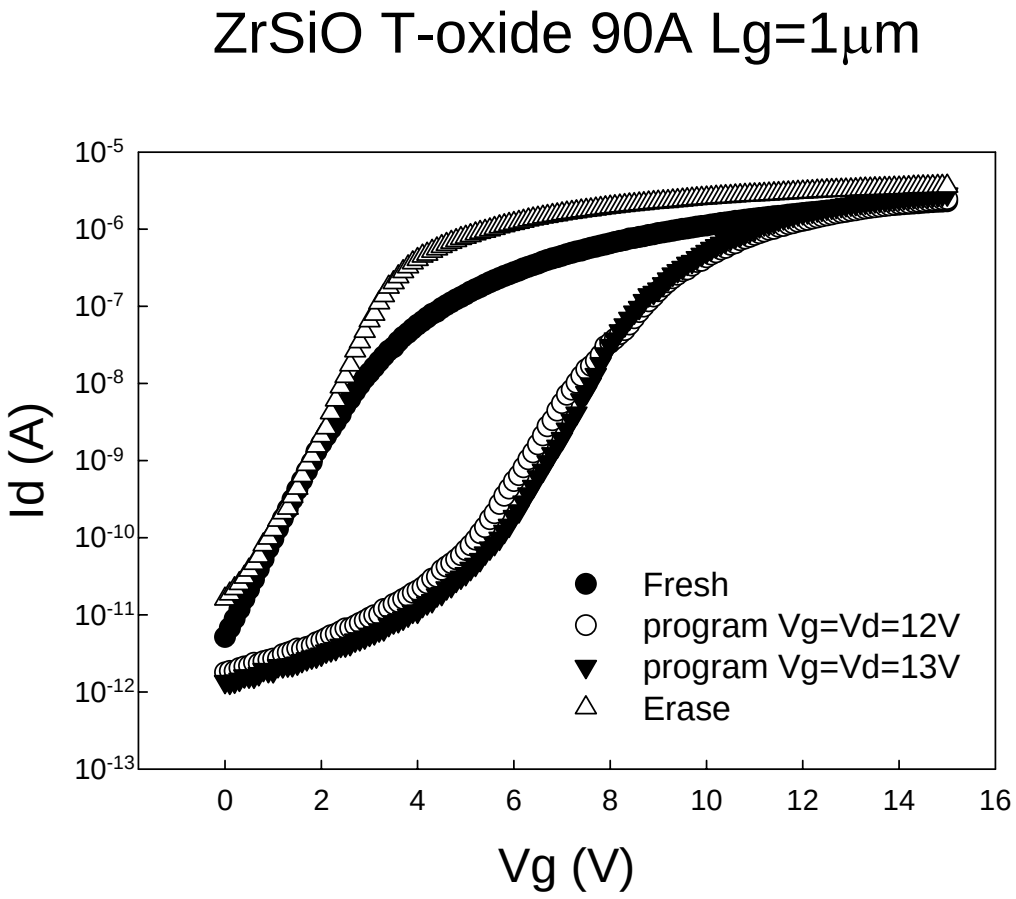

Fig. 3-3 (c) Ids-Vgs curves of the memory in the programmed/erased states for different programming conditions. The trapping layer is Zr-silicate. The programming and erasing times are 1s. A memory window of larger than 5V can be achieved with Vg= Vd=13V programming condition.

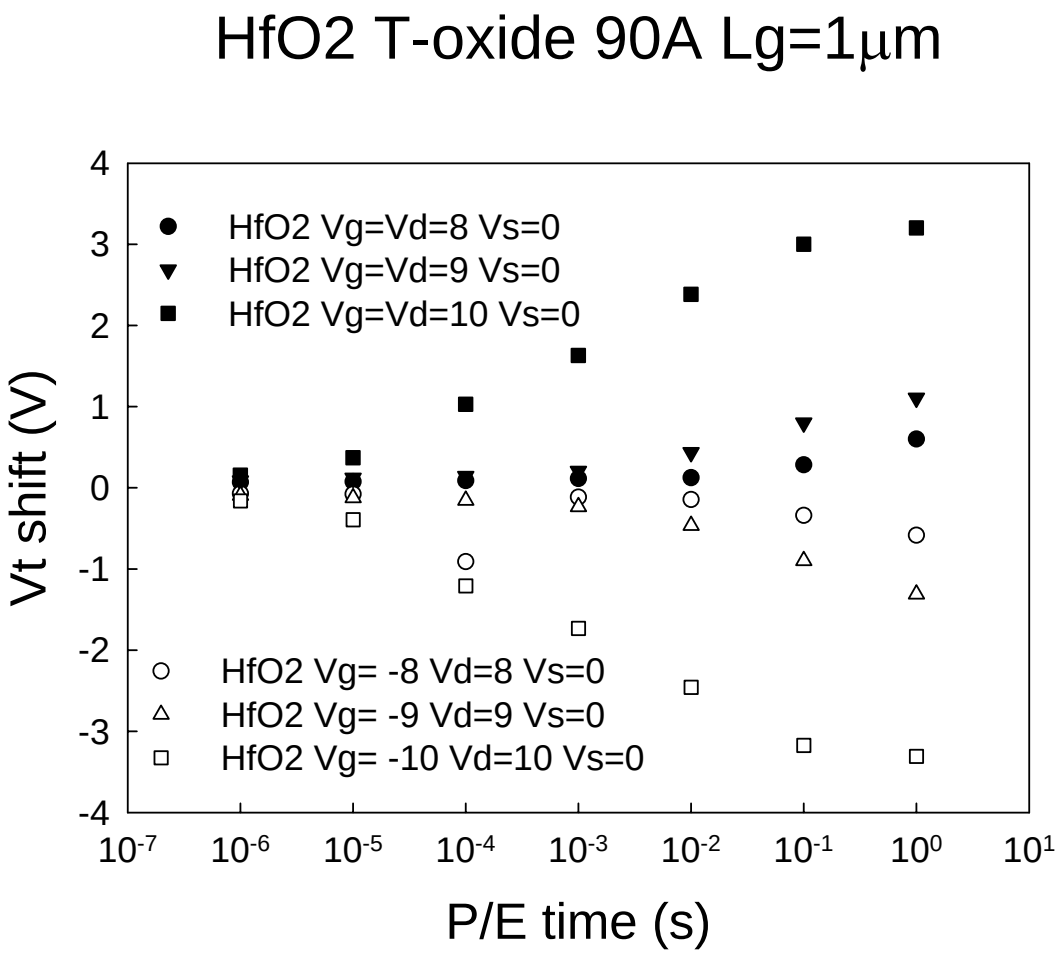

Fig. 3-4 (a) Program and erase characteristics of poly-Si TFT memory with HfO_2 trapping layer for different programming conditions. The programming time can be as short as 0.1ms if the window margin is set to 1V with Vg=Vd=10V. The erasing time is about 0.1 ms

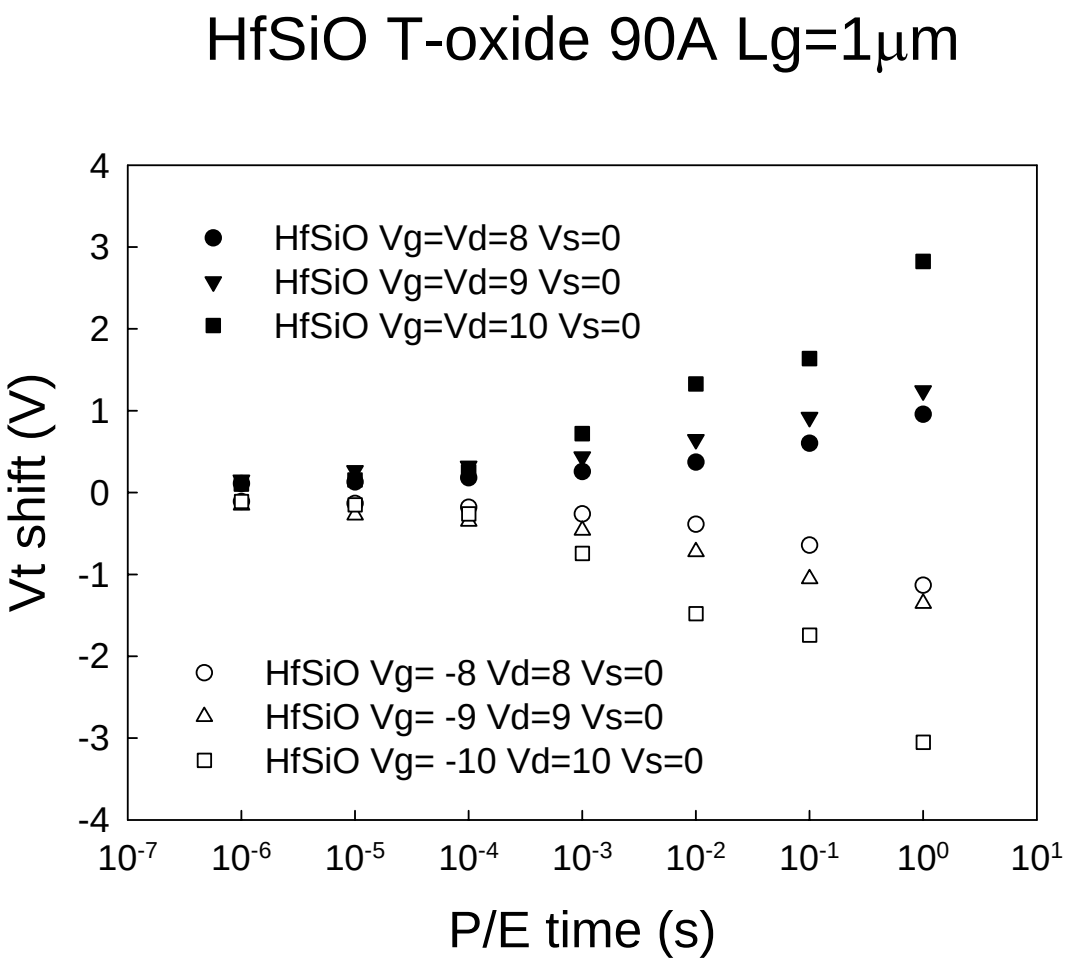

Fig. 3-4 (b) Program and erase characteristics of poly-Si TFT memory with Hf-silicate trapping layer for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 1V with Vg=Vd=10V. The erasing time is about 1 ms

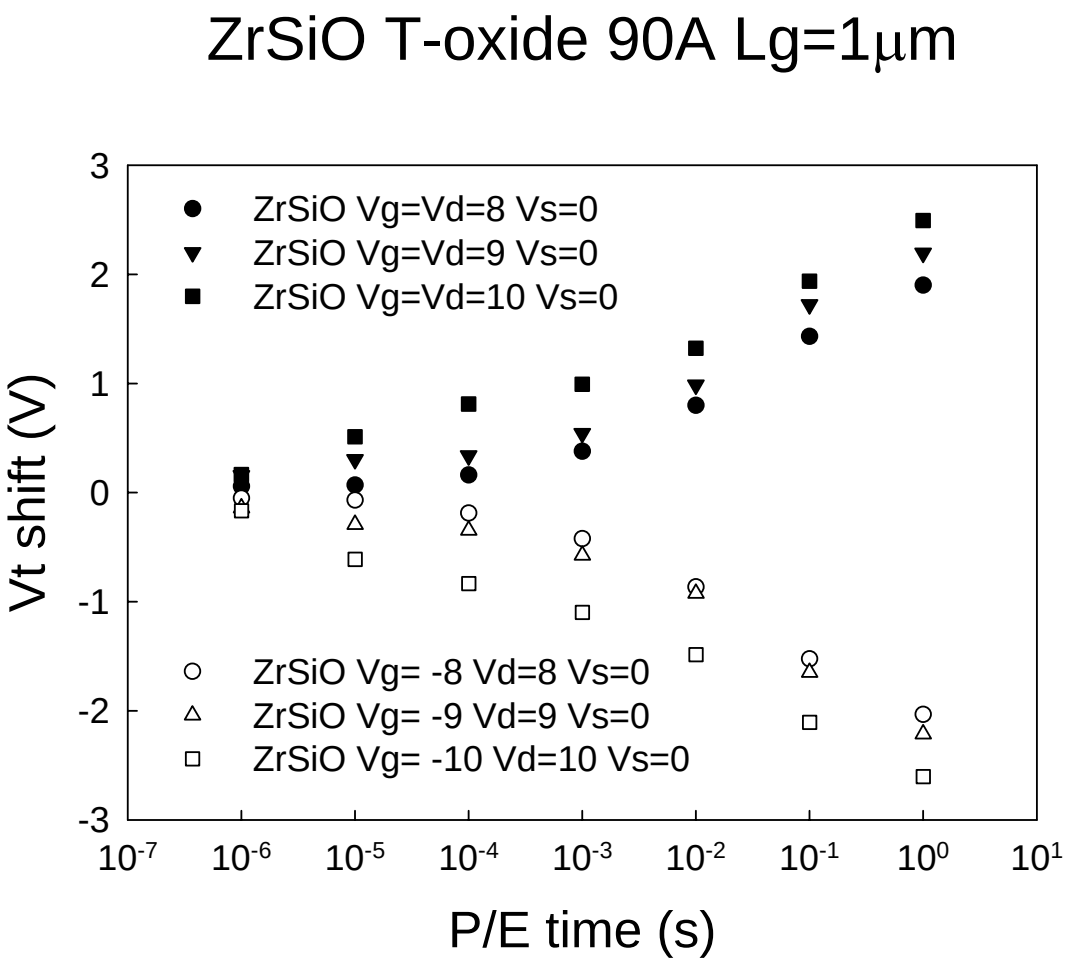

Fig. 3-4 (c) Program and erase characteristics of poly-Si TFT memory with Zr-silicate trapping layer for different programming conditions. The programming time can be as short as 0.1ms if the window margin is set to 1V with Vg=Vd=10V. The erasing time is about 0.1 ms

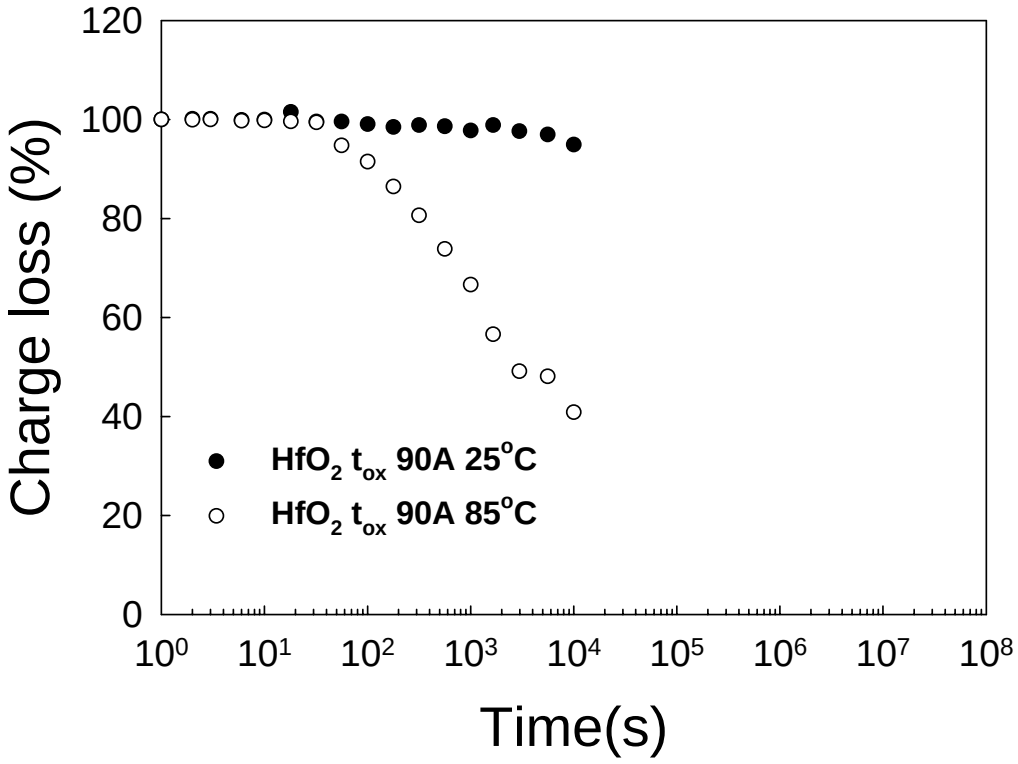

Fig. 3-5 (a) Data retention characteristics of poly-Si TFT memory with HfO_2 trapping layer at T=25℃ and T=85℃.

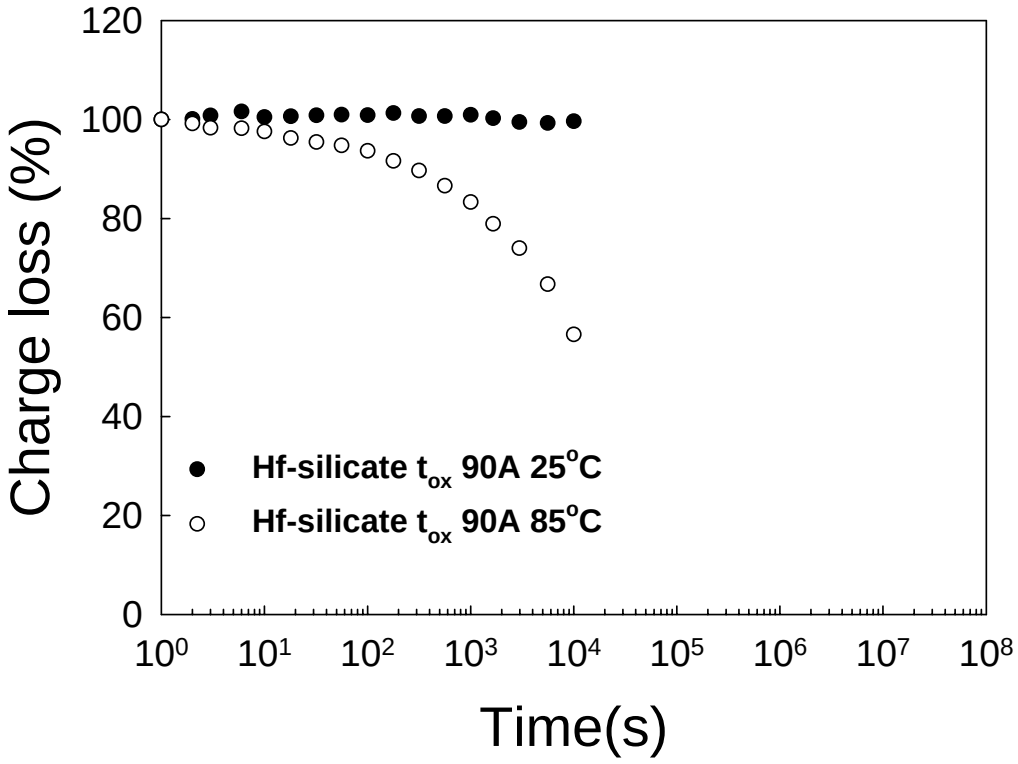

Fig. 3-5 (b) Data retention characteristics of poly-Si TFT memory with Hf-silicate trapping layer at T=25℃ and T=85℃.

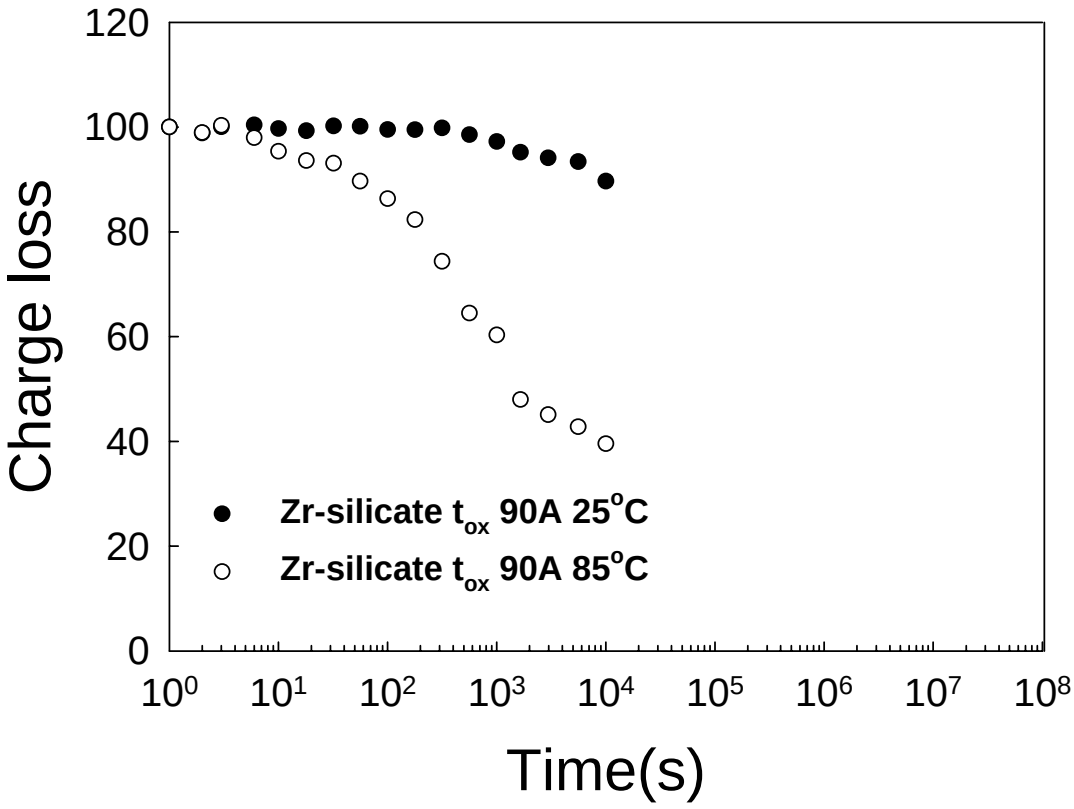

Fig. 3-5 (c) Data retention characteristics of poly-Si TFT memory with Zr-silicate trapping layer at T=25℃ and T=85℃.

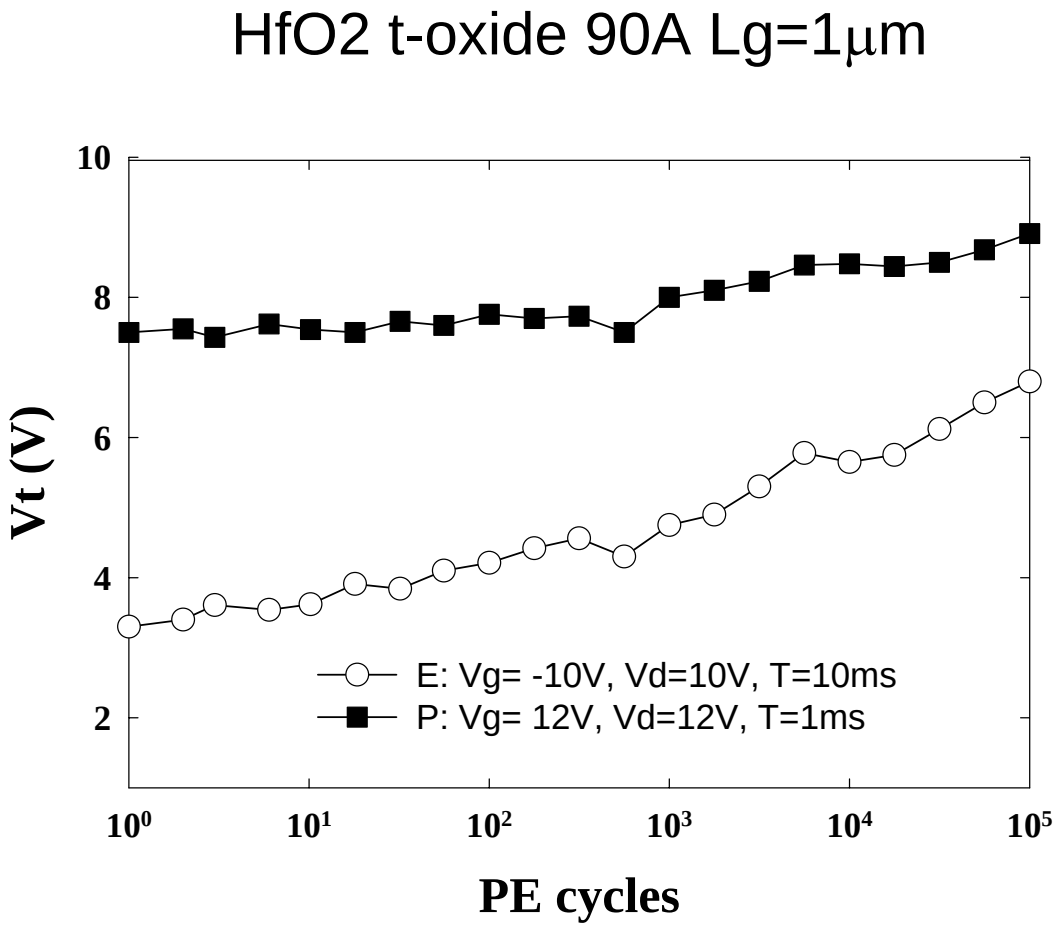

Fig. 3-6 (a) Endurance characteristics of HfO_2 poly-Si TFT memory. Memory window narrows to about 2V after 10^5 P/E cycles.

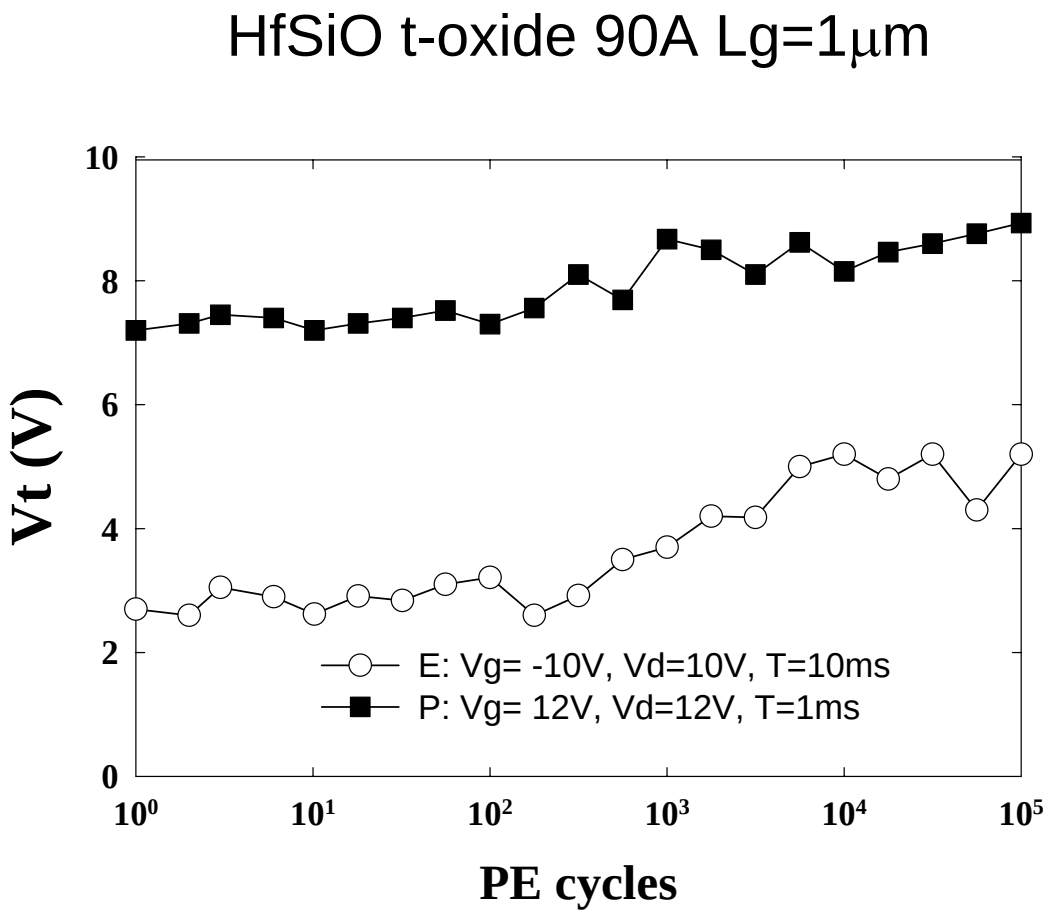

Fig 3-6 (b) Endurance characteristics of Hf-silicate poly-Si TFT memory. Memory window narrowing is less significant and the window is slightly lower than 4V after 10^5 P/E cycles.

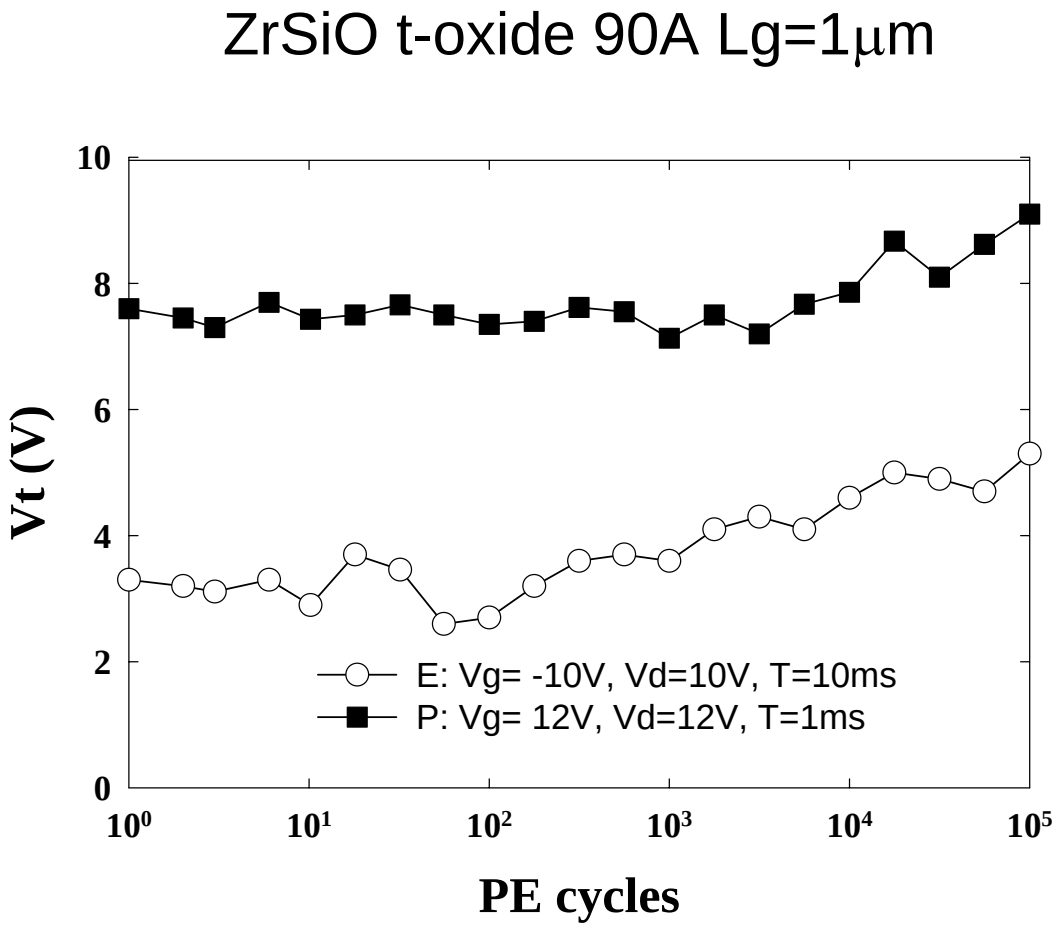

Fig 3-6 (c) Endurance characteristics of Zr-silicate poly-Si TFT memory. Memory window narrowing is less significant and the window is slightly lower than 4V after 10^5 P/E cycles.

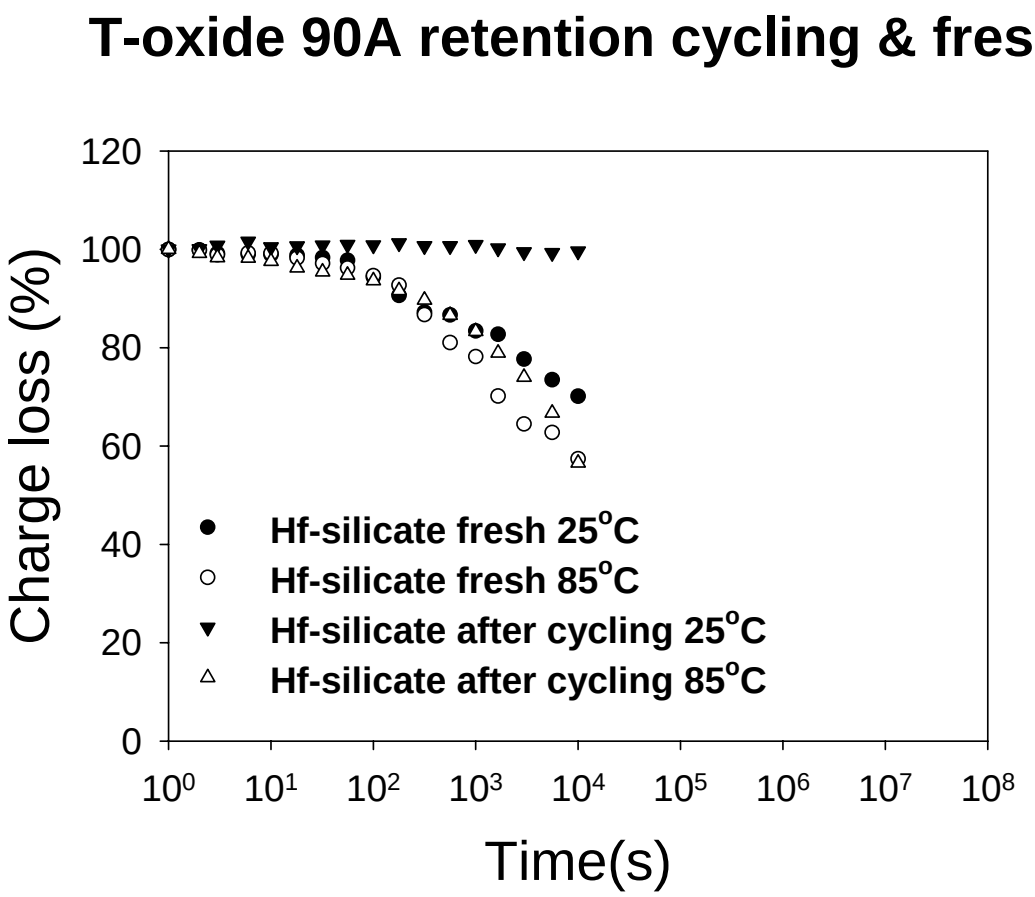

Fig. 3-7 Data retention characteristics of poly-Si TFT memories with cycling and fresh at T=25℃ and T=85℃. The tunneling oxide thickness is 9nm, and trapping layer is Hf-silicate.

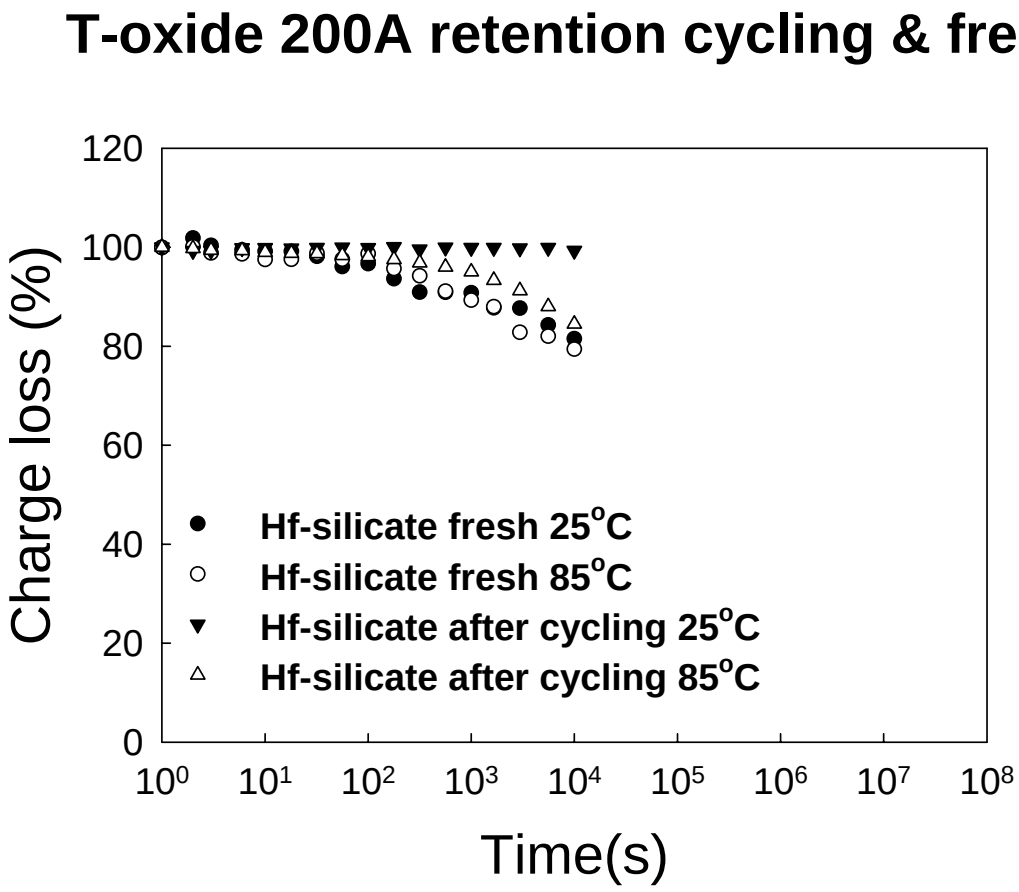

Fig. 3-8 Data retention characteristics of poly-Si TFT memories with cycling and fresh at T=25℃ and T=85℃. The tunneling oxide thickness is 20nm, and trapping layer is Hf-silicate.

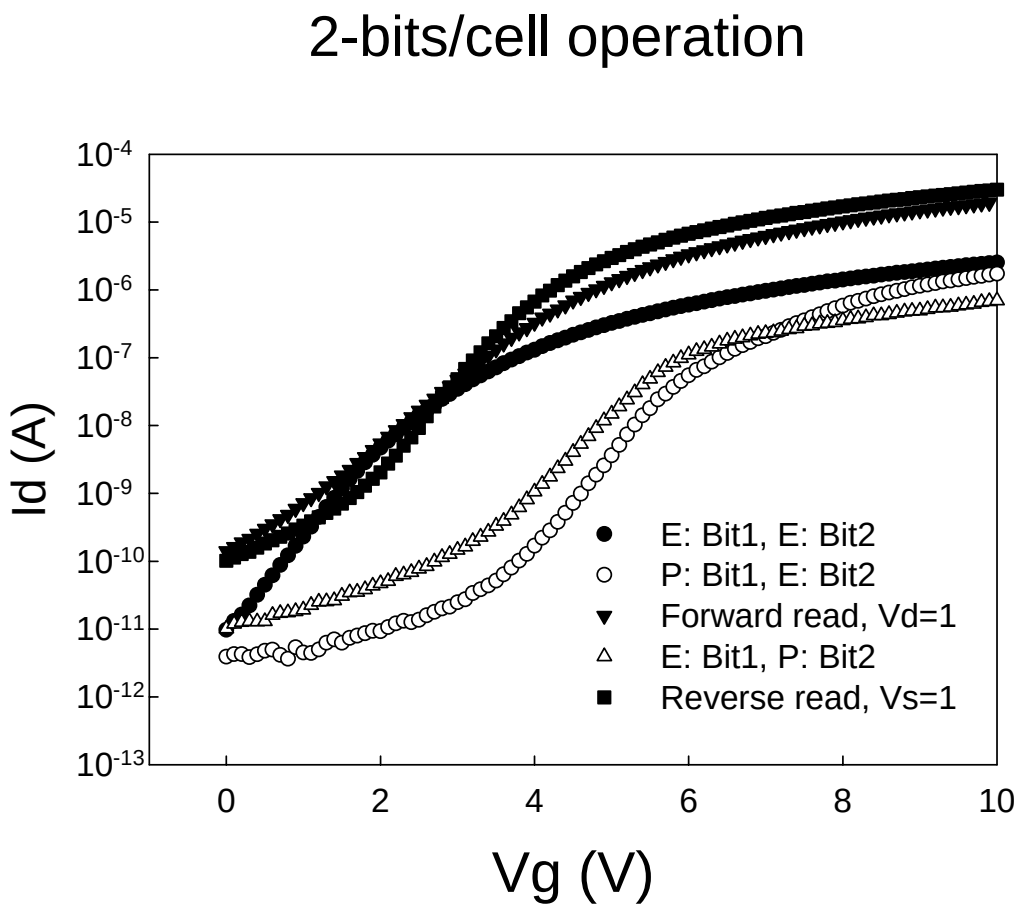

Fig. 3-9 Demonstration of 2 bits/cell operation. E: erased; P: programmed; Bit1: drain side; Bit2: source side.

Table 1. Suggested bias conditions for the 2 bits/cell memory operation.

		Program	Erase	Read
Bit1	Vg	12 V	-10 V	3 V
	Vd	12 V	10 V	0 V
	Vs	0 V	0 V	1 V
Bit2	Vg	12 V	-10 V	3 V
	Vd	0 V	0 V	1 V
	Vs	12 V	10 V	0 V

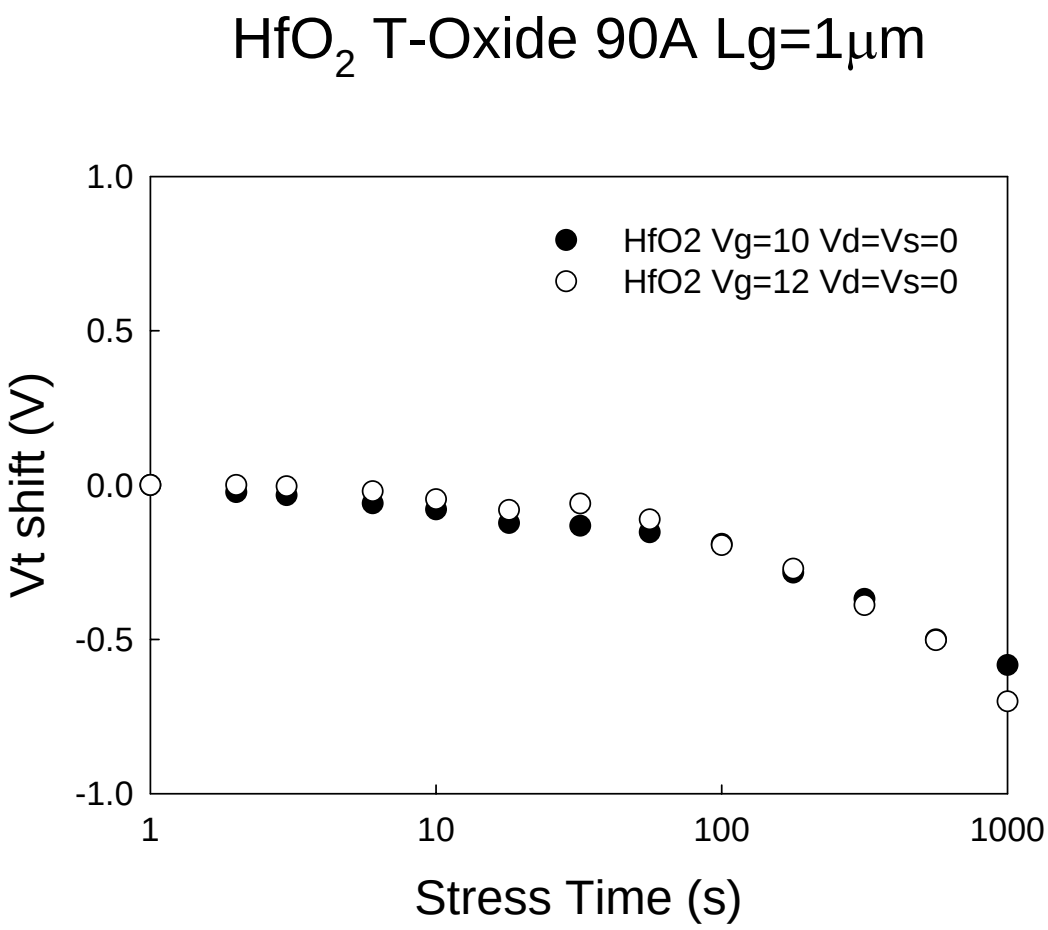

Fig. 3-10 (a) Programming gate disturb characteristics of HfO_2 poly-Si TFT memory with different voltages.

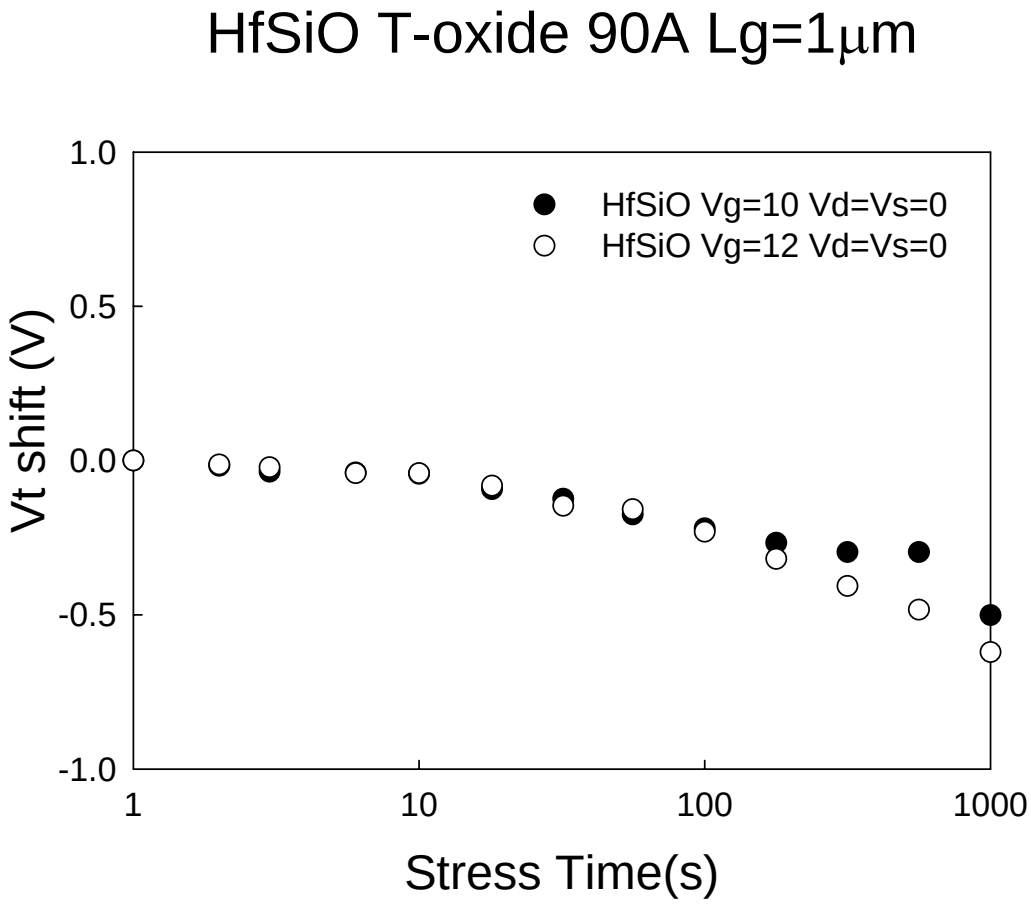

Fig. 3-10 (b) Programming gate disturb characteristics of Hf-silicate poly-Si TFT memory with different voltages.

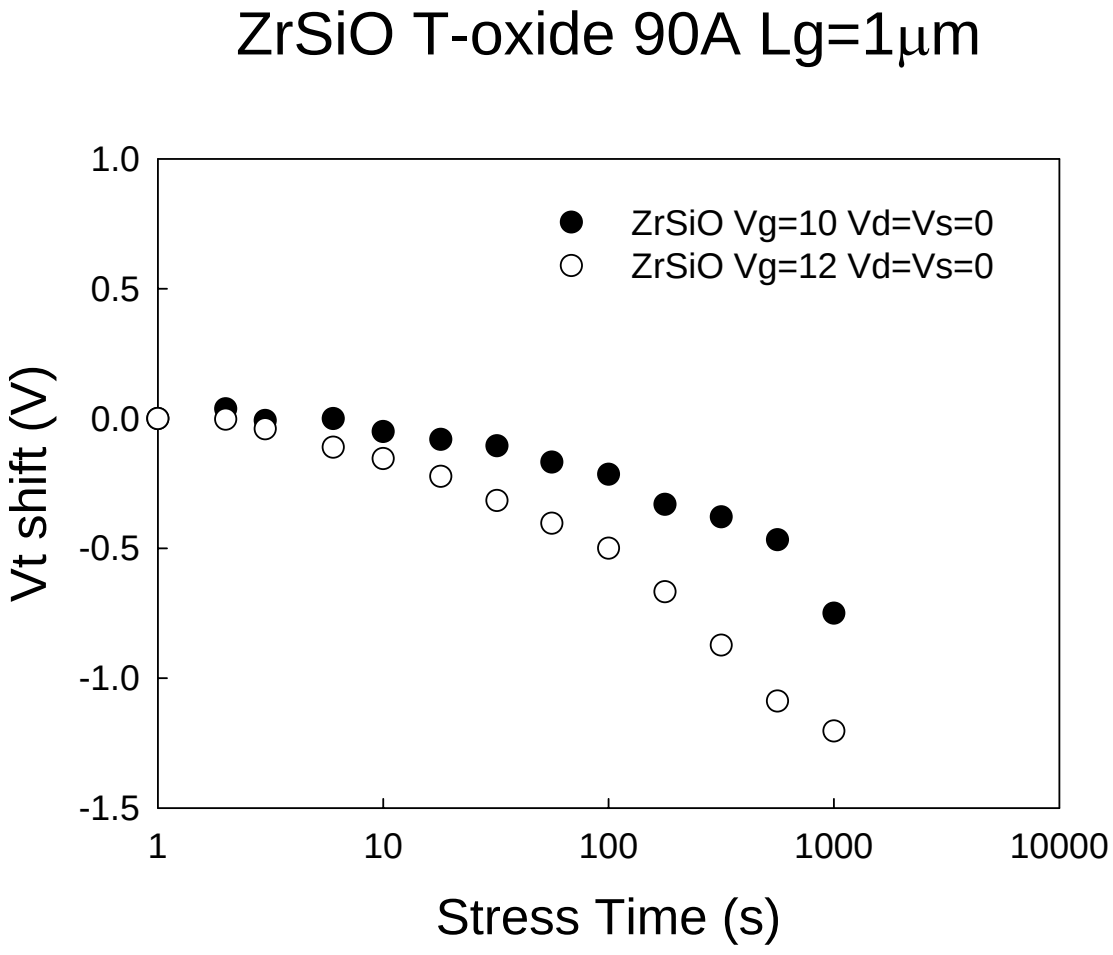

Fig. 3-10 (c) Programming gate disturb characteristics of Zr-silicate poly-Si TFT memory with different voltages.

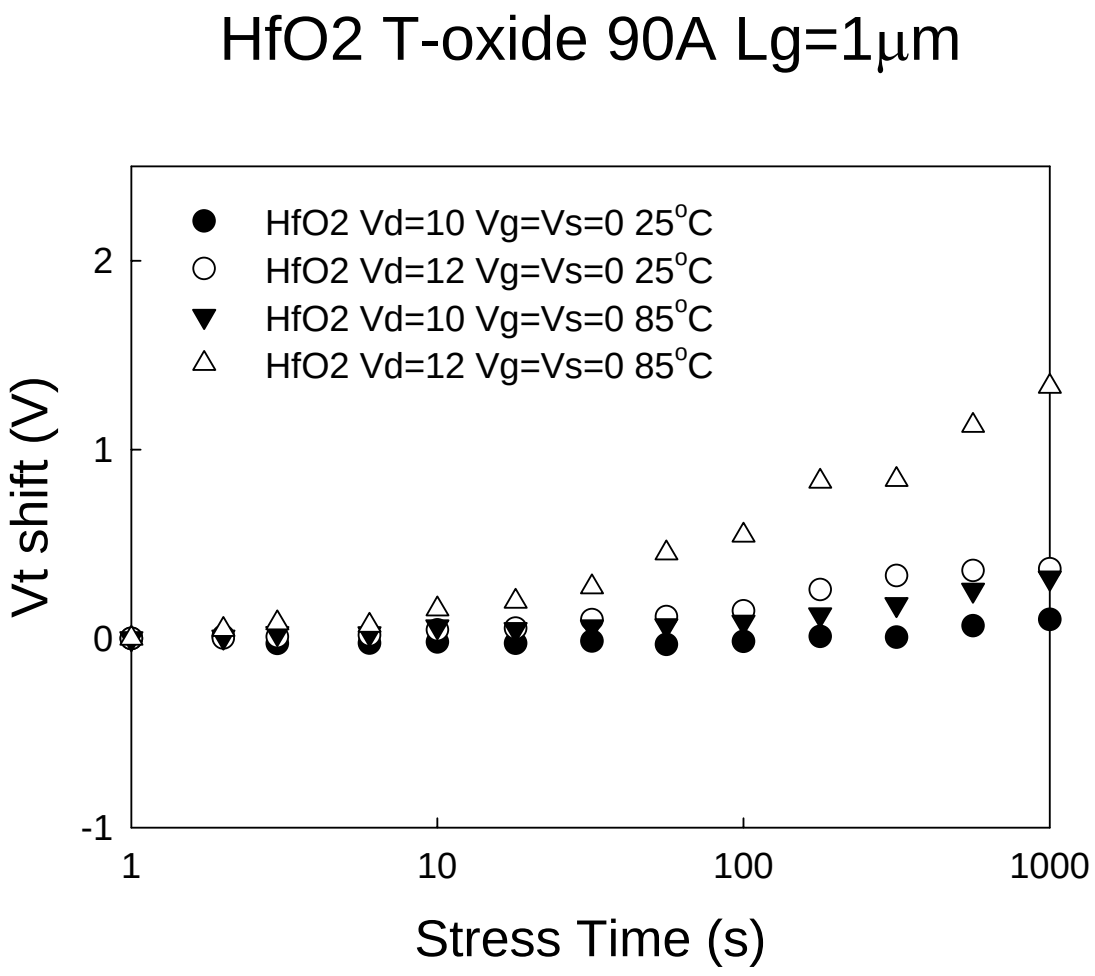

Fig.3-11 (a) Drain disturb characteristics of HfO_2 poly-Si TFT memory with different temperatures and voltages.

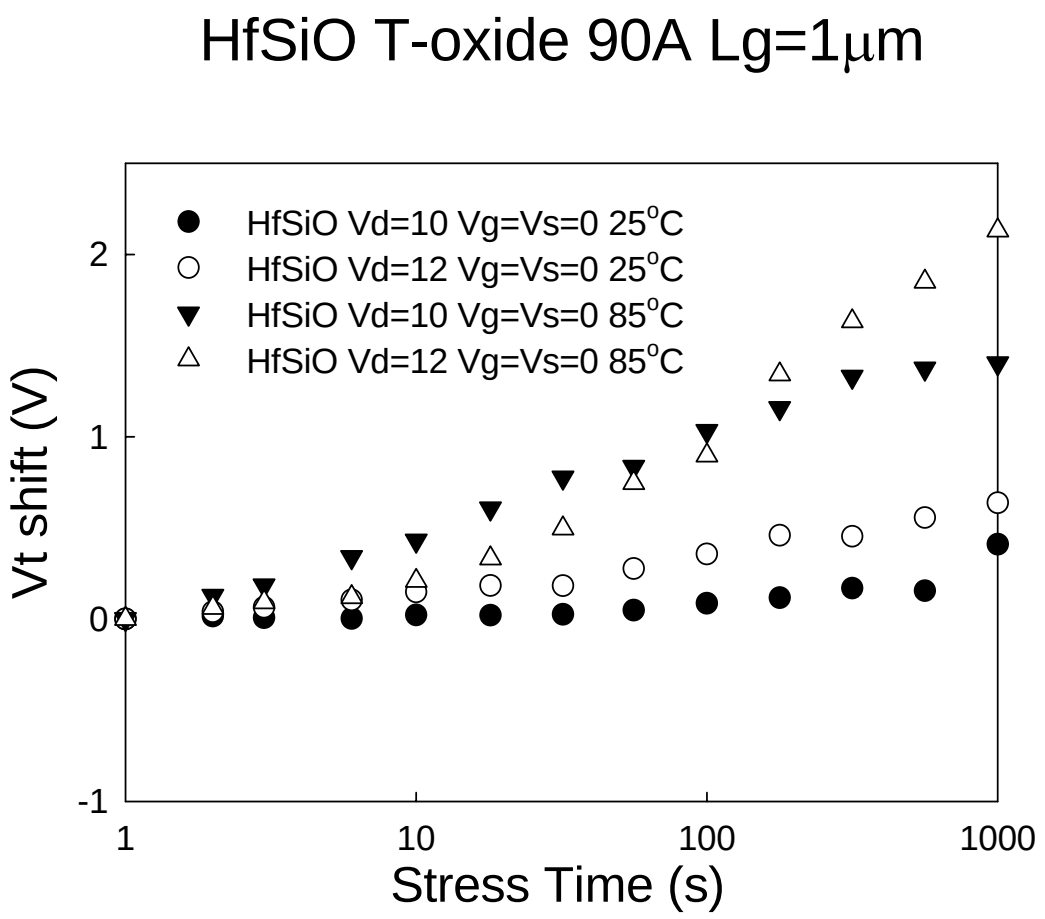

Fig. 3-11 (b) Drain disturb characteristics of Hf-silicate poly-Si TFT memory with different temperatures and voltages.

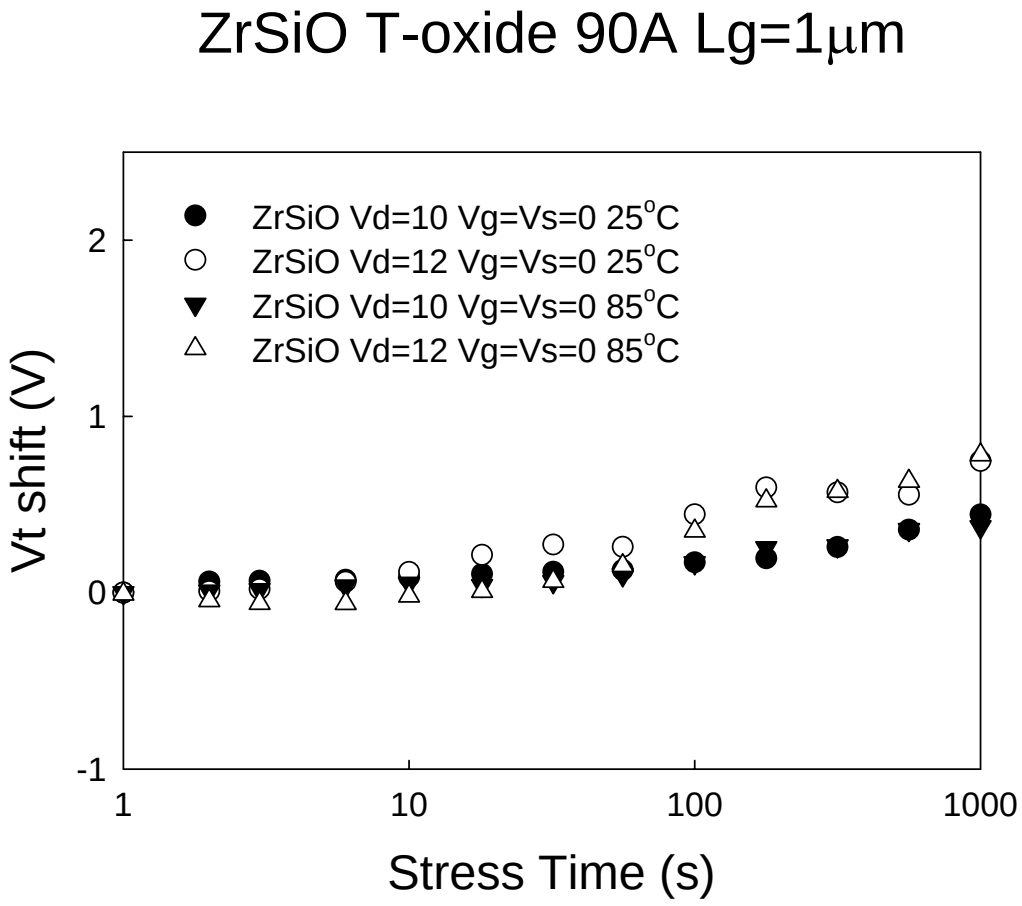

Fig. 3-11 (c) Drain disturb characteristics of Zr-silicate poly-Si TFT memory with different temperatures and voltages.

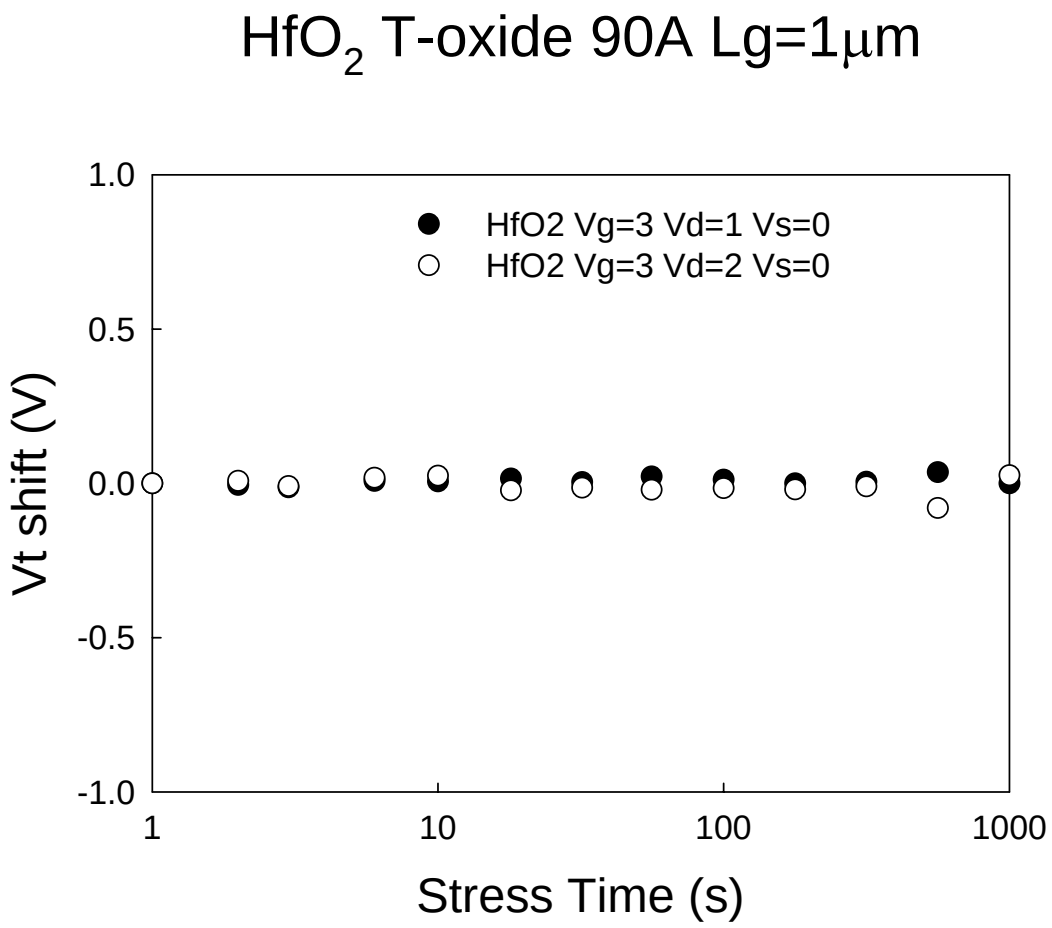

Fig. 3-12 (a) Read disturb characteristics of HfO_2 poly-Si TFT memory with different read conditions at 25°C.

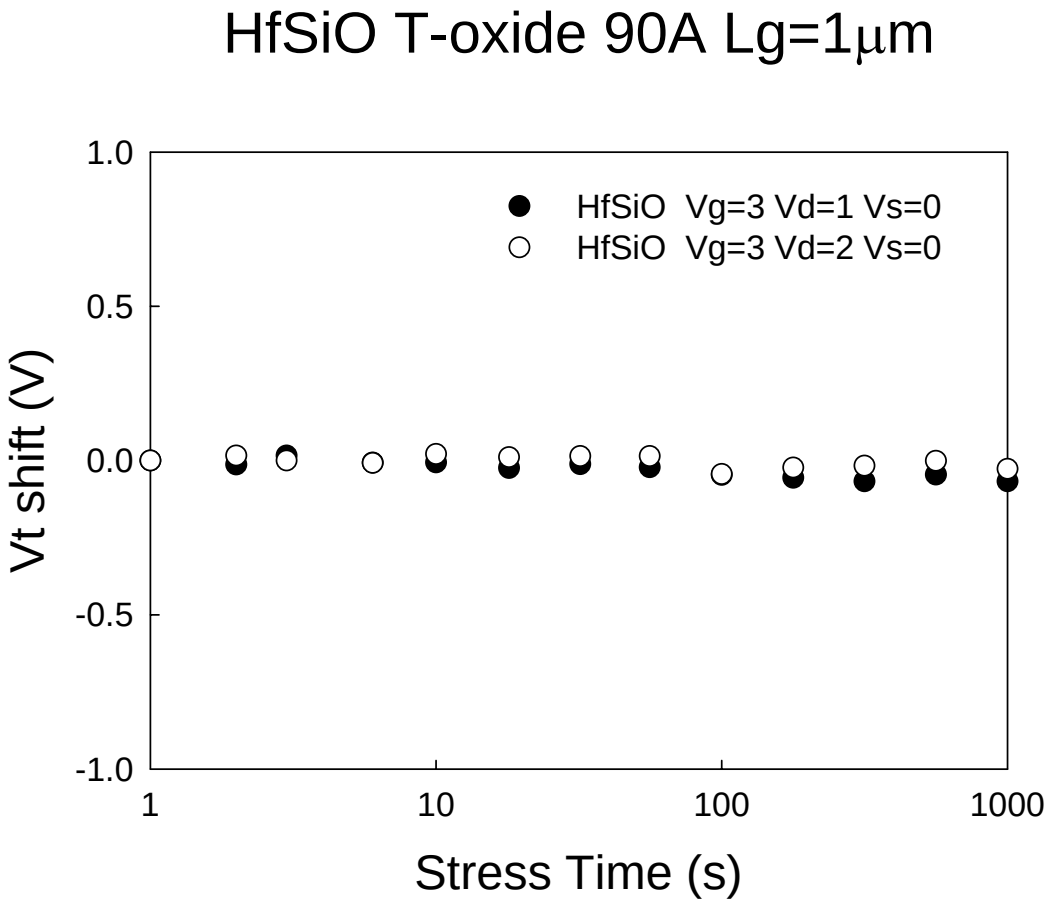

Fig. 3-12 (b) Read disturb characteristics of Hf-silicate poly-Si TFT memory with different read conditions at 25°C

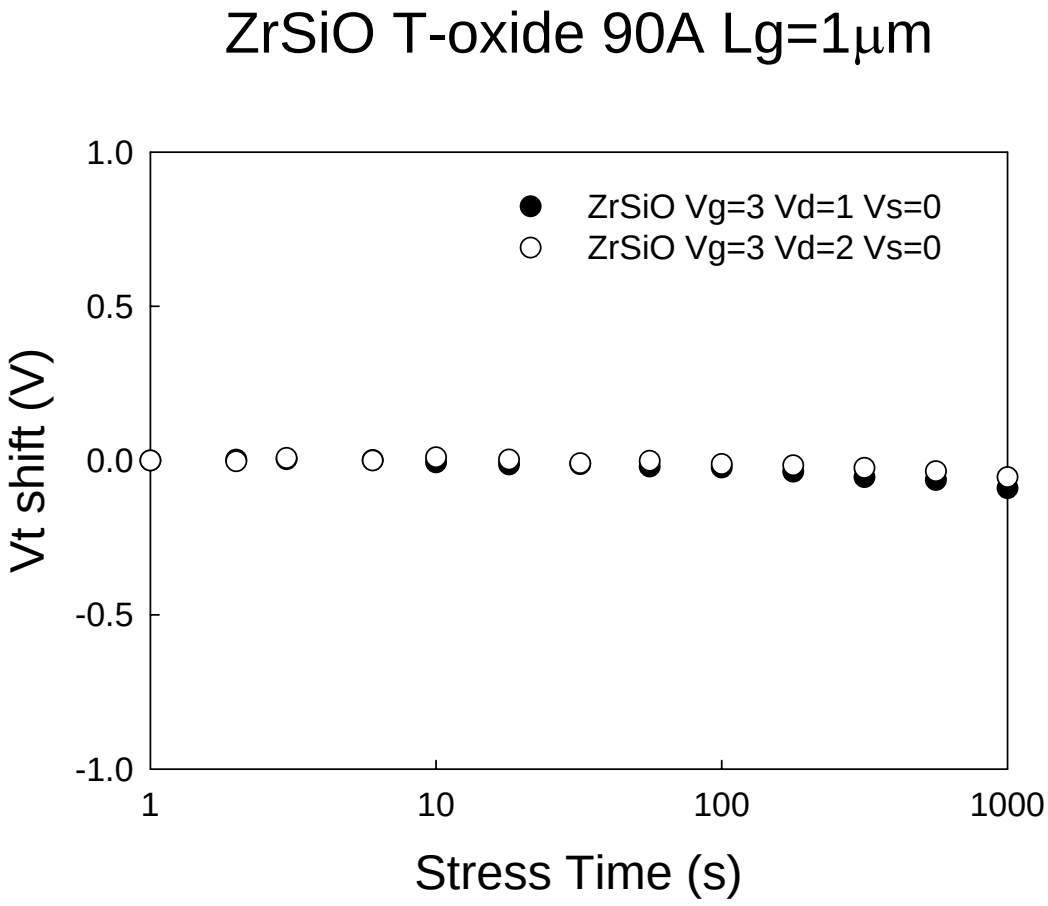

Fig. 3-12 (c) Read disturb characteristics of Zr-silicate poly-Si TFT memory with different read conditions at 25°C

Chapter 4

The electrical characteristics with different tunneling oxide thickness and improvement of NH_3 plasma treatment

4-1 Different tunneling oxide thickness

Fig.4-1 (a)-(c) show the retention behavior of the TFT flash memory device after NH_3 plasma treatment with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) in programmed state, at room temperature (25℃) and high temperature (85℃), respectively. As we mentioned above, the charge loss behavior under the high temperature condition is accelerated seriously than that under the room temperature condition. However, the device with thicker tunneling oxide thickness (20 nm) would have better retention performance than the sample with thinner tunneling oxide thickness (9 nm) as shown in Fig. 4-1 (a)-(c). In addition, the same tendency that the charge loss improved for the device with thicker tunneling oxide thickness was happened for the device with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate). It has been reputed that [12] the flash memory device with the thicker tunneling oxide thickness resulted in a worse performance during P/E speed. Fortunately, this degradation of P/E speed for the different tunneling oxide thickness was not observed in our device as shown in Fig.4-2 (a)-(c). The reason for this phenomenon is the different way of the programming. For the sample with F-N programming [12], the thicker tunneling oxide thickness would have smaller electrical field resulted in the degradation of P/E speed. On the other hand, the device with channel hot electron programming would not degrade the P/E speed, resulting from the lucky electron of channel hot electron injection [13]. According to the lucky electron model of channel hot electron injection [13], the $P(E_{ox})$ were

the same order for the different tunneling oxide thickness with results in the devices with the different tunneling oxide thickness still have almost the same gate current. This reason explains why our device with thicker tunneling oxide thickness can a have better retention behavior while maintaining the P/E speed performance.

The characteristics of gate disturbance for the TFT flash memory devices after NH_3 plasma treatment with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) and tunneling oxide thickness (20 nm & 9 nm) under different applied gate bias stress were shown in Fig.4-3 (a)-(c), respectively. As we can see in Fig.4-3 (a), the threshold voltage shift under 10 V applied gate voltage was smaller than the 12 V applied gate voltage for the device with 9 nm tunneling oxide. But this large Vt shift would much improved for the device with thicker tunneling oxide (20 nm) as shown in this figure. When the applied gate bias was 10 V, the threshold voltage shift was only about -0.2 V for the device with 20 nm tunneling oxide. The same trend was shown in all devices with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) as illustrated in Fig.4-3 (a)-(c). The reason for the improvement of gate disturbance for the device under different gate bias stress is the applied gate bias induced grain boundary trap [14] or interface state trap [14]. The gate disturbance can be affected by the grain boundary trap and the interface state trap. As the grain boundary trap and interface state trap increase, the gate disturbance would become more serious. Because of the threshold voltage was defined as gate voltage and would also been affected by the surface potential [14]. The surface potential would be larger for the device with the thinner gate oxide thickness than the device with the thicker gate oxide thickness resulted in the large trapping density while the applied gate voltage was the same value. In addition, the threshold voltage shift would also be more serious. This discussion can explain why the device with thicker tunneling oxide thickness would have better gate disturbance behavior. The same tendency was famed in all devices with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) as shown in Fig. 4-3 (a)-(c). Even the same trend happened in different trapping layers, the device with the HfO_2

and Hf-silicate trapping layer exhibit the better gate disturbance performance as indicated in these three figures.

The drain disturbance behavior of the TFT flash memory device after NH_3 plasma treatment with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) and tunneling oxide thickness (20 nm & 9 nm) under different applied gate bias stress were shown in Fig.4-4 (a)-(c), respectively. The drain disturbance was not serious in our samples as shown in these figures. The threshold voltage shift was only about 0.5 V for the devices with the HfO_2 and Hf-silicate trapping layer and 0.7 V for the device with Zr-silicate trapping layer, respectively. We can find that the different thickness of tunneling oxide thickness have no effect on the drain disturbance. But the applied drain bias significantly influenced the threshold voltage shift as indicated in these three figures. The Vt shift was increased with increasing of applied drain voltage stress. For the same tunneling oxide thickness, the threshold voltage shift under the low drain bias stress (10 V) was 0.25V smaller than that with the high drain bias stress (12 V). In addition, the same trend was found for all devices with different trapping layers as illustrated in Fig.4-4 (a)-(c).

4-2 Improvement of NH_3 plasma treatment

The NH_3 plasma treatment is one of the useful methods to improve the SiO_2/poly-Si interface and channel quality, resulting from the NH_3 plasma treatment can eliminate the trap density in both the SiO_2/poly-Si interface and channel. Fig.4-5 shown the retention behavior of the TFT flash memory with and without NH_3 plasma treatment. As we can see in this figure, the device with NH_3 plasma treatment had a better retention loss than the sample without NH_3 plasma treatment. Without the NH_3 plasma treatment, the charge loss of the sample with Hf-silicate trapping layer was loss more than 20% while the samples with HfO_2 and Zr-silicate trapping layers were loss more than 40%. After the NH_3 plasma treatment, the charge loss of all the samples were much improved as shown in this figure. This result approved that the NH_3 plasma treatment was a very promising approach to improve the retention behavior of the TFT flash memory. In addition, the NH_3 plasma treatment can improve the drain disturbance of the TFT flash memory device as indicated in Fig.4-6 (a)-(c). These three figures compared the improvement of NH_3 plasma treatment for the devices with different trapping layers (HfO_2, Hf-silicate, and Zr-silicate) and different tunneling oxide thickness. The NH_3 plasma treatment can much reduced the Vt shift of the drain disturbance of the TFT flash memory with HfO_2 and Hf-silicate trapping layers to 0.5V. For the sample with Zr-silicate trapping layer, the Vt shift of the drain disturbance was about 0.6V. This is because the hydrogen atoms of NH_3 can terminate dangling bonds and replace weak bonds in the grain boundaries and SiO_2/poly-Si interface and thus reduce the trap states in the poly-Si channel. To eliminate these trap states can improve both the performance and reliability of poly-Si TFTs. These results mean that the NH_3 plasma treatment not only improves the data retention loss behavior but also the drain disturbance of the TFT flash memory.

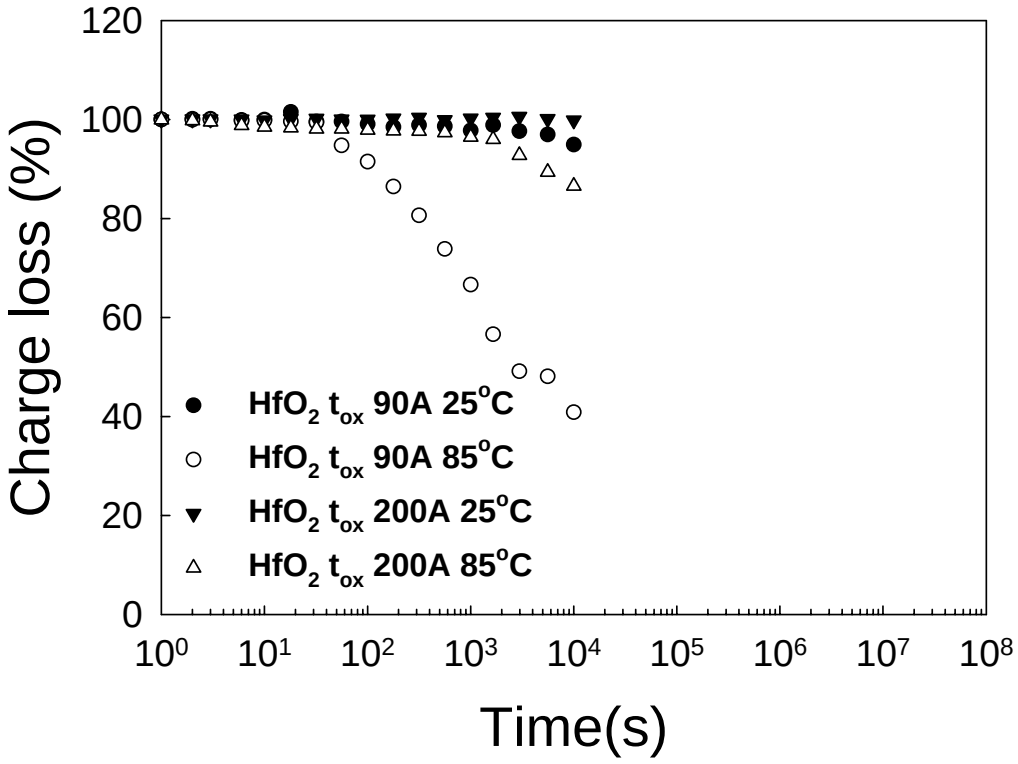

Fig. 4-1 (a) Data retention characteristics of HfO_2 poly-Si TFT memory with different tunneling oxide thickness at T=25℃ and T=85℃.

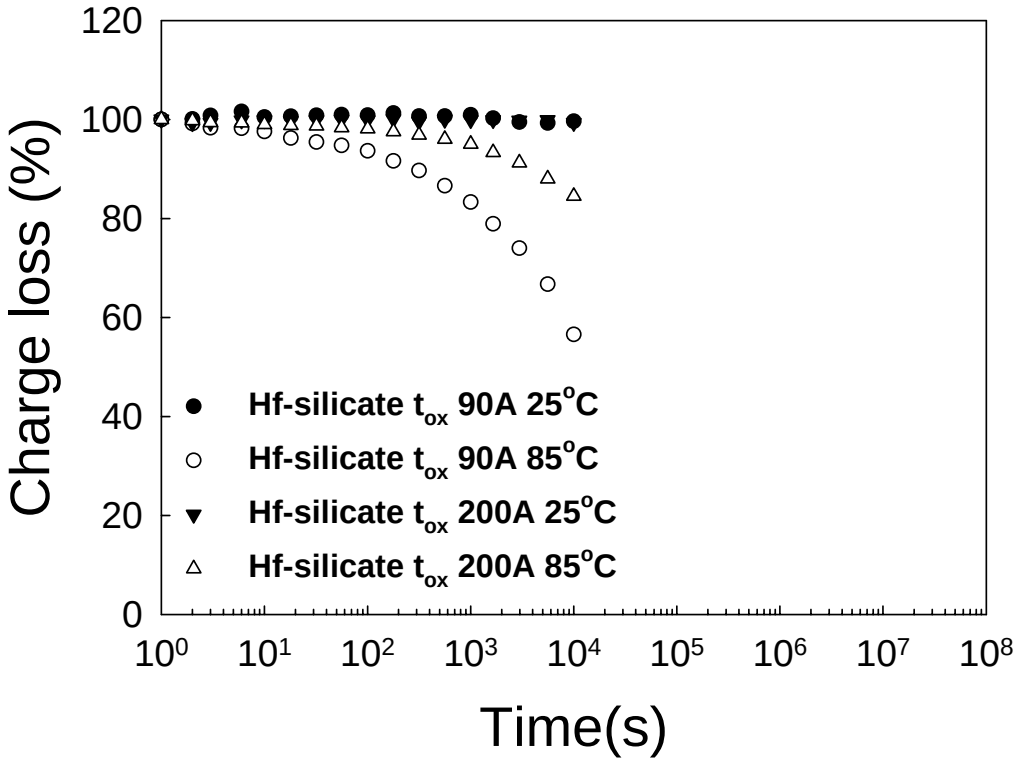

Fig. 4-1 (b) Data retention characteristics of Hf-silicate poly-Si TFT memory with different tunneling oxide thickness at T=25℃ and T=85℃.

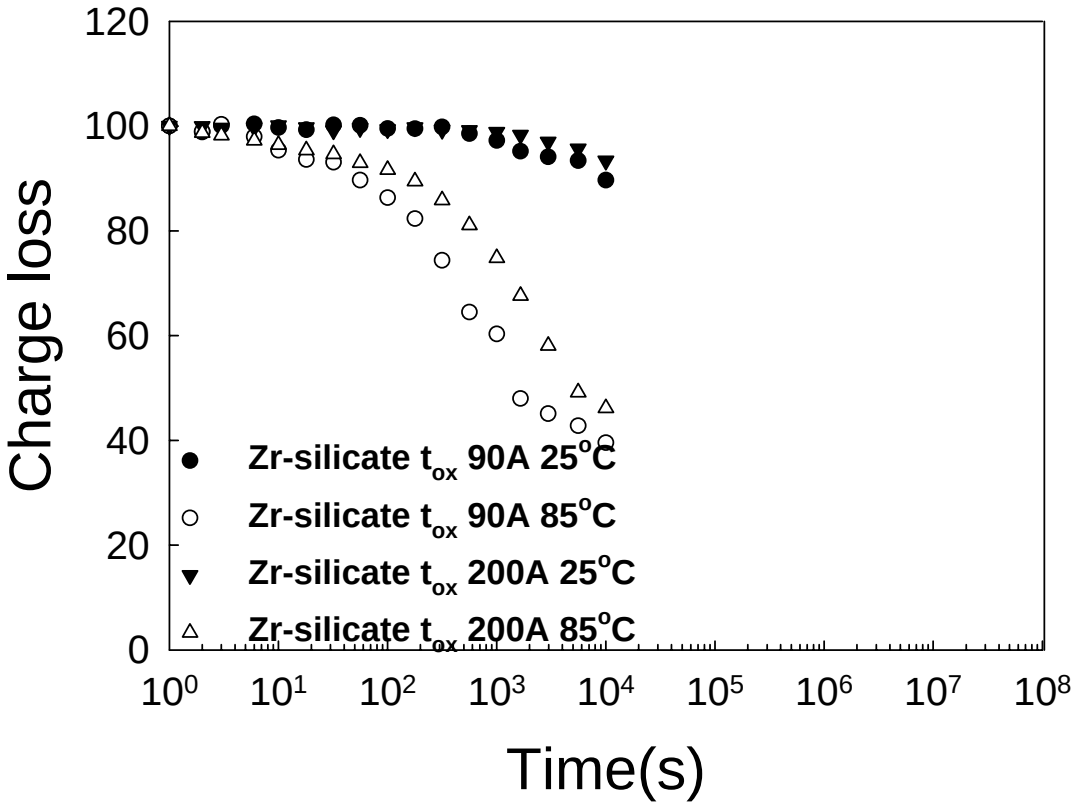

Fig. 4-1 (c) Data retention characteristics of Zr-silicate poly-Si TFT memory with different tunneling oxide thickness at T=25℃ and T=85℃.

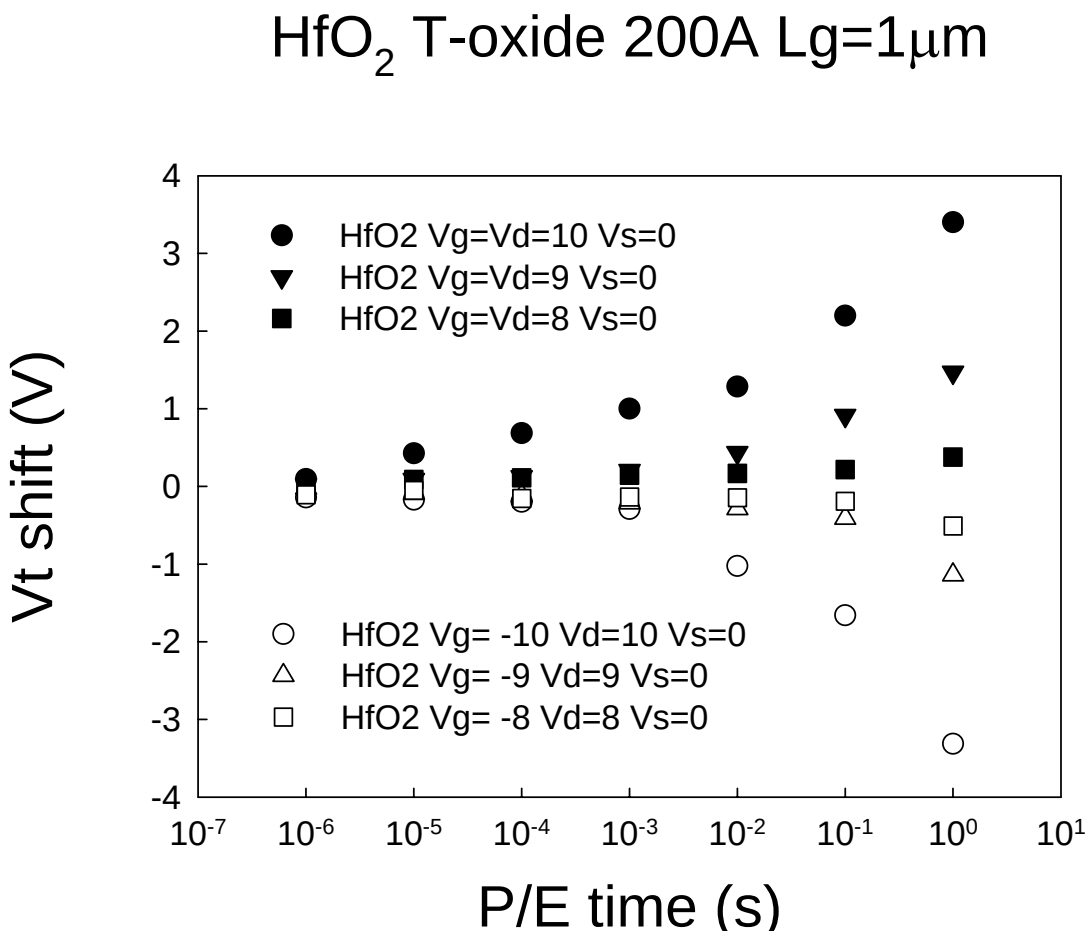

Fig. 4-2 (a) Program and erase characteristics of HfO_2 poly-Si TFT memory with tunneling oxide thickness 20nm for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 1V with Vg=Vd=10V. The erasing time is about 1 ms.

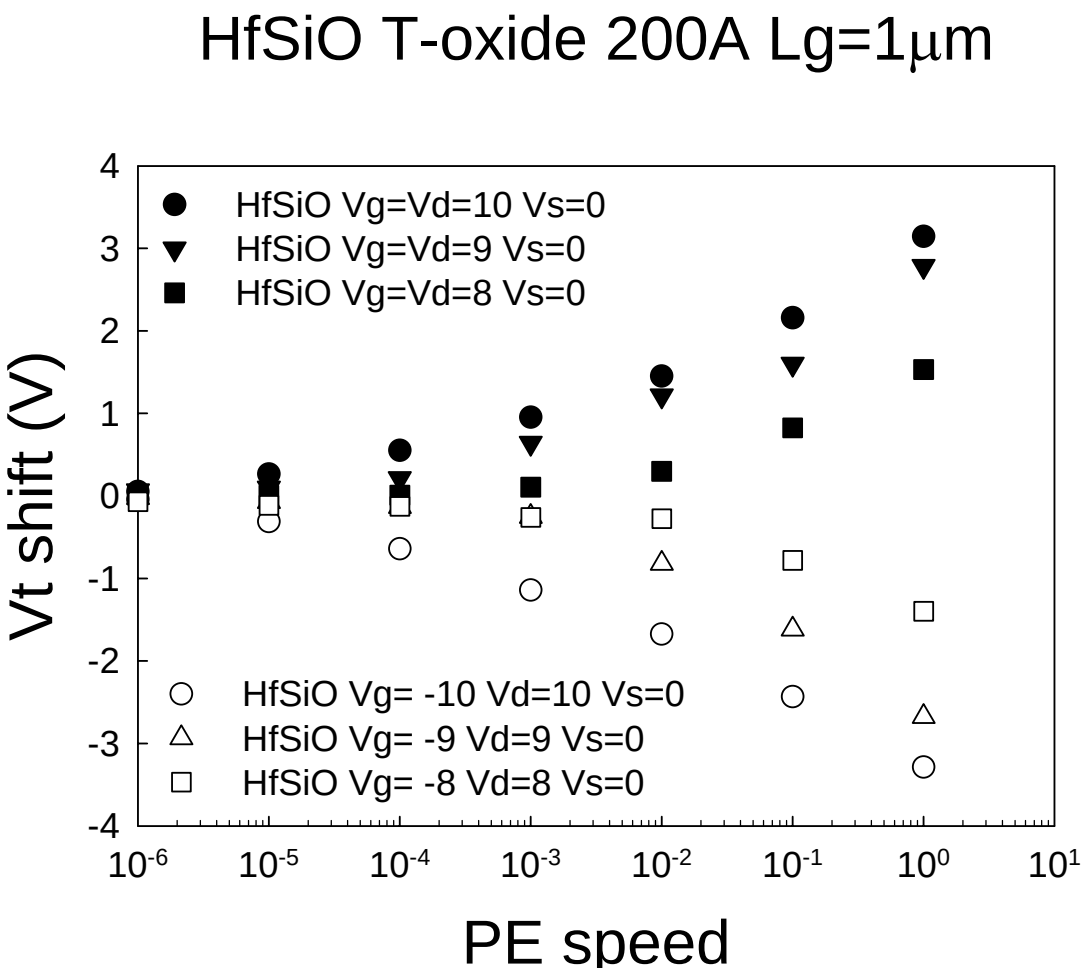

Fig. 4-2 (b) Program and erase characteristics of Hf-silicate poly-Si TFT memory with tunneling oxide thickness 20nm for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 1V with Vg=Vd=10V. The erasing time is about 1 ms.

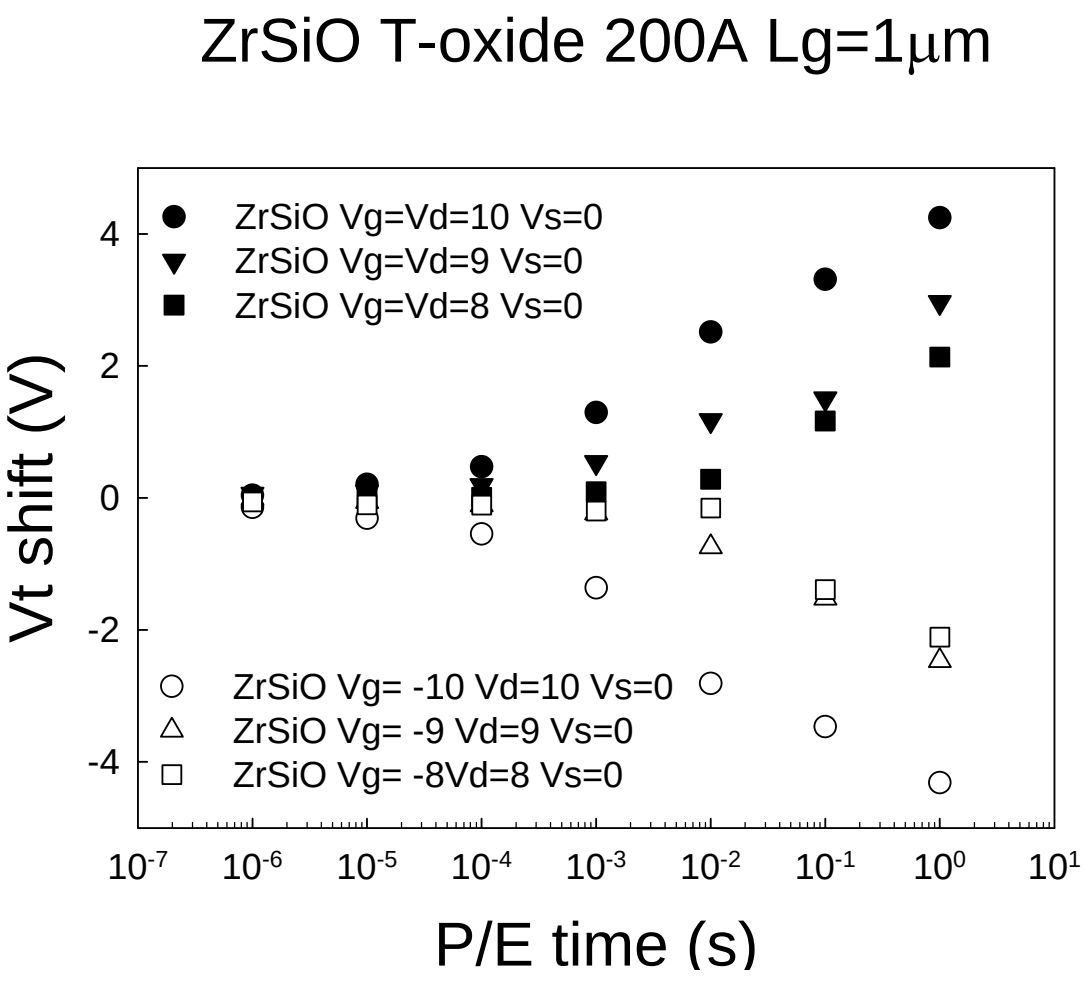

Fig. 4-2 (c) Program and erase characteristics of Zr-silicate poly-Si TFT memory with tunneling oxide thickness 20nm for different programming conditions. The programming time can be as short as 1ms if the window margin is set to 1.5V with Vg=Vd=10V. The erasing time is about 1 ms.

Table 2. Comparison table for the HfO2, Hf-silicate and Zr-silicate poly-Si TFT memories in the aspects of tunneling oxide thickness 9nm and 20nm program speed. The program operation is Vg=10 V, Vd=10 V, and Vs=0. Those programming time are memory window at 1 V.

	Tunneling oxide 9nm	Tunneling oxide 20nm
HfO_2	1×10^{-4} sec	1×10^{-3} sec
Hf-silicate	5×10^{-3} sec	1×10^{-3} sec
Zr-silicate	1×10^{-3} sec	1×10^{-3} sec

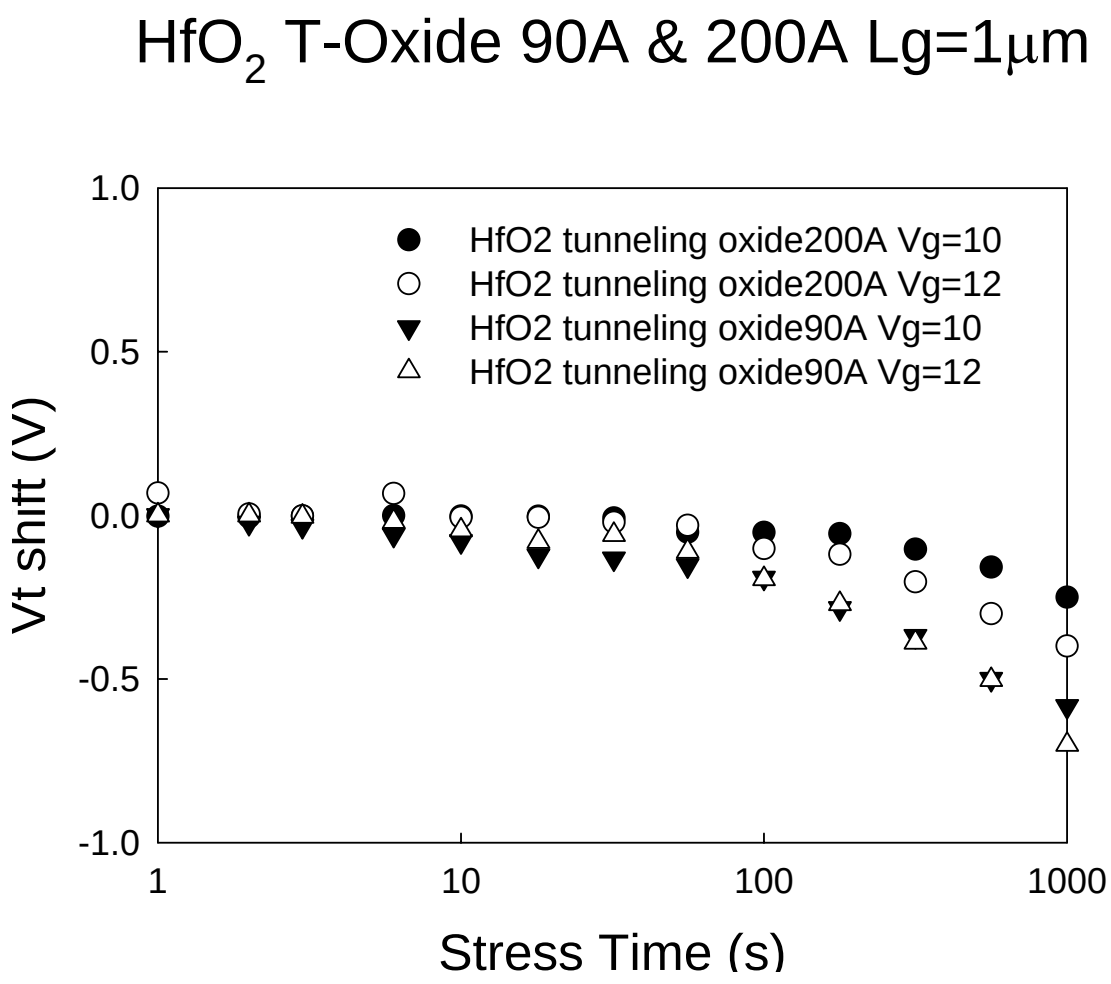

Fig. 4-3 (a) Programming gate disturb characteristics of HfO_2 poly-Si TFT memory with different tunneling oxide thickness and voltages.

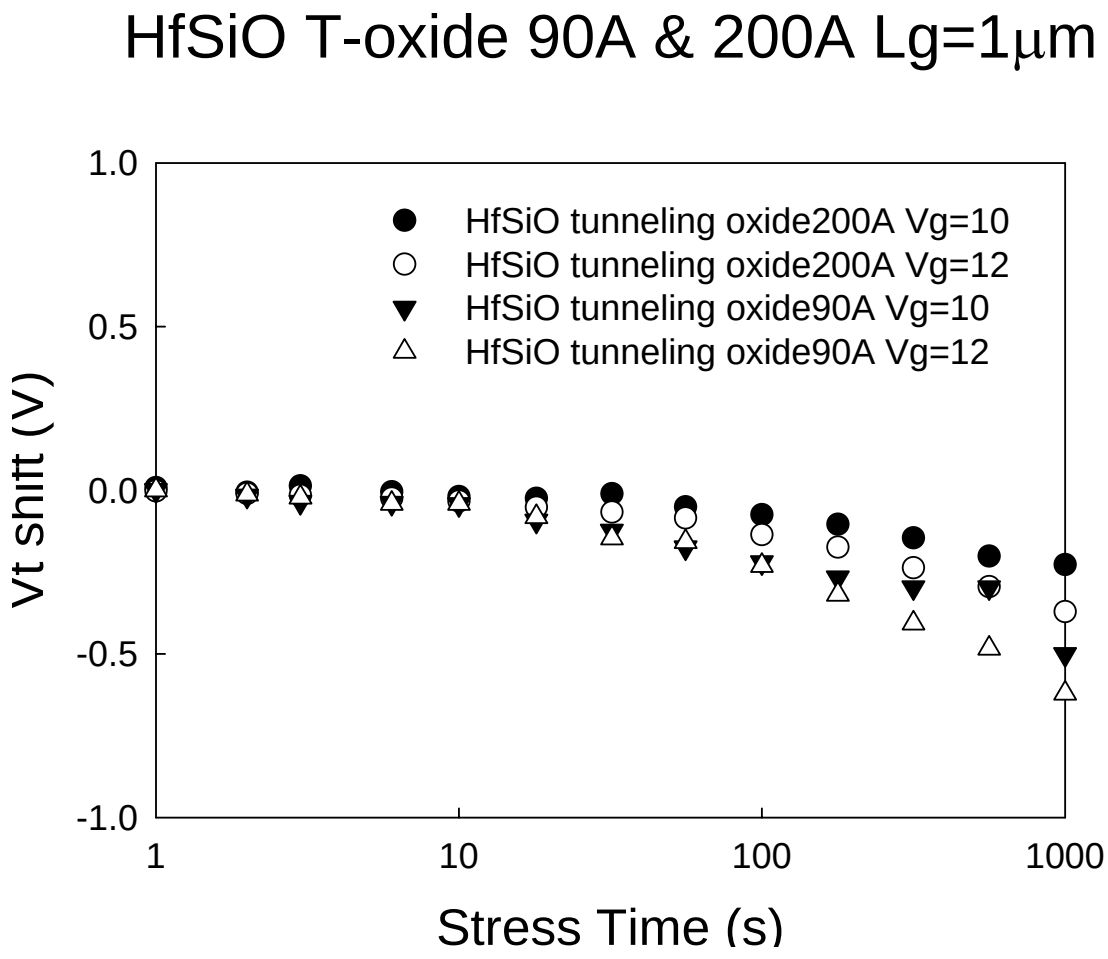

Fig. 4-3 (b) Programming gate disturb characteristics of Hf-silicate poly-Si TFT memory with different tunneling oxide thickness and voltages.

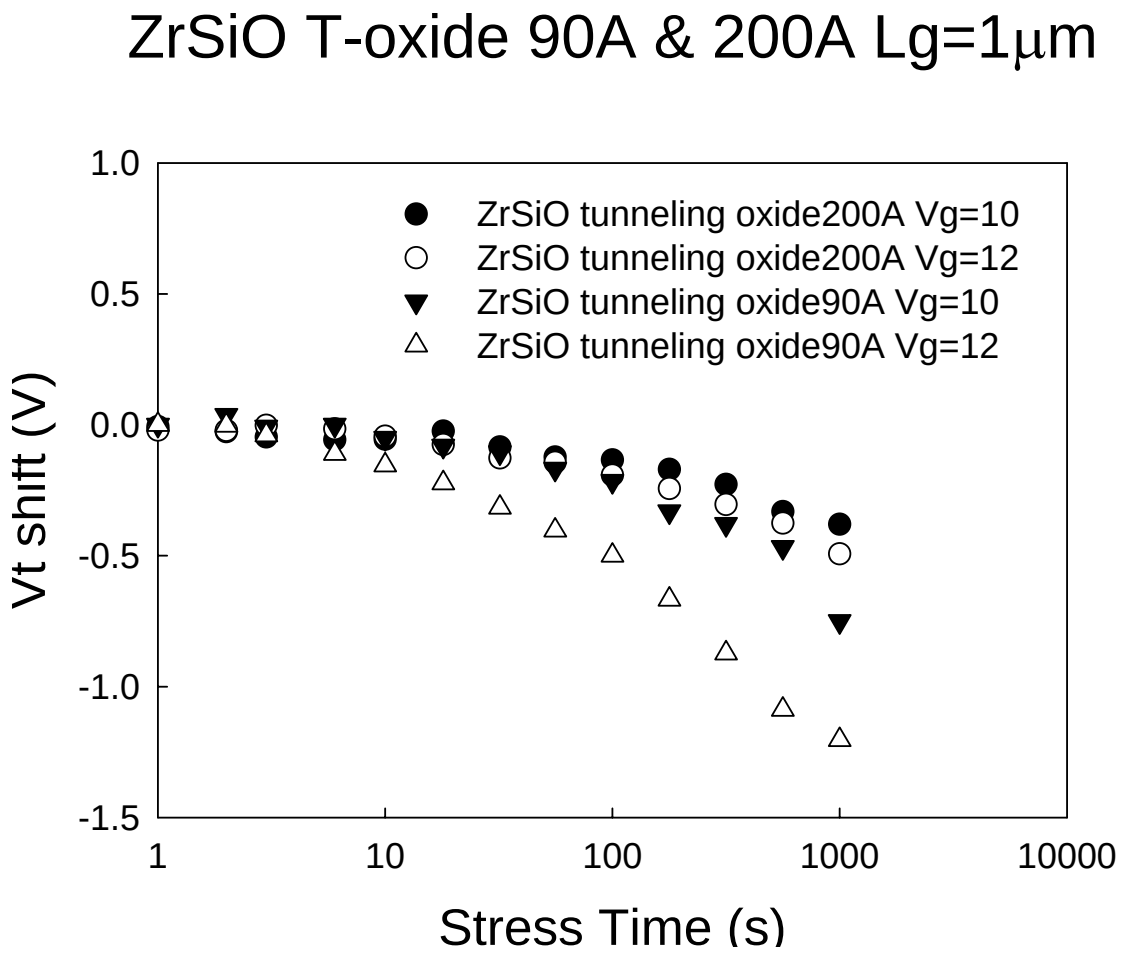

Fig. 4-3 (c) Programming gate disturb characteristics of Zr-silicate poly-Si TFT memory with different tunneling oxide thickness and voltages.

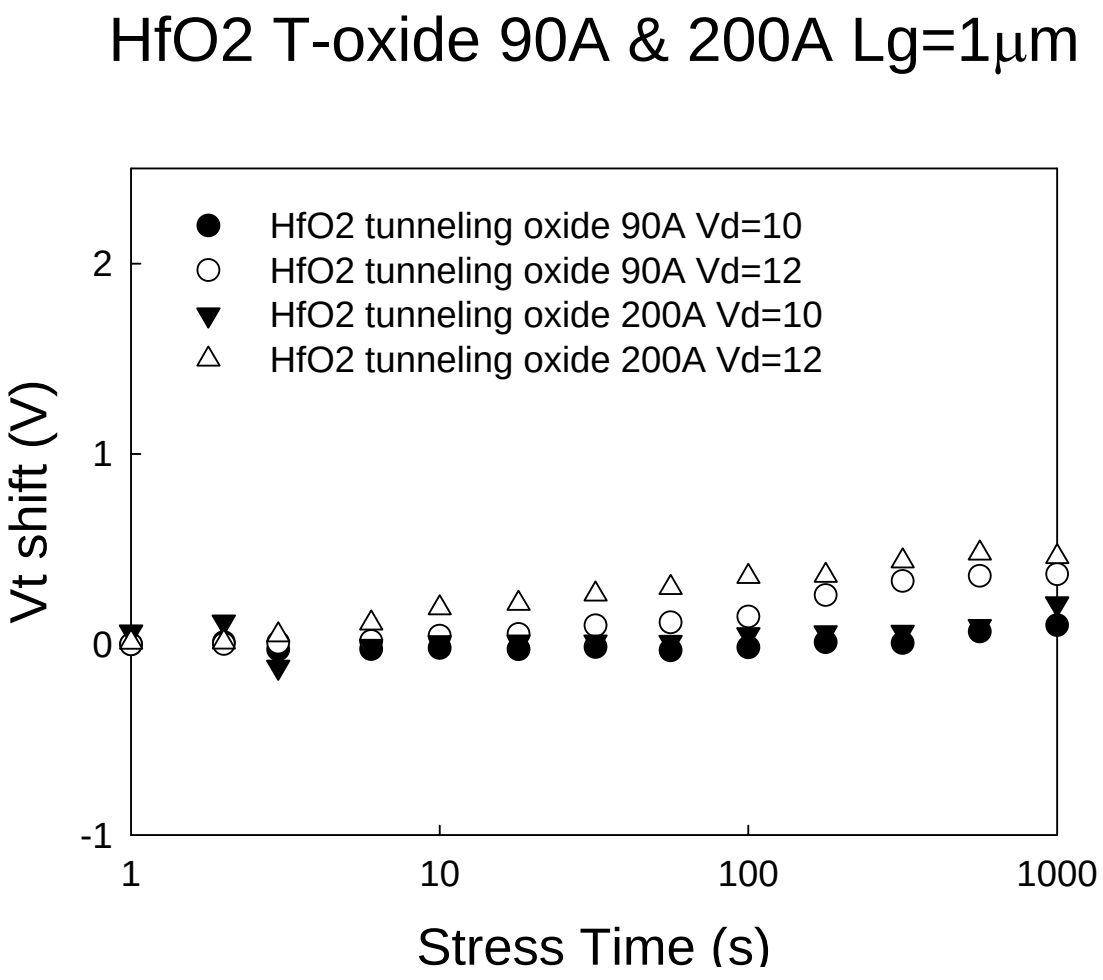

Fig. 4-4 (a) Programming drain disturb characteristics of HfO_2 poly-Si TFT memory with different tunneling oxide thickness and voltages.

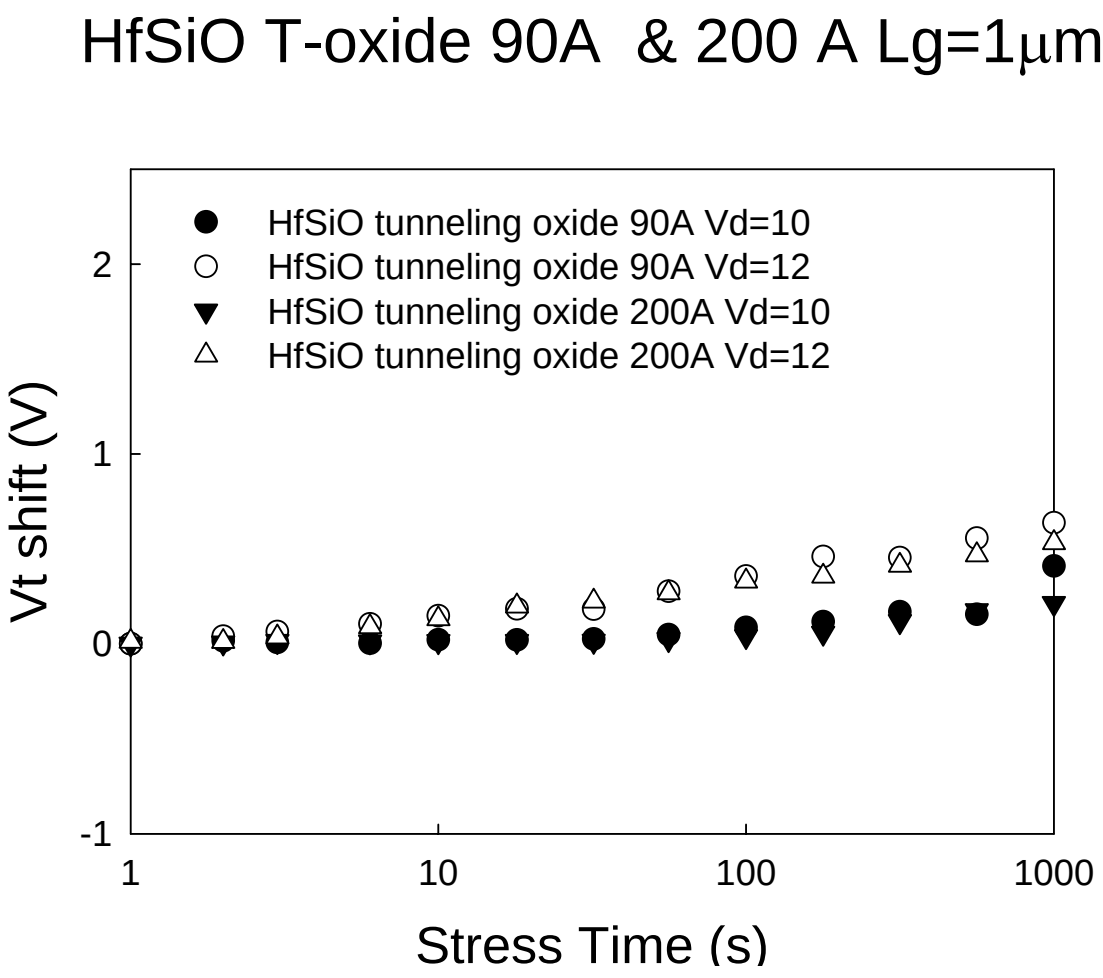

Fig. 4-4 (b) Programming drain disturb characteristics of Hf-silicate poly-Si TFT memory with different tunneling oxide thickness and voltages.

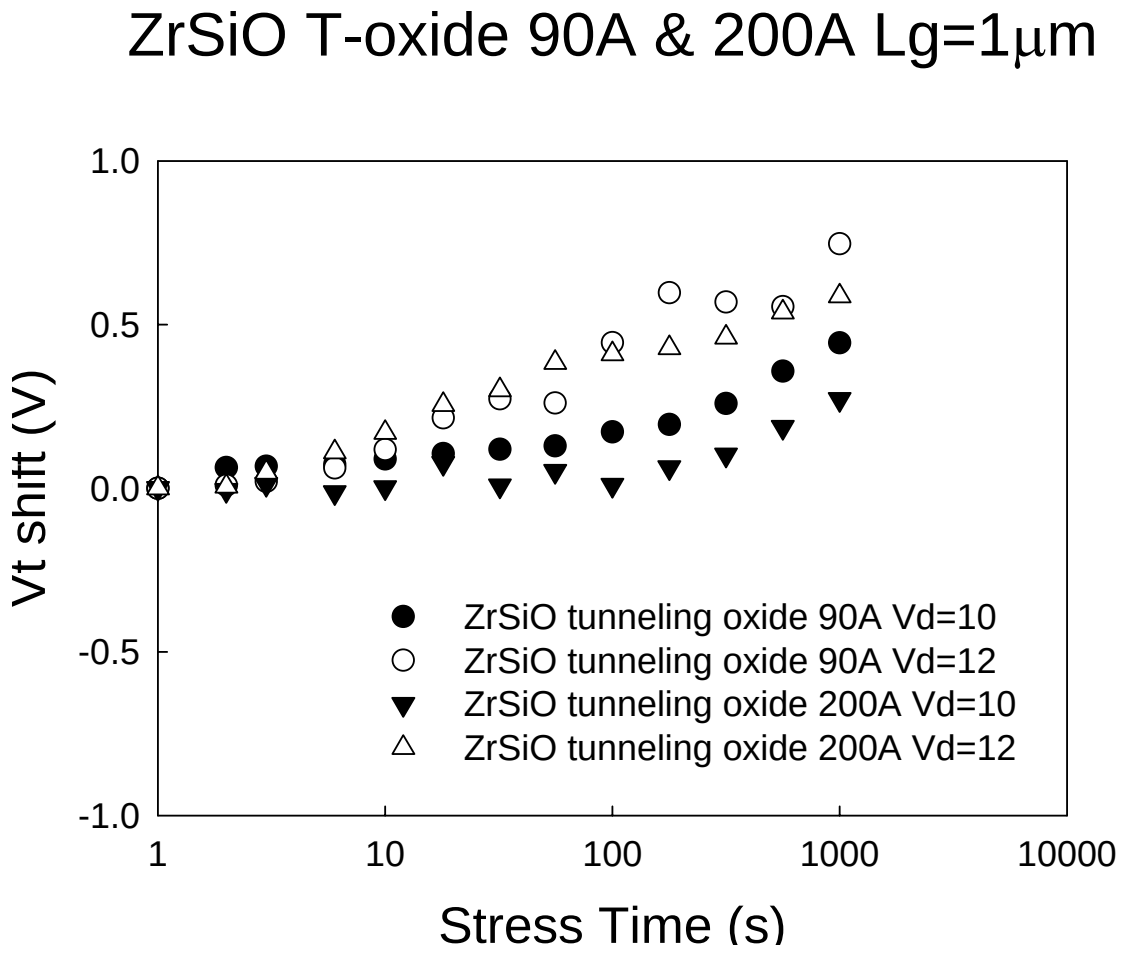

Fig. 4-4 (c) Programming drain disturb characteristics of Zr-silicate poly-Si TFT memory with different tunneling oxide thickness and voltages.

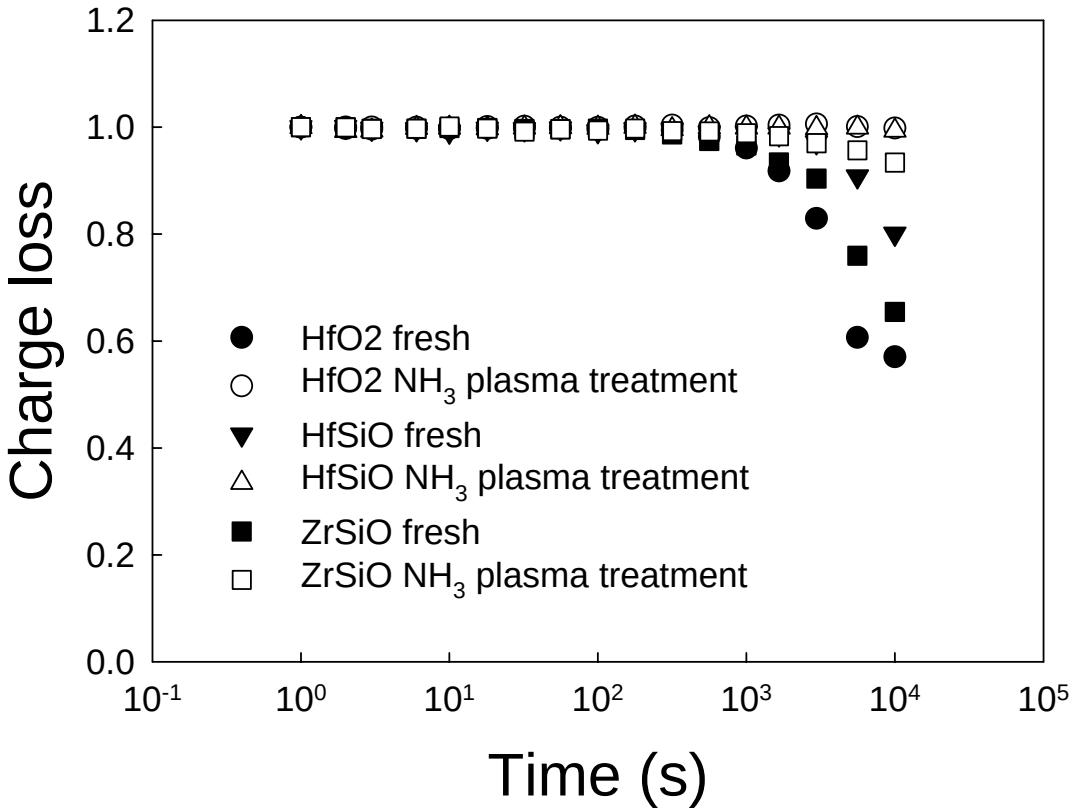

Fig. 4-5 The data retention behavior of the TFT flash memory with and without NH_3 plasma treatment.

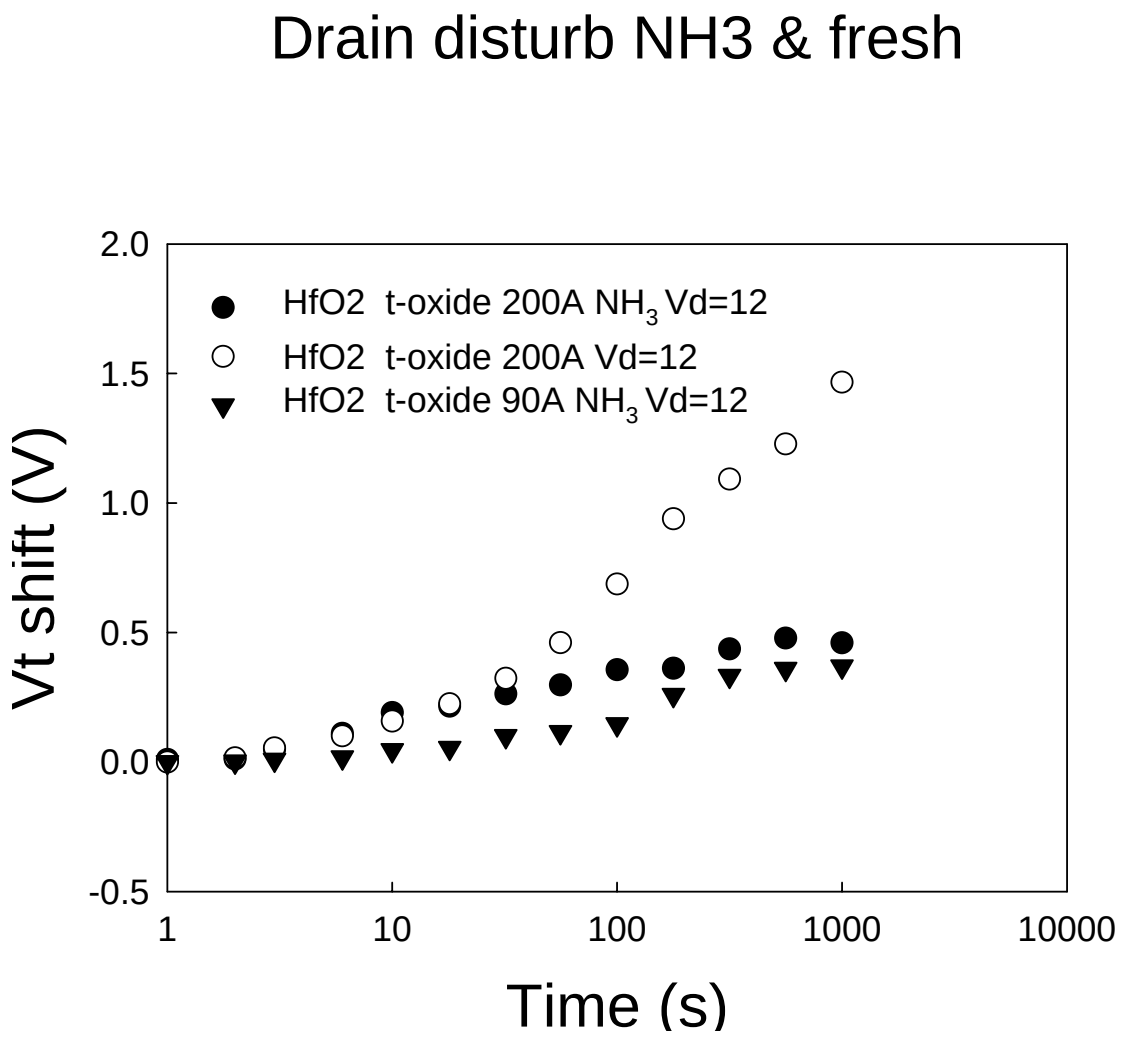

Fig. 4-6 (a) Programming drain disturb characteristics of HfO_2 poly-Si TFT memory with different tunneling oxide thickness and NH_3 plasma treatment.

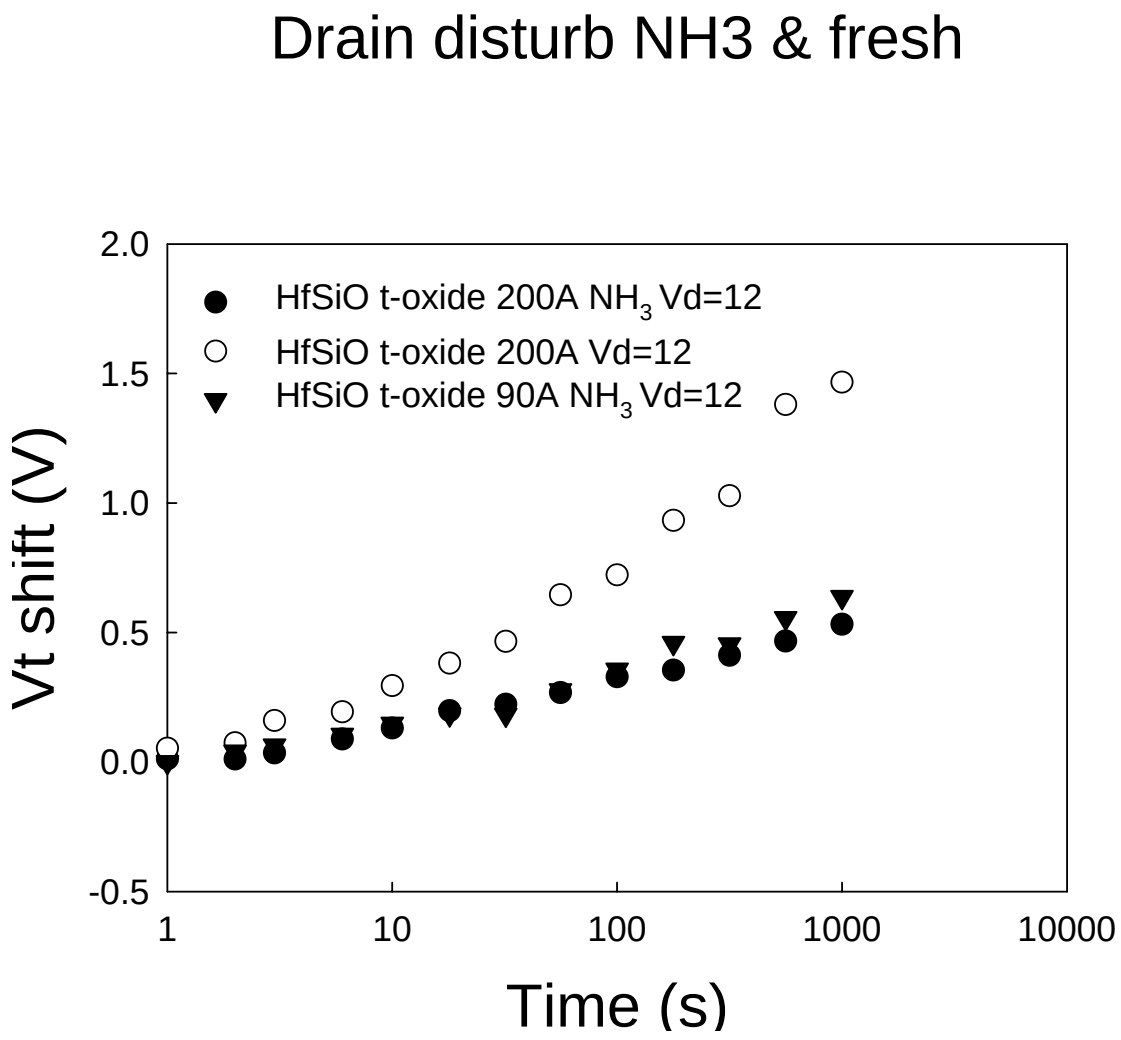

Fig. 4-6 (b) Programming drain disturb characteristics of Hf-silicate poly-Si TFT memory with different tunneling oxide thickness and NH_3 plasma treatment.

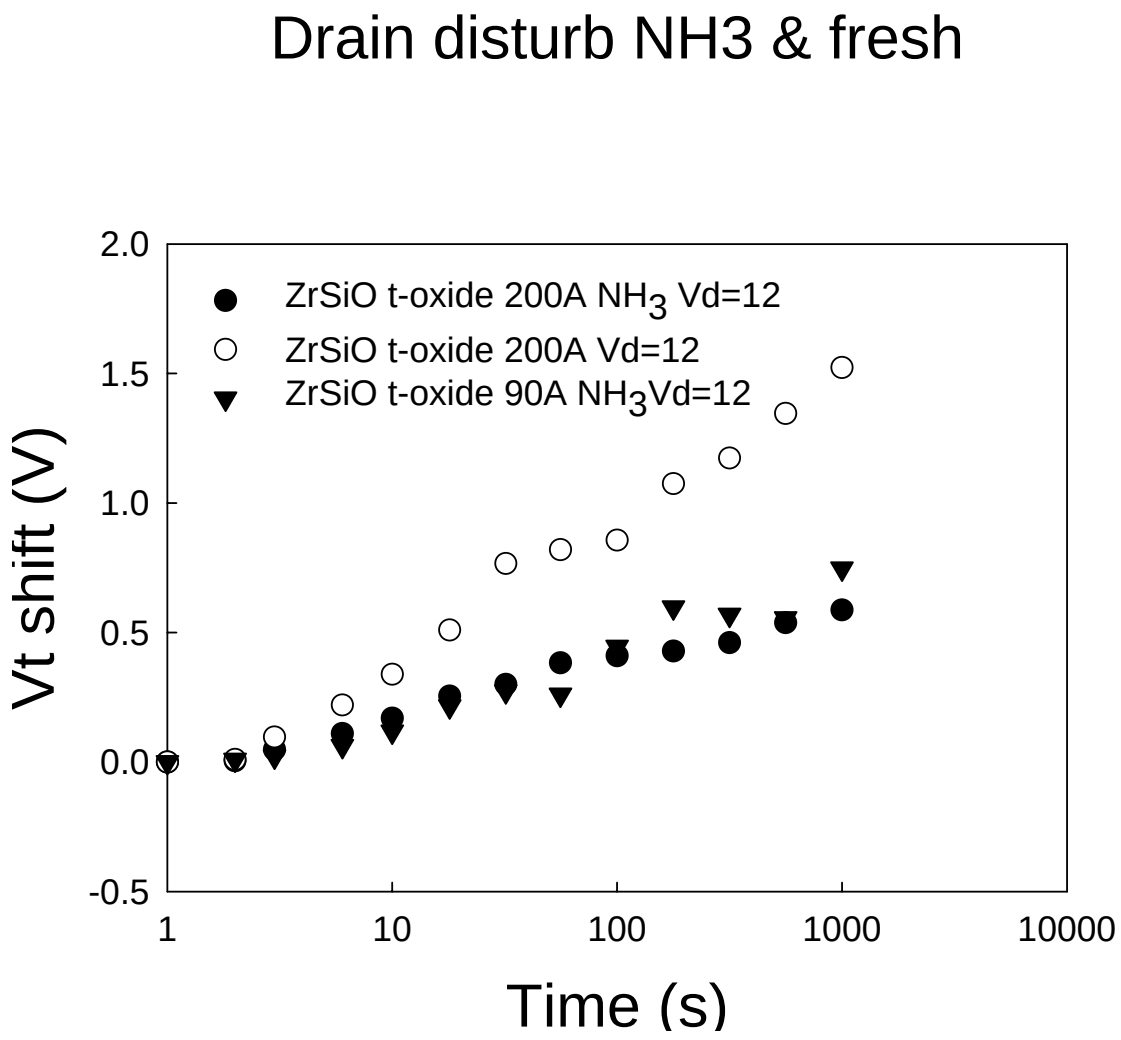

Fig. 4-6 (c) Programming drain disturb characteristics of Zr-silicate poly-Si TFT memory with different tunneling oxide thickness and NH_3 plasma treatment.

Chapter 5

Conclusion

In this thesis, we have studied three kinds of high-k dielectrics, including HfO_2, Hf-silicate and Zr-silicate as the trapping layer for the poly-Si TFT memory devices. By sticking with sufficiently low thermal-budget processing, we have successfully demonstrated the feasibility of fabricating nonvolatile poly-Si TFT flash memories with excellent characteristics ：

(1) The TFT flash memory device with Zr-silicate trapping layer has a window of 5 V while the applied gate bias at 12 V and applied drain bias at 12 V. This means the device in this experiment has a large memory window.

(2) The TFT flash memory device with HfO_2 trapping layer has a good program/erase speed of 0.1 ms while the applied gate bias at 10 V and applied drain bias at 10 V.

(3) The long retention time was also shown in the TFT flash memory device with HfO_2 and Hf-silicate trapping layers. There are not obvious threshold voltage shift for our device during 10000 s measuring.

(4) For the endurance performance in the TFT flash memory device, the P/E window of the device remains about 3 V during 10^5 P/E cycling.

However the drain disturb and gate disturb are still problems in TFT flash memories. Because the drain and gate stress will bring the localized traps along the grain boundaries and interface in the channel, which can significantly affect the Vt shift. This is because the hydrogen atoms of NH_3 can terminate dangling bonds and replace the weak bonds in the grain boundaries and SiO_2/poly-Si interface and thus reduce the trap states in the poly-Si channel. Thus, both the performance and reliability of poly-Si TFTs were also improved. As long as the drain and

gate disturb can be reduced, the TFT flash memories are very promising for future flash memory products.

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論文題目：

高介電常數材料之低溫複晶矽快閃記憶體的研究

Low Temperature Polycrystalline Silicon Thin-Film Flash Memory with High-k Material

指導教授：趙 天 生