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Single-electron effects in non-overlapped multiple-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors

W Lee and P Su

Department of Electronics Engineering, National Chiao Tung University, 1001 University Road, Hsinchu City, 300, Taiwan, Republic of China

E-mail: pinsu@faculty.nctu.edu.tw

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Abstract

This paper systematically presents controlled single-electron effects in multiple-gate silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) with various gate lengths, fin widths, gate bias and temperature. Our study indicates that using the non-overlapped gate to source/drain structure as an approach to the single-electron transistor (SET) in MOSFETs is promising. Combining the advantage of gate control and the constriction of high source/drain resistances, single-electron effects are further enhanced using the multiple-gate architecture. From the presented results, downsizing multiple-gate SOI MOSFETs is needed for future room-temperature SET applications. Besides, the tunnel barriers and access resistances may need to be further optimized. Since the Coulomb blockade oscillation can be achieved in state-of-the-art complementary metal-oxide-semiconductor (CMOS) devices, it is beneficial to build SETs in low-power CMOS circuits for ultra-high-density purposes.

1. Introduction

A single-electron transistor (SET) consists of a conducting island connected to two electron reservoirs through tunnel barriers [1]. When the size of the island as well as its capacitances is scaled sufficiently small, the conductivity is determined by a single charge and shows periodicity. Many studies in the past [1–7] have pointed out that SET is a promising candidate for ultra-low-power and ultra-high-density circuit systems in the next generation [2, 3]. In particular, the SET with a standard silicon nanoelectronics process and compatible with existing complementary metal-oxide-semiconductor (CMOS) device architectures is very attractive. Although various novel silicon-based SETs have been reported for superior room-temperature performance and functionality [4–6], it is difficult for these SETs to be compatible with state-of-the-art CMOS devices.

A direct way to realize CMOS-compatible SETs is raising the Coulomb blockade effects [7] in real CMOS devices. The key parameter is the constriction of carriers. In [8], one approach of electronic confinement, using the non-overlapped-gate architecture as tunnel barriers, has been employed to produce controlled single-electron effects in real planar metal-oxide-semiconductor field-effect transistors (MOSFETs). In [9], electronic confinement by means of high access resistances (i.e. source/drain resistances) yields Coulomb blockade oscillation (CBO) in ultra-thin silicon-on-insulator (SOI) MOSFETs. Although both studies represent attractive schemes to build SETs on large-scale wafers, the charging energy is small (less than about 6 mV) and is not suitable for room-temperature applications. To allow high-temperature operation, the size of the dots needs to be reduced. Therefore, the purpose of this work is to explore further into combining more than one approach in ultra-scaled CMOS devices.

Since multiple-gate SOI MOSFETs are considered as a promising candidate for ultra-scaled CMOS [10], we have conducted an assessment of single-electron effects in these devices near room temperature [11]. The CBO reported in [11] is associated with the presence of tunnel barriers in spacer-defined non-overlapped gate to source/drain regions. Besides, high source/drain resistances in narrow multiple-gate devices

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further facilitate the constriction of carriers. To the best of our knowledge, it is the first demonstration of single-electron effects in multiple-gate SOI MOSFETs with non-overlapped gate to source/drain structures at room temperature. We have also noted that similar ideas have been reported in [23, 24] after our study [11].

In this work, we further demonstrate controlled single-electron effects in these devices through a comprehensive investigation of the observed CBO, which can be modulated by geometry and applied bias. Moreover, the roles of access resistances [9] and the gate–dot coupling strength [12] are assessed. The organization of this paper is as follows. In section 2, we describe our device structure which features the non-overlapped architecture. In section 3, we systematically present single-electron effects for devices with various gate lengths (L_g), fin widths (W_{fin}), gate bias (V_{GS}) and temperature. Then, the impact of access resistances [9], the estimation of gate–dot coupling strength [12] and phenomena of split-peak separations are discussed in section 4. Finally, the conclusion will be drawn in section 5.

2. Devices

Figure 1(a) shows the schematic view of the multi-gate SOI MOSFETs investigated in this study. Our devices were fabricated on separation by implantation of oxygen (SIMOX) SOI wafers using standard CMOS optical lithography [13]. The Si body thickness, H_{fin}, was thinned down to about 40 nm by thermal oxidation. The fin width, W_{fin}, was defined by wet etching and is about 15 and 25 nm. After W_{fin} was developed, the Si-body fin was doped with B^+ with a doping concentration, N_B, about 6×10^{18} cm^{-3}. Afterward the 1.6 nm gate oxide was thermally grown. The ultra-thin gate oxide contributes to not only the suppression of short-channel effects, but also the gate–dot coupling strength of the SET [12]. The *in situ* heavily doped N^+ poly-silicon was subsequently deposited. Using optical lithography and anisotropic reactive ion etching, the gate length, L_g, was defined and ranges from 30 to 60 nm. Without the light-doping-drain/source (LDD/LDS) implantation, the composite spacer of silicon oxide and nitride was deposited and anisotropically etched. Finally, heavily doped N^+ source/drain was made. It is worth noting that all the processes are essentially the same as in traditional CMOS technologies.

The main feature of our device structure is the non-overlapped gate to source and drain regions, which are defined by spacers, as depicted in figure 1(b). With increasing gate voltage, there is a larger carrier concentration under the gate electrode than in the non-overlapped regions (figure 1(c)). In other words, the non-overlapped regions separate inverse carriers from the source/drain and act as the electrostatic tunnel barriers of the single-electron tunneling [8]. It is worth noting that the size of tunnel barriers depends on the non-overlapped regions as well as the spacers. Optimum tunnel barriers can be controlled through modulating the width of spacers. In addition, the high source/drain resistances that are intrinsic to the multiple-gate SOI structure are useful for the constriction of carriers [9].

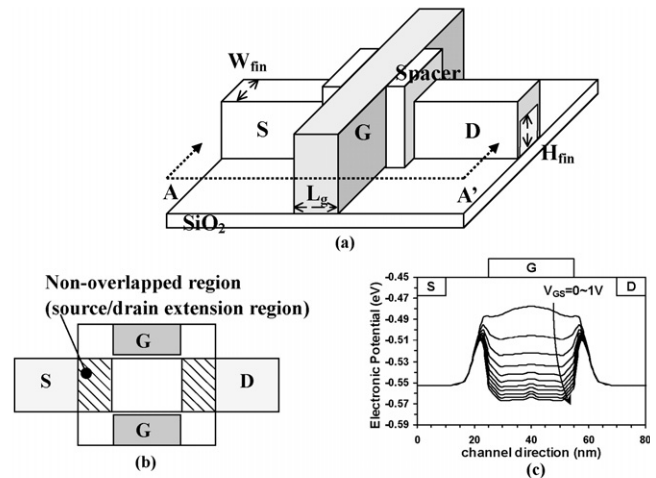

Figure 1. Multiple-gate FinFET SOI structure investigated in this work and (b) its cross-sectional view along A–A′, showing the non-overlapped gate to source/drain regions. (c) A schematic electronic potential plot along the channel between source and drain for the FinFET with non-overlapped regions.

3. Experimental data

In this section we analyze the features of periodic oscillations in G_m ($=dI_D/dV_{GS}$). DC current–voltage measurements (I_D–V_{GS}) were carefully performed using the Agilent 4156C precision semiconductor parameter analyzer in low-noise probe stations. Experiments on the multiple-gate device with $L_g = 30$ nm and $W_{fin} = 25$ nm at different temperatures are described in section 3.1. The geometry dependence and the V_{GS} dependence are analyzed in sections 3.2 and 3.3, respectively.

3.1. Single-electronic effects in multiple gate MOSFETs

Figure 2(a) shows the G_m–V_{GS} characteristics measured at room temperature ($T = 20\,°$C) for device 1 with $L_g = 30$ nm and $W_{fin} = 25$ nm. Periodic oscillations, an indication of the CBO [14], in the G_m–V_G characteristics can be seen. Such periodic oscillations in G_m can be reproduced for device 2 with the same size, as shown in figure 2(b). It is worth noting that the peaks of each period may be repeated at the same gate bias. For devices with large dimensions under the same measurement system, nevertheless, only the thermal noise can be seen. Therefore, the effect of equipment, such as the effect of source accuracy [15], is not responsible for the observed periodic oscillations. We have also noticed that the channel conductance ($G_{DS} = dI_D/dV_{DS}$) is of the same order of magnitude as e^2/h ($\sim 3.87 \times 10^{-5}$ S), which has been considered as one of the most important criteria for the CBO [1, 9].

Figure 3(a) shows the oscillating components, $G_m - \langle G_m \rangle$, for the data in figure 2(a). The period, ΔV_G, can be observed to be $\sim$17 mV. When the temperature decreases from 293 to 233 K, as shown in figure 3(b), the oscillations are reproducible with the same period. To further analyze the periodic oscillations, both the discrete fast Fourier transform

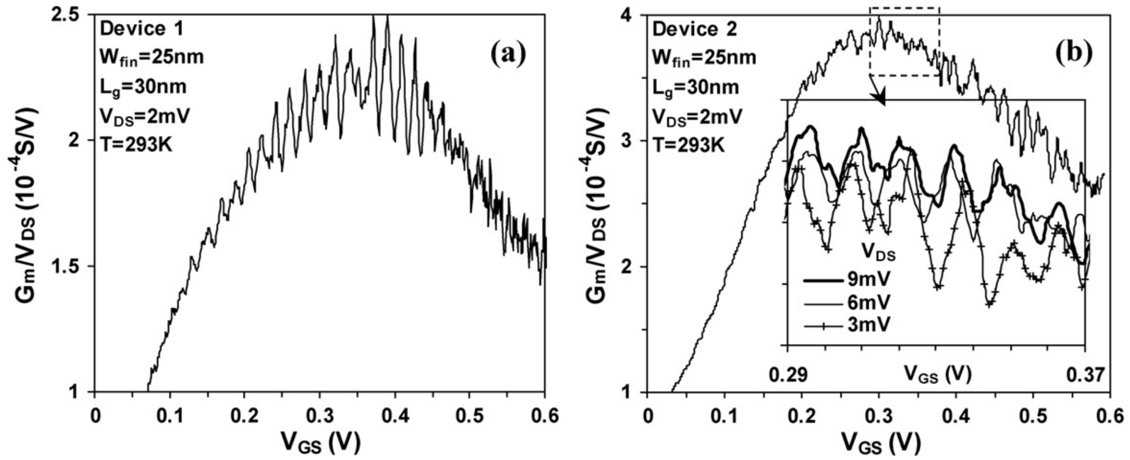

Figure 2. Periodic oscillations occur in G_m/V_{DS} versus V_{GS} characteristics for (a) device 1 and (b) device 2 with $L_g = 30$ nm and $W_{fin} = 25$ nm at $T = 293$ K.

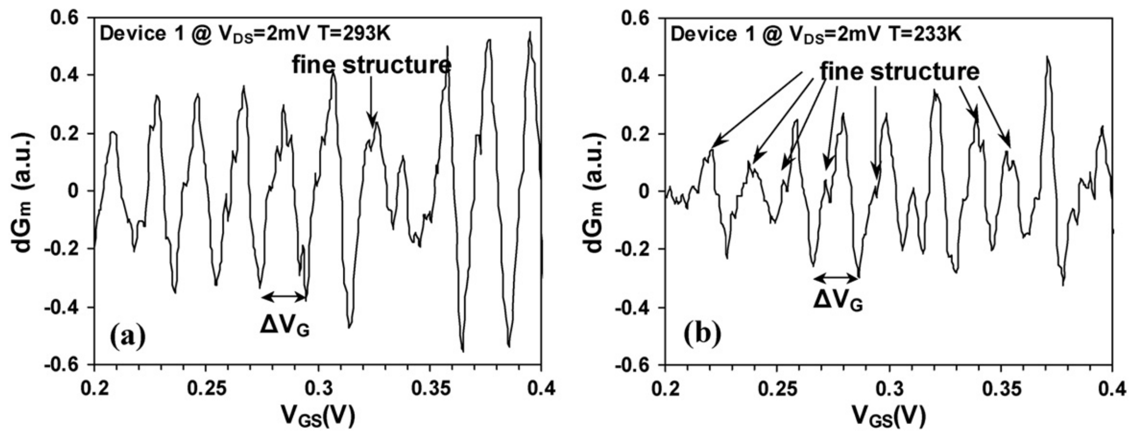

Figure 3. Periodic oscillations occur in dG_m ($= G_m - \langle G_m \rangle$) versus V_{GS} characteristics for device 1 at (a) $T = 293$ K and (b) $T = 233$ K. $\langle G_m \rangle$ is the long-range average.

(FFT) [16] and the histogram of the directly counted peak-to-peak spacing (ΔV_G) [8, 9] can be applied. It can be confirmed from figure 4 that the observed conductance oscillations in figure 3 follow a Gaussian distribution [8, 17–19] with a mean period ($\langle \Delta V_G \rangle$) $\sim$17 mV and a standard deviation (sd) $\sim$3.5 mV. The normalized width of the distribution [8], sd/$\langle \Delta V_G \rangle$, is about 0.2. Similar results have also been obtained in [8] for single-electron effects in planar bulk MOSFETs with the non-overlapped-gate architecture. The Gaussian shape of the ΔV_G distribution has been explained in terms of the charging energy level dynamics due to shape deformation of the quantum dot [17, 18]. In other words, the shape of the quantum dot in our device is not fixed and is deformed by V_{GS}, which can be understood from the simulated V_{GS}-controlled tunnel barriers shown in figure 1(c).

3.2. L_g & W_{fin} dependence

The period of G_m oscillations, $\langle \Delta V_G \rangle$, represents the charging energy and is related to the gate capacitance by e/C_g [1]. For our multiple-gate devices, the gate capacitance C_g is associated with the effective gate area A_{eff} (i.e. $2H_{fin}L_g$). Therefore, we expect that the period $\langle \Delta V_G \rangle$ decreases as L_g increases. Figure 5 shows the G_m–V_{GS} characteristics for device 3 with $L_g = 40$ nm and $W_{fin} = 25$ nm at $T = 20\,^{\circ}$C. The phenomenon of G_m oscillation can still be observed with $\langle \Delta V_G \rangle \sim 15$ mV. Compared with the 17 mV period for devices 1 and 2 with $L_g = 30$ nm, the decreased $\langle \Delta V_G \rangle$ represents the C_g dependence of single-electron effects. Furthermore, such L_g dependence indicates that the quantum dot in our devices is determined by the tunnel barriers of the non-overlapped regions rather than the disordered potential landscape demonstrated in the multi-gate SOI structures of [20].

Figures 6(a)–(c) show oscillating components corresponding to $V_{GS} = 0$–0.2, 0.2–0.4 and 0.4–0.6 V, respectively, for device 4 with $L_g = 40$ nm and $W_{fin} = 15$ nm. From the FFT shown in figure 6(d), we obtain the period ranging from 13 to 10 mV. It is interesting that, although the period is smaller compared with the 15 mV period for device 3 with $W_{fin} = 25$ nm, the phenomenon of G_m oscillation is clearer than that of device 3 (figure 5). The decreased $\langle \Delta V_G \rangle$ for $W_{fin} = 15$ nm may be attributed to the increase of the gate–dot coupling strength, α, which is the ratio between the gate capacitance and the total

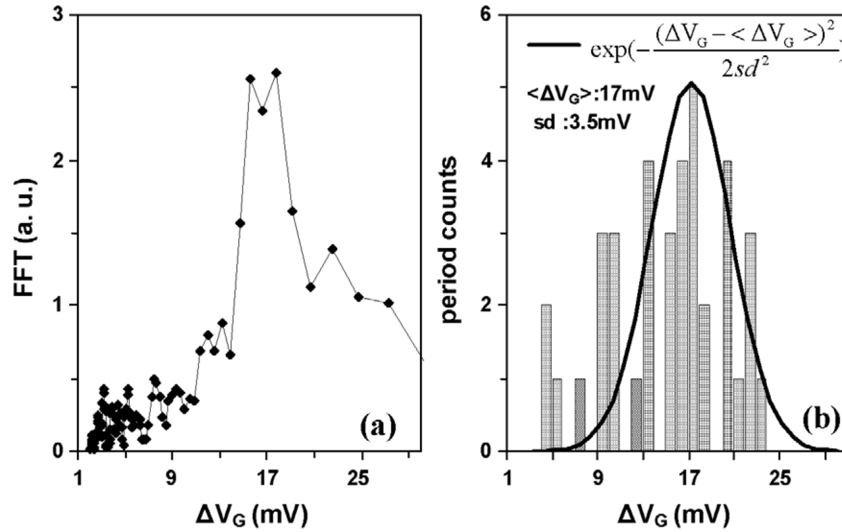

Figure 4. Both (a) the FFT and (b) the histogram of the directly counted peak-to-peak spacing (ΔV_G) confirm that the period ($\langle \Delta V_G \rangle$) in figure 3 is 17 mV.

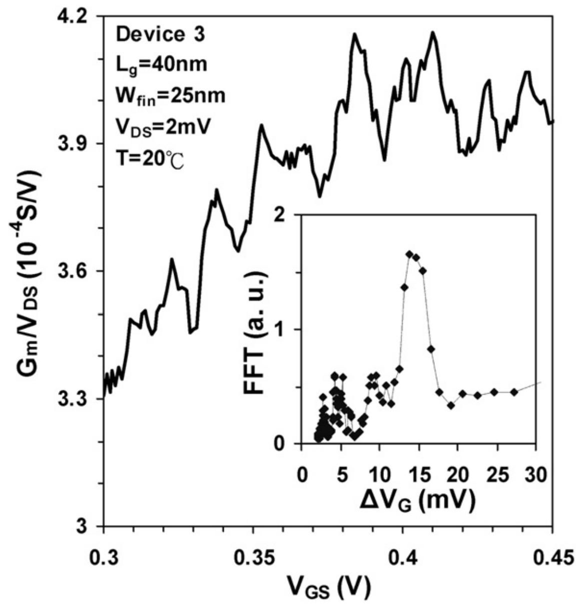

Figure 5. Periodic oscillations occur in G_m/V_{DS} versus V_{GS} characteristics for device 3 with $L_g = 40$ nm and $W_{fin} = 25$ nm at $T = 20\,^\circ$C. Smaller peak-to-peak spacing ($\Delta V_G = 15$ mV) from the FFT can be seen.

capacitance, C_g/C_Σ, and accounts for a portion of the period as [2]

$$\Delta V_G = \frac{C_\Sigma}{C_g}\left(\frac{\Delta\varepsilon}{e}\right) + \frac{e}{C_g}, \tag{1}$$

where $\Delta\varepsilon$ is an average discrete energy spacing in the semiconductor. The stronger gate–dot coupling strength [12] can also further control the leakage current and thus make the conductance oscillations more distinguishable. In addition, when the W_{fin} of multiple-gate devices is reduced, the source/drain resistances increase. Therefore, the carrier is further constricted [9].

3.3. V_{GS} dependence

It is also worth noting in figure 6 that the period of G_m oscillation decreases from 13 to 10 mV when V_{GS} increases from 0 to 0.6 V. For other devices, we can also observe the decreased period with increasing V_{GS}. From (1), we know that ΔV_G is inversely proportional to the gate capacitance C_g, which is associated with the size of dots. Therefore, such V_{GS} dependence of ΔV_G (i.e. ΔV_G decreases as V_{GS} increases) indicates that the size of the quantum dot increases with V_{GS}. The V_{GS} modulated tunnel barriers, as shown in figure 1(c), may account for the V_{GS} dependence of ΔV_G. It is noteworthy that the V_{GS} dependence of the period reveals a possibility of single SET with multiple periods, which may enhance the functionality of SETs.

4. Discussions

We have noted in figure 3(a) that the fine structure of split-peak phenomena occurs at G_m oscillating peaks. As the temperature is decreased from 293 to 233 K, the fine structure becomes clear and is almost reproduced at all peaks (figure 3(b)). To investigate these split-peak phenomena, we performed low-temperature measurements ($T = 56$ K) for device 5 with $L_g = 30$ nm and $W_{fin} = 25$ nm (figure 7(b)). Compared with the high-temperature results in figure 7(a), the fine structure can be clearly seen at $T = 56$ K and $V_{DS} = 0.2$ mV in figure 7(b). One model considering excitation energy levels in the SET operation [3] may explain the fine structure. The excitation energy levels can be observed as long as the carrier energy is larger than the discrete energy spacing $\Delta\varepsilon$ (i.e. $eV_{DS} + K_B T > \Delta\varepsilon$) [21]. An important characteristic for the effect of excitation energy levels is that the number of splitting peaks increases with V_{DS} [21, 22]. To verify this feature, we measured G_m oscillations for device 6 with $L_g = 40$ nm and $W_{fin} = 25$ nm at $V_{DS} = 0.3$ and 10 mV, respectively, under $T = 56$ K. For $V_{DS} = 0.3$ mV in figure 8(a), the fine structure

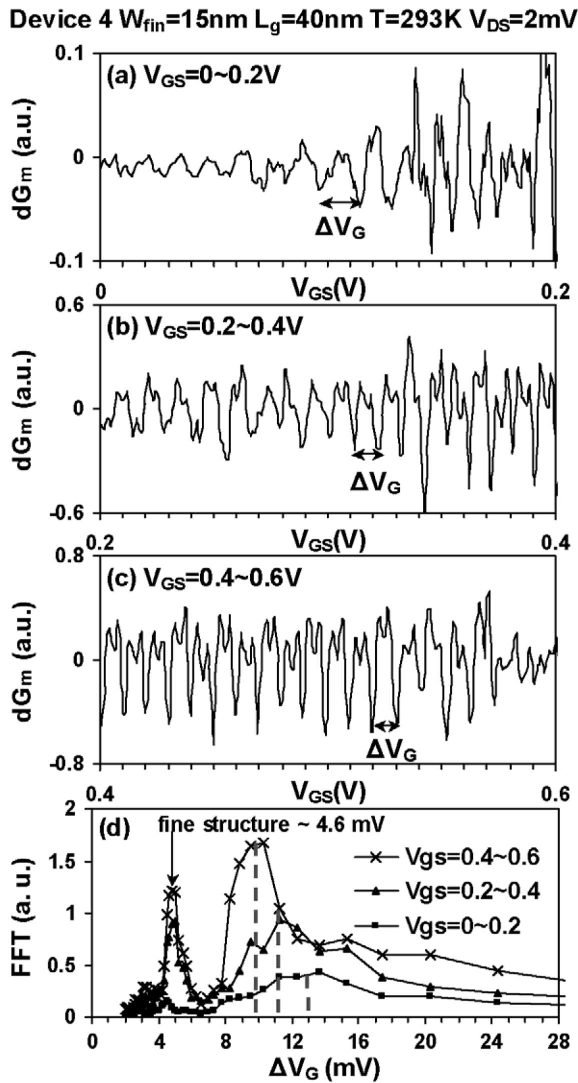

Figure 6. Periodic oscillations occur in dG_m versus V_{GS} characteristics for device 4 with $L_g = 40$ nm and $W_{fin} = 15$ nm at (a) $V_{GS} = 0$–0.2 V, (b) $V_{GS} = 0.2$–0.4 V and (c) $V_{GS} = 0.4$–0.6 V. (d) The FFT of periodic oscillations in different V_{GS} regimes.

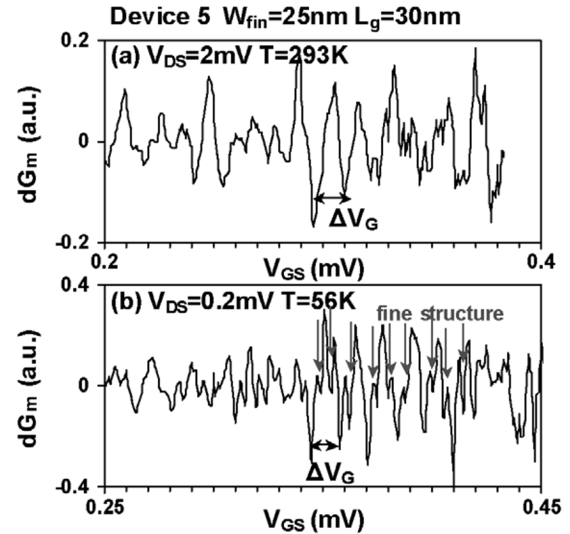

Figure 7. Periodic oscillations occur in dG_m versus V_{GS} characteristics for device 5 with $L_g = 30$ nm and $W_{fin} = 25$ nm at (a) $T = 293$ K and (b) $T = 56$ K.

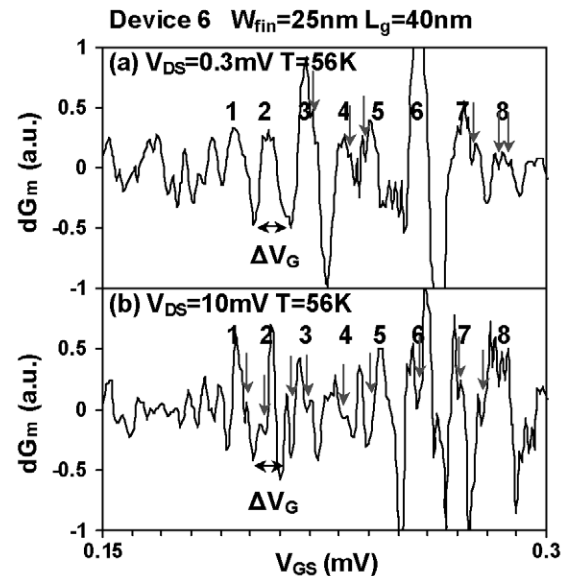

Figure 8. Periodic oscillations occur in dG_m versus V_{GS} characteristics for device 6 with $L_g = 40$ nm and $W_{fin} = 25$ nm at (a) $V_{DS} = 0.3$ mV and (b) $V_{DS} = 10$ mV under $T = 56$ K.

can be seen on a limited number of oscillating peaks. When V_{DS} increases to 10 mV in figure 8(b), we can observe the fine structure for each peak. It is worth noting in figure 8(b) as well as in figure 7(b) that single peaks may develop into triple peaks for our measurements. It implies that three excitation energy levels are available [21, 22]. When the carrier energy is further increased by $K_B T$, however, thermal fluctuation smears out the fine structure, as shown in figures 7(a), 3 and 5. It is also worth noting in figure 6 that the fine structure can be clearly observed at room temperature for device 4 with narrow W_{fin}. This result demonstrates that both the gate–dot coupling strength and the access resistances (i.e. source/drain resistance) are important for enhancing the control of single-electron effects and thus for the realization of room-temperature operation SETs.

To determine the gate–dot coupling strength α of the SET, a Coulomb blockade rhombus diagram can be used. The slopes of the diamond-shape contours are given by $C_g/(C_g + C_s)$ and $-C_g/C_d$, respectively [8]. Figure 9 shows the rhombus diagram for device 2 with $L_g = 30$ nm and $W_{fin} = 25$ nm. From the slopes in figure 9 (black lines), we obtain C_g:C_d:C_s = 9:16:13. For the other device with $L_g = 40$ nm and $W_{fin} = 25$ nm, we obtain C_g:C_d:C_s = 11:9:9 (not shown). We then calculate $\alpha = C_g/(C_g + C_d + C_s) = 0.2$–0.3. Similar results have been reported in [8] and [9]. In addition, from $mL_gC_g/A_{eff} = C_d/W_{eff}$ $(=C_s/W_{eff})$, where $m = C_d/C_g$ $(=C_s/C_g)$ and $C_g/A_{eff} = \varepsilon_{SiO_2}/\mathrm{EOT} \sim 1.33 \times 10^{-6}$ F cm^{-2}, we estimate C_d/W_{eff} (C_s/W_{eff}) to be about 0.71–0.44 (0.58–0.44) fF μm^{-1}. These extracted values are of the same order of magnitude as the measured junction capacitance data.

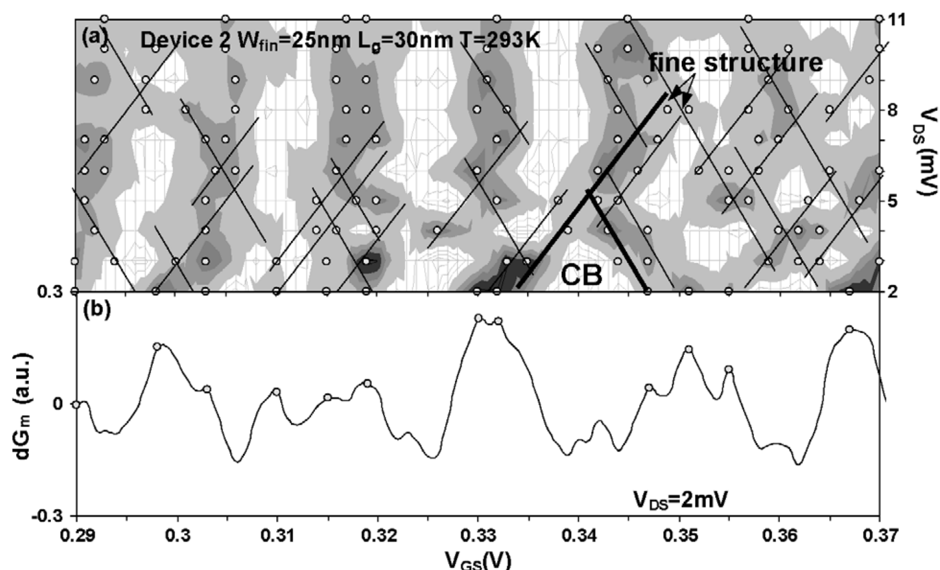

Figure 9. (a) Coulomb blockade rhombus diagram for device 2. (b) dG_m versus V_{GS} characteristics at V_{DS} = 2 mV. The conductance peaks (dots) correspond to the dots at V_{DS} = 2 mV in (a).

5. Conclusions

In summary, we have systematically investigated the controlled single-electron effects in multiple-gate SOI MOSFETs with various L_g, W_{fin}, V_{GS} and temperature. Our study indicates that using the non-overlapped gate to source/drain structure as an approach of the single-electron transistor (SET) in MOSFETs is promising. Combining the advantage of gate control and the constriction of high source/drain resistances, single-electron effects are further enhanced using the multiple-gate architecture. From the presented results, downsizing multiple-gate SOI MOSFETs is needed for future room-temperature SET applications. Besides, the tunnel barriers and access resistances may need to be further optimized. Since the Coulomb blockade oscillation can be achieved in state-of-the-art CMOS devices, it is beneficial to build SETs in low-power CMOS circuits for ultra-high-density purposes.

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