Applied Physics Letters

Improved reliability of Mo nanocrystal memory with ammonia plasma treatment

Chao-Cheng Lin, Ting-Chang Chang, Chun-Hao Tu, Wei-Ren Chen, Chih-Wei Hu, Simon M. Sze, Tseung-Yuen Tseng, Sheng-Chi Chen, and Jian-Yang Lin

Citation: Applied Physics Letters **94**, 062106 (2009); doi: 10.1063/1.3081021
View online: http://dx.doi.org/10.1063/1.3081021
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/94/6?ver=pdfcov
Published by the AIP Publishing

Improved reliability of Mo nanocrystal memory with ammonia plasma treatment

Chao-Cheng Lin,[1] Ting-Chang Chang,[2,a)] Chun-Hao Tu,[1] Wei-Ren Chen,[1] Chih-Wei Hu,[1] Simon M. Sze,[1] Tseung-Yuen Tseng,[1] Sheng-Chi Chen,[3] and Jian-Yang Lin[3]
[1]*Institute of Electronics, National Chiao Tung University, Hsin-Chu 300, Taiwan*
[2]*Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, 70 Lien-hai Road, Kaohsiung 804, Taiwan*
[3]*Department of Opto-Electronic Engineering, National Yunlin University of Science and Technology, Yunlin 64002, Taiwan*

(Received 11 December 2008; accepted 23 January 2009; published online 12 February 2009)

We investigated ammonia plasma treatment influence on the nonvolatile memory characteristics of the charge storage layer composed of Mo nanocrystals embedded in nonstoichiometry oxide (SiO_x). X-ray photoelectron spectra analyses revealed that nitrogen was incorporated into the charge storage layer. Electric analyses indicated that the memory window was reduced and the retention and the endurance improved after the treatment. The reduction in the memory window and the improvement in retention were interpreted in terms of the nitrogen passivation of traps in the oxide around Mo nanocrystals. The robust endurance characteristic was attributed the improvement of the quality of the surrounding oxide by nitrogen passivation. © *2009 American Institute of Physics*.
[DOI: 10.1063/1.3081021]

Nanocrystals embedded in dielectric as a charge storage layer of the floating gate structure attracted much attention for next generation nonvolatile memory. Employing discrete nanocrystals is expected to suppress charge loss due to lateral migration in poly-Si floating gate.[1,2] Nanocrystals have been fabricated by several methods such as ion implantation,[3,4] sputtering,[5,6] and oxidation.[7,8] It is expected that those processes can induce defects or traps in the oxide around nanocrystals during the fabrication process. The induced deficiency in the surrounding oxide can lead to stored charges leaking out of the nanocrystals through trap assisted tunneling.[9,10] Therefore, the quality of the surrounding oxide is an important issue to nanocrystal memory.

In this study, we investigated the effect of ammonia (NH_3) plasma treatment on memory characteristics of Mo nanocrystal memory.[11] The NH_3 plasma treatment technique has been investigated to improve the quality of gate dielectric.[12,13] Our experimental results show that the memory characteristics were influenced by incorporation of nitrogen into the surrounding oxide.

The memory cells were fabricated on 6 in. *p*-type Si substrate. After the substrate was cleaned with standard Radio Corporation of America process, a 5-nm-thick dry oxide was thermally grown at 950 °C on the substrate in a horizontal furnace. An 8-nm-thick Mo silicate layer was subsequently deposited on the oxide layer by cosputtering Mo and Si in Ar (24 SCCM)/O (2 SCCM) (SCCM denotes cubic centimeter per minute at STP) ambience. A 30-nm-thick Si oxide as the control oxide was deposited on the Mo silicate layer by plasma enhanced chemical vapor deposition (PECVD) at 300 °C. Thermal annealing process was performed in N_2 ambience at 900 °C at 60 s to form Mo nanocrystals embedded in SiO_x. Cells were then treated with NH_3 plasma in PECVD chamber for 30 min with a NH_3 gas flow rate of 20 SCCM and the chamber pressure of 67 torr at power of 50 W. To measure the electric characteristics, a 500-nm-thick Al was thermally evaporated through a shadow mask on the control oxide to form the metal-oxide-semiconductor (MOS) structure. The x-ray photoemission spectroscopy (XPS) was adopted to analyze the chemical bonding and composition of the charge storage layer. Electrical characteristics were measured using Keithley4200 and HP4284 Precision *LCR* meter.

Figure 1 shows the XPS spectra of the charge storage layer with and without the plasma treatment, which was performed by using a monochromatic Al $K\alpha$ (1486.6 eV) x-ray. Figure 1(a) shows the XPS Si 2*p* spectra of the charge storage for the sample with and without the plasma treatment. For the sample without the treatment in Fig. 1(a), the peak position of XPS Si 2*p* situated at 102.9 eV indicates that the surrounding oxide of nanocrystals is SiO_x.[14] There is no obvious difference in the peak positions between the samples with and without the treatment. However, it was found that an additional XPS peak (397.8 eV) appears in the Mo 3*p* and N 1*s* spectra of the charge storage layer after the plasma treatment, which indicates that the incomplete bonds in SiO_x

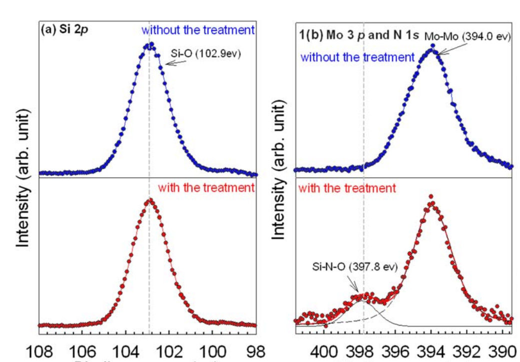

FIG. 1. (Color online) (a) Si 2*p*, (b) Mo 3*p*, and N 1*s* core-level spectra of the charge storage layer composed of Mo nanocrystals embedded in SiO_x with and without the plasma treatment.

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw.

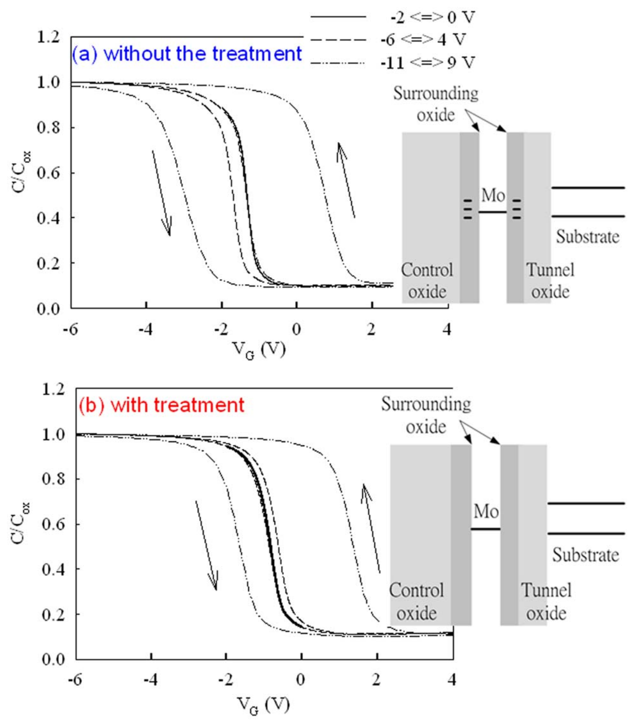

FIG. 2. (Color online) *C-V* curves of the MOS structure with and without the plasma treatment. The inset of the is the simple band diagram of the structure in the flat-band state.

bonded with nitrogen after the plasma treatment, as shown in Fig. 1(b).[15]

Figures 2(a) and 2(b) show the *C-V* curves of MOS structure embedded with Mo nanocrystals for the sample with and without the plasma treatment, respectively. At the smaller sweeping voltage of 2 V, there is a negligible memory window in Figs. 2(a) and 2(b) corresponding to the quasineutral state (i.e., no charge is stored in the charge storage layer under this sweeping range). At the larger sweeping voltages, there are counterclockwise memory hystereses in Fig. 2. The counterclockwise hystereses are due to carrier transport through tunnel oxide between the charge storage layer and the Si substrate. We note that the memory windows of the sample with the plasma treatment are smaller than that without the treatment. For the smaller memory window after the treatment, we speculate the nitrogen passivation in the charge storage layer. It has been suggested that the traps in the oxide around nanocrystals can capture carriers and contribute to the memory window.[16,17] According XPS results,

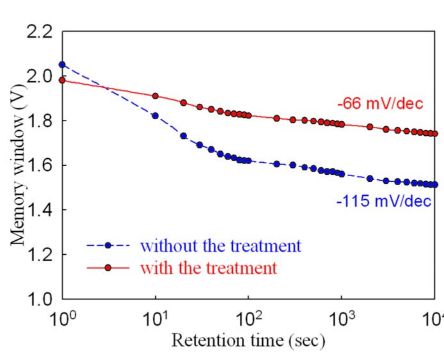

FIG. 3. (Color online) The retention behavior of the MOS structures with and without the plasma treatment.

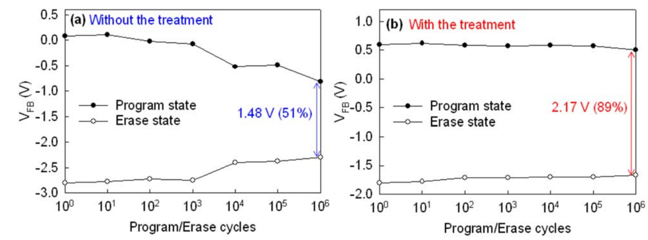

FIG. 4. (Color online) Endurance characteristic of the MOS structures (a) with and (b) without the plasma treatment.

the nitrogen was incorporated into the oxide around the Mo nanocrystals after the treatment. The incorporated nitrogen can passivate the traps in the oxide, which reduces the charge storage centers and leads to the smaller memory window, as indicated in the insets of Fig. 2.

Figure 3 is the comparison of the retention behavior for the samples with and without the plasma treatment. The retention was measured by a stress voltage of 10 V on Al gate electrode for 5 s. The memory window was obtained by comparing the *C-V* curves after the programming to the quasineutral state. It can be found in Fig. 4 that, after the 10^3 s retention time, the decay rate (−66 mV/decade) of the memory window for the sample with the plasma treatment is slower than that without the treatment (−115 mV/decade). The superior retention of the sample with the treatment can be explained by the nitrogen passivation of the traps in the oxide around Mo nanocrystals. When charges are stored in the nanocrystals, the stored charges can escape with the assistance of traps (traps assist tunneling) in the surrounding oxide. Because the traps in the oxide were reduced after the plasma treatment, the retention was improved by suppressing the trap assisted tunneling process.

Figures 4(a) and 4(b) presents the endurance characteristics of the samples with and without plasma treatment under the pulse conditions of $V_G = \pm 15$ V for 1 ms, respectively. In Fig. 4(a), the ΔV_{FB} (the difference in V_{FB} between programming and erase states) reduced significantly, and the ΔV_{FB} remained 51% after 10^6 program/erase cycles. However, the plasma treated sample exhibits robust endurance characteristic (ΔV_{FB} of 89% after 10^6 program/erase cycles). It is known that the ΔV_{FB} reduction during the endurance test is due to the degradation of the gate oxide.[18] The better endurance characteristics of the sample with the plasma treatment can be attributed to the improvement of quality of the surrounding oxide. During the endurance test, the carriers transport between nanocrystals and the substrate can damage the surrounding oxide, which produces more traps. Because the surrounding oxide was strengthened by the nitrogen incorporation after the treatment, the generation rate of traps reduced, resulting in the better endurance characteristic.

In conclusion, the nonvolatile memory characteristics of the Mo nanocrystals were influenced by the ammonia plasma treatment. The *C-V* hysteresis reduced to 3.0 V and retention characteristic improved with decay rate of −66 mV/decade after the plasma treatment due to the nitrogen passivation of the traps in the oxide around the nanocrystals. The incorporation of nitrogen into the charge storage layer through the NH_3 plasma treatment can strengthen the endurance characteristic of Mo nanocrystals memory.

This work was performed at the National Nano Device Laboratories, Taiwan, R.O.C. The authors acknowledge the financial support of the National Science Council (NSC) under Contract Nos. NSC 96-2221-E-009-202-MY3, NSC 96-2112-M-110-013, and NSC-97-3114-M-110-001.

[1] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, Tech. Dig.-Int. Electron Devices Meet **1995**, 521.
[2] Y. Liu, S. Tang, and S. K. Banerjee, Appl. Phys. Lett. **88**, 213504 (2006).
[3] Y.-C. King, T.-J. King, and C. Hu, IEEE Trans. Electron Devices **48**, 696 (2001).
[4] C. Y. Ng, T. P. Chen, L. Ding, M. Yang, J. I. Wong, P. Zhao, X. H. Yang, K. Y. Liu, M. S. Tse, A. D. Trigg, and S. Fung, IEEE Trans. Electron Devices **53**, 730 (2006).
[5] V. Ho, L. W. Teo, W. K. Choi, W. K. Chim, M. S. Tay, D. A. Antoniadis, E. A. Fitzgerald, A. Y. Du, C. H. Tung, R. Liu, and A. T. S. Wee, Appl. Phys. Lett. **83**, 3558 (2003).
[6] K. I. Han, Y. M. Park, S. Kim, S. H. Choi, K. J. Kim, I. H. Park, and B. G. Park, IEEE Trans. Electron Devices **54**, 359 (2007).
[7] L. W. Teo, W. K. Choi, W. K. Chim, V. Ho, C. M. Moey, M. S. Tay, C. L. Heng, Y. Lei, D. A. Antoniadis, and E. A. Fitzgerald, Appl. Phys. Lett. **81**, 3639 (2002).
[8] J. K. Kim, H. J. Cheong, Y. Kim, J. Yi, H. J. Bark, S. H. Bang, and J. H. Cho, Appl. Phys. Lett. **82**, 2527 (2003).
[9] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka, and M. M. Heyns, J. Appl. Phys. **87**, 8615 (2000).
[10] W. R. Chen, T. C. Chang, P. T. Liu, P. S. Lin, C. H. Tu, and C. Y. Chang, Appl. Phys. Lett. **90**, 112108 (2007).
[11] C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, C. W. Hu, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin, Appl. Phys. Lett. **93**, 222101 (2008).
[12] X. Zeng, X. W. Sun, J. Li, and J. K. O. Sin, Microelectron. Reliab. **44**, 435 (2004).
[13] J. R. Shallenberger, D. A. Cole, and S. W. Novak, J. Vac. Sci. Technol. A **17**, 1086 (1999).
[14] B. Gallas, C. C. Kao, S. Fisson, G. Vuye, J. Rivory, Y. Bernard, and C. Belouet, Appl. Surf. Sci. **185**, 317 (2002).
[15] Z. H. Lu, S. P. Tay, R. Cao, and P. Pianetta, Appl. Phys. Lett. **67**, 2836 (1995).
[16] C. Busseret, A. Souifi, T. Baron, S. Monfray, N. Buffet, E. Gautier, and M. N. Semeria, Mater. Sci. Eng., C **19**, 237 (2002).
[17] W. R. Chen, T. C. Chang, J. L. Yeh, S. M. Sze, C. Y. Chang, and U. S. Chen, Appl. Phys. Lett. **91**, 222105 (2007).
[18] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proc. IEEE **85**, 1248 (1997).