A Broadband and Scalable Lossy Substrate Model for RF Noise Simulation and Analysis in Nanoscale MOSFETs With Various Pad Structures

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***Abstract*—An enhanced lossy substrate model is developed with important features of broadband accuracy and scalability. The broadband accuracy is justified by a good match with open pad S-parameters measured up to 110 GHz and MOSFETs' S- and Y-parameters over 40 GHz. The proven model can accurately simulate four noise parameters ($\mathrm{NF_{min}}$, R_n, $\mathrm{Re}(Y_{\mathrm{opt}})$, and $\mathrm{Im}(Y_{\mathrm{opt}})$) and power spectral density of current noises (S_{id} and S_{ig}). The scalability has been validated over nanoscale MOSFETs with different finger numbers and adopting various pad structures (lossy, normal, and small pads). This scalable lossy substrate model attributed to two substrate *RLC* networks under the pads and transmission lines (TMLs) can consistently predict the abnormally strong finger number dependence and nonlinear frequency dependence of noise figure ($\mathrm{NF_{min}}$) revealed in devices with lossy pads. The enhanced model is useful in guiding pad and TML layouts for effective reduction of extrinsic noises and low noise design. Using a normal pad structure, the $\mathrm{NF_{min}}$ can be effectively suppressed to approach the intrinsic performance, which is nearly independent of finger numbers.**

***Index Terms*—Broadband, lossy substrate, nanoscale MOSFET, pad, RF noise, scalable.**

I. Introduction

COMPACT MOSFET model with broadband accuracy and scalability is a critical engine driving the success of RF CMOS circuit design [1]–[7]. To meet the increasing demands on low power and low noise in wireless communication using advanced CMOS technology, an accurate scalable noise model able to predict the lossy substrate noise is strongly required [7]–[9]. However, a reliable noise deembedding method for an accurate extraction of intrinsic noise remains a difficult subject and is particularly challenging for nanoscale devices on a lossy substrate. The fundamental challenge is how to measure and simulate the extrinsic noise in miniaturized devices, which are generally complicated by high-frequency coupling through the pads and transmission lines (TMLs) to the lossy substrate. A noise correlation matrix method [10] was frequently applied for noise deembedding, but the sophisticated matrices calculation sometimes suffers an abnormal fluctuation at lower noise levels and undesired deviation in frequency dependence [11], [12]. Actually, noise correlation matrix method limits itself to discrete data available from measurement and is vulnerable to data fluctuations over frequencies, which cannot be avoided in noise and S-parameter measurement. These limitations make it not applicable to noise simulation and prediction for RF circuit design.

A lossy substrate model was first developed in our previous work for simulating measured noise parameters. A lossy substrate deembedding can then be easily performed through circuit simulation for a reliable extraction of the intrinsic noises [13]–[15]. The accuracy has been checked in RF MOSFETs with various finger numbers and operation under varying frequencies. A comparison with noise correlation matrix method can justify the advantages of lossy substrate deembedding method in terms of accuracy, reliability, and compatibility with circuit simulation.

Restricted bandwidth is a common problem for conventional substrate models assuming a simple resistive network or an *RC* network. The simplified model may be valid in sufficiently low frequency ($\leqq$10 GHz), but is no longer accurate to fit the high-frequency domain up to tens of gigahertz. The limitations of a simple *RC* model have been investigated through a serious comparison between electroquasi-static (EQS) and electrodynamic (ED) models [16]. The results reveal an inductive like characteristics in noise propagation through the substrate and suggest that ED model is indispensable to an accurate simulation in high frequency over several tens of gigahertz. Unfortunately, the electromagnetic (EM) analysis requires complicated computation and extensive memory, and is not suitable for circuit simulations. Thus, an enhanced lossy substrate model is developed in the form of a lumped element circuit to be fully compatible with circuit simulators in terms of easy implementation and computation efficiency. The circuit schematics incorporating two substrate *RLC* networks in series with pads and TML coupling capacitances (C_{pad} and C_{ox}) can accurately simulate substrate losses through the pads and TML, respectively. A characteristic frequency responsible for the minimum of $\mathrm{mag.}(S_{11})$ [or $\mathrm{mag.}(S_{22})$] in pad S-parameter over 110 GHz represents the resonance of substrate *RLC* network and justifies the substrate inductance (L_{Si}) introduced in our lossy substrate model. The adoption of L_{Si} is a key feature, which differentiates the enhanced lossy substrate model from conventional ones and enables a broadband accuracy.

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Beside the broadband accuracy, a scalable lossy substrate model is strongly required to predict high-frequency performance of on-chip devices and circuits with diversified options in pad and TML layouts, as well as metal topologies. To meet this demand, an improved lossy substrate model was initiated in our recent study [17] and demonstrated an apparent scaling trend corresponding to pad structures. However, a scalable model with mathematic expressions for a quantitative analysis and prediction is not yet available. In this paper, the enhanced lossy substrate model can provide a promisingly good solution in this aspect. All the model parameters are scalable and can be predicted by an explicit function depending on C_{pad}. In this manner, the enhanced model can help explore the pad structure effect on high-frequency noises in nanoscale devices and guide an optimal layout in pads and TML for an effective reduction of extrinsic noise and low noise design. Note that the substrate resonance frequency strongly depends on C_{pad} as well, and can be predicted according to the scalable model parameters.

II. Device Technology and Characterization

n-MOSFETs with 100-nm gate length were fabricated in a p-well enclosed by a deep n-well, a so-called triple well process for substrate noise isolation. Note that triple well isolation against noise is limited to a few gigaahert and is no longer valid in very high frequencies up to several tens of gigahertz [18]. A multifinger structure with a fixed finger width of $W_F = 4\ \mu m$ and various finger numbers of $N = 18, 36$, and 72 were designed to investigate the impact on high-frequency noise, as well as the model scalability over device geometries. Ground–signal–ground (GSG) pads for RF measurement were fabricated by Cu/fluorinated silicated glass (FSG) back-end-of-line (BEOL) process with eight layers of Cu and FSG as inter-metal dielectric (IMD). To study lossy substrate effect on high-frequency noise and the extrinsic noise introduced through the pad and TML, three pad structures (lossy, normal, and small) were created. All three share the same ground pad (G-pad) layout and structure, but different signal pads with variation in topology and dimension.

Two-port S-parameters were measured by an Agilent vector network analyzer up to 40 GHz for full structures with devices-under-test (DUTs) and GSG pads together. An ultra-wideband measurement to 110 GHz was done on dummy open pads for broadband model development and validation. Y- and H-parameters can be derived from S-parameters for extraction of gate capacitances and cutoff frequency f_T. Noise parameters ($\text{NF}_{\min}$, R_n, Γ_{opt}, or Y_{opt}) were measured by ATN-NP5B to its limitation at 18 GHz under a fixed gate bias ($V_{\text{gs}}@\max.\ g_m = 0.8$ V) A two-step deembedding procedure assisted by open and short dummy pads was carried out to extract the parallel and series parasitic *RLC* elements. For high-frequency and noise simulation, the incorporation of accurately extracted resistances $(R_g, R_s, R_d, R_{\text{bulk}})$ and inductances (L_g, L_s, L_d) associated with MOSFET's terminals is crucial to improve the accuracy. Gate resistance R_g dominates the input characteristics (S_{11} and Y_{11}), noise figure ($\text{NF}_{\min}$), and current noises (S_{id} and S_{ig}), whereas the bulk parameters R_{bulk}, C_{sb}, and C_{db} primarily influence the output characteristics (S_{22} and Y_{22}), noise resistance (R_n) and its frequency dependence.

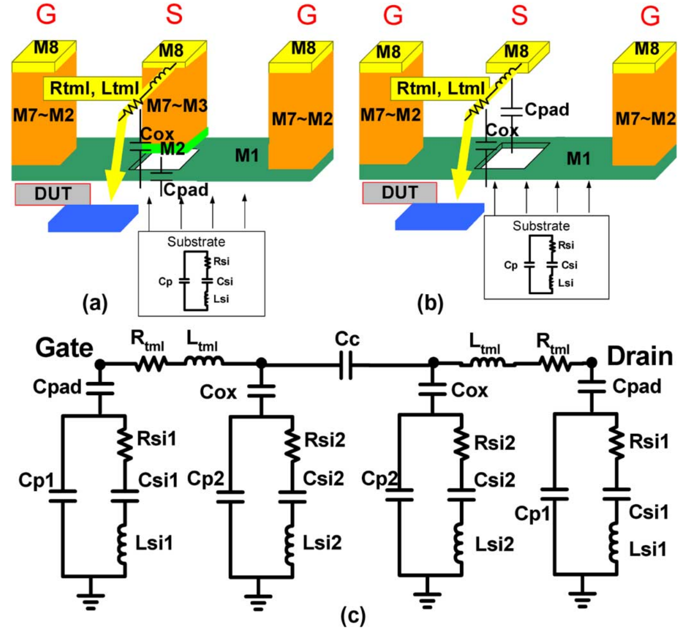

Fig. 1. 3-D configuration of GSG pads. (a) Lossy pad scheme: S-pads with stacked metals from M2 to M8. (b) Normal pad: S-pads with top metal (M8) only. (c) Equivalent circuit schematics of an enhanced lossy substrate model applicable to lossy, normal, and small pad schemes. After [17].

III. Broadband and Scalable Lossy Substrate Model for Various Pad Structures

In this paper, an enhanced lossy substrate model is developed to attain two ultimate goals, namely, broadband accuracy and scalability. The scalability will be extensively verified over various pad structures and their effect on high-frequency S-parameters and noises in nanoscale devices.

A. Pad Structures and Enhanced Lossy Substrate Model

Three GSG pad structures defined as lossy, normal, and small pads with different metal topologies or pad dimensions were fabricated in Cu/FSG BEOL process to investigate the resulting lossy substrate effect. Fig. 1(a) and (b) illustrates the 3-D configuration of lossy and normal pads in which the G-pads were constructed with stacked metals from bottom (M1) to top (M8), while the S-pads were built with two different schemes. For lossy pad scheme in Fig. 1(a), the S-pads are composed of stacked metals from M2 to M8, whereas for the normal pad scheme in Fig. 1(b), they are consisted of top metal (M8) only and excluding all lower metals. As for the small pad scheme, its S-pads just follow that of normal pad scheme but with a smaller size of 50 μm × 35 μm with respect to 50 μm × 50 μm for normal and lossy ones. All three pad structures adopt exactly the same G-pad topology.

Fig. 1(c) depicts the equivalent circuit schematics of the enhanced lossy substrate model to cope with various pad structures. The primary improvement over the original model is the adoption of C_{ox} underneath substrate *RLC* network associated with TML, which represents the coupling capacitance between

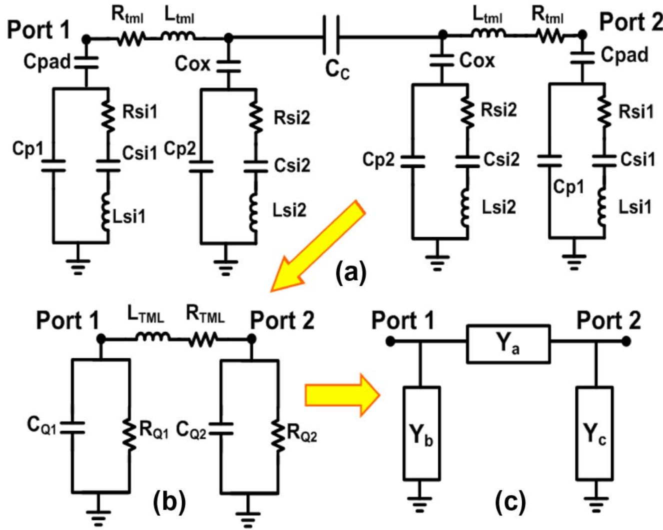

Fig. 2. Equivalent circuit analysis and topology conversion for lossy substrate model parameter extraction.

TML and substrate. As a result, the enhanced model is composed of two substrate *RLC* networks under the pad and TML in which the substrate loss is coupled through the pad and TML via C_{pad} and C_{ox}, respectively.

B. Improved Parameter Extraction Method and Broadband Accuracy

An improved parameter extraction method is developed for the enhance lossy substrate model based on the equivalent circuit in Fig. 1(c) and broadband S-parameter measured to 110 GHz for open pads with various structures in Fig. 1(a) and (b). Through a comprehensive circuit analysis and an appropriate circuit topology conversion illustrated in Fig. 2(a)–(c). The extraction flow was established with corresponding formulas as follows.

At the first step, the original equivalent circuit consisting of two branches of *RLC* networks with physical *RLC* elements at each port form a two-π scheme, as shown in Fig. 2(a). Trough a simple circuit analysis, the two-π scheme was then converted to a single-π topology with a single *RC* network at each port, illustrated in Fig. 2(b). Note that all *RLC* in Fig. 2(a) are physical elements independent of frequency, whereas $R_{Q1(2)}$ and $C_{Q1(2)}$ in Fig. 2(b) incorporate the original *RLC* and frequency dependence. Eventually, the single-π topology in Fig. 2(b) was converted to an equivalent circuit scheme in Fig. 2(c) in which Y_a, Y_b, and Y_c can be directly determined from measured Y_{11}, Y_{12} (Y_{21}), and Y_{22} according to (1)–(3) as follows:

$$Y_a = -Y_{21} = -Y_{12} \quad (1)$$
$$Y_b = Y_{11} + Y_{12} \quad (2)$$
$$Y_c = Y_{22} + Y_{21}. \quad (3)$$

The capacitive elements can then be extracted at very low frequency when the resistance and inductance introduced impedances are negligibly small. The port-to-port coupling capacitance C_c was determined from $\text{Im}(Y_{12})$ in (4). C_{p1}, C_{Si1}, C_{p2}, and C_{Si2} in substrate *RLC* networks were extracted from $\text{Im}(Y_b)$ and $\text{Im}(Y_c)$ [see Fig. 2(c)] in (5) and (6) and relevant approximations for lossy, normal, and small pads in (7) and (8) as follows:

$$C_c = -\frac{\text{Im}(Y_{12})}{\omega} \quad (4)$$
$$C_{Q1} = \frac{C_{\text{pad}}(C_{P1}+C_{\text{Si1}})}{C_{\text{pad}}+(C_{P1}+C_{\text{Si1}})} + \frac{C_{\text{OX}}(C_{P2}+C_{\text{Si2}})}{C_{\text{OX}}+(C_{P2}+C_{\text{Si2}})} = \frac{1}{\omega}\text{Im}(Y_b) \quad (5)$$
$$C_{Q2} = \frac{C_{\text{pad}}(C_{P1}+C_{\text{Si1}})}{C_{\text{pad}}+(C_{P1}+C_{\text{Si1}})} + \frac{C_{\text{OX}}(C_{P2}+C_{\text{Si2}})}{C_{\text{OX}}+(C_{P2}+C_{\text{Si2}})} = \frac{1}{\omega}\text{Im}(Y_c). \quad (6)$$

For lossy pad

$$C_{\text{OX}} \ll (C_{P2}+C_{\text{Si2}}) \Rightarrow \frac{C_{\text{OX}}(C_{P2}+C_{\text{Si2}})}{C_{\text{OX}}+(C_{P2}+C_{\text{Si2}})} \cong C_{\text{OX}}. \quad (7)$$

For normal and small pads

$$C_{\text{OX}} \approx (C_{P2}+C_{\text{Si2}}) \Rightarrow \frac{C_{\text{OX}}(C_{P2}+C_{\text{Si2}})}{C_{\text{OX}}+(C_{P2}+C_{\text{Si2}})} \cong \frac{1}{2}C_{\text{OX}}. \quad (8)$$

TABLE I
COMPARISON OF C_{pad} AND C_{ox} BETWEEN 1-D PLANAR CAPACITOR MODEL, 3-D RAPHAEL SIMULATION, AND OPTIMIZED MODEL

Capacitor	Pad Structures	1D Planar Cap. Model	3D Raphael Simulation	Optimized Model
C_{pad} (fF)	lossy	51.79	69.9	77.87
	normal	12.80	22.36	20
	small	8.98	16.88	13.89
C_{ox} (fF)	lossy	4.542	11.22	10.78
	normal	4.542	9.44	9.93
	small	4.542	8.94	9.91

Note that C_{pad} and C_{ox} are known with the initial values calculated by 3-D *RLC* simulation (Raphael) following layout and process parameters (metal thicknesses, IMD thicknesses, and dielectric constants) instead of extraction. Table I summarizes the comparison between 1-D planar capacitor model, 3-D Raphael simulation, and the optimized ones through a best fitting to measured S-parameters. The results reveal a significant underestimation using 1-D planar model, whereas a very close match with the optimized values when adopting 3-D Raphael simulation. It suggests that the approximation by a simplified 1-D planar capacitor model is no longer valid due to inappropriate neglect of the fringing capacitances in a 3-D topology. C_{ox} are kept at a similar value for different pad structures due to the same metal layout and topology for TML from the pads to intrinsic device. On the other hand, C_{pad} present a significant difference among the three pad structures in which the scaling factors of around 3.9 for the lossy versus normal pads and near 0.75 for the small versus normal pads just approach the theoretical values predicted by 3-D Raphael simulation. The substantially larger C_{pad} for lossy pad compared to normal and small pads, whereas very similar C_{ox} in three different pads present a result consistent with layout and metal topology.

Following the first step, as all the capacitive elements are already known, we can now perform an extraction of resistive and inductive elements (R_{Si1}, L_{Si1}, R_{Si2}, and L_{Si2}) by selecting a

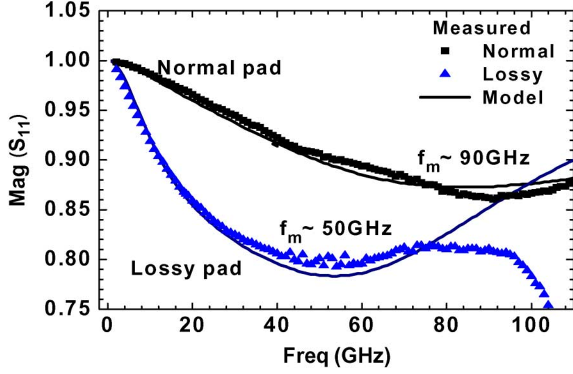

Fig. 3. Measured and simulated magnitude (S_{11}) over frequencies up to 110 GHz for normal and lossy pads. A characteristic frequency responsible for the minimum of $\mathrm{mag.}(S_{11})$ is defined as ω_m. Normal pad: $f_m \sim 90$ GHz. Lossy pad: $f_m \sim 50$ GHz.

very high-frequency domain, where the inductance effect becomes significant. As shown in Fig. 3, the measured $\mathrm{mag.}(S_{11})$ [or $\mathrm{mag.}(S_{22})$] presents a minimum at a frequency f_m situated around 50 GHz (for the lossy pad) or 90 GHz (for the normal pad). This characteristic frequency is due to a resonance appearing in the equivalent *LC* tank of the substrate network. It appears from circuit analysis that $\omega_m (= 2\pi\ f_m)$ can be modeled as a function of L_{Si1} and C_{eff} in (9) and (10). Note that C_{eff} is an effective capacitance representing C_{pad} in series with C_{Si1} and C_{p1}, which are in parallel, referring to Fig. 2(a). In this way, the substrate inductance L_{Si1} can be determined from the measured ω_m and C_{eff} in (9) and (10) with known C_{pad} and C_{Si1}, as well as C_{p1}. L_{Si2} can then be extracted from (11) and (12) under a relevant assumption of $\omega_{02} = \omega_{01}$ with known L_{Si1}, C_{Si1} and C_{Si2} as follows:

$$\omega_m \cong \frac{1}{\sqrt{L_{\mathrm{Si1}} C_{\mathrm{eff}}}} \Rightarrow L_{\mathrm{Si1}} = \frac{1}{C_{\mathrm{eff}} \omega_m^2} \tag{9}$$

$$C_{\mathrm{eff}} = \frac{C_{\mathrm{pad}}(C_{P1} + C_{\mathrm{Si1}})}{C_{\mathrm{pad}} + (C_{P1} + C_{\mathrm{Si1}})} \tag{10}$$

$$\frac{1}{\sqrt{L_{\mathrm{Si1}} C_{\mathrm{Si1}}}} = \omega_{01} \tag{11}$$

$$\frac{1}{\sqrt{L_{\mathrm{Si2}} C_{\mathrm{Si2}}}} = \omega_{02} = \omega_{01} \Rightarrow L_{\mathrm{Si2}} = L_{\mathrm{Si1}} \left(\frac{C_{\mathrm{Si1}}}{C_{\mathrm{Si2}}} \right). \tag{12}$$

Following the second step, all of capacitive and inductive elements are known to go the final step for extracting the resistive elements (R_{Si1} and R_{Si2}). The original expressions of $\mathrm{Im}(Y_b)$ and $\mathrm{Re}(Y_b)$ for extracting R_{Si1} and R_{Si2} are lengthy due to incorporating all *RLC* elements. To simplify the problem, characteristic frequencies ω_{01} and ω_{02} determined by $(L_{\mathrm{Si1}}, C_{\mathrm{Si1}})$ and $(L_{\mathrm{Si2}}, C_{\mathrm{Si2}})$ in (11) and (12) are specified to effectively reduce the formulas, as shown in (13) and (14), corresponding to $\omega_0 = \omega_{01} = \omega_{02}$. As a result, R_{Si1} and R_{Si2} can be easily extracted from (13) and (14) in which all the elements, except themselves, are known from previous steps of the extraction flow. The extracted parameters serving as the initial model can successfully facilitate an optimization process through the best fitting to measured S-parameters over 110 GHz.

TABLE II
OPTIMIZED *RLC* PARAMETERS OF THE ENHANCED LOSSY SUBSTRATE MODEL CORRESPONDING TO THREE PAD STRUCTURES, LOSSY, NORMAL, AND SMALL PADS

Gate Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	**77.87**	**74.97**	**200**	**170.7**	**159.9**		
Normal	20	28.55	44.01	223.9	483	50	0.2
Small	13.89	24.43	33.4	249.5	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)	C_c (fF)	
Lossy	10.78	1.629	**45.98**	**438.5**	**328.8**		
Normal	9.932	2.553	10.13	557.5	570.5	1.103	
Small	9.913	2.635	9.964	561.3	638.3		

Drain Pad RLC model parameters							
Pad layout	C_{pad} (fF)	C_{p1} (fF)	C_{Si1} (fF)	L_{Si1} (pH)	R_{Si1} (Ω)	L_{tml} (pH)	R_{tml} (Ω)
Lossy	**78.88**	**62**	**200**	**170**	**164.3**		
Normal	20.17	24.05	40.31	330	483	50	0.2
Small	12.84	19.72	30	385.5	511.7		
Pad layout	C_{ox} (fF)	C_{p2} (fF)	C_{Si2} (fF)	L_{Si2} (pH)	R_{Si2} (Ω)		
Lossy	11.07	2	**64.02**	**515.9**	**232.3**		
Normal	10.21	2.887	14.29	651.3	483		
Small	9.932	2.635	13.59	668.5	540.3		

Table II presents the optimized *RLC* parameters for the enhanced lossy substrate models associated with lossy, normal, and small pads, respectively. The assumption of $\omega_{01} = \omega_{02}$ made in (12) for initial extraction is justified by the optimized parameters $L_{\mathrm{Si1}}, C_{\mathrm{Si1}}, L_{\mathrm{Si2}}$, and C_{Si2}. The broadband accuracy of the enhanced model is proven by a good match with measured S-parameter over broad frequencies up to 110 GHz in Fig. 3 and an accurate prediction of ω_m at around 90/50 GHz for normal/lossy pads, respectively. The apparently lower ω_m for lossy pad consistently reflects influence from the dramatic increase of C_{pad} originated from the metal stack topology in lossy pads

$$\begin{aligned} C_{Q1} &= \frac{\mathrm{Im}(Y_b)}{\omega_0} \\ &= \frac{\omega_0^2 R_{\mathrm{si1}}^2 C_{\mathrm{pad}} C_{p1}(C_{\mathrm{pad}} + C_{p1}) + C_{\mathrm{pad}}}{1 + \omega_0^2 C_{\mathrm{pad}}^2 R_{\mathrm{si1}}^2 \left(1 + \frac{C_{p1}}{C_{\mathrm{pad}}}\right)^2} \\ &\quad + \frac{\omega_0^2 R_{\mathrm{si2}}^2 C_{\mathrm{ox}} C_{p2}(C_{\mathrm{ox}} + C_{p2}) + C_{\mathrm{ox}}}{1 + \omega_0^2 R_{\mathrm{si2}}^2 C_{\mathrm{ox}}^2 \left(1 + \frac{C_{p2}}{C_{\mathrm{ox}}}\right)^2} \end{aligned} \tag{13}$$

$$\begin{aligned} R_{Q1} &= \frac{1}{\mathrm{Re}(Y_b)} \\ &= \left\{ \frac{\omega_0^2 C_{\mathrm{pad}}^2 R_{\mathrm{si1}}}{1 + \omega_0^2 C_{\mathrm{pad}}^2 R_{\mathrm{si1}}^2 \left(1 + \frac{C_{p1}}{C_{\mathrm{pad}}}\right)^2} \right. \\ &\qquad \left. + \frac{\omega_{01}^2 C_{\mathrm{ox}}^2 R_{\mathrm{si2}}}{1 + \omega_0^2 C_{\mathrm{ox}}^2 R_{\mathrm{si2}}^2 \left(1 + \frac{C_{p2}}{C_{\mathrm{ox}}}\right)^2} \right\}^{-1} \\ \omega_0^2 &= \omega_{01}^2 \\ &= \frac{1}{L_{\mathrm{Si1}} C_{\mathrm{Si1}}} \\ &= \frac{1}{L_{\mathrm{Si2}} C_{\mathrm{Si2}}} \\ &= \omega_{02}^2 \end{aligned} \tag{14}$$

Fig. 4. Scaling trend of *RLC* parameters versus $C_{\rm pad}$ in **improved** lossy substrate models for lossy, normal, and small pads. Gate pad (port-1): (a) capacitive elements C_{p1}, $C_{\rm Si1}$, and $C_{\rm Si2}$ (b) resistive and inductive elements $R_{\rm Si1}$, $L_{\rm Si1}$, $R_{\rm Si2}$, and $L_{\rm Si2}$.

Fig. 5. Scaling trend of *RLC* parameters versus $C_{\rm pad}$ in original lossy substrate models for lossy, normal, and small pads. Gate pad (port-1): (a) capacitive elements C_{p1}, $C_{\rm Si1}$, and $C_{\rm Si2}$ (b) resistive and inductive elements $R_{\rm Si1}$, $L_{\rm Si1}$, $R_{\rm Si2}$, and $L_{\rm Si2}$.

C. Model Scalability Over Various Pad Structures

Fig. 4 illustrates the extracted *RLC* model parameters versus $C_{\rm pad}$ corresponding to lossy, normal, and small pads at port-1 (Gate). All *RLC* elements in this enhanced lossy substrate model present a good scalability featured by a linear function of $C_{\rm pad}$. For capacitive elements shown in Fig. 4(a), each of them can be predicted by a linearly increasing function. The larger $C_{\rm pad}$ introduces larger substrate network capacitances and subsequently worse substrate loss. As for the resistances and inductances in Fig. 4(b), each individual element follows a linearly decreasing function. The larger $C_{\rm pad}$ results in the smaller substrate resistances and inductances. Note that the increase of capacitances while decrease of resistances and inductances lead to the same trend in substrate loss and noise coupling. A similar scaling relationship in *RLC* parameters versus $C_{\rm pad}$ can be achieved for port-2, i.e., drain pad (not shown for brevity), which approach closely what was presented in Fig. 4 for port-1 (gate). The lossy pads featuring larger capacitances and smaller resistances will introduce more extrinsic noise and make devices suffer larger noise. The scalability of *RLC* parameters in the enhanced lossy substrate model is featured by an apparent correlation with pad structures and metal topologies represented by $C_{\rm pad}$. This dependence in the form of a linear function with respect to $C_{\rm pad}$ yields a physics-based and predictive model.

On the other hand, for the original lossy substrate model without $C_{\rm ox}$, the *RLC* parameters versus $C_{\rm pad}$ shown in Fig. 5 revealed abnormal results, such as losing a simple linear function with a single slope. For lossy pad compared with normal or small pads with a big difference in $C_{\rm pad}$, a monotonic increase in substrate network capacitances is demonstrated. However, looking at normal pad versus small pad, an abnormal trend with a negative slope appears in Fig. 5(a), meaning that the larger $C_{\rm pad}$ leads to the smaller substrate capacitances. The abnormal scaling trend makes the original model not scalable in a certain region for different pad structures with small difference in $C_{\rm pad}$. Reviewing Fig. 5(b) for substrate resistances and inductances versus $C_{\rm pad}$, a similar problem of a negative slope in a narrow region is identified in $R_{\rm Si1}$, $R_{\rm Si2}$, and $L_{\rm Si2}$, but the situation is worse in the plot of $L_{\rm Si2}$, which reveals a similar trend over a larger area.

N	$R_g (\Omega)$	$R_s (\Omega)$	$R_d (\Omega)$	$R_{bulk} (\Omega)$	$R_{ds}' (\Omega)$	C_{ds}' (fF)	L_g(pH)	L_d(pH)	L_s(pH)
18	4.819	0.17	0.17	232.3	161.8	4.467	48.61	55.22	17.26
36	2.34	0.15	0.15	168.9	138.4	19.54	47.02	53.62	17.08
72	1.119	0.13	0.13	95.6	64.7	47	45.97	46.41	17.07

Fig. 6. Equivalent circuit of MOSFET with parasitic resistances, capacitances, and inductances for dc, ac, RF, and noise simulation.

IV. Pad Structure Effect on RF Noise—Simulation by Broadband and Scalable Lossy Substrate Model

The enhanced lossy substrate model can be easily integrated with intrinsic devices in a standard circuit simulator for a global noise simulation. The primary objective is to investigate the impact of substrate loss on high-frequency characteristics and noise performance with particular interest in pad structure effects on extrinsic noise in nanoscale MOSFETs with various finger numbers. One more interesting and useful application is an accurate and simple noise extraction method to facilitate noise simulation accuracy for low noise CMOS circuit design.

For the reader's convenience, we recall that the "extrinsic noise" represents the noise generated from all parasitic elements outside of the intrinsic device like the pads, TML, and lossy substrate. The "global noise" represents the sum of intrinsic noise and extrinsic noise. The measured noise, before the pad and lossy substrate deembedding is equal to the global noise.

A. MOSFET Model and Parasitic Parameter Extraction

Fig. 6 presents MOSFET equivalent circuit dedicated to dc, ac, RF, and noise simulation. The four terminal device is transformed into three-terminal configuration because the source and bulk are internally shorted. The gate resistance R_g incorporates poly gate resistance, metal resistance, and channel sheet resistance. For a 100-nm device in a strong inversion region, channel sheet resistance is negligible compared with poly and metal resistances. R_s and R_d incorporate only the metal resistance. $R_{\rm bulk}$ represents the bulk resistance. L_g, L_d, and L_s are the parasitic inductances of the metal lines connecting ground/

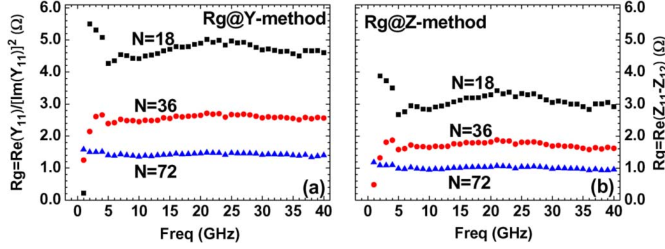

Fig. 7. R_g extracted for 100-nm nMOS with various finger numbers ($N = 18, 36, 72$). (a) Y-method, $R_g = \mathrm{Re}(Y_{11})/[\mathrm{Im}(Y_{11})]^2$. (b) Z-method, $R_g = \mathrm{Re}(Z_{11} - Z_{12})$.

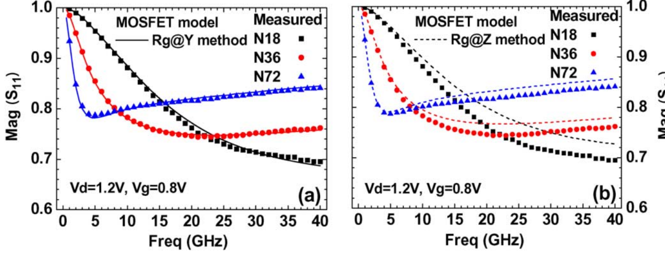

Fig. 8. Comparison of measured and simulated $\mathrm{Mag}(S_{11})$ using R_g extracted for 100-nm nMOS with various finger numbers ($N = 18, 36, 72$) (a) Y-method, $R_g = \mathrm{Re}(Y_{11})/[\mathrm{Im}(Y_{11})]^2$. (b) Z-method, $R_g = \mathrm{Re}(Z_{11} - Z_{12})$.

drain/source (G/D/S) contacts to pads. Their contributions become significant only at very high frequencies.

First, the parasitic R and L (R_g, R_s, R_d, R_{bulk}, L_g, L_s, and L_d) were carefully extracted and deployed in the intrinsic device. An extensive calibration was then done on the intrinsic MOSFET's *I–V* and *C–V* models (BSIM3). Note that gate resistance (R_g) plays a critical role in determining noise parameters such as noise resistance (R_n), noise figure ($\mathrm{NF}_{\min}$), and the drain and gate equivalent current noise generators (S_{id} and S_{ig}). This requires an accurate extraction of R_g to ensuring a reliable and accurate noise simulation, particularly in miniaturized devices. A conventional method denoted as the Z-method takes Z-parameters after two-step deembedding (open and short) and extracts R_g from $\mathrm{Re}(Z_{11} - Z_{12})$, which is assumed an appropriate approximation at sufficiently high frequency [19]. In this study, through a small signal circuit analysis on the MOSFET, we derived a new method using Y-parameters rather than Z-parameters. In this approach, R_g can be expressed as $\mathrm{Re}(Y_{11})/[\mathrm{Im}(Y_{11})]^2$ for MOSFETs in the saturation region, which is valid over a wide range of frequencies. The details of circuit analysis and formulas derivation is not covered in this paper. Fig. 7(a) demonstrates R_g extracted by the Y-method for the 100-nm MOSFET with three different finger numbers. The results extracted using the Z-method are shown in Fig. 7(b). Both methods present an inverse scaling in R_g versus N. However, the Z-method reveals apparently smaller R_g than the Y-method. The accuracy of the extracted R_g is verified by $\mathrm{mag.}(S_{11})$, which has strong dependence on R_g and can consistently justify accuracy of R_g. Fig. 8(a) indicates an excellent match between simulation and measurement achieved for all three MOSFETs adopting R_g extracted from the Y-method. As for using the Z-method, Fig. 8(b) reveals a significant deviation from measurement, particularly worse

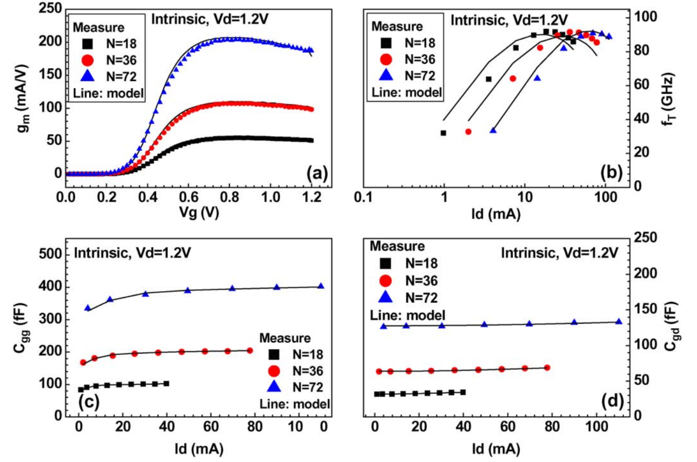

Fig. 9. Comparison between the measurement and simulation of an intrinsic MOSFET model for 100-nm nMOS with various finger numbers ($N = 18, 36, 72$). (a) g_m, (b) f_T, (c) C_{gg}, and (d) C_{gd} at $V_{\mathrm{ds}} = 1.2$ V and varying V_{gs} or I_d.

for the smallest device ($N = 18$) in higher frequencies. The results suggest that the proposed Y-method can enable an improved accuracy in R_g extraction and contribute to a reliable and accurate noise simulation.

In contrast with R_g, which dominates the input characteristics (S_{11} and Y_{11}), the bulk resistance R_{bulk} primarily influence the output characteristics (S_{22} and Y_{22}). Both R_{bulk} and R_g have significant effect on noise resistance (R_n). The increase of R_g raises R_n with a constant shift over the whole frequency range, whereas the variation of R_{bulk} limits its influence on R_n in lower frequencies ($\leqq$5 GHz). Taking the Y-method based on mentioned small signal circuit analysis, R_{bulk} was extracted from $\mathrm{Re}(Y_{22})/[\mathrm{Im}(Y_{22} + Y_{12})]^2$. Moreover, R'_{ds} in series with C'_{ds} were deployed for simulating drain to source inter-metal coupling effect, which has a nonnegligible effect on S_{22} and Y_{22}. The simultaneous adoption of R_{bulk} and R'_{ds} enables a precise fitting to S_{22} and Y_{22} over high frequencies. In this way, a full set of parasitic *RLC* parameters corresponding to different finger numbers (N) were extracted and presented in the table attached with Fig. 6. Note that the inverse of parasitic resistances $1/R_g$, $1/R_{\mathrm{bulk}}$, and $1/R'_{\mathrm{ds}}$, and the parasitic capacitance C'_{ds} approach a linear function of N. The larger N, the smaller resistances ($R_g, R_{\mathrm{bulk}}, R'_{\mathrm{ds}}$), while the larger capacitance C'_{ds} exactly match the multifinger layout.

MOSFET model accuracy was extensively verified through a comparison with *I–V*, *C–V*, Y-, S-, and H-parameters. Fig. 9 indicates a good match with measurement in terms of g_m, C_{gg}, C_{gd} (Y-parameters), and f_T (H-parameters) over a wide range of biases or currents for 100-nm nMOS with various finger numbers ($N = 18, 36$, and 72). Herein, g_m, C_{gg}, and C_{gd} increase with a finger number following a simple linear function of N, whereas f_T keeps nearly a constant value independent of N. This result can be consistently explained by a simple analytical model for f_T with the following expression of $f_T = g_m/2\pi\sqrt{(C_{gg}^2 - C_{gd}^2)}$.

The full circuit model accuracy can then be verified in terms of S-parameters, noise parameters, and equivalent noise current generators. Note that an improved thermal noise model has

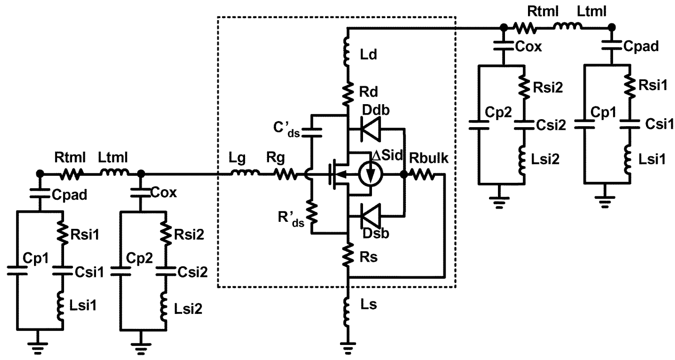

Fig. 10. Full circuit schematics with lossy substrate *RLC* networks integrated with an intrinsic MOSFET. The lossy substrate *RLC* parameters are listed in Table II.

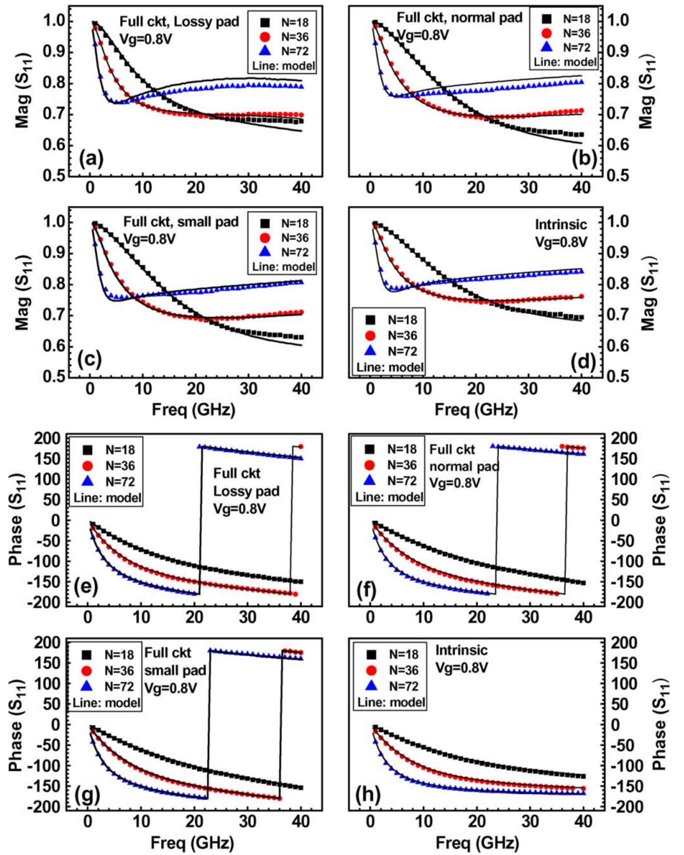

Fig. 11. Comparison of the measured and simulated $S_{11}(\mathrm{mag.,\ phase})$ in the full circuit model for 100-nm nMOS ($N = 18, 36, 72$) adopting three different pads. Mag (S_{11}): (a) lossy pad, (b) normal pad, (c) small pad, and (d) intrinsic devices after pad or lossy substrate deembedding. Phase (S_{11}): (e) lossy pad, (f) normal pad, (g) small pad, and (h) intrinsic devices after pad or lossy substrate deembedding. After [17].

been implemented in our previous work and will appear in IEEE TCAD [20]. A comprehensive short channel effects (SCEs) and parasitic resistance induced excess noise were adequately incorporated for yielding an accurate noise simulation in nanoscale MOSFETs. Fig. 10 depicts the full circuit schematics in which the lossy substrate *RLC* networks are integrated with the calibrated intrinsic MOSFET model for high-frequency S-parameter and noise simulation.

B. Two-Port S-Parameters

Fig. 11 presents a good match in S_{11} (magnitude and phase) between the measurement and simulation for full circuits adopting intrinsic devices with three different pads. The broadband accuracy is proven by measurement up to 40 GHz. The phase polarity change from negative to positive was revealed in Fig. 11(e)–(g) for the full circuits of larger devices ($N = 36$ and 72) at sufficiently high frequency. This result suggests the parasitic inductance effect and it can be eliminated for intrinsic devices via the pad and lossy substrate deembedding, shown in Fig. 10. Again, Fig. 12 demonstrates an excellent fit to the measured S_{22} by the full circuit simulation incorporating lossy, normal, and small pad models and intrinsic characteristics after lossy substrate deembedding. The phase polarity change exhibited in Fig. 12(e)–(g) for the larger devices can be explained by the parasitic inductances associated with port-2 (drain pad), which follows the same mechanism proposed for S_{11} corresponding to port-1 (gate pad). Besides S_{11} and S_{22}, a good agreement is realized for all other S-parameters (S_{12} and S_{21}), as well as Y-parameters (not shown for brevity).

C. Pad Structure Effect on Noise Parameters

In the following, the pad structure effect on noise parameters will be investigated with respect to both frequency dependence and finger number dependence. The global noise incorporating intrinsic and extrinsic noise can be simulated with a full equivalent circuit adopting the enhanced lossy substrate model and compared with measured noise. Subsequently, the intrinsic noise can be extracted through lossy substrate deembedding. A comparison with conventional noise correlation matrix deembedding method will be performed to verify the differences and advantages over the conventional approach.

An improved thermal noise model [20] was implemented in the intrinsic MOSFET and integrated with the enhanced lossy substrate model for noise simulation.

Fig. 13(a)–(c) indicates the simulated global $\mathrm{NF_{min}}$ and its good agreement with measurement for full circuits adopting three pad schemes (lossy, normal, and small pads). Interestingly, the devices adopting lossy pads reveal an abnormally strong finger number dependence and nonlinear behavior with respect to frequency in Fig. 13(a), whereas the finger number dependence is almost eliminated and frequency dependence is recovered to be linear for the normal and small pads shown in Fig. 13(b) and (c). The larger $\mathrm{NF_{min}}$ presented by the smaller finger number (N) in the category of a lossy pad suggests the amplification effect through the larger noise resistance R_n for smaller N. The global $\mathrm{NF_{min}}$ is effectively reduced for devices using a normal or a small pad scheme and the enhanced lossy substrate model can accurately predict the measured pad structure effect on noise. The intrinsic $\mathrm{NF_{min}}$ simulated after a lossy substrate deembedding shown in Fig. 13(d) are nearly independent of finger numbers over a wide range of frequencies up to 18 GHz. The intrinsic $\mathrm{NF_{min}}$ at $V_{\mathrm{gs}} = 0.8$ V corresponding to the maximum g_m is as low as 0.75 dB at 10 GHz and can be further suppressed to around 0.55 dB under $V_{\mathrm{gs}} = 0.5$ V responsible for the minimum $\mathrm{NF_{min}}$ (not shown). Note that noise

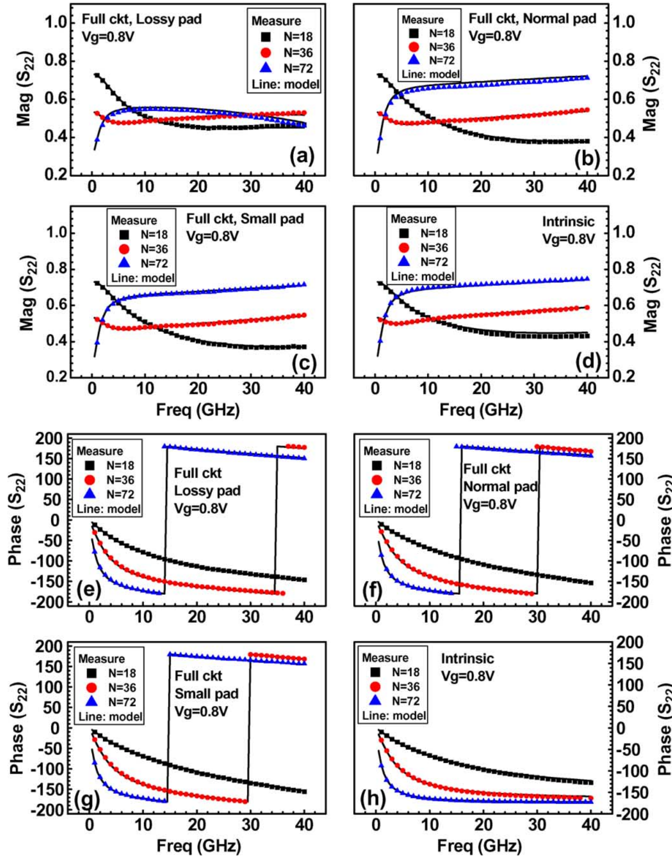

Fig. 12. Comparison of the measured and simulated $S_{22}(\text{mag., phase})$ by the full circuit model for 100-nm nMOS ($N = 18, 36, 72$) adopting three different pads. Mag (S_{22}): (a) lossy pad, (b) normal pad, (c) small pad, and (d) intrinsic devices after pad or lossy substrate deembedding. Phase (S_{22}): (e) lossy pad, (f) normal pad, (g) small pad, and (h) intrinsic devices after pad or lossy substrate deembedding

deembedding using matrix correlation method was performed simultaneously over the measured noise. The results plotted together with lossy substrate deembedding in Fig. 13(d) indicate an effective suppression on the noise in the lossy pad, but remain higher than those in normal pad after deembedding. One more obvious problem as compared to lossy substrate deembedding is a scattered distribution over frequencies, which leads to negative values in lower frequencies and an increase faster than a linear function in a higher frequency domain.

The pad structure effect on four noise parameters $\text{NF}_{\min}$, R_n, $\text{Re}(Y_{\text{opt}})$, and $\text{Im}(Y_{\text{opt}})$ are illustrated in Figs. 14 and 15 for $N = 18$ and 72, respectively, to investigate the finger number dependence of the extrinsic noise coupled through different pads. The smallest device ($N = 18$) reveals the largest sensitivity to the pad structures with a substantial increase in $\text{NF}_{\min}$, $\text{Re}(Y_{\text{opt}})$, and $|\text{Im}(Y_{\text{opt}})|$ for the lossy pad. The sensitivity is significantly suppressed by increasing the finger number. The increase of mentioned noise parameters in the lossy pad becomes much smaller for the largest device with $N = 72$ in Fig. 15(a)–(d). Note that R_n is effectively reduced by increasing N attributed to the smaller R_g and larger g_m, but remains nearly constant with respect to different pad schemes. The scalability and broadband accuracy of the enhanced lossy

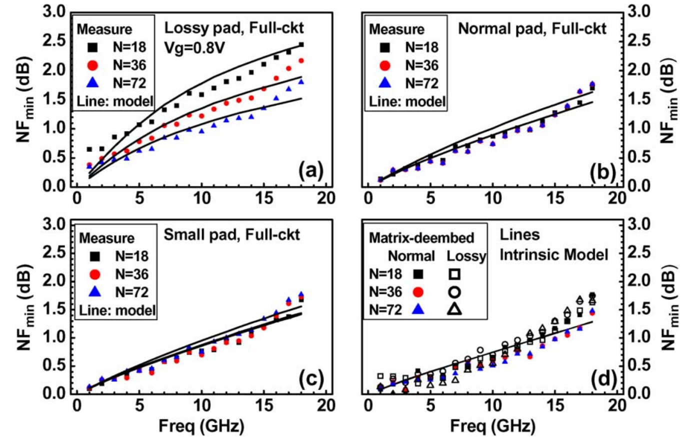

Fig. 13. Comparison of the measured and simulated $\text{NF}_{\min}$ by full circuit model for 100-nm nMOS ($N = 18, 36, 72$) adopting three different pad schemes. (a) Lossy pad, (b) normal pad, (c) small pad, and (d) intrinsic $\text{NF}_{\min}$ after a lossy substrate deembedding and comparison with correlation matrix deembedding results. After [17] and added with correlation matrix deembedding results.

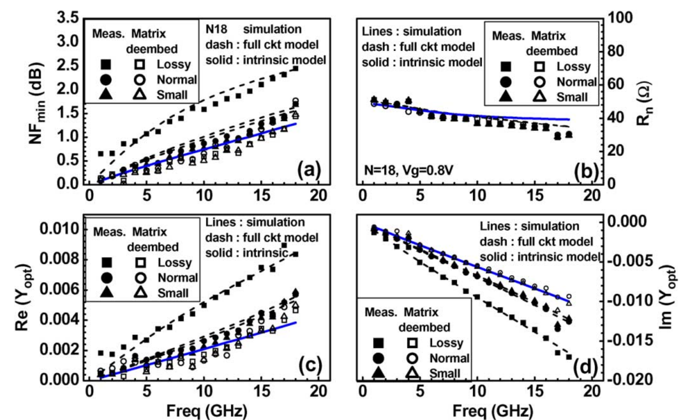

Fig. 14. Measured and simulated noise parameters for 100-nm nMOS by full circuit model of lossy, normal,and small pads and comparison with intrinsic ones using lossy substrate deembedding and noise correlation matrix deembedding $N = 18$. (a) $\text{NF}_{\min}$. (b) R_n. (c) $\text{Re}(Y_{\text{opt}})$. (d) $\text{Im}(Y_{\text{opt}})$. From [17] and added with noise correlation matrix deembedding results.

substrate model is proven by a good agreement with the measured noise parameters associated with various pads, as well as finger numbers, and over a broad frequencies up to 18 GHz. The intrinsic noise parameters extracted through the lossy substrate deembedding (solid lines) indicate an effective reduction and then a recovery to a linear frequency dependence in $\text{NF}_{\min}$, $\text{Re}(Y_{\text{opt}})$, and $\text{Im}(Y_{\text{opt}})$. $\text{NF}_{\min}$ measured from the devices with a normal or small pad structure are effectively suppressed and approach that of an intrinsic device. The results suggest that pads and TML using highest metal only and smallest area, achieving the minimal C_{pad} and C_{ox} can minimize the extrinsic noise introduced from the lossy substrate and approach the intrinsic performance. Note that noise correlation matrix deembedding results (empty symbols) are allocated in the same plot for comparison. An undesired fluctuation over frequencies and deviation from linear distribution appeared in $\text{NF}_{\min}$ and $\text{Re}(Y_{\text{opt}})$.

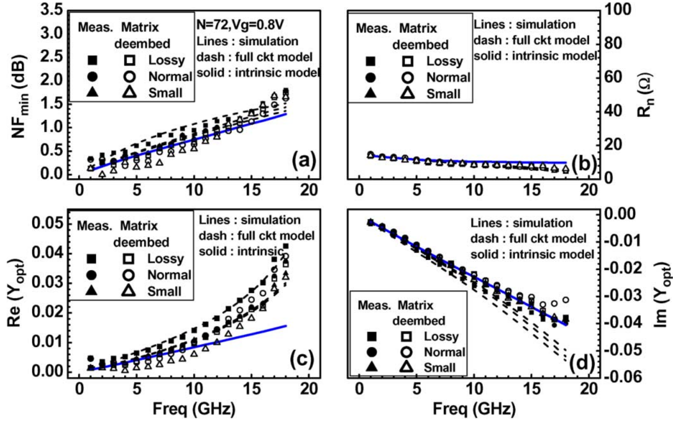

Fig. 15. Measured and simulated noise parameters for 100-nm nMOS by full circuit model of lossy, normal, small pads and comparison with intrinsic ones using lossy substrate deembedding and noise correlation matrix deembedding, $N = 72$. (a) $\mathrm{NF}_{\min}$. (b) R_n. (c) $\mathrm{Re}(Y_{\mathrm{opt}})$. (d) $\mathrm{Im}(Y_{\mathrm{opt}})$. From [17] and added with noise correlation matrix deembedding results.

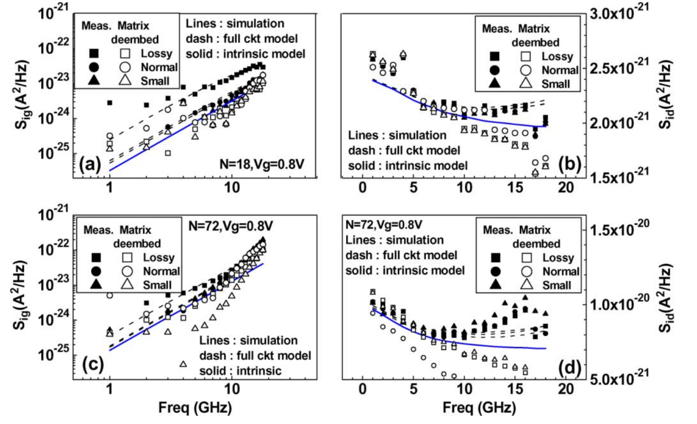

Fig. 16. Measured and simulated S_{ig} and S_{id} for 100-nm nMOS in a full circuit model of lossy, normal, and small pads, and comparison with intrinsic noise extracted using lossy substrate deembedding and noise correlation matrix deembedding method. $N = 18$. (a) S_{ig}. (b) S_{id}, $N = 72$. (c) S_{ig}. (d) S_{id}.

D. Pad Structure Effect on Current Noise

Subsequently, a more extensive verification is performed on the power spectral density (PSD) of drain and gate current noises S_{id} and S_{ig} to explore the lossy substrate effect subject to pad structures. The global current noise S_{ig} and S_{id} can be derived from the measured noise parameters ($\mathrm{NF}_{\min}$, R_n, and Y_{opt}) and Y-parameters following (15)–(18) based on the noise equivalent circuit analysis for a two-port network and the application of noise correlation matrix method [21]

$$S_{\iota g} = \frac{\overline{|\iota_{ng}|^2}}{\Delta f} = 4k_BT \cdot R_n \left\{ |Y_{\mathrm{opt}}|^2 - |Y_{11}|^2 + 2\mathrm{Re}\left[(Y_{11} - Y_{\mathrm{cor}})Y_{11}^*\right]\right\} \quad (15)$$

$$S_{\iota d} = \frac{\overline{|\iota_{nd}|^2}}{\Delta f} = 4k_BT \cdot R_n |Y_{21}|^2 \quad (16)$$

where

$$Y_{\mathrm{cor}} = \frac{F_{\min} - 1}{2R_n} - Y_{\mathrm{opt}} \quad (17)$$

$$F_{\min} = 10^{\frac{\mathrm{NF}_{\min}}{10}}. \quad (18)$$

Fig. 16 presents a good match between the measurement and model for S_{ig} and S_{id} corresponding to $N = 18$ and 72 with lossy, normal, and small pads, respectively. Again, the smallest device $(N = 18)$ reveals a substantially larger S_{ig} corresponding to the lossy pad in Fig. 16(a), whereas there is little difference in S_{id} for various pads in Fig. 16(b). The extrinsic noise in S_{ig} arising from the lossy pads is mitigated for the largest device $(N = 72)$, as shown in Fig. 16(c).

The lossy substrate effect on S_{ig} and S_{id} can be consistently explained by (15)–(18). For the gate current noise S_{ig} in (15), the extrinsic noise revealed by the lossy pads just resorts to a substantial increase of Y_{opt} referred to Fig. 14(c). Regarding the drain current noise S_{id} in (16), a very minor pad structure effect on R_n [see Fig. 14(b)] and $\mathrm{Re}(Y_{21})$ and the dominance of $|Y_{21}|^2$ by $|\mathrm{Re}(Y_{21})|^2$ at a relatively lower frequency (≤18 GHz) explain the insignificant change of S_{id} in Fig. 16(b) and (d). The intrinsic S_{ig} extracted through the lossy substrate deembedding exhibits an obviously lower value and frequency dependence approaching the ideal theory that is proportional to ω^2. As for the intrinsic S_{id} compared with the global one incorporating extrinsic noise, a minor change at lower frequencies, but a suppression to near a constant at higher frequencies reflects the deembedding effect on $|Y_{21}|^2$. At lower frequencies, $|Y_{21}|^2$ is dominated by $|\mathrm{Re}(Y_{21})|^2$, which generally keeps near constant after a deembedding. Going to higher frequencies, $|\mathrm{Im}(Y_{21})|^2$ may take over the influence on S_{id} for larger N before a deembedding. As for the intrinsic one after a deembedding, the substantial decrease of $|\mathrm{Im}(Y_{21})|^2$ will recover the dominance of $|\mathrm{Re}(Y_{21})|^2$ and lead to an effective suppression of S_{id} to near a constant versus frequency. Note that noise correlation matrix deembedding results (empty symbols) are presented in the same plot for a comparison. An undesired fluctuation over frequencies appeared in S_{ig}, as well as S_{id}, and deviation from a linear distribution in S_{ig}. Both the fluctuation and deviation in frequency dependence explain the difficulty and limitation in adopting noise correlation matrix method in noise deembedding and simulation.

Fig. 17 demonstrates the finger number dependence of S_{ig} and a remarkable pad structure effect. As shown in Fig. 17(a), S_{ig} measured with a lossy pad reveals an abnormally small dependence on finger numbers and frequency dependence away from the theoretical frequency dependence proportional to ω^2. As for the normal and small pads in Fig. 17(b) and (c), an obvious finger number dependence is recovered, but the deviation from theoretical frequency dependence still persists at higher frequencies. The intrinsic S_{ig} extracted using lossy substrate deembedding, as shown in Fig. 17(d), can recover both finger number dependence and frequency dependence to a normal condition. One more interesting observation is that lossy pad effect on S_{ig} and $\mathrm{NF}_{\min}$ in terms of finger number dependence just goes in an opposite direction. The lossy pad causes an abnormally strong dependence on N in $\mathrm{NF}_{\min}$ (Fig. 13), whereas an abnormally weak dependence on N in S_{ig} (Fig. 17). As a result, the broadband accuracy and scalability is again certified on the current noises over a broad range of frequencies and various pad structures. Again, noise correlation matrix deembedding results (empty symbols) are presented in Fig. 17(d) for a comparison with lossy substrate deembedding results. A severe

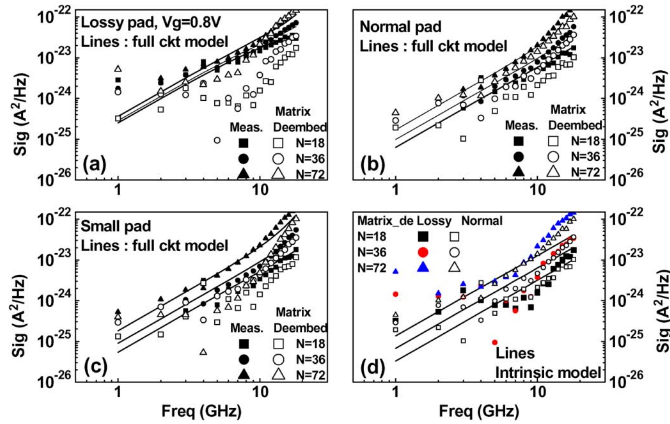

Fig. 17. Comparison of the measured and simulated S_{ig} in a full circuit model for 100-nm nMOS ($N = 18, 36, 72$) adopting different pads and comparison with intrinsic noise extracted by lossy substrate deembedding, as well as noise correlation matrix deembedding method. (a) Lossy pad, (b) normal pad, (c) small pad, and (d) intrinsic S_{ig} after the lossy substrate and pad deembedding

fluctuation over frequencies and deviation from a linear distribution apparent in S_{ig} suggests the weaknesses of noise correlation matrix method in noise deembedding and simulation.

V. Conclusions

A broadband and scalable lossy substrate model has been developed and validated over 100-nm RF MOSFETs with various finger numbers and different GSG pad structures (lossy, normal, and small pads). This enhanced lossy substrate model incorporates substrate *RLC* networks distributed under the pads and TML. The exact distribution of substrate loss through the pads and TML can accurately simulate the resulted extrinsic noise in miniaturized devices over a broadband region. The physical elements $C_{\rm pad}$ and $C_{\rm ox}$ introduced in the enhanced lossy substrate model consistently follow the scaling factors corresponding to the layout and 3-D topology in different pad schemes. A novel parameter extraction method was established and proven with broadband accuracy in open pad S-parameters over 110 GHz. All the model parameters are scalable and can be predicted by a linear function of $C_{\rm pad}$. In this way, the enhanced model can guide and facilitate an optimal layout in pads and TML for an effective reduction of extrinsic noise and low noise design in nanoscale MOSFETs.

For RF noise simulation and analysis, the broadband accuracy is validated by a good match with the measured S-parameters up to 40 GHz, as well as noise parameters and PSD of current noises (S_{id} and S_{ig}) over 18 GHz. The scalability is certified by an accurate prediction for various finger numbers in conjunction with lossy, normal, and lossy pads. A reliable intrinsic noise extraction can be realized using the lossy substrate deembedding method through which the intrinsic problems of conventional noise correlation matrix method can be eliminated.

As a result, this broadband and scalable lossy substrate model can facilitate an optimal design to minimizing the extrinsic noise and approaching the intrinsic device noise performance. Ultimately, this enhanced model can be easily deployed in general circuit simulators to substantially improve RF circuit simulation accuracy for low-power and low-noise design in nanoscale RF CMOS technology.

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