A Comprehensive Investigation of Analog Performance for Uniaxial Strained PMOSFETs

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***Abstract*—This paper presents a comprehensive investigation of the analog performance for uniaxial strained PMOSFETs with sub-100 nm gate length. Through a comparison between co-processed strained and unstrained devices regarding important analog metrics such as transconductance to drain current ratio (g_m/I_d), dc gain, linearity, low-frequency noise, and device mismatch, the impact of process-induced uniaxial strain on the analog performance of MOS devices has been assessed and analyzed. Our results indicate that, although the drain current noise spectral density and drain current mismatch of the strained device under low gate voltage overdrive are increased because of the larger gate-bias sensitivity of carrier mobility, the strained device has almost the same low frequency and mismatch performance as the unstrained one at a given g_m/I_d. This paper may provide insights for analog design using advanced strained devices.**

***Index Terms*—CMOS, DC gain, device mismatch, linearity, low-frequency noise, process-induced strain, uniaxial strained PMOSFET, transconductance to drain–current ratio.**

I. Introduction

As CONVENTIONAL CMOS is reaching its scaling limits, mobility scaling has emerged as a key technology for improving device performance [1]. To enable the mobility scaling, uniaxial strained silicon has been widely used in state-of-the art CMOS technologies [2]–[9].

Although carrier mobility enhancement can help overcome the speed/power barrier for logic applications and enhance the cutoff frequency [10], the impact of uniaxial strain on analog performance, particularly device mismatch and low-frequency noise [11], [12], is still not clear. This issue is important to mixed-mode integrated circuits for system-on-a-chip [13], [14] and merits investigation.

Through a comparison between strained and unstrained devices, this paper investigates the transconductance-to-drain–current ratio (g_m/I_d), dc gain, linearity, low-frequency noise, and device mismatch of the uniaxial strained PMOSFETs [7] with sub-100-nm gate length. Section II introduces the devices used in this paper. In Section III, we compare carrier mobility and several analog metrics such as g_m/I_d, dc gain, and linearity. The impact of uniaxial strain on the low-frequency noise and device mismatch will be investigated in Sections IV and V, respectively. Section VI draws the conclusion.

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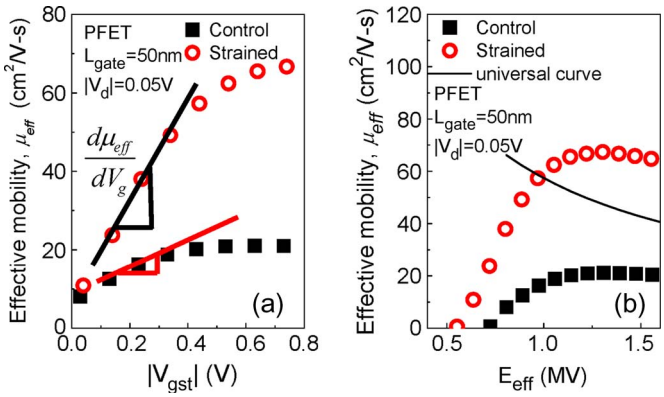

Fig. 1. Extracted effective hole mobility for devices with $L_{\rm gate} = 50$ nm (a) versus $|V_{\rm gst}|$ and (b) versus effective vertical electric field.

II. Devices

Co-processed uniaxial strained and unstrained PMOSFETs are investigated in this paper [15]. Strained and unstrained devices with channel direction $\langle 110 \rangle$ were fabricated on (100) silicon substrate. Shallow Trench Isolation was patterned to define the active region. Then, a 2 nm nitrided oxide was grown on the surface of the wafer. The polygate was implanted with heavily doped P-type species after polydeposition and then was postannealed to increase the gate activation rates. Then, the ultrashallow Highly Doped Drain implant followed by Spike Rapid Thermal Annealing, spacer formation, and source/drain engineering were implemented sequentially. The strained device features compressive uniaxial Contact Etch Stop Layer and SiGe source/drain [16]–[19]. For the transistors with gate length $L_{\rm gate} = 50$ nm, the saturation drain current $(I_{\rm dsat})$ of the strained device is improved more than 100% as compared with its control counterpart.

Since analog circuits are usually biased in the low gate-bias regime (e.g., $V_{\rm gst} = V_g - V_{\rm th} = 0.2$ V) for better power efficiency [20], we focus on the analog performance in the low $V_{\rm gst}$ regime. The threshold voltage $V_{\rm th}$ is extracted by the constant-current method [21].

III. Effective Hole Mobility and g_m/I_d

In this paper, we extract the effective hole mobility $\mu_{\rm eff}$ by the split C–V method [22] with corrections on series resistance and effective channel length. The extracted effective

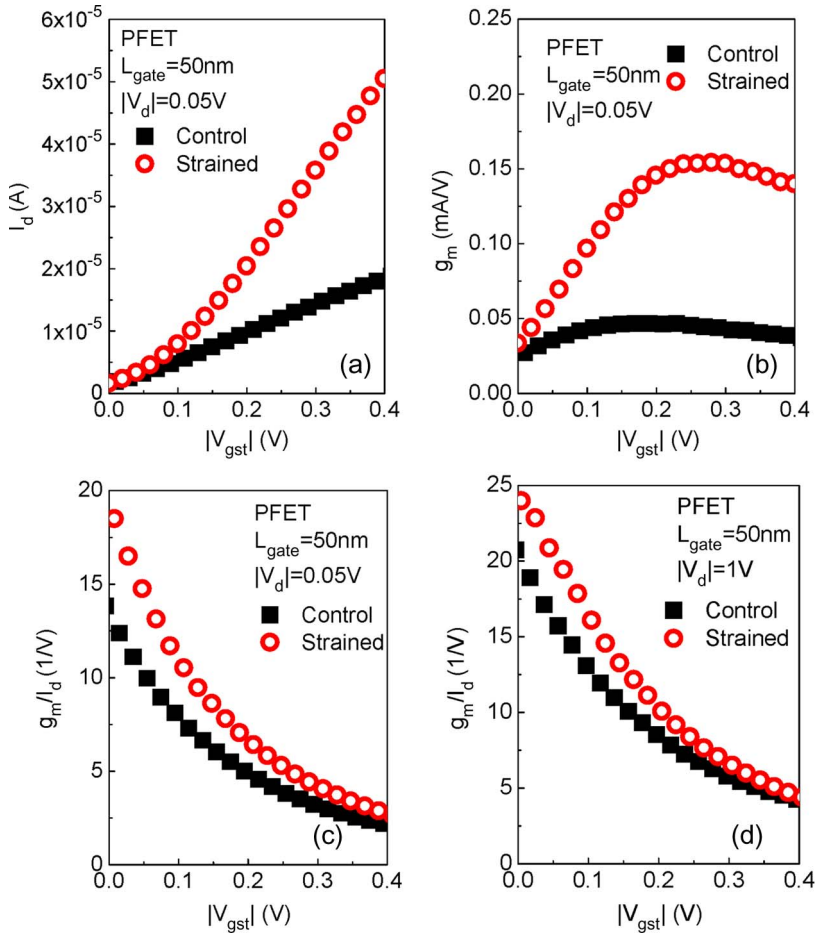

Fig. 2. (a) I_d versus $|V_{\rm gst}|$ at $|V_d| = 0.05$ V, (b) g_m versus $|V_{\rm gst}|$ at $|V_d| = 0.05$ V, (c) g_m/I_d versus $|V_{\rm gst}|$ at $|V_d| = 0.05$ V, and (d) g_m/I_d versus $|V_{\rm gst}|$ at $|V_d| = 1$ V for devices with $L_{\rm gate} = 50$ nm.

hole mobilities as a function of $V_{\rm gst}$ for devices with $L_{\rm gate} = 50$ nm are shown in Fig. 1(a). The strained device shows a superior effective mobility as compared with the unstrained device. Regarding the low value of the mobility for the control device shown in Fig. 1(a) and (b), it has been reported that carrier mobility may be degraded in short channel devices because of process-induced defects located near the source and drain junctions [23]. Besides, heavily doped channel and pocket implants may also be responsible for the low carrier mobility.

The effective hole mobility enhancement is responsible for the drain current (I_d) and transconductance (g_m) improvements of the strained devices [6]–[8], as shown in Fig. 2(a) and (b). Besides, it is shown in Fig. 1 that $\mu_{\rm eff}$ increases with V_g around $|V_{\rm gst}| = 0.2$ V. This is because, in the low V_g regime, the mobility is mainly determined by Coulombic scattering. The mobile carrier screening makes $\mu_{\rm eff}$ increase with V_g. The larger slope of the mobility for the strained device can be attributed to the reduced effective mass [24]–[26] and is responsible for the higher g_m/I_d, as observed in Fig. 2(c) (linear region) and Fig. 2(d) (saturation region).

Fig. 3 compares the dc gain of the strained device with the control device for $L_{\rm gate} = 50$ nm at $|V_d| = 1$ V. The dc gain is defined as dc gain $= g_m \times R_{\rm out}$ with $R_{\rm out}$ being the output resistance. Fig. 3 shows that the dc gain of the strained device is nearly identical to that of the control device for constant $V_{\rm gst}$.

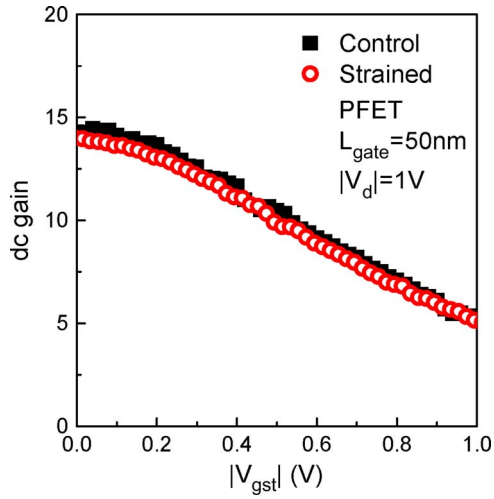

Fig. 3. DC gain for devices with $L_{\rm gate} = 50$ nm at $|V_d| = 1$ V (a) versus $|V_{\rm gst}|$ and (b) versus I_d.

Regarding the linearity performance, it is usually defined as follows: $VIP_3 = \sqrt{24 \cdot g_m/g_{m3}}$ [28] with $g_{m3} = \partial^3 I_d/\partial V_g^3$. VIP_3 is the extrapolated input gate bias amplitude at which the first- and third-order output amplitudes (of the drain current) are equal. For low-distortion operation, VIP_3 should be as high as possible. For strained devices biased by a constant $V_{\rm gst}$, the

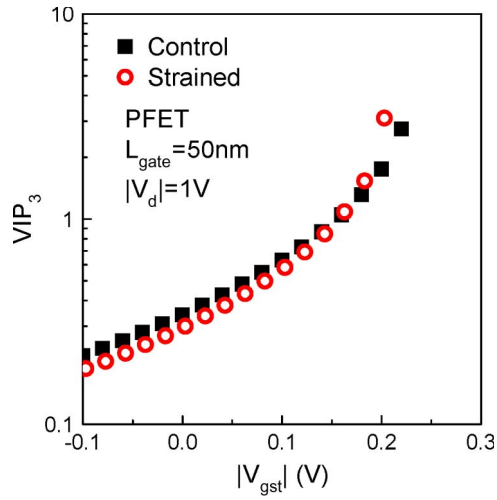

Fig. 4. VIP_3 for devices with $L_{\rm gate} = 50$ nm at $|V_d| = 1$ V (a) versus $|V_{\rm gst}|$ and (b) versus I_d.

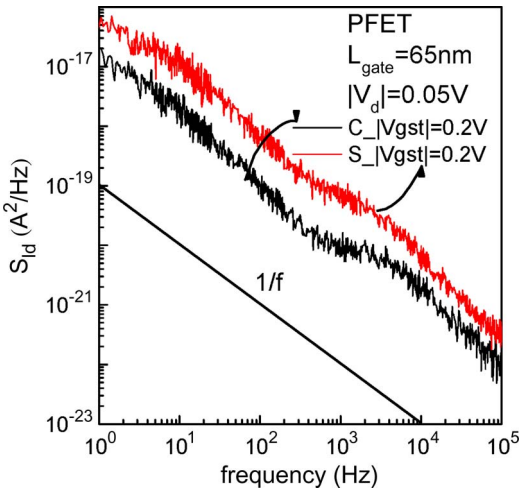

Fig. 5. Drain–current noise spectral density $S_{\rm Id}$ for devices with $L_{\rm gate} = 65$ nm at $|V_d| = 0.05$ V and $|V_{\rm gst}| = 0.2$ V showing typical $1/f^r$ noise type with r close to one.

extracted VIP_3 is nearly identical to that of the control device, as shown in Fig. 4.

IV. Low-Frequency Noise

To assess the impact of strain on low-frequency noise, we have performed noise measurements for devices with $L_{\rm gate} = 65$ nm by the BTA9812 low-frequency measurement system. The drain current noise spectral densities ($S_{\rm Id}$) for the strained and unstrained devices biased at $|V_{\rm gst}| = 0.2$ V are shown in Fig. 5. The spectra show typical $1/f^{\gamma}$ noise type with the frequency index γ close to one.

Fig. 6 shows the measured $S_{\rm Id}$ versus I_d for the strained and unstrained devices at $f = 10$ Hz. It can be seen that the $S_{\rm Id}$ of the strained device is larger than that of the unstrained one. Moreover, the increasing $S_{\rm Id}$ with I_d^2 indicates a carrier-number-fluctuations-dominated $1/f$ noise [29]–[31]. The carrier-number-fluctuations origin of the $1/f$ noise is further shown in Fig. 7, which shows the normalized noise spectral density ($S_{\rm Id}/I_d^2$) as well as $(g_m/I_d)^2$ versus I_d for strained

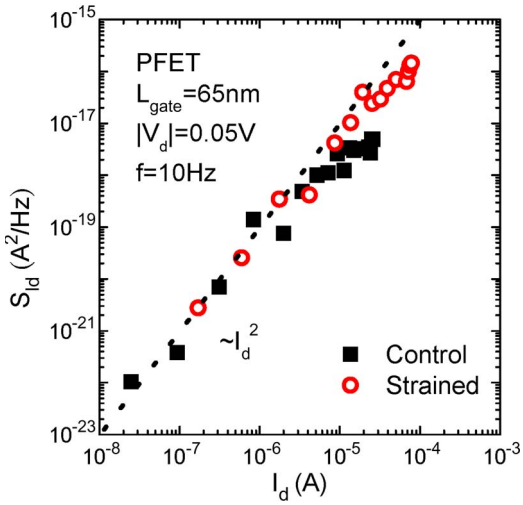

Fig. 6. Drain–current noise spectral density $S_{\rm Id}$ versus I_d at $f = 10$ Hz and $|V_d| = 0.05$ V. The I_d^2 dependent $S_{\rm Id}$ indicates number-fluctuation-dominated $1/f$ noise.

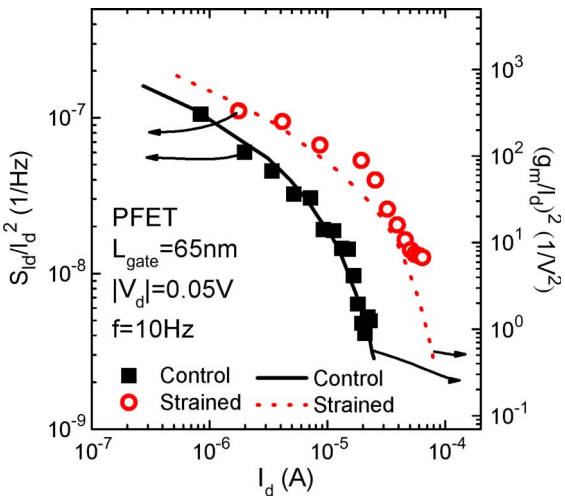

Fig. 7. Normalized current noise spectral density $S_{\rm Id}/I_d^2$ and $(g_m/I_d)^2$ versus I_d for devices with $L_{\rm gate} = 65$ nm and $|V_d| = 0.05$ V. Good proportionality between $S_{\rm Id}/I_d^2$ and $(g_m/I_d)^2$ implies that the enlarged $S_{\rm Id}/I_d^2$ of the strained device can be attributed to the strain-enhanced g_m/I_d.

and unstrained devices. In Fig. 7, $S_{\rm Id}/I_d^2$ shows a fairly good proportionality with $(g_m/I_d)^2$, which also points to a carrier number fluctuations origin of the $1/f$ noise. In addition, it implies that the discrepancies of $S_{\rm Id}/I_d^2$ between the strained and unstrained devices can be attributed to the discrepancies of $(g_m/I_d)^2$. In other words, the enhanced drain–current noise of the strained device at a given $V_{\rm gst}$ results from the strain-improved g_m/I_d.

In Fig. 8, we further show that, for a given g_m/I_d, the $S_{\rm Id}/I_d^2$ of the strained device is almost the same as that of the unstrained one.

Fig. 9 shows the input-referred voltage spectral density ($S_{\rm Vg} = S_{\rm Id}/g_m^2$) at $f = 10$ Hz as a function of $V_{\rm gst}$ taken from the average of ten devices. From Fig. 9, it is shown that the $S_{\rm Vg}$ for strained and unstrained devices are nearly identical. Although Giusi *et al.* [11] have reported that the low-frequency noise of the strained PMOSFET could be degraded due to

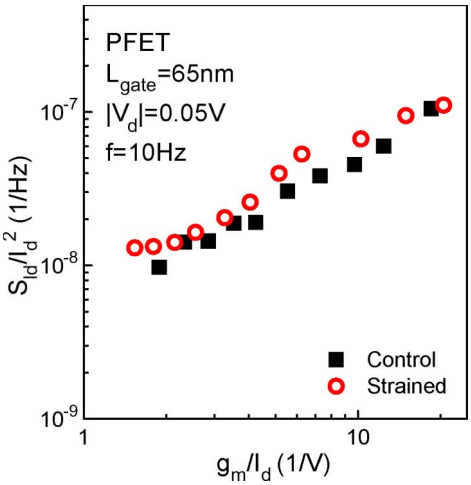

Fig. 8. Normalized current noise spectral density $S_{\rm Id}/I_d^2$ versus g_m/I_d for devices with $L_{\rm gate} = 65$ nm and $|V_d| = 0.05$ V.

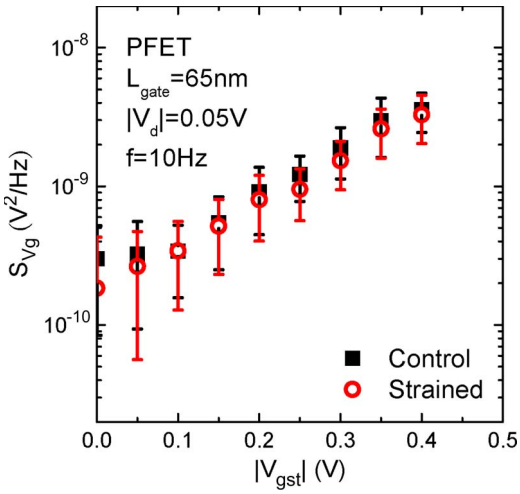

Fig. 9. Input-referred noise spectral density $S_{\rm Vg}$ versus $|V_{\rm gst}|$ for devices with $L_{\rm gate} = 65$ nm at $f = 10$ Hz and $|V_d| = 0.05$ V.

the worse gate dielectric quality when processing the SiGe source/drain, Simoen *et al.* [12] reported that the gate dielectric quality of the strained device may not be degraded and the low-frequency noise performance could be preserved. We have performed charge pumping measurement (Fig. 10) [32], and it is found that the difference of the trap densities between the strained and unstrained devices is within 10%.

V. Device Mismatch

We have extracted the matching properties of the strained and unstrained devices from identical devices in a matching pair configuration on 50 dies. Statistics on the mismatch in the drain current $((\Delta I_d)/I_d)$ and threshold voltage $(\Delta V_{\rm th})$ in the linear and saturation regions have been obtained.

Fig. 11 shows the measured standard deviations of the drain–current mismatch $(\sigma(\Delta I_d)/I_d)$ for the strained and control devices with $L_{\rm gate} = 54$ nm. It can be seen that the $\sigma(\Delta I_d)/I_d$ of the strained device is larger than that of the unstrained one.

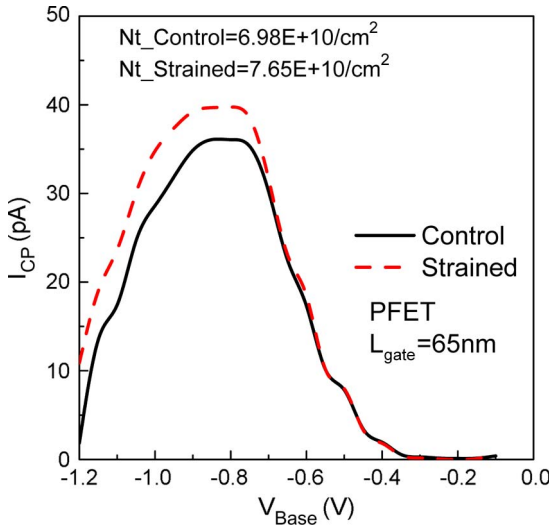

Fig. 10. Measurement results of charge pumping for strained and unstrained devices with $L_{\rm gate} = 65$ nm. $V_{\rm base}$ is the base level of gate pulses.

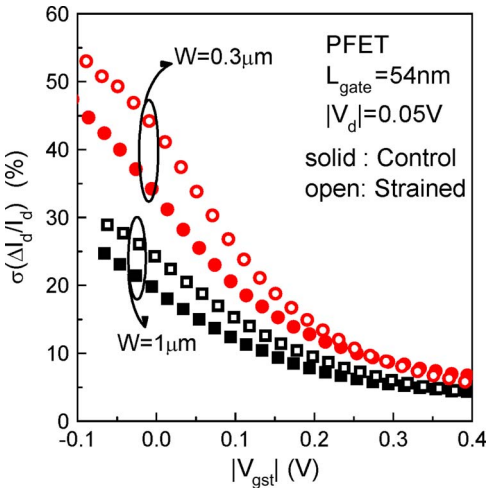

Fig. 11. Drain–current mismatch $\sigma(\Delta I_d)/I_d$ versus $|V_{\rm gst}|$ for devices with $L_{\rm gate} = 54$ nm at $|V_d| = 0.05$ V shows larger drain–current mismatch for the strained device.

The drain–current mismatch in the low $V_{\rm gst}$ regime is dominated by the threshold voltage mismatch $(\Delta V_{\rm th})$ [33] and can be expressed as [34]

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d} \times (\Delta V_{\rm th}). \tag{1}$$

To verify the relevance of $\Delta V_{\rm th}$ to $\Delta I_d/I_d$, (1) can be rewritten as $(\Delta I_d)/g_m = -\Delta V_{\rm th}$ [35], and the correlation (ρ) between $(\Delta I_d)/g_m$ at $V_{\rm gst} = 0$ and $(\Delta I_d)/g_m$ at other low $V_{\rm gst}$ is shown in Fig. 12. It can be seen that the correlation lies between 70% and 100% for both strained and control devices. This ensures that the threshold voltage mismatch is the dominant mechanism that determines the drain current mismatch.

Fig. 13(a) and (b) shows the Pelgrom plot [36] of the $\Delta I_d/I_d$ at $|V_d| = 0.05$ V and 1 V, respectively. Note that the gate length of the strained device needs to be the same $(L_{\rm gate} = 54$ nm) in order to keep similar strain in the channel. This is because

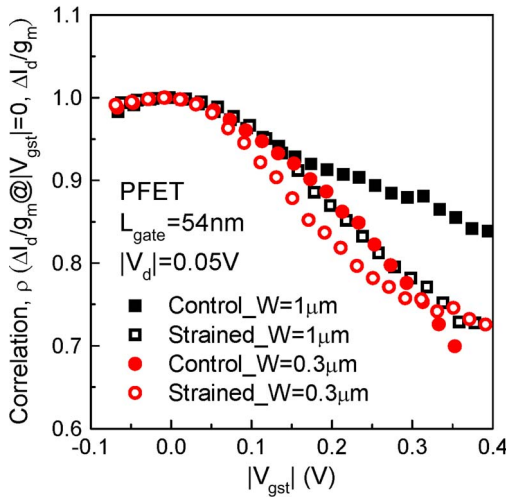

Fig. 12. Correlation (ρ) between $(\Delta I_d)/g_m$ at $V_{\rm gst} = 0$ and $(\Delta I_d)/g_m$ at other $|V_{\rm gst}|$ versus $|V_{\rm gst}|$. The high correlation coefficient ensures the relevance of ΔV_t to $\Delta I_d/I_d$.

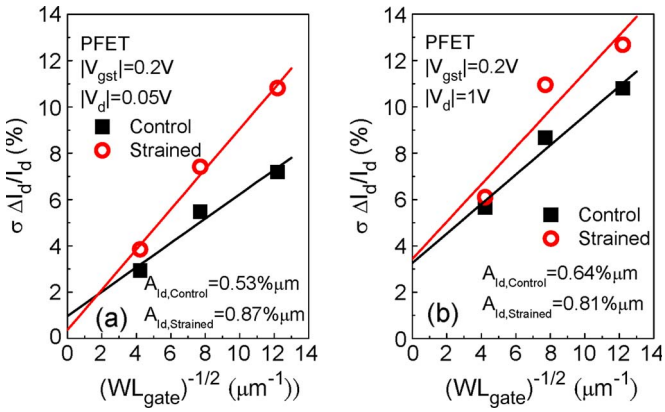

Fig. 13. Drain–current mismatch $\sigma(\Delta I_d)/I_d$ versus $(WL_{\rm gate})^{-0.5}$ shows larger area dependence of $\sigma(\Delta I_d)/I_d$ at $|V_{\rm gst}| = 0.2$ V and (a) $|V_d| = 0.05$ V and (b) $|V_d| = 1$ V.

the channel strain is gate-length dependent in process-induced uniaxial strained devices [5]. Fig. 13 shows that the area dependence of $\sigma(\Delta I_d)/I_d$, $A_{\rm Id}$, for the strained device is larger than that of the control device. To determine whether it is due to the discrepancy in $\Delta V_{\rm th}$, the Pelgrom plot of $\Delta V_{\rm th}$ is shown in Fig. 14. It can be seen that the area dependences of $\sigma(\Delta V_{\rm th})$, $A_{\rm Vth}$, for strained and control devices are almost the same. Therefore, it can be concluded that the increased drain–current mismatch of the strained device for a given $V_{\rm gst}$ results from the enhanced g_m/I_d [see Eq. (1)]. Fig. 15 further shows that, for a given g_m/I_d, the $\sigma(\Delta I_d)/I_d$ for the strained and control devices are nearly identical.

VI. Conclusion

Important analog properties, including low-frequency noise and device mismatch, of uniaxial strained PMOSFETs with sub-100 nm gate length have been investigated. The g_m/I_d for the strained device is higher than its control counterpart because of the higher V_g sensitivity of the carrier mobility present in the strained device. The dc gain and VIP_3 of the strained device are almost the same as those of the unstrained one.

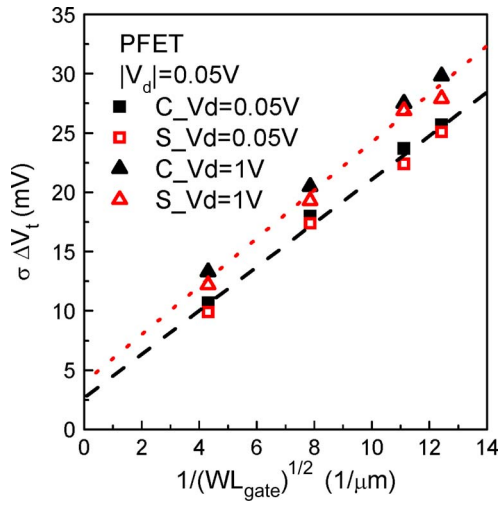

Fig. 14. Threshold voltage mismatch $\sigma(\Delta V_t)$ versus $(WL_{\rm gate})^{-0.5}$ shows similar area dependence of $\sigma(\Delta V_t)$ for the strained and control devices.

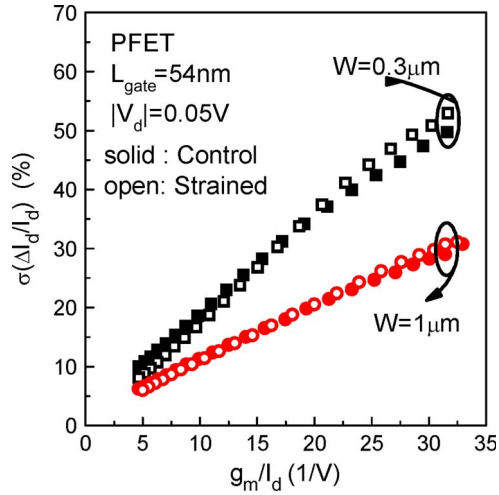

Fig. 15. Drain–current mismatch $\sigma(\Delta I_d)/I_d$ versus g_m/I_d for devices with $L_{\rm gate} = 54$ nm at $|V_d| = 0.05$ V shows nearly identical drain–current mismatch for the strained and unstrained devices.

The increased drain current noise spectral density and drain current mismatch for the strained device under constant gate voltage overdrive can be attributed to the enhanced g_m/I_d. Nevertheless, the low-frequency noise and matching properties for strained and unstrained devices are nearly identical at a given g_m/I_d. This paper may provide insights for analog design using advanced strained devices.

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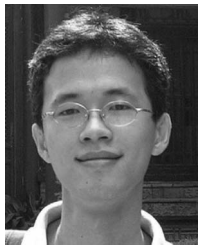

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