Single-Stage Soft-Switching AC–DC Converter With Input-Current Shaping for Universal Line Applications

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***Abstract*—In this paper, a novel single-stage soft-switching ac–dc converter for universal line applications is presented. Unlike the conventional single-stage designs, the proposed input-current shaping scheme is intentionally arranged to be charged in the duty-off time. With this design, the switch current stress in the duty-on time is significantly reduced. Meanwhile, this design produces ac modulation effect on the charging time of the boost inductor so that the input $i-\nu$ curve drawn by the proposed converter has nearly linear relationship. Moreover, an active-clamp flyback–forward topology is used as the downstream dc–dc cell to alleviate voltage stress across the bulk capacitor. By deactivating the flyback subconverter and keeping the forward subconverter supplying the output power at light-load condition, the bulk-capacitor voltage can be alleviated effectively and guaranteed below 450 V in wide ranges of output load and line input (90–265 V_{rms}). Experimental results, obtained from a prototype circuit with 20-V/100-W output, have verified that three achievements can be obtained simultaneously, including the compliance with the line-current harmonic regulations, the reliable alleviation of the bulk-capacitor voltage stress, and the substantially promoted conversion efficiency.**

***Index Terms*—AC–DC converter, input-current shaping (ICS), single stage, soft switching.**

I. Introduction

OWING TO the growing concern about the harmonic pollution of power conversion equipment and the adoption of agency standards such as IEC 61000-3-2, it becomes imperative to embed a function of power factor correction (PFC) or input-current shaping (ICS) in ac–dc converters. Therefore, many studies have examined the relevant issues, and numerous topologies have been proposed [1]–[18]. The most common approach is of two-stage circuit configuration [1]–[3]. In this method, a boost-type converter is employed at the front end to force the line current to track the line voltage. This PFC stage is then followed by a dc–dc converter to provide isolation and the desired regulated output voltage. However, this type of design increases the circuit complexity and cost since the separate PFC stage needs additional components and control circuits. This drawback is undesired in low-power applications, for which circuit complexity and cost are often the dominant concerns.

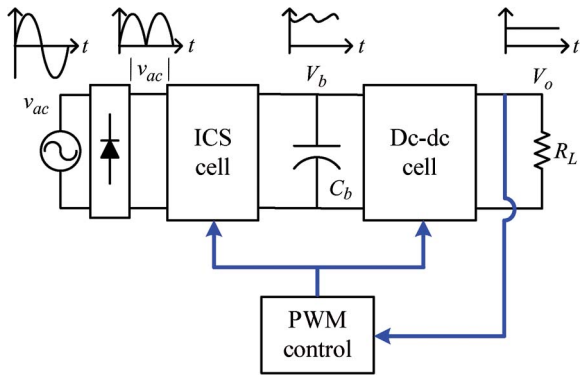

Fig. 1. Functional block diagram of a typical single-stage ac–dc converter.

To reduce the component count and the cost, many feasible single-stage ac–dc converters have been proposed [4]–[17]. With the consideration of the input current quality and output regulation, this type of converter contains two primary circuit parts, as shown in Fig. 1. Those are a boost-type ICS cell and an isolated dc–dc cell. They share the same power switch while saving an active switch and a PFC controller. Only a pulsewidth-modulation (PWM) controller is needed for regulating the output voltage. Additionally, an internal bulk capacitor C_b is used to handle the instantaneous difference between the varying input power and a constant output power. Because the bulk capacitor is sufficiently large, the bulk-capacitor voltage V_b can keep in the condition with small ripple. Thus, the switch duty ratio is almost constant during a half line cycle in the steady state, and the line current can automatically track the line voltage by operating the boost inductor in discontinuous conduction mode (DCM). This design concept is namely the voltage-follower PFC technique [2] or the self-PFC property [3].

Moreover, for the dc–dc regulator circuit, working in the continuous conduction mode (CCM) is usually the preferred mode of operation due to the lower turn-off loss and smaller current stress on the semiconductor devices. Therefore, the combination of a DCM ICS cell and a CCM dc–dc cell is the primary selection for single-stage ac–dc converters. However, the approach has an undesirable feature: The bulk-capacitor voltage arises while the load becomes light. This is due to the average power imbalance between the input and output [12]. It is worth mentioning that an excessively high V_b might be

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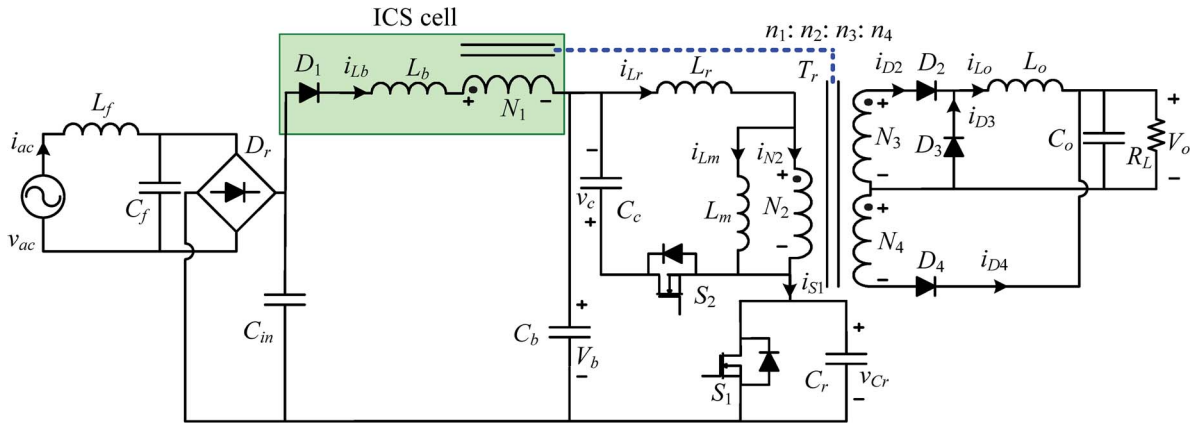

Fig. 2. Proposed single-stage soft-switching ac–dc converter.

produced at high line and light-load operation, which makes the single-stage designs impractical for the applications that require a universal input voltage of 90–265 V_{rms} [11], [12]. To alleviate high bulk-capacitor voltage stress, different methods have been presented [8]–[14]. It is believed that the approach of operating the dc–dc cell in DCM is the most effective and simplest since the addition of extra coupled winding or external circuits is not needed [8], [9]. In this scheme, when the output power decreases, the duty ratio automatically decreases. Consequently, the input power decreases too, and V_b is independent of load variation [8]. However, the resulting high rms current requires a high-current-rating switch and reduces the conversion efficiency, as compared with the CCM dc–dc design. This feature is particularly unfavorable for low-voltage high-current output applications. Furthermore, for the single-stage designs, there is another unavoidable problem. Since the ICS and dc–dc cells are driven by one common switch, both the boost-inductor current and the transformer current simultaneously flow through the switch in the duty-on time. As a result, the switch current stress is relatively high, and more power loss will be introduced too.

In this paper, a novel single-stage ac–dc converter with the configuration shown in Fig. 2 is proposed. The proposed topology is derived from an active-clamp flyback–forward converter plus few additional components for ICS. Through the cooperation of the auxiliary winding N_1, two special functions are provided. First, the boost inductor L_b is charged in the duty-off time; therefore, the current stress on the main switch S_1 is alleviated. Second, in conventional single-stage converters with boost-type ICS cells, the input line current, composed of the average charging and discharging currents of the boost inductor, has quadratic relation to the input line voltage. In the proposed design, the charging time of the boost inductor is designed to be inversely modulated by the instantaneous line voltage, so that the input i–ν curve of the average charging current of the boost inductor can compensate the quadratic deformation presented in the input i–ν curve of the average discharging current. Hence, the line current has the waveform that is analogous to the line-voltage waveform. Moreover, the flyback and forward subconverters are designed to operate in CCM and DCM, respectively. The design objective is to deactivate the flyback subconverter and keep the forward subconverter providing the output power when the converter operates in light-load condition. With the proper arrangement of circuit parameters, the input power can adequately decrease so that the bulk-capacitor voltage alleviation effect can be obtained. The proposed converter is built and tested with 20-V/100-W output. Experimental results show that the bulk-capacitor voltage can be held below 427 V at 265-V_{rms} line input in a wide range of output load. Furthermore, the maximum efficiency at full load is 91.3%, and the measured line-current harmonics satisfy the IEC 61000-3-2 Class D requirements.

II. Proposed Converter

A. Circuit Configuration

The proposed converter, shown in Fig. 2, is derived from a center-tapped flyback–forward converter with the addition of the auxiliary circuit. The auxiliary circuit forms the ICS cell, and the center-tapped flyback–forward converter forms the dc–dc cell. In the proposed converter, a multiwinding transformer T_r is employed. It includes four windings N_1, N_2, N_3, and N_4 with turn numbers n_1, n_2, n_3, and n_4, respectively, and the primary magnetizing inductance L_m. As marked by the shaded area in Fig. 2, the ICS circuit, consisting of the rectifier diode D_1, boost inductor L_b, and auxiliary winding N_1, is inserted between the full-bridge rectifier D_r and the bulk capacitor C_b. The purpose of this circuit is to force the boost-inductor current to be discontinuous and ac modulated to achieve inherent PFC. The diode D_1 is used to provide fast rectification and prevent the filter capacitor $C_{\rm in}$ from being charged by the reverse current of i_{Lb}. Different from the conventional ICS schemes, bulk capacitor C_b is intentionally connected to the undotted end of winding N_1. Through the winding N_1 with enough large turns, the coupled voltage $-V_o \cdot n_1/n_4$ across winding N_1 can force to charge L_b during the duty-off time. Therefore, the current stress of the main switch S_1 can be reduced.

The ICS cell is then followed by an active-clamp flyback–forward circuit which provides isolation and postregulation function. The capacitors C_b and C_o are used for filtering and energy storage. C_r represents the sum of the parasitic capacitances contributed by main switch S_1 and auxiliary switch S_2. L_r represents the sum of the transformer leakage inductance and an external inductor, which forms a series resonant circuit

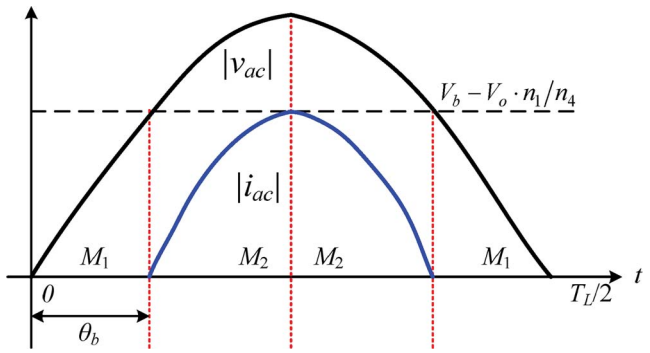

Fig. 3. Operation modes in a half line cycle.

with C_r to enable soft-switching function. The resonant inductor L_r, the clamping capacitor C_c, and the auxiliary switch S_2 form the main part of the active-clamp circuit for limiting the turn-off voltage spike of S_1. The combined structure of flyback and forward circuits using a center-tapped transformer ensures that the energy can be always transferred to the load, irrespective of the state of main switch S_1. In addition, the flyback subconverter is designed to operate in CCM for providing a reflected voltage v_{N1} from the output voltage during the duty-off time. The forward subconverter is designed to operate in DCM all the time even in light-load condition when the flyback subconverter is inactive. Furthermore, the control circuit can be implemented by a simple control loop, a common PWM controller, and a driver circuit.

B. Operating Principles

To simplify the analysis, the following assumptions are made.

1) The switching and conduction losses of the components are neglected.
2) The rectified line voltage $|\nu_{\rm ac}|$ is considered constant during a switching period.
3) The bulk-capacitor voltage V_b and the output capacitor voltage V_o are ripple-free dc in each half line cycle.
4) The leakage inductances of the transformer are neglected.

In each half line cycle, the converter has two operation modes, M_1 and M_2, as shown in Fig. 3. In mode M_1, the rectified line voltage $|\nu_{\rm ac}|$ is lower than $V_b - V_o \cdot n_1/n_4$; thus, diode D_1 is reverse biased, and no line current $I_{\rm ac}$ is formed. In this circumstance, the converter simply operates as an active-clamp flyback–forward dc–dc converter. While $|\nu_{\rm ac}|$ is higher than $V_b - V_o \cdot n_1/n_4$, the converter operates in mode M_2, in which L_b can provide the voltage-boost function, and thus, the line current is established. From the definition of operation modes, the boundary angle θ_b between modes M_1 and M_2 can be obtained as

$$\theta_b = \sin^{-1}\left(\frac{V_b - V_o \cdot n_1/n_4}{|V_{\rm ac(pk)}|}\right) \tag{1}$$

where $|V_{\rm ac(pk)}|$ is the peak rectified line voltage. Furthermore, Fig. 4 shows the topological states of the converter during one switching period. Referring to the symbol definitions, topological states, and key waveforms shown in Figs. 2, 4, and 5, respectively, the detailed operation is explained as follows.

State 1: [Fig. 4(a), $t_0 \le t < t_1$]

In this state, switch S_1 is on and switch S_2 is off. From KVL, the bulk-capacitor voltage V_b equals the sum of the voltage across resonant inductor L_r and the primary winding voltage ν_{N2}. The positive voltage across winding N_2 induces a positive voltage across the secondary winding N_3. Thus, the output inductor current flows through diode D_2, and diodes D_3 and D_4 are reverse biased. Since V_b is approximately constant, both the magnetizing inductance L_m and resonant inductor L_r are linearly magnetized. The voltage and current at the transformer primary side can be obtained as

$$\nu_{N2,t0} = \frac{\frac{V_b}{L_r} + \frac{n_3}{n_2}\frac{V_o}{L_o}}{\frac{1}{L_r} + \frac{1}{L_m} + \left(\frac{n_3}{n_2}\right)^2 \frac{1}{L_o}} \tag{2}$$

$$i_{Lr}(t) = i_{Lm}(t_0) + \frac{\nu_{N2,t0}}{L_m} \cdot (t - t_0) + \frac{n_3}{n_2} \cdot \left(i_{Lo}(t_0) + \frac{\nu_{N2,t0} \cdot n_3/n_2 - V_o}{L_o} \cdot (t - t_0)\right) \tag{3}$$

where

$$i_{Lo,M1}(t_0) = 0 \tag{4}$$

$$i_{Lo,M2}(t_0) = \frac{\nu_{N2,t7} \cdot n_3/n_2 - V_o}{L_o} \cdot D_{s8}T_s \tag{5}$$

with $D_{s8}T_s$, which is equal to $(t_8 - t_7)$, being the duration occupied by State 8. In this state, since the large positive voltage presents across winding N_1, no current flows through L_b. Note that the body diode of S_1 is always cut off in mode M_2.

State 2: [Fig. 4(b), $t_1 \le t < t_2$]

At t_1, S_1 is turned off. The resonant capacitance C_r is charged by the transformer primary side current i_{Lr}. Since C_r is very small, ν_{Cr} rises almost linearly from zero to V_b in a short time.

State 3: [Fig. 4(c), $t_2 \le t < t_3$]

At t_2, ν_{Cr} rises to a high value that makes the primary side voltage ν_{N2} equal to zero. Thus, both the secondary side diodes D_2 and D_3 conduct, and the output inductor current decreases linearly. The resonant tank in this state consists of L_r and C_r.

State 4: [Fig. 4(d), $t_3 \le t < t_4$]

At t_3, ν_{Cr} rises to a value making the body diode of S_2 conduct. Since the clamp capacitor C_c is much greater than the resonant capacitor C_r, the resonant tank is dominated by L_r and C_c. Furthermore, the increase of ν_{Cr} causes i_{Lr} to decrease. Consequently, the diode current i_{D2} keeps decreasing until $i_{D2} = 0$, and contrarily, the diode current i_{D3} increases until $i_{D3} = i_{Lo}$. Before i_{D2} decreases to zero, the primary side voltage v_{N2} still keeps zero value.

State 5: [Fig. 4(e) or 4(f), $t_4 \le t < t_5$]

At t_4, $i_{D2} = 0$ and $i_{D3} = i_{Lo}$. After time t_4, the fast varying current i_{Lr} decreases to a value that is smaller than i_{Lm}; thus, the winding current i_{N2} turns to negative. According to Ampere's law, the winding current i_{D4} will be induced correspondingly. The fact that diode D_4 conducts results in the voltage ν_{N2} being clamped at $-V_o \cdot n_2/n_4$. Shortly, S_2 is turned on before i_{Lr} resonates to the negative direction; thus,

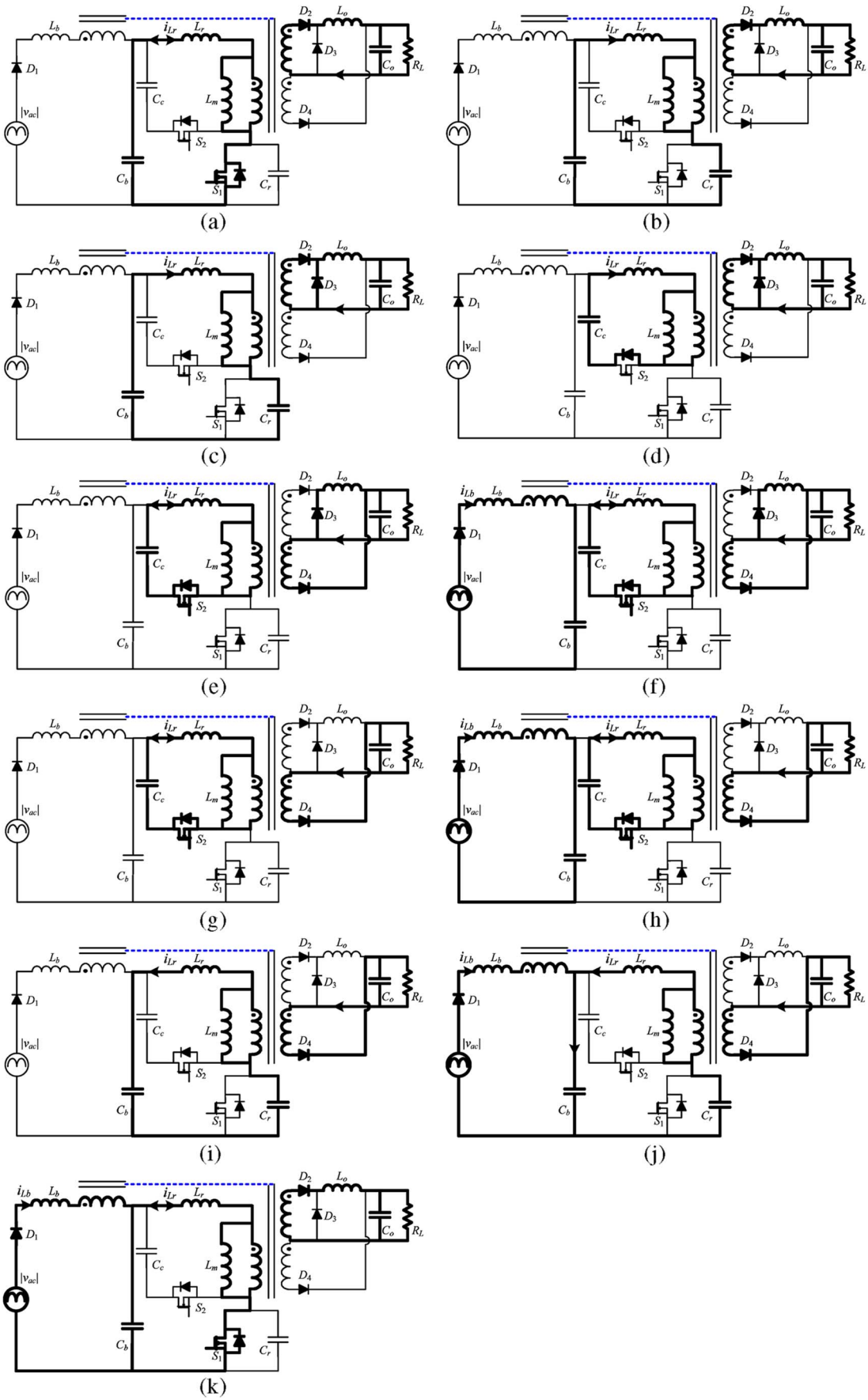

Fig. 4. Topological states of the proposed converter. (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5 for mode M_1. (f) State 5 for mode M_2. (g) State 6 for mode M_1. (h) State 6 for mode M_2. (i) State 7 for mode M_1. (j) State 7 for mode M_2. (k) State 8.

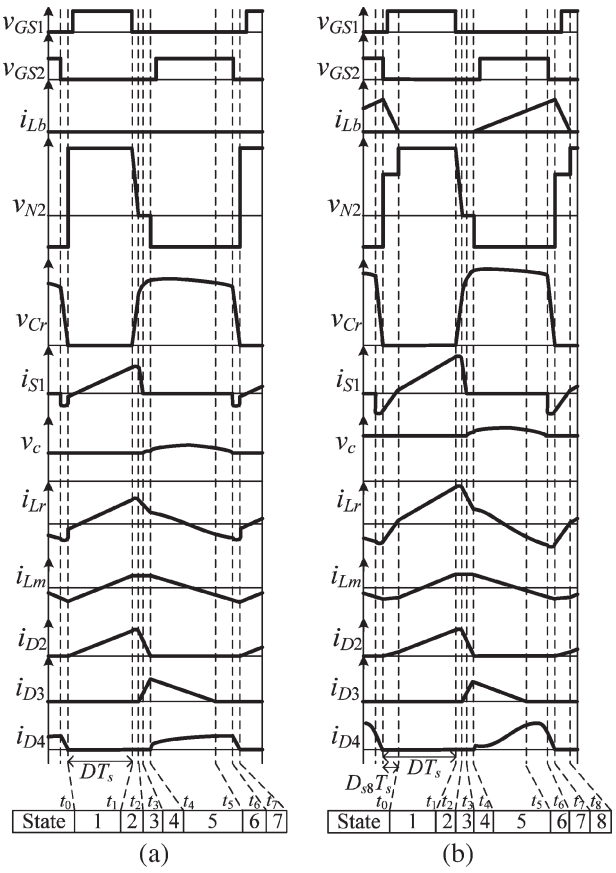

Fig. 5. Steady-state waveforms of the proposed converter in (a) mode M_1 and (b) mode M_2.

zero voltage switching (ZVS) of S_2 is achieved. The resonant tank in this state is formed by L_r and C_c. Within this state, ν_{N1} turns to negative. If $|\nu_{\rm ac}|$ is greater than $V_b - V_o \cdot n_1/n_4$, i.e., in mode M_2 operation, the current i_{Lb} will be generated and is given as follows:

$$i_{Lb}(t) = \frac{1}{L_b}\left(|\nu_{\rm ac}(t)| + \frac{n_1}{n_4}V_o - V_b\right)\cdot(t - t_4). \quad (6)$$

In such a design, the winding N_1 also resets a partial energy stored in L_m to C_b. When i_{Lo} reduces to zero, this state ends. Meanwhile, the DCM operation of L_o is achieved, and D_2 and D_3 are reverse biased.

State 6: [Fig. 4(g) or 4(h), $t_5 \le t < t_6$]

This circuit analysis in this state is the same as that in State 5, except that the output inductor current is zero.

State 7: [Fig. 4(i) or 4(j), $t_6 \le t < t_7$]

At t_6, S_2 is turned off. C_c is disconnected, and L_r and C_r form a new high-frequency resonant circuit. The transformer primary side current i_{Lr} resonates in the negative direction to discharge C_r; therefore, ν_{Cr} decreases from $\nu_c(t_6) + V_b$ to zero, and then, ν_{N2} turns to positive. At t_7, i_{D4} decreases to zero, and after that, D_4 becomes reverse biased. Since the downslope of di_{D4}/dt is determined by the resonant speed, D_4 can be designed to switch softly to reduce the rectifier switching loss. For the mode M_2 case, the current i_{Lb} increases linearly with the same slope as that expressed in (6).

State 8: [Fig. 4(k), $t_7 \le t < t_8$]

At t_7, the body diode of S_1 conducts. Shortly after time t_7, while the body diode of S_1 is conducting, S_1 is turned on to achieve ZVS operation. Since $|\nu_{\rm ac}|$ is smaller than $\nu_{N1} + V_b$, the boost-inductor current i_{Lb} linearly decreases and becomes zero at time t_8 $(= t_0)$. The aforementioned operation gives

$$i_{Lb}(t) = i_{Lb}(t_7) + \frac{|\nu_{\rm ac}| - \nu_{N1,t7} - V_b}{L_b}\cdot(t - t_7) \quad (7)$$

where

$$\nu_{N1,t7}(t) = \frac{\frac{n_1(|\nu_{\rm ac}(t)|-V_b)}{n_2L_b} + \frac{V_b}{L_r} + \frac{n_3V_o}{n_2L_o}}{\frac{L_r+L_m}{L_rL_m} + \left(\frac{n_1}{n_2}\right)^2\frac{1}{L_b} + \left(\frac{n_3}{n_2}\right)^2\frac{1}{L_o}}\cdot\frac{n_1}{n_2}. \quad (8)$$

It should be noted that when the converter operates in mode M_1, this state does not exist.

C. Steady-State Analysis

Based on the circuit analysis of the proposed converter introduced in the previous section, States 2–4 and 7 can be neglected in the steady-state analysis because these four intervals are very short as compared with the total switching period. By employing the voltage-second balance across L_m, one can obtain

$$\nu_{N2,t0}\cdot(D - D_{s8}) - \frac{n_2}{n_4}V_o\cdot(1-D) + \nu_{N2,t7}\cdot D_{s8} = 0 \quad (9)$$

where D_{s8} is defined as $(t_8 - t_7)/T_s$. Similarly, by employing the voltage-second balance across L_r and neglecting the small oscillation term of V_c, one can obtain

$$(V_b - \nu_{N2,t0})\cdot(D - D_{s8}) - \left(V_c - \frac{n_2}{n_4}V_o\right)\cdot(1-D) + (V_b - \nu_{N2,t7})D_{s8} = 0. \quad (10)$$

Also, the voltage-second balance across L_b gives

$$\left(|\nu_{\rm ac}| + \frac{n_1}{n_4}V_o - V_b\right)\cdot(1-D) + \left(|\nu_{\rm ac}| - \frac{n_1}{n_2}\nu_{N2,t7} - V_b\right)\cdot D_{s8} = 0. \quad (11)$$

In mode M_1, since D_{s8} does not exist, the duty ratio in mode M_1, D_{M1}, can be obtained from (9)

$$D_{M1} = \frac{V_o}{\nu_{N2,t0}\cdot n_4/n_2 + V_o}. \quad (12)$$

According to (11), the time function of D_{s8} is obtained as

$$D_{s8}(t) = \frac{|\nu_{\rm ac}(t)| + \frac{n_1}{n_4}V_o - V_b}{\frac{n_1}{n_2}\nu_{N2,t7}(t) + V_b - |\nu_{\rm ac}(t)|}\cdot(1 - D_{M2}(t)). \quad (13)$$

Adding (9) to (10), the clamp-capacitor voltage can be obtained by

$$V_c = \frac{D}{1-D}V_b. \quad (14)$$

According to (10) and (13), the clamp-capacitor voltage in mode M_2 can be further expressed as

$$\nu_{c,M2}(t) = \left[\frac{n_2}{n_4}V_o + \frac{|\nu_{\rm ac}(t)| + \frac{n_1}{n_4}V_o - V_b}{\frac{n_1}{n_2}\nu_{N2,t7}(t) + V_b - |\nu_{\rm ac}(t)|} \cdot (\nu_{N2,t0}(t) - \nu_{N2,t7}(t))\right] \cdot \frac{V_b}{\nu_{N2,t0}}. \quad (15)$$

Thus, from (14) and (15), the time function of the duty ratio in mode M_2 is given by

$$D_{M2}(t) = \frac{\nu_{c,M2}(t)}{V_b + \nu_{c,M2}(t)}. \quad (16)$$

III. Design Considerations

The design specifications of the proposed converter are given as follows: the input voltage range $V_{\rm ac} = 90$–265 $V_{\rm rms}$, output voltage $V_o = 20$ V, rated output power $P_o = 100$ W, and switching frequency $f_s = 100$ kHz. To obtain higher conversion efficiency, the duty ratio range is designed from 0.15 to 0.4. The conversion efficiency η is assumed to be 0.85.

With the consideration of the voltage limitation of commercially available electrolytic capacitors, the maximum bulk-capacitor voltage is needed to be kept below 450 V. Moreover, according to the empirical rule, the moderate value of V_b usually ranges between 1.1 and 1.2 times as high as $V_{\rm ac(pk)}$. However, when $V_{\rm ac} = 265$ $V_{\rm rms}$, the possible maximum value of V_b equals $265 \times \sqrt{2} \times 1.2 = 449.7$, and the value is very close to 450 V. Therefore, in the following design, the target maximum value of V_b, $V_{b,max}$, is chosen to be 1.15 times as high as $V_{\rm ac(pk)}$ at 265-$V_{\rm rms}$ line input. To ensure that the proposed converter operates properly, the circuit parameters including n_2/n_3, n_2/n_4, n_1/n_4, L_r, L_m, L_o, and L_b are determined as follows.

A. Determining the Turns Ratio n_2/n_3

Let $L_m \gg L_r$; thus, the voltage $\nu_{N2,t0}$ is approximated to be V_b. To ensure the DCM operation for the forward subconverter, the primary-to-secondary turns ratio n_2/n_3 should satisfy the following condition:

$$\frac{n_2}{n_3} > \frac{V_{b,\min} D_{\max}}{V_o}. \quad (17)$$

B. Determining the Turns Ratio n_2/n_4

The proposed converter is designed to operate the forward subconverter in DCM and flyback subconverter in CCM. With this design, the bulk voltage can be easily alleviated in the worse case, i.e., the high line input with light-load condition, by deactivating the flyback subconverter. The aforesaid function can be achieved by manipulating the voltage of C_c. In the high line with the light-load case, since D becomes smaller, lower V_c and v_{N2} will be formed. Thus, the induced voltage across N_4, $-\nu_{N4}$, can be designed to be insufficient to forward bias D_4 so that the flyback subconverter is inactive. Based on the aforementioned concept, the following condition must be satisfied:

$$V_{c,\min} \cdot n_4/n_2 < V_o. \quad (18)$$

By substituting (14) into (18), the ratio of n_2/n_4 can be found

$$\frac{n_2}{n_4} = \frac{V_{b,\max}}{V_o} \cdot \frac{D_{\min}}{1 - D_{\min}}. \quad (19)$$

C. Determining the Turns Ratio n_1/n_4

The design objective of determining n_1/n_4 is to find its minimum value with which the input current harmonics can meet the IEC 61000-3-2 Class D requirements. According to (1), the selection of n_1/n_4 is equivalent to the selection of the boundary angle. Thus, the design objective becomes finding the maximum acceptable boundary angle. Since IEC 61000-3-2 Class D gives the requirements of the acceptable harmonics, each input current harmonic should be computed to find the maximum acceptable boundary angle. Since the line current is an analogous sinusoid waveform, the line current during $[\theta_b, \pi - \theta_b]$ can be expressed as

$$i_{\rm ac}(\omega t) = i_{\rm ac}\left(\frac{\pi}{2}\right) \cdot \sin\left((\omega t - \theta_b) \cdot \frac{\pi}{\pi - 2\theta_b}\right) \quad (20)$$

where ω is the angular frequency of the line voltage. Thus, the nth harmonic component I_n can be calculated by Fourier analysis

$$I_n = \frac{\pi - 2\theta_b}{\pi} \cdot i_{\rm ac}\left(\frac{\pi}{2}\right) \cdot \left\{[\sin((n-1)\pi - n\theta_b) - \sin(n\theta_b)] \cdot \frac{1}{(n-1)\pi - 2n\theta_b} - [\sin((n+1)\pi - n\theta_b) - \sin(n\theta_b)] \cdot \frac{1}{(n+1)\pi - 2n\theta_b}\right\} \quad (21)$$

where $n = 1, 3, 5 \ldots 39$.

Consider the Class D regulations that are defined as the ratios of the current harmonics to fundamental-frequency component, I_n/I_1, as long as the output power is determined and no phase displacement exists between the line current and voltage. From (21), we can obtain the normalized value of each harmonic as a function of the boundary angle, as shown in Fig. 6. Fig. 6 shows that the most critical harmonic is the fifth one for complying with the Class D requirements since its acceptable boundary angle is smaller than all the others. Therefore, the maximum allowable boundary angle is 1.005 rad ($= 57.58^\circ$). Next, the turns ratio n_1/n_4 can be obtained by rearranging (1)

$$\frac{n_1}{n_4} = \frac{V_b - V_{\rm ac(pk)} \sin\theta_b}{V_o}. \quad (22)$$

In the proposed converter, a higher line-input voltage causes a larger boundary angle. Thus, we must make sure that the

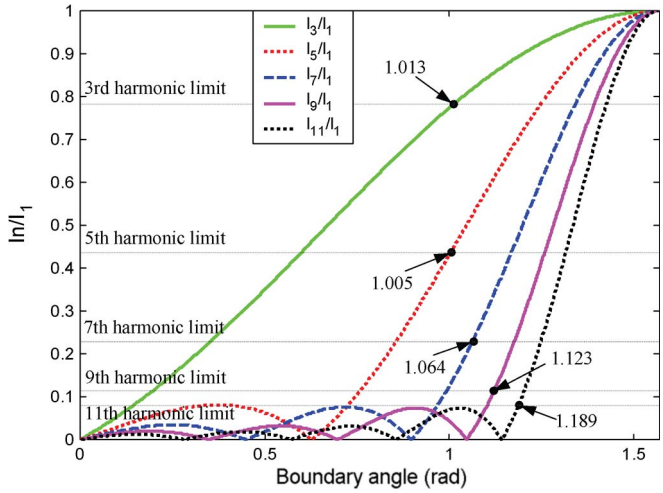

Fig. 6. Maximum boundary angles of 3rd–11th harmonics complying with IEC 61000-3-2 Class D requirements.

design satisfies the requirements of the Class D, specifically at the nominal high line input, which is 230 $V_{\rm rms}$. Substituting $V_b = 1.15 \cdot V_{\rm ac(pk)}$ into (22), we obtain $n_1/n_4 = 4.97$ when $V_{\rm ac} = 230$ $V_{\rm rms}$ and $\theta_b = 1.005$ rad. In other words, $n_1/n_3 = 4.97$ is the boundary complying with Class D limits.

D. Determining the Resonant Inductor L_r

According to the operating principle of State 7, to ensure the ZVS turn-on for S_1, the energy stored in the resonant inductor L_r must be greater than the energy stored in the resonant capacitor C_r. Thus, for the given C_r contributed by the parasitic capacitances of S_1 and S_2, the following relationship should be guaranteed:

$$L_r > \frac{C_r \cdot \left(V_{b,\max} + \frac{n_2}{n_4} V_o\right)^2}{\left(i_{s1,M1}(t_6)\right)^2}. \tag{23}$$

E. Determining the Transformer Primary Magnetizing Inductance L_m

With the design consideration that the flyback subconverter is inactive at high line and light-load condition, the output power provided by the flyback subconverter at 265 $V_{\rm rms}$ and full-load situation is designed to be lower than $P_o/2$. Meanwhile, this subconverter is designed to always operate in CCM at full load. Thus, the inductance L_m must satisfy (24), shown at the bottom of the page.

F. Determining the Output Inductor L_o

According to energy conservation and the design consideration of L_m, the output power provided by the forward subconverter at 265 $V_{\rm rms}$ should be greater than $P_o/2$. To fulfill this design and ensure that L_o always operates in DCM, the following relationship should be guaranteed:

$$L_o < \min\left(\frac{D_{\min}^2 T_s \eta}{P_o} \cdot \left(V_{b,\max}\frac{L_m}{L_m + L_r} \cdot \frac{n_3}{n_2} - V_o\right)^2, \frac{\frac{n_3}{n_2} V_o \cdot \left(\frac{1-D_{\max}}{D_{\max}}\right)}{\frac{V_{b,\min}}{L_r} - \frac{n_2 V_o}{n_3 D_{\max}}\left(\frac{1}{L_m} + \frac{1}{L_r}\right)}\right). \tag{25}$$

G. Determining the Boost Inductor L_b

To achieve the self-PFC property, the boost inductor must operate in DCM over the entire half line cycle. Thus, the design must satisfy the condition of $D_{s8} < D$ in the whole half line cycle. Since the critical boundary condition of CCM and DCM occurs at the lowest peak input voltage, the maximum boost inductance [(26), shown at the bottom of the page] can be determined from (13).

Based on (17)–(26), we choose the desired circuit parameters as follows: the turns of $n_1/n_2/n_3/n_4 = 35/24/9/7$, $L_r = 15$ μH, $L_m = 329$ μH, $L_o = 20$ μH, and $L_b = 105$ μH. Additionally, the determination of C_c is similar to that of the conventional active-clamp flyback converter, and we select C_c to be 0.6 μF. The determination of C_b depends on the desired hold-up time, and the corresponding curves have been drawn in [18]. Inspecting those curves, C_b can be chosen as 300 μF so that 20-ms hold-up time of the proposed converter can be reached.

$$L_m > \frac{\left(\frac{n_2}{n_4} V_o\right)^2}{\frac{n_2}{n_4} \cdot \frac{-\frac{V_{b,\max} V_o D_{\min}}{1-D_{\min}} + \frac{n_2}{n_4} V_o^2}{L_r} - \frac{n_1}{n_4} \cdot \frac{V_o \cdot \left(|V_{\rm ac,pk}| + \frac{n_1}{n_4} V_o - V_{b,\max}\right)}{L_b} - \frac{P_o}{(1-D_{\min})^2 T_s \eta}} \tag{24}$$

$$L_{b,\max} = \frac{\frac{n_1}{n_2} \cdot \left(\frac{1-D_{\max}}{D_{\max}}\right) \cdot \left(V_{\rm ac(pk),min} - V_{b,\min} + \frac{n_1}{n_4} V_o\right)}{\frac{V_{b,\min}}{L_r} + \frac{n_3 V_o}{n_2 L_o} - \frac{n_2}{n_1 D_{\max}}\left[V_{\rm ac(pk),min} - V_{b,\min} + \frac{n_1}{n_4} V_o (1 - D_{\max})\left(\frac{L_r + L_m}{L_r L_m} + \left(\frac{n_3}{n_2}\right)^2 \frac{1}{L_o}\right)\right]} \tag{26}$$

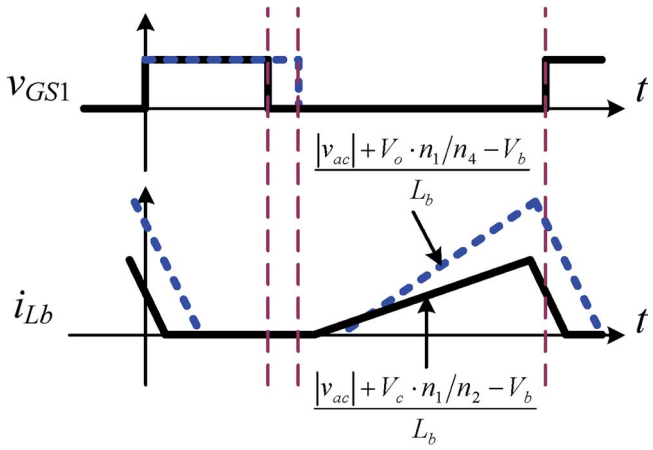

Fig. 7. Duty-on duration change of S_1 and the boost-inductor current change relating to the load change.

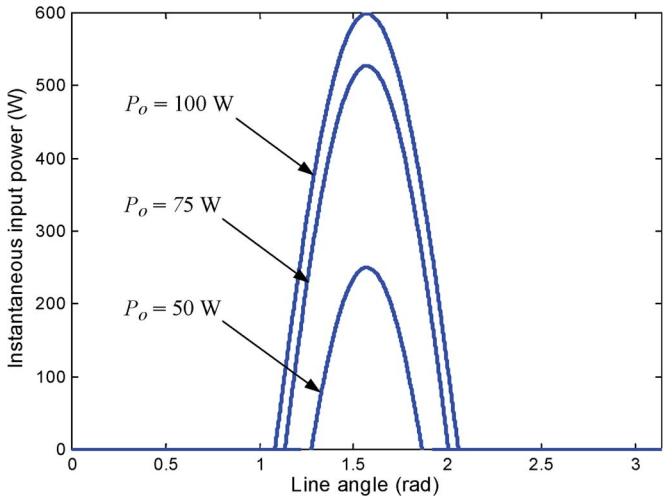

Fig. 8. Variations of instantaneous input power for different loads.

IV. Mechanism for Suppressing Bulk-Capacitor Voltage Stress

To clarify the mechanism for alleviating bulk-capacitor voltage stress in the proposed converter, the analysis of the boost-inductor currents at heavy load and light loads is performed as follows. Fig. 7 shows both the duty-on duration change of S_1 and the boost-inductor current change in a switching period relating to the load change. At the rated condition, both the forward and flyback subconverters work normally. Therefore, the boost inductor is charged by the voltage $|\nu_{\rm ac}| + V_o \cdot n_1/n_4 - V_b$ since the voltage ν_{N1} is reflected from the output side during the duty-off time, as shown by the dashed lines of Fig. 7.

When the load decreases, the bulk-capacitor voltage increases due to the power imbalance between the input and the output. Meanwhile, the duty ratio decreases correspondingly to keep the constant output voltage in CCM operation. When the load decreases further, the reduced clamp-capacitor voltage caused by the decreased duty ratio cannot induce the voltage $-\nu_{N4}$ higher enough to forward bias D_4. Thus, the flyback subconverter is inactive, and only the forward subconverter keeps supplying the output power. In this condition, the voltage ν_{N1} is reflected from the clamp-capacitor voltage instead of the output voltage. Therefore, the boost inductor is charged by the approximate voltage $|\nu_{\rm ac}| + V_c \cdot n_1/n_2 - V_b$, as shown by the solid lines of Fig. 7, where V_c is determined by the duty ratio, as shown in (14). Since the value of $V_c \cdot n_1/n_2$ is smaller than that of $V_o \cdot n_1/n_4$, the solid triangle will have a small area, and a reduced boost-inductor current is produced. With the proper arrangement of turns ratios between N_1, N_2, and N_4, the reduced quantity of input current can yield the result that V_b is alleviated at light load.

Consider that the values of V_b at full and light loads cannot be solved analytically. Instead, we examine the change of input power under load variation. Fig. 8 shows the variations of instantaneous input power for different load conditions under the assumption of constant bulk-capacitor voltage. These curves are sketched by using the parameters obtained in Section III for $V_{\rm ac} = 265$ $\rm V_{rms}$ and $V_b = 1.15 \cdot V_{\rm ac(pk)}$. From Fig. 8, it can be seen that the input power always decreases as the load is reduced. After the average calculation over a half line cycle, the ratio of change rates of the average input power to the average output power, $\Delta P_{\rm in(ave)}/\Delta P_{o(\rm ave)}$, can be obtained as 1.06 when the load is changed from P_o to (3/4)P_o, and the value of $\Delta P_{\rm in(ave)}/\Delta P_{o(\rm ave)}$ is 2.55 when the load is changed from (3/4)P_o to (1/2)P_o. Since the reduction of $P_{\rm in(ave)}$ is greater than that of $P_{o(\rm ave)}$, the actual bulk-capacitor voltage must decrease to maintain the input and output average power balance. Meanwhile, the actual bulk-capacitor voltage has a gradual decrease with the reduction of output load.

V. Analysis of the Line-Current Waveform

For the conventional single-stage designs with boost-type ICS cells, the average charging current of the boost inductor $i_{Lb,\rm ch(ave)}$ has linear relation to the instantaneous line voltage, while the average discharging current of the boost inductor $i_{Lb,\rm dis(ave)}$ primarily has a quadratic characteristic against the instantaneous line voltage. Thus, the resultant input i–ν characteristic curve is nonlinear, and the corresponding line current has a deformed shape [2]. To investigate the line-current waveform drawn by the proposed converter, the input i–ν characteristic curves are examined. As shown in Fig. 2, since the low-pass filter L_f–C_f will filter out the switching-frequency fundamental and harmonic components of i_{Lb}, the rectified line current $|i_{\rm ac}(t)|$ mathematically approximates to the average value of $i_{Lb}(t)$ within a switching period, namely, $|i_{\rm ac}| = i_{Lb,\rm ch(ave)} + i_{Lb,\rm dis(ave)}$. By using (6), (7), (13), (15), and (16), the expressions of $i_{Lb,\rm ch(ave)}$ and $i_{Lb,\rm dis(ave)}$ can be given as (27) and (28), respectively, shown at the bottom of the next page.

With the computation of (27) and (28), $i_{Lb,\rm ch(ave)}$, $i_{Lb,\rm dis(ave)}$, and $|i_{\rm ac}|$ in a half line cycle can be obtained, as shown in Fig. 9. These curves are sketched by using the parameters obtained in Section III for $V_{\rm ac} = 110$ $\rm V_{rms}$ and $V_b = 1.15 \cdot V_{\rm ac(pk)}$. As shown in Fig. 9(a), the i–ν curve of $i_{Lb,\rm ch(ave)}$ can be designed to bend convexly, while that of $i_{Lb,\rm dis(ave)}$ still bends concavely. Since these two bent curves compensate each other, the $|i_{\rm ac}| - |\nu_{\rm ac}|$ curve becomes nearly linear. The special charging mechanism of the proposed ICS scheme is explained

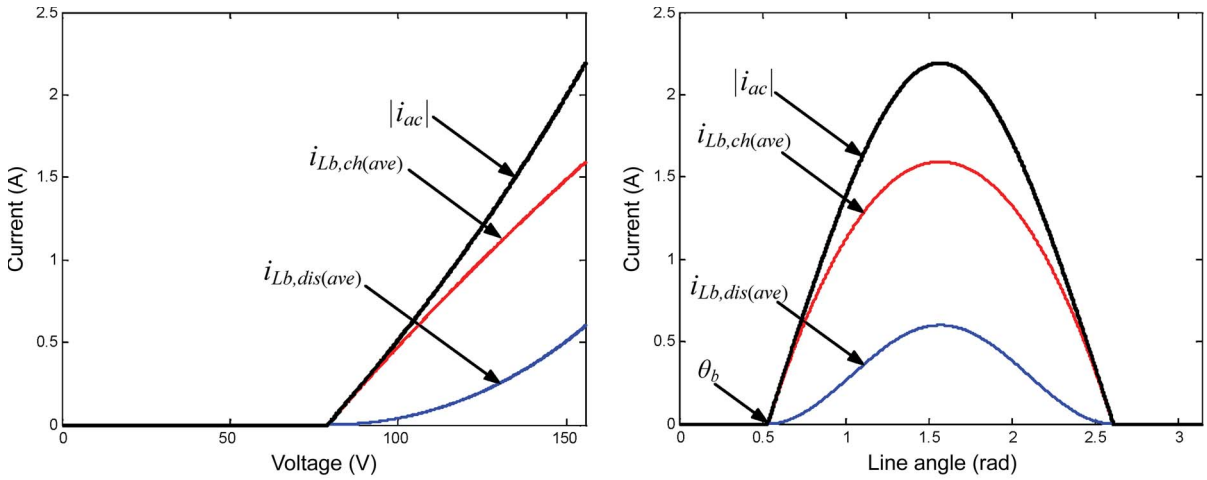

Fig. 9. Comparison of $i_{Lb,\mathrm{ch(ave)}}$, $i_{Lb,\mathrm{dis(ave)}}$, and $|i_{\mathrm{ac}}|$ drawn by the proposed converter in a half line cycle at 110 $\mathrm{V_{rms}}$. (a) Currents as a function of instantaneous line voltage. (b) Current waveforms as a function of line angle.

as follows. When $|\nu_{\mathrm{ac}}(t)|$ increases, the discharging voltage across L_b decreases, and thus, D_{s8} increases correspondingly. Since the charging voltage for energy-storage inductor, i.e., L_m or L_o, in the $D_{s8}T_s$ duration is smaller than that in the $(D - D_{s8})T_s$ duration, as shown in Fig. 5(b), lower output voltage will be formed. Under the constant output-voltage control, the duty ratio D will increase. Therefore, the increase of $|\nu_{\mathrm{ac}}(t)|$ will result in the decrease of $(1 - D)T_s$. Furthermore, the ac modulation effect on $(1 - D)$ makes $i_{Lb,\mathrm{ch(ave)}}(t)$ convexly vary with $|\nu_{\mathrm{ac}}(t)|$. The compensation produces a result in which the second derivative $\partial i_{\mathrm{ac}}^2/\partial^2 \nu_{\mathrm{ac}}$ is small and ranges between -1.1×10^{-4} and 2.2×10^{-4}. This result shows that the relationship between $|i_{\mathrm{ac}}|$ and $|\nu_{\mathrm{ac}}|$ is nearly linear and can be expressed as

$$|i_{\mathrm{ac}}| = \frac{(|\nu_{\mathrm{ac}}| - V_b + V_o \cdot n_1/n_4)}{R_{\mathrm{eq}}} + \text{negligible nonlinear terms} \quad (29)$$

where R_{eq} is the equivalent input resistance. The linear result can be seen clearly from Fig. 9.

VI. Experimental Results

To verify the feasibility and performance of the proposed topology, experimental tests were performed under the specifications described in Section III. The circuit components used for the experiment are listed in Table I.

TABLE I
Component Values for the Prototype Circuit

Component	Device Description
S_1, S_2	SPA11N60C3
D_1	U08A100
D_2, D_3, D_4	U08A20C
L_b	105 μH
L_r	15 μH
L_m	329 μH
L_o	20 μH
n_1: n_2: n_3: n_4	35: 24: 9: 7
C_b	300 μF/450 V
C_r	780 pF
C_c	0.6 μF/400 V
C_o	2000 μF/50 V
PWM controller	UC3843
High-side switch driver	IR2110

Fig. 10 shows the measured waveforms of ν_{GS1}, i_{S1}, and ν_{Cr} from the prototype circuit operating at 110 $\mathrm{V_{rms}}$. Experiments have verified the soft-switching characteristic as well as the excellent active-clamp function resulting in spike suppression on S_1 while the switch turns off. Fig. 11 shows the measured line-voltage and line-current waveforms at $V_{\mathrm{ac}} = 110$ and 230 $\mathrm{V_{rms}}$. It can be seen that the current waveform has a near-sinusoidal shape in mode M_2. Fig. 12 shows that the detailed current harmonics measured from the experimental prototype operating in both nominal high and low line inputs can satisfy the requirements of IEC 61000-3-2 Class D. Fig. 13

$$i_{Lb,\mathrm{ch(ave)}}(t) = \frac{(1 - D_{M2}(t))^2 T_s}{2L_b} \cdot \left(|\nu_{\mathrm{ac}}(t)| + \frac{n_1}{n_4} V_o - V_b\right) \quad (27)$$

$$i_{Lb,\mathrm{dis(ave)}}(t) = \frac{(1 - D_{M2}(t))^2 T_s}{2L_b} \cdot \frac{\left(|\nu_{\mathrm{ac}}(t)| + \frac{n_1}{n_4} V_o - V_b\right)^2 \cdot \left[\frac{L_r + L_m}{L_r L_m} + \left(\frac{n_1}{n_2}\right)^2 \cdot \frac{1}{L_b} + \left(\frac{n_3}{n_2}\right)^2 \cdot \frac{1}{L_o}\right]}{\frac{n_1 V_b}{n_2 L_r} + \frac{n_1 n_3 V_o}{n_2^2 L_o} + \left[\frac{L_r + L_m}{L_r L_m} + \left(\frac{n_3}{n_2}\right)^2 \cdot \frac{1}{L_o}\right] \cdot (V_b - |\nu_{\mathrm{ac}}(t)|)} \quad (28)$$

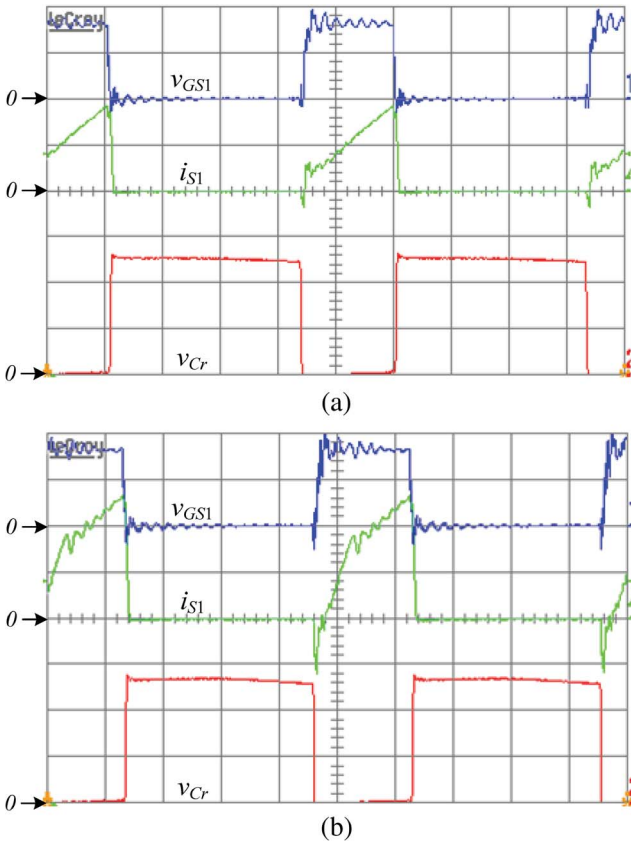

Fig. 10. Measured waveforms of ν_{GS1} (10 V/div), i_{S1} (2 A/div), and ν_{Cr} (100 V/div) at (a) mode M_1 and (b) mode M_2 (time scale: 2 μs/div).

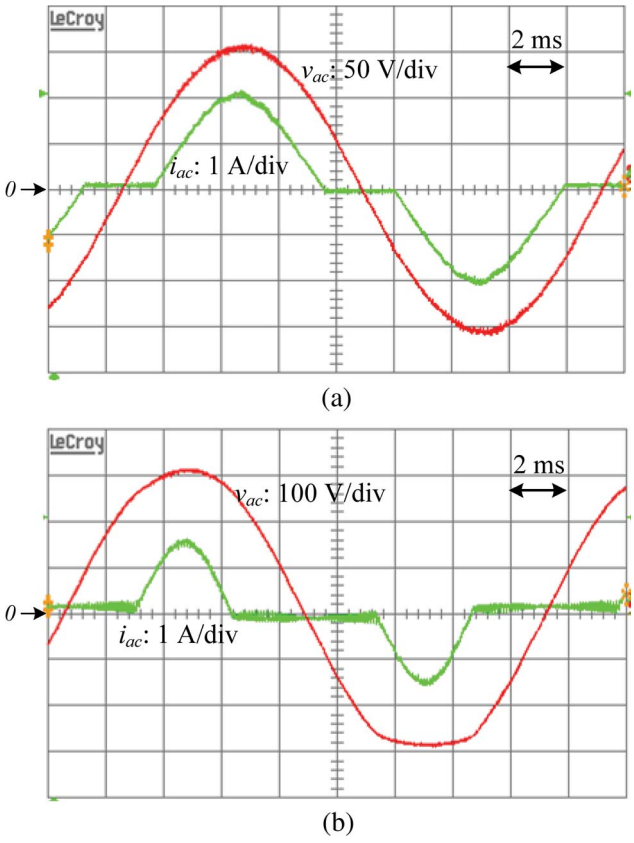

Fig. 11. Measured line-voltage and line-current waveforms at (a) $V_{\rm ac}$ = 110 $V_{\rm rms}$ and (b) $V_{\rm ac}$ = 230 $V_{\rm rms}$ with 20-V/100-W output.

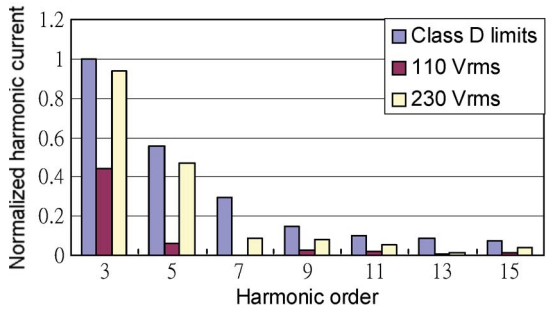

Fig. 12. Measured line-current harmonics comparison at full load.

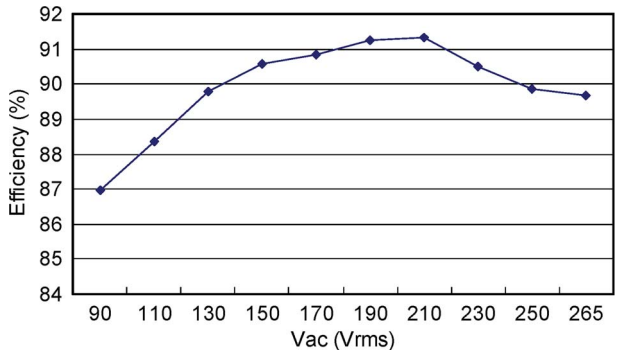

Fig. 13. Conversion efficiency versus input voltage.

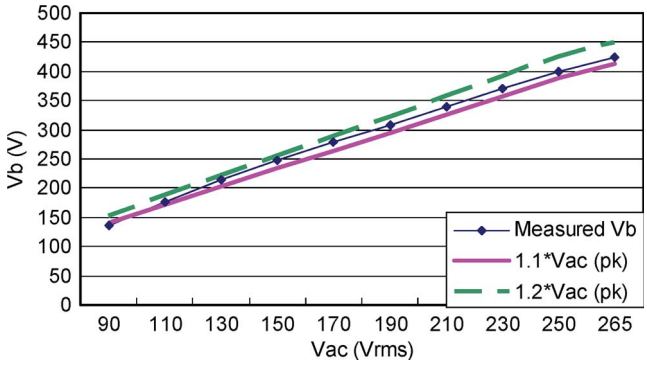

Fig. 14. Bulk-capacitor voltage versus input voltage.

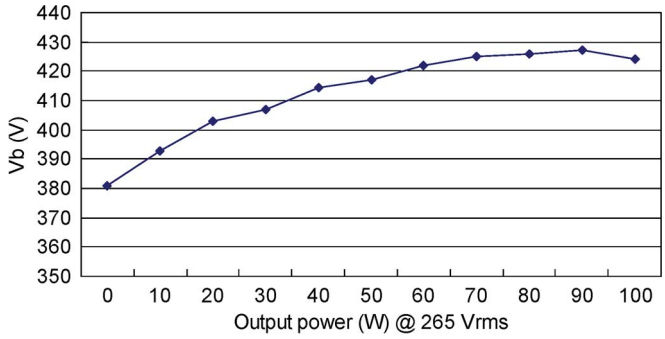

Fig. 15. Bulk-capacitor voltage versus output power at 265-$V_{\rm rms}$ line input.

shows that the conversion efficiency at full load is 87%–91.3%. Fig. 14 shows that the bulk-capacitor voltages are maintained within a desirable range (1.1–1.2 times as high as the peak line voltage) for the universal line-voltage range (90–265 $V_{\rm rms}$). Fig. 15 shows the bulk-capacitor voltages with load variation at

265-$V_{\rm rms}$ line input. The measured data indicate that the maximum bulk-capacitor voltage is 427 V, so the commercially available 450-V-rated capacitors can be used safely.

VII. Conclusion

In this paper, a novel single-stage ICS ac–dc converter for universal line applications has been proposed based on an active-clamp flyback–forward topology. Different from the conventional ICS schemes, the boost inductor in the ICS cell is charged in the duty-off time. By employing the proposed technique, two key advantages are obtained. First, during the duty-on time, the current stress across the main switch is alleviated. Second, the effective duty ratio of the ICS cell, $(1-D)$, is modulated by the instantaneous line voltage. This modulation produces a result, a better linear relationship between the line current and voltage through the conduction interval. Moreover, by the intentional arrangement of deactivating the flyback subconverter of the dc–dc cell at light load, the voltage stress across C_b can be alleviated effectively.

Experimental results show that the maximum bulk-capacitor voltage is 427 V in a wide range of output load at 265-$V_{\rm rms}$ line input. Owing to the ability to keep V_b below a desirable value ($V_b < 450$ V) under wide line and load variations, the proposed converter is suitable for the universal line-voltage applications. Experimental results have also demonstrated the proposed line-current correction function by a well-shaped current waveform which meets the IEC 61000-3-2 Class D requirements satisfactorily. Furthermore, the high conversion efficiency has verified the effectiveness of the switch current stress alleviation and soft-switching function.

Appendix

Equation (2): According to Fig. 4(a), the circuit equations are given by

$$n_2 i_{N2}(t) = n_3 i_{Lo}(t) \tag{30}$$

$$i_{Lr}(t) = i_{Lm}(t) + i_{N2}(t) \tag{31}$$

$$V_b - v_{N2,t0} = L_r \frac{di_{Lr}(t)}{dt} \tag{32}$$

$$\nu_{N2,t0} = L_m \frac{di_{Lm}(t)}{dt} \tag{33}$$

$$\frac{n_3}{n_2}\nu_{N2,t0} - V_o = L_o \frac{di_{Lo}(t)}{dt}. \tag{34}$$

Substituting (30) into (31) to replace i_{N2} and then differentiating (31) with respect to t, one can obtain

$$\frac{di_{Lr}(t)}{dt} = \frac{di_{Lm}(t)}{dt} + \frac{n_3}{n_2}\cdot\frac{di_{Lo}(t)}{dt}. \tag{35}$$

Substituting (32)–(34) into (35) yields

$$\frac{V_b - \nu_{N2,t0}}{L_r} = \frac{\nu_{N2,t0}}{L_m} + \frac{n_3}{n_2}\cdot\frac{\frac{n_3}{n_2}\nu_{N2,t0} - V_o}{L_o}. \tag{36}$$

Rearranging (36), $v_{N2,t0}$ can be obtained, as shown in (2).

Equation (8): According to Fig. 4(k), the circuit equations are given by

$$i_{Lr}(t) = i_{Lm}(t) + i_{N2}(t) \tag{37}$$

$$n_1 i_{Lb}(t) + n_2 i_{N2}(t) = n_3 i_{Lo}(t) \tag{38}$$

$$|v_{\rm ac}(t)| - v_{N1,t7}(t) - V_b = L_b \frac{di_{Lb}(t)}{dt} \tag{39}$$

$$V_b - \nu_{N2,t7}(t) = L_r \frac{di_{Lr}(t)}{dt} \tag{40}$$

$$\nu_{N2,t7}(t) = L_m \frac{di_{Lm}(t)}{dt} \tag{41}$$

$$\frac{n_3}{n_2}\nu_{N2,t7}(t) - V_o = L_o \frac{di_{Lo}(t)}{dt}. \tag{42}$$

Substituting (37) into (38) to replace i_{N2} and then differentiating (38) with respect to t, one can obtain

$$n_1 \frac{di_{Lb}(t)}{dt} + n_2\left(\frac{di_{Lr}(t)}{dt} - \frac{di_{Lm}(t)}{dt}\right) = n_3 \frac{di_{Lo}(t)}{dt}. \tag{43}$$

Substituting (39)–(42) into (43) yields

$$n_1 \cdot \frac{|v_{\rm ac}(t)| - \nu_{N1,t7}(t) - V_b}{L_b} + n_2 \cdot \left(\frac{V_b - \nu_{N2,t7}(t)}{L_r} - \frac{\nu_{N2,t7}(t)}{L_m}\right) = n_3 \cdot \frac{\frac{n_3}{n_2}\nu_{N2,t7}(t) - V_o}{L_o}. \tag{44}$$

Replacing $\nu_{N2,t7}(t)$ with $(n_2/n_1)\cdot\nu_{N1t7}(t)$ and rearranging (44), $\nu_{N1,t7}$ can be obtained, as shown in (8).

Equation (24): From Ampere's law and Fig. 4(f), one can obtain

$$-i_{N2} = \frac{n_1}{n_2} i_{Lb} + \frac{n_4}{n_2} i_{D4} = i_{Lm} - i_{Lr}. \tag{45}$$

Rearranging (45), i_{D4} can be found as follows:

$$i_{D4} = \frac{n_2}{n_4}\left(i_{Lm} - i_{Lr} - \frac{n_1}{n_2} i_{Lb}\right). \tag{46}$$

By integrating (46) through the duty-off time and then multiplying (46) by V_o/T_s, one can obtain the output power provided by the flyback subconverter. In the proposed converter, the output power provided by the flyback subconverter at 265 $V_{\rm rms}$ and full-load situation is designed to be lower than $P_o/2$. Therefore

$$\frac{V_o}{T_s}\int_0^{(1-D)T_s} \frac{n_2}{n_4}\cdot\left(i_{Lm}(t) - i_{Lr}(t) - \frac{n_1}{n_2} i_{Lb}(t)\right) dt < \frac{P_o}{2\eta}. \tag{47}$$

Substituting the time functions of i_{Lm}, i_{Lr}, and i_{Lb} into (47) yields

$$\frac{V_o}{T_s}\frac{n_2}{n_4}\int_0^{(1-D)T_s} \left[\left(i_{Lm}(t_4) - \frac{V_o}{L_m}\frac{n_2}{n_4}t\right) - \left(i_{Lm}(t_4) - \frac{-V_c + V_o\cdot n_2/n_4}{L_r}t\right) - \frac{n_1}{n_2}\cdot\frac{|v_{\rm ac}| + V_o\cdot n_1/n_4 - V_b}{L_b}t\right] dt < \frac{P_o}{2\eta} \tag{48}$$

where $V_c = DV_b/(1-D)$. Equation (48) can be solved for L_m to yield (24).

Equation (25): In the proposed converter, the output power provided by the forward subconverter at 265 $V_{\rm rms}$ is arranged to be greater than $P_o/2$. Therefore, one can obtain

$$\frac{L_o I_{Lo(\rm pk)}^2}{2} > \frac{P_o T_s}{2\eta} \tag{49}$$

where

$$I_{Lo(\rm pk)} \approx \left(V_{b,\max} \frac{L_m}{L_m + L_r} \cdot \frac{n_3}{n_2} - V_o \right) \cdot \frac{D_{\min} T_s}{L_o}. \tag{50}$$

The aforementioned approximation is considered under the assumption of $L_m \gg L_r$. Substituting (50) into (49) yields

$$L_o < \frac{D_{\min}^2 T_s \eta}{P_o} \cdot \left(V_{b,\max} \frac{L_m}{L_m + L_r} \cdot \frac{n_3}{n_2} - V_o \right)^2. \tag{51}$$

Moreover, to ensure that L_o always operates in DCM, the following relationship should be guaranteed:

$$\left(\frac{n_3}{n_2} \nu_{N2,t0}(t) - V_o \right) \cdot DT_s < V_o \cdot (1 - D) T_s. \tag{52}$$

Substituting (2) into (52) yields

$$\frac{\frac{V_b}{L_r} + \frac{n_3}{n_2}\frac{V_o}{L_o}}{\frac{1}{L_r} + \frac{1}{L_m} + \left(\frac{n_3}{n_2}\right)^2 \frac{1}{L_o}} < \frac{n_2}{n_3}\frac{V_o}{D}. \tag{53}$$

Rearranging (53) yields

$$L_o < \frac{\frac{n_3}{n_2} V_o \cdot \left(\frac{1 - D_{\max}}{D_{\max}} \right)}{\frac{V_{b,\min}}{L_r} - \frac{n_2 V_o}{n_3 D_{\max}} \cdot \left(\frac{1}{L_m} + \frac{1}{L_r} \right)}. \tag{54}$$

The value of L_o must satisfy both the conditions of (51) and (54); therefore, (25) can be obtained.

Equation (26): The value of inductor L_b should be selected so that the condition of $D_{s8} < D$ can be satisfied in the whole half line cycle. From (13), one can obtain

$$\frac{|\nu_{\rm ac}(t)| + \frac{n_1}{n_4} V_o - V_b}{\frac{n_1}{n_2} \nu_{N2,t7}(t) + V_b - |\nu_{\rm ac}(t)|} \cdot (1 - D) < D. \tag{55}$$

In (55), since the denominator of the left term is always greater than zero, (55) can be rearranged as

$$\left(|\nu_{\rm ac}(t)| + \frac{n_1}{n_4} V_o - V_b \right) \cdot (1 - D) < \left(\frac{n_1}{n_2} \nu_{N2,t7}(t) + V_b - |\nu_{\rm ac}(t)| \right) D. \tag{56}$$

Substituting (8) into (56) and rearranging (56) yield

$$\left(\frac{|\nu_{\rm ac}(t)| - V_b}{D} + \frac{n_1}{n_4} V_o \frac{1 - D}{D} \right) \frac{n_2}{n_1} < \frac{\frac{n_1 (|\nu_{\rm ac}(t)| - V_b)}{n_2 L_b} + \frac{V_b}{L_r} + \frac{n_3 V_o}{n_2 L_o}}{\frac{L_r + L_m}{L_r L_m} + \left(\frac{n_1}{n_2}\right)^2 \frac{1}{L_b} + \left(\frac{n_3}{n_2}\right)^2 \frac{1}{L_o}}. \tag{57}$$

Since the critical boundary condition of CCM and DCM occurs at the lowest peak input voltage, according to (57), one can obtain the maximum boost inductance $L_{b,max}$, i.e., (26), by applying $V_{\rm ac(pk),min}$, $V_{b,\min}$, and $D_{\max}$.

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