奈米尺寸之製程應變矽互補式金氧半場效電晶體之

載子傳輸與負偏壓溫度不穩定之研究

研究生：林宏年　　指導教授：林鴻志 博士
黃調元 博士

國立交通大學電子工程系電子研究所

摘要

本論文中，我們主要探討製程引致單軸應力對互補式金氧半場效電晶體(CMOS)之載子傳輸(carrier transport)與負偏壓溫度不穩定(NBTI)的影響。載子傳輸方面，我們先以通道背向散射(channel backscattering)觀點來檢驗通道應力對高橫向電場下載子傳輸的影響。藉由背向散射參數與溫度的指數關係，我們可得一簡單的數學表示式以萃取通道背向散射係數(channel backscattering ratio)與相關參數，討論這些參數的變化對汲極電流的作用，並且分析何種機制造成應力引致背向散射參數的變化。我們亦探討通道應力對低橫向電場載子傳輸的作用。接著，我們提出一模型以關連低電場的載子傳輸與高電場下通道背向散射行為。依據此模型，我們首先提出一萃取源汲極寄生電阻的方法，可適用於奈米尺寸的製程應變矽 CMOS，而無需處理通道遷移率與通道長度無關等等備受爭議的假設，以不同製程技術的 CMOS 來檢驗此模型並萃取其源汲極寄生電阻。最後，我們探討通道應力對負偏壓溫度不穩定(NBTI)的作用。

第二至第五章為載子傳輸的部分。第二章首先介紹通道背向散射理論及其電流電壓模型，接著比較幾種萃取通道背向散射率的方式。於本論文裡，我們利用背向散射參數與溫度的指數特性，推導出萃取背向散射率的數學式子，且考慮載子退化與寄生電阻對背向散射率的影響。第三章，使用製程應變矽(PSS) CMOS，從通道背向散射觀點來評估通道應力對高電場載子傳輸的影響。我們發現通道應力會改變 CMOS 其背向散射率，且隨著通道應力增加，背向散射率變化的幅度愈大，其中背向散射率的增加與降低與應

力極性相關：具伸張應力的 nMOSFETs 會降低背向散射率；然而具壓縮應力的 pMOSFETs 會惡化背向散射率。這些變化對電流的作用，與造成此現象的機制亦涵蓋於第三章內。

第四章裡，我們提出一模型，此模型以源汲極寄生電阻、通道電阻、彈道傳輸率與寄生電阻的變化量等四個參數將製程引致的低電場通道遷移率增益、線性區與飽和區汲極電流增益關聯起來。此模型揭露出線性區、飽和區的汲極電流增益可表示為遷移率增益的線性函數，其截距大小與寄生電阻的變化量、源汲極電阻對通道電阻的比率有關。其中源汲極電阻對通道電阻的比率、彈道傳輸率分別決定著製程引致的遷移率增益對線性區、飽和區汲極電流增益的轉換效率。依據此模型，我們也發展出一適用於奈米尺寸製程應變矽 CMOS 其計算源汲極寄生電阻的方法。第五章裡，以不同製程技術的奈米通道尺寸應變矽 CMOS 來探討汲極電流增益、遷移率增益的關係，並且萃取其寄生電阻，分析比較不同製程技術對其影響。我們觀察到對任一製程技術而言，源汲極寄生電阻會逐漸地削減應變通道其提升電流的益處。我們也發現應變矽 nMOSFETs 與 pMOSFETs 其汲極電流增益與遷移率增益有一不同的比例關係。對 nMOSFETs，其線性區與飽和區汲極電流增益大小相似，且電流的增益約只為通道遷移率增益的一半。然而對 pMOSFETs，其線性區汲極電流增益比飽和區的來的大，與通道遷移率增益大小相似。造成此現象的機制亦探討之。

第六章則為通道應力對負偏壓溫度不穩定的作用探討。以三維應變工程來看，從通道寬度方向降低通道的壓縮應力，不僅有益於電流提升且改善元件其 NBTI 可靠度。此章節亦探討動態(dynamic)NBTI 中退化回復的機制，與通道應力引致較大的 NBTI 退化之原因。最後於第七章裡，我們做一簡單摘要，並對此論文的延續工作與未來方向做一建議。

關鍵字: 載子傳輸、通道背向散射、互補式金氧半場效電晶體、負偏壓溫度不穩定性、電阻萃取、單軸應變矽。

Study of Carrier Transport and Negative Bias Temperature Instability (NBTI) of Nanoscale Process-Strained Si (PSS) CMOSFETs

Student: Hong-Nien Lin

Advisors: Dr. Horng-Chih Lin
Dr. Tiao-Yuan Huang

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

Abstract

In this dissertation, we primarily investigate the impact of process-induced uniaxial strain of CMOSFETs on low-field carrier transport and high-field channel backscattering phenomenon. By utilizing the temperature power-dependence of drain current, we can deduce an analytic expression for extracting the channel backscattering ratio and related factors, and then analyze and discuss the mechanism responsible for strain-induced backscattering factor modulation. Here, we also propose a model for correlating the low-field carrier transport and high-field channel backscattering. According to this model, we develop a new methodology to extract the total source/drain (S/D) parasitic resistance for nanoscale strained MOSFETs. Then, we employ strained CMOSFETs by different technology nodes to examine our model and demonstrate the new extraction method. Finally, we study the effect of channel stress on negative bias temperature instability (NBTI) of pMOSFETs.

The channel backscattering theory, the current-voltage modeling, and the deduction of the analytic expression for evaluating the channel backscattering ratio are shown in Chapter 2. Then, we used process-strained Si (PSS) CMOSFETs to estimate its effect on carrier transport in terms of the backscattering factor modulation in Chapter 3. It is found that the channel stress results in the modulation of channel backscattering ratio, which becomes more evident with increasing channel stress. Moreover, the backscattering ratio modulation is dependent on stress polarity, i.e., tensile PSS nMOSFETs have decreased backscattering ratio

whereas compressive PSS pMOSFETs exhibit increased backscattering ratio. The mechanism accounting for this observation is also discussed.

In Chapter 4, we proposed a model for correlating the strain-induced low-field channel mobility gain, linear drain current gain, and saturation drain current gain in terms of the S/D resistance, the channel resistance, the ballistic efficiency, and the reduction of S/D resistance. It is demonstrated for the first time that the linear and saturation drain current gains can be modeled as linear functions of channel mobility gain with the intercept of S/D resistance reduction, where the S/D-to-channel resistance ratio and the ballistic efficiency determine the translating efficiency of channel mobility gain to the linear and saturation drain current gains, respectively. Based on this model, we also developed a new methodology for extracting the total S/D parasitic resistance of nanoscale strained MOSFETs.

In Chapter 5, we employed state-of-the-art strained CMOSFETs by different technology nodes to examine the correlation between the channel mobility gain and drain current gain. We found that the S/D parasitic resistance gradually diminishes the benefit of strain-enhanced drain current gain regardless of adopting technology nodes. In addition, for PSS nMOSFETs, the linear and saturation drain current gains are comparable, where both current gains are around half of channel mobility gain. However, for PSS pMOSFETs, the linear drain current gain is comparable to the channel mobility gain and larger than the saturation one. The reasons accounting for this phenomenon are discussed as well.

In Chapter 6, we studied the NBTI of PSS pMOSFETs with different channel stress levels. It is noted that decreasing the channel compressive stress along the channel width direction not only improves the drain current but also the device reliability of NBTI. Moreover, mechanisms for degradation recovery during dynamic NBTI stress and aggravated NBTI degradation for pMOSFETs with larger channel stress are also discussed.

Finally, in Chapter 7, we summarize key findings and suggest the future works of this study.

Keywords: Carrier transport, channel backscattering, CMOSFET, NBTI, resistance extraction, uniaxial strained Si.

Acknowledgment

首先要感謝黃調元老師、林鴻志老師，於碩、博士生涯期間予我課業與研究上的指導與鼓勵。謝謝他們予我這個機會能於台積電半工半讀，除了減輕經濟上的負擔，亦予我很大的自由發展與研究空間。我想致力於研究發展是回報他們恩惠的最好方式。亦感謝林鴻志老師於待人處事上的諄諄教誨。

接著衷心地感謝生命中的貴人：台積電前瞻科技發展一部李文欽經理與陳宏瑋博士。他們於研究期間對我的支持、鼓勵、論文內容上的建議與深度探討，使我獲益良多也倍感窩心。此外，於參與 VLSI、IEDM 會議時經濟上的協助，帶領我見識許多業界、學界上知名的人事；於家裡發生事故的同時，對我的關懷與協助；在我艱困、無奈的時刻裡彌足珍貴，從此體驗到人生寶貴的一課，對我而言是良師兼益友，所施予的恩惠，此生莫敢忘懷。另外，謝謝柯誌欣博士、葛崇祐先生於本論文研究上的協助；謝謝王靜亞博士於研究期間的關懷。

謝謝先進元件實驗室的王夢凡、俞正明、李達元、盧文泰與葉冠麟博士們於博士研究初期時的研究教導與討論；亦謝謝陳國華先生、顏承正先生於生活上的照顧；謝謝同期的呂嘉裕博士、李明賢先生，我們所一起走過的歲月；謝謝學弟景森、俊榮與行徽，於許多事務上的協助。謝謝才華洋溢的碩廷，於音樂、吉他方面的教學；謝謝體健身強的柏儀，教我如何衝浪、浮潛，和你一起到野外探險的日子仍記憶猶新。謝謝偉豪於研究上、生活上的點滴分享。

謝謝國家奈米元件實驗室 Ms. Iris Lin 對我的關懷與問候；謝謝劉政財先生教導我做人明辨是非的道理；謝謝沈世文先生於我博士研究初期上的幫忙。

感謝外文系的黃秀英奶奶，於博士生涯期間破例讓我修習系上的日文課。昨天去找您時，您依舊如昔，嘹喨的聲音、活潑的表情與充滿活力的肢體語言，深深地烙印於腦海中。當你回想起我時，霎那間的微笑，我想對我而言是最好的畢業禮物。祝奶奶您依舊活潑、健康、充滿活力。

感謝新竹家扶中心大哥姊課輔隊的夥伴們，讓我參與一些想做的事情。感謝黃小妹，讓我得有機會給妳課後輔導，得知妳考上不錯的學校，著實地替妳感到開心。

感謝護理之家淑靜姐於博士研究初期對我的關懷與支持。感謝山東田清月香女士、畢業於上海女子師範大學的奶奶(您的哀歌還不錯聽喔!)、還有多次奪得上海國際標準舞錦標賽冠軍的爺爺，謝謝您們讓我有機會陪伴您們，得以增添人生的色彩與回憶。期望您們依舊健康有朝氣、長命百歲。

感謝我的知心好友小蔡與小賴，陪我一起撐過那段煎熬的歲月。

感謝生命中的那個人，很開心認識妳，不經意的溫柔流露與貼心舉動，對我是莫大的鼓勵與支持，謝謝妳。

最後，感謝養育、教育我的父母，從我呱呱墜地的開始，您們給了我一切，現在是我回報的開始。

CONTENTS

TABLE CAPTIONS

Chapter 3

Chapter 4

Chapter 5

FIGURE CAPTIONS

Chapter 2

Chapter 3

Chapter 4

Chapter 6

LIST OF SYMBOLS

B_0	Nondegenerate ballistic efficiency
B	Degenerate ballistic efficiency
B_{sat0}	Nondegenerate saturation ballistic efficiency
B_{sat}	Degenerate saturation ballistic efficiency
$B_{sat0,Ctrl}$	Nondegenerate saturation ballistic efficiency of the control MOSFET
$B_{sat0,PSS}$	Nondegenerate saturation ballistic efficiency of process-strained Si (PSS) MOSFETs
C	Capacitance
C_{eff}	Effective gate capacitance
E_1	First subband energy level
E_F	Fermi level
f	Stress frequency of dynamic negative bias temperature instability (DNBTI)
G_D	Output conductance
G_{mi}	Intrinsic transconductance
G_m	Transconductance
$G_{m,max}$	Maximum transconductance
I_{CP}	Charge pumping current
I_d	Drain current
I_{dlin}	Linear drain current
I_{dsat}	Saturation drain current
$I_{dlin,Ctrl}$	Linear drain current of the control MOSFET
$I_{dlin,PSS}$	Linear drain current of process-strained Si (PSS) MOSFETs
$I_{dsat,Ctrl}$	Saturation drain current of the control MOSFET
$I_{dsat,PSS}$	Saturation drain current of process-strained Si (PSS) MOSFETs

I_{off}	Off-current
I_{on}	On-current
J_G	Gate leakage-current density
k	A factor of determining the translating efficiency of ΔR_{SD} to ΔI_{dlin}
k_B	Boltzmann constant
L	Gate length
L_{Mask}	Mask gate length
$L_{physical}$	Physical gate length
l_0	Nondegenerate k_BT layer thickness
l	Degenerate k_BT layer thickness
$l_{0,Ctrl}$	Nondegenerate k_BT layer thickness of the control MOSFET
$l_{0,PSS}$	Nondegenerate k_BT layer thickness of process-strained Si (PSS) MOSFETs
m^*	Carrier effective mass
N_{it}	Interface trap density
n_{S1}	Carrier density in the first subband energy level
n_S	Inversion carrier density
Q_{inv}	Inversion charge density
q	Electronic charge
R_{CH}	Channel resistance
$R_{CH,Ctrl}$	Channel resistance of the control MOSFET
$R_{CH,PSS}$	Channel resistance of process-strained Si (PSS) MOSFETs
R_D	Total drain-side parasitic resistance
$R_{D,Ctrl}$	Total drain-side parasitic resistance of the control MOSFET
$R_{D,PSS}$	Total drain-side parasitic resistance of process-strained Si (PSS) MOSFETs
R_S	Total source-side parasitic resistance
$R_{S,Ctrl}$	Total source-side parasitic resistance of the control MOSFET

$R_{S,PSS}$	Total source-side parasitic resistance of process-strained Si (PSS) MOSFETs
R_{SD}	Total source/drain (S/D) parasitic resistance
$R_{SD,Ctrl}$	Total source/drain (S/D) parasitic resistance of the control MOSFET
$R_{SD,PSS}$	Total source/drain (S/D) parasitic resistance of process-strained Si (PSS) MOSFETs
R_{TOTAL}	Total resistance
$R_{TOTAL,Ctrl}$	Total resistance of the control MOSFET
$R_{TOTAL,PSS}$	Total resistance of process-strained Si (PSS) MOSFETs
r_0	Nondegenerate channel backscattering ratio
r	Degenerate channel backscattering ratio
r_{sat0}	Nondegenerate saturation channel backscattering ratio
r_{sat}	Degenerate saturation channel backscattering ratio
$r_{sat0,PSS}$	Nondegenerate saturation channel backscattering ratio of process-strained Si (PSS) MOSFETs
S	Subthreshold Swing
T	Temperature
t	Stress time
U_D	Reduced drain voltage
V_{BD}	Gate dielectric breakdown voltage
V_D	Drain voltage
V_G	Gate voltage
V_T	Threshold voltage
$V_{T,pre}$	Pre-stressed threshold voltage
$V_{T,lin}$	Linear threshold voltage
$V_{T,sat}$	Saturation threshold voltage
W	Gate width

α	Temperature coefficient of I_{dsat}
β	A numerical factor accounting carrier degeneracy effect for l_0
$\varepsilon(0)$	Electric field at the top of source-to-channel barrier
η_F	Reduced Fermi energy
η	Temperature coefficient of $V_{T,sat}$
λ_0	Nondegenerate mean-free-path (MFP) for channel backscattering
λ	Degenerate mean-free-path (MFP) for channel backscattering
$\lambda_{0,Ctrl}$	Nondegenerate MFP for channel backscattering for the control MOSFET
$\lambda_{0,PSS}$	Nondegenerate MFP for channel backscattering for process-strained Si (PSS) MOSFETs
μ	Low lateral-field channel mobility
μ_{Ctrl}	Low lateral-field channel mobility of the control MOSFET
μ_{PSS}	Low lateral-field channel mobility of process-strained Si (PSS) MOSFETs
τ	Device lifetime
υ_{inj0}	Nondegenerate carrier injection velocity
υ_{inj}	Degenerate carrier injection velocity
$\upsilon_{inj0,Ctrl}$	Nondegenerate carrier injection velocity of the control MOSFET
$\upsilon_{inj0,PSS}$	Nondegenerate carrier injection velocity of process-strained Si (PSS) MOSFETs
υ_{th}	Thermal velocity
$\hbar$	Reduced Planck constant
ΔB_{sat0}	Change in nondegenerate saturation ballistic efficiency
Δf	Change in stress frequency of dynamic negative bias temperature instability (DNBTI)
ΔI_{CP}	Change in charge pumping current
ΔI_{dlin}	Change in linear drain current

ΔI_{dsat}	Change in saturation drain current
ΔN_{it}	Change in interface trap density
ΔR_D	Change in total drain-side parasitic resistance
ΔR_S	Change in total source-side parasitic resistance
ΔR_{SD}	Change in total source/drain (S/D) parasitic resistance
ΔS	Change in subthreshold swing
ΔT	Change in temperature
ΔV_{DIBL}	V_G difference between linear and saturation region by constant current method
$\Delta V_{T,sat}$	Change in saturation threshold voltage
$\Delta V_{T,BT}$	Negative bias temperature instability (NBTI)-induced threshold voltage shift
$\Delta \upsilon_{inj0}$	Change in nondegenerate carrier injection velocity
$\Delta \mu$	Change in low lateral-field channel mobility
$\Im_n(\eta_F)$	Fermi-Dirac integral of order n as a function of η_F
$\Im_n(\eta_F - U_D)$	Fermi-Dirac integral of order n as a function of η_F and U_D