Chapter 1

Introduction

1.1 Background

With continuous shrinking of the process technology nodes of metal oxide semiconductor field-effect transistors (MOSFETs), the development of bulk MOSFET technology has faced a number of challenges, such as process complexities, lithography limits, and so on, in an effort to meet the drive current and device performance according to the international technology roadmap for semiconductors (ITRS) [1.1]. Therefore, a lot of alternative techniques were proposed to address the issues. For example, pursuing strained materials to replace Si channel can provide higher carrier mobility [1.2]. Adopting high-*k* dielectrics for MOSFETs facilitates the continuous shrinking of equivalent oxide thickness (EOT) and the reduction of gate leakage current [1.3]. In addition, to more effectively control the electrostatic field of nanoscale devices, new device architectures were investigated as well [1.4].

Among these approaches, presently strain engineering has been successfully integrated into complementary metal-oxide-semiconductor (CMOS) process for improving device performance and operation speed of integrated circuit (IC) [1.5]–[1.8]. Strain-enhanced channel mobility and drain current are considered as important performance indices for evaluating the feasibility of a strain technique. However, as the gate length scales into nanoscale regime, strain-induced enhancement becomes more complicated to predict as the carrier ballistic transport, and source/drain (S/D) parasitic resistance effects start to prevail for state-of-the-art CMOS [1.5][1.9][1.10]. On the other hand, the conventional current-voltage (*I*-*V*)

modeling approaches based on drift-diffusion carrier transport in the bulk Si is no longer adequate to predict the electrical characteristics of short-channel MOSFETs [1.11]. Recently, Lundstrom *et al*. [1.12]–[1.16] developed a simple and analytic compact expression based on one-flux approach [1.17][1.18] for modeling electrical characteristics of ultrasmall MOSFETs when channel lengths become comparable to carrier scattering mean-free-path (MFP).

To fully exploit the advantages of strained Si techniques down to sub-100-nm regime, it is essential to fully understand the carrier transport properties under both low and high lateral electric fields. Based on the scattering theory, Lundstrom *et al*. [1.19] proposed simple equations for correlating the fractional change of low-field channel mobility ($\Delta\mu$), the linear drain current gain (ΔI_{dlin}), and the saturation drain current gain (ΔI_{dsat}) as follows

$$\Delta I_{dlin} = (1 - B_{lin})\Delta\mu, \tag{1.1a}$$

$$\Delta I_{dsat} = (1 - B_{sat})\Delta\mu, \tag{1.1b}$$

where B_{lin} and B_{sat} are the linear and saturation ballistic efficiency, respectively. Lundstrom *et al*. found that ΔI_{dlin} is similar to $\Delta\mu$ due to the fact that B_{lin} is close to zero, and ΔI_{dsat} is roughly half of $\Delta\mu$ since B_{sat} is around 0.5 for current technology [1.20][1.21].

1.2 Motivation

Nevertheless, there are still some issues that need to be fully understood. Firstly, the influence of channel stress on the channel backscattering characteristics needs to be considered because stress may affect the carrier transport properties, but few works addressed this topic [1.10][1.22]–[1.25]. Secondly, as the channel length scales into

nanoscale regime, the correction of total source/drain (S/D) parasitic resistance should be included for mobility gain estimation. Unfortunately, the well-known resistance extraction methods, e.g., shift and ratio [1.26] and total resistance slope-based methods [1.27], may not be adequate for strained Si devices because of the assumption of channel-length-independent mobility. In addition, the contribution of S/D resistance reduction should be included in (1.1a) and (1.1b). Thirdly, if the ΔI_{dlin} and ΔI_{dsat} of strained MOSFETs is comparable with each other for current technology [1.6], there will be an unreasonable result, i.e., B_{lin} being close to B_{sat}, according to (1.1a) and (1.1b), because the ballistic efficiency strongly depends on lateral electric field [1.28]. That is, a more suitable expression determining the dependence of $\Delta\mu$ on ΔI_{dlin} should be used. Furthermore, to obtain optimized device performance without sacrificing its device reliability, it is worthy to examine the impact of channel stress on device reliability. Based on the above considerations, we organize our thesis as shown in the following section.

1.3 Organization of the Dissertation

The organization of this dissertation is stated as follows. In Chapter 2, we introduce the theory and current-voltage modeling of channel backscattering. By the temperature power dependence, we deduce related analytic expressions for estimating the channel backscattering ratio and related factors. Then, in Chapter 3, the influence of process-induced uniaxial strain on channel backscattering behaviour is evaluated in terms of these factors, and the mechanism accounting for the modulation of these factors is also discussed. In Chapter 4, we propose a model for correlating the low-field carrier transport and high-field channel backscattering of uniaxial strained CMOSFETs. Based on this model, we also demonstrate a new methodology to extract the source/drain parasitic resistance. In Chapter 5, the

state-of-the-art strained CMOSFETs with different technology nodes are used to examine the correlation between low-field and high-field carrier transport. In Chapter 6, the effect of channel stress on negative bias temperature instability (NBTI) is discussed. Finally, in Chapter 7, we conclude some key results and suggest some future works.