Chapter 3

Channel Backscattering Characteristics of Nanoscale Process-Strained Silicon (PSS) CMOSFETs

3.1 Introduction

Recently, uniaxial strain techniques are actively pursued to give the device performance a much-needed boost in 90-nm node and beyond [3.1]–[3.3]. Mobility enhancement induced by strain in the channel has been widely characterized, and it was found that only half of the mobility enhancement is all that are needed to account for the observed saturation drain current increase [3.4]. To reconcile this discrepancy and to understand carrier transport in nanoscale regime, channel backscattering theory has been widely investigated for accurately modeling the current voltage (*I*–*V*) characteristics, and estimating the gap of drain current between ballistic limit and current technology [3.5]–[3.10]. For these channel backscattering models, although the *I*–*V* expressions are not entirely identical between them, the saturation drain current are basically determined by two key parameters, i.e., channel backscattering ratio and carrier injection velocity [3.12]. The channel backscattering ratio generally refers to the fraction of the injected carriers that are scattered back to the source where the injected carriers with injection velocity enter into the channel. In other words, the transmitted carriers reaching the drain ultimately determine the drain current. Therefore, it is expected that a detailed understanding of channel backscattering behavior of nanoscale strained MOSFETs is vital for further boosting the device drain current. However, few channel backscattering *I*–*V* models [3.13][3.14] and experimental electrical characterization [3.15]–[3.19] have taken into consideration of the influence of strain on channel backscattering characteristics up to now.

In this chapter, based on the methodology of evaluating the channel backscattering ratio introduced in Chapter 2, we will demonstrate its extraction flow step by step, and then analyze the impact of uniaxial process-induced tensile and compressive strains on channel backscattering characteristics in terms of carrier mean-free-path (MFP) for channel backscattering (λ_0), k_BT layer thickness (l_0), channel backscattering ratio (r_{sat0}), ballistic efficiency (B_{sat0}), and carrier injection velocity (υ_{inj0}). Furthermore, the mechanism accounting for strain-induced backscattering parameter modulation and the correlation between saturation drain current, ballistic efficiency, and carrier injection velocity will be included as well. Finally, based on the analytic expression deduced in Chapter 2, we will compare the channel backscattering ratio with and without degenerate carrier statistics and source/drain (S/D) parasitic resistance (R_{SD}).

3.2 Channel Backscattering Characteristics of Process-Strained Si (PSS) CMOSFETs

In this section, we characterize the channel backscattering behavior of control and strained CMOSFETs in terms of the related backscattering factors. Firstly, we will demonstrate the extraction process of the temperature-dependent methodology for evaluating the ratio of carrier MFP for channel backscattering to k_BT layer thickness (λ_0 / l_0), channel backscattering ratio (r_{sat0}), ballistic efficiency (B_{sat0}), and carrier injection velocity (υ_{inj0}). Then, we study the influence of process-induced uniaxial strain on these factors. In addition, strain-enhanced drain current is also analyzed in terms of ballistic efficiency, and carrier injection velocity.

3.2.1 Experimental

Fig. 3.1 shows a schematic view of process-strained Si (PSS) MOSFET

employed in this work, where channel stress was induced from MOSFET process steps, such as shallow trench isolation (STI), silicidation, contact etch stop layer (CESL), embedded SiGe in S/D regions, and so on [3.3]. To explore the influence of process-induced uniaxial strain on channel backscattering characteristics, we employed the split conditions shown in Table 3.1. For PSS nMOSFETs, channel stress was primarily achieved by tensile stress CESL, where high stress (HS) and low stress (LS) were attained by modulating the intrinsic stress level of CESL. For PSS pMOSFETs, we adopted the embedded epitaxy SiGe in S/D regions for all splits with the same Ge fraction but slightly modulated conditions: PSS_HS and PSS_LS splits have different offset spacer thicknesses (S_1 for PSS_HS, and S_2 [$> S_1$] for PSS_LS) but with the same SiGe recess depth (t_1), while PSS_HS2 and PSS_LS splits have the same offset spacer thickness (S_2) but with different SiGe recess depths (t_2 [$> t_1$] for PSS_HS2). Since all PSS CMOSFETs have wide channel width and short channel length, it is rational to speculate that electrical characteristics of PSS MOSFETs are primarily affected by channel stress along the current direction (i.e., longitudinal channel stress).

3.2.2 Transfer and Output Current–Voltage (*I–V*) Characteristics

Fig. 3.2(a) shows the drain current (I_d) versus gate voltage (V_G) characteristics of the control and PSS_HS CMOSFETs. Nominally identical subthreshold I_d–V_G characteristics, as indicated by similar threshold voltages (V_T), subthreshold swings, and drain-induced barrier lowerings (DIBLs), are observed for both the control and PSS_HS devices. Here, the almost identical subthreshold transfer curves (I_d–V_G) between the control and PSS_HS excludes factors that would induce changes of channel backscattering ratio (r_{sat0}), because both carrier mean-free-path (MFP) for channel backscattering (λ_0) and k_BT layer thickness (l_0) (see (2.1c) in Chapter 2) are

considerably affected by V_G and V_D [3.5]. These excluded factors include poor short channel behavior, process-to-process and die-to-die variations. For example, larger DIBL means a stronger lateral electric field in a MOSFET, which produces sharper potential profile near the source side, and thus thinner l_0 and smaller r_{sat0} [3.7][3.15].

Fig. 3.2(b) shows the drain current (I_d) versus drain voltage (V_D) characteristics of the control and PSS_HS CMOSFETs. Based on the similar inversion capacitance–voltage (C–V) characteristics between the control and PSS_HS devices, as shown in Fig. 3.3, PSS_HS nMOSFETs and pMOSFETs show about 19 % and 36 % gain in saturation drain current (I_{dsat}) at $|V_G - V_{T,sat}| = |V_D| = 1$ V, where $V_{T,sat}$ is the saturation threshold voltage defined as $V_{T,sat} = V_{T,lin} - \Delta V_{DIBL}$. $V_{T,lin}$ is the linear threshold voltage evaluated by maximum transconductance ($G_{m,max}$) method, and ΔV_{DIBL} is calculated by constant current method as $\Delta V_{DIBL} = V_T(@|V_D| = 10\text{ mV}) - V_T(@|V_D| = 1\text{ V})$, where V_T is defined as the V_G at $|I_d| = 0.1 \times W/L\ \mu A$.

3.2.3 Temperature Coefficients of Saturation Drain Current and Threshold Voltage

According to the analytic expression developed by the temperature-dependent extraction method [3.20], as shown in (2.10) of Chapter 2, we can extract the λ_0 / l_0 ratio at room temperature (T= 23 ℃) after inputting parameters α, η, V_G, and $V_{T,sat}$, where α and η are the temperature coefficients of I_{dsat} and $V_{T,sat}$, respectively. Figs. 3.4(a) and 3.4(b) show the percentage change of I_{dsat} measured at low-temperatures (T= 0, –15, –30, –45 ℃) relative to that measured at room temperature (T= 23 ℃) as a function of physical gate length ($L_{physical}$) for nMOSFETs ($L_{physical}$= 55–195 nm), and pMOSFETs ($L_{physical}$= 75–315 nm), respectively. For a given $L_{physical}$, all devices exhibit increased I_{dsat} with decreasing temperature, which is ascribed to the phonon scattering events being suppressed as temperature is lowered (from 296 K down to

228 K in this work) [3.21]. On the other hand, for a given temperature, the I_{dsat} increment decreases with decreasing $L_{physical}$ since the influence of halo/pocket implants on channel mobility deterioration is stronger for short channel devices [3.22]. Then, by fitting a group of data with the same $L_{physical}$ in Figs. 3.4(a) and 3.4(b), we obtain the dependence of temperature coefficient of I_{dsat}, i.e., α, on $L_{physical}$, as shown in Fig. 3.4(c). It is found that, as $L_{physical}$ shrinks to sub-100-nm regime, PSS_HS nMOSFETs with uniaxial tensile strain show a slight increase in α relative to the control, whereas PSS_HS pMOSFETs with uniaxial compressive strain show a significant degradation in α [3.16][3.17].

Figs. 3.5(a) and 3.5(b) show the shift of low-temperature (T= 0, –15, –30, –45 ℃) $V_{T,sat}$ relative to room-temperature (T= 23 ℃) $V_{T,sat}$ as a function of $L_{physical}$ for nMOSFETs and pMOSFETs, respectively. Irrespective of strained channel, the $|V_{T,sat}|$ of all devices increases with decreasing temperature, which is attributed to the change of band gap [3.23] and is consistent with the results of MOSFET modeling for low temperature [3.24]. The temperature coefficient of $V_{T,sat}$, i.e., η, can be extracted by fitting the slope of $\Delta V_{T,sat}$ versus ΔT and the results are shown in Fig. 3.5(c), where the sign of η is positive for pMOSFETs owing to its decreasing shift of $V_{T,sat}$ with decreasing temperature [3.23]. In addition, the difference of η between the control and PSS_HS MOSFETs is negligible.

3.2.4 Influence of Uniaxial Stress on Channel Backscattering Ratio

Fig. 3.6(a) shows the extracted λ_0 / l_0 ratio for the control and PSS_HS CMOSFETs. A slight increase in λ_0 / l_0 is observed for tensile PSS_HS nMOSFETs, while compressive PSS_HS pMOSFETs show significant reduction in λ_0 / l_0. Moreover, we found that for PSS_HS CMOSFETs the trend of strain-induced λ_0 / l_0 modulation is similar to that of α shown in Fig. 3.4(c), because both PSS_HS and

control MOSFETs have almost identical η [as shown in Fig. 3.5(c)] and $V_{T,sat}$ [as shown in Fig. 3.2(a)]. This suggests that the sensitivity of I_{dsat} on low temperature primarily determines the λ_0 / l_0 ratio [3.16]. According to (2.1c) in Chapter 2, owing to the inverse proportion between r_{sat0} and λ_0 / l_0, PSS_HS nMOSFETs show a slight improvement (decrease) in r_{sat0} relative to the control, whereas the r_{sat0} of PSS_HS pMOSFETs exhibit a noticeable degradation (increase) and becomes more evident in sub-100-nm regime. In contrast to the dependence of r_{sat0} on $L_{physical}$, the B_{sat0} of all devices increases with decreasing $L_{physical}$. In addition, the B_{sat0} of PSS_HS nMOSFETs slightly improves, while that of PSS_HS pMOSFETs significantly degrades. The above results indicate that as carriers are injected from the source into the channel, the injected electrons suffer less channel backscattering ratio for nMOSFETs with uniaxial tensile stress, while injected holes encounter much more channel backscattering for pMOSFETs with uniaxial compressive stress.

For tensile PSS_HS nMOSFETs, the decrease in r_{sat0} results from a reduction in carrier scattering and thus an increase in MFP, which is related to the improved average of the microscopic relaxation time multiplying by the carrier velocity [3.25]. This explanation of strained-induced r_{sat0} decrease for nMOSFETs is found by full-band Monte Carlo simulation as well [3.13][3.25]. However, the reasons accounting for deteriorated r_{sat0} of strained pMOSFETs have not been reported and understood yet. We will address this point later in Section 3.3.

3.2.5 Correlation between Strain-Induced Saturation Drain Current Gain, Ballistic Efficiency Modulation, and Injection Velocity Enhancement

As shown in (2.3) of Chapter 2, I_{dsat} is entirely determined by ballistic efficiency (B_{sat0}) and carrier injection velocity (υ_{inj0}) for a given inversion charge density (Q_{inv}). First, we evaluate the Q_{inv} of a MOSFET with an area of 100 μm^2 under strong

inversion, taking into account V_T roll-off and DIBL effect, as shown in Fig. 3.7(a) [3.26]. Once I_{dsat}, B_{sat0}, and Q_{inv} are found, then the υ_{inj0} of a MOSFET can be calculated by (2.3). In Fig. 3.7(b), PSS_HS CMOSFETs show improved υ_{inj0} relative to the control, especially for PSS_HS pMOSFETs with shorter $L_{physical}$, which is consistent with the results of previous reports [3.6][3.14][3.25][3.27][3.28]. Thanks to strain-induced energy band splitting, carriers prefer to occupy the energy subband with lower carrier conduction mass, and then the reduction of effective mass raises the υ_{inj0} by (2.1f) in Chapter 2 [3.6][3.14][3.28]. Besides, some materials with lower density of state for MOSFET channel region, such as strained Si, also account for injection velocity enhancement, since degenerate carrier velocity is inversely proportional to the square root of density of state [3.6][3.14][3.28]. Here, PSS_HS pMOSFETs demonstrate more significant $\Delta\upsilon_{inj0}$ as compared with PSS_HS nMOSFETs, because the device structure with embedded epitaxial SiGe in S/D regions significantly lowers the in-plane hole mass, which stemmed from band warping and carrier repopulation [3.2].

Then, from Figs. 3.6(c) and 3.7(b), we plot the dependence of the I_{dsat} enhancement (ΔI_{dsat}) on strain-induced υ_{inj0} improvement ($\Delta\upsilon_{inj0}$) and B_{sat0} modulation (ΔB_{sat0}) for tensile PSS_HS nMOSFETs ($L_{physical}$= 55–195 nm) and compressive PSS_HS pMOSFETs ($L_{physical}$= 75–315 nm) in Fig. 3.8, where ΔI_{dsat}, $\Delta\upsilon_{inj0}$, and ΔB_{sat0} are defined as $\Delta I_{dsat}= (I_{dsat,PSS} - I_{dsat,Ctrl}) / I_{dsat,Ctrl}$, $\Delta\upsilon_{inj0}= (\upsilon_{inj0,PSS} - \upsilon_{inj0,Ctrl}) / \upsilon_{inj0,Ctrl}$, and $\Delta B_{sat0}= (B_{sat0,PSS} - B_{sat0,Ctrl}) / B_{sat0,Ctrl}$, respectively, and the subscripts "Ctrl" and "PSS" represent the control and PSS devices, respectively. The solid line in the figure shows the linear one-to-one proportion. For longer channel of PSS_HS CMOSFETs (nMOSFETs [$L_{physical}$= 195 nm], and pMOSFETs [$L_{physical}$= 145–315 nm]), the ΔB_{sat0} is negligible but the $\Delta\upsilon_{inj0}$ is noticeably improved relative to the control. Similarly, for shorter channel devices (nMOSFETs [$L_{physical}$= 55–85 nm], and pMOSFETs [$L_{physical}$=

75–125 nm]), both PSS_HS devices show significantly improved υ_{inj0}, especially for pMOSFETs. On the other hand, ΔB_{sat0} of pMOSFETs is small and becomes negative as $\Delta I_{dsat} > 20\%$, while that of nMOSFETs is positive for ΔI_{dsat}. We also observe that ΔI_{dsat} is roughly equal to the sum of ΔB_{sat0} and $\Delta\upsilon_{inj0}$ [3.16][3.17], where a slight underestimation of ΔI_{dsat} for PSS_HS nMOSFETs is due to a minor Q_{inv} difference between PSS_HS and the control [3.17]. The above findings suggest that for strained nMOSFETs, uniaxial tensile strain is beneficial for boosting the drain current since both υ_{inj0} and B_{sat0} are increased. For strained pMOSFETs with uniaxial compressive stress, the I_{dsat} is still improved through the significant enhancement of υ_{inj0} at the expense of B_{sat0} loss. If one could conceive a clever method to enhance ballistic efficiency without sacrificing injection velocity enhancement, ultimate PSS performance should be reachable. Thus, it is vital to understand what mechanisms account for B_{sat0} degradation of strained pMOSFETs. This will be discussed in the next section.

3.3 Mechanism for Strain-Induced Backscattering Ratio Modulation

In this section, we will first study the mechanism for backscattering ratio reduction of PSS nMOSFETs. Then, analysis is performed on splits with different channel stresses for PSS pMSOFETs with focus on their channel backscattering characteristics in terms of channel backscattering ratio and carrier injection velocity. The phenomenon for backscattering ratio increase of PSS pMOSFETs is also addressed.

3.3.1 Mechanism for Decrease in Backscattering Ratio of PSS nMOSFETs

Here, we study the mechanism for r_{sat0} modulation of PSS_HS CMOSFETs in terms of carrier MFP for channel backscattering (λ_0) and k_BT layer thickness (l_0),

since the change of r_{sat0} is directly related to the modulated λ_0 and l_0, as indicated in (2.1c) of Chapter 2. We first evaluate λ_0 by using (2.1d) of Chapter 2, where low-field channel mobility of MOSFETs is estimated by the total resistance slope-based method [3.29]. Then, l_0 can be calculated by substituting the extracted λ_0 into λ_0 / l_0 ratio. Fig. 3.9 shows $\lambda_{0,PSS}$-to-$\lambda_{0,Ctrl}$ ratio ($\lambda_{0,PSS} / \lambda_{0,Ctrl}$) versus $l_{0,PSS}$-to-$l_{0,Ctrl}$ ratio ($l_{0,PSS} / l_{0,Ctrl}$) for tensile PSS_HS nMOSFETs ($L_{physical}$= 55–85 nm) and compressive PSS_HS pMOSFETs ($L_{physical}$= 75–105 nm). The $l_{0,PSS}$ of PSS_HS CMOSFETs is reduced to about 90% of $l_{0,Ctrl}$, where the thinning of $l_{0,PSS}$ may be attributed to the strain-induced energy band modulation which causes a sharper potential profile [3.16]. Furthermore, tensile PSS_HS nMOSFETs depict a slight increase of λ_0, consistent with the results of Monte Carlo simulation of [3.25], i.e., electron MFP increases with increasing strain through the increment of microscopic relaxation time and carrier injection velocity, as mentioned earlier. However, compressive PSS_HS pMOSFETs show moderate decrease of λ_0 despite a significantly increased υ_{inj0}.

3.3.2 Influence of SiGe Proximity and Recess Depth on Backscattering Ratio of PSS pMOSFETs

According to the information presented in previous reports and the device structure, we speculate that two mechanisms may account for r_{sat0} degradation (increase) of compressive PSS_HS pMOSFETs: 1) excess carrier scattering caused by the encroachment of Ge into the channel [3.18]; 2) enhanced phonon scattering due to compressed lattice constant relative to the control [3.30]. To examine the possibility of the first mechanism for increased r_{sat0}, we utilize the energy dispersive spectroscopy (EDS) of transmission electron microscopy (TEM) to estimate the magnitude of Ge signal near the source side of channel region. The results are shown in Fig. 3.10. From the TEM cross-section and Ge signal distribution of PSS_HS pMOSFETs, the first

mechanism seems to be minor since Ge signal in the source side of channel region is negligible.

Then, we divide the PSS pMOSFETs into three splits, i.e., PSS_LS, PSS_HS and PSS_HS2, by varying SiGe recess depth and offset spacer thickness (Table 3.1) to examine the second mechanism. For PSS pMOSFETs, comparable ΔI_{dsat} is observed for PSS_HS (36%) and PSS_HS2 (35%) splits at $|V_G - V_{T,sat}| = |V_D| = 1$ V and $L_{physical} =$ 75 nm, while the I_{dsat} gain is down to 23% for PSS_LS [3.18]. It indicates how significant the proximity of S/D SiGe to channel region and its volume affect the performance enhancement [3.18][3.31]. Figs 3.11(a) and 3.11(b) compare the extracted r_{sat0} and υ_{inj0} among all splits of PSS pMOSFETs ($L_{physical} = 75–125$ nm). It is noted that, with deeper SiGe recess depth (e.g., PSS_HS2 [$t_2 > t_1$] relative to PSS_LS [t_1]), r_{sat0} degradation (increase) is observed, where PSS_HS2 split that exhibits larger SiGe volume is expected to induce higher channel stress. Moreover, by comparing the r_{sat0} of PSS_HS2 and PSS_HS splits, it is worthy to note that PSS_HS split has larger r_{sat0} than PSS_HS2, where PSS_HS split has smaller offset spacer thickness, i.e., its SiGe heterojunction is closer to channel region. The rank of r_{sat0} for all PSS splits relative to the control is shown as follows: PSS_HS > PSS_HS2 > PSS_LS > Ctrl. This r_{sat0} rank of all PSS splits indicates that: 1) r_{sat0} is more sensitive to the proximity of S/D SiGe to the channel region than SiGe recess depth; 2) the modulation of channel backscattering ratio is related to the channel stress level. The rank of υ_{inj0} of all PSS splits, as shown in Fig. 3.11(b), is the same as that of r_{sat0}, which also confirms the argument that the r_{sat0} change is mainly affected by channel stress.

3.3.3 Mechanism for Increase in Backscattering Ratio of PSS pMOSFETs

According to [3.30], compressed lattice-induced excess phonon scattering is ascribed to phonon redistribution. That is, lattice distortion can induce changes in

phonon frequency that alters the phonon distribution. Because for PSS pMOSFETs with embedded SiGe S/D, the uniaxial compressive stress is spatially distributed from S/D into the channel region and is expected to be higher at the source side [3.32], the lattice constant also varies spatially. As the lattice constant decreases with increasing compressive stress, the phonon distribution is affected, which may account for severer phonon scattering. As a result, worse channel backscattering ratio is found [3.18]. λ_0 and l_0 are experimentally extracted and the results are shown in Fig. 3.11(c). PSS_HS pMOSFETs have the smallest λ_0, i.e., worst channel backscattering ratio, among all PSS splits. In addition, theoretical Monte Carlo simulation for quasi-ballistic MOSFETs indicates that phonon scattering suppresses the carrier ballistic efficiency and thus significantly reduces the drain current [3.33]. This positively verifies the second mechanism: compressed lattice induces excess phonon scattering and causes an increase of the channel backscattering ratio of PSS pMOSFETs.

In Fig. 3.12, similar to the case of PSS pMOSFETs, nMOSFETs with lower channel stress (PSS_LS) show negligible ΔB_{sat0}, compared with the control, where the I_{dsat} gain of PSS_LS and PSS_HS splits are 7 % and 19 % at $|V_G - V_{T,sat}| = |V_D| = 1$ V, respectively [3.19]. This finding reveals that channel stress definitely affects the channel backscattering behavior of nanoscale strained CMOSFETs, and the degree of r_{sat0} change depends on the channel stress level of PSS CMOSFETs.

3.4 Influence of Carrier Degeneracy and S/D Parasitic Resistance on Channel Backscattering Ratio

In this section, we will discuss the influence of carrier degeneracy, and S/D parasitic resistance on channel backscattering ratio.

3.4.1 Comparison of Nondegenerate and Degenerate-Limited Channel

Backscattering Ratio

As stated earlier in Section 2.4.2, when inversion carrier density (n_S) is comparable to 10^{13} cm^{-2} (or the MOSFET is biased at high V_G [> V_T]), carrier degeneracy effect should be considered for more accurate *I*–*V* model but complicated mathematics will be involved in the evaluation of r_{sat0} [3.34]. Thus, we adopt the assumption of degenerate-limited carrier statistics for simplifying the mathematics calculation [3.35], where the analytic expression of evaluating degenerate-limited r_{sat} is shown as (2.13) in Chapter 2. Fig. 3.13(a) shows the ballistic efficiency of the control and PSS_HS CMOSFETs with nondegenerate and degenerate-limited carrier statistics. For devices with degenerate-limited carrier statistics, higher B_{sat} is found, which is primarily due to degeneracy effect resulting in longer carrier MFP for channel backscattering (λ) relative to nondegenerate carrier MFP (λ_0) [3.15][3.19]. It is also noted that the trend of strain-induced ballistic efficiency change relative to the control is the same for both nondegenerate and degenerate-limited cases although a quantitative offset exists between the two cases. Moreover, we plot the dependence of ΔI_{dsat} on ballistic efficiency modulation for both carrier statistics cases, as shown in Fig. 3.13(b). The similar dependence for both cases again justifies that the nondegenerate assumption is adequate for evaluating the influence of uniaxial stress on channel backscattering characteristics.

3.4.2 Influence of S/D Parasitic Resistance on Channel Backscattering Ratio

Utilizing the deduced analytic expressions of (2.10) and (2.17) shown in Chapter 2, we estimate the nondegenerate ballistic efficiency with and without S/D parasitic resistance (R_{SD}) in Fig. 3.14. For pMOSFETs, the B_{sat0} of both the control and PSS_HS with R_{SD} are almost unchanged relative to that without R_{SD}. While for nMOSFETs, R_{SD} slightly reduces the magnitude of B_{sat0} by around 7 %. Despite the

slight offset arising from R_{SD} effect, the trend of strain-induced B_{sat0} modulation is similar for both cases. It suggests that in this study the characterization of channel backscattering parameters without R_{SD} consideration is still adequate for analyzing the channel backscattering behavior of PSS MOSFETs.

3.5 Conclusions

In this chapter, we have characterized process-strained Si (PSS) CMOSFETs to investigate the influence of uniaxial strain on channel backscattering characteristics. By using a temperature-dependent analytic model to evaluate the channel backscattering ratio (r_{sat0}), and comparing with the control, we found that the r_{sat0} modulation is different between PSS nMOSFETs and PSS pMOSFETs: the r_{sat0} is slightly improved (reduced) for tensile PSS nMOSFETs but significantly degraded (increased) for compressive PSS pMOSFETs. To understand the mechanism responsible for the above observation, we have also characterized the r_{sat0} of PSS CMOSFETs with lower channel stress. We found that the higher the channel stress, the more decrease (increase) in the r_{sat0} of tensile (compressive) PSS nMOSFETs (pMOSFETs), revealing that the strain-induced backscattering ratio modulation is dependent on the stress polarity. The finding also suggests that the modulation of backscattering ratio results from the strain effect. Furthermore, by estimating the carrier mean-free-path for channel backscattering (MFP, λ_0) and k_BT layer thickness (l_0) of PSS CMOSFETs, it is noted that the slightly increased λ_0 may account for the reduced r_{sat0} of tensile PSS nMOSFETs, and the significantly increased r_{sat0} of PSS pMOSFETs may be attributed to the excess phonon scattering caused by the compressed lattice. Furthermore, we have studied the correlation between I_{dsat} gain (ΔI_{dsat}), ballistic efficiency modulation (ΔB_{sat0}), and carrier injection velocity change ($\Delta \upsilon_{inj0}$), where ΔI_{dsat} is found to be roughly equal to the sum of ΔB_{sat0} and $\Delta \upsilon_{inj0}$. PSS

nMOSFETs demonstrate enhancement in B_{sat0} and υ_{inj0}, both of which are beneficial for I_{dsat} improvement. However, PSS pMOSFETs exhibit significantly increased υ_{inj0} and degraded B_{sat0}, which suggests a trade-off in overall I_{dsat} improvement. Our results thus suggest that if one could conceive a clever method to enhance ballistic efficiency without sacrificing the I_{dsat} enhancement from raised injection velocity, ultimate performance boost of PSS pMOSFETs should be expected. Finally, we have compared the B_{sat0} with and without the consideration of degenerate carrier statistics, and source/drain (S/D) parasitic resistance (R_{SD}). The similar trend indicates that the impact of process-induced strain on channel backscattering characteristics can be fairly projected by the nondegenerate assumption and/or neglecting the R_{SD} effect.

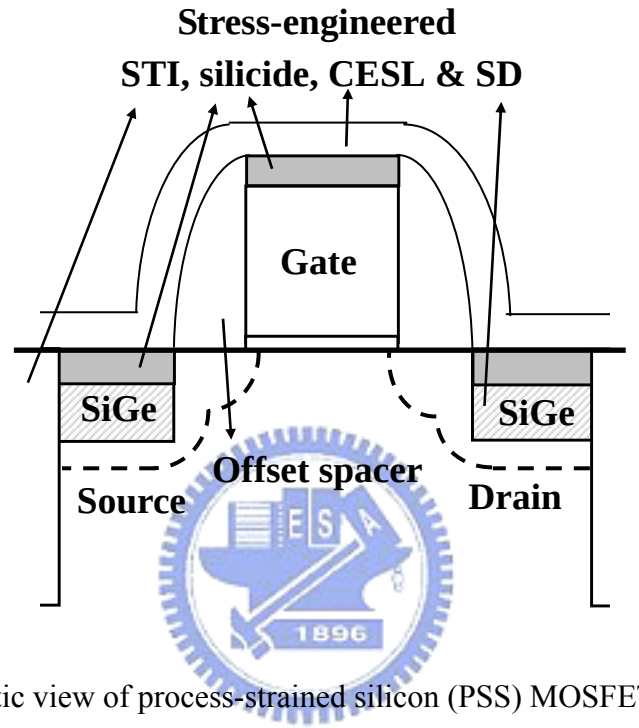

Fig. 3.1. Schematic view of process-strained silicon (PSS) MOSFETs.

Table 3.1. Splits of process-strained Si (PSS) CMOSFETs, where "HS" and "LS" represent high stress and low stress in the channel by modulating process conditions, respectively.

PSS nMOSFETs		
High stress tensile CESL	**PSS_HS**	
Low stress tensile CESL	**PSS_LS**	
PSS pMOSFETs		
	Offset spacer thickness S_1	**Offset spacer thickness S_2 ($S_2 > S_1$)**
SiGe recess depth t_1	**PSS_HS**	**PSS_LS**
SiGe recess depth t_2 ($t_2 > t_1$)	**—**	**PSS_HS2**

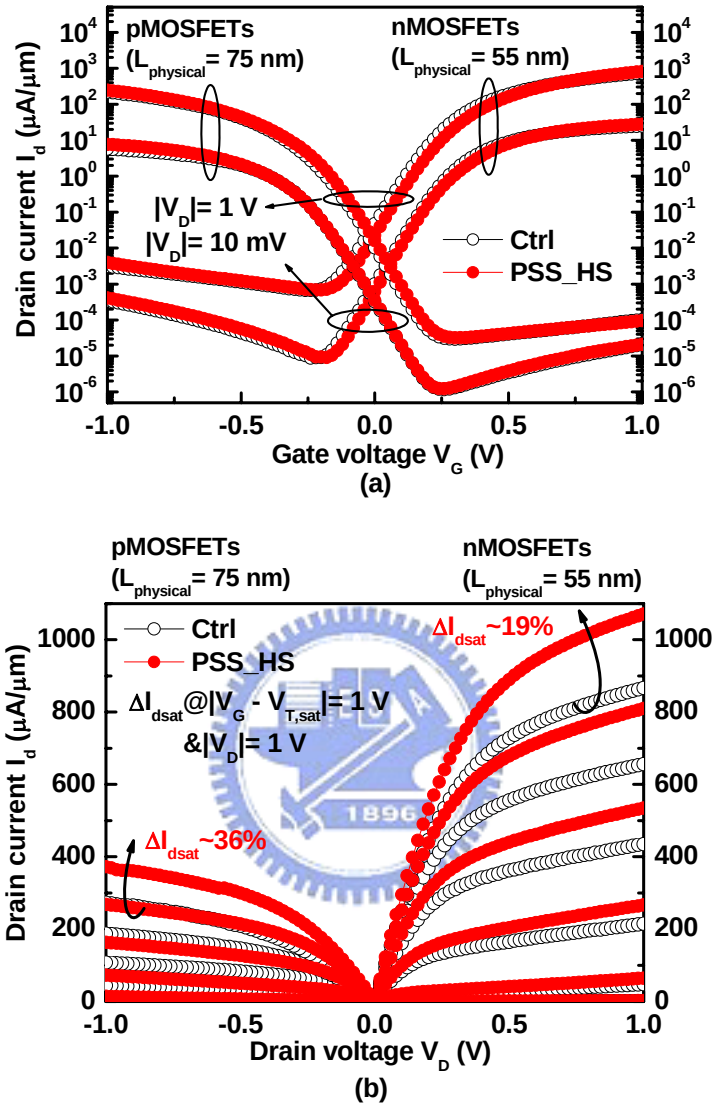

Fig. 3.2. (a) Drain current versus gate voltage (I_d–V_G), and (b) drain current versus drain voltage (I_d–V_D) characteristics of the control and high-stress process-strained Si (PSS_HS) CMOSFETs, where $V_{T,sat}$ is the saturation threshold voltage.

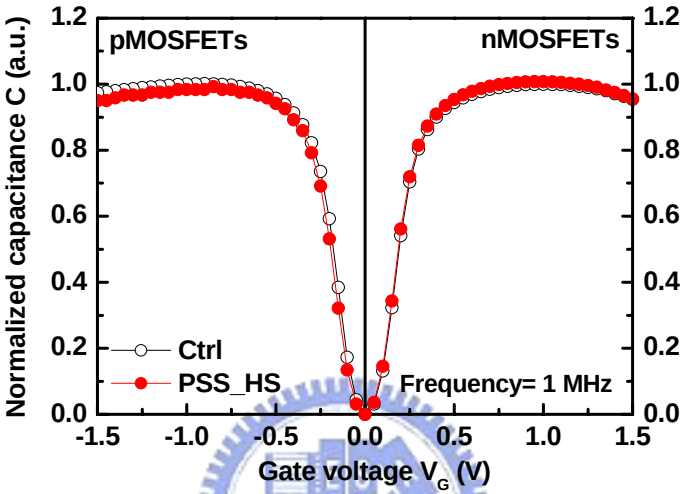

Fig. 3.3. Capacitance versus gate voltage (*C*-*V*) characteristics in inversion region for the control and PSS_HS CMOSFETs. The capacitance is normalized with respect to the capacitance of the control at $|V_G|$= 1 V. Nominally identical inversion *C*-*V* curves are observed.

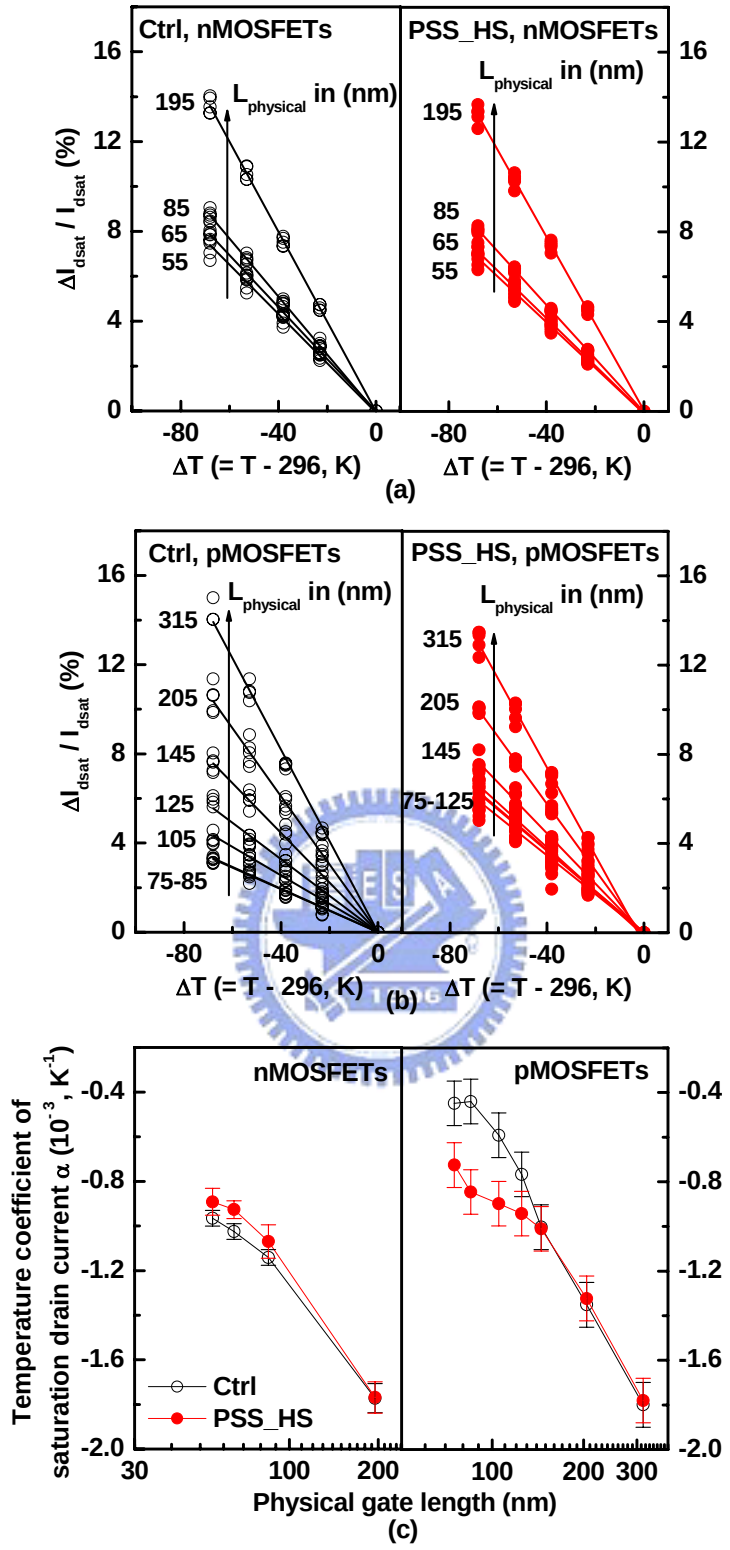

Fig. 3.4. Percentage change of I_{dsat} measured at low-temperatures (T= 0, –15, –30, –45℃) relative to that measured at room-temperature (T= 23 ℃) as a function of physical gate length ($L_{physical}$) for the control and PSS_HS (a) nMOSFETs ($L_{physical}$= 55–195 nm), and (b) pMOSFETs ($L_{physical}$= 75–315 nm). The fitting slope of ΔI_{dsat} / I_{dsat} versus ΔT represents the temperature coefficient of I_{dsat} (α), as shown in (c).

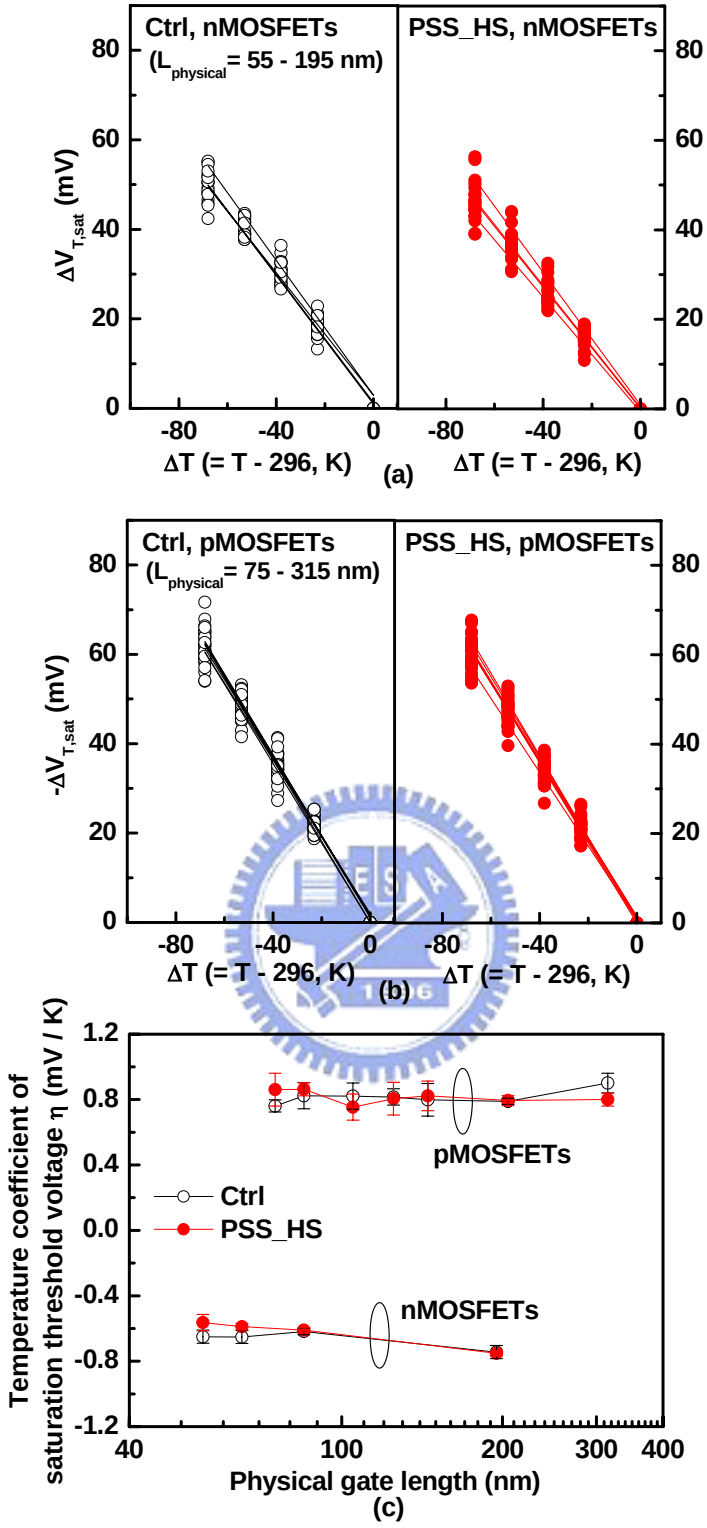

Fig. 3.5. Shift of low-temperature (T= 0, –15, –30, –45℃) saturation threshold voltage ($V_{T,sat}$) relative to room temperature (T= 23℃) $V_{T,sat}$ as a function of physical gate length ($L_{physical}$) for the control and PSS_HS (a) nMOSFETs ($L_{physical}$= 55–195 nm), and (b) pMOSFETs ($L_{physical}$= 75–315 nm). The fitting slope of $\Delta V_{T,sat}$ versus ΔT represents the temperature coefficient of $\Delta V_{T,sat}$ (η), as shown in (c).

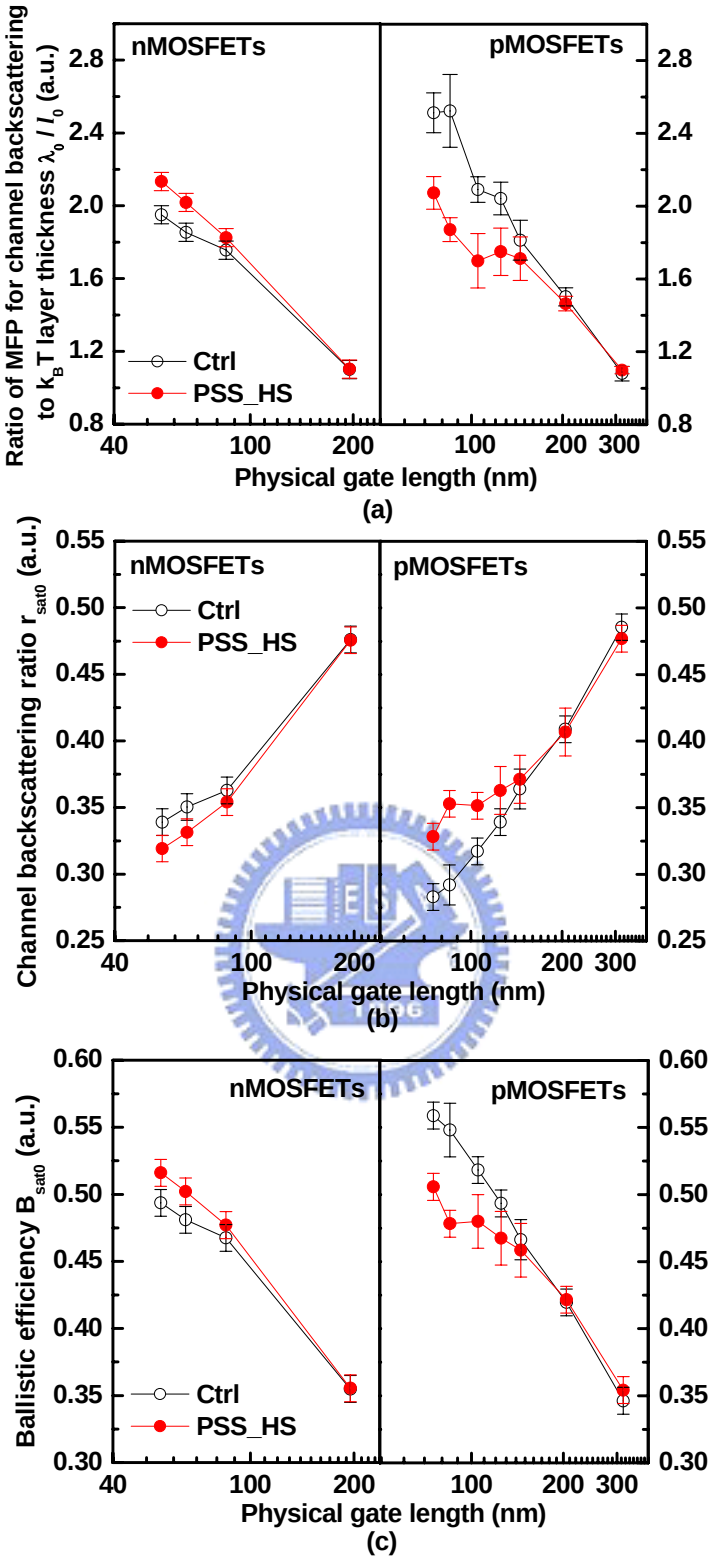

Fig. 3.6. (a) Ratio of carrier mean-free-path (MFP) for channel backscattering (λ_0) to k_BT layer thickness (l_0) extracted by the temperature-dependent analytic model. From λ_0 / l_0, channel backscattering ratio (r_{sat0}= 1 / [1 + λ_0 / l_0]) and ballistic efficiency (B_{sat0}= [1 − r_{sat0}] / [1 + r_{sat0}]) can be found for the control and PSS_HS CMOSFETs, as shown in (b) and (c), respectively.

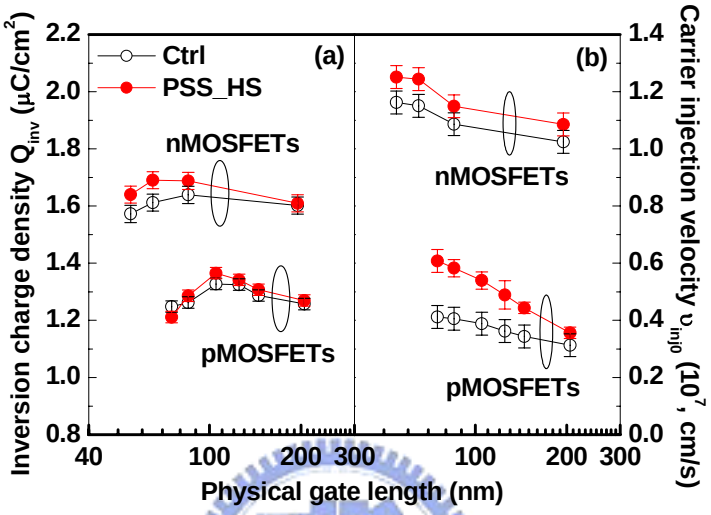

Fig. 3.7. Comparisons of the extracted (a) inversion charge density (Q_{inv}), and (b) carrier injection velocity (υ_{inj0}) between the control and PSS_HS CMOSFETs.

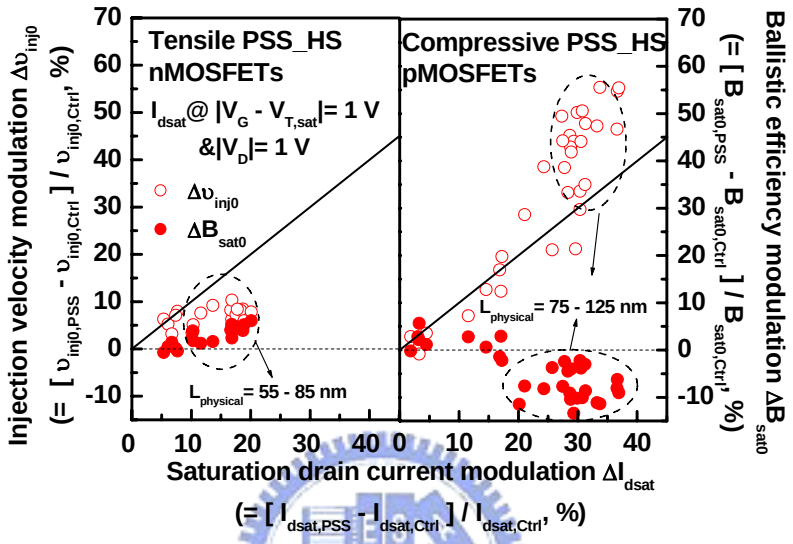

Fig. 3.8. Dependence of strain-induced injection velocity enhancement ($\Delta\upsilon_{inj0}$= [$\upsilon_{inj0,PSS}$ − $\upsilon_{inj0,Ctrl}$] / $\upsilon_{inj0,Ctrl}$, *y*-axis in left), and ballistic efficiency modulation (ΔB_{sat0}= [$B_{sat0,PSS}$ − $B_{sat0,Ctrl}$] / $B_{sat0,Ctrl}$, *y*-axis in right) on saturation drain current gain (ΔI_{dsat}= [$I_{dsat,PSS}$ − $I_{dsat,Ctrl}$] / $I_{dsat,Ctrl}$) for tensile PSS_HS nMOSFETs ($L_{physical}$= 55–195 nm) and compressive PSS_HS pMOSFETs ($L_{physical}$= 75–315 nm), where the subscripts "PSS" and "Ctrl" represent the PSS and control devices, respectively. The solid line is the linear proportional line.

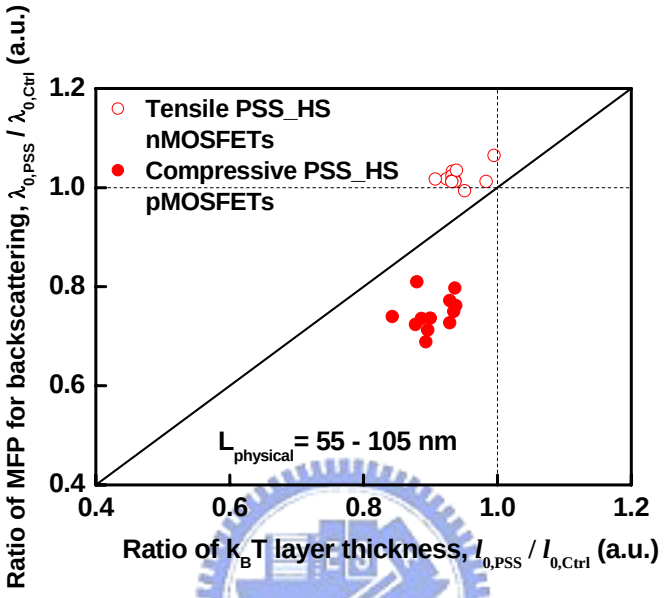

Fig. 3.9. $\lambda_{0,PSS}$-to-$\lambda_{0,Ctrl}$ ratio ($\lambda_{0,PSS}$ / $\lambda_{0,Ctrl}$) versus $l_{0,PSS}$-to-$l_{0,Ctrl}$ ratio ($l_{0,PSS}$ / $l_{0,Ctrl}$) for tensile PSS_HS nMOSFETs ($L_{physical}$= 55–85 nm) and compressive PSS_HS pMOSFETs ($L_{physical}$= 75–105 nm).

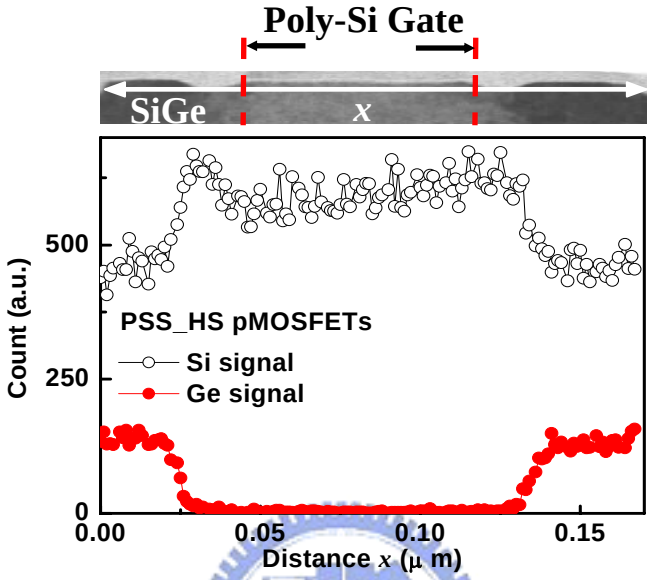

Fig. 3.10. Cross-sectional transmission electron microscopy (TEM) image of PSS_HS pMOSFETs and the energy dispersive spectroscopy (EDS) spectrum. It is noted that Ge signal drops abruptly in the adjacent region of SiGe S/D and Si channel. No Ge diffusion into the channel is observed.

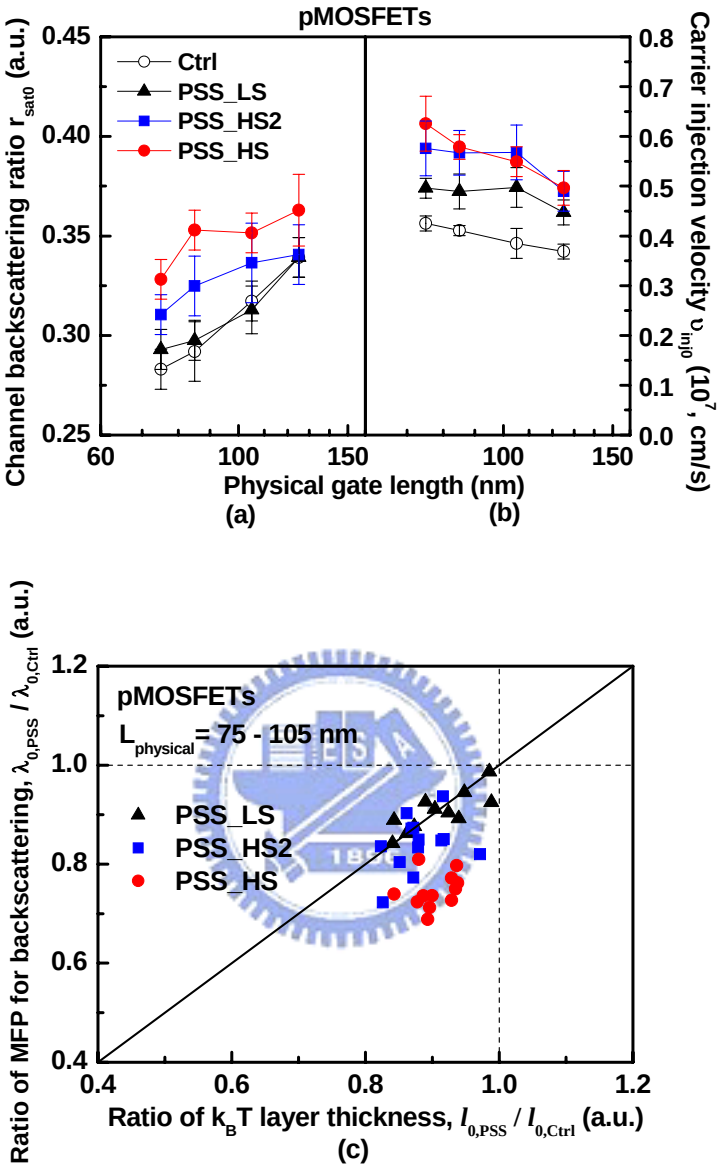

Fig. 3.11. Comparisons of extracted (a) channel backscattering ratio (r_{sat0}), (b) carrier injection velocity (υ_{inj0}), and (c) $\lambda_{0,PSS}$-to-$\lambda_{0,Ctrl}$ ratio ($\lambda_{0,PSS}$ / $\lambda_{0,Ctrl}$) versus $l_{0,PSS}$-to-$l_{0,Ctrl}$ ratio ($l_{0,PSS}$ / $l_{0,Ctrl}$) for the control and PSS pMOSFETs ($L_{physical}$= 75–105 nm) with different splits, where "LS" and "HS" represent low stress and high stress devices, respectively.

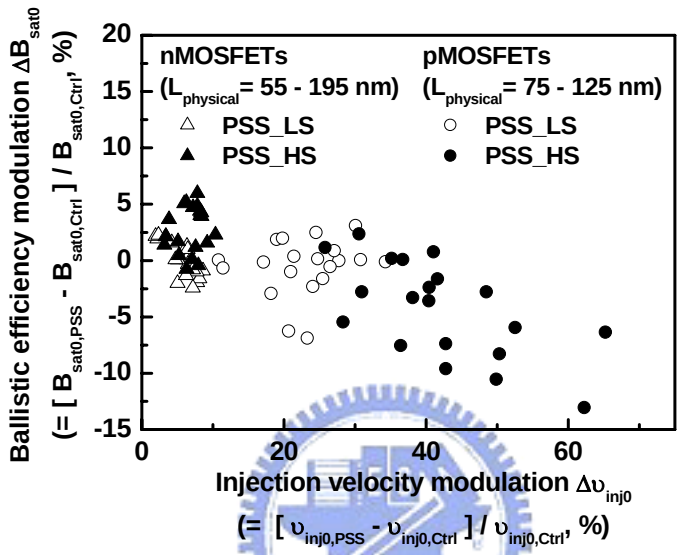

Fig. 3.12. Ballistic efficiency modulation (ΔB_{sat0}) versus carrier injection velocity enhancement ($\Delta\upsilon_{inj0}$) for PSS_HS and PSS_LS CMOSFETs. PSS_HS nMOSFETs depict enhanced ΔB_{sat0} and $\Delta\upsilon_{inj0}$ relative to control devices. PSS_HS pMOSFETs show enhanced $\Delta\upsilon_{inj0}$ but degraded ΔB_{sat0}, suggesting a trade-off in overall drain current enhancement.

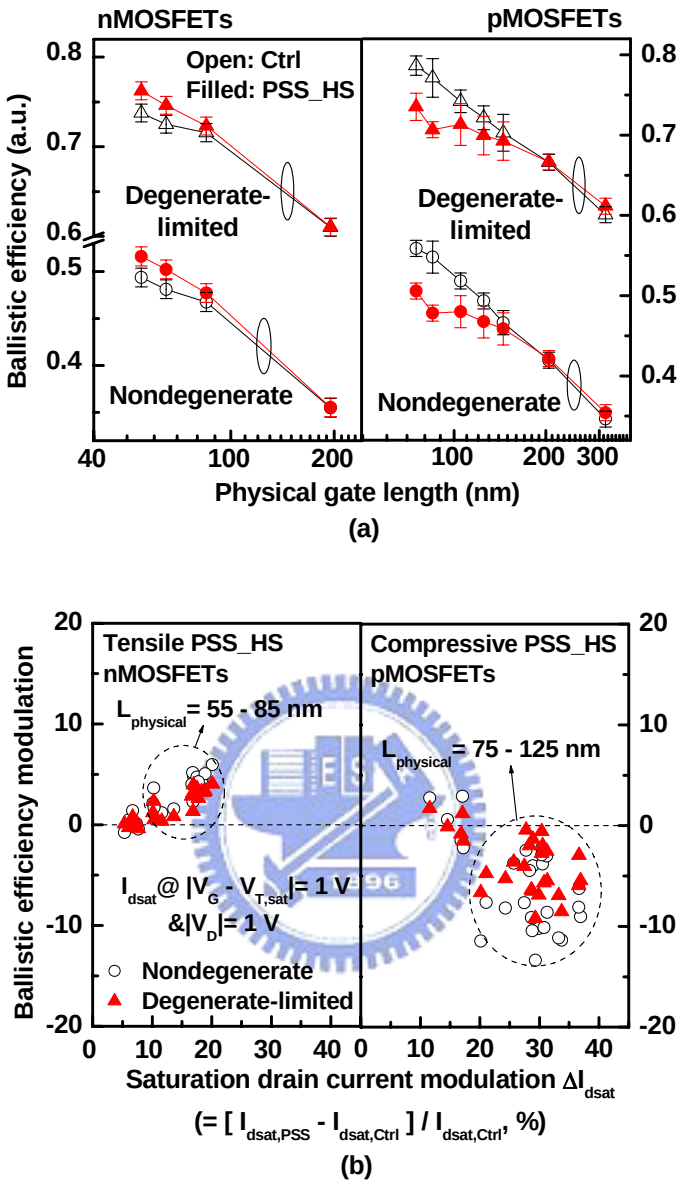

Fig. 3.13. (a) Extracted ballistic efficiency, and (b) dependence of saturation drain current gain (ΔI_{dsat}) on ballistic efficiency modulation for the control and PSS_HS CMOSFETs with nondegenerate and degenerate-limited carrier statistics.

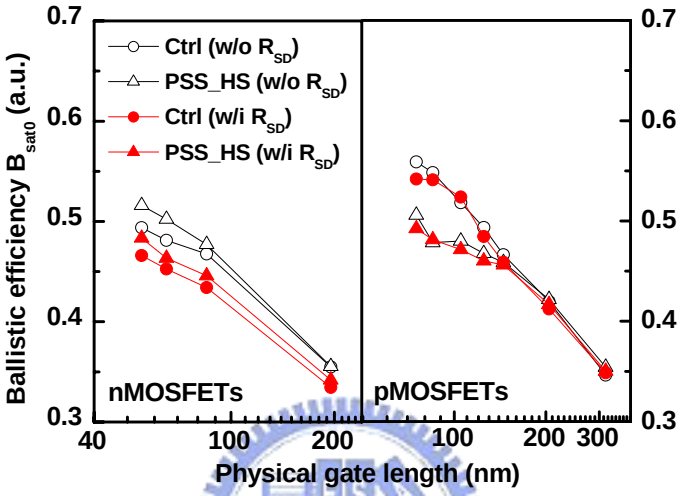

Fig. 3.14. Comparisons of extracted ballistic efficiency of the control and PSS_HS CMOSFETs with and without the consideration of parasitic source/drain (S/D) resistance (R_{SD}).