Chapter 4

A New Methodology of Extracting Source/Drain Parasitic

Resistance for Nanoscale Strained CMOSFETs

4.1 Introduction

Presently uniaxial strain engineering has become one of the mainstream techniques to boost the performance of MOSFETs in nanoscale regime. Thanks to its capability of enhancing channel mobility and drain current without facing lithography limits and process scaling issues, strained techniques are more promising to achieve the targeted performance of MOSFETs, according to international technology roadmap for semiconductors (ITRS), relative to conventional scaling techniques [4.1]. Generally, the enhancements in channel mobility and drain current are considered as important criteria in evaluating the feasibility of a strain technique for CMOS manufacturing. However, as the gate length is aggressively shrunk into sub-100-nm regime, source/drain (S/D) parasitic resistance (R_{SD}) becomes a more and more important contributor to the total resistance (R_{TOTAL}) because of the significant reduction of strain-induced channel resistance (R_{CH}) [4.2]. The resultant R_{SD} progressively deteriorates the current gain of strained MOSFETs in nanoscale regime [4.3][4.4]. Thus, accurate extraction of R_{SD} in nanoscale devices is useful to estimate its influence on drain current degradation and/or further investigate the engineering of R_{SD} reduction for attaining better device performance.

There are a lot of measurement techniques in extracting R_{SD} for deep submicrometer CMOS technology [4.5]. Among them, the shift-and-ratio (S&R) [4.6] and total resistance slope-based methods [4.7] are widely adopted for characterization. For the S&R method, R_{SD} can be simply extracted through the calculation of

mathematical formulas, which merely requires the transfer characteristics (I_d–V_G) of the long- and short-channel devices. However, some assumptions employed in the S&R method, i.e., channel-length-independent mobility and gate-voltage (V_G)-independent R_{SD}, are not adequate for deep-submicrometer MOSFETs with heavy halo implants and lightly doped drain (LDD) structure [4.6][4.8][4.9]. Since the overlap of halo-implanted regions causes the decrease of effective channel mobility of short channel devices, the assumption that the channel mobility is constant over all channel lengths is invalid [4.8]. On the other hand, since the resistance of S/D regions under the gate is modulated by V_G, the independence of R_{SD} on V_G assumed in the S&R method is also inadequate for LDD MOSFETs [4.9].

To circumvent the above issues, Niu *et al*. proposed the R_{TOTAL} slope-based method, where R_{SD} is extracted by fitting the plot of R_{TOTAL} versus the effective channel length (L_{eff}), and extending the fitting line to zero channel length [4.7]. Unlike the S&R method, the R_{TOTAL} slope-based method does not require the exact value of L_{eff} since the device-to-device variation in channel length is reflected on the corresponding L_{eff}. In other words, the R_{SD} extraction is not affected by the characterization techniques of L_{eff} as long as the electrical determination of L_{eff} is consistent for all devices. Furthermore, this method allows the R_{SD} to be any function of V_G, which is suitable for LDD MOSFETs. Despite of these advantages, the R_{TOTAL} slope-based method still suffers from some issues. Firstly, the accuracy of R_{SD} evaluation depends on the quantity of devices. Fitting a linear line from a few data points often results in large uncertainties in fitting slope and intercept (i.e., the magnitude of R_{SD}). Secondly, the R_{TOTAL} does not scale linearly with channel length down to nanoscale regime [4.10]. This is attributed to the reverse short channel effect (RSCE) in devices with shorter channel, leading to stronger Coulomb scattering and higher vertical field under the same gate overdrive, compared with longer channel

devices, causing the reduced channel mobility and increased channel resistivity. Finally, channel mobility is assumed to be independent on the range of L_{eff} used to estimate R_{SD} [4.11]. Thus, greater uncertainty for devices with stronger channel-length-dependent mobility, such as nanoscale strained MOSFETs, is expected.

The S&R and R_{TOTAL} slope-based methods, as stated above, are not suitable for quantifying the channel mobility of nanoscale strained MOSFETs since the channel mobility significantly depends on the values of the L_{eff} and R_{SD}. Therefore, in this work, we propose a new method capable of extracting the R_{SD} without relying on the assumption of channel-length-independent mobility [4.12].

4.2 Methodology of Extracting S/D Parasitic Resistance

In this section, before introducing the extraction methodology of R_{SD}, we will investigate the correlation between low-field channel mobility gain ($\Delta\mu$), linear drain current gain (ΔI_{dlin}), and saturation drain current gain (ΔI_{dsat}) in terms of deduced equations. In addition, we will summarize the basic and key equations in a table, and several parameters employed in the equations will be highlighted for its physical meanings.

4.2.1 Low-Field Channel Mobility Gain versus Linear Drain Current Gain

For a MOSFET operating in the linear region, the total resistance (R_{TOTAL}), composed of the intrinsic channel resistance (R_{CH}) and extrinsic S/D parasitic resistance (R_{SD}) (generally including the accumulation layer resistance (R_{ac}), the spreading resistance (R_{sp}), the sheet resistance (R_{sh}), and the contact resistance (R_{co}) as shown in Fig. 4.1) [4.13], is defined as

$$R_{\text{TOTAL}} = \frac{V_{\text{D}}}{I_{\text{dlin}}} = R_{\text{CH}} + R_{\text{SD}}, \qquad (4.1)$$

where V_{D} and I_{dlin} represent the drain voltage and linear drain current, respectively. In (4.1), the equation of I_{dlin} with R_{SD} consideration is expressed as

$$\frac{I_{\text{dlin}}}{W} = \frac{\mu Q_{\text{inv}} \left(V_{\text{D}} - I_{\text{dlin}} R_{\text{SD}} \right)}{L} = \frac{V_{\text{D}} - I_{\text{dlin}} R_{\text{SD}}}{R_{\text{CH}}}, \qquad (4.2)$$

where W, L, μ, and Q_{inv} are the channel width, channel length, low lateral-field channel mobility, and inversion charge density, respectively [4.2]. And it is noted that μ can be related to R_{CH} by $\mu = L / Q_{\text{inv}} R_{\text{CH}}$, where the unit of R_{CH} is Ω-μm. Considering a process-strained Si (PSS) MOSFET [4.14], we can express the enhanced I_{dlin} and μ relative to the control device as

$$\Delta I_{\text{dlin}} = \frac{I_{\text{dlin,PSS}} - I_{\text{dlin,Ctrl}}}{I_{\text{dlin,Ctrl}}}, \qquad (4.3a)$$

and

$$\Delta \mu = \frac{\mu_{\text{PSS}} - \mu_{\text{Ctrl}}}{\mu_{\text{Ctrl}}}, \qquad (4.3b)$$

where the subscripts "PSS" and "Ctrl" represent the strained and control MOSFETs, respectively. Substituting (4.1) and the expression of μ into (4.3a) and (4.3b), respectively, and taking the assumption that both the control and PSS devices exhibit the same W, L, and Q_{inv}, we can rearrange (4.3a) and (4.3b) in terms of R_{TOTAL} and R_{CH} as

$$\Delta I_{\text{dlin}} = \frac{\dfrac{V_D}{R_{\text{TOTAL,PSS}}} - \dfrac{V_D}{R_{\text{TOTAL,Ctrl}}}}{\dfrac{V_D}{R_{\text{TOTAL,Ctrl}}}} = \frac{R_{\text{TOTAL,Ctrl}} - R_{\text{TOTAL,PSS}}}{R_{\text{TOTAL,PSS}}}, \tag{4.4a}$$

and

$$\Delta\mu = \frac{\left(\dfrac{L_{\text{eff}}}{W_{\text{eff}}Q_{\text{inv}}R_{\text{CH,PSS}}}\right) - \left(\dfrac{L_{\text{eff}}}{W_{\text{eff}}Q_{\text{inv}}R_{\text{CH,Ctrl}}}\right)}{\dfrac{L_{\text{eff}}}{W_{\text{eff}}Q_{\text{inv}}R_{\text{CH,Ctrl}}}} = \frac{R_{\text{CH,Ctrl}} - R_{\text{CH,PSS}}}{R_{\text{CH,PSS}}}. \tag{4.4b}$$

Dividing (4.4a) by (4.4b), we can relate ΔI_{dlin} to $\Delta\mu$ as follows

$$
\begin{aligned}
\frac{\Delta I_{\text{dlin}}}{\Delta\mu} &= \left(\frac{R_{\text{TOTAL,Ctrl}} - R_{\text{TOTAL,PSS}}}{R_{\text{TOTAL,PSS}}}\right)\frac{R_{\text{CH,PSS}}}{R_{\text{CH,Ctrl}} - R_{\text{CH,PSS}}} \\
&= \left(\frac{R_{\text{SD,Ctrl}} + R_{\text{CH,Ctrl}} - R_{\text{SD,PSS}} - R_{\text{CH,PSS}}}{R_{\text{SD,PSS}} + R_{\text{CH,PSS}}}\right)\frac{R_{\text{CH,PSS}}}{R_{\text{CH,Ctrl}} - R_{\text{CH,PSS}}} \\
&= \frac{1}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}\left(1 + \frac{R_{\text{SD,Ctrl}} - R_{\text{SD,PSS}}}{R_{\text{CH,Ctrl}} - R_{\text{CH,PSS}}}\right)
\end{aligned} \tag{4.5}
$$

Rearranging (4.5), we can express ΔI_{dlin} as a linear function of $\Delta\mu$ with an offset of resistance (ΔR_{SD}) as

$$
\begin{aligned}
\Delta I_{\text{dlin}} &= \frac{\Delta\mu}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}} + \frac{1}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}\left(\frac{R_{\text{SD,Ctrl}} - R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\right) \\
&= \frac{1}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}\Delta\mu + \frac{R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}\Delta R_{\text{SD}}
\end{aligned} \tag{4.6}
$$

$$= \frac{R_{\text{CH,PSS}}}{R_{\text{TOTAL,PSS}}}\Delta\mu + \frac{R_{\text{SD,PSS}}}{R_{\text{TOTAL,PSS}}}\Delta R_{\text{SD}}, \tag{4.6$'$}$$

where ΔR_{SD} represents the resistance variation, and is defined as $\Delta R_{\text{SD}} = (R_{\text{SD,Ctrl}} -$

$R_{SD,PSS}$) / $R_{SD,PSS}$. It is worthy to note that, as shown in (4.6), the contribution of both $\Delta\mu$ and ΔR_{SD} to ΔI_{dlin} depends on the magnitude of $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio. For example, for long-channel devices with $R_{SD,PSS}$ being much smaller than $R_{CH,PSS}$, $\Delta\mu$ almost equals ΔI_{dlin} because the contribution of ΔR_{SD} to ΔI_{dlin} is negligible. However, as the $R_{SD,PSS}$ of a MOSFET is equal to $R_{CH,PSS}$, such as in nanoscale strained MOSFETs, not only $\Delta\mu$ but also ΔR_{SD} are influential to ΔI_{dlin}. Thus, it is expected that, as the channel length is continuously scaled down, the progressively increased $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio, i.e., the percentage of $R_{SD,PSS}$ to $R_{TOTAL,PSS}$, results in the reduction of $\Delta\mu$-to-ΔI_{dlin} contribution, and the increase of ΔR_{SD}-to-ΔI_{dlin} contribution, as shown in (4.6′). It implies that the S/D parasitic resistance gradually becomes the bottleneck for fully exploiting the benefit of strained MOSFETs down to nanoscale regime.

4.2.2 Low-Field Channel Mobility Gain versus Saturation Drain Current Gain

Dissimilar to the situation of linear drain current, the importance of low lateral field channel mobility to high lateral field carrier transport (saturation drain current) is unclear from the standpoint of conventional current-voltage (*I–V*) model of MOSFETs. This is because as the channel length is shrunk into sub-100-nm regime, the conventional model needs to be modified to account for the off-equilibrium carrier transport, such as velocity overshoot [4.15][4.16] and quasi-ballistic transport [4.17]. Nevertheless, some works, by combining the theoretical Monte Carlo simulation [4.16] and experimental results [4.18] provide the evidence that the effective carrier mobility at low lateral electric field strongly affects the transconductance at saturation region, where the current performance is strongly sensitive to the off-equilibrium transport behaviour. Moreover, Lundstrom *et al.* [4.19], from the viewpoint of scattering theory, developed a simple expression to provide a quantitative relation between effective

channel mobility gain and saturation drain current gain (ΔI_{dsat}) as

$$\Delta I_{dsat} = \left(1 - B_{sat0,PSS}\right)\Delta\mu, \tag{4.7}$$

where $B_{sat0,PSS}$ and $\Delta\mu$ are the ballistic efficiency and low-field channel mobility gain of PSS MOSFETs, respectively. It is used to evaluate how close a MOSFET can operate to ballistic transport limit, i.e., $B_{sat0,PSS}= 1$, where carriers encounter no scattering events from source to drain. In addition, as shown in (4.7), $B_{sat0,PSS}$ also determines the sensitivity of ΔI_{dsat} to $\Delta\mu$. For example, for state-of-the-art technology, $B_{sat0,PSS}$ is about 0.5 [4.20][4.21], so roughly half of $\Delta\mu$ is effectively translated into ΔI_{dsat}. Here, similar to (4.6), we adapt (4.7) with the consideration of R_{SD} as

$$\Delta I_{dsat} = \left(1 - B_{sat0,PSS}\right)\Delta\mu + k\Delta R_{SD}, \tag{4.8}$$

where k is a parameter of determining the translating efficiency of ΔR_{SD} to ΔI_{dsat}. Generally speaking, the value of k should not be larger than unity. The magnitude of k may depend on device dimensions and process conditions [4.22][4.23]. For example, a 25% resistance reduction in embedded SiGe S/D pMOSFET with a 37 nm physical gate length translates to a 7% on-current enhancement, where k is about 0.28 [4.23].

4.2.3 Linear Drain Current Gain versus Saturation Drain Current Gain

Combining (4.6) and (4.8) and eliminating $\Delta\mu$, we obtain the key equation of correlating ΔI_{dlin} with ΔI_{dsat} for strained MOSFETs in terms of its $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio, $B_{sat0,PSS}$, k factor, and ΔR_{SD} as follows

$$\Delta I_{\text{dlin}} = \frac{1}{1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}} \left(\frac{\Delta I_{\text{dsat}} - k\Delta R_{\text{SD}}}{1 - B_{\text{sat0,PSS}}} \right) + \frac{1}{1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}} \left(\frac{R_{\text{SD,Ctrl}} - R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}} \right)$$

$$= \frac{1}{\left(1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\right)\left(1 - B_{\text{sat0,PSS}}\right)} \Delta I_{\text{dsat}} + \frac{\dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\left(1 - B_{\text{sat0,PSS}}\right) - k}{\left(1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\right)\left(1 - B_{\text{sat0,PSS}}\right)} \Delta R_{\text{SD}}. \qquad (4.9)$$

Then making the derivatives of (4.6), (4.8) and (4.9), we can obtain the key equations in this work as follows

$$\frac{\partial\left(\Delta I_{\text{dlin}}\right)}{\partial\left(\Delta\mu\right)} = \frac{1}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}}, \qquad (4.10)$$

$$\frac{\partial\left(\Delta I_{\text{dsat}}\right)}{\partial\left(\Delta\mu\right)} = 1 - B_{\text{sat0,PSS}}, \qquad (4.11)$$

and

$$\frac{\partial\left(\Delta I_{\text{dlin}}\right)}{\partial\left(\Delta I_{\text{dsat}}\right)} = \frac{1}{\left(1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}\right)\left(1 - B_{\text{sat0,PSS}}\right)}. \qquad (4.12)$$

Table 4.1 summarizes the essential equations deduced above. It is noted that these equations consist of several key indexes, i.e., the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio ($R_{\text{SD,PSS}}$ / $R_{\text{CH,PSS}}$), the $R_{\text{CH,PSS}}$-to-$R_{\text{TOTAL,PSS}}$ ratio ($R_{\text{CH,PSS}}$ / $R_{\text{TOTAL,PSS}}$), the $R_{\text{SD,PSS}}$-to-$R_{\text{TOTAL,PSS}}$ ratio ($R_{\text{SD,PSS}}$ / $R_{\text{TOTAL,PSS}}$), the $B_{\text{sat0,PSS}}$ and k factor. The first three indexes are related to the relationship between the low-lateral-field channel mobility, resistance variation, and linear drain current. The $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio is to evaluate both $\Delta\mu$-to-ΔI_{dlin} and ΔR_{SD}-to-ΔI_{dlin} translating efficiency. Once the $R_{\text{SD,PSS}}$-to-$R_{\text{CH,PSS}}$ ratio is obtained, both $R_{\text{CH,PSS}}$-to-$R_{\text{TOTAL,PSS}}$ and $R_{\text{SD,PSS}}$-to-$R_{\text{TOTAL,PSS}}$ ratios can be calculated by (4.1), where both ratios are also used to evaluate the

$\Delta\mu$-to-ΔI_{dlin} and ΔR_{SD}-to-ΔI_{dlin} translating efficiency, respectively. Furthermore, as stated in Chapter 2, $B_{\mathrm{sat0,PSS}}$ is extracted by a temperature-dependent analytic model, and correlates the low-field channel mobility gain with high-field carrier transport (saturation drain current). Finally, k factor is used to evaluate the contribution of resistance reduction to saturation drain current gain, where k factor can be obtained from the extrapolation of (4.6), (4.8), and (4.9).

4.2.4 Methodology of Extracting the Ratio of S/D Parasitic Resistance to Channel Resistance

Fig. 4.2 shows the flow chart of the proposed methodology to extract the $R_{\mathrm{SD,PSS}}$-to-$R_{\mathrm{CH,PSS}}$ ratio of nanoscale strained MOSFETs where the formula of each item is shown next to the corresponding pattern [4.24]. The flow of extracting B_{sat0}, as mentioned in Chapter 2, is shown in the left part enclosed by the dash line, where α and η represent the temperature coefficients of I_{dsat} and $V_{\mathrm{T,sat}}$, respectively. $V_{\mathrm{T,sat}}$ is determined by maximum-transconductance ($G_{\mathrm{m,max}}$) method with drain-induced barrier lowering (DIBL, ΔV_{DIBL}) consideration. Extracting α, η, and $V_{\mathrm{T,sat}}$, we can calculate the ratio of channel backscattering mean-free-path (λ_0) to $k_{\mathrm{B}}T$ layer thickness (l_0), channel backscattering ratio (r_{sat0}) and B_{sat0}, according to the formulas. As shown in (4.12), the derivative of ΔI_{dlin} to ΔI_{dsat}, i.e., the fitting slope of ΔI_{dlin} versus ΔI_{dsat}, is determined by the $R_{\mathrm{SD,PSS}}$-to-$R_{\mathrm{CH,PSS}}$ ratio and $B_{\mathrm{sat0,PSS}}$. In other words, once $B_{\mathrm{sat0,PSS}}$ and the fitting slope of ΔI_{dlin} versus ΔI_{dsat} are known, the $R_{\mathrm{SD,PSS}}$-to-$R_{\mathrm{CH,PSS}}$ ratio can be easily obtained. By substituting the $R_{\mathrm{SD,PSS}}$-to-$R_{\mathrm{CH,PSS}}$ ratio into (4.1), the R_{SD} (and R_{CH}) of strained MOSFETs with nanoscale channel length can be easily found without relying on the controversial assumption and the uncertainty in estimating the effective channel length.

4.3 Conclusions

In this chapter, we propose a new methodology of extracting the ratio of S/D parasitic resistance ($R_{SD,PSS}$) to channel resistance ($R_{CH,PSS}$) for process-strained Si (PSS) MOSFETs with the channel length down to sub-100-nm regime. The extraction of resistance ratio is built on the correlation between linear drain current gain (ΔI_{dlin}) and saturation drain current gain (ΔI_{dsat}) of PSS MOSFETs. From the definitions of total resistance and linear drain current, and assuming that both the control and PSS MOSFETs have nominally identical channel length, channel width, and inversion charge density, we can deduce ΔI_{dlin} as a linear function of low-field channel mobility gain ($\Delta\mu$) with an offset of resistance reduction (ΔR_{SD}), where the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio is the key factor in determining the translating efficiency of $\Delta\mu$ to ΔI_{dlin}. Similarly, ΔI_{dsat} can be expressed as a linear function of $\Delta\mu$ with an offset ΔR_{SD}, where the ballistic efficiency ($B_{sat0,PSS}$) affects the sensitivity of ΔI_{dsat} to $\Delta\mu$. By combining these two linear equations and eliminating $\Delta\mu$, we can deduce the correlation between ΔI_{dlin} and ΔI_{dsat}, where the derivative of ΔI_{dlin} to ΔI_{dsat} is entirely controlled by both the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio and $B_{sat0,PSS}$. In other words, as long as the $B_{sat0,PSS}$ and fitting slope of ΔI_{dlin} versus ΔI_{dsat} are obtained, the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio can be extracted easily without being susceptible to uncertainties of effective channel length evaluation and the assumption of constant channel mobility for all channel lengths.

Silicide **Spacer** **Gate**

R_{sp}

R_{ac}

R_{co} R_{CH}

R_{sh}

Extrinsic Resistance, R_{SD} | **Intrinsic Resistance, R_{CH}**
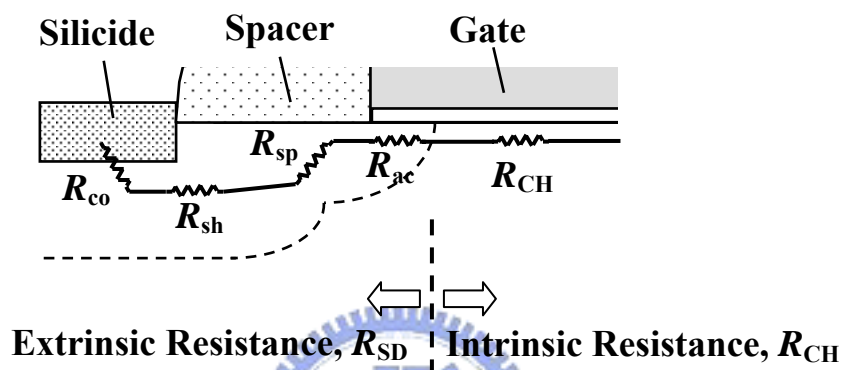
Fig. 4.1. Schematic view showing the extrinsic S/D parasitic resistance (R_{SD}) and intrinsic channel resistance (R_{CH}) of a MOSFET, where the R_{SD} generally is composed of the four components, i.e., the accumulation layer resistance (R_{ac}), the spreading resistance (R_{sp}), the sheet resistance (R_{sh}), and the contact resistance (R_{co}), as defined in [4.12].

Table 4.1. Summary of essential equations correlating the low-field channel mobility gain ($\Delta\mu$), linear drain current gain (ΔI_{dlin}), and saturation drain current gain (ΔI_{dsat}) of process-strained Si (PSS) MOSFETs. Several key indexes employed in the equations are also defined.

Definitions of R_{TOTAL} & I_{dlin} [4.2]

$$R_{\text{TOTAL}} = V_{\text{D}}/I_{\text{dlin}} = R_{\text{CH}} + R_{\text{SD}} \quad\cdots\cdots\cdots\cdots\cdots\cdots\cdots (4.1)$$

$$I_{\text{dlin}} = W\mu Q_{\text{inv}}\left(V_{\text{D}} - I_{\text{dlin}}R_{\text{SD}}\right)/L = \left(V_{\text{D}} - I_{\text{dlin}}R_{\text{SD}}\right)/R_{\text{CH}} \quad\cdots\cdots (4.2)$$

ΔI_{dlin} vs. $\Delta\mu$, from (4.1) & (4.2)

$$\Delta I_{\text{dlin}} = \frac{\Delta\mu}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}} + \frac{\left(R_{\text{SD,PSS}}/R_{\text{CH,PSS}}\right)\Delta R_{\text{SD}}}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}} \quad\cdots\cdots\cdots (4.6)$$

$$= \frac{R_{\text{CH,PSS}}}{R_{\text{TOTAL,PSS}}}\Delta\mu + \frac{R_{\text{SD,PSS}}}{R_{\text{TOTAL,PSS}}}\Delta R_{\text{SD}} \quad\cdots\cdots\cdots\cdots\cdots (4.6')$$

where $\Delta R_{\text{SD}} = \left(R_{\text{SD,Ctrl}} - R_{\text{SD,PSS}}\right)/R_{\text{SD,PSS}}$

ΔI_{dsat} vs. $\Delta\mu$, adapted from [4.18]

$$\Delta I_{\text{dsat}} = \left(1 - B_{\text{sat0,PSS}}\right)\Delta\mu + k\Delta R_{\text{SD}} \quad\cdots\cdots\cdots\cdots\cdots (4.8)$$

k : parameter, ≤ 1

ΔI_{dlin} vs. ΔI_{dsat}, from (4.6) & (4.8)

$$\Delta I_{\text{dlin}} = \frac{\Delta I_{\text{dsat}}}{\left(1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\right)\left(1 - B_{\text{sat0,PSS}}\right)} + \frac{\dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\left(1 - B_{\text{sat0,PSS}}\right) - k}{\left(1 + \dfrac{R_{\text{SD,PSS}}}{R_{\text{CH,PSS}}}\right)\left(1 - B_{\text{sat0,PSS}}\right)}\Delta R_{\text{SD}} \quad\cdots (4.9)$$

Derivative of ΔI_{dlin} to $\Delta\mu$

$$\frac{\partial\left(\Delta I_{\text{dlin}}\right)}{\partial\left(\Delta\mu\right)} = \frac{1}{1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}} \quad\cdots\cdots\cdots (4.10)$$

Derivative of ΔI_{dsat} to $\Delta\mu$

$$\frac{\partial\left(\Delta I_{\text{dsat}}\right)}{\partial\left(\Delta\mu\right)} = 1 - B_{\text{sat0,PSS}} \quad\cdots\cdots\cdots\cdots\cdots (4.11)$$

Derivative of ΔI_{dlin} to ΔI_{dsat}

$$\frac{\partial\left(\Delta I_{\text{dlin}}\right)}{\partial\left(\Delta I_{\text{dsat}}\right)} = \frac{1}{\left(1 + R_{\text{SD,PSS}}/R_{\text{CH,PSS}}\right)\left(1 - B_{\text{sat0,PSS}}\right)} \quad\cdots (4.12)$$

Key indexes

$R_{\text{SD,PSS}}/R_{\text{CH,PSS}}$: evaluate both $\Delta\mu$-to-ΔI_{dlin} and ΔR_{SD}-to-ΔI_{dlin} translating efficiency

$R_{\text{CH,PSS}}/R_{\text{TOTAL,PSS}}$: evaluate ΔI_{dlin}-to-$\Delta\mu$ sensitivity

$R_{\text{SD,PSS}}/R_{\text{TOTAL,PSS}}$: evaluate ΔR_{SD}-to-ΔI_{dlin} translating efficiency

$B_{\text{sat0,PSS}}$: evaluate ΔI_{dsat}-to-$\Delta\mu$ sensitivity

k: evaluate ΔR_{SD}-to-ΔI_{dsat} translating efficiency

W, L & Q_{inv}: Channel width, length, and inversion charge density

R_{TOTAL}, R_{CH} & R_{SD}: Total, channel, and S/D parasitic resistance

B_{sat0}: Nondegenerate ballistic efficiency

The subscripts "PSS" and "Ctrl" denote strained and control MOSFETs, respectively.

$$\left(\alpha\right) = \frac{\Delta I_{dsat}}{I_{dsat}\Delta T} = \frac{I_{dsat1} - I_{dsat2}}{I_{dsat2}(T_1 - T_2)}$$

$$\left(\eta\right) = \frac{\Delta V_{T,sat}}{\Delta T} = \frac{V_{T,sat1} - V_{T,sat2}}{T_1 - T_2}$$

$$\left(V_{T,sat}\right) = V_{Tlin}(G_{m,max}) + \Delta V_{DIBL}(const. I_d)$$

$$\left(\lambda_0/l_0\right) = \frac{4}{0.5 - \left(\alpha + \frac{\eta}{V_G - V_{T,sat}}\right)T} - 2$$

$$\left(r_{sat0}\right) = \frac{1}{1 + \lambda_0/l_0}$$

$$B_{sat0} = \frac{1 - r_{sat0}}{1 + r_{sat0}}$$

$$\text{Fitting slope of } \Delta I_{dlin} \text{ vs. } \Delta I_{dsat} = \frac{\partial(\Delta I_{dlin})}{\partial(\Delta I_{dsat})}$$

$$R_{SD}\text{-to-}R_{CH} = \frac{1}{(1 - B_{sat})\frac{\partial(\Delta I_{dlin})}{\partial(\Delta I_{dsat})}} - 1$$
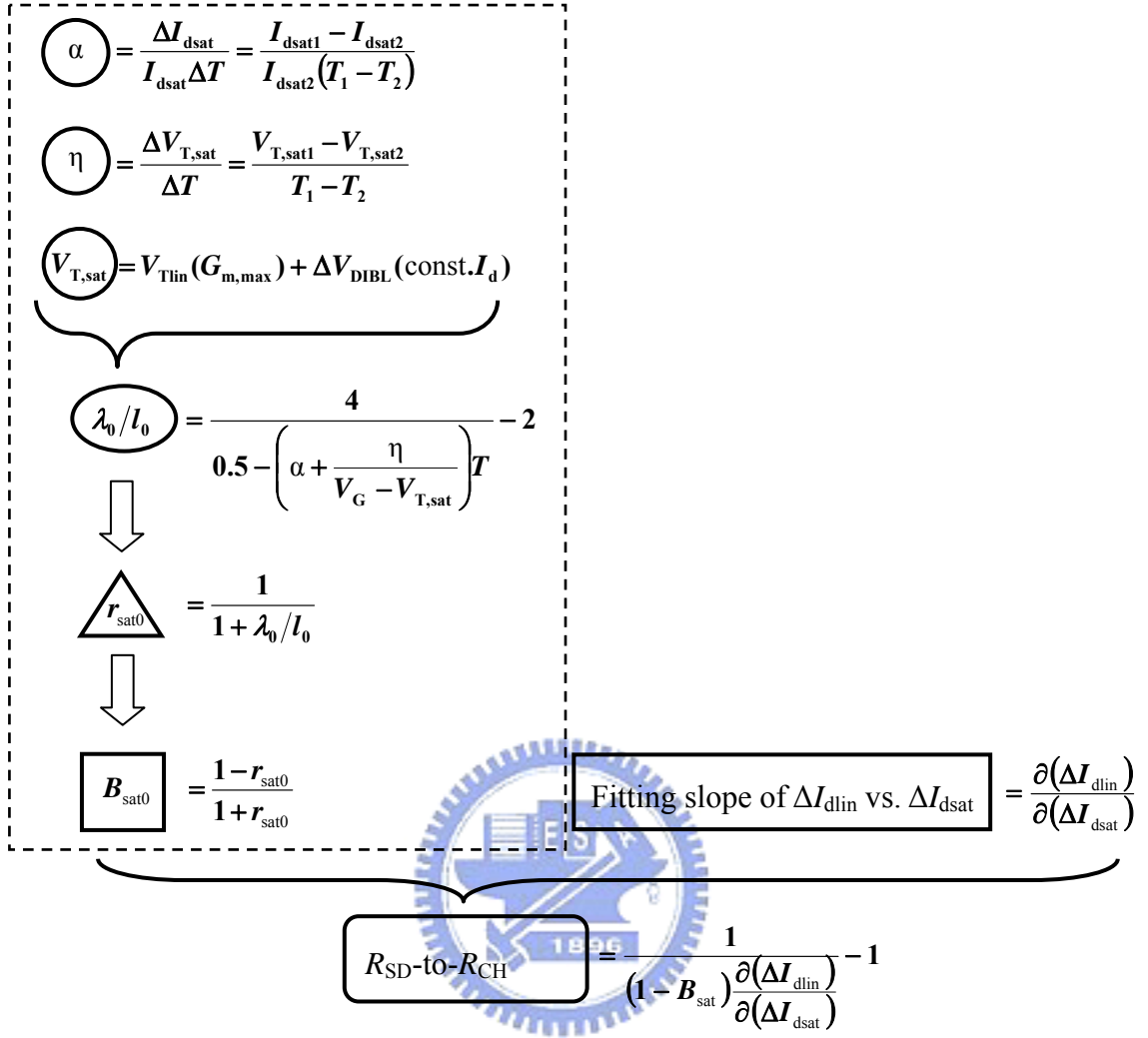
Fig. 4.2. Flow chart of the proposed methodology to extract the ratio of S/D parasitic resistance (R_{SD}) to channel resistance (R_{CH}) for nanoscale strained MOSFETs where the formula of each item is shown next to the corresponding pattern [4.24]. The flow of extracting ballistic efficiency (B_{sat0}), as mentioned in Chapter 2, is shown in the left part enclosed by the dash line, where α and η represent the temperature coefficients of saturation drain current (I_{dsat}) and threshold voltage ($V_{T,sat}$), respectively. $V_{T,sat}$ is determined by maximum-transconductance ($G_{m,max}$) method with drain-induced barrier lowering (DIBL, ΔV_{DIBL}) consideration. Extracting α, η and $V_{T,sat}$, we can calculate the ratio of channel backscattering mean-free-path (λ_0) to $k_B T$ layer thickness (l_0), channel backscattering ratio (r_{sat0}) and B_{sat0}, according to the definitions. Combining B_{sat0} and fitting slope of ΔI_{dlin} versus ΔI_{dsat}, we can obtain the R_{SD}-to-R_{CH} ratio. Then, the R_{SD} of nanoscale strained MOSFETs can be easily found by substituting the R_{SD}-to-R_{CH} ratio into (4.1).