Chapter 5

Correlating Drain Current with Strain-Induced Channel Mobility of Process-Strained Si (PSS) CMOSFETs

5.1 Introduction

Presently, process-induced strain techniques have been successfully integrated into CMOS process for improving device performance and operation speed of integrated circuit (IC) [5.1]–[5.4]. The profound adoption of process-strained techniques in industry, such as shallow trench isolation (STI) [5.5]–[5.7], embedding SiGe [5.1]–[5.3] or SiC [5.8] epitaxy in source/drain (S/D) regions, stress memorization technique [5.9]–[5.11], fully silicided (FUSI) metal gate [5.12]–[5.14], silicide in S/D regions [5.15], SiN contact-etch-stop-layer (CESL) [5.16]–[5.20], and so on, stems from the following advantages. Firstly, slightly changing a few steps in CMOS process is compatible with silicon-based ULSI process and beneficial to reduce the manufacturing cost. Secondly, as compared with substrate-strained techniques having global strain, such as biaxially strained Si on SiGe substrate [5.21][5.22], process-strained techniques exhibiting local strain are more effective in boosting the performance in state-of-the-art CMOS technologies since process-induced local strain significantly increases with device dimension scaling, while substrate-induced global strain decreases. Lastly, at high vertical electric field appreciable channel mobility gain can still be maintained for process-strained techniques but drastically diminishes for substrate-strained cases [5.23]. The deteriorated channel mobility gain is due to the fact that the quantized surface potential reduces the band separation, where mobility gains of substrate-strained techniques mainly arise from reduced intervalley scattering (i.e., increased band

separation). For process-strained techniques, thanks to band warping and carrier repopulation resulting in significant reduction of carrier effective mass, considerable mobility gain can persist not only at high field but also be achievable at low strain [5.23]. Large mobility improvement at low strain is critical owing to dislocation generation at high strain producing yield loss and integration issues [5.24].

Indeed, the process-strained technique has been considered as the most promising candidate for boosting device performance in industry without sacrificing huge process cost. Here, to evaluate the feasibilities of various strained techniques on CMOS manufacturing, drain current and carrier mobility are generally used as criteria. However, as the channel length aggressively scales down, the distribution of electrostatic field is different from that in long channel devices, and forces carrier transport to be off-equilibrium, causing carrier channel backscattering [5.25]–[5.27], or velocity overshoot [5.28][5.29]. The off-equilibrium transport becomes more evident to affect device drive current. As a consequence, in order to continuously pursue device performance down to sub-100-nm regime and beyond, investigating carrier transport at both low and high lateral electric field is vital. However, the relationship between low-field channel mobility and high-field carrier transport is not well studied yet. There are some reasons accounting for this situation. The most critical one among these reasons is the difficulty of extracting the low-field channel mobility of nanoscale MOSFETs since some well-known methods still suffer from ambiguous assumption and inaccurate evaluation [5.30]. Constant channel mobility for all dimensions asserted in these methods is not adequate for process-strained MOSFETs. On the other hand, as intrinsic channel resistance decreases and becomes comparable to/or smaller than S/D parasitic resistance, the influence of S/D parasitic resistance on mobility correction becomes more prominent. However, all existing techniques of characterizing S/D parasitic resistance fail for nanoscale devices due to

the assumption of constant mobility for all channel lengths.

In this work, as stated earlier in Chapter 4, we propose a new methodology of evaluating short channel mobility from the fitting slopes of linear drain current gain versus saturation drain current gain, and ballistic efficiency. We can easily extract the ratio of S/D parasitic resistance to channel resistance without involving the above issues. In this chapter, we employ strained CMOSFETs with different process technologies to examine our model and investigate carrier transport behaviour at both low and high lateral electric field.

5.2 Experimental and Electrical Characteristics

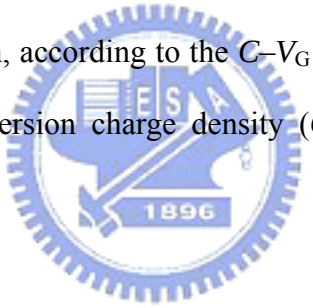
5.2.1 Experimental

A process-strained Si (PSS) technique, as demonstrated in [5.31], was used to achieve the preferred channel strain for nMOSFETs and pMOSFETs, respectively, where the PSS technique includes STI, silicide, SiN CESL, and embedded SiGe S/D. Table 5.1 shows the split of PSS MOSFETs featuring state-of-the-art CMOS Process A (physical gate length $L_{physical}$= 39–124 nm), B ($L_{physical}$= 55–85 nm), and C ($L_{physical}$= 75–125 nm), where the channel strain of PSS nMOSFETs of all processes is primarily achieved by tensile SiN CESL, and that of PSS pMOSFETs of Process A and C is achieved by embedding SiGe S/D, while for PSS pMOSFETs of Process B compressive SiN CESL is used for comparison. Since all PSS devices have wide channel width and nanoscale channel length, it is reasonable to assume that device characteristics are primarily dominated by longitudinal channel stress (along the current direction).

5.2.2 Electrical Characteristics

Figs. 5.1 and 5.2 show drain current (I_d) versus gate voltage (V_G), and drain

current (I_d) versus drain voltage (V_D) characteristics of both control and PSS CMOSFETs of Process A ($L_{physical}$= 39 nm), B ($L_{physical}$= 55 nm), and C ($L_{physical}$= 75 nm). Both the control and PSS MOSFETs exhibit nominally identical subthreshold I_d–V_G characteristics, as indicated by similar threshold voltage (V_T), subthreshold swings, and drain-induced barrier lowerings (DIBLs, as shown in Fig. 5.3) for both control and PSS MOSFETs. So the assumption of the same effective channel length (L_{eff}) and width (W_{eff}) for the control and PSS devices adopted in our method is reasonable. Fig. 5.4 shows the capacitance (C) versus V_G curves in inversion region for the control and PSS CMOSFETs, where the capacitance is normalized with respective to the capacitance of the control device at $|V_G|$= 1 V. The similar C–V_G curves indicate the same capacitance equivalent oxide thickness (CET) for both control and PSS devices. Then, according to the C–V_G and I_d–V_G curves, it is rational to assume the equivalent inversion charge density (Q_{inv}) for the control and PSS devices.



5.2.3 Dependence of Strain-Induced Drain Current on Gate Length

Based on the above electrical characteristics, as shown in Fig. 5.5, we calculate linear drain current gain (ΔI_{dlin}) and saturation drain current gain (ΔI_{dsat}) of PSS MOSFETs, where ΔI_{dlin} and ΔI_{dsat} are defined as $\Delta I_{dlin}= (I_{dlin,PSS} - I_{dlin,Ctrl}) / I_{dlin,Ctrl}$ and $\Delta I_{dsat}= (I_{dsat,PSS} - I_{dsat,Ctrl}) / I_{dsat,Ctrl}$, respectively. Both I_{dlin} (@$|V_D|$= 50 mV) and I_{dsat} (@$|V_D|$= 1 V) are measured at $|V_G - V_T|$= 1 V, where V_T is defined as $|I_d|= 0.1\times W/L$ μA. For PSS nMOSFETs of all processes, ΔI_{dlin} is comparable to/or slightly smaller than ΔI_{dsat}, whereas for PSS pMOSFETs, ΔI_{dlin} is larger than ΔI_{dsat} except for PSS pMOSFETs of Process B. The result indicates that, as compared with the strained technique of SiN-capped CESL, embedding SiGe S/D provides significant I_{dlin} improvement than I_{dsat} gain regardless of process technologies. According to related

studies [5.1]–[5.3], reducing S/D parasitic resistance is a key feature of the strained technique of SiGe S/D, which also induces large uniaxial compressive strain beneficial to raise the drain current. On the other hand, the above result implies that I_{dlin} is more sensitive to series resistance reduction than I_{dsat}, which will be verified later.

Considering the dependence of drain current improvement on $L_{physical}$, we note that both ΔI_{dlin} and ΔI_{dsat} of PSS pMOSFETs gradually deteriorate with $L_{physical}$ scaling, especially for PSS pMOSFETs of Process A. Some reports explain that decreasing current gain may result from increased surface doping concentration [5.16], or non-scaling S/D parasitic resistance [5.23][5.32]. In contrast to PSS pMOSFETs, the drain current gain of PSS nMOSFETs are less dependent on $L_{physical}$ because their S/D parasitic resistance is equal to/or larger than their channel resistance (as demonstrated later in Fig. 5.8.) Therefore, it is speculated that for nMOSFETs, S/D parasitic resistance has limited the advantages of strain engineering in boosting the drive current. Similarly, pMOSFETs will encounter this issue when its drive current is reaching the level as high as that of nMOSFETs.

5.3 Results and Discussion

In this section, we will discuss the correlation between linear drain current gain and low-field channel mobility gain in terms of ratio of S/D parasitic resistance to channel resistance. Similarly, the dependence of saturation drain current gain (at high field) on low-field channel mobility gain is also investigated by ballistic efficiency with regard to the scattering theory. In addition, the dependence of channel mobility and parasitic resistance on drive current is included as well.

5.3.1 Dependence of Ballistic Efficiency on Gate Length

Fig. 5.6 shows the dependence of ballistic efficiency ($B_{sat0,PSS}$) on $L_{physical}$ for PSS CMOSFETs of Process A, B, and C. For all strained processes, as $L_{physical}$ decreases, $B_{sat0,PSS}$ of PSS CMOSFETs increases, which means that carrier transport is closer to ideal ballistic transport limit, i.e., $B_{sat0,PSS}$= 1, where carriers encounter no scattering events from source to drain [5.25]. The behavior of increased $B_{sat0,PSS}$ can be explained as follows. At a given $|V_D|$ (=1 V, in this work), owing to the effect of drain electric field penetrating the channel, shorter-channel devices have larger potential gradient along the channel. Then, the sharper potential profile results in larger DIBL (in Fig. 5.3) and thinner k_BT layer thickness (l_0) [5.33][5.34]. Because $B_{sat0,PSS}$ is inversely proportional to l_0, as shown in Chapter 2, higher $B_{sat0,PSS}$ can be achieved for shorter $L_{physical}$. Here, comparing the $B_{sat0,PSS}$ magnitude of a given $L_{physical}$ between Process A, B, and C, we found that the $B_{sat0,PSS}$ versus $L_{physical}$ curves progressively shift downward, especially for PSS pMOSFETs of Process A, as more advanced process technologies are adopted. Ref. [5.35] reported similar trend from the Monte Carlo simulation. When process technologies are continuously scaled, increasing doping concentration is necessary to keep the short channel effect in check. As a result, larger vertical electric field is generated in the channel surface, which significantly raises carrier surface scattering probability, thus deteriorates carrier scattering mean-free-path (λ_0) and $B_{sat0,PSS}$ (= $1 / [1 + 2l_0 / \lambda_0]$) [5.35].

Here, it is worthy to note that the $B_{sat0,PSS}$ of each process seems to saturate at about 0.5 for minimum $L_{physical}$, where [5.36]–[5.38] also found that the increment of $B_{sat0,PSS}$ gradually diminishes with $L_{physical}$ scaling from experimental extraction or Monte Carlo simulation. From this observation, [5.38] concludes that conventional MOSFETs scaling practices maintain a constant channel backscattering ratio ($r_{sat0,PSS}$), i.e., constant $B_{sat0,PSS}$, regardless of process technologies. In other words, around 0.5 of $B_{sat0,PSS}$ magnitude at nominally minimum $L_{physical}$ will be expected as long as the

well-tempered electrical characteristics of a MOSFET referring to international technology roadmap for semiconductors (ITRS) are targeted, even for more aggressively scaled technologies. Actually, if $L_{physical}$ is scaled down to be smaller than the nominal device dimension of each process technology in this work, further increase in $B_{sat0,PSS}$ is certainly expected and will result in unacceptable short channel behavior.

Here, based on the above observations, two essential physical features are captured. The first one is that only if carrier scattering mean-free-path (λ_0) is much larger than k_BT layer thickness (l_0) (i.e., $\lambda_0 >> l_0$), rather than channel length (i.e., $\lambda_0 >> L$) [5.38], the ballistic transport limit can be attained. Another key point is that, according to (4.7) of Chapter 4, roughly half of low-filed channel mobility gain is contributed toward the saturation drain current improvement for current technology with $B_{sat0,PSS}$ being about 0.5 [5.39].

5.3.2 Correlation between Linear Drain Current Gain and Saturation Drain Current Gain

The dependence of ΔI_{dlin} on ΔI_{dsat} for PSS CMOSFETs of Process A ($L_{physical}$= 39–124 nm), B ($L_{physical}$= 55–85 nm), and C ($L_{physical}$= 75–125 nm) is shown in Fig. 5.7(a). Overall, for PSS nMOSFETs, ΔI_{dlin} is comparable to ΔI_{dsat}, while for PSS pMOSFETs, ΔI_{dlin} is larger than (i.e., roughly two times of) ΔI_{dsat}, which is observed in some studies as well [5.1][5.2][5.16][5.40][5.41]. In Fig. 5.7(a), by linearly fitting a group of devices with nominally identical $L_{physical}$, we show the corresponding fitting slope (i.e., the derivative of ΔI_{dlin} to ΔI_{dsat}) and intercept in Figs. 5.7(b) and 5.7(c), respectively. All PSS CMOSFETs show a decreasing fitting slope with $L_{physical}$ scaling, and at a given $L_{physical}$, PSS pMOSFETs exhibit larger fitting slope than PSS nMOSFETs regardless of process technologies. This phenomenon is attributed to

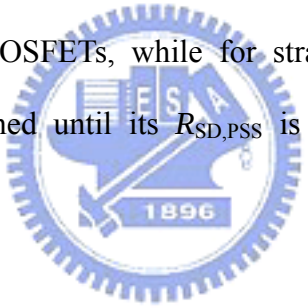
different ratios of S/D parasitic resistance ($R_{SD,PSS}$) to channel resistance ($R_{CH,PSS}$) between PSS nMOSFETs and PSS pMOSFETs (as shown later in Fig. 5.8), where PSS devices have similar $B_{sat0,PSS}$ (being close to 0.5). Then, according to (4.12) of Chapter 4, it is expected that ΔI_{dlin} will be similar to/or smaller than ΔI_{dsat} for PSS nMOSFETs since its $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio is comparable to/or larger than unity [5.2]. Similarly, thanks to the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio being smaller than unity, PSS pMOSFETs have higher ΔI_{dlin} than ΔI_{dsat} [5.1][5.2].

In Fig. 5.7(c), PSS pMOSFETs of Process A and C demonstrate appreciable intercepts, while the other devices have negligible ones at all $L_{physical}$. At zero mobility gain, the positive and non-zero intercept means that drain current improvement totally comes from the reduction of parasitic resistance. According to some studies [5.42][5.43], embedding SiGe in S/D regions is capable of providing an abrupt lateral doping profile and high dopant activation, which reduce the spreading and extension resistances. Furthermore, lower contact resistance of metal-semiconductor interface is attained owing to the smaller bandgap of SiGe.

Relative to the strained technique of embedding SiGe S/D, all PSS MOSFETs with CESL show insignificant intercepts, which is consistent with the results of [5.4][5.17]–[5.20]. According to piezoresistance theory, higher doping level (i.e., comparable to/or larger than 10^{19} cm^{-3}) in S/D regions make the influence of stress on resistance negligible [5.44]. The theoretical calculation of [5.44] was confirmed by experimental characterization of [5.45] as well. Ref. [5.45] found that 0.12% tensile strain merely results in 1.2% decrease of S/D parasitic resistance, where the strain magnitude is presented in terms of the difference of nature lattice constant between Si (a_{Si}= 5.43 Å) and Ge (a_{Ge}= 5.65 Å)). Based on this estimation, about 0.31% strain level induced by CESL in this work only results in 3.1% decrease of S/D parasitic resistance, which confirms the experimental observation.

5.3.3 Ratio of S/D Parasitic Resistance to Channel Resistance

Fig. 5.8 shows the ratio of total S/D parasitic resistance ($R_{SD,PSS}$) to channel resistance ($R_{CH,PSS}$) of PSS CMOSFETs at various $L_{physical}$. For all processes, PSS CMOSFETs reveal similar behavior of gradually increasing $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio with shrinking $L_{physical}$. The combination of non-scaling $R_{SD,PSS}$ and the drastic reduction of strain-induced $R_{CH,PSS}$ accounts for the significantly increasing $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio [5.46][5.47]. It is noted that for PSS nMOSFETs of all processes, the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio is raised to larger than unity, but for PSS pMOSFETs the ratio is still smaller than unity even at minimum $L_{physical}$. It discloses that the S/D parasitic resistance has become a limiting factor in further boosting the drain current of strained nMOSFETs, while for strained pMOSFETs, the current improvement is still maintained until its $R_{SD,PSS}$ is comparable to/or higher than $R_{CH,PSS}$.



5.3.4 Dependence of Strain-Enhanced Channel Mobility on Linear Drain Current Gain and Saturation Drain Current Gain

Fig. 5.9 shows the correlation between $\Delta\mu$, ΔI_{dlin} and ΔI_{dsat} for PSS CMOSFETs of Process A ($L_{physical}$= 39 nm), B ($L_{physical}$= 55 nm) and C ($L_{physical}$= 75 nm), where both I_{dlin} (@$|V_D|$= 50 mV) and I_{dsat} (@$|V_D|$= 1 V) are measured at $|V_G - V_T|$=1 V, and μ (@$|V_D|$= 50 mV, and $|V_G - V_T|$=1 V) is evaluated by (4.2) in Chapter 4 with $R_{SD,PSS}$ correction. The solid line is chosen as the best fitting line of all data. Here, it is worthy to point out that the proposed method of extracting the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio in this work bases on (4.10) and (4.11) in Chapter 4, i.e., the dependences of $\Delta\mu$ on ΔI_{dlin} and ΔI_{dsat}, respectively. Thus, investigating the deviation between experimental fitting slopes and the corresponding parameters is to examine whether these two

dependences are valid or not. In the plot of $\Delta\mu$ versus ΔI_{dlin} (i.e., left parts of Figs. 5.9(a) to 5.9(c)), the value of $(1 + R_{SD,PSS} / R_{CH,PSS})$ from Fig. 5.8 and the deviation of fitting slope relative to $(1 + R_{SD,PSS} / R_{CH,PSS})$ are shown in the left and right parts of parentheses below the fitting slope, respectively. Similarly, in the plot of $\Delta\mu$ versus ΔI_{dsat} (right parts of Figs. 5.9(a) to 5.9(c)), the magnitude of $(1 / [1 - B_{sat0,PSS}])$ from Fig. 5.6 and the corresponding deviation are also shown in the left and right parts of parentheses, respectively. We found that all deviations are smaller than 10%, which provides the evidence of validating these two dependences. Simultaneously, the insignificant deviation verifies the validity of proposed model for nanoscale MOSFETs as well.

Furthermore, in Fig. 5.9, for PSS nMOSFETs of all processes and PSS pMOSFETs of Process B, insignificant intercepts of ΔI_{dlin} and ΔI_{dsat} at zero $\Delta\mu$ are observed, which again justify the argument in Fig. 5.7, i.e., the contribution of ΔR_{SD} to drain current enhancement being insignificant for the strained technique of capping SiN CESL above the gate. For PSS pMOSFETs of Process A and C, the non-zero intercept indicates that the drain current improvement results from the contribution of reduced S/D parasitic resistance due to SiGe S/D. In addition, comparing the magnitude of intercepts of left and right parts in Figs. 5.9(a) and 5.9(c), we note that reducing S/D resistance is more beneficial for I_{dlin} gain than I_{dsat} improvement irrespective of process technologies. This implies that the sensitivities of linear and saturation drain current to resistance reduction are different. This phenomenon will be addressed in the next subsection.

5.3.5 Sensitivities of Linear and Saturation Drain Current to S/D Resistance Reduction

To understand the mechanism responsible for the observation shown in Fig. 5.9,

we extract the translating efficiency of ΔR_{SD} to ΔI_{dlin} and ΔI_{dsat} at various $L_{physical}$, i.e., the ratio of $R_{SD,PSS}$ to total resistance ($R_{TOTAL,PSS}$) and the k factor, according to (4.6′) and (4.8) in Table 4.1, respectively. As shown in Fig. 5.10, we note that both $R_{SD,PSS}$-to-$R_{TOTAL,PSS}$ ratio and k factor progressively increase with reducing $L_{physical}$. Besides, at longer $L_{physical}$ these two factors become similar, while at smaller $L_{physical}$ the variation between these two factors becomes evident. We explain this finding as follows. First, as defined in Chapter 4, the ΔR_{SD} can be rearranged as

$$\Delta R_{SD} = \frac{R_{SD,Ctrl} - R_{SD,PSS}}{R_{SD,PSS}} = \frac{R_{S,Ctrl} + R_{D,Ctrl} - R_{S,PSS} - R_{D,PSS}}{R_{S,PSS} + R_{D,PSS}}, \quad (5.1)$$

where $R_{S,Ctrl}$ (or $R_{S,PSS}$) and $R_{D,Ctrl}$ (or $R_{D,PSS}$), which contribute to the $R_{SD,Ctrl}$ (or $R_{SD,PSS}$), represent the individual parasitic resistance in the source and drain sides, respectively. We define the reduction of source- and drain-side resistances as $\Delta R_S = (R_{S,Ctrl} - R_{S,PSS}) / R_{S,PSS}$, and $\Delta R_D = (R_{D,Ctrl} - R_{D,PSS}) / R_{D,PSS}$, and assume that $R_{S,Ctrl} = R_{D,Ctrl} = 0.5R_{SD,Ctrl}$ (or $R_{S,PSS} = R_{D,PSS} = 0.5R_{SD,PSS}$) [5.48]. Eq. (5.1) can be rearranged as

$$\Delta R_{SD} = \frac{\Delta R_S + \frac{R_{D,Ctrl} - R_{D,PSS}}{R_{S,PSS}}}{1 + \frac{R_{D,PSS}}{R_{S,PSS}}} = \frac{\Delta R_S}{2} + \frac{R_{D,Ctrl} - R_{D,PSS}}{2R_{D,PSS}} = \frac{\Delta R_S + \Delta R_D}{2}. \quad (5.2)$$

Eq. (5.2) reveals that ΔR_{SD} is equal to half of the sum of ΔR_S and ΔR_D, which is only adequate for a MOSFET operating at linear region because low lateral electric field validates the assumption of $R_S = R_D$. However, at saturation region, the electric field is high enough to pinch off the channel region near the drain side, and forces carrier transport to be off-equilibrium, such as velocity overshoot [5.28][5.29], which

invalidates the above assumption as a result of drain-side resistance being smaller than source-side resistance [5.49]. Therefore, we speculate that the reduction of source-side resistance is beneficial for raising both I_{dlin} and I_{dsat} owing to nearly unchanged potential profile near the source side. However, I_{dsat} is less sensitive to the reduction of drain-side resistance than I_{dlin}, which may be ascribed to the off-equilibrium transport behaviour. In addition, the difference between the $R_{SD,PSS}$-to-$R_{TOTAL,PSS}$ ratio and k factor becomes more evident as $L_{physical}$ shrinks. For example, for PSS pMOSFETs of Process A at $L_{physical}$= 124 nm, the translating efficiency of ΔR_D-to-ΔI_{dlin} (6.3%) and ΔR_D-to-ΔI_{dsat} (2.5%) are comparable. As $L_{physical}$ is scaled down to 39 nm, roughly 45% and 27% of the reduction of S/D parasitic resistance are translated into ΔI_{dlin} and ΔI_{dsat}, respectively, which is consistent with the result of [5.50] by process and device simulations.

In Fig. 5.11, we plot the percentage of ΔR_{SD} on ΔI_{dlin} and ΔI_{dsat} at various $L_{physical}$. As $L_{physical}$ scales down, PSS pMOSFETs of both processes show similar behavior, i.e., the drain current gain attributed to the reduction of S/D parasitic resistance gradually increases [5.51], while the ratio of strain-enhanced mobility gain to current performance progressively diminishes [5.52]. As the channel length continuously shrinks down, the position of S/D doping junctions is closer to the channel center, and the influence of R_{SD} on drain current gain becomes more important [5.53]. On the other hand, the overlap of halo doping induces large vertical electric field and more ionized impurity scattering, which deteriorate strain-enhanced channel mobility gain in nanoscale regime [5.54]. This finding is also observed in four-point bending experiment by virtue of externally applying mechanical stress [5.52].

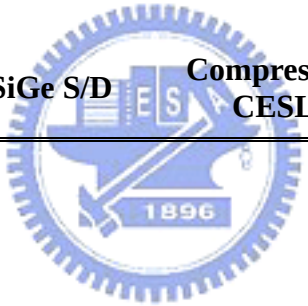
5.4 Conclusions

In this work, we demonstrate a new methodology of extracting S/D parasitic

resistance ($R_{SD,PSS}$) of nanoscale MOSFETs by correlating the low field channel mobility gain ($\Delta\mu$), linear drain current gain (ΔI_{dlin}), and saturation drain current gain (ΔI_{dsat}). Process-strained Si (PSS) CMOSFETs with state-of-the-art process technologies are employed to examine the extraction method. It is found that at the same channel length, ΔI_{dlin} is comparable to ΔI_{dsat} for PSS nMOSFETs, but much higher than ΔI_{dsat} for PSS pMOSFETs. The different ratios of $R_{SD,PSS}$ to channel resistance ($R_{CH,PSS}$) between PSS CMOSFETs having similar ballistic efficiency ($B_{sat0,PSS}$) account for this observation, where both $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio and $B_{sat0,PSS}$ are the key factors in determining the correlation between ΔI_{dlin} and ΔI_{dsat}. Similar $B_{sat0,PSS}$ of 0.5 results in roughly half of strain-enhanced channel mobility being translated into ΔI_{dsat} for both PSS CMOSFETs. On the other hand, due to the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratio of PSS nMOSFETs being close to unity, only half of $\Delta\mu$ is translated into ΔI_{dlin}, while for PSS pMOSFETs, ΔI_{dlin} is slightly less than $\Delta\mu$ owing to the $R_{SD,PSS}$ being smaller than $R_{CH,PSS}$. Furthermore, we also noted that, as $L_{physical}$ aggressively scales down, the enhanced drain current gain attributed to resistance reduction becomes more significant, while the ratio of channel mobility gain to drain current gain progressively deteriorates. It suggests that the engineering of decreasing S/D parasitic resistance plays a more prominent role for maintaining and further boosting the device performance of strained MOSFETs with sub-100-nm process technology and beyond.

Table 5.1. Splits of process-strained Si (PSS) CMOSFETs [5.31] fabricated by different process technologies A, B, and C, where the channel strain of CMOSFETs are primarily achieved by tensile and compressive CESL, and SiGe S/D, respectively.

Strained Techniques	Process A	Process B	Process C
PSS nMOSFETs	Tensile CESL	Tensile CESL	—
PSS pMOSFETs	SiGe S/D	Compressive CESL	SiGe S/D



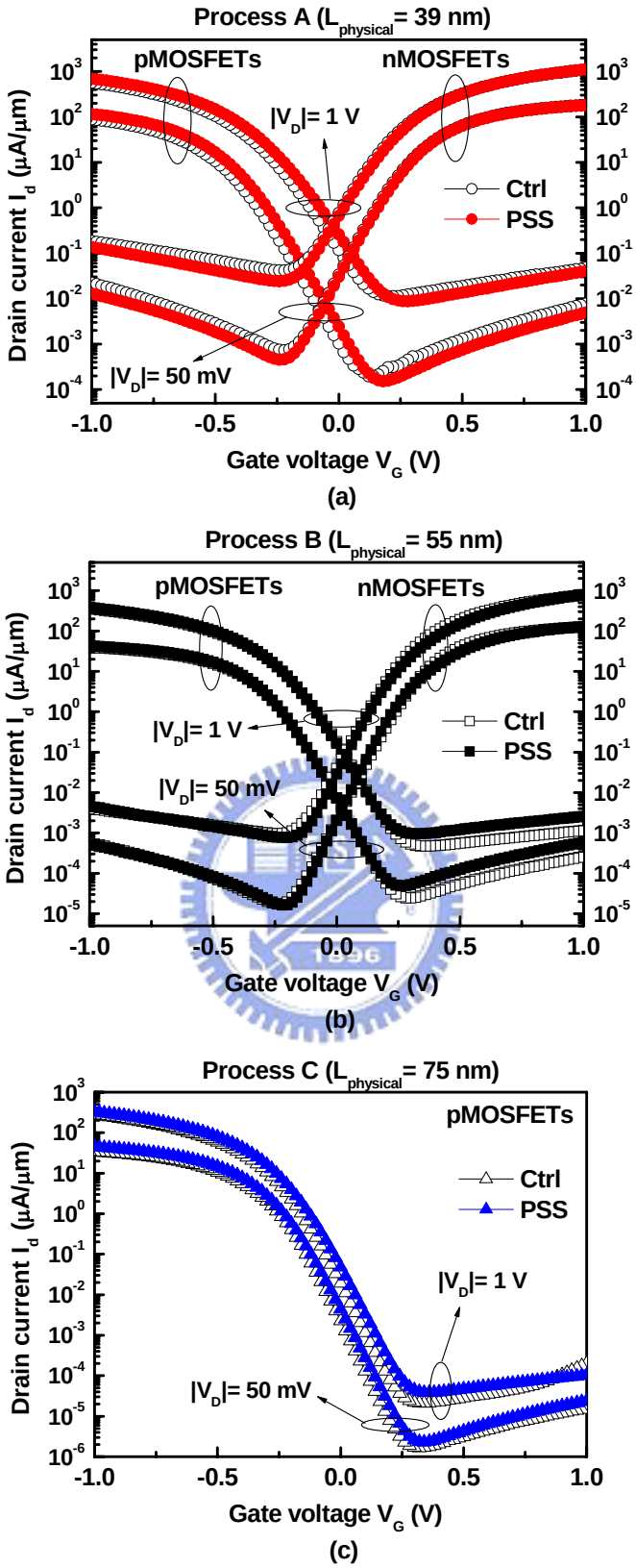


Fig. 5.1. Drain current (I_d) versus gate voltage (V_G) characteristics of PSS and control CMOSFETs of Process (a) A, (b) B, and (c) C.

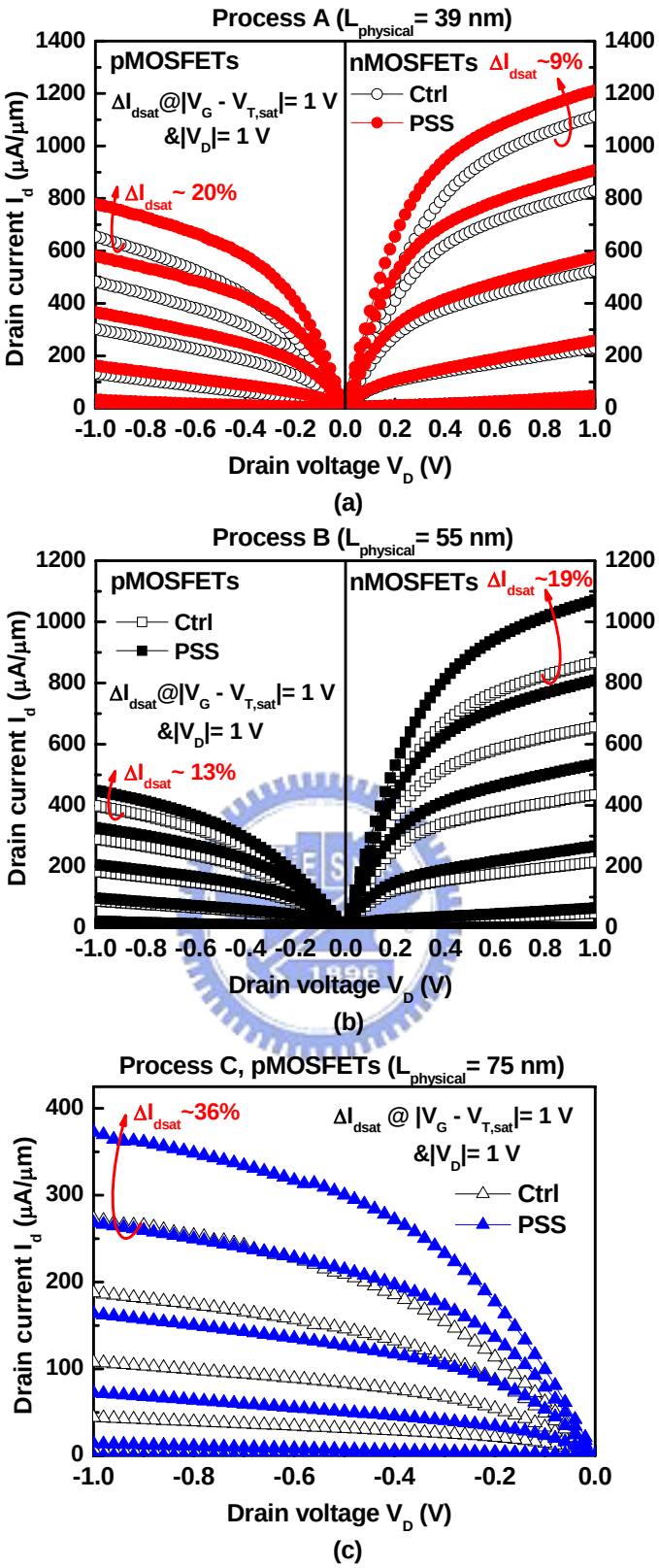


Fig. 5.2. Drain current (I_d) versus drain voltage (V_D) characteristics of PSS and control CMOSFETs of Process (a) A, (b) B, and (c) C. The enhancement of saturation drain current (ΔI_{dsat}) was measured at $|V_G - V_{T,sat}|$= 1 V and $|V_D|$= 1 V, where $V_{T,sat}$ represents the threshold voltage at saturation region.

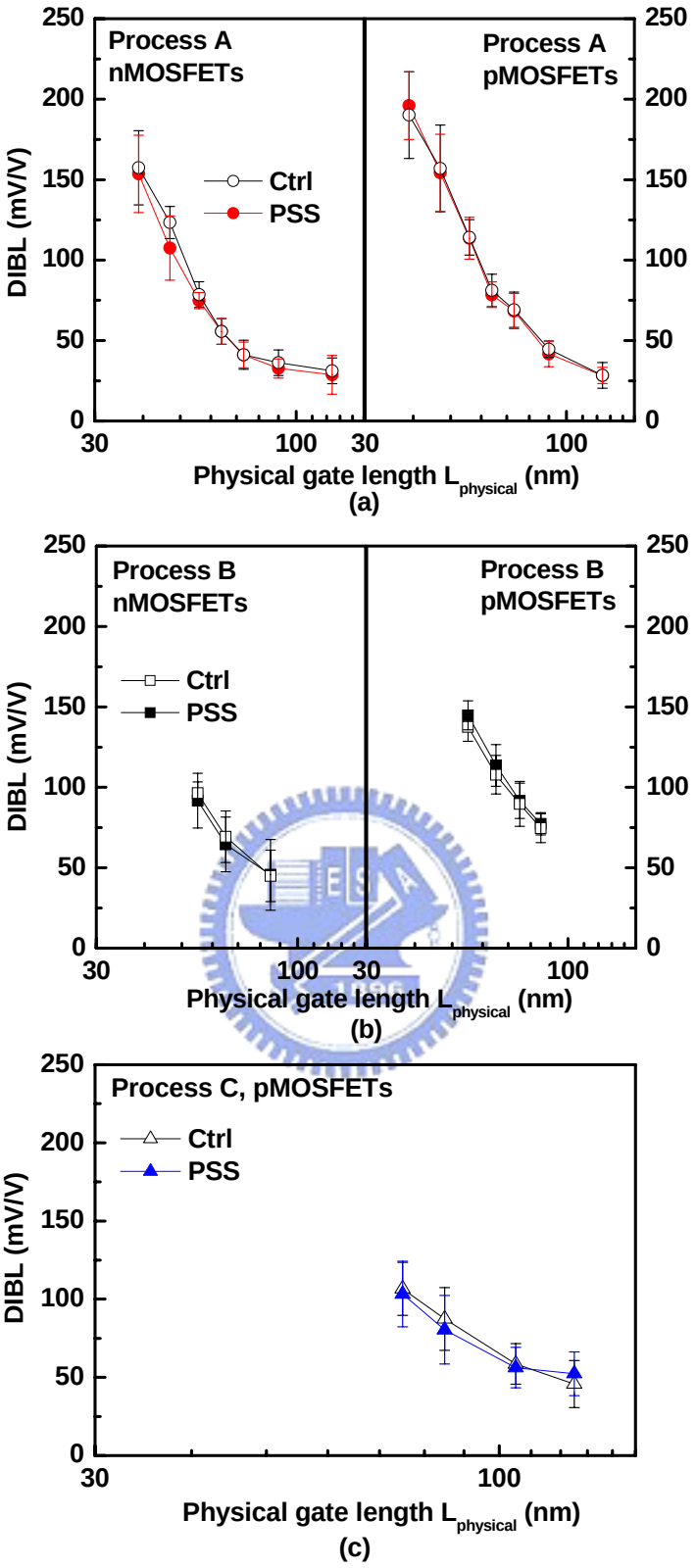


Fig. 5.3. Comparisons of DIBLs between PSS and control CMOSFETs of Process (a) A, (b) B, and (c) C at various physical gate lengths ($L_{physical}$). For all $L_{physical}$, PSS MOSFETs depict similar DIBL as control devices.

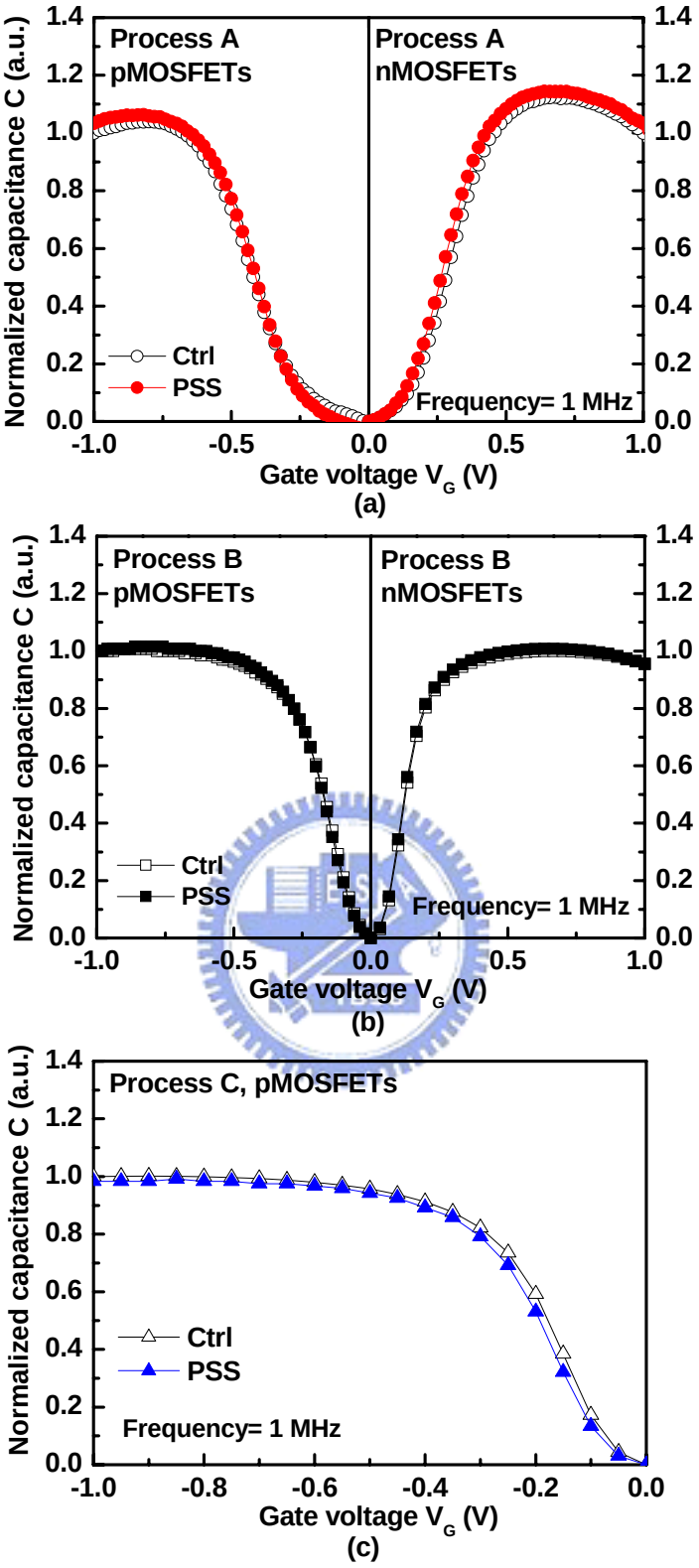


Fig. 5.4. Inversion capacitance (C) versus gate voltage (V_G) characteristics for control and PSS CMOSFETs of Process (a) A, (b) B, and (c) C. The capacitance is normalized with respect to the capacitance of the control at $|V_G|$= 1 V.

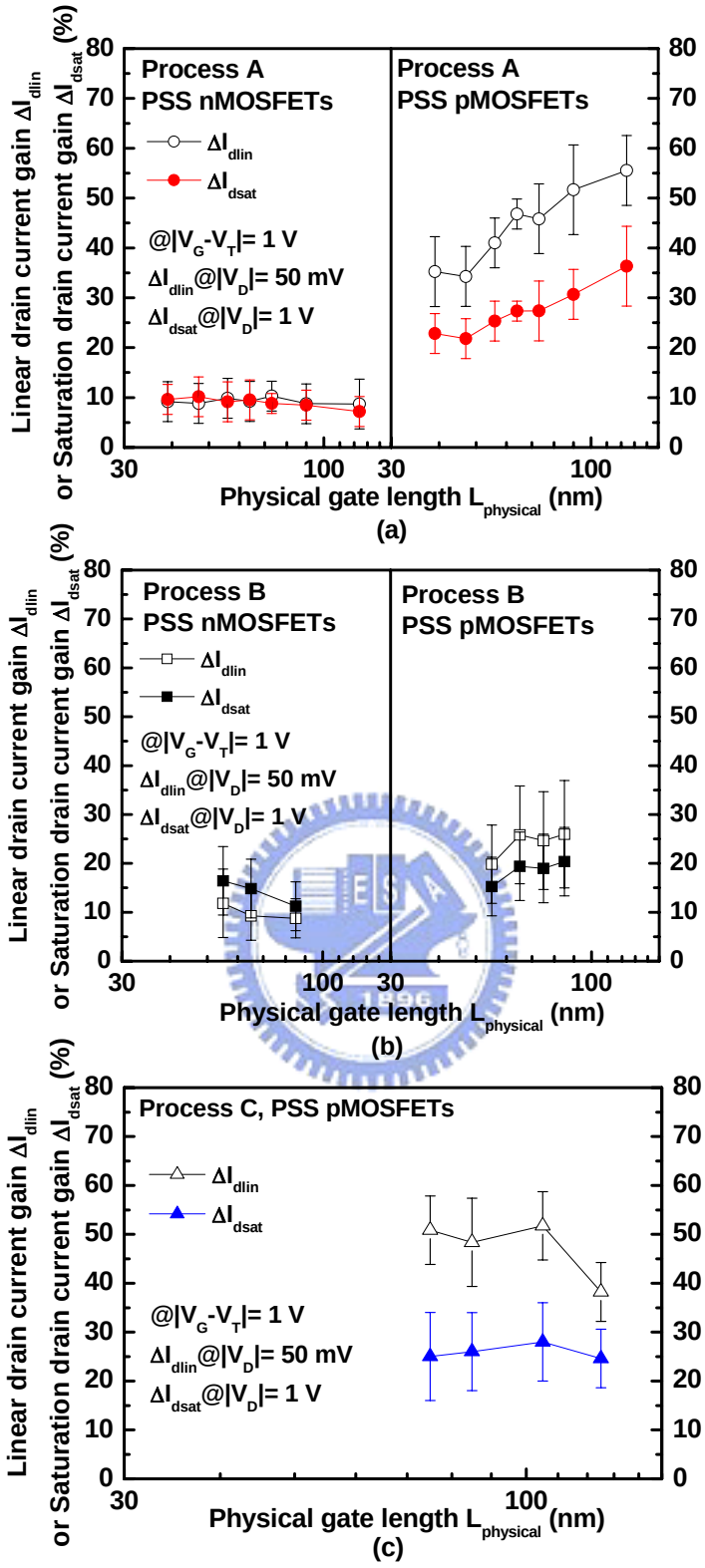


Fig. 5.5. Dependence of linear drain current gain (ΔI_{dlin}) and saturation drain current gain (ΔI_{dsat}) on $L_{physical}$ of PSS CMOSFETs of Process (a) A, (b) B, and (c) C, where ΔI_{dlin} and ΔI_{dsat} are defined as $\Delta I_{dlin}= (I_{dlin,PSS} - I_{dlin,Ctrl}) / I_{dlin,Ctrl}$, and $\Delta I_{dsat}= (I_{dsat,PSS} - I_{dsat,Ctrl}) / I_{dsat,Ctrl}$. It is noted that ΔI_{dlin} is comparable to ΔI_{dsat} for all PSS nMOSFETs but much higher than ΔI_{dsat} for PSS pMOSFETs except Process B.

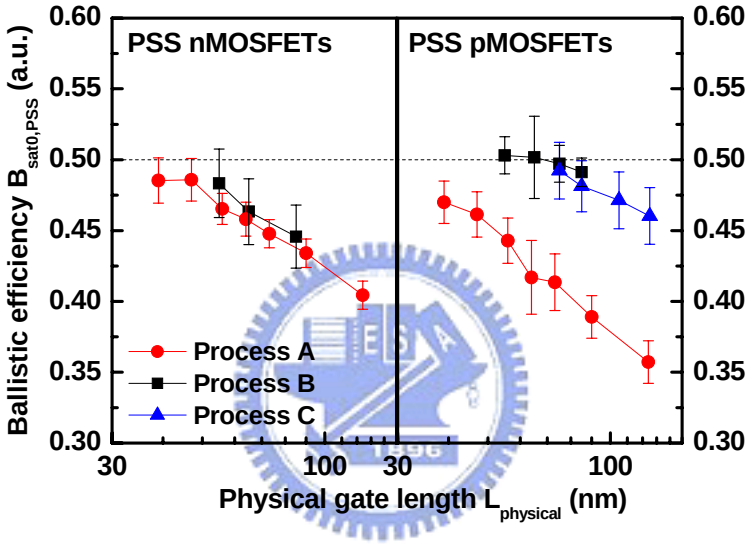


Fig. 5.6. Dependence of ballistic efficiency ($B_{sat0,PSS}$) on $L_{physical}$ for PSS CMOSFETs of Process A, B, and C. Irrespective of process technologies, the $B_{sat0,PSS}$ of all PSS MOSFETs increases with $L_{physical}$ scaling, which indicates that carrier transport is closer to ballistic transport regime, i.e., $B_{sat0,PSS}$= 1, where carriers encounter no scattering events from source to drain.

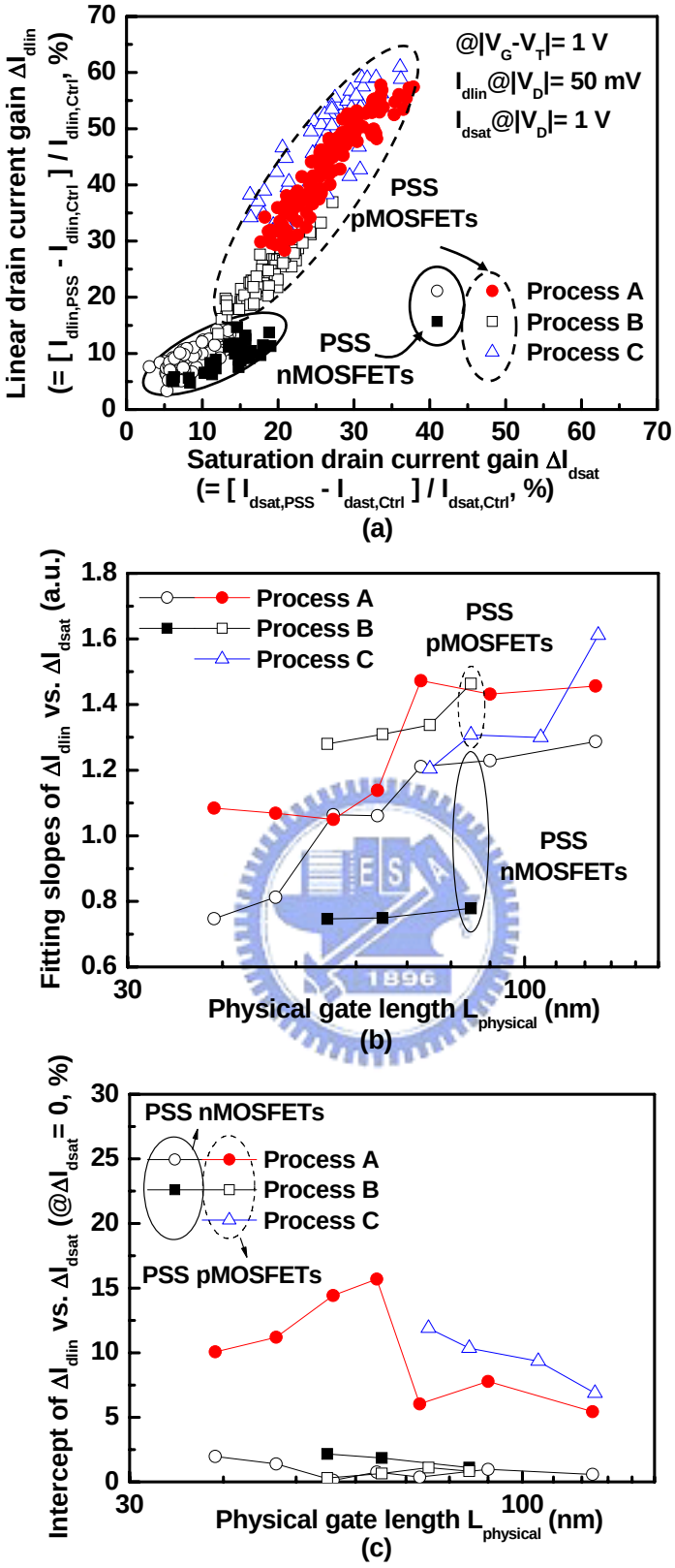


Fig. 5.7. (a) ΔI_{dlin} versus ΔI_{dsat} for PSS CMOSFETs of Process A ($L_{physical}$= 39–124 nm), B ($L_{physical}$= 55–85 nm), and C ($L_{physical}$= 75–125 nm). (b) The best fitting slope, and (c) corresponding intercept, obtained by linearly fitting a group of devices with nominally identical $L_{physical}$.

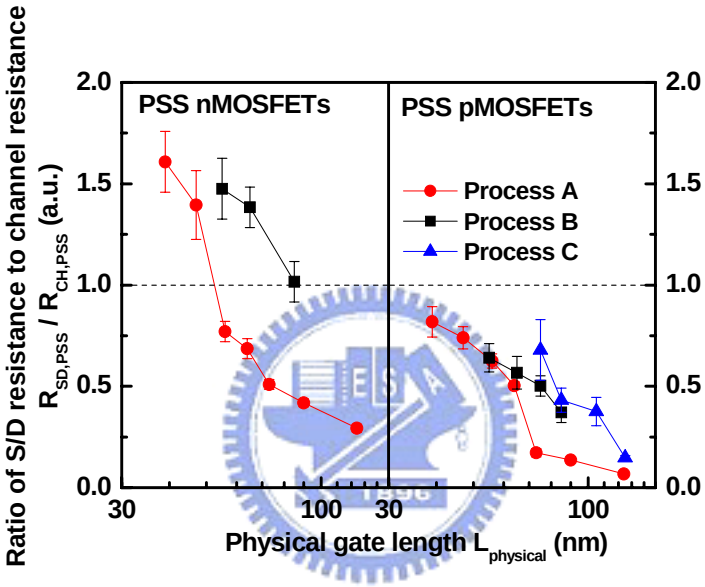


Fig. 5.8. Ratio of S/D parasitic resistance ($R_{SD,PSS}$) to channel resistance ($R_{CH,PSS}$) of PSS CMOSFETs at various $L_{physical}$. It is found that the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratios of all PSS CMOSFETs increase with $L_{physical}$ scaling regardless of process technologies. In addition, the $R_{SD,PSS}$-to-$R_{CH,PSS}$ ratios of PSS nMOSFETs at smaller $L_{physical}$ are higher than unity, while for PSS pMOSFETs the ratios still are smaller than unity.

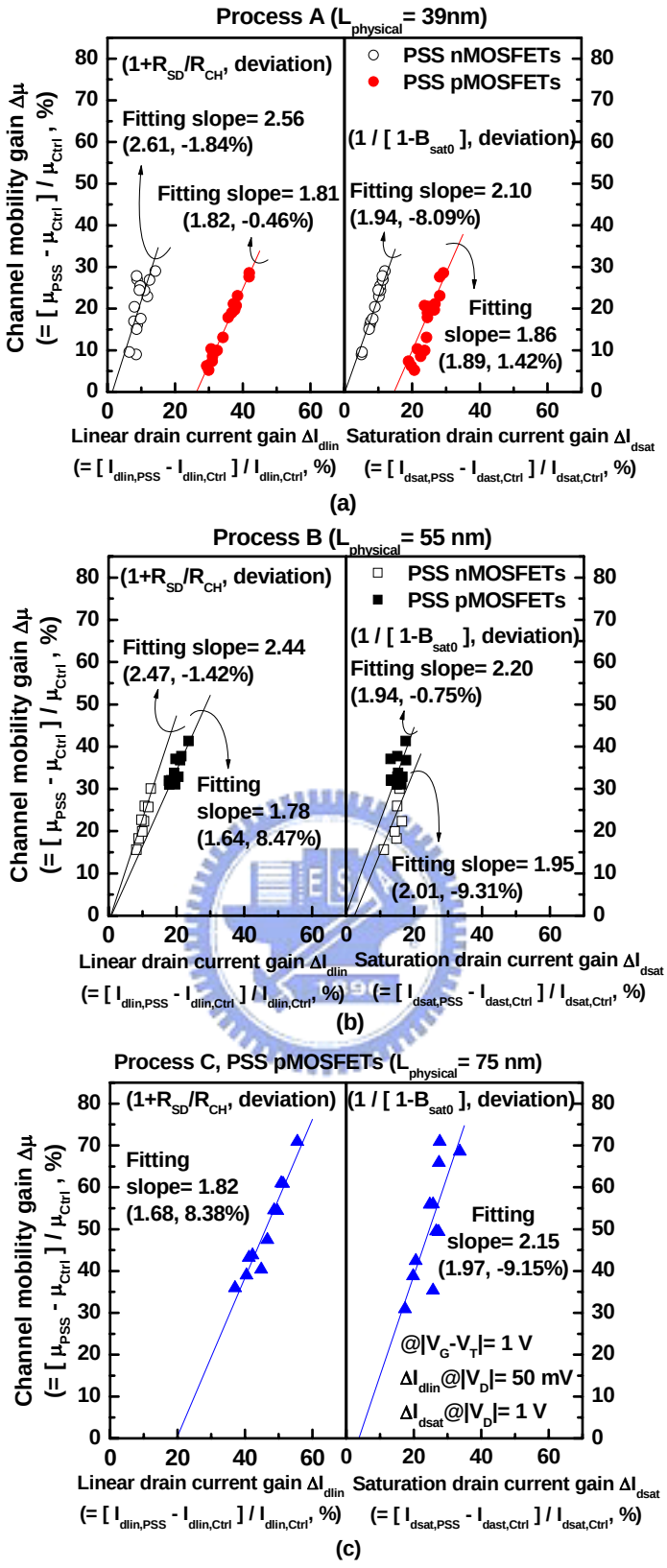


Fig. 5.9. Δμ versus ΔI_{dlin} (left part), and Δμ versus ΔI_{dsat} (right part) for PSS CMOSFETs of Process (a) A, (b) B, and (c) C. The solid line represents the best fitting line. In the left side of parenthesis below the fitting slope is related factors, i.e., $(1 + R_{SD,PSS} / R_{CH,PSS})$ and $(1 / [1 - B_{sat0,PSS}])$ in the left and right figures, respectively. The deviation relative to fitting slope is also shown in the right side of parenthesis.

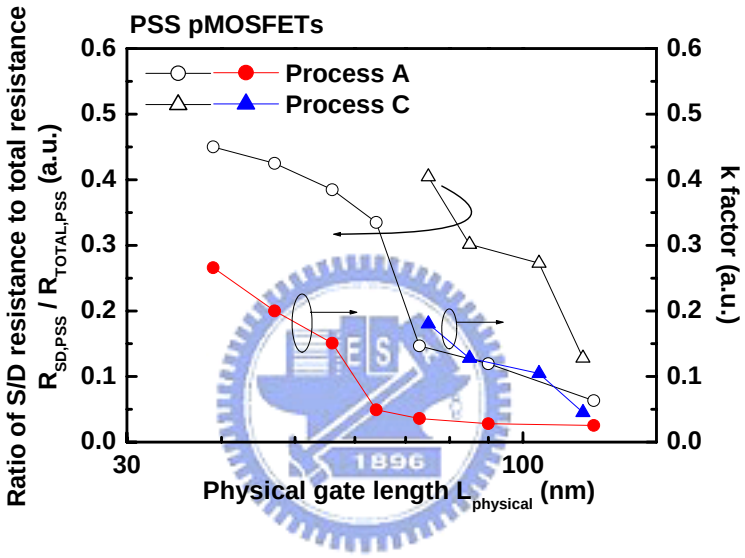


Fig. 5.10. Ratios of S/D parasitic resistance ($R_{SD,PSS}$) to total resistance ($R_{TOTAL,PSS}$) (i.e., ΔI_{dlin}-to-ΔR_{SD} sensitivity) and k factor (i.e., ΔI_{dsat}-to-ΔR_{SD} sensitivity) for PSS pMOSFETs of Process A and C. Both factors increase with $L_{physical}$ scaling. It is also noted that the $R_{SD,PSS}$-to-$R_{TOTAL,PSS}$ ratio is roughly two times of k factor, which suggests R_{SD} reduction of SiGe S/D is more beneficial to I_{dlin} improvement than I_{dsat} gain.

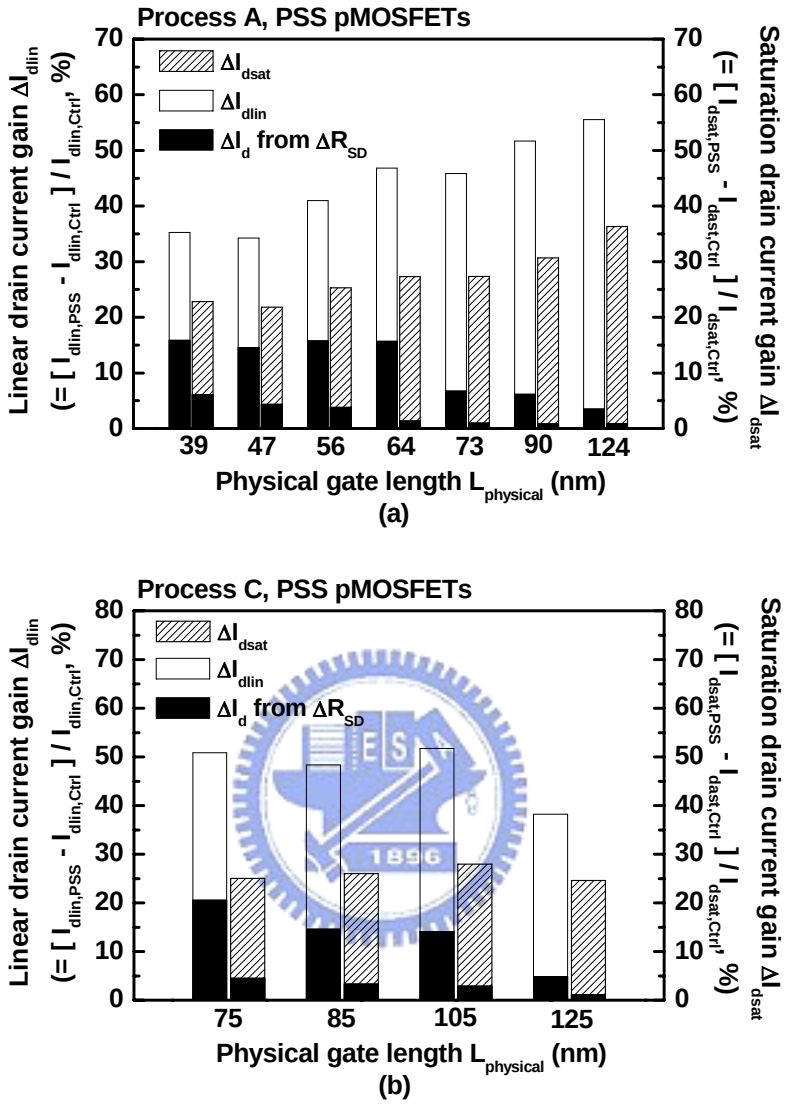


Fig. 5.11. Dependence of ΔI_{dlin} and ΔI_{dsat} on $L_{physical}$ for PSS pMOSFETs of Process (a) A, and (b) C. The filled region of each column represents the drain current gain entirely attributed to the reduction of $L_{physical}$. It is noted that the contribution of reduced R_{SD} to both I_{dlin} and I_{dsat} increases with $L_{physical}$ scaling.