Chapter 6

Negative Bias Temperature Instability (NBTI) of Process-Strained Si (PSS) pMOSFETs

6.1 Introduction

The implementation of mechanical stress in MOSFET channel region has attracted a lot of interest in CMOS manufacturing because of the significant enhancement of drive current and circuit operation speed. Various strained techniques for inducing channel stress have been reported for further boosting the performance of CMOS as channel length is aggressively scaled down to nanometer regime [6.1]–[6.5]. Improvements in channel mobility and drain current are considered as important performance indices for evaluating the feasibility of a strain technique in CMOS fabrication. However, few reports addressed the impact of channel stress on device reliability and/or gate dielectric integrity, such as hot carrier injection (HCI) [6.6][6.7], negative bias temperature instability (NBTI) [6.8], time dependent dielectric breakdown (TDDB) [6.9], and so on. Among these issues, NBTI-induced degradation has become a critical reliability concern for pMOSFETs as gate oxide is aggressively scaling down [6.10]–[6.12]. Thus, to maintain the strain benefit of boosting device performance without deteriorating the device reliability, it is vital to investigate the effect of channel stress on device reliability.

In this chapter, we will focus on the study of NBTI for strained pMOSFETs. NBTI occurs in a MOSFET stressed with negative gate voltage (V_G) at elevated temperature (T), where all other terminals of a MOSFET (source, drain, and substrate) are electrically grounded. Typical stress temperatures of NBTI lie in the temperature range between 100 and 250℃ with oxide electric fields typically below 6 MV/cm

[6.13]. Elevated temperature or oxide electric field alone can deteriorate the gate dielectric integrity, and their combination will accelerate the NBTI-induced degradation, where threshold voltage shift ($\Delta V_{T,BT}$), transconductance change and drain current degradation are usually used as degradation criteria for NBTI. Here, the change of the above parameters is ascribed to the generation of electrically activated oxide traps during NBTI stress, which is generally described by the reaction-diffusion model as follows [6.13][6.14]–[6.17]

$$\text{Reaction}: \ Si_3 \equiv SiH + X \rightarrow Si_3 \equiv Si\bullet + (\text{fixed oxide charge})^+ + Y_{\text{Interface}}, \qquad (6.1a)$$

$$\text{Diffusion}: \ Y_{\text{Interface}} \xleftrightarrow{\text{diffusion}} Y_{\text{Bulk}}, \qquad (6.1b)$$

where (6.1a) and (6.1b) are the reaction and diffusion processes of NBTI degradation, respectively. Firstly, owing to the aid of elevated temperature and oxide electric field, a precursor *X* (e.g., hole-related species [6.13][6.15]) interacts with and breaks Si–H bonds at the Si/SiO_2 interface. After dissociation of Si–H bonds, some oxide defects, including the interface traps [i.e., Si dangling bonds, denoted by Si• in (6.1a)] and positive fixed oxide charges, and byproduct *Y* (e.g., hydrogen-related species [6.14][6.16][6.17]) are generated at the interface. Then, the species *Y* diffuse away from the interface toward the bulk region of gate oxide.

Some models concluded that NBTI-induced degradation is determined by both Si–H bond breaking rate and diffusing rate of species *Y*, where both reaction rates are functions of temperature and oxide electric field [6.18][6.19]. Since the generated Si dangling bonds may be immediately annealed out (or re-passivated) by H-related species *Y*, the mechanism limiting the deterioration rate depends on the stress temperature and gate voltage [6.11]. When the pMOSFET is stressed at 100–250℃

temperature range with low electric field (< 6 MV/cm) [6.13], a typical condition encountered during burn-in and circuit operation, it is found that the dependence of NBTI-induced degradation on stress time (t) will follow a power-law relation with $t^{0.25}$, i.e., $\Delta V_{T,BT} = ct^{0.25}$, where c is a constant [6.14]. The $t^{0.25}$ dependence indicates that NBTI degradation is mainly limited by diffusion process [6.14]. Then, according to the power-law dependence, device lifetime under the defined degradation criteria can be obtained by extrapolating the data measured under severe stress conditions.

However, the extracted device lifetime from unipolar stress voltage (only negative gate voltage, i.e., static NBTI) is generally underestimated and not suitable of predicting the "real" lifetime of devices for real-life circuit operation [6.20]–[6.22]. Because the gate of the pMOSFET in a CMOS inverter is alternately switched between positive and negative bias, the negative bias-induced degradation (i.e., stress cycles) will be partially recovered as the gate is under positive gate bias (i.e., relax cycles), which results in less degradation than static NBTI. Although dynamic NBTI (including both stress and relax cycles) exhibits the recovery behaviour, the degradation is temporarily recovered and keeps increasing when relax cycles are removed and stress cycles are applied.

In this work, we will study the effect of channel stress on NBTI for pMOSFETs with different channel stresses. The NBTI-induced threshold voltage shift ($\Delta V_{T,BT}$) and projected device lifetime will be employed to evaluate the degradation under static and dynamic NBTI. Moreover, the mechanisms responsible for recovery behaviour of dynamic NBTI and worsen degradation due to higher channel stress will be discussed as well.

6.2 Experimental and Electrical Characteristics

Here, we will briefly introduce the process-strained Si (PSS) technique employed

in this work and the experiment for negative-bias temperature instability (NBTI) investigation. Before NBTI stress, the pre-stressed transfer characteristics, the drain current gain and gate oxide integrity of PSS pMOSFETs will be characterized.

6.2.1 Experimental

Devices used in this work were strained pMOSFETs with 1.6 nm nitrided oxide (SiON) as the gate dielectric, where channel stress is induced by the process-strained Si (PSS) technique, as shown in Fig. 6.1 [6.5]. The PSS technique engineers channel stress through CMOS processes, such as shallow trench isolation (STI), silicide, contact etch stop layer (CESL), and so on. According to experimental results [6.5] and theoretical calculation [6.23], the PSS-induced current change can be modeled as a linear function of the three-dimensional (3D) strain components. That is, independently modulating the strain component in each direction (*x*-, *y*-, *z*-axis) changes the drain current of the PSS MOSFET, where *x*-, *y*-, *z*-axis refer to channel current direction, channel width direction, and the direction normal to Si/SiO_2 interface. According to the results of 3D strain engineering [6.5][6.23], decreased compressive strain in *y*-axis direction is beneficial for current improvement of both nMOSFETs and pMOSFETs. Addressing PSS pMOSFETs in this work, we mainly modulated the STI process to achieve higher compressive stress (HS) and lower compressive stress (LS) in *y*-axis direction, where PSS_HS split adopted standard STI processes. Fig. 6.2 shows the simulated stress profile of PSS_HS and PSS_LS pMOSFETs, where the channel stress of PSS_HS split is about –520 MPa (minus sign denotes compressive stress) but decreases to –220 MPa for PSS_LS split.

6.2.2 Pre-Stressed Transfer Characteristics and Gate Oxide Integrity

Before electrically stressing PSS pMOSFETs at high temperature (*T*) and

negative gate voltage (V_G), we measured transfer characteristics (I_d–V_G), drain current gain, and gate oxide integrity. As shown in Fig. 6.3(a), PSS_HS and PSS_LS pMOSFETs with mask gate length (L_{Mask}) of 0.13 μm exhibit almost identical subthreshold transfer curves (I_d–V_G), which suggest similar threshold voltage (V_T), subthreshold swing (S), and drain-induced barrier lowering (DIBL) for both PSS splits. In addition, nominally identical, pre-stressed electrical characteristics between these two splits justify that the difference of NBTI-induced parameter degradation is ascribed to the effect of channel stress. In Fig. 6.3(b), it is found that at a given off-current (I_{off}), PSS_LS split shows about 5% gain of on-current (I_{on}) relative to PSS_HS split, which reveals that a lower compressive stress in y-axis is achieved for PSS_LS split through 3D strain engineering [6.5].

Besides similar subthreshold I_d–V_G curves, as shown in Figs. 6.4(a)–6.4(c), PSS_HS and PSS_LS pMOSFETs also show essentially identical capacitance-voltage (C–V_G) curves, gate leakage current ($|J_G|$), and gate dielectric breakdown voltage ($|V_{BD}|$), which suggests that both PSS splits have identical capacitance equivalent thickness (CET) and gate oxide integrity (e.g., similar interface trap density) before NBTI stress. Nevertheless, some previous works reported that: 1) externally applying mechanical compressive stress to MOS capacitors induces about 1.5% degradation of depletion-layer capacitance, as compared with the unstrained case, since strain-induced band splitting changes the density-of-state (DOS) effective mass [6.24]; 2) applying tensile mechanical stress perpendicular to the current direction increases around 2% of gate leakage current for short-channel pMOSFETs, which stems from decreased barrier height between the channel and gate dielectric and increased carrier tunnelling probabilities [6.25]; 3) aggravated degradation in time dependent dielectric breakdown (TDDB) for scaled MOSFETs is caused by STI-induced compressive stress because the interaction of mechanical stress and hydrogen species becomes

more evident for small-dimension devices [6.9]. The above results were not found in this work, presumably due to different experimental and process conditions. On the other hand, strictly speaking, process-to-process and/or die-to-die variations of device parameters probably could account for the 2% modulation as stated above.

6.3 Static Negative Bias Temperature Instability (SNBTI)

To explore the impact of channel stress on NBTI, we electrically stressed PSS_HS and PSS_LS pMOSFETs with different temperatures and large negative gate voltage. The NBTI-induced threshold voltage shift and projected device lifetime are used to evaluate the extent of degradation. And the effect of different channel widths and lateral lengths of active region on static NBTI is investigated as well.

6.3.1 Dependence of NBTI-Induced Degradation on Active Region Dimensions

Figs. 6.5(a) and 6.5(b) show the dependence of NBTI-induced V_T shift ($\Delta V_{T,BT}$) on different channel widths (W) of pMOSFETs with the same physical gate length ($L_{physical}$= 90 nm), and different lateral lengths of active region with symmetric source/drain (S/D) layout, respectively, where the static NBTI is performed at V_G= –2.4V, T= 150℃, and stress time t= 1000s. The V_T is defined as the gate voltage at I_d= 0.1×W/L μA. By taking the error bars into consideration, it is noted that both PSS splits depict comparable $\Delta V_{T,BT}$ for all channel widths and lateral lengths of active region, which implies that NBTI is insensitive to the channel stress level in this work. According to the electrical bias configuration of NBTI, it is reasonable to expect that NBTI-induced degradation due to vertical oxide electric field should not have any dependence on device dimensions [6.13][6.26]. However, some process issues and device structures, e.g., boron diffusion into the channel [6.27] and channel stress distribution [6.7][6.8][6.28][6.29], will cause larger NBTI degradation for

small-dimension devices. It has been reported that STI-induced drain current gain of pMOSFETs increases with decreasing channel width because of noticeably reduced compressive strain in *y*-axis [6.5]. Moreover, the channel stress to the gate oxide modulates the bond length and angle of Si–H bonds [6.28], and in turn decreases its bonding energy, which generates excess interface oxide traps and larger NBTI degradation [6.7][6.8][6.29]. Here, the independence of $\Delta V_{T,BT}$ on active region dimensions for both PSS splits may be attributed to insignificant modulation of channel stress with varying device dimensions. Furthermore, comparable $\Delta V_{T,BT}$ between the two PSS splits may result from small channel stress difference (by only 5% current gain) and/or the BT stress conditions. When the BT stress is applied under severer conditions or for a longer time, the story may be different (PSS_HS split shows severer NBTI behaviour, which will be shown later) [6.30][6.31].

6.3.2 Influence of Channel Stress on NBTI-Induced Degradation

Fig. 6.6(a) shows the NBTI-induced V_T shifts ($\Delta V_{T,BT}$) of PSS_HS and PSS_LS pMOSFETs ($L_{physical}$= 110nm) at V_G= –2.4V and different temperatures (T= 75, 100, 125, 150℃). It is noted that for lower stress temperatures (T= 75 and 100℃), the $\Delta V_{T,BT}$ of both PSS splits are comparable with each other, while for higher stress temperatures (T= 125 and 150℃), the deviation of $\Delta V_{T,BT}$ between PSS splits gradually widens with increasing stress time. The observation verifies the argument that mechanical stress near the Si/SiO_2 interface deteriorates the gate dielectric integrity since the mechanical stress weakens the bonding energy and induces excess interface traps [6.7][6.9][6.29]. In addition, long-term harsh NBTI stress (i.e., higher temperature and large gate voltage) and/or larger channel stress manifest the impact of channel stress on NBTI behaviour.

Next, we study what mechanisms are responsible for the worse NBTI behaviour

of PSS_HS pMOSFETs. Re-plotting the linear scale of both *x*- and *y*-axis in Fig. 6.6(a) to log scale and fitting the data, we can extract the slopes (i.e., exponent *n*) of various stress temperatures in Fig. 6.6(b), according to the power-law relation of $\Delta V_{T,BT} = ct^n$. All exponents of both PSS splits range from 0.2 to 0.3, consistent with the empirical value of 0.25 in the reaction-diffusion mechanism for modeling NBTI behaviour [6.14]–[6.17]. As stated earlier, the $t^{0.25}$ dependence means that the NBTI degradation is primarily controlled by the diffusion process, i.e., the rate at which the released species (hydrogen-related) is consumed through diffusion into the gate oxide [6.16]. As compared with PSS_LS pMOSFETs, PSS_HS split exhibits worse NBTI behaviour and similar degradation rate with the time evolution of $t^{0.25}$, which implies that the channel stress primarily impacts the reaction process of NBTI degradation mechanism [6.30][6.31], i.e., accelerating the dissociation rate of Si–H bonds by mechanical stress weakening its bonding strength.

Figs. 6.7(a) and 6.7(b) show the dependence of NBTI-induced V_T shifts ($\Delta V_{T,BT}$) and device lifetime on the inverse of temperature (1000/*T*), where stress temperatures are *T*= 75, 100, 125, 150℃ (i.e., *T*= 2.87, 2.68, 2.51, 2.36K^{-1} in terms of 1000/*T*), and all device lifetimes are normalized to that of PSS_HS split stressed at *T*= 150℃. It is found that, after long-term and severe stress (V_G= –2.4V, *T*= 150℃, and stress time *t*= 5000s), the lifetime of PSS_HS pMOSFETs is roughly half of that of PSS_LS split.

6.4 Dynamic Negative Bias Temperature Instability (DNBTI)

Besides static NBTI, we also characterize the dynamic NBTI of PSS_HS and PSS_LS pMOSFETs in this work. Here, the mechanism for degradation recovery of dynamic NBTI and the influence of stress frequency on dynamic NBTI-induced degradation are discussed.

6.4.1 Comparisons of Degradation Behaviour under Static and Dynamic NBTI

Figs. 6.8(a) and 6.8(b) show the V_T degradation behaviour of static and dynamic NBTI plotted in linear- and log-scale, respectively. For static NBTI, merely unipolar gate voltage (V_G= –2.4V) is applied. While for dynamic NBTI, bipolar gate voltage (V_G= –2.4V for stress cycles, and V_G= 1V for relax cycles) is used. As stress time increases, the $\Delta V_{T,BT}$ of static NBTI keeps increasing, while that of dynamic NBTI is partially recovered (decreased) during relax cycles, but continues degrading (increasing) as the stress cycles are reapplied. Furthermore, the deviation of $\Delta V_{T,BT}$ between static and dynamic NBTI also increases with stress time. So at a given degradation criterion of $\Delta V_{T,BT}$= 30 mV [6.20][6.21][6.32], the evaluated device lifetime of dynamic NBTI (τ_2) is around ten times of that of static NBTI (τ_1). As mentioned above, the dynamic NBTI stress is more suitable for accurately projecting the device lifetime from the viewpoint of real-life circuit operation. This observation is also addressed in some studies [6.20]–[6.22][6.32].

6.4.2 Mechanism for Degradation Recovery

Similar to the degradation behaviour of static NBTI, the PSS_HS pMOSFETs depict worse $\Delta V_{T,BT}$ under dynamic NBTI stress, as shown in Fig. 6.9(a). To understand the mechanism for this observation, we calculate $\Delta V_{T,BT}$ of each stress/relax cycle of both PSS splits, as shown in Figs. 6.9(b) and 6.9(c). $\Delta V_{T,BT}$ of each cycle is normalized to pre-stressed $V_{T,pre}$ as follows

$$\text{Stress cycle } \left|\frac{\Delta \boldsymbol{V}_{\mathbf{T,BT}}(t)}{\boldsymbol{V}_{\mathbf{T,pre}}}\right| = \left|\frac{\boldsymbol{V}_{\mathbf{T,BT}}[(2i-2)\times 10^3 + t] - \boldsymbol{V}_{\mathbf{T,BT}}[(2i-2)\times 10^3]}{\boldsymbol{V}_{\mathbf{T,pre}}}\right|, \quad (6.2a)$$

$$\text{Relax cycle } \left|\frac{\Delta \boldsymbol{V}_{\mathbf{T,BT}}(t)}{\boldsymbol{V}_{\mathbf{T,pre}}}\right| = \left|\frac{\boldsymbol{V}_{\mathbf{T,BT}}[(2i-1)\times 10^3 + t] - \boldsymbol{V}_{\mathbf{T,BT}}[(2i-1)\times 10^3]}{\boldsymbol{V}_{\mathbf{T,pre}}}\right|, \quad (6.2b)$$

where t is the stress time ($0 \le t \le 1000$), and i represents the number of stress/relax cycle ($1 \le i \le 3$). We found that for all stress cycles, the worst degradation occurs in the first cycle, and $\Delta V_{T,BT}$ significantly reduces to a level comparable to that of relax cycles with cycle number increasing, while for all relax cycles, similar $\Delta V_{T,BT}$ is observed. From this finding, it is speculated that the degradation recovery is partial and temporary in nature [6.33]. In addition, during NBTI stress the deteriorated gate dielectric contains recoverable (annealed) and permanent (fixed) oxide traps [6.22]. Some works reported that NBTI stress generates excess interface oxide traps and positive bulk oxide trap, where the trapping and detrapping of bulk oxide traps can explain the comparable $\Delta V_{T,BT}$ between stress ad relax cycles as the cycle number increases [6.10][6.22][6.30][6.31][6.34]–[6.37]. However, some works asserted instead that the repassivation of Si dangling bonds by hydrogen diffusing toward the Si/SiO_2 interface dominates the recovery mechanism [6.12][6.18][6.21][6.33].

Therefore, we extracted the change of interface trap density (ΔN_{it}) and subthreshold swing shift (ΔS) during stress/relax cycles, as shown in Fig. 6.10. The ΔN_{it} is obtained by the incremental frequency (Δf @1 MHz) charge pumping (CP) technique with fixed base voltage. The incremental frequency method is to take the difference of CP current (I_{CP}) measured at two different frequencies for eliminating the gate leakage-induced noise [6.38]. For example, the noise-reduced I_{CP} of 1 MHz is obtained by subtracting $I_{CP1}(f_1$@1 MHz) from $I_{CP2}(f_2$@2 MHz), i.e., $\Delta I_{CP}(\Delta f$@1 MHz)= $I_{CP2}(f_2$@2 MHz) – $I_{CP1}(f_1$@1 MHz), where f is the charge pumping frequency. It is worthy to note that the ΔN_{it} of both PSS splits significantly increase during stress cycles but slightly change during relax cycles, which suggests that the repassivation of Si dangling bonds by ionic hydrogen-related species, e.g., H^+ and H_3O^+, probably do not play any role on the degradation recovery. In other words, trapping and

de-trapping of holes mainly accounts for $\Delta V_{T,BT}$ recovery [6.34]–[6.36].

6.4.3 Fast- and Slow-State Interface Oxide Traps

In Fig. 6.10, we also show and compare the extracted subthreshold swing shift (ΔS). Different from the behaviour of ΔN_{it} with stress time, the ΔS of both PSS splits keep increasing during stress and relax cycles. Besides, the ΔS of PSS_HS pMOSFETs is roughly two times that of PSS_LS split. Comparing the different behaviour of ΔN_{it} and ΔS exhibited by the two PSS splits, we speculate two viewpoints as follows: 1) The NBTI-deteriorated gate dielectric contains interface oxide traps with different response times. Some of the interface oxide traps belong to electrical fast-states, capable of following the high frequency signal (e.g., high frequency CP), whereas the other interface oxide traps belong to electrical slow-states with typical switching time from 10^{-2} to 1 s [6.39][6.40]. The slow-state interface oxide traps, i.e., border traps, are different from the fast-state ones by their response time and location. Generally, the border traps, i.e., near-interfacial oxide traps, are located in the oxide within 0.2–2 nm of Si/SiO_2 interface [6.41]. Although some specific CP technique can sense the border trap density [6.40][6.42][6.43], the field-sensing techniques, e.g., subthreshold swing [6.44] and *C*–*V* technique [6.45], are more suitable for monitoring the slow-state interface oxide traps. 2) The worse NBTI behaviour of PSS_HS pMOSFETs may result from the excess slow-state interface oxide traps induced by the mechanical stress. Some studies pointed out that the border trap also could be caused by different phenomena, such as the lattice distortion related to the highly strained Si/SiO_2 interface [6.44] and the use of nitrided oxides [6.39][6.41][6.46]. In state-of-the-art manufacturing the nitrided oxides are widely employed, and as the gate dielectric thickness scales down, the incorporated nitrogen concentration is increased in order to reduce the gate leakage. As a result,

border traps will become increasingly important [6.39].

6.4.4 Dependence of Stress Frequency on Dynamic NBTI Degradation

In this work, we also applied trapezoid pulse to the gate terminal with pulse frequency (from 100K to 1 MHz) as the parameter for simulating the circuit operation of CMOS inverter, where the input trapezoid pulse has “high” and “low” logic states (V_{Hi}= 1 V for relax cycle, and V_{Lo}= –2.4 V for stress cycle), and the duty cycle of the pulse is 50 %. Figs. 6.11(a) and 6.11(b) show the dependence of $\Delta V_{T,BT}$ and device lifetime on stress frequency of dynamic NBTI, respectively, where the lifetime of all devices are normalized to that of PSS_HS split under static NBTI stress. Similar to the degradation behaviour of PSS_HS pMOSFETs under static NBTI stress, after stress time of 2000 s, the PSS_HS split depicts larger $\Delta V_{T,BT}$ and its device lifetime is reduced to half of that of PSS_LS split under dynamic NBTI stress. In addition, it is worthy to note that the degradation behaviour of dynamic NBTI is insensitive to its stress frequency irrespective of channel stress level [6.18][6.20][6.21].

6.5 Conclusions

In this work, we have investigated the degradation behaviour of strained pMOSFETs under static and dynamic negative bias temperature instability (NBTI) stress. Utilizing the process-strained Si (PSS) technique and three-dimensional (3D) strain engineering, we have fabricated PSS pMOSFETs with both lower compressive stress (LS) and higher compressive stress (HS) along the *y*-axis (channel width direction). We found that reducing compressive stress along *y*-axis not only enhances drain current (about 5%) but also prolongs device lifetime of NBTI (about two times) for PSS_LS pMOSFETs. In addition, it is observed that the impact of mechanical stress on NBTI degradation becomes more evident under long-term and severe stress

conditions because higher mechanical stress induces excess oxide traps. These traps are formed through the weakening of chemical bonds at or near the interface by stress which in turn could accelerate the dissociation of Si–H bonds. By evaluating the degradation behaviour of interface trap density and subthreshold swing under dynamic NBTI stress, it is speculated that NBTI-induced oxide traps contains not only the interface oxide traps (i.e., fast-state) but also the near-interfacial oxide traps (slow-state), i.e., border traps, where the trapping and detrapping behaviour of border traps accounts for degradation recovery during dynamic NBTI stress. Finally, we also found that the worse degradation behaviour for higher channel stress is attributed to the generation of excess near-interfacial oxide traps.

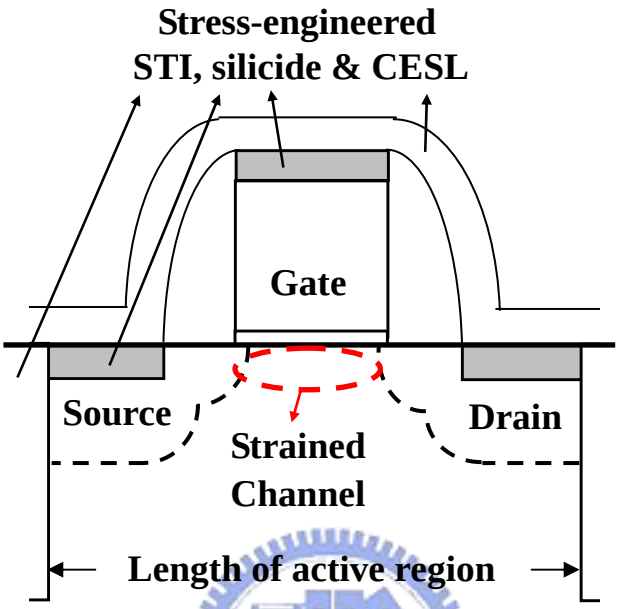
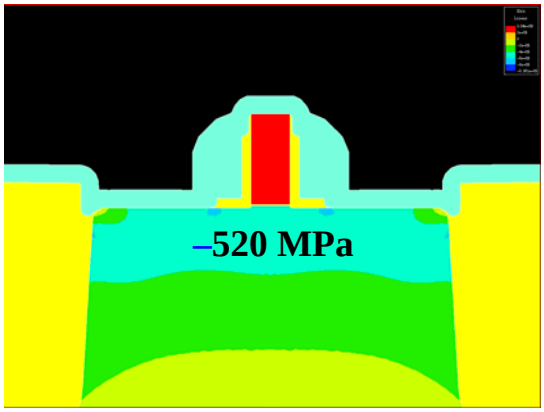
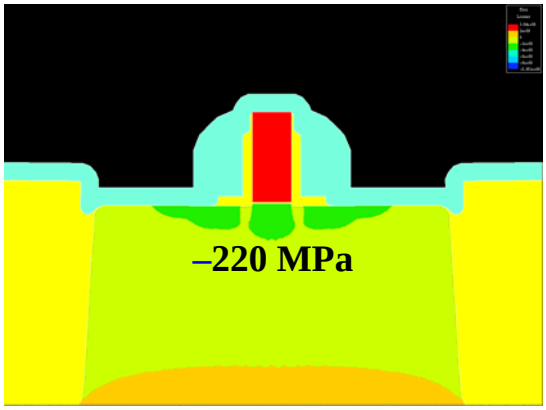


Fig. 6.1. Schematic view of process-strained Si (PSS) pMOSFETs, where channel stress is engineered from the combination of shallow trench isolation (STI), silicide and contact etch stop layer (CESL).



(a)



(b)

Fig. 6.2. Simulated stress profile for (a) PSS_HS, and (b) PSS_LS pMOSFETs by TSuprem4. PSS_HS and PSS_LS devices exhibit about –520 and –220 MPa in the center of channel region, respectively, where minus sign denotes compressive stress.

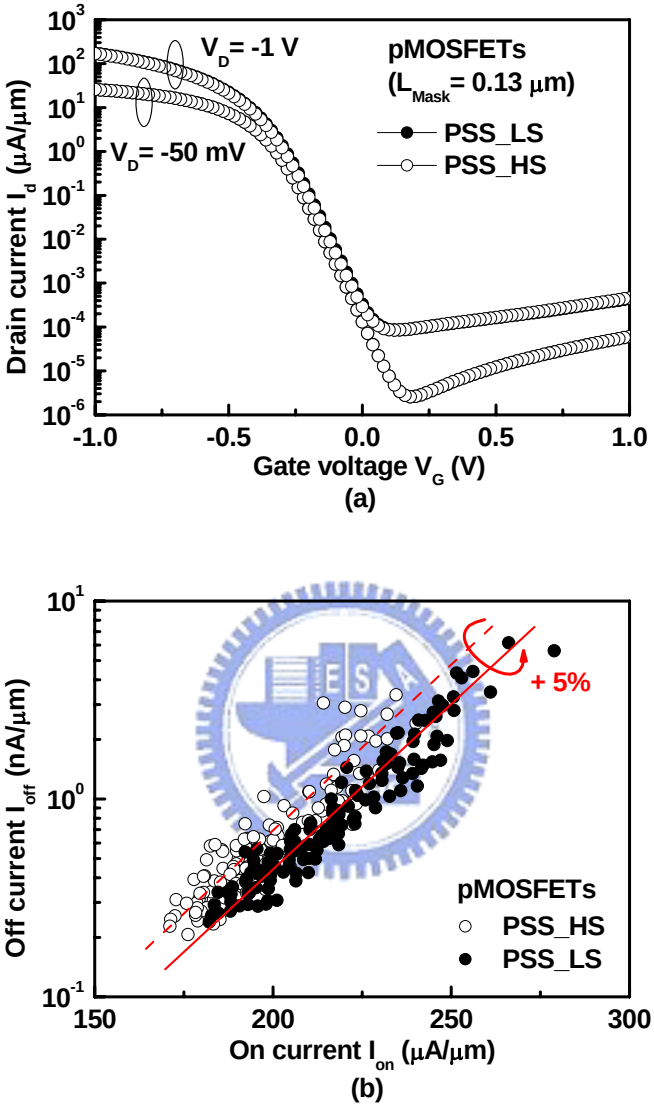


Fig. 6.3. (a) Drain current (I_d) versus gate voltage (V_G), and (b) off-current (I_{off}) versus on-current (I_{on}) characteristics for PSS_HS and PSS_LS pMOSFETs.

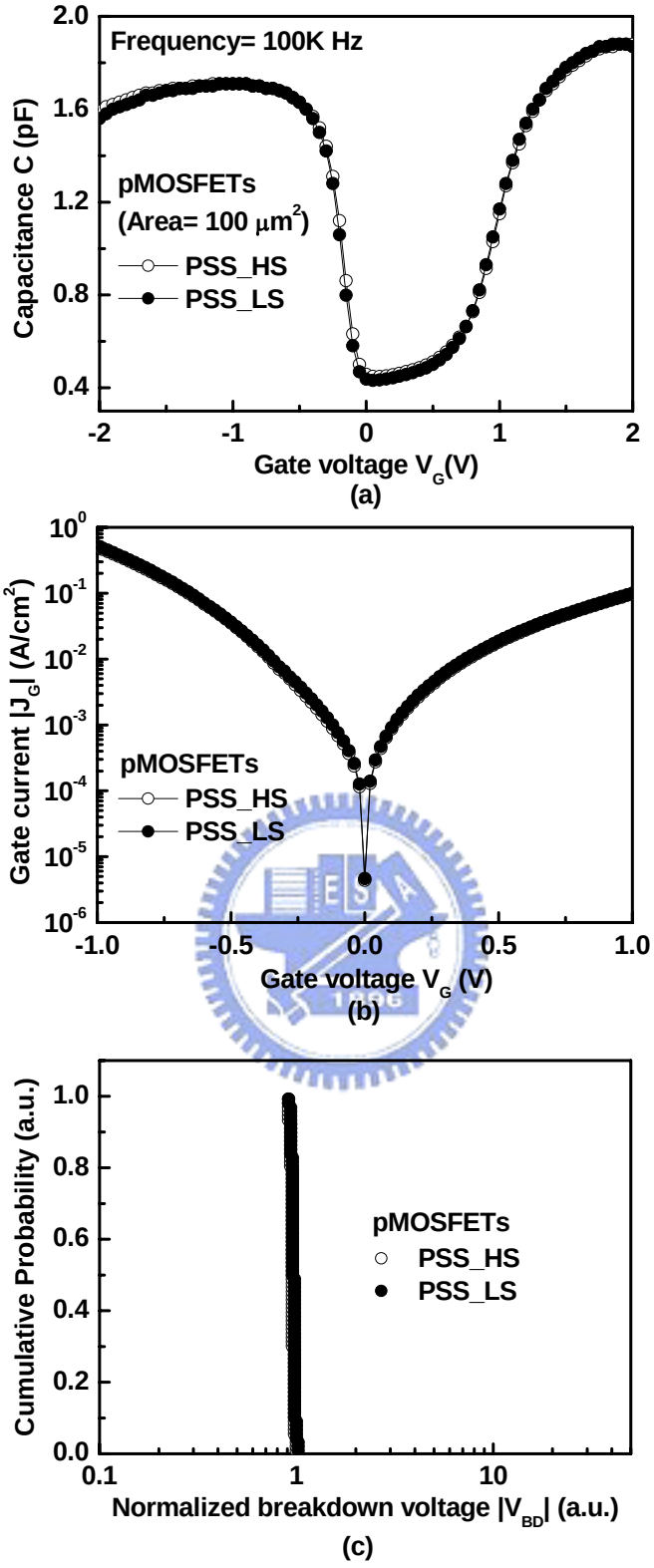


Fig. 6.4. (a) Capacitance (C) versus gate voltage (V_G), (b) gate current ($|J_G|$), and (c) cumulative probability of normalized gate dielectric breakdown voltage ($|V_{BD}|$) for PSS_HS and PSS_LS pMOSFETs.

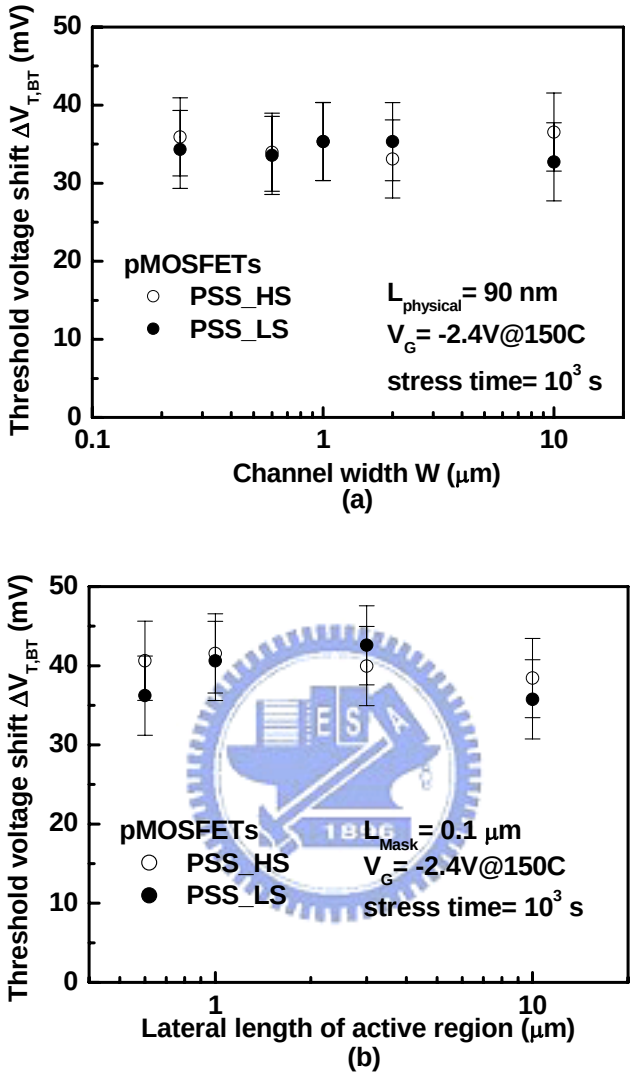


Fig. 6.5. Negative bias temperature instability (NBTI)-induced threshold voltage shift ($\Delta V_{T,BT}$) versus (a) channel width (W), and (b) lateral length of active region for both PSS_HS and PSS_LS pMOSFETs.

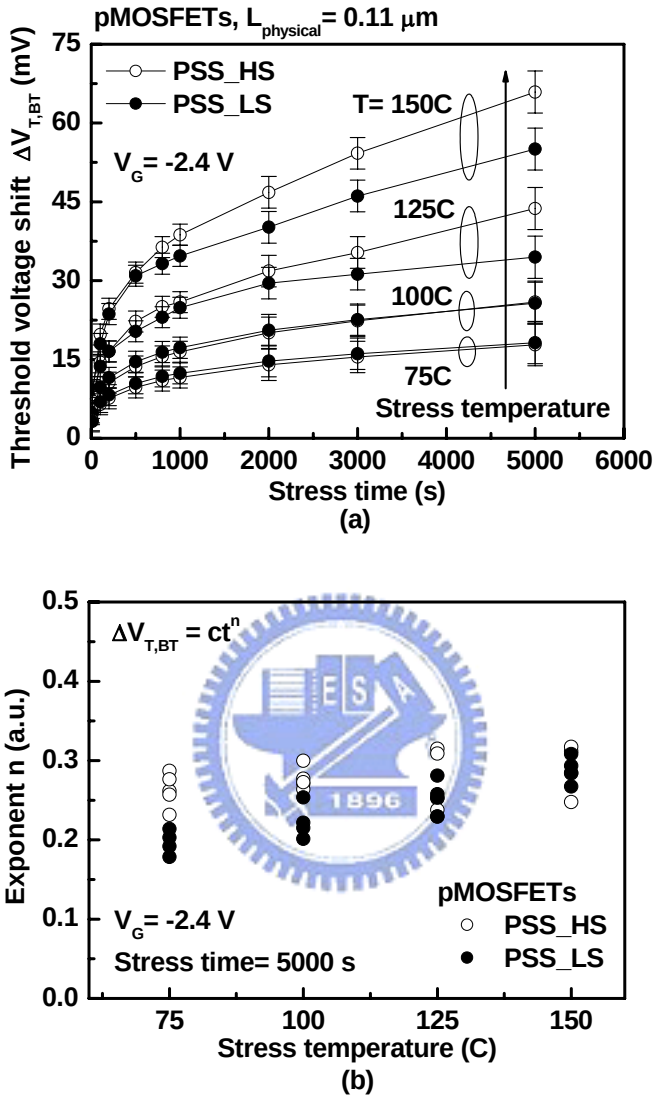


Fig. 6.6. (a) Dependence of NBTI-induced threshold voltage shift ($\Delta V_{T,BT}$) on stress time (t) with stress temperature (T= 75, 100, 125, 150℃) as parameter for PSS_HS and PSS_LS pMOSFETs. According to the power-law relation of $\Delta V_{T,BT}= ct^n$, the exponent (n) of various stress temperatures in (b) can be extracted by linearly fitting the plot of $\Delta V_{T,BT}$ (in log scale) versus t (in log scale).

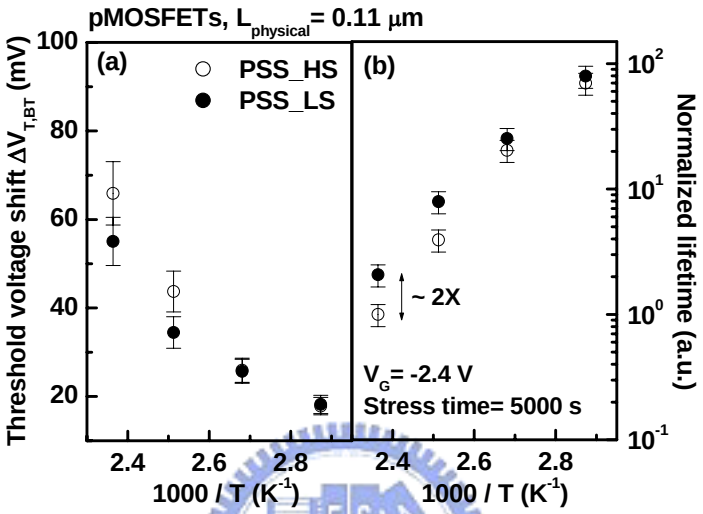


Fig. 6.7. Dependence of (a) NBTI-induced V_T shift ($\Delta V_{T,BT}$), and (b) device lifetime on the inverse of stress temperature (1000 / T) for PSS_HS and PSS_LS pMOSFETs, where stress temperatures are T= 75, 100, 125, and 150℃. In (b), the lifetime of all PSS devices are normalized with respect to that of PSS_HS stressed at T= 150℃.

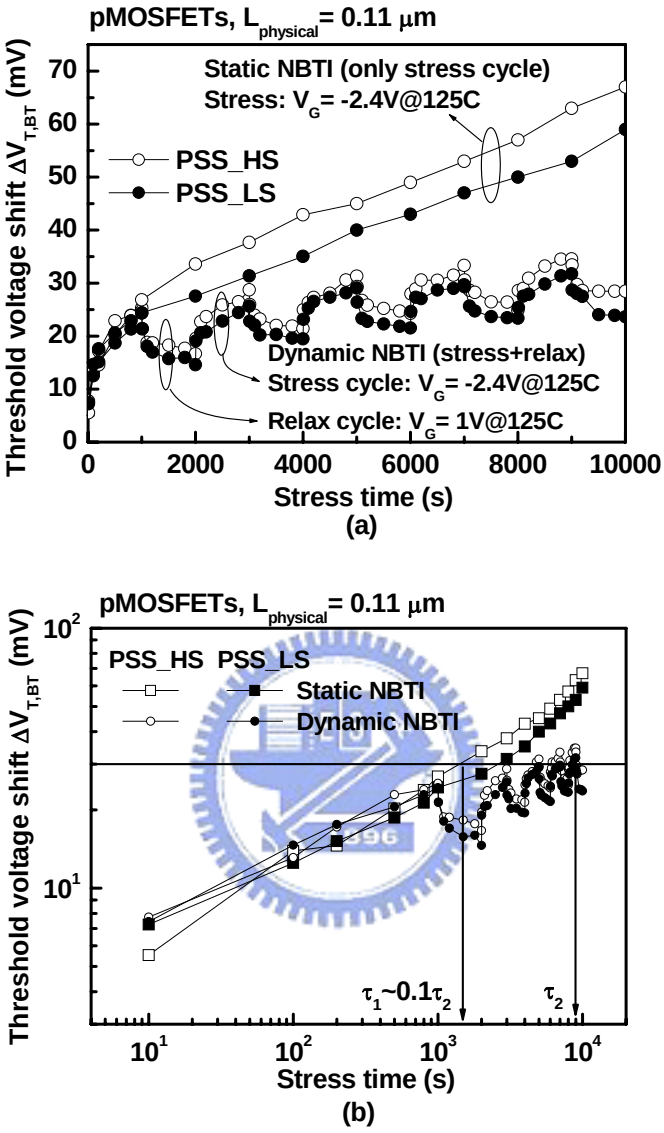


Fig. 6.8. Comparisons of NBTI-induced V_T shift ($\Delta V_{T,BT}$) under static and dynamic stress in (a) linear-scale, and (b) log-scale plots. Static NBTI consists of only stress cycles (V_G= –2.4V@T= 125℃), while dynamic NBTI includes stress and relax cycles (V_G= 1V@T= 125℃) for simulating the real circuit operation.

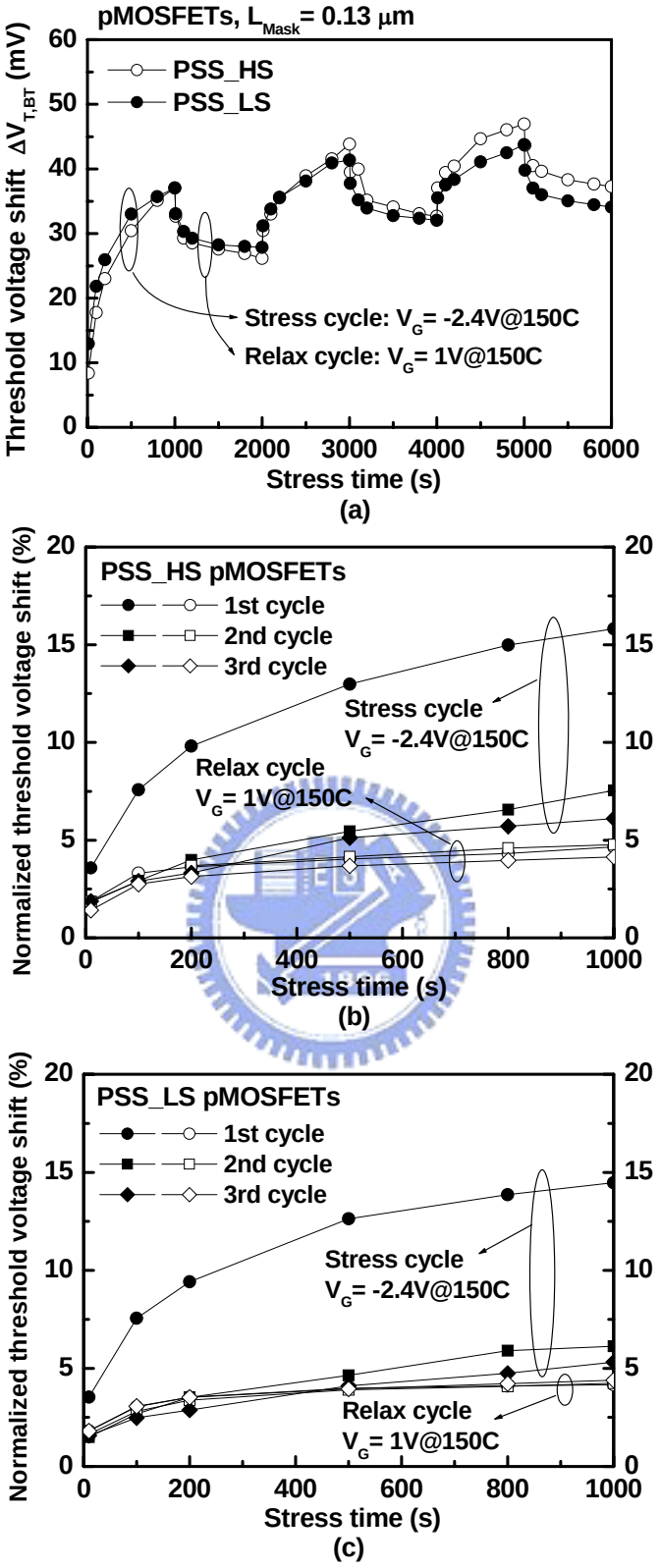


Fig. 6.9. (a) NBTI-induced V_T shift ($\Delta V_{T,BT}$) versus stress time, and the corresponding $\Delta V_{T,BT}$ of each stress/relax cycle for (b) PSS_HS, and (c) PSS_LS pMOSFETs, where $\Delta V_{T,BT}$ of each stress/relax cycle is normalized to pre-stressed V_T.

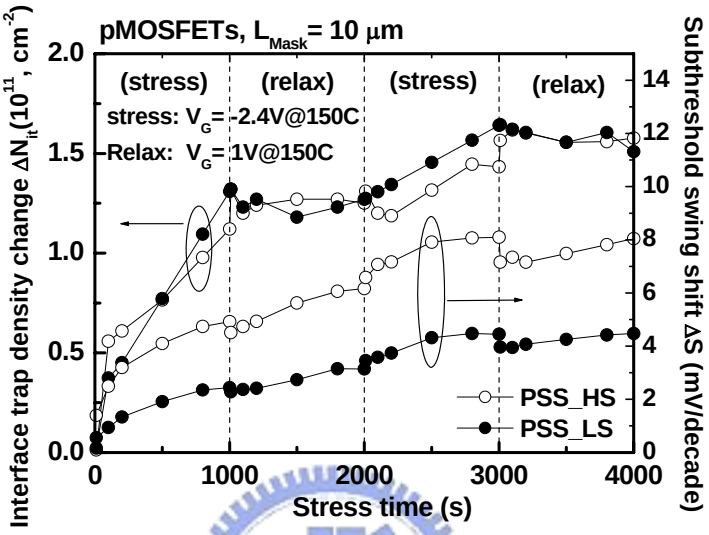


Fig. 6.10. Dynamic NBTI-induced interface trap density change (ΔN_{it}) and subthreshold swing shift (ΔS) for PSS_HS and PSS_LS pMOSFETs.

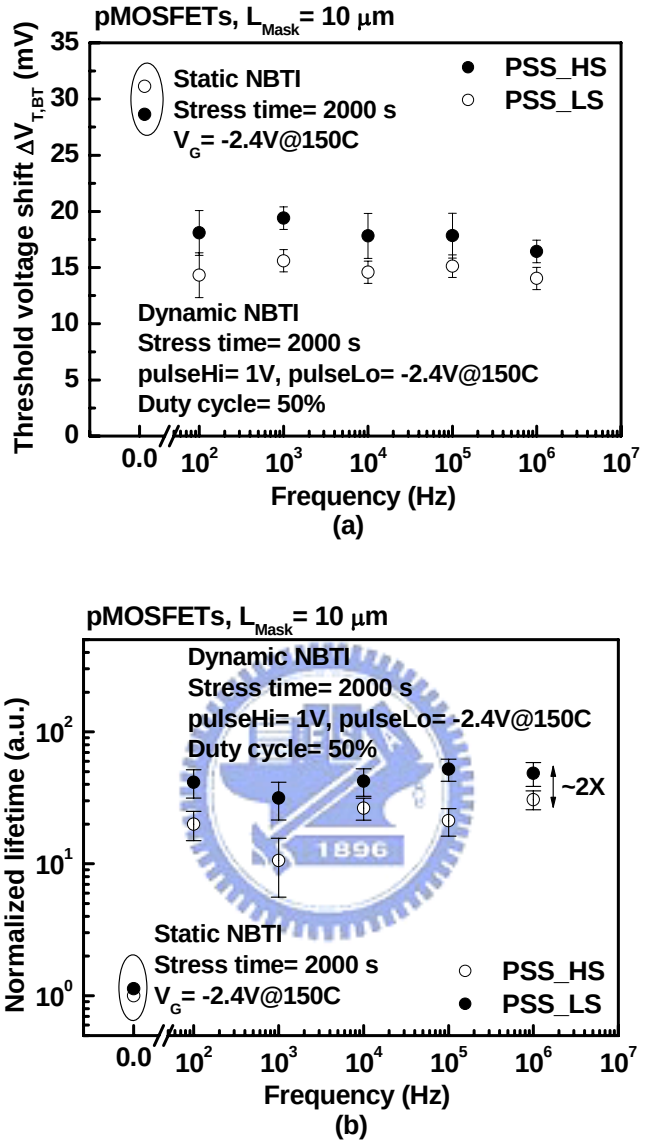


Fig. 6.11. Dependence of (a) dynamic NBTI-induced V_T shift ($\Delta V_{T,BT}$), and (b) the projected device lifetime on stress frequency for PSS_HS and PSS_LS pMOSFETs. In (b), the lifetime of all devices are normalized to that of PSS_HS split under static NBTI stress.