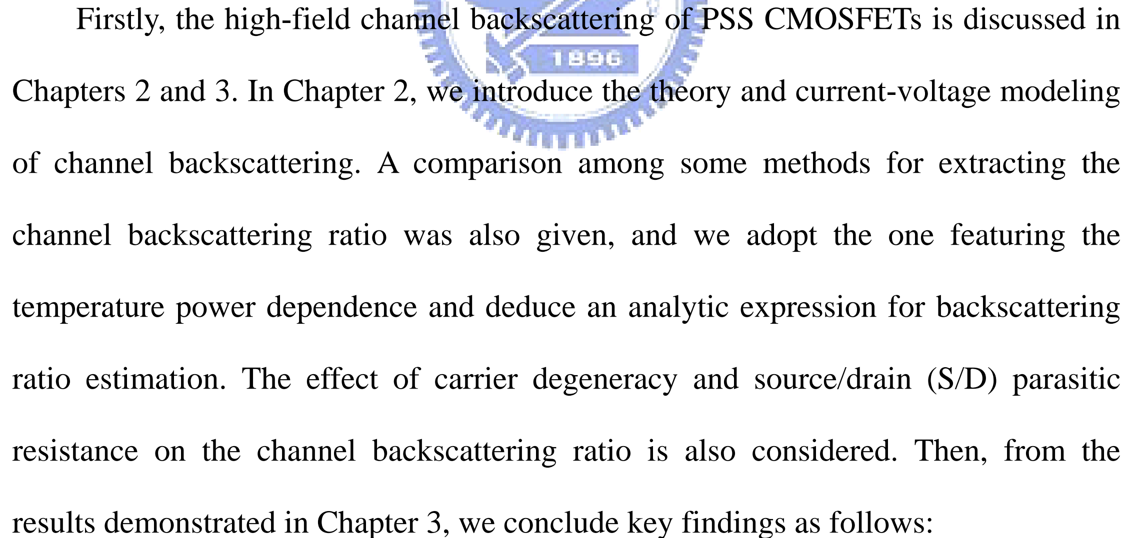
Chapter 7

Summary and Future Works

7.1 Summary

In this thesis we have characterized the carrier transport and reliability of state-of-the-art CMOSFETs with the process-strained Si (PSS) technique. Major efforts were devoted to the impact of process-induced uniaxial strain on low-field carrier transport and high-field channel backscattering, and their correlation as the CMOS technology nodes scale down. In addition, the influence of channel stress on negative bias temperature instability (NBTI)-induced degradation is also investigated.

7.1.1 Summary of Chapters 2 and 3



Firstly, the high-field channel backscattering of PSS CMOSFETs is discussed in Chapters 2 and 3. In Chapter 2, we introduce the theory and current-voltage modeling of channel backscattering. A comparison among some methods for extracting the channel backscattering ratio was also given, and we adopt the one featuring the temperature power dependence and deduce an analytic expression for backscattering ratio estimation. The effect of carrier degeneracy and source/drain (S/D) parasitic resistance on the channel backscattering ratio is also considered. Then, from the results demonstrated in Chapter 3, we conclude key findings as follows:

(1) The channel stress affects the high-field carrier transport, and the impact becomes more evident as the channel stress increases, where the ballistic efficiency is improved for tensile-PSS nMOSFETs but degraded for compressive-PSS pMOSFETs.

(2) Saturation drain current gain is related to the sum of ballistic efficiency

modulation and change in injection velocity. Thanks to strain-induced effective mass reduction, both PSS nMOSFETs and PSS pMOSFETs show noticeable enhancement in injection velocity. The PSS nMOSFETs depict improved ballistic efficiency and injection velocity, which are both positive to drain current. However, the PSS pMOSFETs show significant enhancement of injection velocity but degraded ballistic efficiency, which results in a trade-off for current gain.

(3) Slight increase in carrier scattering mean-free-path (MFP) accounts for the ballistic efficiency enhancement of PSS nMOSFETs. Compressed lattice-induced excess phonon scattering and then decreased scattering MFP is responsible for ballistic efficiency reduction of PSS pMOSFETs.

7.1.2 Summary of Chapters 4 and 5

The low-field carrier transport of PSS CMOSFETs is discussed in Chapters 4 and 5. In Chapter 4, we propose a model for correlating the low-field and high-field carrier transport of PSS CMOSFETs. The model features key relations as follows: the linear and saturation drain current gains can be modeled as linear functions of low-field channel mobility gain with the intercept of S/D resistance reduction, where the ratio of S/D parasitic resistance to channel resistance and the ballistic efficiency determine the translating efficiency of low-field channel mobility gain on the linear drain current gain and saturation drain current gain, respectively. By elimination of channel mobility gain, we deduce the dependence between the linear and saturation drain current gain. Then, from the above correlations, we develop a new methodology for evaluating total S/D parasitic resistance for nanoscale strained MOSFETs without dealing with the uncertainty of determining the electrical channel length and the ambiguous assumption of constant channel mobility for all channel lengths.

Next, in Chapter 5, we use state-of-the-art PSS CMOSFETs with different technology nodes for examining the proposed model. According to the experimental results, we conclude some observation as follows.

(1) Irrespective of featuring technology nodes, the total S/D parasitic resistance will gradually diminish the benefit of strain-enhanced channel mobility and drain current since the ratio of S/D parasitic resistance to channel resistance increases with decreasing channel length.

(2) The linear drain current gain is similar to the saturation drain current gain for PSS nMOSFET, while it is larger than the saturation one for PSS pMOSFETs. It is attributed to the fact that PSS nMOSFETs exhibit comparable S/D resistance and channel resistance, whereas the S/D resistance is smaller than the channel resistance for PSS pMOSFETs.

(3) Conventional MOSFETs scaling practices maintain a similar ballistic efficiency of 0.5 regardless of the technology nodes employed, which reveals that for a "well-tempered" short channel device, only half of strain-enhanced mobility gain can be translated into the saturation drain current gain.

7.1.3 Summary of Chapter 6

Finally, we study the NBTI degradation of PSS pMOSFETs with different channel stresses, and discuss the mechanisms for degradation recovery during dynamic NBTI stress and the higher channel strain-induced worse degradation. Some conclusions are shown as follows.

(1) For PSS pMOSFETs, decreasing the channel compressive stress along the channel width direction improves not only the drain current but also the device reliability of NBTI.

(2) The mechanism for degradation recovery during dynamic NBTI stress is the

detrapping of near-interfacial oxide traps, i.e., border traps or slow-state interface oxide traps.

(3) PMOSFETs with larger channel stress exhibit aggravated NBTI degradation, which results from mechanical stress-induced generation of excess near-interfacial oxide traps.

7.2 Suggestions for Future Works

There are some suggestions for future works.

(1) The above conclusions are valid for MOSFETs with uniaxial process-strained Si channel. The effect of other kinds of strained techniques, such as substrate-induced biaxial strain method, on channel backscattering characteristics may be different from our results and has not been reported yet.

(2) It is worthy to study the correlation between low-field channel mobility gain, linear drain current gain, saturation drain current gain, and S/D parasitic resistance reduction of biaxial-strained nanoscale CMOSFETs and compare the results with the uniaxial strain case.

(3) Here, it should be emphasized that the extracted low-field channel mobility of nanoscale devices is relative to the control counterparts, rather than an absolute one. For accurate absolute mobility estimation, someone must develop a new methodology for accurately evaluating the electrical channel length without ambiguous issues.

(4) One of our major contributions is to find that decreasing uniaxial compressive stress along the channel width of pMOSFETs improves not only its drain current but also the device lifetime under NBTI stress. Therefore, it is interesting to examine the effect of channel stress on device reliability,

such as hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and NBTI, by the three-dimensional (3D) strain engineering, and then find the optimized channel stress configuration with current gain and device reliability improvement. In addition, the NBTI study of pMOSFETs with embedded SiGe S/D is also critical since embedding SiGe in S/D regions have become one of the mainstream techniques for boosting the device performance of nanoscale pMOSFETs.