Chapter 1

Introduction

1.1 Introduction to SiGe HBTs

Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) have become major devices for radio frequency (RF) circuit implementation partly due to its excellent performance which have enabled products with lower power consumption, and higher functional integration. Also contributing to the popularity of SiGe HBTs is the fact that common radio architectures are well suited to implementation in a combination of bipolar and CMOS devices, as well as the fact that SiGe HBTs are available today from a variety of sources making it easily accessible and affordable.

Several applications have driven advances in SiGe technology since the first SiGe bipolar devices were demonstrated in the late 1980s [1]. Initially, SiGe HBTs were conceived as a replacement to the Si bipolar for ECL, high speed digital integrated circuits (ICs) but CMOS advancements in density, performance, and power consumption, quickly made it the logical choice for all but a very few of these applications. Later, communication applications, in the form of wireless and wire-line transceiver circuits, emerged as the primary driving force for development of SiGe HBTs.

The requirement of wireless transceiver brought SiGe HBTs into volume production as SiGe HBTs made possible the integration of low noise LNAs and low power frequency synthesizers [3]. Likewise, SiGe HBTs are rapidly emerging as a competitor to III-V technologies such as GaAs and InP for wireless and wireline application, since it provides comparable device-level performance while maintaining

compatibility with the economy-of-scale, and hence cost benefits, associated with conventional Si IC manufacturing [1]. Todays, SiGe HBTs are providing a path for performance improvement and cost reduction of various applications and opening possibilities for the implementation of RF circuits at higher frequencies. Commercial SiGe HBTs with transistor performance in the range of 50-100 GHz now exist in multiple companies worldwide and recent work [2] has demonstrated that manufacturable SiGe HBT technologies with performance well-above 380 GHz can be achieved by profile and structural design.

1.2 Motivation

SiGe HBTs have shown excellent microwave and noise performance and are very attractive for millimeter-wave and optical-electronic applications. As the range of SiGe HBTs applicability constantly widens, the need for accurate small-signal and noise models is a key factor for successful employment of these devices in circuit systems. The complete characterization of SiGe HBTs in terms of scattering parameters (S-parameters) and noise is necessary for computer aided design (CAD) of monolithic microwave integrated circuits (MMICs) and optical-electronic integrated circuits (OEICs).

An accurate SiGe HBTs small-signal model is necessary for an accurate characterization of SiGe HBTs high-frequency noise. The most commonly used small-signal parameter extraction technique is numerical optimization of the model generated S-parameters to fit the measured data. It is well known that optimization techniques may result in nonphysical and/or nonunique values of the components. Determination of small-signal model parameters by direct extraction is preferred over

numerical optimization because of uniqueness, efficiency, and physical meaningfulness [4], [5]. Many approaches for an accurate and physically oriented parameter extraction of HBT have been suggested in the literatures, especially for III-V HBTs where the substrate has negligible effect on the performance [6]-[12]. Recently, a few direct parameter extractions for SiGe HBTs have also been reported [13]-[15], and some of them have taken into account the substrate effects in their own methods. Although we have applied the previous methods to the modeling of our SiGe HBTs, the results are not so successful, especially when dealing with large area SiGe HBTs. We found that it is caused by improper modeling results of substrate network. Therefore, it is urgent to develop an accurate and simple direct extraction method for small-signal modeling of SiGe HBTs together with a proper modeling of substrate network.

Transistor high-frequency noise is another crucial issue in high-frequency circuit design as it sets the lowest sensitivity in the communication system. An accurate noise model is required for low noise circuit design. As SiGe BiCMOS technology becomes mature, SiGe HBTs have been applied widely in high-frequency circuit design. The essence of bipolar transistor RF noise model in current CAD is to assume that base and collector current noises are shot noise (white noise), with a power spectral density of $2qI_B$ and $2qI_C$, respectively. The base and collector current noises are also assumed to be uncorrelated. However, as the transistor technology improves, SiGe HBTs were operated in a higher frequency and it is worthy investigating whether aforementioned assumptions are still valid in high frequency range. Thus, it is urgent to develop an extraction technique for the fundamental noise sources of SiGe HBTs. By applying the developed technique, we can investigate the frequency and current dependence of the base and collector noise sources and discussing the correlation of them.

1.3 Thesis Outline

The content in this thesis includes many parts.

Chapter 1 introduces the history of SiGe HBTs, their applications and the motivation of this thesis.

Chapter 2 introduces the original of hybrid-π small-signal equivalent circuit of III-V HBTs and proposes a novel parameter extraction method of the hybrid-π small-signal equivalent circuit of III-V HBTs.

Chapter 3 presents an improved parameter extraction technique for the small-signal modeling of SiGe HBTs. Differing from other methods, the proposed technique considers the internal feedback signal through intrinsic circuit elements when extracting the substrate network parameters. Transforming the intrinsic equivalent circuit into its common-collector configuration, all the circuit elements are extracted directly without using any optimization.

Chapter 4 explains the anomalous dip in scattering parameters S_{12} of SiGe HBTs quantitatively by using the proposed analytical equation of out impedance and feedback voltage ratio.

Chapter 5 presents a computation method for extracting noise parameters of a linear two-port network using a genetic algorithm. The developed method inherits the advantages of the Vasilescu's method of requiring no initial values. Besides, the computer-time of genetic search is independent on the number of measured source impedance and considers noise figure and source admittance errors simultaneously.

Chapter 6 presents a systematic extraction procedure to extract the base current noise (S_{ib}), collector current noise (S_{ic}), of SiGe HBTs and their cross correlation $S_{ib,ic*}$ directly from the measured S-parameter and RF noise parameters. A systematic 4×4 four-port Y-parameters ([Y_{ee}], [Y_{ei}], [Y_{ie}], and [Y_{ii}]) calculation method is developed and applied in the four-port noise de-embedding procedure.

Chapter 7 makes the conclusions of the thesis.

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Chapter 2

Small-Signal Modeling of III-V HBTs

2.1 Introduction of Small-Signal modeling of III-V HBTs

To develop the direct extraction method for small-signal modeling of SiGe HBTs, it is better to investigate the small-signal modeling of III-V HBTs first. Small-signal modeling of III-V HBTs where the substrate network has negligible effect on the performance is much easier as compared to that of SiGe HBTs. Therefore, in this chapter, we discuss the origin of small-signal equivalent circuit of III-V HBTs [1] and also present a novel extraction method for the small-signal modeling of III-V HBTs [2].

2.2 Origin of Small-Signal Equivalent Circuit of HBTs

Figure 2.1 shows the cross section view of a conventional III-V HBT. The intrinsic HBT shown in the dashed box of Fig. 2.1 denotes the active operation region under emitter area. The region outside the dashed box contributes the parasitic elements to the intrinsic HBT. To derive the small-signal equivalent circuit, we can start from the intrinsic HBT and then add the parasitic elements to the intrinsic HBT to obtain a complete small-signal equivalent circuit of III-V HBTs.

Figure 2.2 illustrates the intrinsic HBT in a small-signal operation, biased in the common-base configuration. The small-signal voltage v_{be} and v_{cb} are superimposed on the DC biases V_{BE} and V_{CB}, respectively. The overall applied voltage are $v_{BE} = V_{BE} + v_{be}$ and $v_{CB} = V_{CB} + v_{cb}$. The resulting emitter and collector currents are $I_E + i_e$, and $I_C + i_c$, respectively, where I_E and I_C are the values corresponding to the DC operation point when the applied voltages are V_{BE} and V_{CB}. The overall emitter and collector currents can be written as functions of the base-emitter and base-collector voltages [1]:

$$i_E = I_E + i_e = f_1(v_{BE}, v_{CB}) \tag{2.1}$$

and

$$i_C = I_C + i_c = f_2(v_{BE}, v_{CB}). \tag{2.2}$$

After Taylor's expansions, we can easily obtain following equations:

$$\begin{bmatrix} \tilde{i}_e \\ \tilde{i}_c \end{bmatrix} = \begin{bmatrix} y_{ee} & y_{ec} \\ y_{ce} & y_{cc} \end{bmatrix} \begin{bmatrix} \widetilde{v_{be}} \\ \widetilde{v_{cb}} \end{bmatrix} = \begin{bmatrix} \left.\frac{\partial i_E}{\partial v_{BE}}\right|_{V_{CB}} & \left.\frac{\partial i_E}{\partial v_{CB}}\right|_{V_{BE}} \\ \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{V_{CB}} & \left.\frac{\partial i_C}{\partial v_{CB}}\right|_{V_{BE}} \end{bmatrix} \begin{bmatrix} \widetilde{v_{be}} \\ \widetilde{v_{cb}} \end{bmatrix} \tag{2.3}$$

where

$$\begin{bmatrix} v_{be} & i_e \\ v_{cb} & i_c \end{bmatrix} = \begin{bmatrix} \widetilde{v_{be}} e^{jwt} & \tilde{i}_e e^{jwt} \\ \widetilde{v_{cb}} e^{jwt} & \tilde{i}_c e^{jwt} \end{bmatrix}. \tag{2.4}$$

Our goal is to express the four Y-parameters, y_{ee}, y_{ec}, y_{ce} and y_{cc}, in terms of physical parameters such as base-emitter capacitance, base-emitter resistance, and etc. Fig. 2.3 shows the schematic diagram of the small-signal current flows in a normal operation will be used for the development of the Y-parameters.

2.2.1 Derivation of y_{ee}

From (2.3), y_{ee} is defined as the partial derivative of i_e with respect to v_{be} when V_{CB} is kept constant. When v_{be} is applied on top of V_{BE}, there are two components of small-signal currents giving rise to the overall i_e. The first component is the capacitive current flowing through the base-emitter junction capacitance, and the second component is the incremental current due to a change in the minority carrier concentration in the base. The overall i_e is expressed as:

$$i_e = i_{e1} + i_{e2} \tag{2.5}$$

when v_{be} is applied on top of V_{BE}, the depletion thickness of the base-emitter junction decreases or increases depending on whether the magnitude of v_{be} is positive or negative, respectively. Following the basic semiconductor theory [1], the small-signal current i_{e1}, which is equal to the time derivative of the small-signal charge variation, is expressed as:

$$i_{e1} = jwC_{je}\widetilde{v_{be}}e^{jwt} \tag{2.6}$$

where C_{je} is the base-emitter junction capacitance.

The second small-signal emitter current component results from the perturbation of base minority carrier concentration due to v_{be}. By solving the time-varying current continuity equation in the base region [1], we finally find such small-signal emitter current is equal to

$$i_{e2} = I_E \frac{q\widetilde{v_{be}}}{kT}\zeta_{ac}X_B \coth\left(\zeta_{ac}X_B\right) \tag{2.7}$$

where X_B is base thickness and ζ_{ac} is frequency dependent diffusion length and is defined as

$$\zeta_{ac} = \sqrt{\frac{1+jw\tau_n}{D_n\tau_n}} \tag{2.8}$$

where D_n and τ_n are electron diffusion coefficient and electron recombination lifetime, respectively. With (2.6) and (2.7), the small-signal y_{ee} parameter is obtained as

$$y_{ee} = \frac{\tilde{i}_e}{\widetilde{v_{be}}}\bigg|_{\widetilde{v_{cb}}=0} = g_e\zeta_{ac}X_B \coth\left(\zeta_{ac}X_B\right) + jwC_{je} \tag{2.9}$$

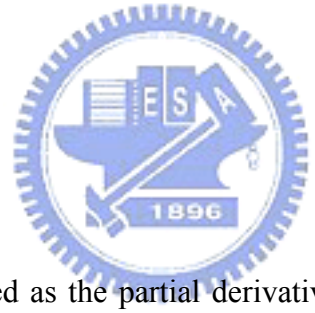
where g_e is the emitter conductance and is equal to $qI_E/\eta kT$ (η is the ideality factor of collector current). With the assumption that X_B/L_n is small, y_{ee} is approximated as

$$y_{ee} = g_e + jw\left(C_D + C_{je}\right) \tag{2.10}$$

where C_D, the diffusion capacitance of base-emitter junction, is given by

$$C_D = g_e \frac{X_B^2}{3D_n}. \tag{2.11}$$

One should be noted that the assumption that X_B/L_n is negligible small is only valid at low frequency range. At frequencies approaching f_T, the exact equation of y_{ee} cannot be simplified into a parallel RC-lumped representation as in (2.10) and the term diffusion capacitance is no longer meaningful. Therefore, when performing small-signal modeling on HBTs, the modeling frequency should be kept below f_T so that we can use the conventional RC-lumped equivalent circuit to model the frequency response of base-emitter junction.



2.2.2 Derivation of y_{ce}

From (2.3), y_{ee} is defined as the partial derivative of i_c with respect to v_{be} when V_{CB} is kept constant. From Fig. 2.3, y_{ce} can be written as

$$y_{ce} = \frac{\tilde{i}_c}{\tilde{v}_{be}}\bigg|_{\tilde{v}_{cb}=0} = \frac{\tilde{i}_c}{\tilde{i}_{cc}}\frac{\tilde{i}_{cc}}{\tilde{v}_{be}}\bigg|_{\tilde{v}_{cb}=0}. \tag{2.12}$$

Unlike i_e, which originates from two distinctive locations, i_{cc} comes purely from the modified carrier concentration inside the base. There is no associated capacitive current from the base-collector junction capacitance because the base-collector bias is maintained constant in the y_{ce} calculation. Therefore, the magnitude of i_{cc} is,

$$\tilde{i}_{cc} = -qD_n A_E \frac{d\tilde{n}}{dx}\bigg|_{x=X_B}. \tag{2.13}$$

At low frequencies, the derivative of (2.13) with respective to $\widetilde{v_{be}}$ is obtained as:

$$\frac{\widetilde{i_{cc}}}{\widetilde{v_{be}}}\Big|_{\widetilde{v_{cb}}=0} \approx -\alpha_{T0} g_e \left(1 - j\frac{w}{3w_0}\right) \tag{2.14}$$

where α_{T0} is the DC base transport factor:

$$\alpha_{T0} = 1 - \frac{X_B^2}{2L_n^2} \tag{2.15}$$

and w_0 is the inverse of the base transit time:

$$w_0 = \frac{2D_n}{X_B^2}. \tag{2.16}$$

We now seek the relationship between i_c and i_{cc}. The base-collector junction is a high-field region where a carrier travels at a constant velocity equal to the saturation velocity, v_{sat}. Applying the Maxwell equation to the derivation [1], we obtain

$$\frac{i_c(t)}{i_{cc}(t)} = \frac{\sin(w\tau_m/2)}{w\tau_m/2}\exp(-jw\tau_m) \tag{2.17}$$

where

$$\tau_m = \frac{X_{dep}}{v_{sat}}. \tag{2.18}$$

Since $\sin(w\tau_m/2)/(w\tau_m/2)$ is nearly unity even at high frequencies, y_{ce} can be written as either of the following equations:

$$y_{ce} = -\alpha_{T0} g_e \left[1 - j(1-m)\frac{w}{w_0}\right]\exp(-jw\tau_m/2) \tag{2.19}$$

and

$$y_{ce} = -\alpha_{T0} g_e \left[1 - j(1-m)\frac{w}{w_0} - j\frac{w\tau_m}{2}\right]. \tag{2.20}$$

2.2.3 Derivation of y_{ec}

y_{ec} is defined as the partial derivative of i_e with respect to v_{cb} when V_{BE} is kept constant. From (2.3), y_{ec} is

$$y_{ec} = \frac{\tilde{i}_e}{\tilde{v}_{cb}}\bigg|_{\tilde{v}_{be}=0} . \tag{2.21}$$

This often relates to the so-called Early effect [3]. Basically, when a positive v_{cb} small-signal is applied, the neutral base thickness decreases slightly because of the applied v_{cb} causes the depletion region in the base-collector junction to expand. Because the base doping is more heavily doped than in the collector, most of the depletion region expansion occurs in the collector. Nonetheless, a finite portion of the depletion expansion also occurs in the base side. However, similar characteristics are hardly observed in HBTs because the base doping in HBTs is more heavily doped, unlike in Si BJTs, whose base doping has to be lighter than its emitter doping. Therefore, the reduction in the neutral base thickness is simply too small to cause a noticeable amount of increase in collector current. We therefore can approximate y_{ec} as zero for HBTs:

$$y_{ec} \approx 0 . \tag{2.22}$$

2.2.4 Derivation of y_{cc}

y_{cc} is equal to the partial derivative of i_c with respect to v_{cb} when V_{BE} is kept constant. From (2.3), y_{cc} is

$$y_{cc} = \frac{\tilde{i}_c}{\tilde{v}_{cb}}\bigg|_{\tilde{v}_{be}=0} . \tag{2.23}$$

As the discussion of y_{ec}, there is a small change in i_c due to the Early effect when v_{cb} is

varied. Unlike i_e, however, i_c includes another component in addition to the Early effect as shown in Fig. 2.3. It is the current component associated with charging up the base-collector junction capacitance (C_{jc}). If we neglect the contribution from the Early effect, y_{cc} is approximated as

$$y_{cc} = jwC_{jc} . \tag{2.24}$$

2.3 Common-Emitter y-Parameters of Intrinsic HBT

From the derivation of common-base y-parameters of intrinsic HBT in Sec 2.2, we arrive at

$$\begin{bmatrix} y_{ee} & y_{ec} \\ y_{ce} & y_{cc} \end{bmatrix}_b = \begin{bmatrix} g_e\left[1 + jm\frac{w}{w_0}\right] + jwC_{je} & 0 \\ -\alpha_{T0}g_e\left[1 - j(1-m)\frac{w}{w_0} - j\frac{w\tau_m}{2}\right] & jwC_{jc} \end{bmatrix}. \tag{2.25}$$

The value of m used here is a fitting parameter and is generally 2/3, as derived. To obtain a better fit, sometimes m is varied between 0 and 1. The common-emitter y-parameters of intrinsic HBT, y_e, is then derived as

$$y_e = \begin{bmatrix} g_e(1-\alpha_{T0}) + jw\left(C_{je} + C_{jc}\right) + jg_e\left(\frac{w\tau_m}{2} + \frac{w}{w_0}\right) & -jwC_{jc} \\ \alpha_{T0}g_e\left[1 - j(1-m)\frac{w}{w_0} - j\frac{w\tau_m}{2}\right] - jwC_{jc} & jwC_{jc} \end{bmatrix}. \tag{2.26}$$

By using the circuit transformation with only one dependent current source shown in Fig. 2.4, we can build the well-known hybrid-π equivalent circuit of HBTs. Using y_e given in (2.25) or (2.26), the branch elements is found as

$$y_{11e} + y_{12e} = \frac{g_e}{\beta_{dc}} + jw\left(C_{je} + \frac{g_e}{w_0}\right) + jg_e\frac{w\tau_m}{2}, \tag{2.27}$$

$$-y_{12e} = jwC_{jc}, \tag{2.28}$$

$$y_{22e} + y_{12e} = 0, \tag{2.29}$$

and

$$y_{21e} - y_{12e} = \alpha_{T0}g_e\left[1 - j(1-m)\frac{w}{w_0}\right]\exp\left(\frac{w\tau_m}{2}\right) \tag{2.30}$$

where β_{dc} is DC current gain. Base on (2.27)-(2.30) and the model shown on Fig. 2.4(a), the common-emitter small-signal equivalent circuit of intrinsic HBTs is constructed as shown in Fig. 2.4(b). In accordance with some commonly used symbol, we replace input resistance β_{dc}/g_e by R_π and a portion of the input capacitance ($C_{je} + g_e/w_0$) by C_π. If we neglect $g_e w\tau_m/2$ in the input capacitance and $\exp(w\tau_m/2)$ in the current generator, then the equivalent circuit becomes identical to the familiar intrinsic hybrid-π small-signal model as shown in the dashed box of Fig. 2.5. In Fig. 2.5, we also added the intrinsic base resistance, R_{bi}, and outer part base-collector capacitance, C_{bcx}, to complete the transistor model. Unlike C_{bci} which models the reverse base-collector capacitance that most of collector current flows, C_{bcx} models the reverse base-collector capacitance that no collector current flows. Outside the dashed box are three extrinsic resistances and three extrinsic inductances.

2.4 A Novel Approach for Parameter Determination of HBT Small-Signal Equivalent Circuits

In this section, we will present a novel approach for parameter determination of HBT small-signal equivalent circuit. Direct parameter extraction is believed to be the most accurate method for equivalent-circuits modeling of HBTs. Using this method, the parasitic elements, followed by the intrinsic elements, are determined analytically. Therefore, the quality of the extrinsic elements extraction plays an important role in the accuracy and robustness of the entire extraction algorithm. This section introduces a novel extraction method for the extrinsic elements, which have been proven to be strongly correlated with the intrinsic elements. By utilizing the specific correlation, the equivalent circuit modeling is reduced to an optimization problem of determining six specific extrinsic elements. Converting the intrinsic equivalent circuit into its common-collector configuration, all intrinsic circuit elements are extracted using exact closed-form equations for hybrid-π equivalent circuits. The modeling results are presented, showing that the proposed method can yield a good fit between the measured and calculated S-parameters.

2.4.1 Hybrid-π equivalent circuit of the HBT transistor

The hybrid-π HBT equivalent circuit used in this study has been introduced in Sec 2.3. Fig. 2.5 shows the equivalent circuit in common-emitter configuration, which is divided into two parts. The intrinsic part shown within the dashed box excludes the elements R_E, L_E, R_B, L_B, R_C, and L_C and contains most bias-dependent elements.

Figure 2.6 shows the Y_{int} in the common-collector configuration. The respective ABCD-parameters, A_{int}, are described as [2]

$$A_{\text{int}} = \begin{bmatrix} A_{c,11} & A_{c,12} \\ A_{c,21} & A_{c,22} \end{bmatrix} \tag{2.31}$$

where

$$A_{c,11} = 1 + R_{bi}Y_{bc}\,, \tag{2.32}$$

$$A_{c,12} = \frac{1}{G_m + Y_\pi}\left(1 + R_{bi}Y_{bc} + R_{bi}Y_\pi\right), \tag{2.33}$$

$$A_{c,21} = Y_{bc} + Y_{ex} + R_{bi}Y_{ex}Y_{bc}\,, \tag{2.34}$$

and

$$A_{c,22} = \frac{1}{G_m + Y_\pi}\left[Y_{ex}\left(1 + R_{bi}Y_{bc} + R_{bi}Y_\pi\right) + Y_{bc} + Y_\pi\right] \tag{2.35}$$

with

$$Y_{bc} = \frac{1}{R_{bci}} + jwC_{bci}\,, \tag{2.36}$$

$$Y_\pi = \frac{1}{R_\pi} + jwC_\pi\,, \tag{2.37}$$

$$Y_{ex} = jwC_{bcx}\,, \tag{2.38}$$

and

$$G_m = G_{m0}\exp\left(-jw\tau_\pi\right). \tag{2.39}$$

The extrinsic part of the HBT, located outside Y_{int}, is related to Y_{int} through the following equations:

$$Z_{\text{int}} = Z_{meas} - Z_{ext} \tag{2.40}$$

and

$$Z_{ext} = \begin{bmatrix} R_E + R_B + jw(L_E + L_B) & R_E + jw(L_E) \\ R_E + jw(L_E) & R_E + R_C + jw(L_E + L_C) \end{bmatrix} \tag{2.41}$$

where Z_{meas} is the measured Z-parameters.

2.4.2 Analytical Determination of the Equivalent Circuit Elements

Like conventional FET modeling, once the extrinsic elements are known, along with the equivalent circuit shown in Fig. 2.5, the intrinsic elements can be determined analytically. First, the overall S-parameters are converted to Z-parameters, and then the Z-parameters in common-emitter configuration of Y_{int} are obtained using (2.40) and (2.41). After a series of standard network parameter transformations, the ABCD-parameters in common-collector configuration of Y_{int}, A_{int}, are determined.

Consider the $A_{c,11}$ and $A_{c,21}$ shown in (2.32) and (2.34). Re-arranging both equations gives

$$R_{bi} = \frac{A_{c,11} - 1}{Y_{bc}} \tag{2.42}$$

and

$$Y_{ex} = \frac{A_{c,21} - Y_{bc}}{A_{c,11}} \tag{2.43}$$

and, therefore, we obtain

$$\mathrm{Im}\left[R_{bi}\right] = \mathrm{Im}\left[\frac{A_{c,11} - 1}{A_{c,21} - Y_{ex}A_{c,11}}\right] = 0 \tag{2.44}$$

and

$$\mathrm{Re}\left[Y_{ex}\right]=\mathrm{Re}\left[\frac{A_{c,21}R_{bi}-A_{c,11}+1}{A_{c,11}R_{bi}}\right]=0\,. \tag{2.45}$$

Normalizing (2.44) and (2.45), leads to

$$\mathrm{Im}\left[\left(A_{c,11}-1\right)\left(A_{c,21}-Y_{ex}A_{c,11}\right)^{*}\right]=0 \tag{2.45}$$

and

$$\mathrm{Re}\left[\left(A_{c,21}R_{bi}-A_{c,11}+1\right)A_{c,11}^{*}\right]=0\,. \tag{2.46}$$

From the above equations, R_{bi} and Y_{ex} can be determined as

$$R_{bi}=\frac{\mathrm{Re}\left[\left(A_{c,11}-1\right)A_{c,11}^{*}\right]}{\mathrm{Re}\left[A_{c,21}A_{c,11}^{*}\right]} \tag{2.47}$$

and

$$Y_{ex}=\frac{-j\,\mathrm{Re}\left[\left(A_{c,11}-1\right)A_{c,21}^{*}\right]}{\mathrm{Re}\left[\left(A_{c,11}-1\right)A_{c,11}^{*}\right]}, \tag{2.48}$$

respectively. Then, Y_{bc} can be derived as

$$Y_{bc}=\frac{\left(A_{c,11}-1\right)}{R_{bi}}\,. \tag{2.49}$$

The equations for extracting Y_{π} and G_m are listed as

$$Y_{\pi}=\frac{\left|A_{\mathrm{int}}\right|\left(A_{c,11}-1\right)}{R_{bi}\left(A_{c,22}-A_{c,12}Y_{ex}-\left|A_{\mathrm{int}}\right|\right)} \tag{2.50}$$

and

$$G_m = \frac{(1-|A_{\text{int}}|)}{|A_{\text{int}}|} Y_\pi . \tag{2.51}$$

The equivalent circuit elements in Y_{int} at each frequency point are derived from (2.48)-(2.51). The detail expressions are given as follows:

$$R_{bc} = \frac{1}{\text{Re}(Y_{bc})}, \tag{2.52}$$

$$R_\pi = \frac{1}{\text{Re}(Y_\pi)}, \tag{2.53}$$

$$C_{bc} = \frac{\text{Im}(Y_{bc})}{w}, \tag{2.54}$$

$$C_\pi = \frac{\text{Im}(Y_\pi)}{w}, \tag{2.55}$$

$$\tau_\pi = \frac{-1}{w} \tan^{-1}\left[\frac{\text{Im}(G_m)}{\text{Re}(G_m)}\right], \tag{2.56}$$

and

$$G_{m0} = \frac{\text{Re}(G_m)}{\cos(w\tau_\pi)} . \tag{2.57}$$

2.4.3 Effect of Extrinsic Elements on Determining Intrinsic Elements

As mentioned in Sec 2.4.2, once extrinsic elements are given, the bias-dependent elements are determined uniquely through (2.47)-(2.51) and (2.52)-(2.57). Notably, at millimeter wave frequency, a slight change in any of the extrinsic elements can lead to drastic changes in some intrinsic elements values. Fig. 2.7 plots the frequency characteristic of C_π with respect to L_C for the bias condition of V_{CE} = 1.5 V and I_B = 600 μA, showing that a small change in L_C, heavily affects the

intrinsic element C_π. Therefore, the intrinsic elements can be written as functions of the extrinsic elements, Z_{ext} and the angular frequency as follows:

$$R_{bi} = f_1\left(w_i, Z_{ext}\right), \tag{2.58}$$

$$C_{bci} = f_2\left(w_i, Z_{ext}\right), \tag{2.59}$$

$$R_\pi = f_3\left(w_i, Z_{ext}\right), \tag{2.60}$$

$$C_\pi = f_4\left(w_i, Z_{ext}\right), \tag{2.61}$$

$$R_{bc} = f_5\left(w_i, Z_{ext}\right), \tag{2.62}$$

and

$$C_{bcx} = f_6\left(w_i, Z_{ext}\right). \tag{2.63}$$

If the extracted intrinsic lumped-circuit elements are valid at each measured frequency, then the elements values show negligible frequency responses. By finding the specific extrinsic elements, R_B, R_C, R_E, L_B, L_C and L_E, minimizing the frequency dependence of intrinsic elements, the equivalent circuit modeling is reduced to an optimization problem.

2.4.4 The Complete Parameter Extraction Algorithm

Figure 2.8 shows the complete parameter extraction algorithm. First procedure, the extrinsic parameters are initialized to their appropriate range determined from open-collector measurements [4], [5], making them close to the physically meaningful minimum of the optimization error function.

Second, the extrinsic elements are optimized so that the intrinsic elements exhibit smaller frequency dependences. The objective function for this condition is presented as

$$E_1^k\left(R_B,R_C,R_E,L_B,L_C,L_E\right)=\frac{1}{N-1}\sum_{i=0}^{N-1}\left|\rho_k f_k\left(w_i,Z_{ext}\right)-\overline{\sum_{j=0}^{N-1}\rho_k f_k\left(w_j,Z_{ext}\right)}\right|^2 \quad (2.64)$$

where k varies from 1 to 6; N denotes the total number of measured frequency points; the over bar denotes the mean values, and ρ_k denotes a normalizing factor to make f_k vary between zero and one.

Furthermore, to refine the modeling results, (2.65) is considered as a loose constraint.

$$E_2^k\left(R_B,R_C,R_E,L_B,L_C,L_E\right)=\sum_{p=1}^{2}\sum_{q=1}^{2}\sum_{i=0}^{N-1}W_{pq}\left|S_{pq}^c\left(w_i,Z_{ext}\right)-S_{pq}^m\left(w_i,Z_{ext}\right)\right|^2 \quad (2.65)$$

where the superscripts c and m denote the calculated and measured S-parameters, respectively, and W_{pq} denotes the weighting factor of S_{pq}. The mean values of intrinsic elements are used for computing S_{pq}^c. The extended error vector then comprises

$$\varepsilon\left(w_i,R_B,R_C,R_E,L_B,L_C,L_E\right)=\begin{bmatrix}\sum_{k=1}^{6}E_1^k\left(R_B,R_C,R_E,L_B,L_C,L_E\right)\\ E_2^k\left(R_B,R_C,R_E,L_B,L_C,L_E\right)\end{bmatrix}. \quad (2.66)$$

Initially, the values of extrinsic parameters R_B, R_C, R_E, L_B, L_C and L_E are selectively assigned from the first procedure. All the parameters within Y_{int}, are evaluated from (2.56)-(2.63). Then, the process is conducted iteratively to obtain the lowest possible error vector value from (2.66). If the error vector (2.66) is below the designed error criteria, the extrinsic and intrinsic elements are extracted, completing the equivalent circuit modeling.

2.5 Results and Discussions

To validate and assess the accuracy of the proposed extraction method, several 4×20 μm^2 InGaP/GaAs common emitter HBT devices fabricated in-house [6] were investigated. The measurements were performed with a HP8510C network analyzer and Cascade Microtech probes with a frequency sweep from 1 GHz to 20 GHz. The flowchart depicted in Fig. 2.8 was implemented on Agilent IC-CAP.

Figure 2.9 compares the measured and calculated S-parameters for the bias point at V_{CE} = 1.5 V, I_C = 17.3 mA, and I_B = 300 μA. There was good agreement between the results. Table 2.1 gives the small-signal model parameter's values for some bias points can be correlated to the physical principle of HBT operation. C_{bcx} models the extrinsic component of base-collector junction capacitances where the collector current flow is negligible. For HBT's biasing in the forward active mode, the base-collector junction is reverse-biased, and the diffusion capacitance is negligible. The slight decrease in (C_{bcx} + C_{bci}) with increasing I_C is attributed to the current-induced broadening of the base/collector depletion layer, and to the variation of space charge with V_{CB} due to electron velocity modulation [7]. The intrinsic base resistance R_{bi} splits the base-collector capacitance into intrinsic (C_{bci}) and extrinsic components (C_{bcx}). The reduction of R_{bi} at higher currents is caused by emitter current crowding [8]. The dynamic resistance R_π models the variation in the emitter current resulting from base-emitter voltage changes. The reduction in R_π with increasing I_B follows the inverse current relationship $R_\pi = \beta_{dc}\eta kT/qI_E$. The reduction of the base-collector resistance R_{bc} may be due to the Early effect.

The base-emitter capacitance C_π includes the terms related to the base-emitter junction depletion capacitance and the base-emitter diffusion capacitance. Since the base-emitter junction depletion capacitance does not vary much with V_{BE} [8], the

increase in C_π is mainly contributed by the base-emitter diffusion capacitance. The diffusion capacitance is the variation in the minority carrier charge in the quasi-neutral emitter and in the quasi-neutral base with respect to the change in V_{BE}. As I_C increases (i.e. V_{BE} increases), the minority carrier both in the emitter and base region also increases. Therefore, C_π increase as I_C increases.

2.6 Summary

This chapter discusses the origin of small-signal equivalent circuit of III-V HBTs and also presents a novel extraction method for the small-signal modeling of III-V HBTs. In the derivation of small-signal equivalent circuit, we start from the examination of its physical phenomena in common-base configuration. Through the transformation between common-base and common-emitter configuration, the commonly used hybrid-π small signal equivalent circuit of HBTs is obtained. Assuming that the equivalent circuit is valid over the whole frequency range of the measurements, the extrinsic elements are iteratively determined by minimizing the variance of the intrinsic elements as an optimization criterion. The proposed method leads to a good fit between the measured and calculated S-parameters.

Table 2.1 Extracted model parameters for the bias condition of V_{CE} = 1.5 V and I_B = 300 μA, 400 μA, 500 μA and 600 μA.

Hybrid-π Topology	I_C = 17.3 mA I_B = 300 μA	I_C = 24 mA I_B = 400 μA	I_C = 31.7 mA I_B = 500 μA	I_C = 40 mA I_B = 600 μA
L_B (pH)	26.36	26.2	26.4	26.5
L_C (pH)	12.93	12.8	12.91	12.74
L_E (pH)	12.81	12.74	12.8	12.3
R_B (Ω)	5.71	5.6	5.647	5.75
R_C (Ω)	6.096	6.0	5.852	6.1
R_E (Ω)	5.772	5.7	5.801	5.724
C_{bcx} (fF)	76.39	76.21	77.38	77.42
C_{bci} (fF)	39.96	34.77	31.88	31.29
C_π (pF)	2.632	3.113	3.428	3.631
R_{bi} (Ω)	11.1	8.474	7.308	6.259
R_π (Ω)	103.9	78.34	58.49	45.32
R_{bc} (kΩ)	79.98	72.98	64.87	55.54
G_{m0} (S)	0.481	0.643	0.8047	0.979
τ_π (ps)	2.395	2.033	1.735	1.482

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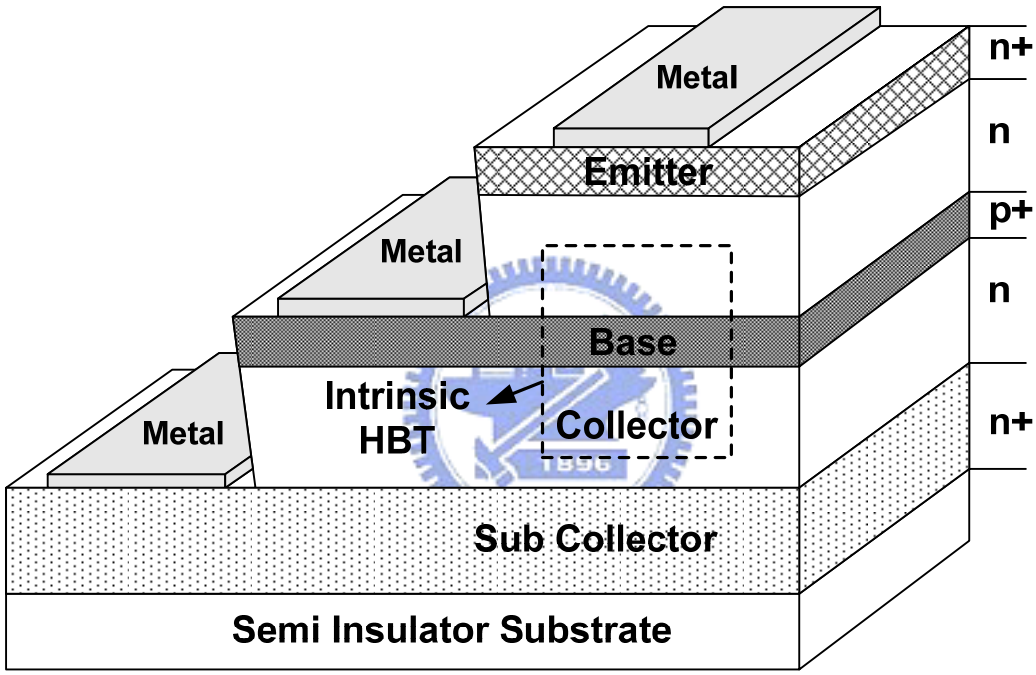


Fig. 2.1 Cross section of III-V HBTs.

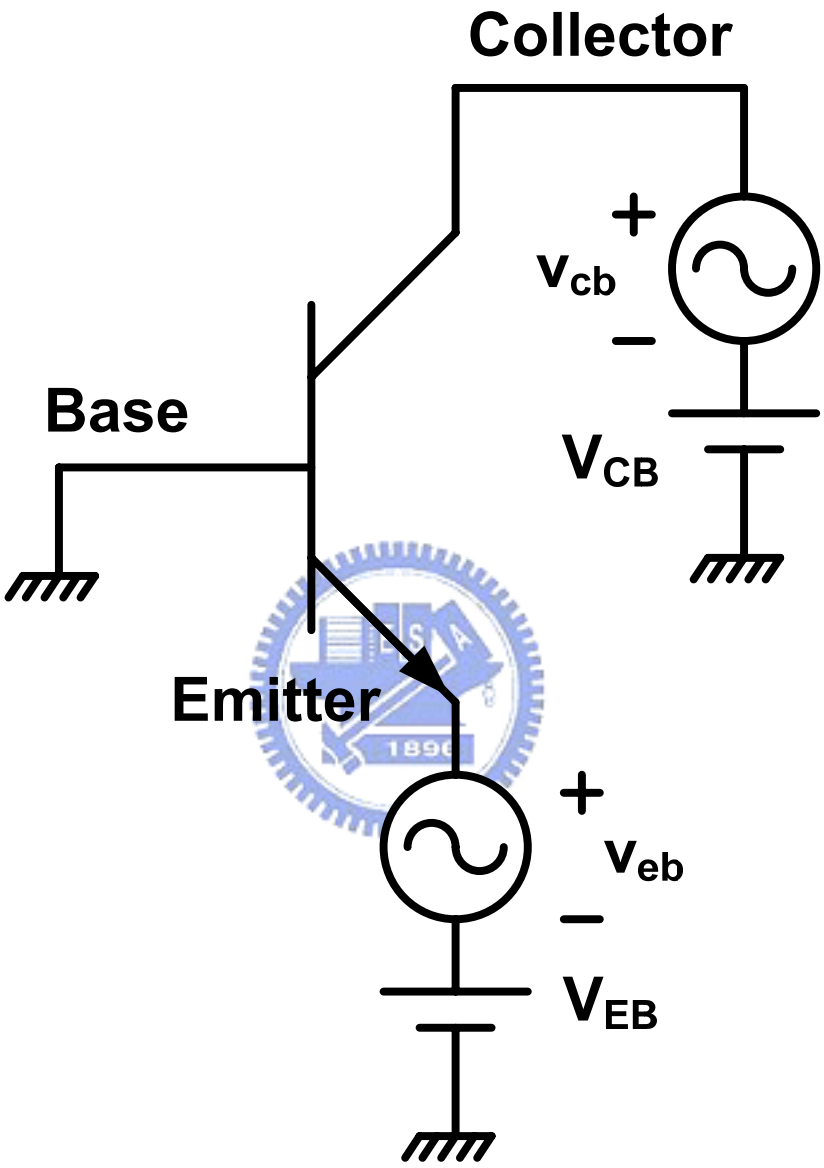


Fig. 2.2 HBTs biased in the common-base configuration.

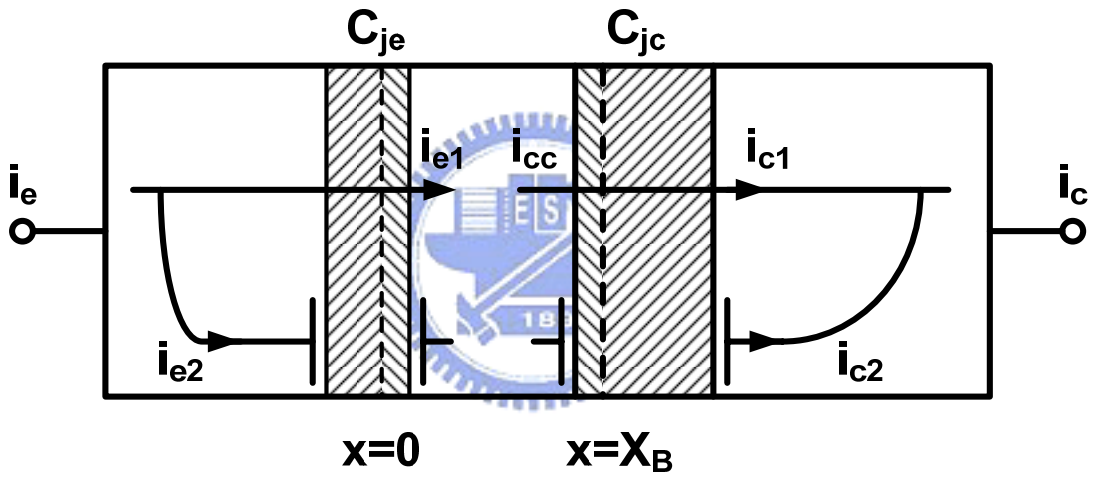
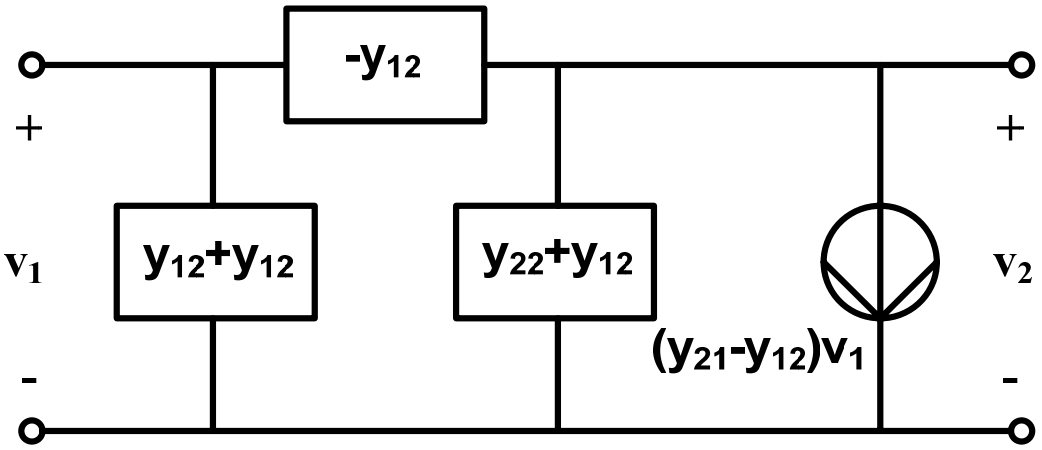
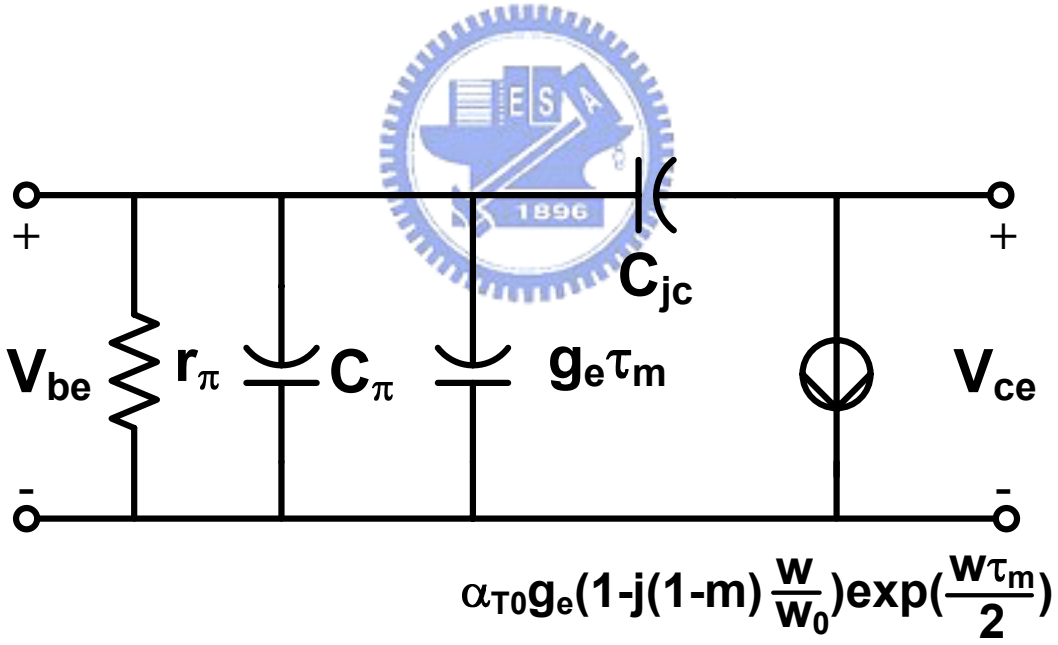


Fig. 2.3 Schematic diagram of the small-signal current flows biased in the common-base configuration.



(a)



(b)

Fig. 2.4 (a) Two-port circuit representation using Y-parameters. (b) A small-signal HBT model based on the circuit representation of Fig. 2.4(a).

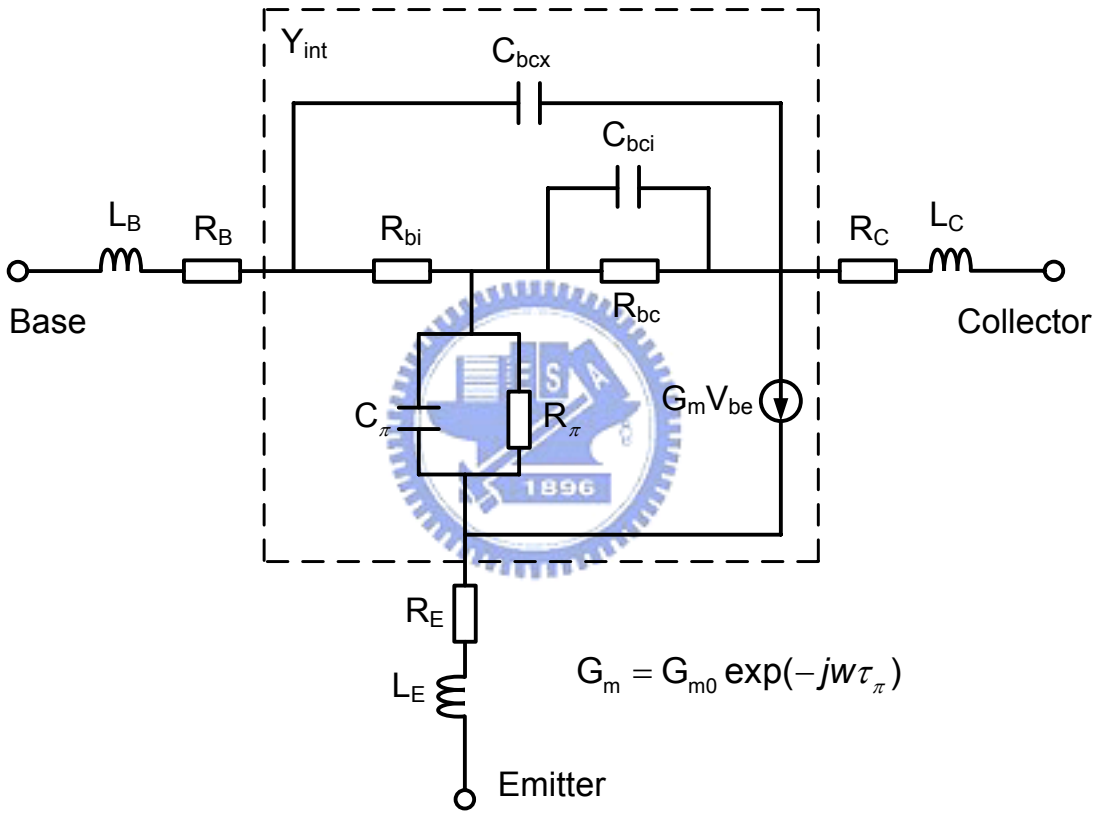


Fig. 2.5 Small-signal equivalent circuit of III-V HBTs.

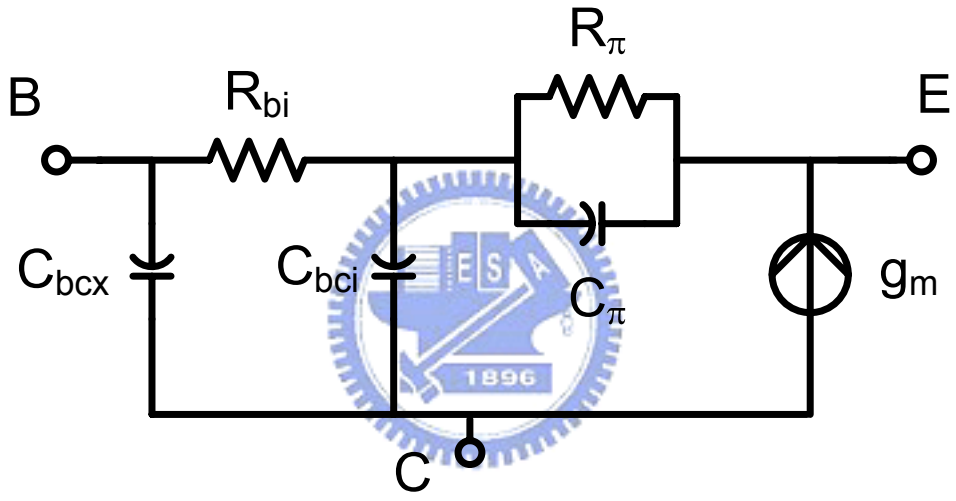


Fig. 2.6 Small-signal equivalent circuit model of intrinsic III-V HBT in common collector configuration.

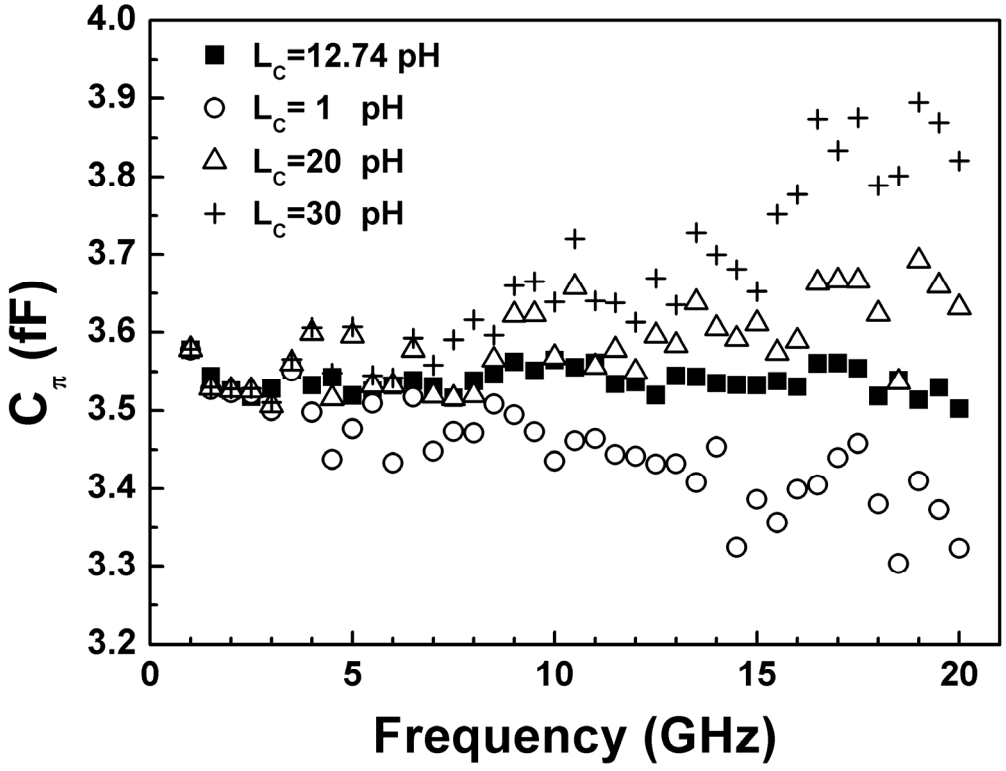


Fig. 2.7 Frequency characteristics of the intrinsic π-topology parameter C_π with L_C as parameter. The HBT is biased at V_{CE} = 1.5 V, I_B = 600 μA and I_C = 40 mA.

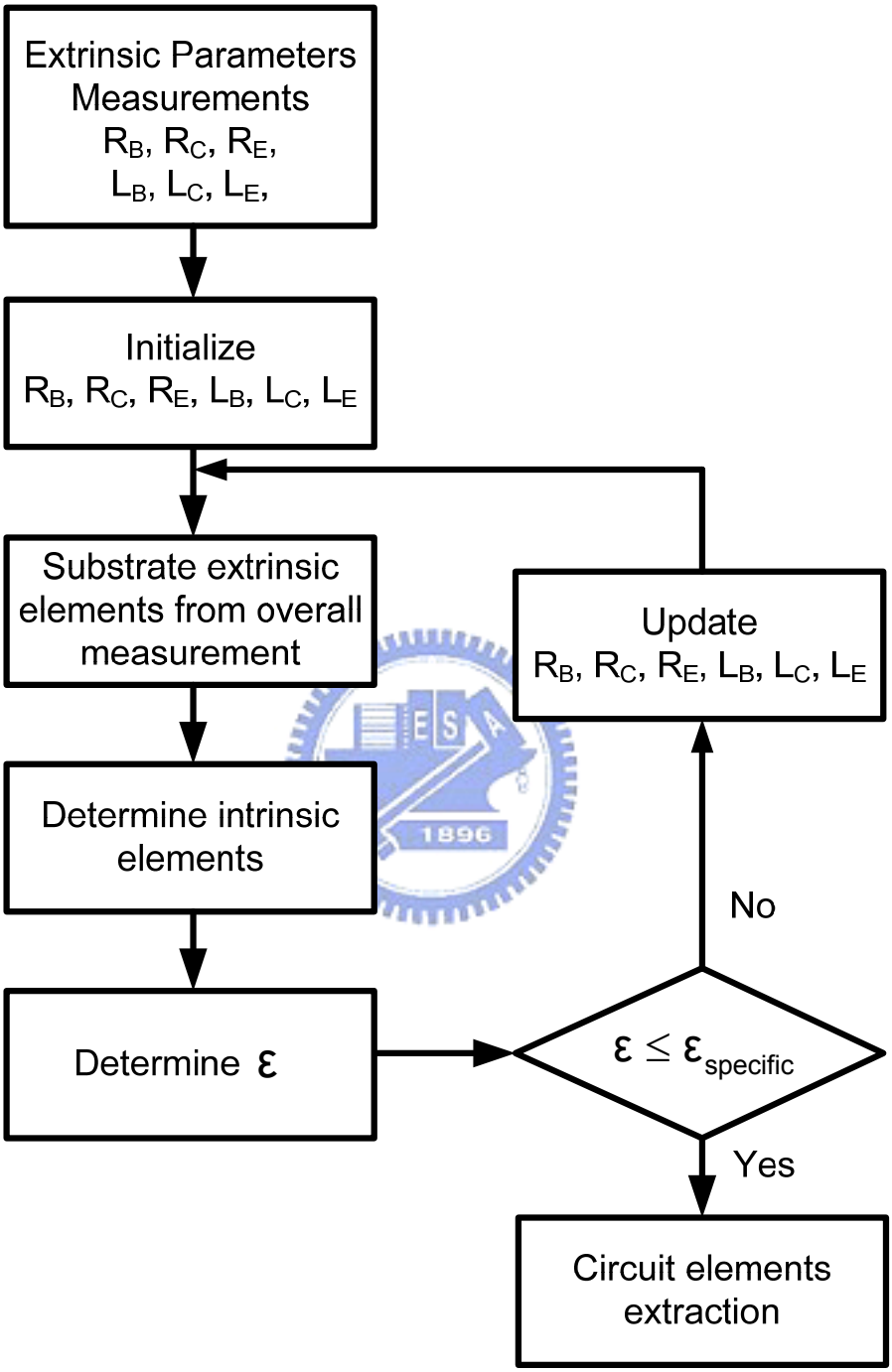


Fig. 2.8 Complete parameter extraction algorithm of proposed method.

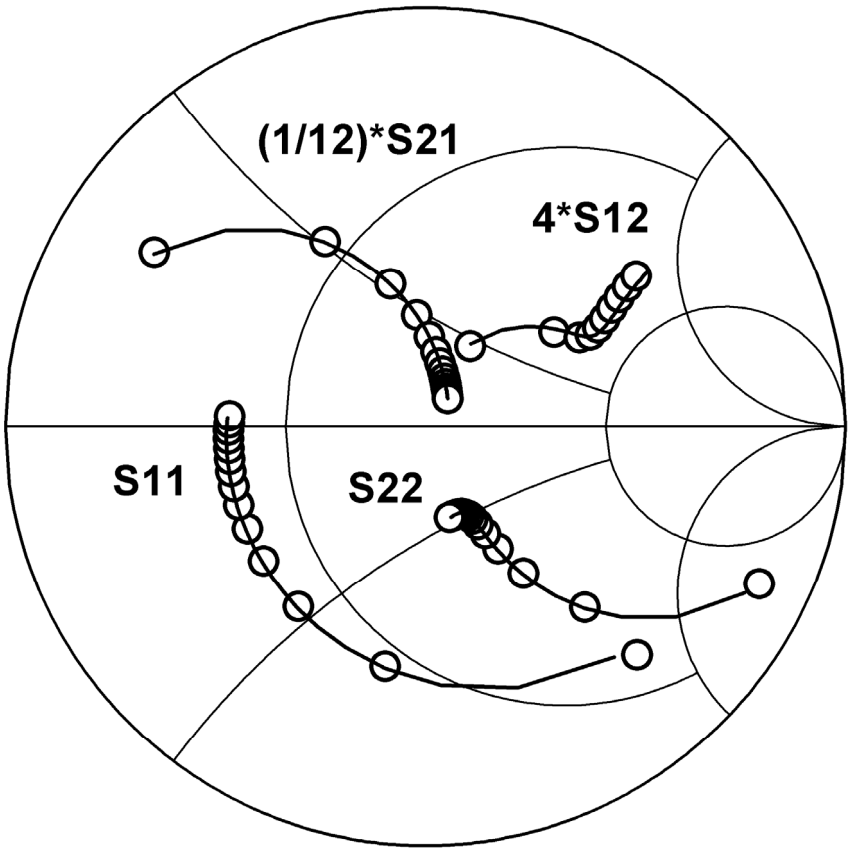


Fig. 2.9 Comparison of the measured and calculated S-parameters for the bias point at V_{CE} = 1.5 V, I_C = 17.3 mA, and I_B = 300 μA.

Chapter 3

Small-Signal Modeling of SiGe HBTs

3.1 Introduction of Small-Signal modeling of SiGe HBTs

SiGe heterojunction bipolar transistors (HBTs) were first demonstrated in the late 1980s [1] and quickly become popular in wireless communication applications, in the form of wireless transceiver circuits [2], [3], due to the higher performance than Si devices and higher integration level than III-V devices. An accurate extraction method for small-signal equivalent circuit of SiGe HBTs is vital for designing a circuit, evaluating the process technology and optimizing device performance. Recently, several papers have reported small-signal equivalent-circuit parameter-extraction methods for SiGe HBTs [4]-[7] in which the substrate effects have been taken into account. Johansen et al. describe in [4] a direct substrate network parameter extraction technique where feedback signal through the internal circuit elements was neglected. The S-parameters measured with only collector port connected was used in [5], allowing a direct parameter extraction of a three-element substrate network. An alternative parameter extraction approach for substrate network of SiGe HBTs was also proposed in [6], in which the collector-substrate depletion capacitance was directly extracted from measured $\mathrm{Im}(Y_{22}+Y_{21})/\omega$ at low frequency and the substrate resistance and substrate capacitance were extracted from two analytical equations under certain assumption. Finally, Lee et al. proposed a parameter extraction approach [7], in which a new collector-substrate parasitic capacitance was used accounting for the parasitic capacitance arising from the open-short de-embedding procedure.

Most of these extraction techniques for the substrate network were based on the

use of frequency behavior of ($Y_{22}+Y_{21}$). However, we found that the feedback signal through the internal circuit elements makes ($Y_{22}+Y_{21}$) deviate from the admittance of substrate network and the modeling results may have no physical meaning if the parameters extraction of substrate network is directly performed on the measured ($Y_{22}+Y_{21}$). Therefore, to extract the substrate network parameters, the intrinsic circuit elements of SiGe HBTs should be determined first.

In this chapter, we present a simple and accurate parameter-extraction method of a high-frequency small-signal SiGe HBTs model and an improved extraction method of substrate network parameters. The equivalent circuit adopted in this study is based on the hybrid-π topology which is popular in commercial circuit simulators such as VBIC, MEXTRAM, and HICUM. Based on the algorithm proposed in [8], [9], this paper expands the essence of the extraction technique in hybrid-π topology HBT small-signal modeling. Since the intrinsic base resistance is involved in the extraction of some intrinsic circuit parameters, an accurate extraction of the resistance is important to avoid any accumulated errors. Two formulas to determine the intrinsic base resistance are presented followed by an accuracy improvement procedure to achieve a better accuracy of the extraction results. All the circuit elements are extracted directly from measured S-parameter without any pre-knowledge or numerical optimization. In the extraction of substrate network parameters, we extract the intrinsic circuit parameters first to erase the influence of feedback signal through the internal circuit elements. The proposed extraction procedure was experimentally verified on a SiGe HBT in the frequency range 1-30 GHz [10].

3.2 Small-Signal Equivalent Circuit of SiGe HBTs

Figure 3.1 shows the cross section view of a typical SiGe HBT. The intrinsic SiGe HBT which describes the active region under emitter area is similar to that of III-V HBTs. Additionally, SiGe HBTs contain a conductive p^- well which constitutes a substrate network as shown in the dashed box of Fig. 3.1. When performing small-signal modeling of SiGe HBTs, the substrate network should be taken into consideration or we can't get good modeling results in higher frequency range.

Figure 3.2 shows the complete small-signal equivalent circuit of SiGe HBTs under forward active mode operation. A three-element substrate network is applied in the equivalent circuit. The C_{sub} describes the depletion capacitance between n^+ sub collector and p^- well region. The effective substrate resistance, R_{bk} and effective bulk capacitance, C_{bk} is accounted for the dielectric behavior. According to the simulation results in [11], the applied three-element substrate network is very simple and can roughly be applied in the frequency region below 20 GHz. In fact, to be more accurate, there are two substrate networks, one attached to the bottom of the buried-layer of the transistor, another attached to the periphery. But the extraction of two substrate networks is very difficult, especially due to the limited accuracy of measured S-parameters at very high frequencies. Therefore, we apply the three-element substrate network in our study as a tradeoff between the modeling complexity and the modeling efficiency.

The equivalent circuit shown in Fig. 3.2 is divided into two parts, the inner part (in the dashed box) containing the bias-dependent intrinsic elements, and the outer part with the mostly bias-independent extrinsic elements. The three inductances, L_B, L_C and L_E, model the inductance behavior of the metal pad in base, collector and emitter region, respectively. The three resistances, R_B, R_C and R_E, model the resistance behavior of the

region outside the intrinsic HBT. The C_{bep} and C_{bcp} model the parasitic capacitance between the base and emitter spacer region and between base and collector spacer region, respectively.

3.3 Small-Signal Modeling of SiGe HBTs

To extract the equivalent circuit parameters, pad parasitics have to be carefully removed first from measured S-parameters through a de-embedding procedure. Some remaining parasitic not removed in the de-embedding procedure such as parasitic capacitances, pad inductances and series resistances are relatively small, but lead eventually to the errors in extracting intrinsic elements. Thus, their values should be determined carefully. After removing the residual parasitic, the extraction of substrate network parameters and subsequently the intrinsic parameters can then be performed.

3.3.1 Extraction of Extrinsic Elements and Substrate Network Parameters

As reported in [12]-[14], the extraction of parasitic elements is made by biasing the device first in forward operation (high base current I_B) in order to extract the parasitic resistances (R_{bx}, R_c, R_e) and inductances (L_b, L_c, L_e). The device is then biased in the cutoff operation mode (collector voltage V_{CE} = 0 V and reverse and/or low forward base voltage V_{BE}), permitting the extraction of the parasitic capacitances (C_{bep} and C_{bcp}).

Under the bias conditions (V_{BE} = 0 V and forward and/or low reverse collector voltage), the substrate network parameters can be estimated from the Y-parameters analysis of the equivalent circuit shown in Fig. 3.2. After removing the extrinsic

inductances, parasitic capacitances, extrinsic base resistance and collector resistance, the equivalent circuit of Fig. 3.2 is reduced to that of Fig. 3.3(a).

In this study, the substrate network Y_{sub}, is constituted of substrate-collector depletion capacitance C_{sub}, effective substrate resistance R_{bk} and effective bulk capacitance C_{bk} accounting for Si dielectric behavior. For simplicity, the influence of emitter resistance R_e has been neglected where the approximation is valid for $\left(\omega R_e C_\pi\right)^2 \ll 1$. We transform the intrinsic part of the device equivalent circuit (R_{bi}, C_π, C_{bci}) using the well-known T↔Π transformations shown in detail in the right side of Fig. 3.3(b). After the two-port matrix operations, the admittance parameters of $[Y_k]$ shown in Fig. 3.3(b) is obtained as

$$Y_{11,k} = jwC_{bcx} + \frac{jw\left(C_{bci} + C_\pi\right)}{1 + jwR_{bi}\left(C_{bci} + C_\pi\right)}, \tag{3.1}$$

$$Y_{12,k} = Y_{21,k} = -jwC_{bcx} - \frac{jwC_{bci}}{1 + jwR_{bi}\left(C_{bci} + C_\pi\right)}, \tag{3.2}$$

and

$$Y_{22,k} = Y_{sub} + jwC_{bcx} + \frac{jwC_{bci}(1 + jwR_{bi}C_\pi)}{1 + jwR_{bi}(C_{bci} + C_\pi)}. \tag{3.3}$$

From (3.2) and (3.3), we can derive

$$Y_{22,k} + Y_{21,k} = Y_{sub} + Y_3 \tag{3.4}$$

where

$$Y_{sub} = \frac{\omega^2 R_{bk} C_{sub}^2}{1 + \omega^2 R_{bk}^2 \left(C_{bk} + C_{sub}\right)^2} + j\omega C_{sub}\left(\frac{1 + \omega^2 R_{bk}^2 C_{bk}\left(C_{bk} + C_{sub}\right)}{1 + \omega^2 R_{bk}^2 \left(C_{bk} + C_{sub}\right)^2}\right) \tag{3.5}$$

and

$$Y_3 = \frac{-\omega^2 C_{bci} C_\pi R_{bi}}{1+\omega^2 R_{bi}^2 \left(C_{bci}+C_\pi\right)^2} + j\frac{\omega^3 C_{bci} C_\pi \left(C_{bci}+C_\pi\right) R_{bi}^2}{1+\omega^2 R_{bi}^2 \left(C_{bci}+C_\pi\right)^2}. \tag{3.6}$$

From (3.4), it is clear that ($Y_{22,k}+ Y_{21,k}$) deviates from Y_{sub} by an additional term, Y_3, which is constituted of the intrinsic circuit elements. If the extraction of substrate network parameters is performed on $Y_{22,k}+ Y_{21,k}$, the conductance of substrate network will be underestimated and the susceptance of substrate network will be overestimated.

To extract substrate network parameters, Y_3 should be determined first. From (3.1) and (3.2), R_{bi} and C_π can be obtained as

$$R_{bi} = \mathrm{Re}\left[\frac{1}{Y_{11,k}+Y_{12,k}}\right]\frac{\mathrm{Re}(Y_{11,k}+Y_{12,k})}{\mathrm{Re}(Y_{11,k})} \tag{3.7}$$

and

$$\omega C_\pi = -\mathrm{Im}\left(\frac{1}{Y_{11,k}+Y_{12,k}}\right)^{-1}. \tag{3.8}$$

As shown in Fig. 3.4, the R_{bi} extracted from (3.7) is nearly constant and the ωC_π extracted from (4.8) is linear. We find R_{bi} = 19.04 Ω and C_π = 78.97 fF at V_{CE} = 3.0 V, and V_{BE} = 0 V for the 3×0.34×8 μm^2 SiGe HBT. In the low frequency range, Re($Y_{11,k}$) can be approximately rewritten as [15]

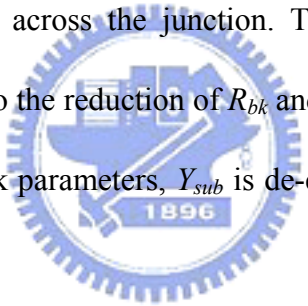
$$\mathrm{Re}(Y_{11,k}) = \frac{\omega^2 R_{bi}\left(C_\pi+C_{bci}\right)^2}{1+\omega^2 R_{bi}^2\left(C_\pi+C_{bci}\right)^2} \sim \omega^2 R_{bi}\left(C_\pi+C_{bci}\right)^2\Big|_{\text{at low frequency}} \tag{3.9}$$

under the assumption, $\omega^2 R_{bi}^2 \left(C_\pi + C_{bci}\right)^2 \ll 1$. A typical result of (3.9) at V_{CE} = 3.0 V, and V_{BE} = 0 V for a 3×0.34×8 μm^2 SiGe HBT is shown in Fig. 3.5 from which the slope is fitted as 1.393×10^{-25}. The intrinsic base-collector capacitance C_{bci} can be extracted as 6.553 fF from $C_{bci} = \beta^{0.5} R_{bi}^{-0.5} - C_\pi$ where β is the slope of Re($Y_{11,k}$) versus ω^2 plot. Substituting extracted values of R_{bi}, C_π and C_{bci} to (3.6), Y_3 is obtained. From (3.4), Y_{sub} is then obtained by removing Y_3 from $Y_{22,k}$ + $Y_{21,k}$. Since the accuracy of extracted C_{bci} will strongly affect on Y_{sub}, it is necessary to check the validation of the extracted values. In this study, the C_{bci} is obtained from the calculation of R_{bi}, C_π and β. The extracted R_{bi} is frequency independent as shown in Fig. 3.4(a). The extracted C_π is collector voltage independence and is equal to the Im(Y_{11} + Y_{12})/ω - C_{bep} at low frequency. Since, Re($Y_{11,k}$) under cutoff mode operation has been widely used in [15]-[17], we believe β can be extracted accurately. Therefore the extracted C_{bci} is reliable.

Figure 3.6 shows the comparison between measured ($Y_{22,k}$ + $Y_{21,k}$) and Y_{sub} for a 3×0.34×8 μm^2 SiGe HBT biased at V_{BE} = 0 V and V_{CE} = 0, 3 V. Due to the internal feedback signal through Y_3, Re($Y_{22,k}$ + $Y_{21,k}$) and Im($Y_{22,k}$ + $Y_{21,k}$)/ω show a deviation from Re(Y_{sub}) and Im(Y_{sub})/ω as operation frequency beyond 5 GHz and 10 GHz, respectively. As shown in Fig. 3.7, a negative value of Re($Y_{22,k}$ + $Y_{21,k}$) can also be found in the SiGe HBTs with emitter width larger than 0.5 μm. This indicates that Y_3 (or intrinsic circuit elements) indeed affects the measured ($Y_{22,k}$ + $Y_{21,k}$). If the extraction of substrate network parameters is directly performed on $Y_{22,k}$ + $Y_{21,k}$, a negative effective substrate resistance will be extracted and the modeling results of substrate network may contribute error in the extraction of intrinsic circuit elements.

After obtaining Y_{sub} from (3.4), C_{sub}, R_{bk} and C_{bk} can be determined by the previously reported method [5], [15]. Fig. 3.8 shows the collector-voltage dependence of the extracted substrate network parameters. The solid line shown in Fig. 3.8 is the empirical fitting for C_{sub} by the equation, $C_{sub} = C_{sub,p} + C_{sub,0}\left(1 - V_{ce}/V_{sci}\right)^{-m_{sc}}$, and the fitting value are 10.83 fF, 9.54 fF, 0.702 V and 0.47 for $C_{sub,p}$, $C_{sub,0}$, V_{sci}, and m_{sc}, respectively.

To explain the bias dependence of R_{bk} and C_{bk}, a simple N^+-P junction shown in Fig. 3.9 is used to represent the collector-substrate junction of SiGe HBTs. When the collector voltage increases, the collector-substrate depletion width, W_{sub}, increases due to an increasing reverse bias across the junction. Therefore, the width of neutral region, W_{bk}, reduces, leading to the reduction of R_{bk} and the increase of C_{bk} [18]. After extraction of substrate network parameters, Y_{sub} is de-embedded through the standard two-port operation.



3.3.2 Extraction of Intrinsic Circuit Elements

Usually, the admittance parameters of the intrinsic HBT in common-emitter configuration, $[Y_n]$ are used to extract intrinsic circuit elements [19], [20]. A much simpler set of equations is obtained, if the equivalent circuit of the intrinsic HBT is transformed to its common-collector configuration as shown in Fig. 3.10 [8], [9]. After two-port matrix operations, we arrive at the following ABCD-parameters $[A_c]$ of the intrinsic HBT

$$A_{c,11} = 1 + R_{bi}Y_{bc}\,, \tag{3.10}$$

$$A_{c,12} = \frac{1}{g_m + Y_\pi}\left(1 + R_{bi}Y_{bc} + R_{bi}Y_\pi\right), \tag{3.11}$$

$$A_{c,21} = Y_{bc} + Y_{ex} + R_{bi}Y_{ex}Y_{bc}, \tag{3.12}$$

and

$$A_{c,22} = \frac{1}{g_m + Y_\pi}\left[Y_{ex}\left(1 + R_{bi}Y_{bc} + R_{bi}Y_\pi\right) + Y_{bc} + Y_\pi\right] \tag{3.13}$$

where $g_m = g_{m0}\exp\left(-j\omega\tau\right)$, $Y_\pi = 1/R_\pi + j\omega C_\pi$, $Y_{bc} = j\omega C_{bci}$, and $Y_{ex} = j\omega C_{bcx}$. The advantage of transforming the intrinsic circuit into its common-collector configuration is that some circuit parameters such as g_m and Y_π only appear in $A_{c,12}$ and $A_{c,22}$ and this facilitates the extraction of some intrinsic circuit parameters.

3.3.3 Extraction of of R_{bi}, C_{bci}, C_π, and C_{bcx}

From (3.11) and (3.13), the well-known ABCD-parameter formulation for extraction of intrinsic base resistance, R_{bi}, given in [8] is shown as

$$\mathrm{Re}\left(\frac{A_{c,12}}{A_{c,22}}\right) = \frac{\omega^2 R_{bi}\left(C_{bci} + C_\pi\right)^2}{\omega^4 R_{bi}^2 C_{ex}^2\left(C_{bci} + C_\pi\right)^2 + \omega^2\left(C_{bci} + C_\pi + C_{ex}\right)^2}. \tag{3.14}$$

Since the ω^4 term in denominator is much small than the ω^2 term at middle to high frequency range, (3.14) is simplified to

$$\mathrm{Re}\left(\frac{A_{c,12}}{A_{c,22}}\right) \sim R_{bi}\frac{\left(C_{bci} + C_\pi\right)^2}{\left(C_{bci} + C_\pi + C_{ex}\right)^2}\Bigg|_{\text{at middle to high frequency}} \tag{3.15}$$

which set up the lower limit of R_{bi}. Another equation for extraction of R_{bi} can be obtained from (3.10) to (3.13)

$$\begin{aligned}\mathrm{Re}\left(\frac{A_{c,12}}{|A_c|}\right) &= R_{bi}\left(1+\frac{C_{bci}}{C_\pi}\right)+\frac{1}{\omega^2 R_\pi C_\pi^2} \\ &\sim R_{bi}\left(1+\frac{C_{bci}}{C_\pi}\right)\Big|_{\text{at middle to high frequency}}\end{aligned} \tag{3.16}$$

where $|A_c|$ denotes ($A_{c,11}A_{c,22} - A_{c,12}A_{c,21}$). It is clear that (3.16) set up the upper limit of R_{bi}. Typical results of (3.15) and (3.16) are shown in Fig. 3.11. We find the lower limit and upper limit of R_{bi} are 18.15 Ω and 16.35 Ω, respectively, at I_B = 7.915 μA, I_C = 1.332 mA and V_{CE} = 3.0 V for the 3×0.34×8 μm^2 SiGe HBT. The R_{bi} estimated from (3.15) is then applied to obtain intrinsic base-collector capacitance, C_{bci}, through following equation

$$\mathrm{Im}\left(A_{c,11}\right) = \omega R_{bi} C_{bci}\,. \tag{3.17}$$

The value of $R_{bi}C_{bci}$ is calculated from the slope of (3.17) when plotted versus the angular frequency ω as shown in Fig. 3.12. It should be noted that the adopted R_{bi} from (3.15) only serve as an initial value and it will be corrected in the accuracy improvement procedure.

By examing (3.10) to (3.13), we can extract intrinsic base-emitter capacitance, C_π, through following equation

$$\begin{aligned}\mathrm{Im}\left(\frac{A_{c,12}}{|A_c|}\right) &= \frac{\omega \mathrm{R}_\pi C_{bci} R_{bi} - \omega \mathrm{R}_\pi^2 C_\pi}{1+\left(\omega \mathrm{R}_\pi C_\pi\right)^2} \\ &\sim \frac{-1}{\omega \mathrm{C}_\pi}\left(1-\frac{R_{bi}}{R_\pi}\frac{C_{bci}}{C_\pi}\right)\Big|_{\text{at middle to high frequency}}\,, \\ &\sim \frac{-1}{\omega \mathrm{C}_\pi}\Big|_{\text{at middle to high frequency}}\end{aligned} \tag{3.18}$$

The value of C_π is calculated from the slope of (3.18) when plotted versus 1/ω, as

shown in Fig. 3.13.

To extract the extrinsic base-collector capacitance, C_{bcx}, we obtain following equation by inspecting (3.10) and (3.12)

$$\mathrm{Im}\left(\frac{A_{c,11}}{A_{c,21}}\right)=\frac{\omega^3 R_{bi}^3 C_{bci}^2 C_{bcx}-\omega\left(C_{bci}+C_{bcx}\right)}{\omega^4\left(R_{bi}C_{bci}C_{bcx}\right)^2+\omega^2\left(C_{bci}+C_{bcx}\right)^2}. \tag{3.19}$$

In the low to middle frequency range, the ω^4 term in denominator is much smaller than the ω^2 term. Also, the ω^3 term in numerator is much smaller than the ω term. Thus, (19) is simplified to

$$\mathrm{Im}\left(\frac{A_{c,11}}{A_{c,21}}\right)\sim\left.\frac{-1}{\omega\left(C_{bci}+C_{bcx}\right)}\right|_{\text{at low to middle frequency}}. \tag{3.20}$$

The value of $C_{bci}+C_{bcx}$ is calculated from the slope of (3.20) when plotted versus $1/\omega$, as shown in Fig. 3.14. Since the value of C_{bci} has been previously determined, C_{bcx} is obtained by subtracting $C_{bci}+C_{bcx}$ from C_{bci}.

3.3.4 Accuracy Improvement of R_{bi}, C_{bci} and C_{bcx}

In (3.17) and (3.20), we found that R_{bi} plays a significant role on the accuracy of extracted C_{bci} and subsquentlly the accuracy of extracted C_{bcx}. However, the estimated value of R_{bi} from (3.15) is lower than the real one. Thus, an accuracy improvement procedure is necesarry and listed as follows:

(1) As mentioned in Sec 3.3.3, the value of R_{bi} estimated from (3.15) is applied in the extraction of C_{bci} through (3.17). The extraction result of C_{bci} is used in the

extraction of C_{bcx} through (3.20).

(2) The new lower limit and new upper limit of R_{bi} is obtained by taking extracted C_{bci} and C_{bcx} in the calculation of (3.21) and (3.22), respectively.

$$R_{bi}\big|_L = \frac{\left(C_{bci}+C_\pi+C_{bcx}\right)^2}{\left(C_{bci}+C_\pi\right)^2} \times \mathrm{Re}\left(\frac{A_{c,12}}{A_{c,22}}\right)\Big|_{\text{at middle to high frequency}}. \tag{3.21}$$

$$R_{bi}\big|_U = \left(1+\frac{C_{bci}}{C_\pi}\right)^{-1} \times \mathrm{Re}\left(\frac{A_{c,12}}{|A_c|}\right)\Big|_{\text{at middle to high frequency}}. \tag{3.22}$$

The calculated $R_{bi}\big|_L$ is sent back to step (1) to repeat the calculation to step (2). Once the the difference between $R_{bi}\big|_L$ and $R_{bi}\big|_U$ is minimum, $R_{bi}\big|_L$ is treated as the final R_{bi}. A typical result of proposed accuracy improvement procedure for the 3×0.34×8 μm^2 SiGe at I_B = 7.915 μA, I_C = 1.332 mA and V_{CE} = 3.0 V, is shown in Table I. The difference between $R_{bi}\big|_L$ and $R_{bi}\big|_U$ decreases very quickly in the first four iterations. The extracted R_{bi}, C_{bci}, and C_{bcx} are found to be 17.873 Ω, 4.55 fF, and 15.26 fF, respectively.

3.3.5 Extraction of R_π, g_{m0} and τ

The remaining unknowns are intrinsic transconductance, g_{m0}, excess phase delay, τ, and base-emitter resistance, R_π which can be calculated as follows:

$$\frac{1}{R_\pi} = \mathrm{Re}\left(\frac{A_{c,11}|A_c|}{A_{c,12}-|A_c|R_{bi}}\right). \tag{3.23}$$

The value of R_π is estimated as 2.922 kΩ at I_B = 7.915 μA, I_C = 1.332 mA and V_{CE} =

3.0 V for the 3×0.34×8 μm^2 SiGe HBT, as shown in Fig. 3.15.

The transconductance, g_{m0}, and the excess phase delay, τ, is calculated as follows:

$$g_m = \frac{1-|A_c|}{|A_c|} Y_\pi , \tag{3.24}$$

$$g_{m0} = \sqrt{\mathrm{Re}(g_m)^2 + \mathrm{Im}(g_m)^2} , \tag{3.25}$$

and

$$\tau = -\tan^{-1}\left(\frac{\mathrm{Im}(g_m)}{\mathrm{Re}(g_m)}\right) \times \frac{1}{\omega}. \tag{3.26}$$

Fig. 3.16 shows the extracted results for the 3×0.34×8μm^2 SiGe HBT biased at I_B = 7.915 μA, I_C = 1.332 mA and V_{CE} = 3.0 V. The extracted g_{m0}, and τ are 50.31 mS and 1.709 psec, respectively. Both of g_{m0}, and τ are found to be nearly constant in the interested frequency range.

3.4 Results and Discussions

The proposed direct extraction method was applied to determine the parameters of the test devices, which were multifingered SiGe HBTs fabricated by 0.35-μm BiCMOS technology [10]. The DUT has three fingers and the emitter width and emitter length are 0.34 μm and 8 μm, respectively. Typical cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are about 23 GHz and 40 GHz, respectively. S-parameters are measured in the common emitter configuration using on-wafer RF probes and an HP 8510C vector network analyzer. The initial calibration was performed on a separate ceramic calibration substrate using a SOLT calibration

method.

Figure 3.17 shows the comparisons between the measured and calculated S-parameters for V_{CE} = 2 V, V_{BE} = 0.8 V which is the worst fit in the test bias conditions. Good agreements over the whole frequency range were obtained. Table II give the small-signal model parameters' values for the extracted bias-dependent and bias-indepedent elements. The residual discrepancies calculated by the error function [7], [21] is 0.752%. Therefore, we believe that the proposed method is an accurate extraction technique applicable to evaluate the process technology and optimize the transistor design.

3.5 Summary

In this chapter, an improved extraction technique for the small-signal modeling of SiGe HBTs is proposed. Differing from other methods, this technique considers the internal feedback signal through intrinsic circuit elements when extracting the substrate network parameters. Without this, we may extract negative effective substrate resistance in large area SiGe HBTs since the measured Re(Y_{22} + Y_{21}) is negative due to the interaction of intrinsic circuit elements. Transforming the intrinsic equivalent circuit into its common-collector configuration, all the circuit elements are extracted directly without using any optimization. Two formulas of intrinsic base resistance (R_{bi}) are presented, followed by an accuracy improvement procedure to obtain better accuracy of the intrinsic base-collector capacitance (C_{bci}) and extrinsic base-collector capacitance (C_{bcx}). Simplified formulas to determine base-emitter

resistance (R_π), base-emitter capacitance (C_π), transconductance (g_m) and excess phase delay (τ) are presented. The measured and calculated S-parameters have an excellent agreement with below 1% discrepancy in the frequency range of 1–30 GHz over a wide range of bias points.

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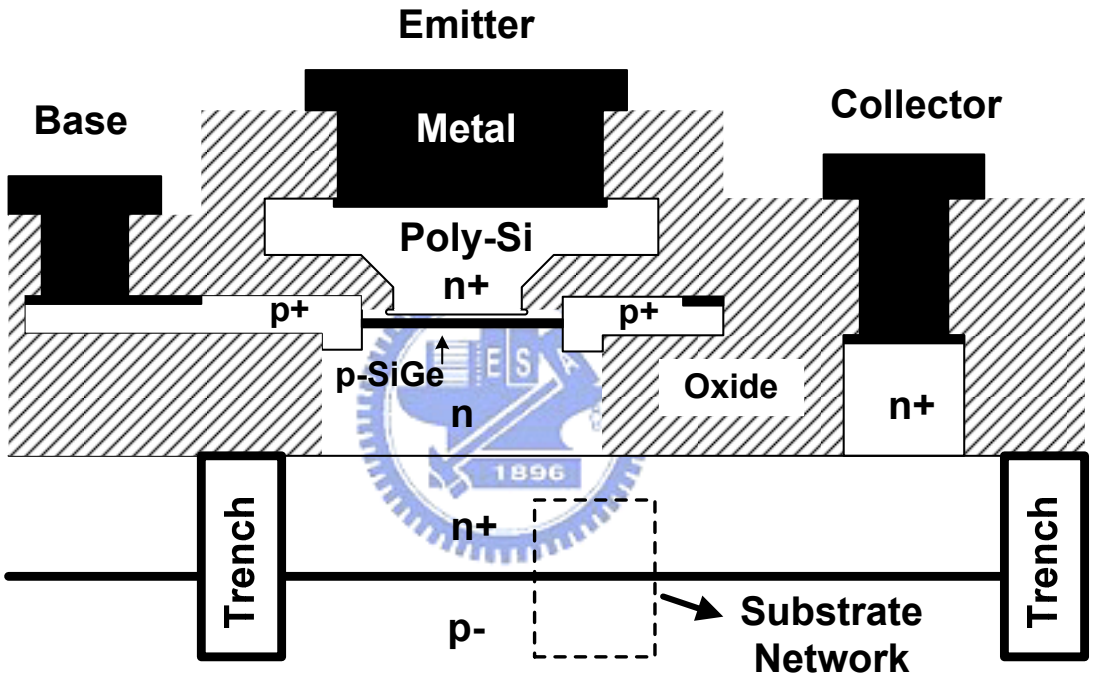


Fig. 3.1 Cross section of SiGe HBTs.

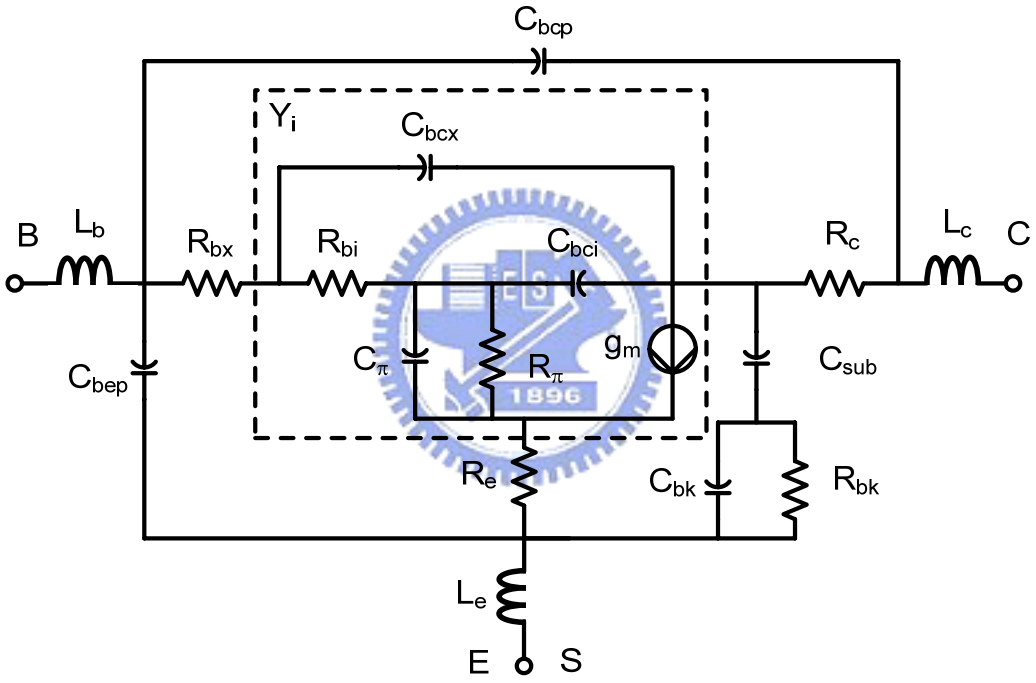


Fig. 3.2 Small-signal equivalent circuit model for a SiGe HBT in the forward active region.

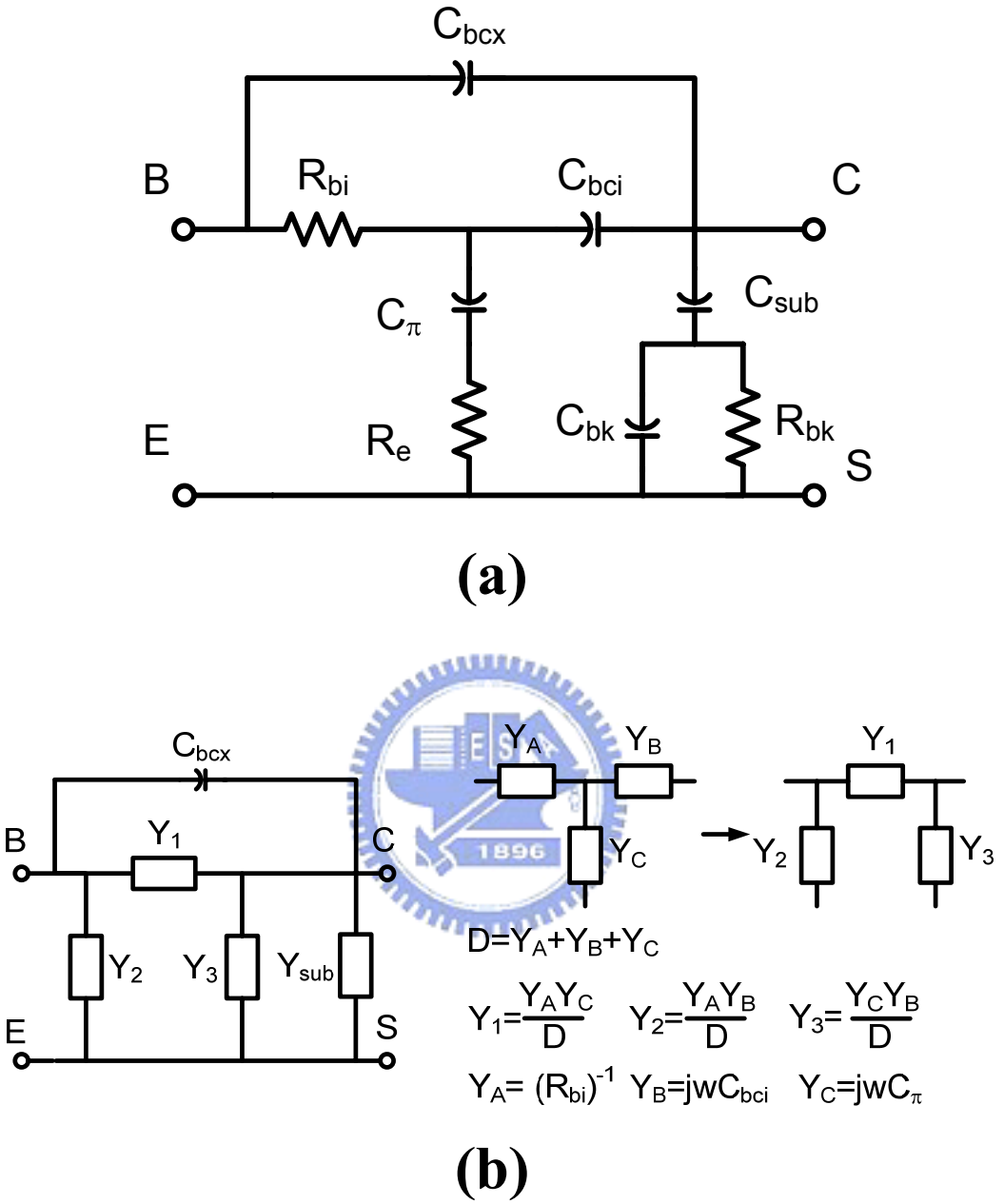
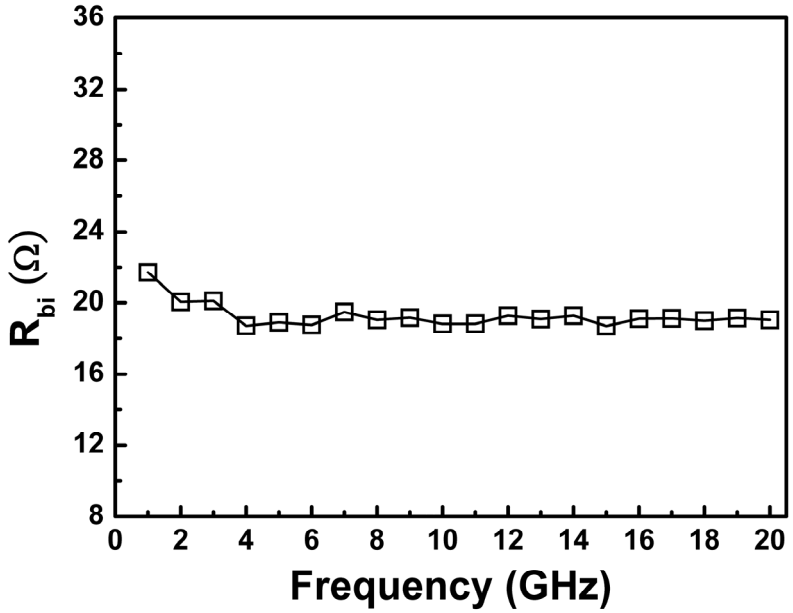
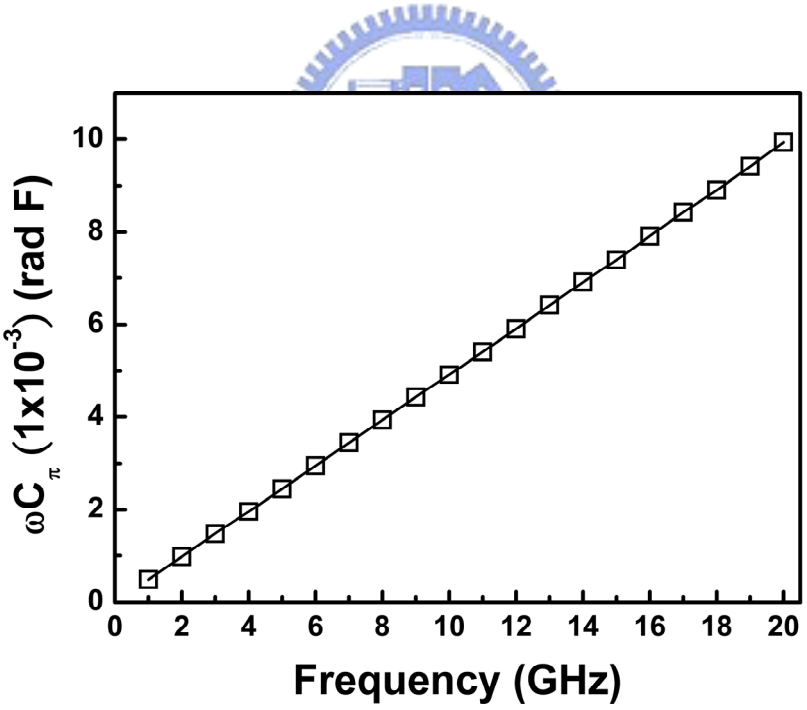


Fig. 3.3 (a) Small-signal equivalent circuit model for a SiGe HBT biased at V_{BE}=0 and forward and/or low reverse collector voltage after de-embedding the "open" dummy pad and removing the extrinsic inductances, extrinsic base resistance and extrinsic collector resistance. (b) Application of the T↔Π transformation to the HBT device equivalent circuit shown in (a).



(a)



(b)

Fig. 3.4 Frequency dependencies of the extracted (a) R_{bi} and (b) ωC_π for a SiGe HBT biased at V_{BE} = 0 V and V_{CE} = 3 V.

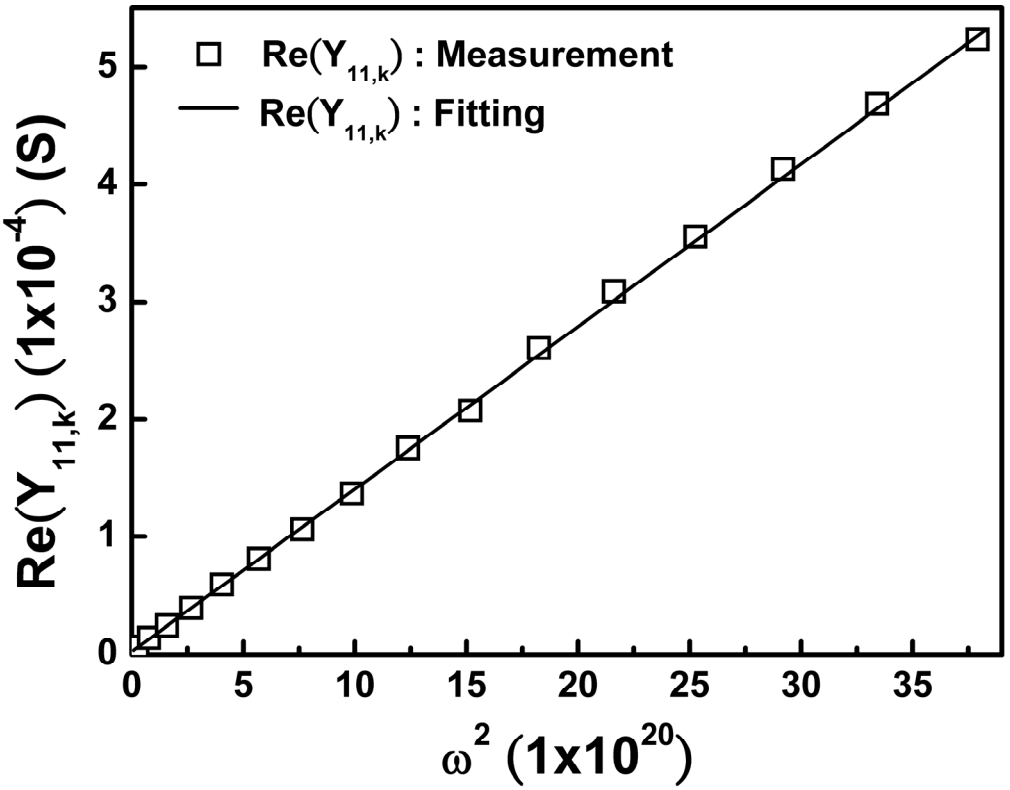
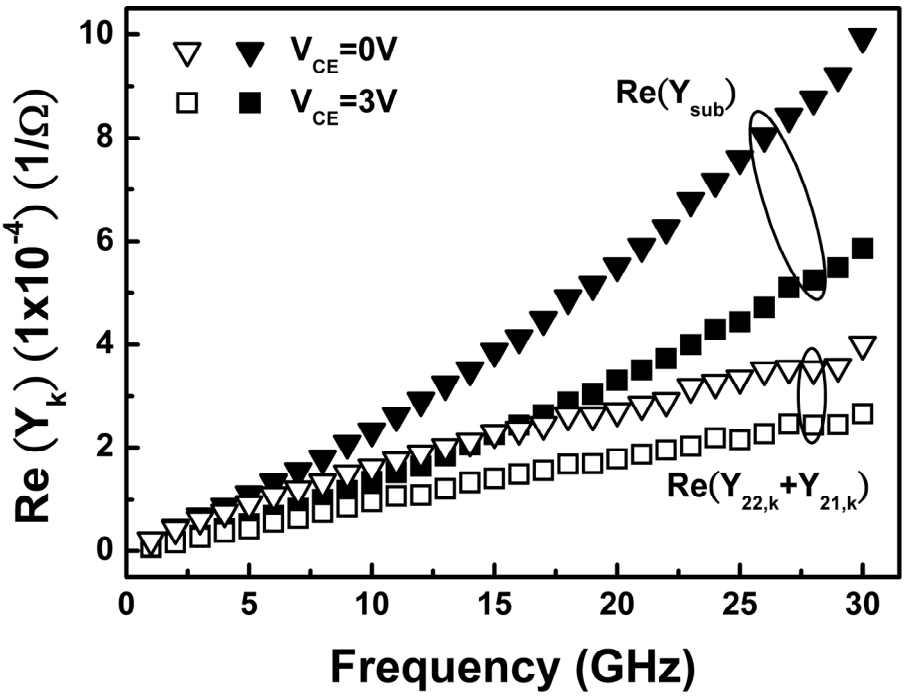
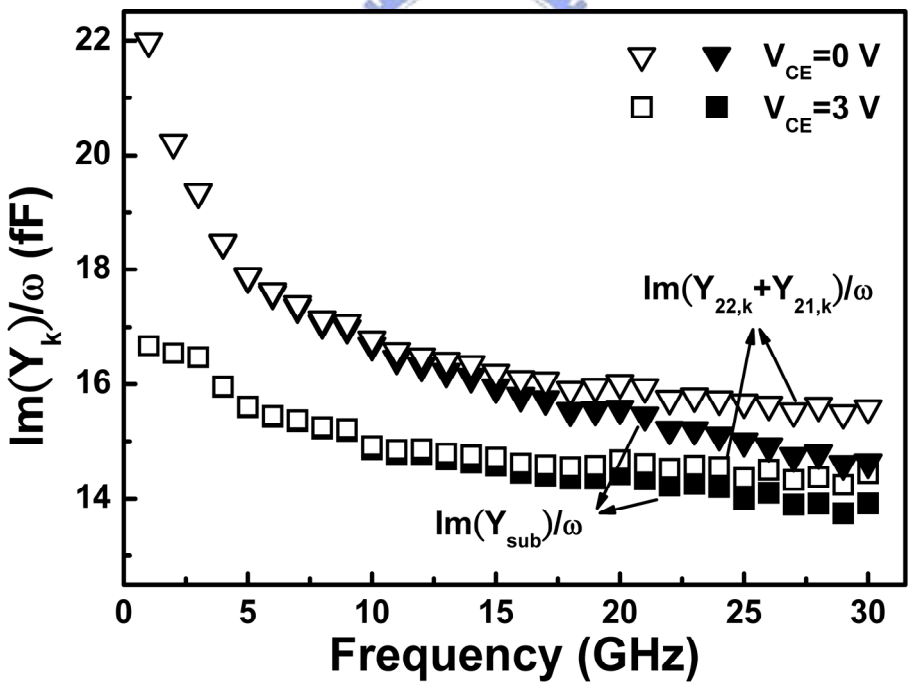


Fig. 3.5 Plot of Re($Y_{11,k}$) versus ω^2 for the calculation of C_{bci} for a SiGe HBT biased at V_{BE} = 0 V and V_{CE} = 3 V.



(a)



(b)

Fig. 3.6 Comparison between Y_{sub} and $Y_{22,k} + Y_{21,k}$ for a SiGe HBT biased at V_{BE} = 0 V and V_{CE} = 0V, 3V (a) Re(Y_{sub}) and Re($Y_{22,k} + Y_{21,k}$). (b) Im(Y_{sub}) and Im($Y_{22,k} + Y_{21,k}$).

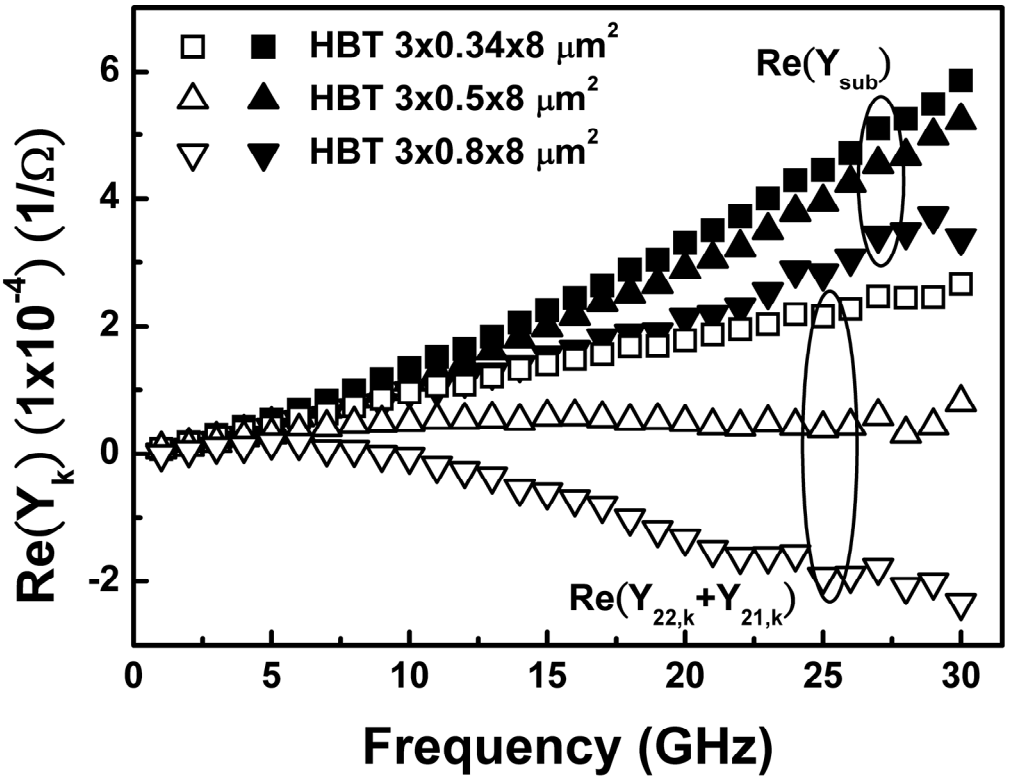


Fig. 3.7 Frequency dependence of the extracted Re(Y_{sub}) and Re($Y_{22,k} + Y_{21,k}$) for three SiGe HBTs with different emitted width (0.34 μm, 0.5 μm, 0.8 μm) biased at V_{BE} = 0 V and V_{CE} = 3 V.

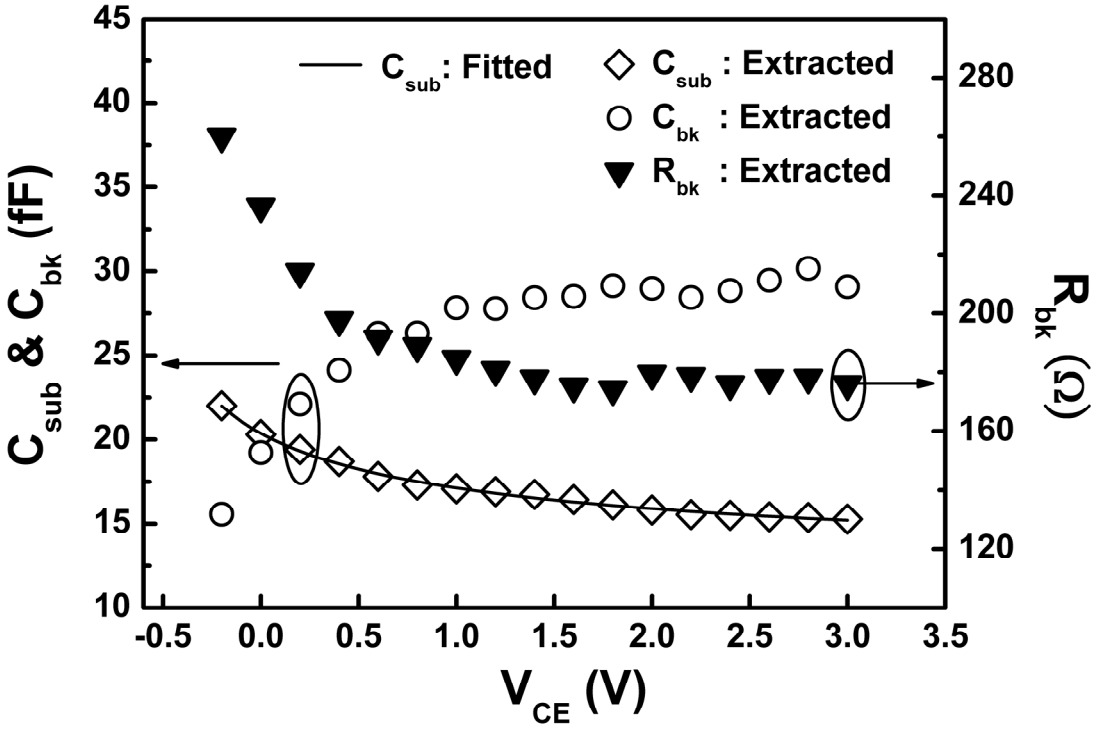


Fig. 3.8 Collector-voltage dependence of the extracted C_{sub}, R_{bk} and C_{bk} for a SiGe HBT biased at V_{BE} = 0 V. Solid line gives the empirical fitting for C_{sub}.

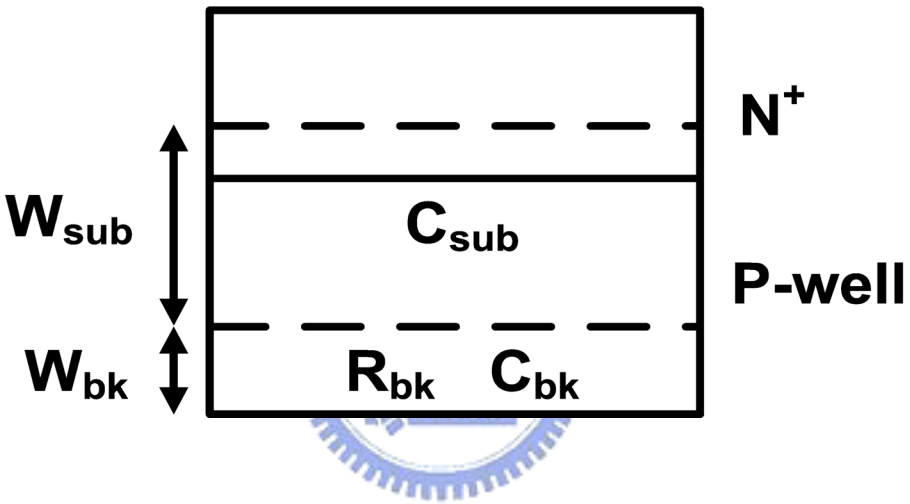


Fig. 3.9 Cross section view of a simple N+-P junction.

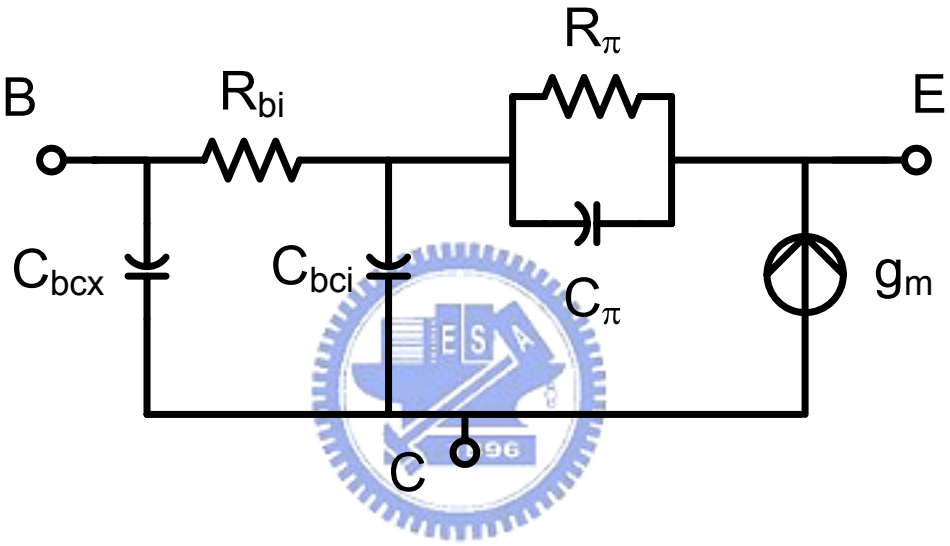


Fig. 3.10 Small-signal equivalent circuit model of intrinsic SiGe HBT in common collector configuration.

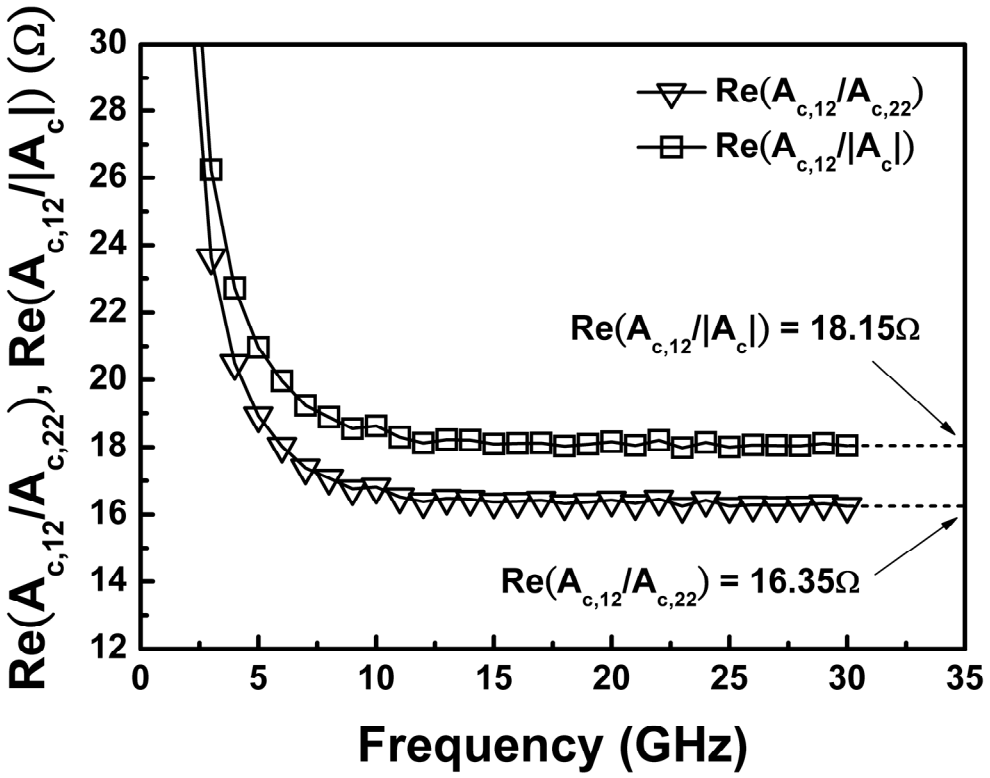


Fig. 3.11 Plot of Re($A_{c,12}/A_{c,22}$) and Re($A_{c,12}/|A_c|$) versus frequency. V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA, and I_B = 7.915 μA.

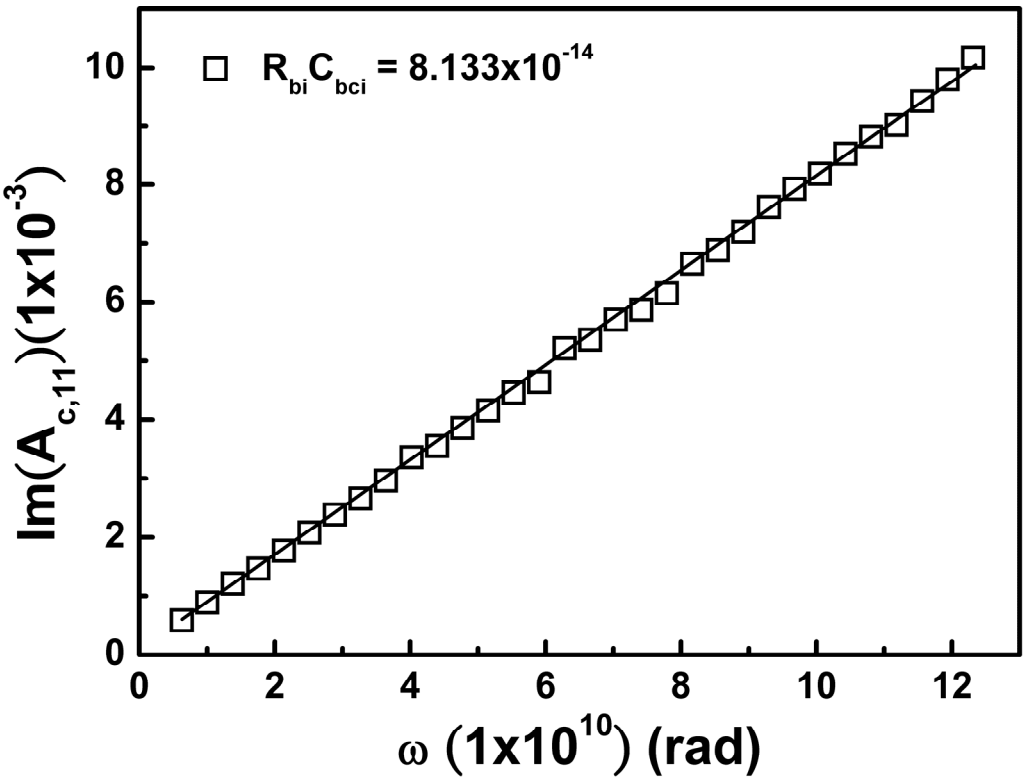


Fig. 3.12 Plot of Im($A_{c,11}$) versus ω. V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA, and I_B = 7.915 μA.

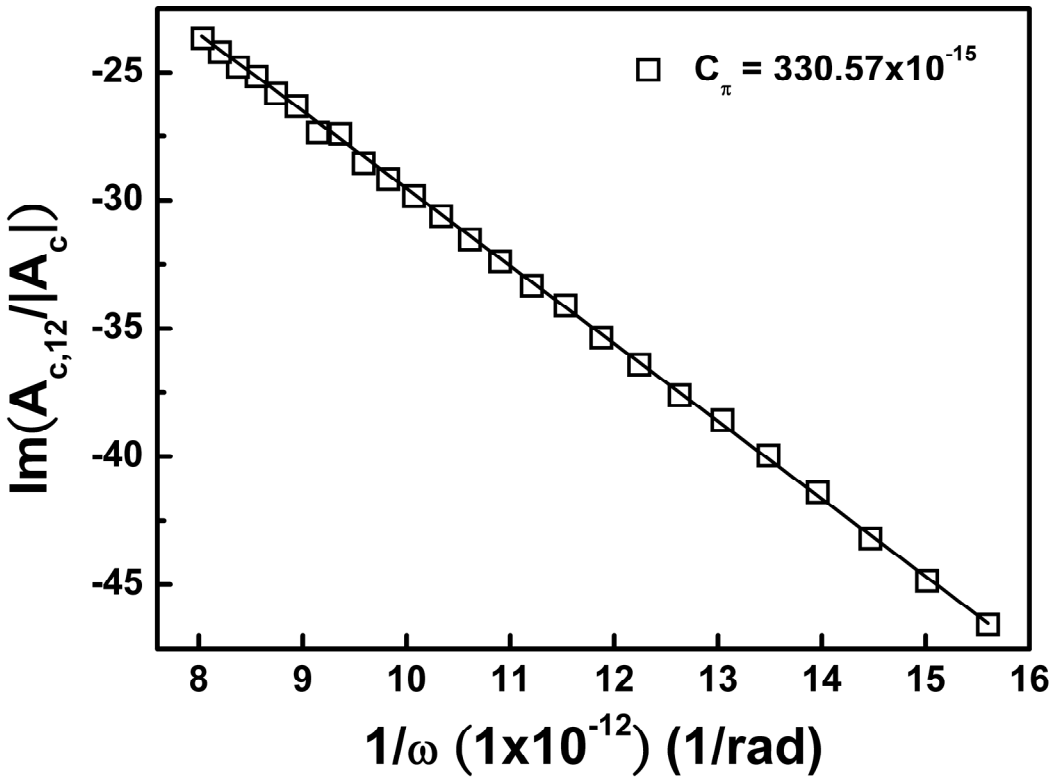


Fig. 3.13 Plot of Im($A_{c,12}$/|A_c|) versus 1/ω. V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA, and I_B = 7.915 μA.

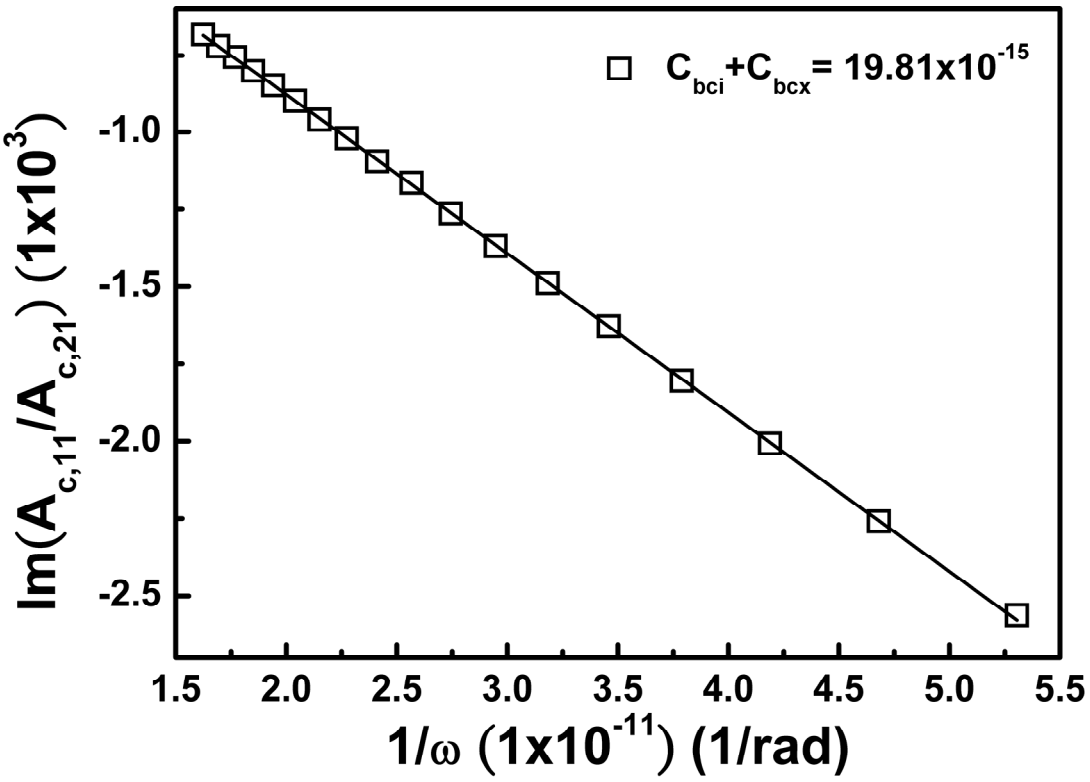


Fig. 3.14 Plot of Im($A_{c,11}/A_{c,21}$) versus 1/ω. V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA, and I_B = 7.915 μA.

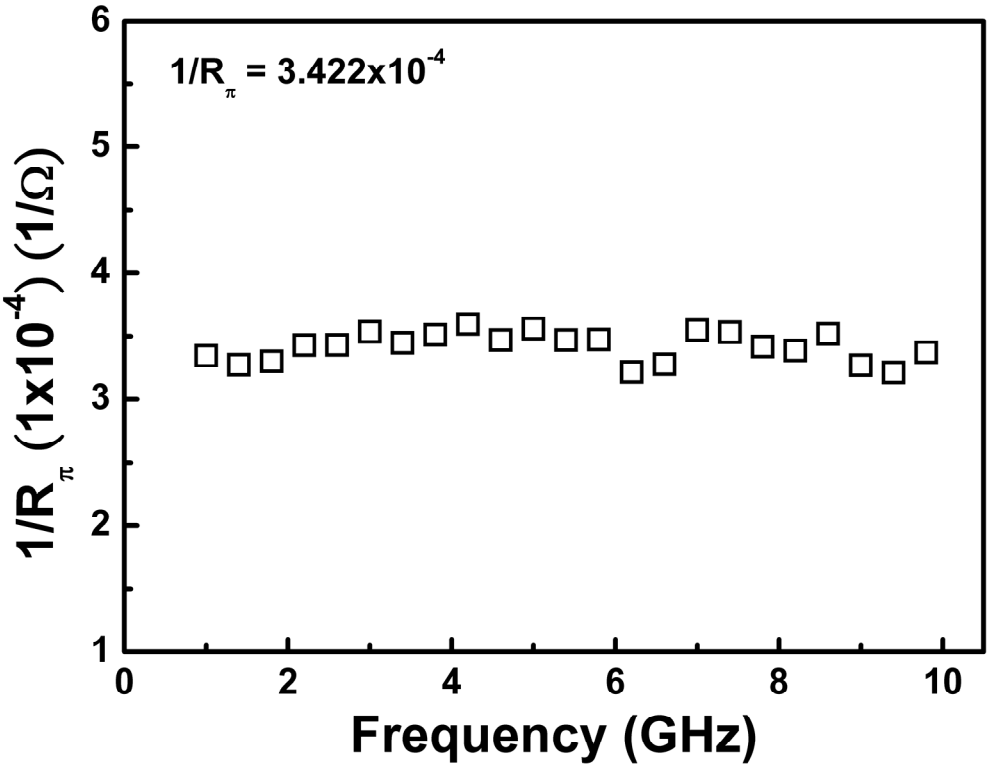


Fig. 3.15 Frequency dependence of extracted $1/R_\pi$ for a SiGe HBT biased at V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA and I_B = 7.915 μA.

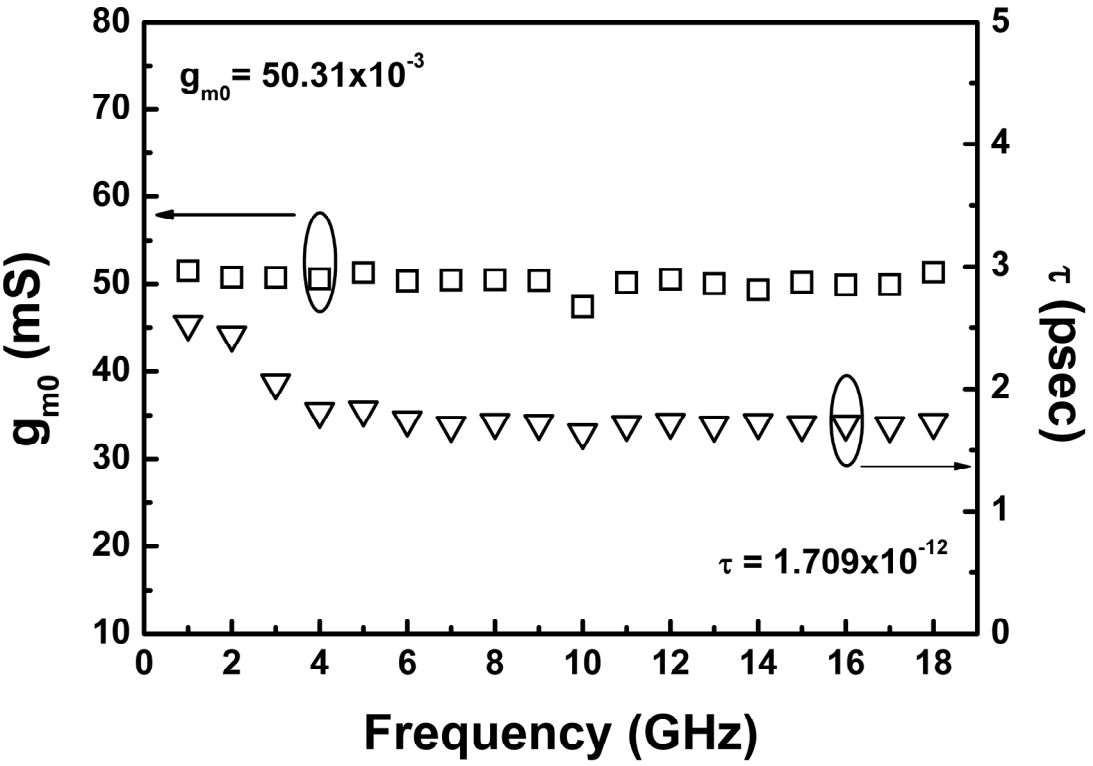


Fig. 3.16 Frequency dependence of extracted g_{m0} and τ for a SiGe HBT biased at V_{BE} = 0.83 V, V_{CE} = 3 V, I_C = 1.333 mA and I_B = 7.915 μA.

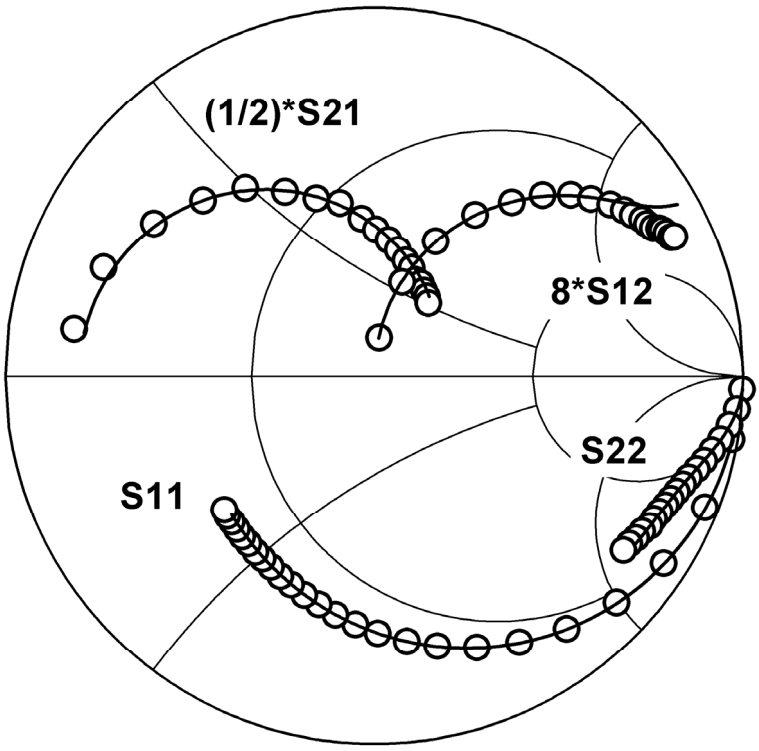


Fig. 3.17 Measured (Symbol) and simulated (line) S-parameters of the 3×0.34×8 μm^2 SiGe HBT in the frequency range of 1–30 GHz, at V_{BE} = 0.8 V, V_{CE} = 2 V, I_B = 2.477 μA, and I_C = 0.414 mA.

Chapter 4

An Analysis of Base Current Effect on the Anomalous Dip of Scattering Parameter S_{12} in SiGe HBTs

4.1 Introduction of Anomalous Dip of Scattering Parameter

Scattering parameters have been used extensively in the analysis of microwave devices. In some transistors, the anomalous dip or kink phenomenon is appeared in some of the four S-parameters. For example, the anomalous dip of S_{11} is observed in RF power MOSFETs with a large gate-drain offset [1]. In HBTs, the anomalous dip of S_{11} becomes obvious as the base current increases [2]. The kink phenomenon in transistor scattering parameters S_{22} of FETs/HBTs have also been reported and explained quantitatively [3], [4]. However, the anomalous dip in scattering parameter S_{12} of HBTs which can be seen frequently in the literature [4], [5] has never been reported in detail. In addition, this anomalous dip is much more frequently seen in bipolar transistors as compared with MOSFETs.

In this chapter, we derive an analytic expression of transistor scattering parameter S_{12} in terms of Y-parameters of the hybrid-π model of SiGe HBTs to explain the anomalous dip of S_{12} quantitatively. This study can be used in conjunction with the analysis of the anomalous dip in S_{11} and S_{22} to provide a complete set of analysis in microwave transistor scattering parameters. From the analysis, we found that the concept of dual-feedback circuit methodology which has been widely used in the analysis of the anomalous dips in S_{11} and S_{22} [1]-[4] can not be directly applied in the

analysis of the anomalous dip of S_{12}. The calculated S_{12} based on the derived analytical equation can get a better agreement with the measurement results. Furthermore, it was found that under constant collector-emitter voltage (V_{CE}), an increase of base current (I_B) enhances the anomalous dip of S_{12}.

4.2 S_{12} versus Base Current

The HBTs studied in this work were fabricated with a 0.35 μm SiGe BiCMOS technology. The emitter width and emitter length of the device under test are 1.24 μm and 32 μm, respectively. The S-parameters were measured in a common-emitter configuration using an HP8510C network analyzer with on-wafer SOLT calibration. The measurement frequency range was from 0.2 to 20 GHz. This setup together with Infinity coplanar ground–signal–ground probes provided reliable RF measurements.

Small-signal hybrid-π models of the SiGe HBTs were created for studying the anomalous dip in scattering parameter S_{12}. To obtain the intrinsic RF performance and even the correct description of devices, a three-step de-embedding technique [5] which utilized an open, a short1, a short2, and a through dummy structures was adopted. The values of the model parameters of the hybrid-π model were then obtained based on the analytical transformations mentioned in chapter 3. For simplicity, the substrate is only modeled as a simple capacitance.

Figure 4.1(a) shows the measured scattering parameters S_{12} of a SiGe HBT with different base current. The extracted extrinsic and intrinsic elements are listed in Table 4.1 and Table 4.2, respectively. The extracted base-emitter capacitance (C_π) is 1.892, 1.404 and 0.884 pF for the device biased at V_{CE} = 2 V and I_B = 234, 79.6 and 17.2 μA,

respectively. Under a constant V_{CE}, an increase of base current corresponds to an increase of C_π, which makes the anomalous dip more prominent [i.e. moves to a lower frequency]. The reason will be discussed in Sec 4.4. Fig. 4.1(b) shows the measured scattering parameters S_{12} before and after pad lines and interconnects [i.e., L_b, L_e, L_c, C_{bep}, and C_{cep} in Fig. 4.2(a)] de-embedded. As can be seen, after the pad lines and interconnects are de-embedded, the kink frequency shows a small change (increases from 4.8 GHz to 5.4 GHz). This means the extrinsic elements due to pad lines and interconnects only affect the shape of S_{12} and do not affect the appearance of the dip phenomenon. Therefore, the dip phenomenon may mainly originate from the interaction of the intrinsic parameters, R_π, C_π, C_{bcx}, C_{bci}, R_{bi}, and g_m.

4.3 Expressions of Scattering Parameters S_{12}

The setup for the measurement of transistor S-parameters is shown in Fig. 4.2(a), where Z_0(= $1/Y_0$) equals 50 Ω and is connected to the input and output ports of the device-under-test. S_{11} and S_{21} can be measured by setting $V_2 = 0$ and $V_1 \neq 0$, while S_{22} and S_{12} can be measured by setting $V_1 = 0$ and $V_2 \neq 0$. The physical meaning of S_{12} is twice the reverse voltage gain V_{o1}/V_2. If the expression for the output impedance Z_{out} of this circuit has been found, shown in Fig. 4.3(b) is obtained as

$$S_{12} = 2\frac{Z_{out} - R_C - jwL_C}{Z_{out} + Z_0} \cdot \frac{V_{o1}}{V_{out,i}}. \tag{4.1}$$

In general, it is hard to find the output impedance of the circuit in Fig. 4.2(a). However, the problem will be much easier to solve if the circuit is viewed as a dual-feedback circuit in which $R_e + j\omega L_e$ is the local series-series feedback element

and C_{bcx} is the local shunt-shunt feedback element. In addition, pad parasitic capacitances C_{bep} and C_{cep} can be neglected because pad lines and interconnects only affect the shape of S_{12} and do not influence the appearance of the dip phenomenon. In order to simplify the circuit analysis, we temporarily neglect the inductors and transform the circuit of Fig. 4.2(a) into that of Fig. 4.2(b) with some circuit element modifications [3], which are also shown in Fig. 4.2(b).

The intrinsic output impedance defined in Fig. 4.2(b) can be expressed as

$$Z_{out,i} = \frac{\left(R_\pi^{'} \left\| \frac{1}{sC_\pi^{'}} + R_{bi}^{'} \right. \right) \| Z_{o1} + \frac{1}{sC_{bc}}}{1 + g_m^{''} \left(R_\pi^{'} \left\| \frac{1}{sC_\pi^{'}} + R_{bi}^{'} \right. \right) \| Z_{o1}} \tag{4.2}$$

where $g_{m0}^{'} = g_{m0}/(1+g_{m0}R_e)$, $C_{bc} = C_{bci} + C_{bcx}$, $C_\pi^{'} = C_\pi/(1+g_{m0}R_e)$, $R_\pi^{'} = R_\pi(1+g_{m0}R_e)$, $R_{bi}^{'} = R_{bi}(1+g_{m0}R_e) + R_e$, $g_{m0}^{''} = g_{m0}^{'} \cdot R_\pi^{'}/(R_\pi^{'} + R_{bi}^{'}(1+sC_\pi^{'}R_\pi^{'}))$ and $Z_{O1} = Z_O + R_b$. Once this intrinsic output impedance is known, the normal output impedance is simply the series combination of $Z_{out,i}$ and R_c as follows:

$$Z_{out} = Z_{out,i} + R_c \, . \tag{4.3}$$

By using the derived normal output impedance and inspecting Fig. 4.2(b), S_{12} is given as follows:

$$S_{12} = 2\frac{Z_{out} - R_C}{Z_{out} + Z_0} \cdot \frac{sC_{bc}}{sC_{bc} + \frac{1 + sC_\pi^{'}R_\pi^{'}}{R_{bi}^{'} + R_\pi^{'} + sC_\pi^{'}R_{bi}^{'}R_\pi^{'}} + \frac{1}{Z_0 + R_b}} \frac{Z_0}{Z_0 + R_b} \, . \tag{4.4}$$

As shown in Fig. 4.3, the derived S_{12} based on the dual-feedback circuit methodology doesn't yield a good fit with the measured S_{12}. To well explain the anomalous dip of S_{12}, a general analytic expression of transistor scattering parameter S_{12} is derived in terms of intrinsic Y-parameters (without R_b and R_c but with R_e) as follows:

$$S_{12} = \frac{Z_{out,i}}{Z_{out,i} + R_C + Z_0} H(s) \tag{4.5}$$

where

$$Z_{out,i} = \frac{1 + Y_{11,b}(R_b + Z_0)}{Y_{22,b} + \Delta Y_b (R_b + Z_0)} \tag{4.6}$$

and

$$H(s) = Z_0 \frac{2Y_{12,a}}{1 + Y_{11,a}(R_b + Z_0)}. \tag{4.7}$$

The Y-parameters used in $Z_{out,i}$ ($Y_{ij,b}$) and $H(s)$ ($Y_{ij,a}$) are the intrinsic Y-parameters of the SiGe HBT shown in Fig. 4.2(b) and Fig. 4.2(a), respectively. ΔY_b is the determinant given by $\Delta Y_b = Y_{11,b} \times Y_{22,b} - Y_{12,b} \times Y_{21,b}$. As shown in Fig. 4.3, the derived analytical representation of S_{12} shows a better agreement with measured S_{12}. In (4.6), the dual-feedback circuit methodology is applied in the calculation of output impedance ratio (first term in the RHS of (4.5)). On the other hand, as depicted in (4.7), the feedback network, $H(s)$, is calculated from the original equivalent circuit. The arrangement is because the dual-feedback circuit methodology can not get a good approximation in the feedback network but a good approximation in the input or output impedance. That may be the reason the dual-feedback theory is often used in

the analysis of transistor scattering parameters S_{11} and S_{22} [1]-[4].

4.4 Results and Discussions

Figure 4.4 shows the measured S-parameters from 0.1 to 20 GHz of the SiGe HBT with emitter size of 1.24×32 μm^2 biased at V_{CE} = 2 V and I_B = 79.6 μA. The anomalous dip of S_{12} and S_{22} appear at about 6.6 and 4.4 GHz, respectively. The S-parameters generated by the small-signal model are also shown in Fig. 4.4, which is in good agreement with the measured data.

Based on the two-pole approximation, the output impedance ratio and H(s) can be interpreted in terms of poles and zeros [6] as shown follows:

$$\frac{Z_{out}}{Z_{out}+R_c+Z_o} \approx 1 \times \frac{\left(1+\frac{s}{w_{bz1}}\right)}{\left(1+\frac{s}{w_{bp1}}\right)\left(1+\frac{s}{w_{bp2}}\right)} \tag{4.8}$$

$$H(s) \approx \frac{\left(R_e+r_\pi^{'}\right)C_{\mu 1}^{'}+R_{bin}C_{\mu 1}}{R_e+R_{bin}+r_\pi^{'}+Z_p} \frac{s\left(1+\frac{s}{w_{Hz1}}\right)}{\left(1+\frac{s}{w_{Hp1}}\right)} \tag{4.9}$$

where w_{bz1} and w_{Hz1} are the zeros of output impedance ratio and feedback network, respectively. w_{bp1}, w_{bp2}, and w_{Hp1} are the poles of output impedance ratio and feedback network, respectively. In (4.7) and (4.8), some of poles and zeros located in high frequency range (>200 GHz) are previously neglected due to their small influence on S_{12} in the interested frequency range ($0.2 < f < 20$ GHz). The derived poles and zero

are listed in Table 4.3.

Figure 4.5 shows the phase plot of S_{12} for both the measured and simulated data. The phase of the output impedance ratio and the feedback network are also shown in Fig. 4.5. The shape of the frequency response of S_{12} is dependent on the locations of its zeros with respect to its poles. f_{bz1}, f_{bp1}, f_{bp2}, f_{Hp1} and f_{Hz1} can be calculated from Tables 4.1 and 4.2 and their values are indicated in Fig. 4.5. The calculated f_{Hp1} and f_{bz1} are close to each other and therefore their effect on the phase change of S_{12} is small. The closeness of f_{Hp1} and f_{bz1} can be observed from the similar analytic representation shown in Table 4.3. The phase change of S_{12} is then dominated by the interaction between f_{bp1}, f_{bp2} and f_{Hz1}. In modeling SiGe HBTs, the zero in the feedback network, f_{Hz1}, often falls between the two poles in the output impedance ratio, f_{bp1} and f_{bp2}. At low frequency, the phase of S_{12} is decreased by the pole, f_{bp1}. As the frequency increases, the phase contribution of f_{Hz1} makes the phase of S_{12} increase. As the frequency continues increasing, the phase of S_{12} will be decreased again by the pole, f_{bp2}. It is the interaction between the poles in the output impedance ratio and zeros in the feedback network that causes the appearance of the anomalous dip in the transistor scattering parameter S_{12}.

The reason why under constant V_{CE}, an increase of I_B makes the anomalous dip more prominent [see Fig. 1(a)] can be observed from Table 4.2 and Table 4.3 (w_{Hz1}). An increase of I_B makes the B/E junction biased in a higher forward voltage, then the B/E depletion capacitance and B/E diffusion capacitance increase, i.e. C_π increases, and hence w_{Hz1} moves to a lower frequency, which makes the anomalous dip more

prominent. As I_B decreases, the value of C_π decreases, then from Table 4.2 and Table 4.3, w_{Hz1} and w_{bp2} move toward to each other. As w_{Hz1} moves close to or beyond w_{bp2}, the anomalous dip is disappeared or moves out of the interested frequency range. In high base current bias condition where w_{Hz1} is far below w_{bp2}, the dip frequency can be roughly estimated as $(f_{bp1} \times f_{Hz1})^{0.5}$.

Comparing HBTs and MOSFETs with same active area (emitter width×emitter length for HBTs and gate length×gate width for MOSFETs), the value of C_π often shows several times larger than that of gate to source capacitance, C_{gs}. In HBTs, C_π is composed of the depletion capacitance and the diffusion capacitance, and varies in a wide range as the bias condition changes. In MOSFETs, C_{gs} saturates to the value about $2/3C_{ox}$ (oxide capacitance). Therefore, in MOSFETs, the zero in the feedback network often located in a higher frequency range. This may be one reason why it is much easier to see the anomalous dip in HBTs than in MOSFETs.

From the discussion, the “anomalous dip” is a “normal behavior” of S_{12}. From the perspective of device physics, the appearance of the dip results from the interaction among R_π, C_π, C_{bcx}, C_{bci}, R_{bi}, and g_m. It has nothing to do with any nonideal characteristic due to device defects or trapping of carriers, etc. If any of the intrinsic circuit elements causes a decrease of the zero in the feedback network, then the dip will become more prominent.

4.5 Summary

In this chapter, the anomalous dip in scattering parameters S_{12} of SiGe HBTs is explained quantitatively for the first time. The results show that the dual-feedback circuit methodology which is widely used in the analysis of the anomalous dips in S_{11} and S_{22} can not be directly applied in the analysis of the anomalous dip in scattering parameters S_{12} due to its poor approximation in the feedback network. An analytic expression of the transistor scattering parameter S_{12} based on the Y-parameters representation is derived to explain the anomalous dip of S_{12}. The calculated S_{12} from the derived analytical expression is in good agreement with the measurement results of SiGe HBTs. It is proven that one zero in the output impedance ratio is close to one pole in the feedback network. Therefore their effect on the frequency response of S_{12} is small. The results also show that the relationship between one zero in the feedback network and two poles in the output impedance ratio causes the appearance of the anomalous dip of S_{12} in a polar chart. The present analysis can enable RF engineers to understand the behaviors of S-parameters more deeply, and, hence, may be helpful for RF integrated circuit (RFIC) designs.

References

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Table 4.1 Extracted extrinsic elements of the small-signal SiGe HBT model.

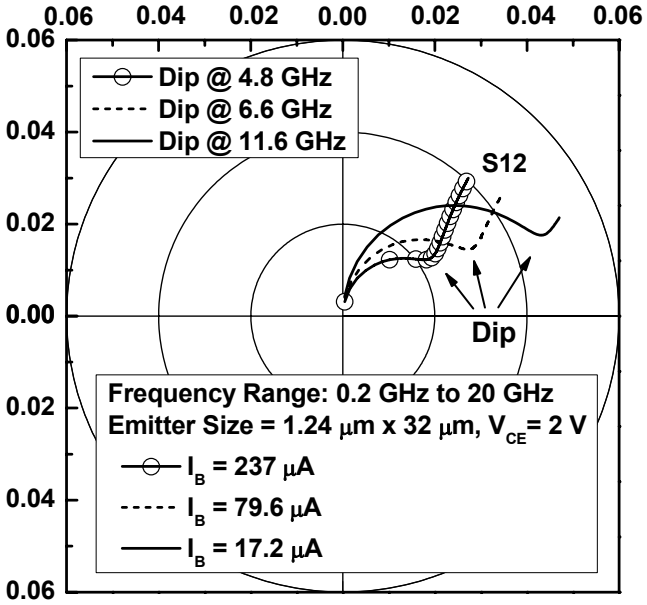
C_{bep} (fF)	C_{cep} (fF)	R_b (Ω)	R_c (Ω)	R_e (Ω)	L_b (pH)	L_c (pH)	L_e (pH)
24.46	20.6	8.617	9.942	0.637	33.96	5.0	14.88

Table 4.2 Extracted intrinsic elements of the small-signal SiGe HBT model for the bias condition of I_B = 237 μA, 79.6 μA, and 17.2 μA.

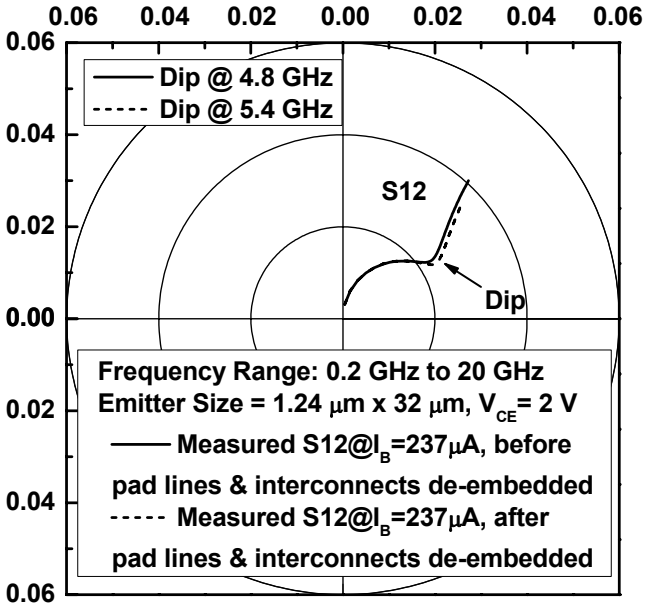
Parameter	I_B = 237 μA	I_B = 79.6 μA	I_B = 17.2 μA
C_π (pF)	1.892	1.404	0.884
C_{bcx} (fF)	11.89	11.38	10.78
C_{bci} (fF)	25	27.68	25.43
R_{bi} (Ω)	18.78	20.82	22.92
R_π (Ω)	126.2	288.8	999.2
g_{m0} (mS)	306.7	118.2	27.61
τ (pSec)	0.6154	0.6374	0.7632

Table 4.3 Expressions of poles and zeros of output impedance ratio and feedback network by dominant pole (zero) approximation

Poles of $\frac{Z_{out,i}}{Z_{out,i}+R_C+Z_0}$	$w_{bp1} \approx \frac{1}{R_\pi^{'}} \frac{R_\pi^{'}+Z_p}{Z_p C_{bc}\left[\frac{\left(R_{bi}^{'}+Z_q+g_{m0}^{'}R_{bi}^{'}Z_q\right)}{R_\pi^{'}}+1+g_{m0}^{'}Z_q\right]+C_\pi^{'}\left(Z_p+R_{bi}^{'}\right)+Z_q C_{bc}}$ $w_{bp2} \approx \frac{Z_p C_{bc}\left[\frac{\left(R_{bi}^{'}+Z_q+g_{m0}^{'}R_{bi}^{'}Z_q\right)}{R_\pi^{'}}+1+g_{m0}^{'}Z_q\right]+C_\pi^{'}\left(Z_p+R_{bi}^{'}\right)+Z_q C_{bc}}{C_{bc}C_\pi^{'}\left(R_{bi}^{'}Z_p+R_{bi}^{'}Z_q+Z_pZ_q\right)}$
Zeros of $\frac{Z_{out,i}}{Z_{out,i}+R_C+Z_0}$	$w_{bz1} \approx \frac{1}{R_\pi^{'}Z_p C_{bc}+C_\pi^{'}\left(R_{bi}^{'}+Z_p\right)} \frac{R_\pi^{'}+Z_p}{}$
Poles of $H(s)$	$w_{Hp1} \approx \frac{1}{R_\pi^{'}Z_p C_{bc}+C_\pi^{'}\left(R_{bi}+Z_p\right)+R_{bi}C_{bci}+C_\pi^{'}R_e+Z_pR_{bi}C_{bcx}/R_\pi^{'}} \frac{R_\pi^{'}+R_{bi}+Z_p}{}$
Zeros of $H(s)$	$w_{Hz1} \approx \frac{1}{C_\pi^{'}} \frac{R_\pi^{'}C_{bc}+R_{bi}C_{bcx}}{R_eR_\pi^{'}C_{bc}+R_{bi}C_{bcx}R_\pi^{'}}$
Definition of some symbols	$Z_p = R_b + Z_0$ $Z_q = R_c + Z_0$

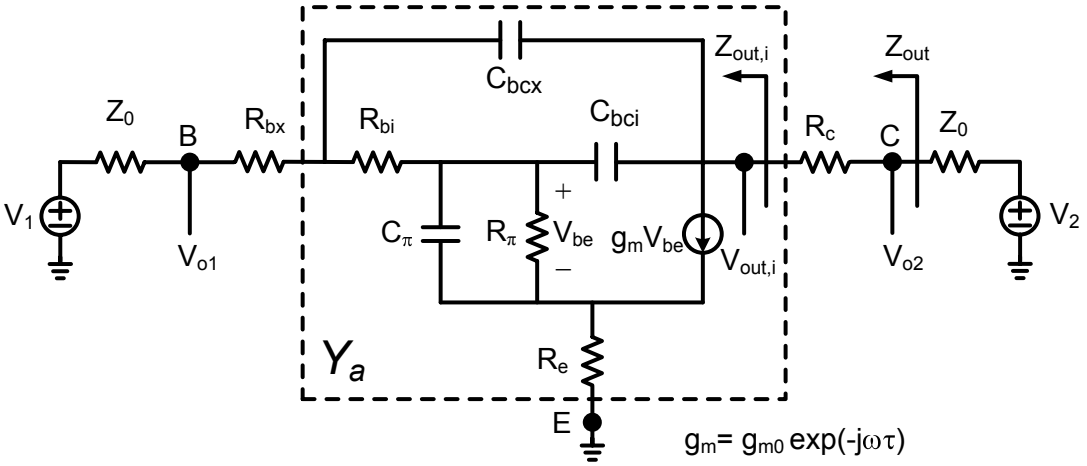


(a)

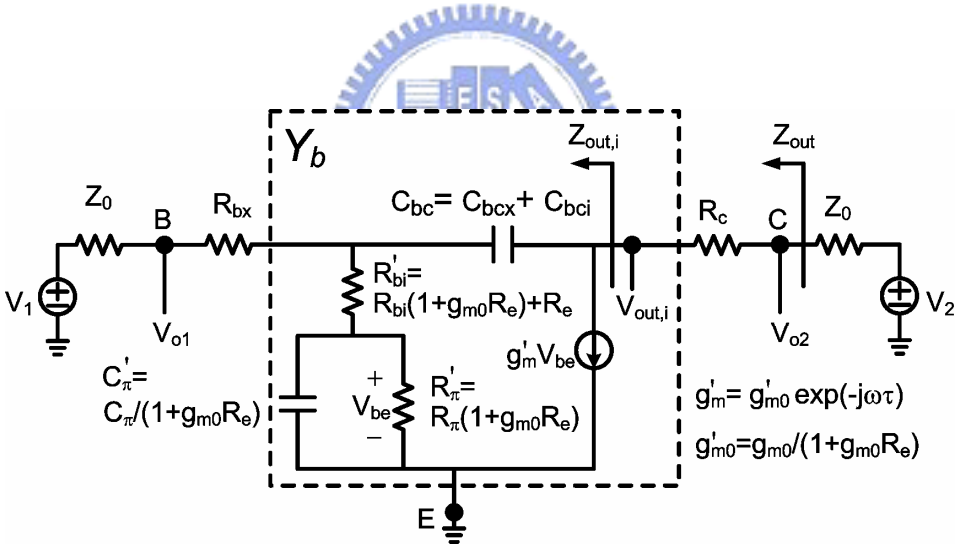


(b)

Fig. 4.1 (a) Measured scattering parameters S_{12} of a SiGe HBT with emitter size of 1.24×3.2 μm^2 biased at V_{CE} = 2 V and I_B = 237 μA, 79.6 μA, 17.2 μA. (b) The measured scattering parameters S_{12} before and after pad lines and interconnects de-embedded. The measured SiGe HBT is with emitter size of 1.24 ×3.2 μm^2 biased at V_{CE} = 2 V and I_B = 237 μA.



(a)



(b)

Fig. 4.2 Setup for the measurement of the SiGe HBTs S-parameters. (a) A complete circuit including a small-signal hybrid-π model. (b) A simplified circuit with the local series-series feedback element (R_e) absorbed.

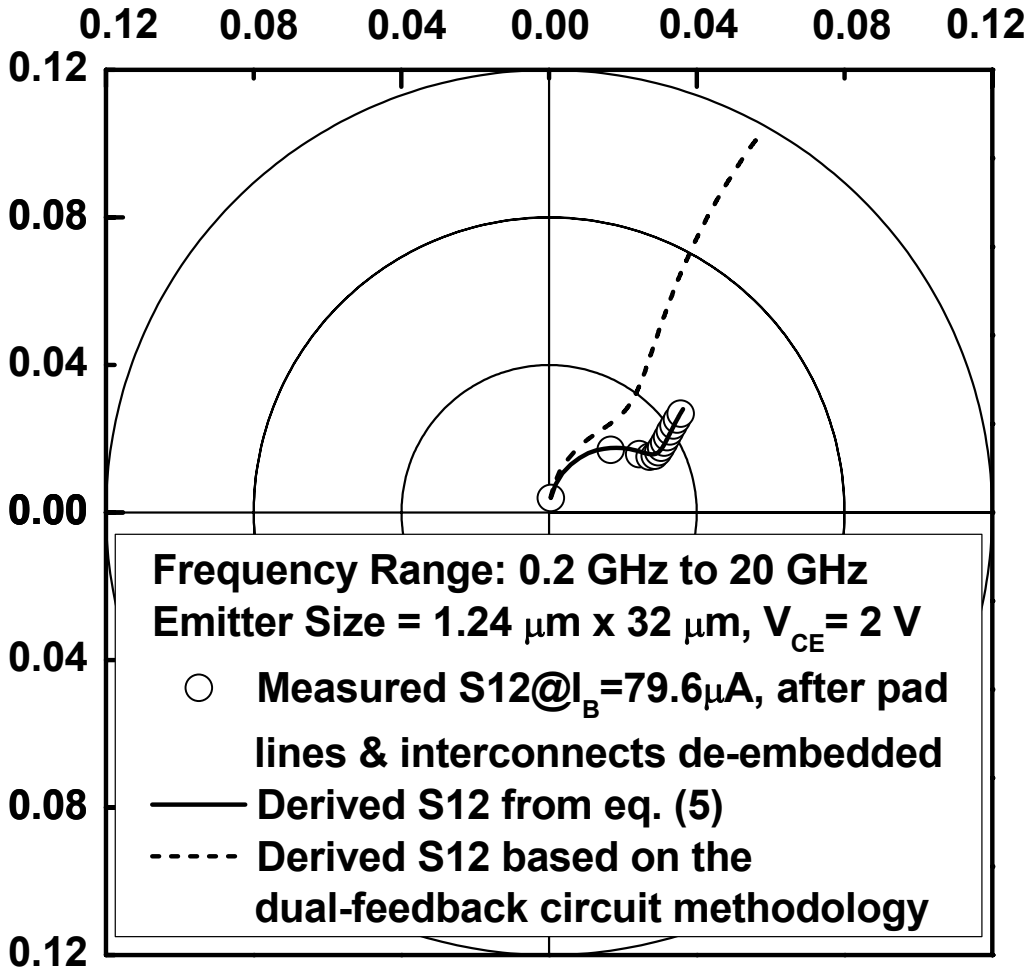


Fig. 4.3 Comparison of the experimental and calculated scattering parameters S_{12} of a SiGe HBT with emitter size of 1.24×3.2 μm^2 biased at V_{CE} = 2 V and I_B = 79.6 μA.

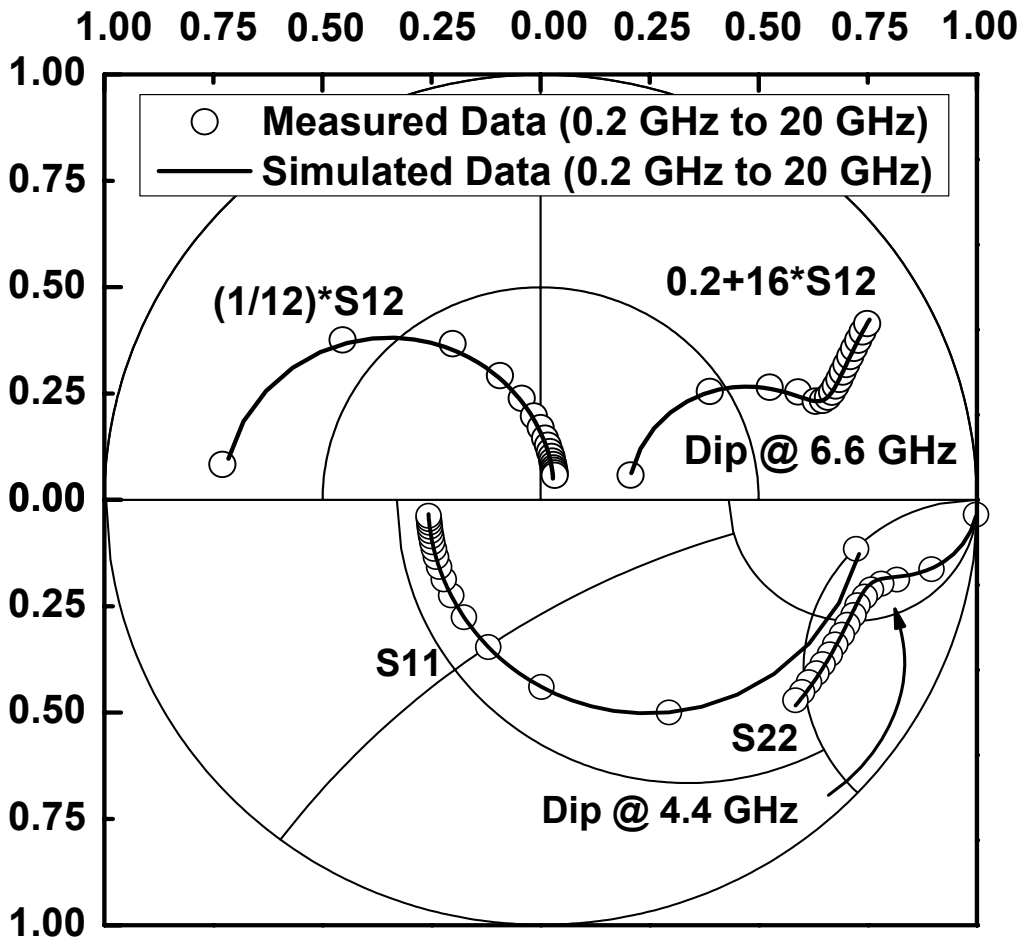
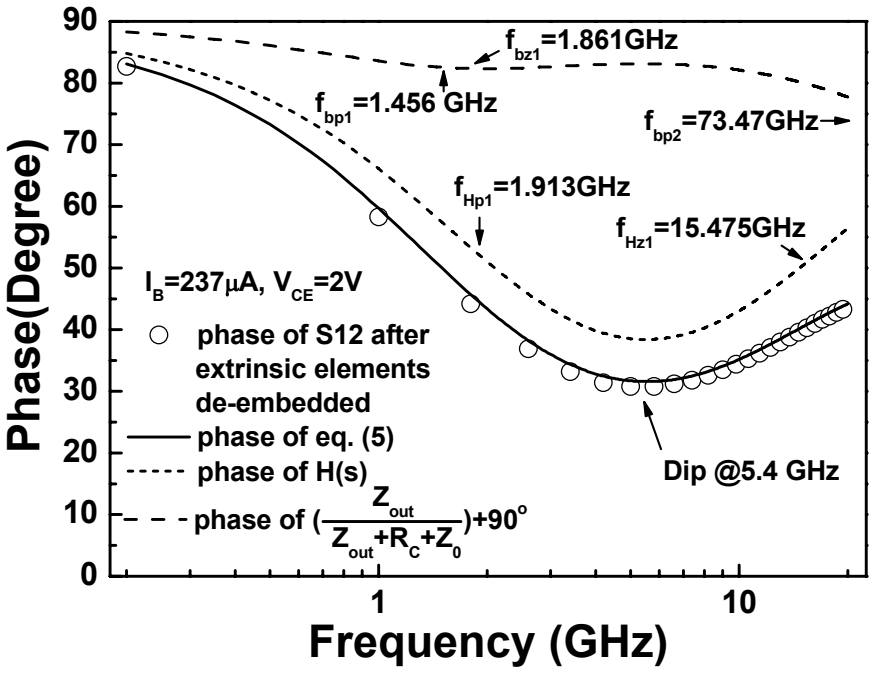
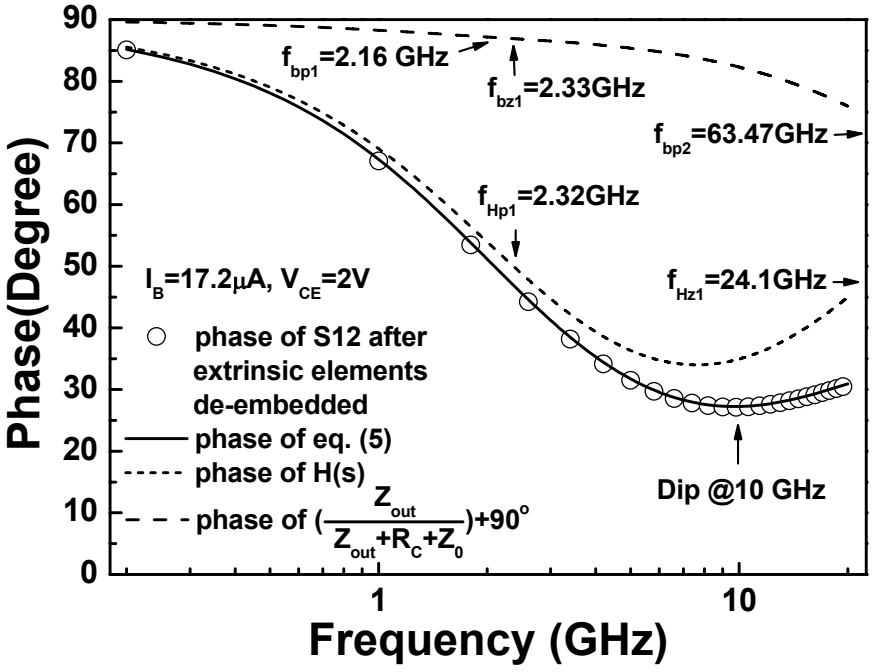


Fig. 4.4 Measured and modeled S-parameters of a SiGe HBT with emitter size of 1.24× 3.2 μm^2 biased at V_{CE} = 2 V and I_B = 79.6 μA.



(a)



(b)

Fig. 4.5 Frequency response of the phase of the scattering parameters S_{12} of a SiGe HBT with emitter size of 1.24×3.2 μm^2. (a) The SiGe HBT is biased at V_{CE} = 2 V and I_B = 237 μA. (b) The SiGe HBT is biased at V_{CE} = 2 V and I_B = 17.2 μA.

Chapter 5

Computation of Four Noise Parameters Using Genetic Algorithm

5.1 Introduction of Noise Parameters

Transistor high-frequency noise is a crucial issue in high-frequency circuit design as it sets the lowest sensitivity in the communication system. Accurate calculation of transistor noise parameters is important for the investigation of transistor fundamental physic phenomena. The "multiple impedance" technique which is best suited for appropriate automatic characterization and therefore most commonly used, derives noise parameters from noise figure data taken with various source admittance.

The "multiple impedance" technique is based on the relationship between the noise figure F of a linear two-port at a given frequency f and the source admittance $Y_s = G_s + jB_s$ given by the following equation [1]:

$$F = F_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{5.1}$$

where minimum noise figure F_{min}, the equivalent noise resistance R_n and the optimum source admittance $Y_{opt} = G_{opt} + jB_{opt}$ yielding a minimum noise figure are referred to as the four noise parameters at frequency *f*. Therefore at least four noise figure data F_i values and the associated source admittances $Y_s = G_{si} + jB_{si}$ are required at each frequency to compute the four noise parameters with appropriate extraction software based on (5.1).

The issue of noise parameters calculation from an over-dimensioned data set (a

data set is defined as the measured values of F, G_s, and B_s) has been addressed widely and several well-known techniques have been proposed [2]-[5]. Lane method [2] consists of performing noise figure measurements for more than four arbitrary source admittances with a least squares method used for data processing. The result of Lane method serves as initial values for Mitama method, which considers noise figure and source admittance errors [3]. Mitama method consists of minimizing the distance between the estimated data, which must be located on the noise surface, and the measured ones not located on it due to measurement uncertainties. The result of Lane method also provides the initial values for Boudiafs method [4] which extends Williamson method [6] to fit the best line to the measured statistical data. Another widely used method proposed by Vasilescu et al. [5] consists of directly solving a system of four nonlinear equations and finding the best solutions which yield the minimum sum of error function in the whole possible solution sets. Latter, a small modification was suggested by Laurent [7] to avoid solutions with no physical meaning in Vasilescu method. Among these methods, some considers the measured error in F only [2], [5], some requires initial values [3], [4] and some may be inefficient when numerous data sets are measured since all the possible combinations are calculated and examined [5], [7].

In chapter 5, a genetic algorithm (GA) has been adopted to overcome the shortcomings of pre-described methods. The present method directly searches the four noise parameters by finding the best solution set, which minimizes the measured source admittance error, as well as the measured F error.

5.2 Determine the Noise Parameters

It may be noted that for an arbitrary noise-figure measurement with a known generator admittance, (5.1) has four unknowns, F_{min}, R_n, G_{opt} and B_{opt}. By choosing four known values of generator admittance, a set of four linear equations are formed and the solution of the four unknowns can be found. (5.1) may be transformed to

$$F = F_{\min} + \frac{R_n \left|Y_{opt}\right|^2}{G_s} - 2R_n G_{opt} + \frac{R_n \left|Y_s\right|^2}{G_s} - 2R_n B_{opt} \frac{B_s}{G_s}. \tag{5.2}$$

Let

$$X_1 = F_{\min} - 2R_n G_{opt}, \tag{5.3}$$

$$X_2 = R_n \left|Y_{opt}\right|^2, \tag{5.4}$$

$$X_3 = R_n, \tag{5.5}$$

and

$$X_4 = R_n B_{opt}. \tag{5.6}$$

Then the generalized equation may be written as

$$F_i = X_1 + \frac{1}{G_{si}} X_2 + \frac{\left|Y_{si}\right|^2}{G_{si}} X_3 - 2\frac{B_{si}}{G_{si}} X_4 \tag{5.7}$$

or, in matrix form,

$$[F] = [A][X] \tag{5.8}$$

and the solution becomes

$$[X]=[A]^{-1}[F]. \tag{5.9}$$

The computation of four noise parameters often involves the minimization of the difference between the measured data and estimated data. For example, Lane method obtains the four noise parameters by minimizing the Z-axis difference as shown by the dotted line ε_L in Fig. 5.1. Mitama method tries to minimize the normal distance between the estimated data and measured data indicated as shown by the solid line ε_M in Fig. 5.1. Vasilescu method determines the noise parameters by minimizing Z-axis difference ε_L with a weighting factor equal to $1/F_i$. Thus, the computation of the noise parameters can be treated as a simple optimization problem.

5.3 Optimization Using GAS

In chapter 5, the error function defined in (5.2) is used to minimize F_i estimated error associated with Y_{si} estimated error for the ith measured data set (F_i, G_{si}, B_{si}) which is shown by ε_i in Fig. 5.1

$$\varepsilon=\sum_{i=1}^{N}\left[w_{Fi}\left(F_{Ci}-F_i\right)^2+w_{Gi}\left(G_{Ci}-G_{si}\right)^2+w_{Bi}\left(B_{Ci}-B_{si}\right)^2\right] \tag{5.2}$$

where

N	number of measured data sets,
W_{Fi}	weighting factor for noise figure,
W_{Gi}	weighting factor for source conductance,
W_{Bi}	weighting factors for source susceptance,
F_{Ci}	i-th calculated noise figures,
G_{Ci}	i-th calculated source conductance,
B_{Ci}	i-th calculated source susceptance,

and

F_i	i-th measured noise figure at the $G_{si}+jB_{si}$.

For given four noise parameters (F_{min}, R_n, G_{opt}, and B_{opt}) and source admittance (G_{si} and B_{si}), the calculated noise figure can be directly obtained from (5.1) and is shown as

$$F_{Ci} = F_{\min} + \frac{R_n}{G_{si}}\left[\left(G_{si} - G_{opt}\right)^2 + \left(B_{si} - B_{opt}\right)^2\right]. \tag{5.3}$$

The calculated source admittance is obtained in a similar way and is shown as

$$B_{Ci} = B_{opt} + \sqrt{\left(F_i - F_{\min}\right)\frac{G_{si}}{R_n} - \left(G_{si} - G_{opt}\right)^2} \qquad \text{for } B_{si} \geq B_{opt}, \tag{5.4a}$$

$$B_{Ci} = B_{opt} - \sqrt{\left(F_i - F_{\min}\right)\frac{G_{si}}{R_n} - \left(G_{si} - G_{opt}\right)^2} \qquad \text{for } B_{si} < B_{opt}, \tag{5.4b}$$

$$G_{Ci} = G_{opt} + \frac{1}{2R_n}\left[\left(F_i - F_{\min}\right) + \sqrt{\left(F_{\min} - F_i\right) - 4R_n^2\left(B_{si} - B_{opt}\right)^2 - 4R_n G_{opt}\left(F_{\min} - F_i\right)}\right], \tag{5.5a}$$

$$\text{for } G_{si} \geq \frac{1}{2R_n}\left(F_i - F_{\min}\right) + G_{opt}$$

and

$$G_{Ci} = G_{opt} + \frac{1}{2R_n}\left[\left(F_i - F_{\min}\right) - \sqrt{\left(F_{\min} - F_i\right) - 4R_n^2\left(B_{si} - B_{opt}\right)^2 - 4R_n G_{opt}\left(F_{\min} - F_i\right)}\right], \tag{5.5b}$$

$$\text{for } G_{si} < \frac{1}{2R_n}\left(F_i - F_{\min}\right) + G_{opt}$$

The Genetic algorithm (GA) is a global optimization technique that avoids many shortcomings exhibited by local search techniques. In this section, we apply a GA for solving the problem described in the Sec 5.2. A generic flowchart of the algorithm

used in this study is shown in Fig. 5.2. Some details of implementing the GA are highlighted in coordination with this research.

Population is a group of randomly initialized individuals (represented by chromosomes). Each chromosome contains genes, which correspond to the four noise parameters (F_{min}, R_n, $|G_{opt}|$ and $\angle|G_{opt}|$) in this study. Real encoding is adopted in this study. The generated random numbers have a range associated with a prior calculation or a prior knowledge..

Evolution function evaluates an individual's fitness. The objective function is developed in a way that it determines how close the randomly generated solutions are to the optimal solution. In this study, each chromosome is evaluated based on the objective function defined as (5.2).

Selection function simulates the mechanism of natural selection by which the gene with a smaller error function will have more chance to be inherited by the next generation. Roulette wheel selection is used most frequently, but when the fitness of different individuals varies widely, the optimization efficiency will be affected. Therefore, in this study, rank selection was applied, which was proven to be both suitable and effective.

Crossover operation simulates chromosomes' exchanging genes to create a new offspring. The new offspring will inherit advantages from the parents, the chromosomes in the last generation, in order to obtain a smaller error function.

Mutation operation is carried out by randomly changing one or more genes of the created offspring. It simulates the chromosomes' mutation in order to introduce new

characteristics that do not exist in the parents in order to increase the offspring's variance.

5.4 Results and Discussions

To test the proposed method, we set $W_{Bi} = W_{Gi} = 0$, $W_{Fi} = 1/F_i$ and reduce the root of (5.2) to unity and then (5.2) reduces to the error function used in Vasilescu method. Fig. 5.3 shows the calculated sum of error in our GA method using the experimental data sets in Table I [5]. As seen from Fig. 5.3, the calculated sum of error drops rapidly at the first 100 generations and finds the best solution: $F_{min} = 0.4546$ dB, $R_n = 4.8234$ Ω, $G_{opt} = 23.9379$ mS and $B_{opt} = 25.2417$ mS which yield the 0.643 % sum of error at the end of the search. The final result in the genetic search is almost the same as compared to the result in [8], which used the best combination of data sets in [5] (sets 1, 4, 5, 9), verifying the validity of the proposed method.

The advantage of Vasilescu method is that it requires no initial values and thus the method is widely used today [9]. However, the drawback is its time-consumption when the number of measured source admittance becomes very large. Fig. 5.4 gives the plot of computer-time as a function of the measured source impedance number for Vasilescu method and genetic search. Since Vasilescu method calculates the whole possible solutions, the computer-time increases approximately proportional to $N!/4!(N-4)!$ where N is the number of measured data sets. The computer-time of genetic search is mainly dependent on the number of generation and the population size, and thus seems to be constant as the measured data sets increases. It indicates the proposed method has better computation efficiency as compared to Vasilescu method.

In Fig. 5.5, the computed noise parameter standard deviation as a function of the number of measured source impedance N is shown both for the present and for the conventional method [3], [5]. For each N, one thousand different data sets were randomly selected from a source impedance constellation with forty normally distributed source impedances [7]. Then, noise parameters and standard deviations were calculated for each N case. The figure shows that a comparable noise parameter deviation is obtained as compared with conventional method.

Figure 5.6 gives the measured noise parameters of a 0.18-μm NMOSFET. As can be seen, in the frequency about 2 GHz, Lane's method fails to find the four noise parameters in the test device possibly due to an increasing uncertainty as $|\Gamma_{opt}|$ increases. Without an initial value from Lane's method, Mitama method and Boudiaf method fail to find the device's noise parameters. Only Vasilescu method can obtain a reasonable solution. However, Vasilescu method only considers error contribution from F_{min}. Thus the proposed method provides another choice for the computation of the four noise parameters.

5.5 Summary

In this chapter, a computation method for extracting noise parameters of a linear two-port network using a genetic algorithm is proposed. The developed method inherits the advantages of the Vasilescu's method of requiring no initial values. Besides, the computer-time of genetic search is independent on the number of measured source impedance and considers noise figure and source admittance errors simultaneously.

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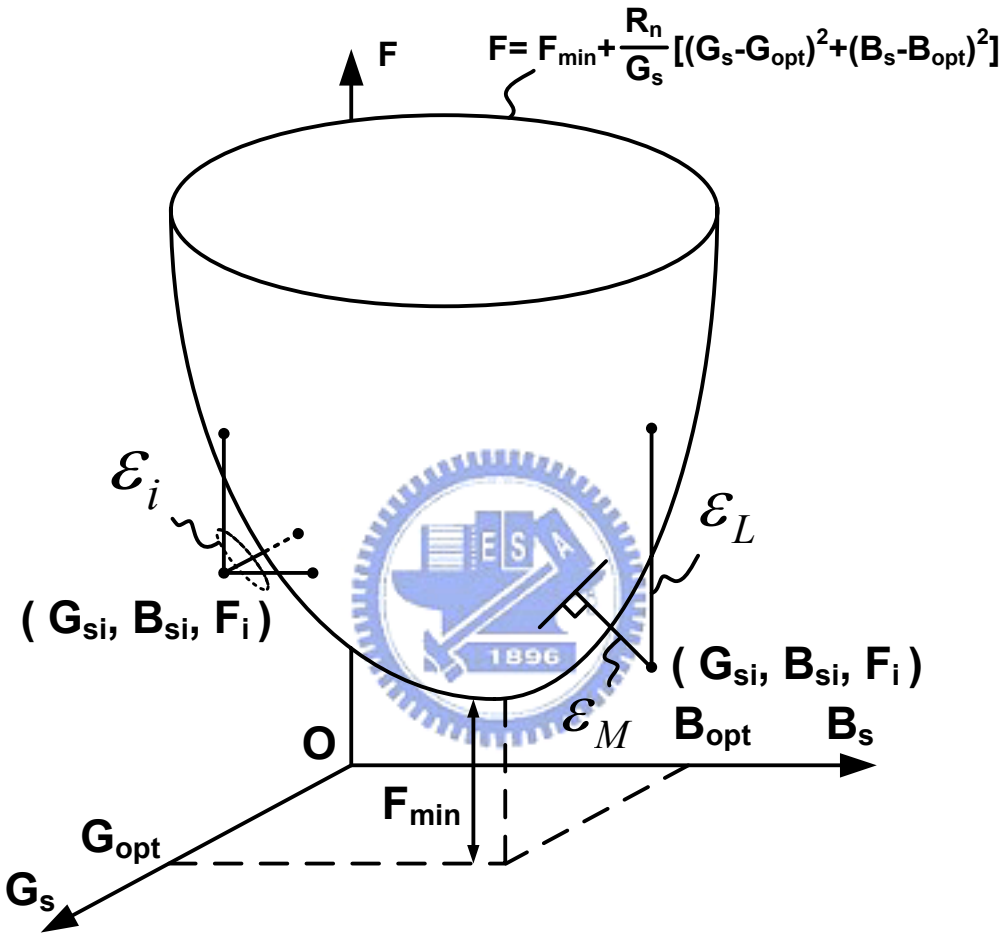


Fig. 5.1 Estimated error ε_i for the proposed method. The lines designated by ε_L and ε_M, represent the corresponding error function used in the conventional method [1], [2], respectively.

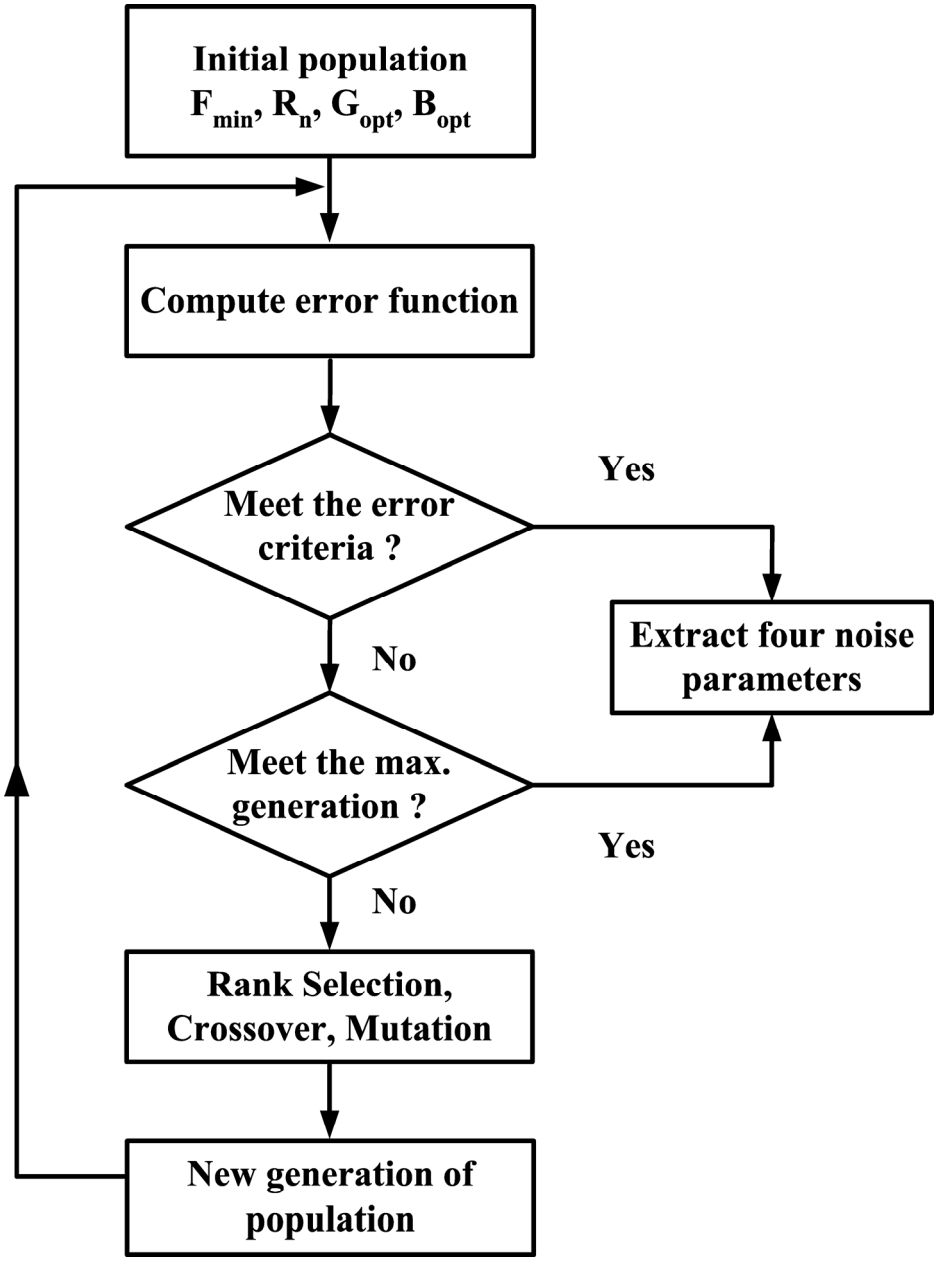


Fig. 5.2 Schematic flowchart of the GA used in this work.

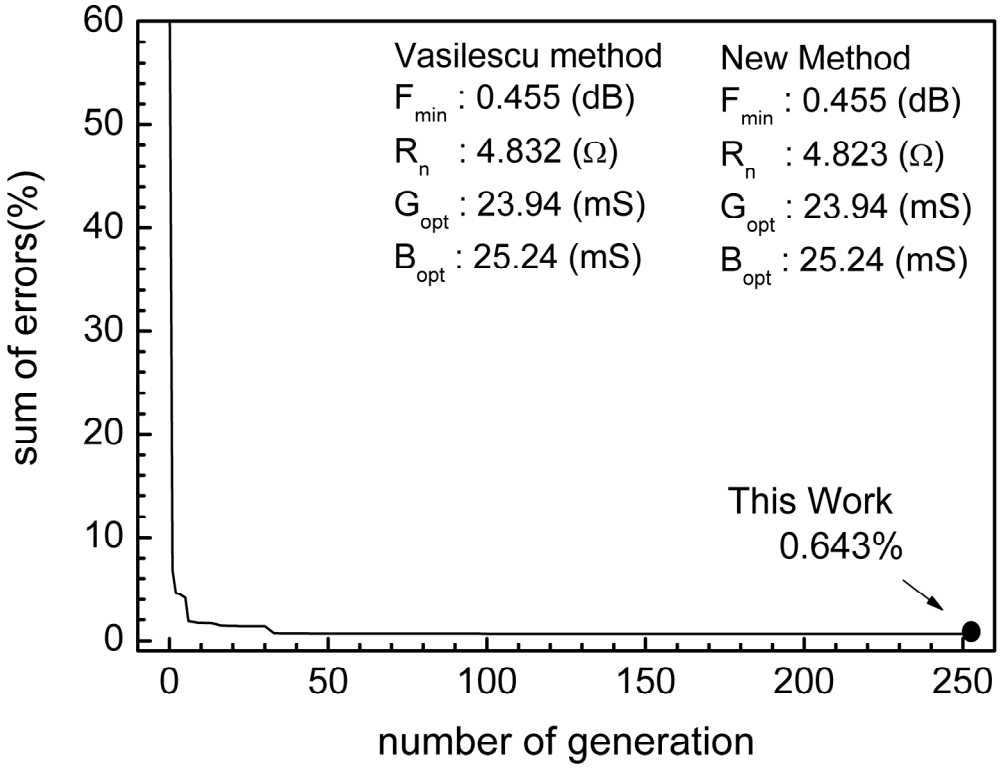


Fig. 5.3 Sum of error as a function of generation number for determination of noise parameters using genetic algorithms.

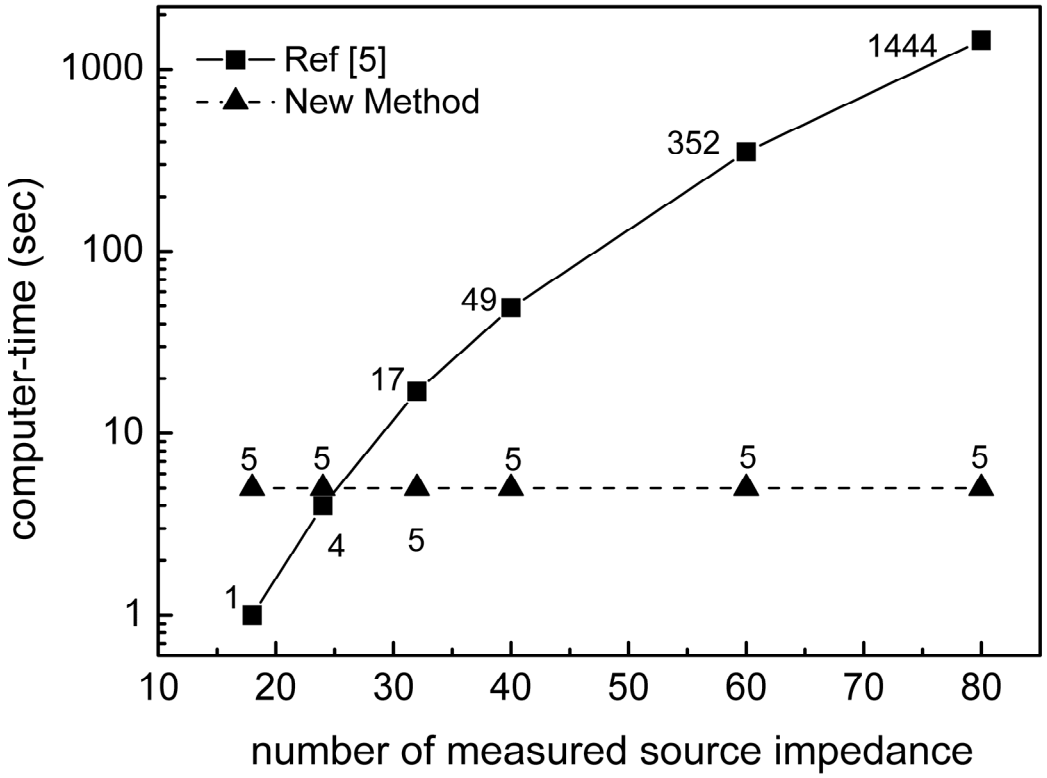


Fig. 5.4 Computation time as a function of number of measured source impedance. The computation of both methods are performed on a AMD-1.3GHz computer.

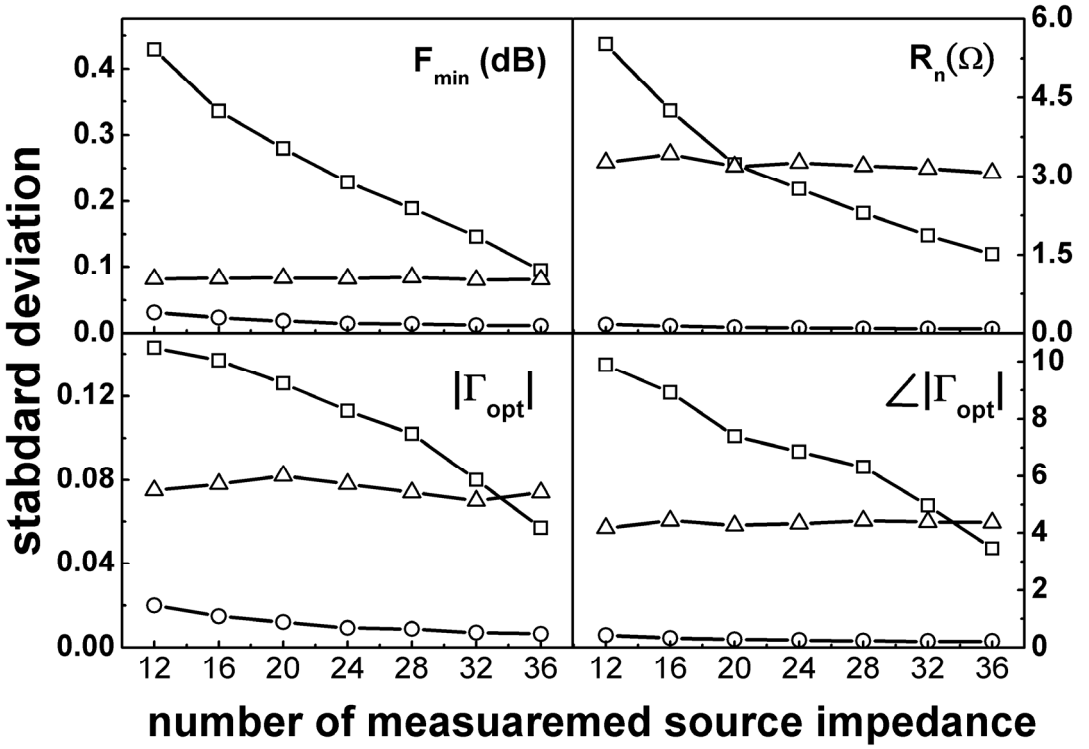


Fig. 5.5 The computed noise parameter standard deviation as a function of the number of measured source impedance. Circle: Mitima method, Triangle: Proposed method and Square: Vasilescu method.

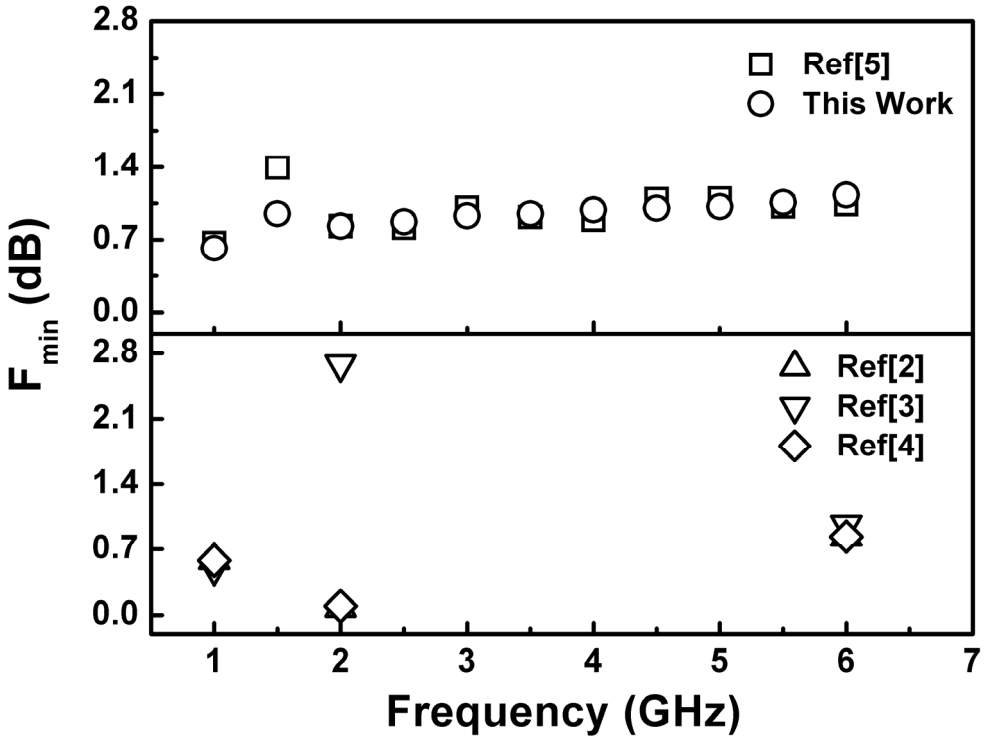


Fig. 5.6 Calculated four noise parameters using proposed computation method.

Chapter 6

Extraction of Base Current Noise, Collector Current Noise and Their Correlation of SiGe HBTs

6.1 Introduction of Noise Source Extraction

RF applications generally impose more serious device design constraints than digital applications. SiGe HBT technology, because it has higher intrinsic performance than Si BJT technology at similar process complexity and delivers better cost-performance than GaAs technology, has recently emerged as a contender for the RF market. Recently, modeling the noise of SiGe HBTs has received a lot of attention. Noise modeling is necessary for accurate prediction of noise behavior in radio frequency (RF) circuits. In a number of papers, the minimum noise figure and other quantities are being calculated from currents and resistances [1]-[4], or in terms of Y-parameters [5], [6]. All of these models predict the noise in terms of the measured (or modeled) currents and small-signal parameters, such that there is no need for difficult noise measurements.

The essence of SiGe HBTs RF noise modeling in these papers is to assume that the base and collector current noises are shot noise, with a power spectral density of $2qI_B$ and $2qI_C$, respectively [7]. The base and collector current noises are also assumed to be uncorrelated. Such an approach is used by SPICE Gummel-Poon, VBIC, Mextram, and Hicum models. However, at high frequencies, such an approach may be no longer valid. The base and collector current noises may be no longer shot like, and

their correlation may become appreciable [8]. In this chapter, a systematic procedure to extract the base current noise (S_{ib}), collector current noise (S_{ic}), and their cross correlation $S_{ib,ic*}$ directly from the S-parameter and RF noise parameter measurement is presented. We extract the base and collector current noises of SiGe HBTs by de-embedding transistor parasitics from measured noise parameters. We develop a systematic four-port Y-parameters calculation method which can be applied in the de-embedding of noise contribution from the transistor parasitic. The extracted noise current of SiGe HBTs fabricated in a 0.35 μm BiCMOS technology versus frequency, bias condition are presented and discussed.

6.2 Four-Port Parasitic De-embedding Theory

First, we shall establish in this section, the theoretical basis for the four-port parasitic de-embedding scheme by following mathematical treatment developed in [9], [10]. As shown in Fig. 6.1, the general two-port network is treated as a four-port network. Let ports 1 and 2 of the network be denoted as the external ports, and the corresponding voltages and currents as the external voltages and currents. Let ports 3 and 4 denote the internal ports, and the corresponding notation for the voltages and currents. Let V_e and I_e be the extrinsic voltage and current vectors, and V_i and I_i be the intrinsic voltage and current vectors [11]

$$\begin{pmatrix} V_e \\ V_i \end{pmatrix} = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix}. \tag{6.1}$$

Thus, we have [10]

$$\begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix}. \tag{6.2}$$

where $[Y_{ee}]$, $[Y_{ei}]$, $[Y_{ie}]$, and $[Y_{ii}]$ are four 2×2 matrices. Hence, the extrinsic Y-parameters and the intrinsic device Y-parameters can then be related as

$$Y^{DUT} V_e = Y_{ee} V_e + Y_{ei} V_i \tag{6.3}$$

and

$$-Y^{INT} V_i = Y_{ie} V_e + Y_{ii} V_i \tag{6.4}$$

where Y^{INT} and Y^{DUT} are the intrinsic device Y-parameters and the two-port Y-parameters of the DUT, respectively. One thus obtain

$$Y^{INT} = -Y_{ie} \left(Y^{DUT} - Y_{ee} \right)^{-1} Y_{ei} - Y_{ii}. \tag{6.5}$$

Once the 16 variables of the 4×4 matrix ($[Y_{ee}]$, $[Y_{ei}]$, $[Y_{ie}]$, and $[Y_{ii}]$) are known, one can build the appropriate one-to-one relationship between the extrinsic and intrinsic Y-parameters.

6.3 Four-Port Noise De-embedding Theory

To simplify the noise de-embedding procedure and apply it to broadband noise extraction, we use the noise current correlation matrix *SY* to represent a generalized noisy system. In a two-port system, the minimum noise figure F_{min}, noise impedance R_n, and optimum noise admittance Y_{opt} can be directly converted into the noise current correlation matrix SY_2.

$$SY_2 = \begin{bmatrix} \overline{i_{n,1}i_{n,1}^*} & \overline{i_{n,1}i_{n,2}^*} \\ \overline{i_{n,2}i_{n,1}^*} & \overline{i_{n,2}i_{n,2}^*} \end{bmatrix} = \begin{bmatrix} \overline{i_{n,1}i_{n,1}^*} & \overline{i_{n,1}i_{n,2}^*} \\ \overline{i_{n,2}i_{n,1}^*} & \overline{i_{n,2}i_{n,2}^*} \end{bmatrix}. \tag{6.6}$$

Figure 6.2 shows the equivalent circuit of the noise model of a two-port DUT. For accurately modeling the four-port parasitic noise behavior, four noise current sources $\vec{i}_n$ and the 4×4 noise current correlation matrix SY_4 are used. The noise current sources and the correlation matrix can be written as

$$SY_4 = \begin{bmatrix} SY_{n,11} & SY_{n,12} & SY_{n,13} & SY_{n,14} \\ SY_{n,21} & SY_{n,22} & SY_{n,23} & SY_{n,24} \\ SY_{n,31} & SY_{n,32} & SY_{n,33} & SY_{n,34} \\ SY_{n,41} & SY_{n,42} & SY_{n,43} & SY_{n,44} \end{bmatrix} = \begin{bmatrix} \overline{i_{n,1}i_{n,1}^*} & \overline{i_{n,1}i_{n,2}^*} & \overline{i_{n,1}i_{n,3}^*} & \overline{i_{n,1}i_{n,4}^*} \\ \overline{i_{n,2}i_{n,1}^*} & \overline{i_{n,2}i_{n,2}^*} & \overline{i_{n,2}i_{n,3}^*} & \overline{i_{n,2}i_{n,4}^*} \\ \overline{i_{n,3}i_{n,1}^*} & \overline{i_{n,3}i_{n,2}^*} & \overline{i_{n,3}i_{n,3}^*} & \overline{i_{n,3}i_{n,4}^*} \\ \overline{i_{n,4}i_{n,1}^*} & \overline{i_{n,4}i_{n,2}^*} & \overline{i_{n,4}i_{n,3}^*} & \overline{i_{n,4}i_{n,4}^*} \end{bmatrix} = \overline{\vec{i}_n \vec{i}_n^{\dagger}} \tag{6.7}$$

where $SY_{n,ij}$, i and j = 1,2,3,4 are the noise current correlation between ports i and j. For brevity, $\vec{i}_n$ and SY_4 are also written as

$$\vec{i}_n = \begin{pmatrix} i_{n,1} \\ i_{n,2} \\ i_{n,3} \\ i_{n,4} \end{pmatrix} = \begin{pmatrix} i_{n,e} \\ i_{n,i} \end{pmatrix} \tag{6.8}$$

and

$$SY_4 = \begin{bmatrix} SY_{n,ee} & SY_{n,ei} \\ SY_{n,ie} & SY_{n,ii} \end{bmatrix} = 4kT\,\mathrm{Re}\left(\begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \right) \tag{6.9}$$

where $\overrightarrow{i_{n,e}}$ and $\overrightarrow{i_{n,i}}$ are extrinsic and intrinsic noise current sources, respectively. The four-port I-V relation of the DUT, considering noise currents, can then be written as

$$\begin{pmatrix} I_e + i_{n,e} \\ I_i + i_{n,i} + i_{n,\mathrm{int}} \end{pmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix}. \tag{6.10}$$

One can thus calculate the intrinsic noise correlation matrix as [10]

$$SY_{n,\mathrm{int}} = D^{-1}\left(SY_{n,total} - SY_{n,ee}\right)\left(D^{+}\right)^{-1} - SY_{n,ii} - D^{-1}SY_{n,ei} - SY_{n,ie}\left(D^{+}\right)^{-1} \tag{6.11}$$

where $D = -Y_{ei}\left(Y^{INT} + Y_{ii}\right)^{-1}$.

6.4 Calculation of 4×4 Four-Port Y matrix of DUT

From (6.5) and (6.11), the 4×4 matrix, ([Y_{ee}], [Y_{ei}], [Y_{ie}], and [Y_{ii}]), play an important role on the whole parasitic and noise de-embedding theory. However, most researchers use circuit simulator [12] or the test structure [9] to obtain the four-port Y matrix. In this section, direct calculation of the 4×4 matrix from the nodal matrix is presented. Once the 4×4 matrix is obtained, the intrinsic noise source is obtained by substituting the 4×4 matrix back to (6.5) and (6.11).

6.4.1 Operand Definition

Once the nodal matrix of the two-port network is formulated, we can obtain the 4×4 four-port Y matrix by perfoming some simple operands on the nodal matrix. The detail of the operands is given in this section. The operand to eliminate node n in the matrix is defined as

$$Y'_{i,j} = Y_{i,j} - \frac{Y_{n,j} \times Y_{i,n}}{Y_{n,n}}. \tag{6.12}$$

The operand to combinate node m to node n in the matrix is defined as

$$Y'_{i,n} = Y_{i,n} + Y_{i,m} \tag{6.13}$$

and

$$Y'_{n,j} = Y_{n,j} + Y_{m,j}. \tag{6.14}$$

Once the row and column element of node m is combinated to that of node *n*, the node *m* is then eliminated from the nodal matrix. The operand to short node *n* to ground is defined as

$$Y'_{i,n} = Y_{i,n+1} \tag{6.15}$$

and

$$Y'_{n,j} = Y_{n+1,j}. \tag{6.16}$$

The operand to change reference voltage to node *n* is defined as

$$Y'_{i,n} = \sum_{1 \text{ to } n-1} Y_{i,x} \tag{6.17}$$

and

$$Y'_{n,j} = \sum_{1 \text{ to } n-1} Y_{x,j} \,. \tag{6.18}$$

6.4.2 Calculation of Y_{ee} and Y_{ii}

We use a simple two-port network to illustrate how to calculate the $[Y_{ee}]$ and $[Y_{ii}]$ with the defined operands. Fig. 6.3 shwos the adopted two-port network. The network cotains five nodes and therefore we can write down a 5×5 nodal matrix as

$$M_{5\times5} = \begin{bmatrix} Y_1+Y_2 & 0 & -Y_2 & 0 & 0 \\ 0 & Y_3 & 0 & -Y_3 & 0 \\ -Y_2 & 0 & Y_2 & 0 & 0 \\ 0 & -Y_3 & 0 & Y_3+Y_4 & 0 \\ 0 & 0 & 0 & 0 & Y_5 \end{bmatrix}. \tag{6.19}$$

From the definition, $[Y_{ee}]$ is defined as the I_e/V_e when node 3, 4 and 5 are short together. Performing (6.13) and (6.14) to short node 5 and node 4 to node 3, we arrive at following 3×3 nodal matrix

$$M_{ee,3\times3} = \begin{bmatrix} Y_1+Y_2 & 0 & -Y_2 \\ 0 & Y_3 & -Y_3 \\ -Y_2 & -Y_3 & Y_2+Y_3+Y_4+Y_5 \end{bmatrix}. \tag{6.20}$$

By removing the node 3 from 3×3 nodal matrix using (6.12), $[Y_{ee}]$ is obtained as

$$[Y_{ee}] = \begin{bmatrix} Y_1 + Y_2 - \dfrac{Y_2 \times Y_2}{\Sigma} & -\dfrac{Y_2 \times Y_3}{\Sigma} \\ -\dfrac{Y_2 \times Y_3}{\Sigma} & Y_3 - \dfrac{Y_3 \times Y_3}{\Sigma} \end{bmatrix} \tag{6.21}$$

where $\Sigma = Y_2 + Y_3 + Y_4 + Y_5$.

$[Y_{ii}]$ is dedined as I_i/V_i when node 1, 2 are short to ground. Performing (6.15) and (6.16) on the 5×5 nodal matrix, we arrive at

$$M_{ii,3\times3} = \begin{bmatrix} Y_2 & 0 & 0 \\ 0 & Y_3 + Y_4 & 0 \\ 0 & 0 & Y_5 \end{bmatrix}. \tag{6.22}$$

Changing the reference voltage of the network to node 5 by using (6.17) and (6.18), we obtain

$$M'_{ii,3\times3} = \begin{bmatrix} Y_2 & 0 & Y_2 \\ 0 & Y_3 + Y_4 & Y_3 + Y_4 \\ Y_2 & Y_3 + Y_4 & \Sigma \end{bmatrix}. \tag{6.23}$$

By removing the node 5 from 3×3 nodal matrix using (6.12), $[Y_{ii}]$ is obtained as

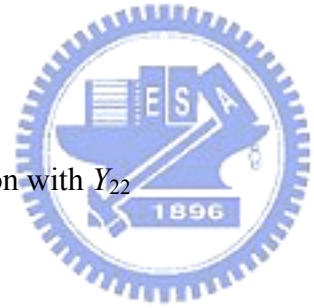
$$[Y_{ii}] = \begin{bmatrix} Y_2 - \dfrac{Y_2 \times Y_2}{\Sigma} & -\dfrac{Y_2 \times (Y_3 + Y_4)}{\Sigma} \\ -\dfrac{Y_2 \times (Y_3 + Y_4)}{\Sigma} & Y_3 + Y_4 - \dfrac{(Y_3 + Y_4) \times (Y_3 + Y_4)}{\Sigma} \end{bmatrix}. \tag{6.24}$$

6.4.3 Calculation of Y_{ei} and Y_{ie}

$[Y_{ei}]$ and $[Y_{ie}]$ are defined as I_e/V_i when V_e equals to zero and I_i/V_e when V_i equals to zero, respectively. Since calculation of $[Y_{ei}]$ and $[Y_{ie}]$ involves two different reference voltages, it is hard to calculate $[Y_{ei}]$ and $[Y_{ie}]$ directly using simple operand defined in Sec 6.4.1. However, with a small modification in the nodal matrix, $[Y_{ei}]$ and $[Y_{ie}]$ can be easily obtained.

Y_{32} and Y_{42} is calculated when the port 1 is shorted to ground and port 3, 4 and 5 are tied together. Performing operands (6.13)-(6.16), (6.19) is reduced to

$$M_{2\times 2,32} = \begin{bmatrix} Y_3 & -Y_3 \\ -Y_3 & \Sigma \end{bmatrix}. \tag{6.25}$$



Also, Y_{32} has following relation with Y_{22}

$$Y_{32} = Y_{22}\frac{i_3}{i_2} \tag{6.26}$$

where $i_3 = Y_2 \times V_3$. Therefore, Y_{32} is obtained as

$$Y_{32} = Y_{22}\frac{Y_2 \times \mathrm{Det}\begin{bmatrix} Y_3 & 1 \\ -Y_3 & 0 \end{bmatrix}}{D} \tag{6.27}$$

where D is determine of (6.25). In a similar way, Y_{42} ($i_4 = -(Y_2 + Y_5)\times V_3$) is derived as

$$Y_{42} = Y_{22}\frac{-(Y_2 + Y_5) \times \mathrm{Det}\begin{bmatrix} Y_3 & 1 \\ -Y_3 & 0 \end{bmatrix}}{D}. \tag{6.28}$$

Y_{31} and Y_{41} is calculated when the port 2 is shorted to ground and port 3, 4 and 5

are tied together. Performing operands (6.13)-(6.16), (6.19) is reduced to

$$M_{2\times2,31}=\begin{bmatrix} Y_1+Y_2 & -Y_2 \\ -Y_2 & \Sigma \end{bmatrix}. \tag{6.29}$$

With a similar procedure used in Y_{32} and Y_{42}, Y_{31} ($i_3 = Y_2\times(V_3 - V_1)$) and Y_{41} ($i_4 = (Y_3 + Y_4)\times V_3$) is obtained as

$$Y_{31}=Y_{11}\frac{Y_2\times\left(\mathrm{Det}\begin{bmatrix} Y_1+Y_2 & 1 \\ -Y_2 & 0 \end{bmatrix}-\mathrm{Det}\begin{bmatrix} 1 & -Y_2 \\ 0 & \Sigma \end{bmatrix}\right)}{D} \tag{6.30}$$

and

$$Y_{32}=Y_{11}\frac{\left(Y_3+Y_4\right)\times\mathrm{Det}\begin{bmatrix} Y_1+Y_2 & 1 \\ -Y_2 & 0 \end{bmatrix}}{D} \tag{6.31}$$

where D is determine of (6.29).

Since the extrinsic circuit is often constituted with parasitic elements, the $[Y_{ei}]$ will equal to $[Y_{ie}]$. To calculate $[Y_{ei}]$ manually, we can perform operands (6.13)-(6.16), (6.19) is reduced to

$$M_{2\times2,13}=\begin{bmatrix} Y_2 & 0 \\ 0 & Y_3+Y_4+Y_5 \end{bmatrix} \tag{6.32}$$

and

$$M_{2\times2,14}=\begin{bmatrix} Y_2+Y_5 & 0 \\ 0 & Y_3+Y_4 \end{bmatrix}. \tag{6.33}$$

With a similar procedure used in Y_{31} and Y_{41}, Y_{13} ($i_1 = -Y_2\times V_3$) and Y_{23} ($i_2 = -Y_3\times V_4$) is

obtained as

$$Y_{13} = -Y_{33}\frac{Y_2 \times \mathrm{Det}\begin{bmatrix} 1 & 0 \\ -1 & Y_3+Y_4+Y_5 \end{bmatrix}}{D} \tag{6.34}$$

and

$$Y_{23} = -Y_{33}\frac{Y_3 \times \mathrm{Det}\begin{bmatrix} Y_2 & 1 \\ 0 & -1 \end{bmatrix}}{D} \tag{6.35}$$

where D is determine of (6.32). Performing similar procedure on (6.33), Y_{14} ($i_1 = -Y_2 \times V_3$) and Y_{24} ($i_2 = -Y_3 \times V_4$) is obtained as

$$Y_{14} = -Y_{44}\frac{Y_2 \times \mathrm{Det}\begin{bmatrix} -1 & 0 \\ 1 & Y_3+Y_4 \end{bmatrix}}{D} \tag{6.36}$$

and

$$Y_{24} = -Y_{44}\frac{Y_3 \times \mathrm{Det}\begin{bmatrix} Y_2+Y_5 & -1 \\ 0 & 1 \end{bmatrix}}{D} \tag{6.37}$$

where D is determine of (6.33).

6.5 Results and Discussions

The SiGe HBTs used in this study are from a 25 GHz typical f_T BiCMOS technology with an emitter area of 3×0.34×8 μm^2. S-parameters are measured on-chip using HP8510 and noise parameters are measured using ATN NP5B. Pad de-embedding is done using an open structure. The small-signal equivalent circuit used in this chapter is constructed based on physical device structure as shown in Fig.

6.4.

Enclosed in the dash box is the intrinsic transistor as been derived in chapter 2. Noise sources are drawn as filled sources. The major noise sources are the thermal noise of the thermal resistance, both intrinsic and extrinsic, and the intrinsic transistor base and collector current noises, shown as S_{ib} and S_{ic}. The equivalent circuit parameters are extracted using the method proposed in chapter 3. Excellent modeling of Y-parameters is obtained at the interested frequency range and current bias conditions. Using the equivalent circuit parameters extracted, the correlation matrix of the base and collector current noises is extracted from the noise correlation matrix of DUT by removing the extrinsic elements outside the dash box through (6.11) with the proposed 4×4 matrix. The noise source extraction procedure is followed the flow chart shown in Fig. 6.5.

Figure 6.6 shows the comparison between the measured S-parameters from ATN NP5B and modeled S-parameters extracted from the measured S-parameters using HP8510. Good agreement is obtained in the interested frequency range. Fig. 6.7 shows the extracted S_{ib} for the bias condition of I_B = 2 μA, 10 μA and 20 μA. From Fig. 6.7, we found that the extracted S_{ib} is strongly frequency dependent and match to the theoretic estimation (solid line in the figure) only at low frequency range. This can provide experimental evidence for the frequency dependence of S_{ib} observed using microscopic noise simulation [8]. In [13], non-quasi-static assumption is used to explain any frequency dependence in S_{ib} and a delay resistance R_d is put in series with C_π to give rise to a frequency dependent of S_{ib}. Here, we suggest S_{ib} modifies slightly

to $2qI_B(1+\alpha f)$.

Figure 6.8 shows the extracted S_{ic} for the bias condition of I_B = 2 μA, 10 μA and 20 μA. The bias dependence of S_{ic} is shown in Fig. 6.9. We found that the extracted S_{ic} is frequency independent and is matched to the theoretic estimation (solid line in the figure) only at low base current region. The power spectral of S_{ic} equals to $2qI_C$ is used in SPICE model and Transport noise model [14]. The extracted results show that the assumption of $2qI_C$ may not give a good simulation result at high current region. A modification of S_{ic} is suggested as $2\beta qI_C$ where β is function of bias current. However, in [12], S_{ic} is found to be higher than the theoretic estimation, $2qI_C$. The additional noise is thought to be contributed by base majority carrier velocity fluctuations, which becomes more important with increasing injection level. To investigate physical basics of S_{ic}, more accurate measurement should be performed at the high current region.

Figure 6.10 shows the correlation coefficient between S_{ib} and S_{ic} versus frequency. For the SPICE model, the correlation coefficient is assumed to be zero. In this study, the extracted correlation coefficient is small but increases as bias current increases. However, we can not assure the extracted correlation coefficient is physical meaningful because the extracted S_{ib} is sensitive to the measurement error. To test the accuracy of extracted S_{ib} and S_{ic}, $SY_{n,int}$ is assumed to be as

$$SY_{n,\mathrm{int}} = \frac{1}{2}\times\begin{bmatrix} 2qI_B(1+\alpha f) & 2qI_C\left(e^{jw\tau}-1\right) \\ 2qI_C\left(e^{-jw\tau}-1\right) & 2q\beta I_C \end{bmatrix}. \tag{6.39}$$

(6.39) is the assumption that $S_{ib} = 2qI_B(1 + \alpha f)$, $S_{ic} = 2q\beta I_C$ and their correlation equals to $2qI_C(e^{-jw\tau}-1)$ [15] where τ is the noise transit time of SiGe HBTs [14]. Reversing (6.11) into

$$SY_{n,total} = SY_{n,ee} + D\left(SY_{n,\text{int}} + SY_{n,ii} + D^{-1}SY_{n,ei} + SY_{n,ie}\left(D^{+}\right)^{-1}\right)D^{+} \tag{6.40}$$

and substituting (6.39) into (6.40), we can obtain the total noise performance of the interested SiGe HBTs. The simulation results of four noise parameters based on (6.40) are shown in Fig. 6.11 for the bias condition of $I_B = 14$ μA. The assumption used in (6.39) can well model the four noise parameters. The slightly deviation in Angle(Γ_{opt}) is probably caused by the measurement difference between ATN-NP5B and HP-8510. What also shown in Fig. 6.11 are four noise parameters extraction results for the intrinsic part HBTs. From Fig. 6.11(a), the frequency dependence of F_{min} is mainly caused by the extrinsic circuit elements. The F_{min} of intrinsic HBTs shows negligible frequency dependence. Therefore, for a wireless circuit, to obtain a better noise performance, the effect of extrinsic circuit elements should be minimized.

From Fig. 6.11(b), R_n is frequency independent both for the intrinsic part and total noise performance. The difference between intrinsic part R_n and total R_n roughly equals to the total base resistance, $R_{bi} + R_{bx}$ [16]. Therefore, in wireless circuits, a lower base resistance is required for a better noise performance. Figure 6.11(c) and Fig. 6.11(d) show the frequency dependence of Mag(G_{opt}) and Angle(G_{opt}), respectively. The Angle(G_{opt}) of intrinsic part HBT is f higher than that of total HBT. The mag(G_{opt}) of intrinsic part HBT shows negligible frequency dependence. Lower

frequency dependence of mag(G_{opt}) is preferred for the noise matching in wireless circuits.

6.6 Summary

In this chapter, a complete noise source extraction technique of SiGe HBTs is developed to extract the base and collector current noise and their correlation for 25GHz f_T SiGe HBTs. Unlike conventional methods, a four-port noise source de-embedded technique is used to remove the influence of extrinsic circuit elements. Simple operands is defined and then performed to obtain 4×4 four-port Y-parameters, ([Y_{ee}], [Y_{ei}], [Y_{ie}], and [Y_{ii}]). The base current noise is frequency dependent, while the collector current noise equals to $2qI_C$, but remains white. Their correlation is frequency dependent and cannot be neglected. The extracted base current noise and correlation is sensitive to measurement error. A more accurate measurement is required to obtain the real base current noise and correlation.

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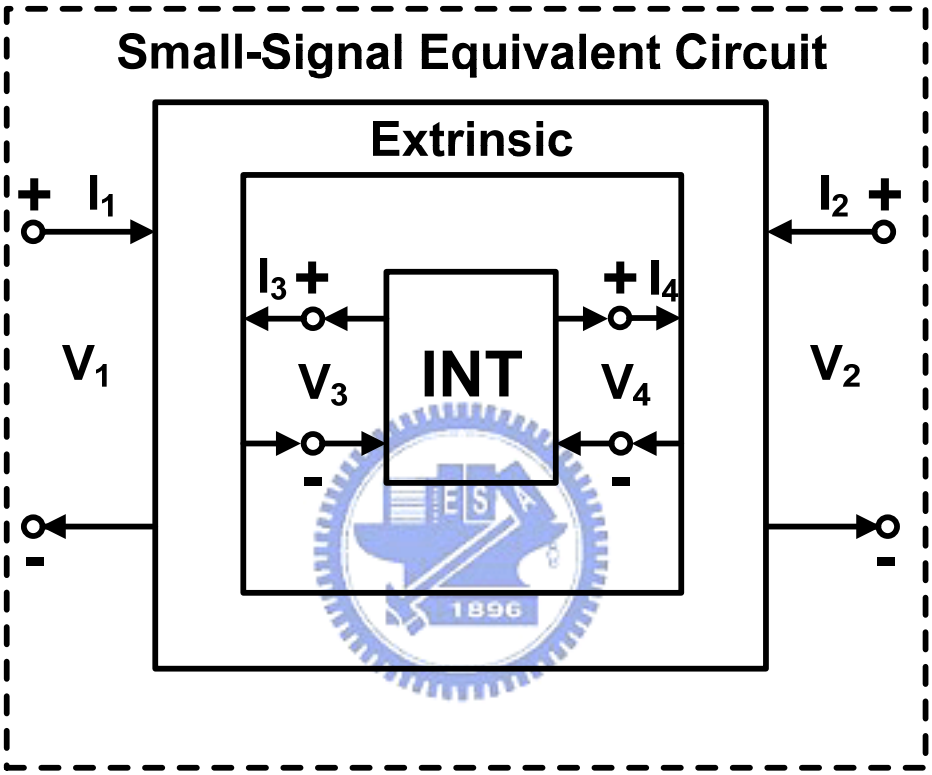


Fig. 6.1 Illustration of a general four-port structure. The two extrinsic ports of the DUT are denoted ports 1 and 2, and the two ports of intrinsic device (INT) are denoted ports 3 and 4.

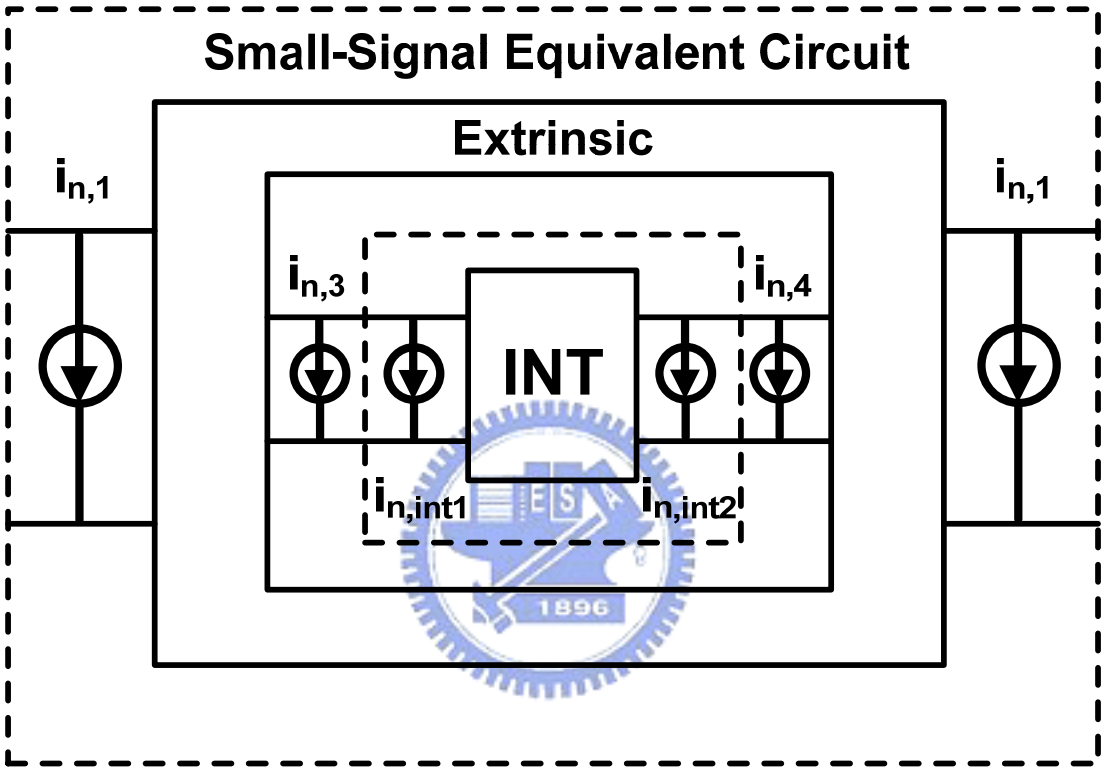


Fig. 6.2 Equivalent circuit of the noise model of the DUT. Here, i_{n1}, i_{n2}, i_{n3}, and i_{n4} are noise current sources at ports 1–4, respectively, and $i_{n,int1}$ and $i_{n,int2}$ are the noise current sources of the intrinsic two-port system.

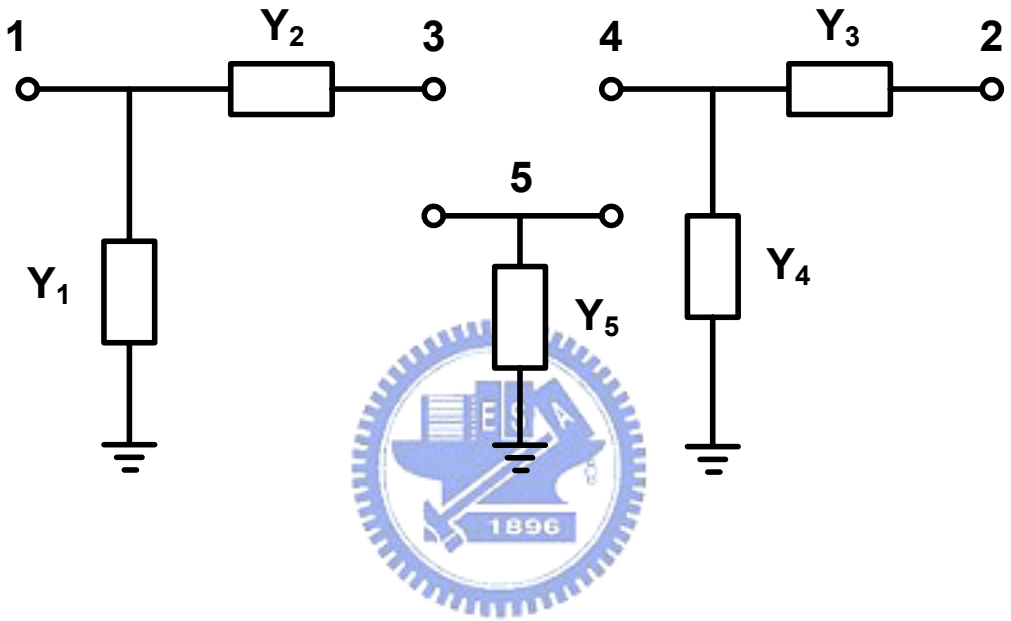


Fig. 6.3 A simple two-port network used for calculating the 4×4 four-port Y-parameters.

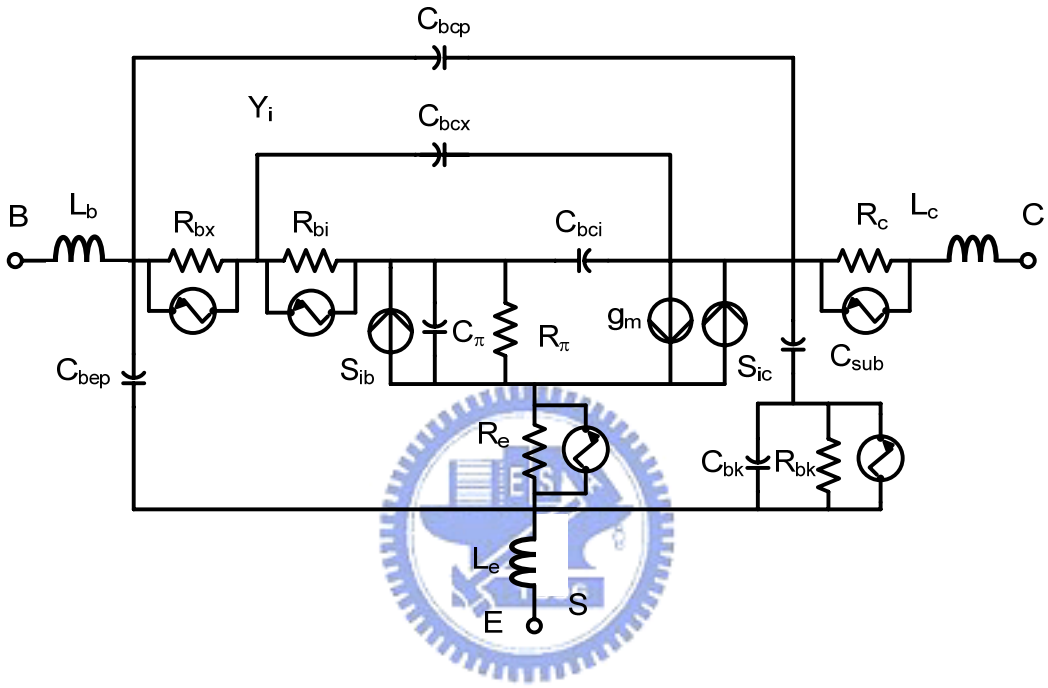


Fig. 6.4 Small-signal equivalent circuit of SiGe HBTs and corresponding noise sources.

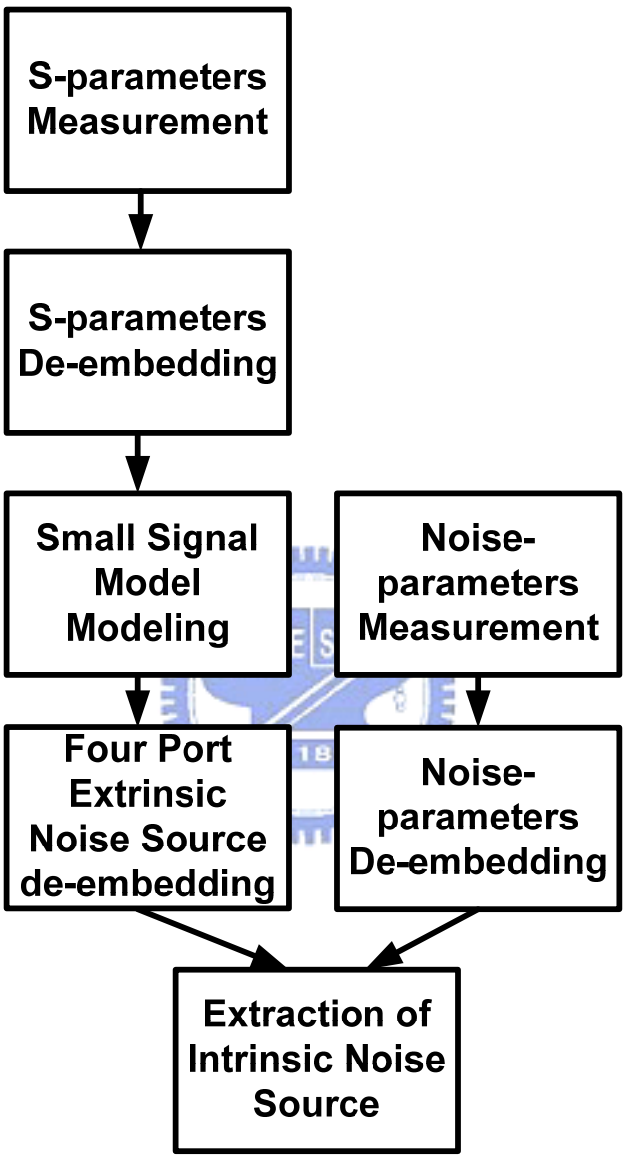


Fig. 6.5 Flow chart of extraction of intrinsic noise sources.

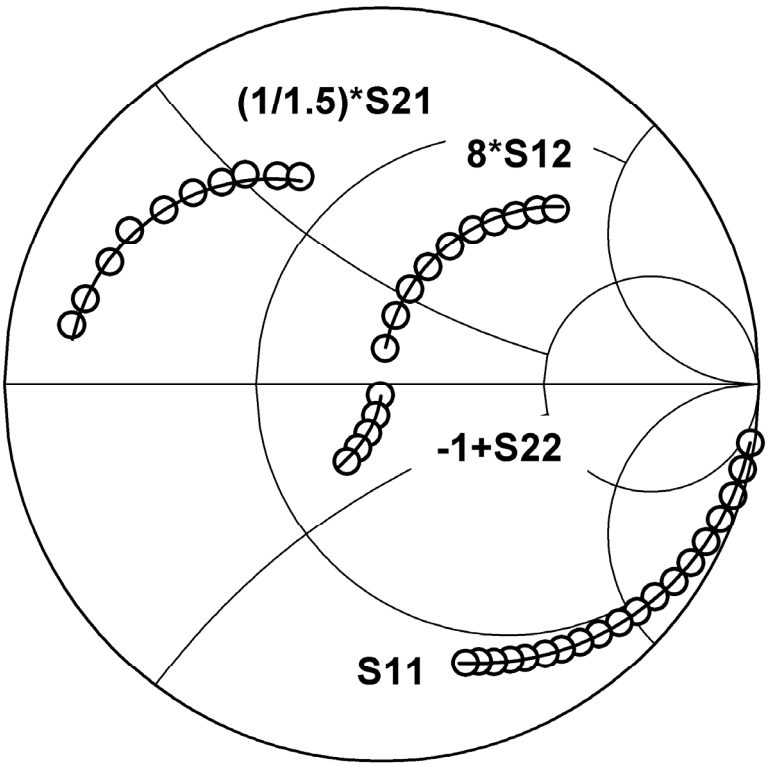


Fig. 6.6 Comparison of modeling results extracted from S-parameters measured from HP-8510 with measured S-parameters from ATN-NP5B.

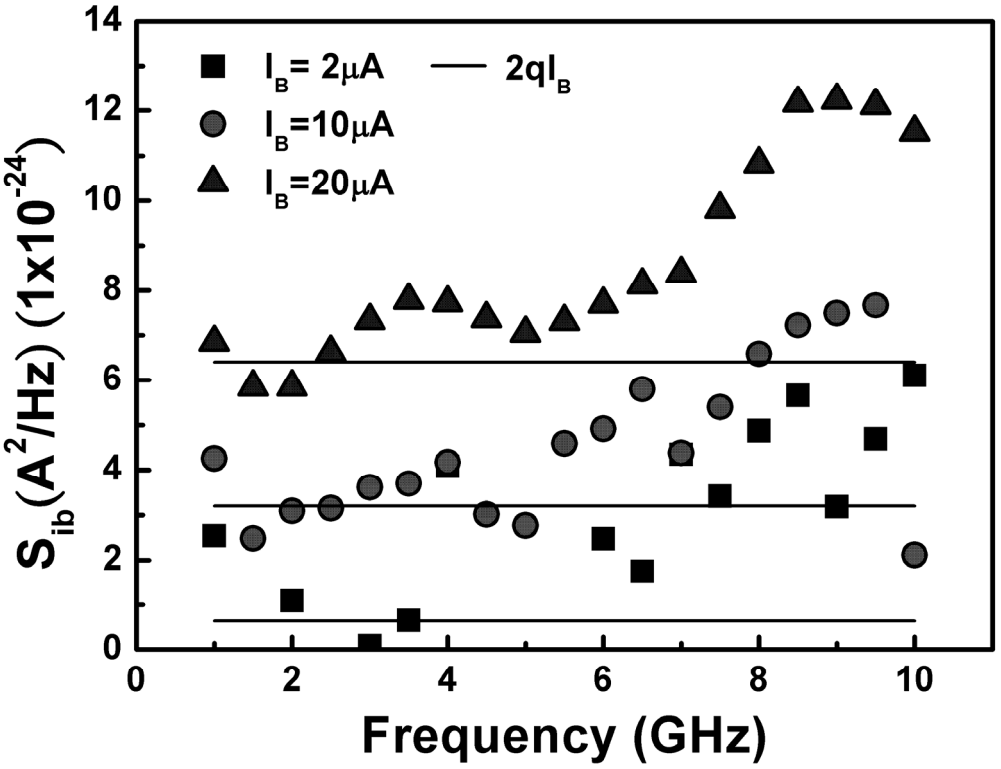


Fig. 6.7 Extracted base current noise versus frequency.

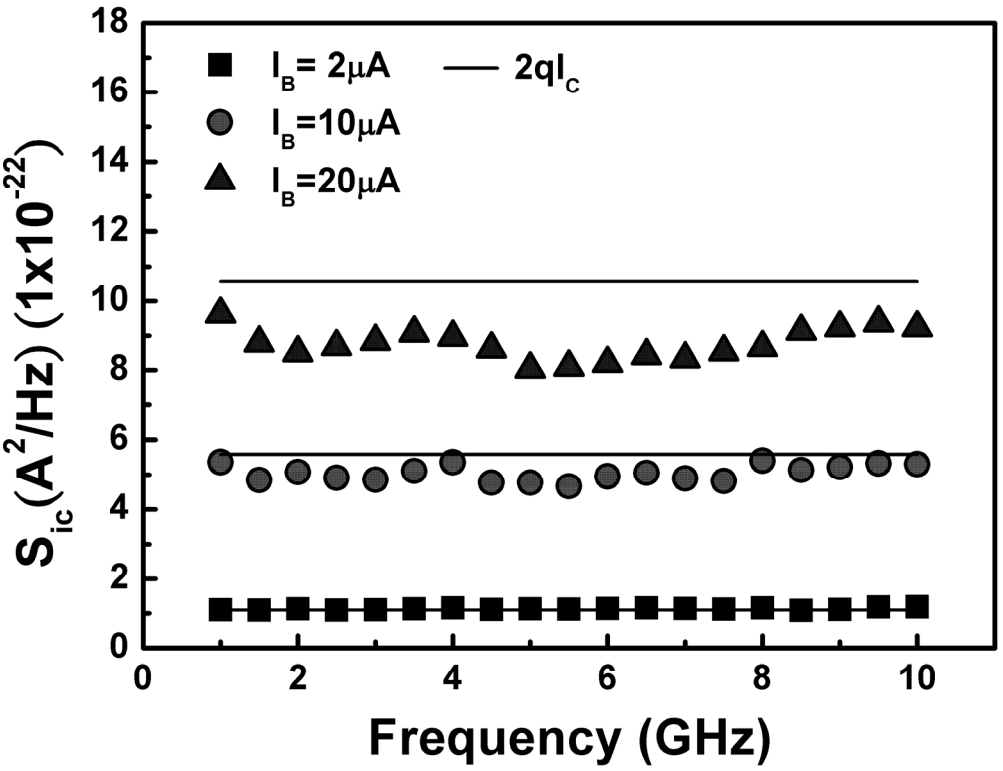


Fig. 6.8 Extracted collector current noise versus collector current.

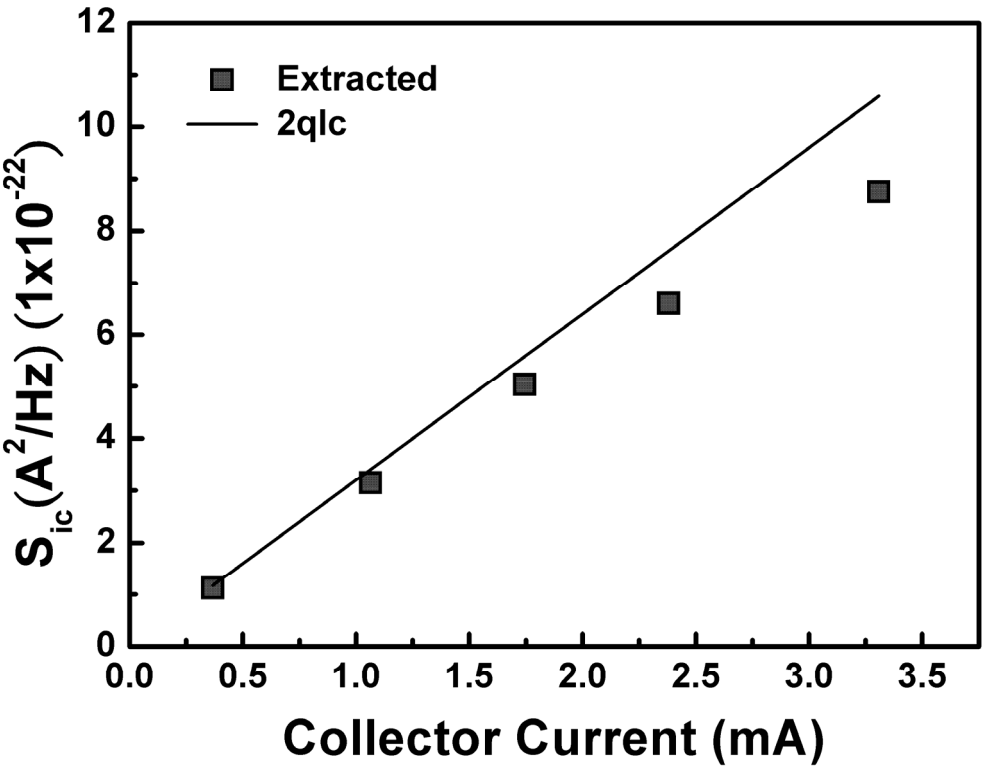


Fig. 6.9 Extracted collector current noise versus collector current.

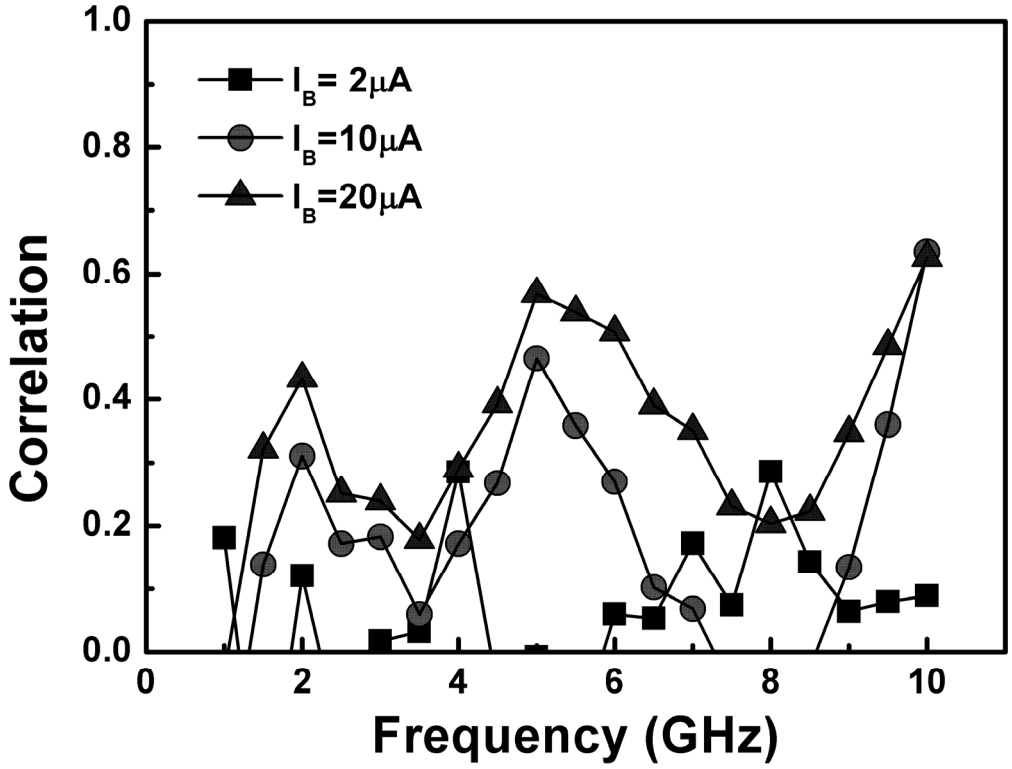
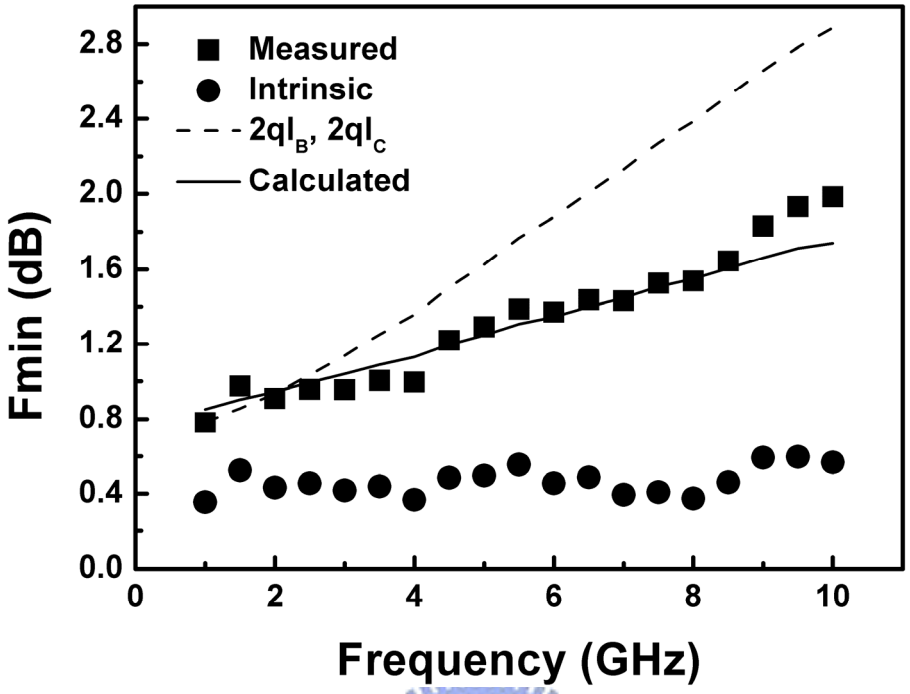
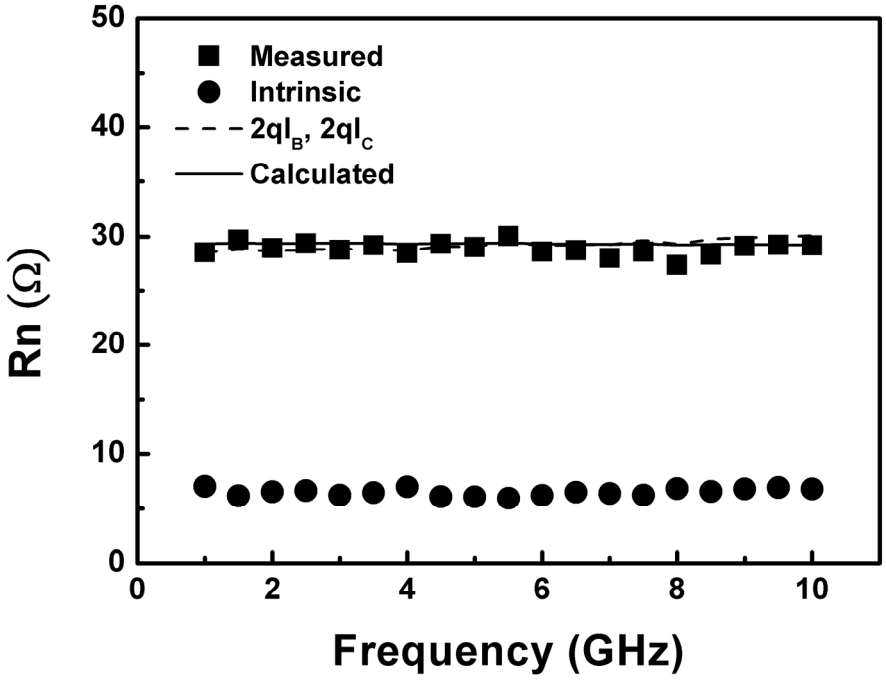


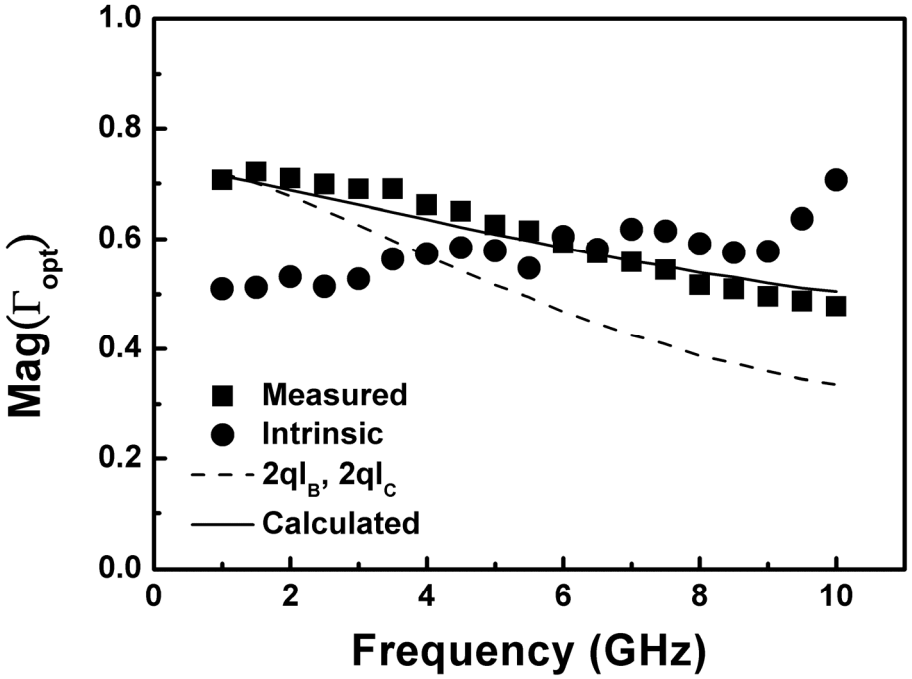
Fig. 6.10 Extracted correlation between base current noise and collector current noise.


Measured
Intrinsic
2qlB, 2qlC
Calculated
Fmin (dB)
Frequency (GHz)
0.0
0.4
0.8
1.2
1.6
2.0
2.4
2.8
0
2
4
6
8
10

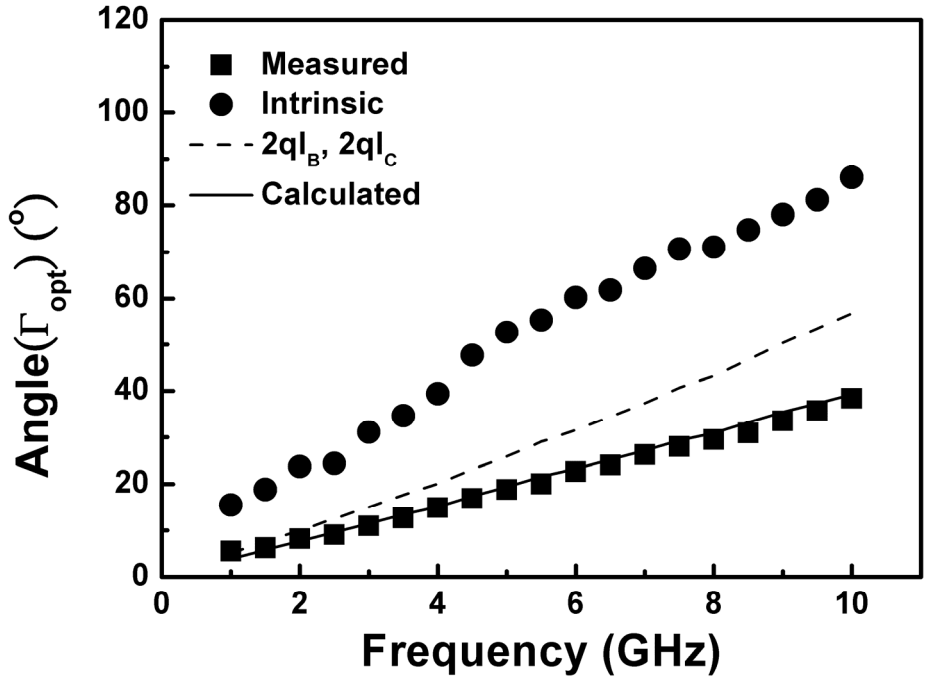
(a)


Measured
Intrinsic
2qlB, 2qlC
Calculated
Rn (Ω)
Frequency (GHz)
0
10
20
30
40
50
0
2
4
6
8
10

(b)



(c)



(d)

Fig. 6.11 Measured four noise parameters and calculated four noise parameters based on the proposed model and conventional $2qI_B$, $2qI_C$ assumption.

Chapter 7

Conclusions

For the conclusion of this thesis, firstly in chapter 2, we introduce the original of hybrid-π small-signal equivalent circuit of III-V HBTs and try to derive the closed form representation of all the circuit elements. The derived equations are then applied in a novel parameter extraction method of the hybrid-π small-signal equivalent circuit. Assuming that the equivalent circuit is valid over the whole frequency range of the measurements, the extrinsic elements are iteratively determined by minimizing the variance of the intrinsic elements as an optimization criterion. The proposed method leads to a good fit between the measured and calculated S-parameters.

However, applying the closed-form method in SiGe HBTs we observed that the algorithm does not work in all cases. This occurs especially when the estimation of extrinsic circuit elements is not accurate enough. For these cases, where the exact algorithm fails, a practical approach is developed, which is described in chapter 3. Unlike the proposed method in chapter 2, two formulas for the extraction of intrinsic base resistance (R_{bi}) are presented, followed by an accuracy improvement procedure to obtain better accuracy of the intrinsic base-collector capacitance (C_{bci}) and extrinsic base-collector capacitance (C_{bcx}). Simplified formulas to determine base-emitter resistance (R_π), base-emitter capacitance (C_π), transconductance (g_m) and excess phase delay (τ) are presented. When extracting the substrate network, we found that without considering the internal feedback signal through intrinsic circuit elements we may

extract negative effective substrate resistance in large area SiGe HBTs since the measured Re($Y_{22} + Y_{21}$) is negative.

In chapter 4, we applied the proposed parameter extraction method of SiGe HBTs to explain the anomalous dip in scattering parameters S_{12} of SiGe HBTs quantitatively. The conventional method which adopted the dual-feedback circuit methodology to analysis the anomalous dips in S_{11} and S_{22} can not be directly applied in the analysis of the anomalous dip in scattering parameters S_{12} due to its poor approximation in the feedback network. The results show that the relationship between one zero in the feedback network and two poles in the output impedance ratio causes the appearance of the anomalous dip of S_{12} in a polar chart. As I_B increases, the B/E depletion capacitance and B/E diffusion capacitance increase, i.e. C_π increases, and the zero moves to a lower frequency, which makes the anomalous dip more prominent. Comparing HBTs and MOSFETs with same active area, the value of C_π often shows several times larger than that of gate to source capacitance, C_{gs}. This may be the reason why it is much easier to see the anomalous dip in HBTs than in MOSFETs.

To investigate the transistor fundamental noise phenomena, an accurate calculation of transistor noise parameters is required. In chapter 5, a computation method for extracting noise parameters of a linear two-port network using a genetic algorithm is proposed. The developed method inherits the advantages of the Vasilescu's method of requiring no initial values. Besides, the computer-time of genetic search is independent on the number of measured source impedance and considers noise figure and source admittance errors simultaneously.

In chapter 6, we try to develop a systematic extraction procedure to extract the the

base current noise (S_{ib}), collector current noise (S_{ic}), of SiGe HBTs and their cross correlation $S_{ib,ic*}$ directly from the S-parameter and RF noise parameter measurement. The de-embedding of noise contribution from transistor parasitic is followed the conventional four-port noise de-embedding procedure. A systematic 4×4 four-port Y-parameters ([Y_{ee}], [Y_{ei}], [Y_{ie}], and [Y_{ii}]) calculation method is developed and applied in the four-port noise de-embedding procedure. The extraction results show that the base current noise is frequency dependent, while the collector current noise equals to $2qI_C$, but remains white. However, the extracted base current noise and correlation between S_{ib} and S_{ic} is sensitive to measurement error. A more accurate measurement is required to obtain the real base current noise and correlation between S_{ib} and S_{ic}.