Publication List

(a) Journal Papers

3. A類國際性期刊論文

(1) C. T. Chan, C. J. Tang, T. Wang, H. C.-H. Wang, and D. D. Tang, "Characteristics and physical mechanisms of positive bias temperature stress induced drain current degradation in HfSiON nMOSFETs," accepted and to be published in *IEEE Trans. on Electron Devices (TED)*, 2006

3. A類國際性期刊論文

(2) T. Wang, C. T. Chan, C. J. Tang, C. W. Tsai, H. C.-H. Wang, M. H. Chi, and D. D. Tang, "A novel transient characterization technique to investigate trap properties in HfSiON gate dielectric MOSFETs – from single electron emission to PBTI recovery transient," accepted and to be published in *IEEE Trans. on Electron Devices (TED)*, 2006

(3) M. C. Chen, S. H. Ku, C. T. Chan, and T. Wang, "Comparison of oxide breakdown progression in ultra-thin oxide silicon-on-insulator and bulk metal- oxide-semiconductor field effect transistors," *J. Appl. Phys.*, Vol. 96, pp.3473-3477, 2004

(4) M. C. Chen, S. H. Gu, C. T. Chan, and T. Wang, "Soft breakdown enhanced hysteresis effects in ultrathin oxide silicon-on-insulator metal-oxide- semiconductor field effect transistors," *J. Appl. Phys.*, Vol. 96, pp.2297-2300, 2004

(b) Conference Papers

2. A類國際會議論文

(5) C. T. Chan, C. J. Tang, Tahui Wang, H. C.-H. Wang, and D. D. Tang, "Positive Bias and Temperature Stress Induced Two-Stage Drain Current Degradation in HfSiON nMOSFET's," *IEEE International Electron Devices Meeting (IEDM), Washington D.C.*, pp. 571-574, 2005

(6) C. T. Chan, H. C. Ma, C. J. Tang, and Tahui Wang,

"Investigation of Post-NBTI Stress Recovery in pMOSFETs by Direct Measurement of Single Oxide Charge De-Trapping," *VLSI Tech. Dig. (VLSI), Kyoto, Japan,* pp. 90-91, 2005
Best Student Paper Award

(7) H. C. H. Wang, C. W. Tsai, S. J. Chen, C. T. Chan, H. J. Lin, Y. Jin, H. J. Tao, S. C. Chen, C. H. Diaz, T. Ong, A. S. Oates, M. S. Liang, and M. H. Chi, "Reliability of HfSiON as Gate Dielectric for Advanced CMOS Technology," *VLSI Tech. Dig. (VLSI), Kyoto, Japan,* pp. 170-171, 2005

(8) C. T. Chan, C. J. Tang, C. H. Kuo, H. C. Ma, C. W. Tsai, H. C.-H. Wang, M. H. Chi, and Tahui Wang, "Single-Electron Emission of Traps in HfSiON as High-k Gate Dielectric for MOSFETs," *Proc. Int. Reliab. Phys. Symp. (IRPS)*, pp. 41-44, San Jose, U.S.A., pp. 2005

(9) C. T. Chan, C. H. Kuo, C. J. Tang, M. C. Chen, and Tahui Wang, "Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI pMOSFETs," *Proc. International Conference on Solid State Devices and Materials (SSDM)*, pp. 238-239, Tokyo, Japan, 2004
Marubun Travel Grant (selected for young researchers)

(10) C. T. Chan, C. H. Kuo, C. J. Tang, M. C. Chen, Tahui Wang, S. Huang Lu, H. C. Hu, T. F. Chen, C. K. Yang, M. T. Lee, D. Y. Wu, J. K. Chen, S. C. Chien, and S. W. Sun, "Comparison of Oxide Breakdown Progression in Ultra-Thin Oxide SOI and Bulk pMOSFETs," *Proc. Int. Symp. Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp.49-52, Hsinchu, Taiwan, 2004
Best Paper Award in reliability**, Invited Paper** to 2004 ESREF in Swiss

(11) S. H. Gu, M. T. Wang, C. T. Chan, N. K. Zou, C. C. Yeh, W. J. Tsai, T. C. Lu, Tahui Wang, Joseph Ku, and C.-Y. Lu, "Investigation of Programmed Charge Lateral Spread in a Two-bit Storage Nitride Flash Memory Cell by Using a Charge Pumping Technique," Proc. *Int. Reliab. Phys. Symp. (IRPS),*

pp.639-640, Phoenix, U.S.A., 2004

(12) Tahui Wang, C. W. Tsai, M. C. Chen, C. T. Chan, and H. K. Chiang, "Negative Substrate Bias Enhanced Breakdown Hardness in Ultra-Thin Oxide pMOSFETs," *Proc. Int. Reliab. Phys. Symp. (IRPS),* pp.437-441, Dallas, U.S.A., 2003

(13) Tahui Wang, W. J. Tsai, S. H. Gu, C. T. Chan, C. C. Yeh, N. K. Zou, T. C. Lu, Sam Pan, and C. Y. Lu, "Reliability Models of Data Retention and Read-Disturb in 2-bit Nitride Storage Flash Memory Cells," **Invited Paper**, *IEDM Tech. Dig.*, pp.169-172, U.S.A., 2003

五、著作總點數：___8____ (依新法記點)