先進閘極介電層互補式金氧半電晶體中電壓溫度引致不穩定性之研究

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摘　　要

本論文提出一新穎之量測方法，並據以研究先進閘極介電層互補式金氧半電晶體中電壓溫度引致之不穩定性。此方法包括一自行組裝之電腦自動化量測電路系統，以及特殊設計之實驗技巧。傳統量測方法於加壓與量測之間，存在大約數秒之延遲，期間發生的電荷散逸將嚴重影響實驗數據的可信度與完整性。本論文所提之創新方法可有效縮短延遲至數微秒，成功攫取暫態訊號，發現新的現象並得以研究其物理。

第二章詳述此新穎量測電路之各零組件、系統效能、並展示於實際 CMOS 元件以及記憶體元件測試之量測結果。第三章介紹應用第二章所提之電路所發展之實驗方法－「暫態回復技巧」。此法之理論基礎與實際應用都將詳列於此章。吾人發現，經電壓溫度加壓，大面積元件具有可觀之回復效應；回復過程中，汲極電流對時間呈現 log 關係。同樣地，小面積元件亦有回復現象，但其汲極電流對時間的關係，則以不連續的、階梯式的圖像呈現。吾人研究發現，此量子化行為，乃一顆一顆儲存於介電層缺陷中的電荷散逸所致。藉由研究電場以及溫度對單電荷散逸之影響，吾人提出一可解析之物理模型－「熱助穿隧」，成功地解釋所得之實驗結果。此模型配合實驗結果，可進一步粹取缺陷特性，如活化能以及缺陷密度等等。最後，吾人以此方法比較不同閘極材料中缺陷的特性之異同。

第四章探討 HfSiON nMOSFETs 中正電壓溫度所引致之不穩定性（PBTI）。有別於傳統量測，本研究以第二章所述之量測方法發現，延遲轉換將嚴重低估 PBTI 所造成的退化量。吾人實驗結果發現 PBTI 引致之汲極電流退化呈現兩階段（two-stage degradation）發展。第一個階段由填補初始缺陷（initial trap filling）主導退化，具 log 時間關係並與溫度呈現負相關。第二階段，額外缺陷產生（additional trap generation）的效應將超越初始缺陷填補，成為退化主因；此階段與時間成指數（power-law）關係並與溫度成正相關。此外，吾人利用第二章所提之單電荷散逸量測和暫態回復技巧、輔以常用的電荷幫浦（charge pumping）法所得之實驗結果，與前述退化模型相呼應。最後評估的是製程對缺

陷產生以及兩階段退化特性的影響。

第五章研究 HfSiON pMOSFETs 中負電壓溫度所引致之不穩定性(NBTI)。低電壓或者室溫加壓，汲極電流退化的現象與一般預期無異：隨加壓時間呈現一路退化的趨勢、增加電壓強度或溫度則退化更嚴重。但再升高電壓或溫度，吾人則觀察到汲極電流隨時間之變化呈現奇特的「轉彎現象」（turn-around）：一開始汲極電流增加，到某時間點增加至最大值後開始降低，其後便一路減少並回歸到電流退化。愈高電壓以及愈高溫度下愈明顯。在本研究所有實驗條件下，在 10 秒以前汲極電流都會進入退化，所以一般量測方法若是忽略暫態效應，將無法清楚地觀測到此特殊現象。吾人提出一「雙極電荷模型」成功解釋實驗結果，並再次以單電荷散逸量測、以及電荷幫浦法，驗證所提出之物理模型。

最後於第六章，吾人總結本論文之貢獻，並提出未來研究方向的建議。

關鍵字：互補式金氧半電晶體，可靠度，高介電閘極氧化層，正電壓溫度引致不穩定性，負電壓溫度引致不穩定，回復，暫態量測，單電荷散逸，缺陷特性，兩階段退化，雙極電荷模型

Bias Temperature Instability in CMOSFETs with Advanced Gate Dielectrics

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ABSTRACT

This thesis proposes a novel characterization methodology to study the bias temperature instability (BTI) in advanced gate dielectrics (mainly high-k) for CMOS technology. The methodology includes a computer-automated measurement circuit system and specially-designed experimental techniques. The system minimizes the switching delay between stress and measurement down to ~μs, and successfully retrieves the valuable information which has been ignored in a conventional method where during the switching delay significant charge de-trapping takes place.

The components, capabilities, and demonstrations of the proposed transient measurement system are described in detail in Chapter 2. In Chapter 3, a novel recovery transient technique involving direct measurement of single charge phenomena is presented. Both large- and small-area MOSFETs are characterized. In a large-area device, the post-BTI drain current exhibits a recovery transient and follows logarithmic time dependence. In a small-area device, individual trapped charge emission from gate dielectric traps is observed during recovery, which is manifested by a staircase-like drain current evolution with time. By measuring the effects of electric field and temperature on the charge emission times, one can identify the physical mechanism for charge escape. An analytical model based on thermally assisted tunneling can successfully reproduce measured transient characteristics. One can also extract trap properties such as the activation energy and the trap density. Applications of the technique to comparison between different gate dielectric materials are also demonstrated.

Drain current degradation in HfSiON gate dielectric nMOSFETs due to positive bias and temperature (PBT) stress is investigated in Chapter 4 by using the fast transient measurement system introduced in Chapter 2. The degradation exhibits two stages, featuring different degradation rates and stress temperature dependence. The first stage degradation is attributed to charging of the pre-existing high-k dielectric traps and has log(t) dependence on stress time and negative temperature dependence while the second stage degradation is mainly caused by new high-k trap creation following a power-law time relation and positive temperature dependence. The high-k trap growth rate is characterized by two techniques, the recovery transient technique proposed in Chapter 3 and the well-known charge pumping technique. Finally, the impact of processing on high-k trap growth is evaluated.

In Chapter 5, negative bias temperature instability (NBTI) is explored for pMOSFET's with HfSiON as the high-k gate dielectric. An anomalous turn-around in NBT stress induced drain current change is observed. For low stress gate voltage amplitude ($|V_g|$) and/or low temperature, the drain current degrades with time and increase in stress strength aggravates the degradation. Further increase in ($|V_g|$) and/or in temperature, in contrast, leads to an anomalous turn-around in the temporal evolution of drain current. The drain current initially enhances, reaches a peak, goes downhill, and eventually enters degradation. The phenomenon occurs within 10 seconds for most stress conditions in this work, and thus is easily neglected in a conventional method. The measured enhancement grows with increasing stress $|V_g|$ and temperature. A physical model incorporating bipolar charge trapping is proposed to account for the experimental results. Direct measurement of single charge de-trapping and charge pumping measurement are performed and the results justify the model.

Finally, the contributions of this dissertation are summarized and the directions for the future works are suggested in Chapter 6.

Keyword: CMOS Reliability, High-k, PBTI, NBTI, Recovery, Transient Measurement, Single Charge Emission, Trap Properties, Two Stage Degradation, Bipolar Charging Model

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Chapter 3

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Table 3.2 Summary of the values used in the text.

Chapter 5

Table 5.1 Summary of dominant degradation mechanisms under various stress conditions. Detailed discussions are given in the text.

FIGURE CAPTIONS

Chapter 1

Fig. 1.1 Projections of gate leakage current and equivalent oxide thickness (EOT) from ITRS roadmap for high-performance (a) and low-standby-power (b) applications.

Fig. 1.2 Summary of high-k materials being studied. Data quoted from [1.15].

Fig. 1.3 The organization of the dissertation.

Chapter 2

Fig. 2.1 The operating principles of a conventional measurement method in characterization of non-volatile memories (a) and of CMOS devices (b).

Fig. 2.2 Energy band diagrams during stressing or programming (a) and during measurement (b). Charge de-trapping may take place during measurement.

Fig. 2.3 The measurement setup including components with radio frequency response for self-heating free characterization in SOI devices proposed in [2.1].

Fig. 2.4 The pulse-IV measurement setup incorporating a series resistance proposed in [2.3].

Fig. 2.5 The measurement setup using an operational amplifier proposed in [2.4].

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Fig. 2.7 The image of the transient measurement circuit.

Fig. 2.8 Recovery transient in a high-k nMOS device. As clearly shown, significant charge de-trapping occurs in sub-second regime. Detailed physics will be discussed in the following chapters.

Fig. 2.9 Program state retention characteristics spanning eight decades of time.

Chapter 3

Fig. 3.1 (a) Schematic diagram for PBTI recovery transient measurement. (b) The waveforms applied to the gate and drain during stress and recovery phases.

Fig. 3.2 Temporal evolutions of the drain current before and after stress in a nMOSFET with SiO_2 as the gate dielectric, measured by the experimental setup in Fig. 3.1.

Fig. 3.3 Temporal evolutions of the drain current before and after stress in a large area high-k nMOSFET. V_g=0.7V, 0.2s for stress and V_g/V_d=0.1V/0.2V for recovery. The device dimension is W/L=100μm/0.08μm. The symbols represent measurement data and the line calculation.

Fig. 3.4 Recovery drain current transients before and after stress in a small-area device. The bias condition for stress is the same as in Fig. 3.3, and for recovery V_g/V_d=0.3V/0.2V. The device dimension is W/L=0.16μm/0.08μm. Each current jump is attributed to single trapped charge escape from high-k gate dielectric. Only three electrons are trapped during stress. The emission time of the three trapped electrons is denoted as τ_1, τ_2, and τ_3.

Fig. 3.5 Temperature dependence of $<\tau_1>$. The activation energy extracted from the Arrhenius plot is 0.18eV. Each data point is an average of ten readings.

Fig. 3.6 Dependence of trapped electron emission times on recovery gate voltage. Ten measurements are made for each recovery V_g to take average.

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Fig. 3.8 The energy band diagram corresponding to the stress condition where V_g=0.7V is applied to inject electron into the high-k traps.

Fig. 3.9 Schematic representation of the band diagram in recovery phase and trap positions. E_a is the activation energy for SRH-like thermally assisted tunneling (TAT).

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Fig. 3.11 Normalized drain current evolution with recovery time for two stress V_g's (0.7V and 1V). The V_g in recovery phase is 0.1V.

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Fig. 3.15 Comparison of the recovery V_g dependence of charge emission times for a (a) high-k nMOS, (b) high-k pMOS, and (c) SiO_2 pMOS device.

Fig. 3.16 Comparison of the temperature dependence of the first charge emission time. The activation energy E_a is extracted to be (a) 0.18eV for high-k nMOS, (b) 0.14eV for high-k pMOS, and (c) 0.5eV for SiO_2 pMOS device.

Chapter 4

Fig. 4.1 (a) Setup for fast transient measurement as described in Chapter 2. (b) Pulses applied to gate and drain for stress and measurement. The stress time (t_{stress}) is scheduled on a log-time base and the stress gate voltage ($V_{g,stress}$) varies. The measurement condition is $V_{g,meas}$=1.2V and $V_{d,meas}$=0.2V. A measurement time (t_{meas}) of 50 μs is chosen such that it is long enough to integrate signals reliably and short enough to avoid additional degradation.

Fig. 4.2 Linear drain current degradation as a result of PBTI stress at V_g=2.2V and 2.4V, T=100C. Two-stage degradation is observed. The onset time of the accelerated degradation is denoted by τ_c (corner time). The first stage degradation is the degradation before τ_c, and the second stage is after τ_c.

Fig. 4.3 The drain current degradation rate in the first stage (a) and in the second stage (b). The second stage degradation is obtained by subtracting the extrapolation of the first stage degradation from the measured ΔI_d.

Fig. 4.4 Stress temperature effect on I_d degradation for V_g=1.8V (a) and 2.2V (b). A cross-over of the I_d degradation at T=25C and 125C is noticed and a larger stress V_g gives an earlier crossover.

Fig. 4.5 The corner time τ_c versus stress V_g at T=25C and 125C. The I_d degradation is driven into the second stage earlier (a smaller τ_c) at a higher stress V_g and temperature.

Fig. 4.6 The characterization procedure of the two methods for high-k trap density extraction. (a) A drain current recovery transient technique. (b) A two-frequency charge pumping technique.

Fig. 4.7 Drain current recovery transients measured at V_g/V_d=0.25V/0.1V in a fresh and in a post-2000s-PBTI-stressed device.

Fig. 4.8 Normalized drain current recovery transients measured at V_g/V_d=0.25V/0.1V for different PBTI stress times: t=0s, 1s, and 2000s. Devices dimension is W/L=100μm/0.08μm. The increased slope implies additional traps are generated during stress.

Fig. 4.9 The energy band diagram illustrating high-k trapped charge de-trapping during drain current recovery transient.

Fig. 4.10 The pre- and post-stress I_d-V_g characteristics in a linear scale (a) and in a semi-log scale (b).

Fig. 4.11 High-k trap density versus stress time from the recovery transient technique. The trap density is normalized to the initial high-k trap density.

Fig. 4.12 Drain current recovery transient in a small-area device with W/L=0.16μm/0.08μm: (a) for stress time=0s only one current jump is observed, and (b) after stress at V_g=3V, T=100C for 100s, up to five current jumps are presented. The increase in the number of current jumps indicates additional traps are created during stress.

Fig. 4.13 High-k trap density versus stress time from the CP technique. The trap density is normalized to the initial high-k trap density. (a) Stress temperature=25C, (b) stress gate voltage=2V.

Fig. 4.14 Generated high-k trap density versus stress time from the recovery transient and the CP techniques. The stress condition is V_g=2.2V, T=25C.

Fig. 4.15 Comparison of BTI-limited lifetime between the "optimal" and the "control" devices [4.2]. The BTI measurements are performed by using a conventional characterization method.

Fig. 4.16 Comparison of hot carrier injection limited lifetime between the "optimal"

and the "control" devices [4.2]. The measurements are performed by using a conventional characterization method.

Fig. 4.17 Comparison of time-to-breakdown between the "optimal" and the "control" devices [4.2].

Fig. 4.18 PBTI stress robustness of two devices: "optimal" vs. "control." While both have an identical transfer characteristic shown in the inset, the device with optimal nitrogen incorporation presents a better immunity against PBTI stress in terms of high-k trap generation.

Fig. 4.19 Comparison of I_d degradation between "optimal" and "control." The optimal samples show a lower initial trap density and better stress immunity (i.e., a larger τ_c).

Fig. 4.20 Stress temperature effect on I_d degradation rate in the "optimal" sample. The cross-over is still observed, indicating the existence of two-stage degradation.

Chapter 5

Fig. 5.1 NBTI degradation measured by using a conventional method and by using the transient measurement system described in Chapter 2. The transient measurement technique retrieves significant amount of I_d instability and anomalous characteristics.

Fig. 5.2 The pulse trains applied to gate and drain.

Fig. 5.3 Stress V_g dependence of NBT stress induced drain current change. Anomalous current enhancement during the initial stage of stressing and a turn-around behavior are observed for high $|V_g$'s$|$.

Fig. 5.4 Stress temperature dependence of NBT stress induced drain current change. Anomalous turn-around is also observed for high T.

Fig. 5.5 Stress V_g effect at different stages of stressing. For short stress durations (0.1s, 10s), a concave-up V_g dependence is observed. For prolonged stressing (1000s), the trend evolves to that as expected, or higher $|V_g|$ induces worse degradation.

Fig. 5.6 Stress temperature effect at different stages of stressing. While for a short stress duration (10s) $\Delta I_{d,lin}$ changes from degradation for low T to

enhancement for high T, a long stressing period (1000s) gives a trend as expected, or a higher T induces worse degradation.

Fig. 5.7 Energy band diagram at equilibrium (a), for a low stress $|V_g|$ (b), and for a high stress $|V_g|$ (c). ΔE_t denotes the available trap sites in high-k readily for trapping valence electrons from the poly-gate, and increases significantly for a high stress $|V_g|$.

Fig. 5.8 Recovery transient I_d in small area devices for short stress time (0.2s) for a low $|V_g|$ (-1.5V) (a), and for a high $|V_g|$ (-2.2V). Discontinuous current changes represent charge escape from dielectric traps, revealing the charge species injected during stress. An upward jump corresponds to a single hole charge, and a downward shift to a single electron. For the low $|V_g|$ case, only two holes are trapped during stress, while for the high $|V_g|$ case both electrons and holes are introduced into dielectric traps during stress.

Fig. 5.9 A schematic diagram illustrating the bias conditions for charge pumping measurement in a pMOSFET.

Fig. 5.10 Charge pumping measurement before and after stress. The effect of stress $|V_g|$ is indicated in (a). Impact of high-k integrity is compared in (b).

Fig. 5.11 Impact of high-k integrity on ΔI_d behavior. High-k integrity determines the polarity of ΔI_d.

Fig. 5.12 Even for a stress time long as 1000s, the V_g dependence still exhibits a turn-around feature, as opposed to that for an optimal device as indicated in Fig. 5.5.

LIST OF SYMBOLS

C_{db}	Drain-to-bulk capacitance
C_{gd}	Gate-to-drain capacitance
C_p	Parasitic capacitance
$C(x_i)$	Capacitance for trapped charges located at x_i from high-k/IL interface
D_{it}	Interface trap density
E_a	Trap activation energy
E_t	Trap energy (from the conduction band)
f_c	Fermi-Dirac distribution function
G_m	Transconductance
k	Boltzmann constant
I	Current
I_b	Bulk current
I_d	Drain current
I_e	Electron current
I_h	Hole current
I_{sd}	Source/Drain current
L	Gate length
L_{eff}	Effective gate length
m_0	Free electron mass
m^*_k	Electron effective mass in high-k
$m^*_{ox,e}$	Hole effective mass in high-k
$m^*_{ox,h}$	Hole effective mass in SiO_2
N_C	Effective density of states in the Si conduction band
N_{HK}	Volume high-k trap density
N^V_{HK}	Area high-k trap density
N_t	Trap density
Q	Trapped electron density
q	Electronic charge
T	Temperature
T_{HK}	Physical thickness of a high-k layer

T_{ox}	Physical thickness of a SiO_2 layer
t	Time
t_{BD}	Time-to-breakdown
t_{meas}	Measurement time
t_{stress}	Stress time
V	Voltage
V_d (V_D)	Drain voltage
$V_{d,meas}$	Measurement drain voltage
$V_{d,stress}$	Stress drain voltage
V_g (V_G)	Gate voltage
V_{gh}	High-level gate voltage for charge pumping measurement
V_{gl}	Low-level gate voltage for charge pumping measurement
$V_{g,meas}$	Measurement gate voltage
$V_{g,stress}$	Stress gate voltage
V_t	Threshold voltage
W	Channel width
$\overline{x_{eff}}$	Effective distance of trapped charges from high-k/IL interface
x_i	Distance of the i^{th} trapped charge from high-k/IL interface
$\hbar$	Reduced Planck constant
ΔE_t (ΔE)	Energy range for dielectric traps of interest
ΔG_m	Change in transconductance
ΔI_d	Change in drain current
$\Delta I_{d,lin}$	Change in linear drain current
ΔV_t	Change in threshold voltage
Φ_B	High-k/SiO_2 conduction band offset
α_k	Coefficient of tunneling probability through high-k
α_{ox}	Coefficient of tunneling probability through SiO_2
ε_{HK}	Dielectric constant of high-k gate dielectric
μ_n	Electron mobility
ν	Attempt-to-escape frequency
σ_0	Trap cross section

τ_c	Corner time for the two stage PBTI drain current degradation
τ_i	The i^{th} trapped charge emission time
τ_0	Characteristic time for tunneling
υ_{th}	Thermal velocity