Chapter 1

Introduction

1.1 Backgrounds

The dimensions of the smallest demonstrated prototypes of silicon based CMOS devices [1.1][1.2] have been rapidly approaching the "physical limit" – the inter-atomic distance. Continual downscaling boosts device performance to meet the Moore's Law at the expense of growing leakage problems. The tunneling currents through the gate dielectrics [1.3] (as the gate leakage current) and through the channel [1.4] (as the subthreshold leakage current) increase exponentially with decreasing gate dielectric thickness and with shorter channel length respectively. The resultant intolerable standby power consumption has made further scaling impractical. To resolve this dilemma, solutions have been proposed from two predominant perspectives: high circuit performance (HP) and low standby power (LSTP). The former necessitates technology boosters, including: a) strained silicon technology [1.5]-[1.7] and germanium transistors [1.8][1.9] which offer higher carrier mobility; b) replacement of poly-silicon with metallic materials as the gate electrode [1.10][1.11] which eliminate the equivalent oxide thickness (EOT) loss due to poly-depletion effect, and c) Schottky-barrier [1.12][1.13] or raised [1.14] source/drain which reduce the parasitic series resistance. The latter resorts to introduction of high permittivity (high-k) materials as the gate dielectrics [1.15][1.16]. As shown in Fig. 1.1, the projection of EOT and corresponding gate leakage requirement from ITRS roadmap [1.17] indicates that for all applications regardless of HP or LSTP, suppression of leakage

currents always deserves high priority for a smaller off-state current may directly reduce the standby power or may help increase I_{on}-to-I_{off} ratio. This work thus concentrates on the high-k technology.

Several issues in high-k technology are believed to possibly hinder its development: a) process related problems including thermal instability [1.18][1.19], and b) physics related fundamentals such as mobility degradation as a result of soft optical phonon scattering [1.20], and threshold voltage (V_t) control in the presence of Fermi-level pinning [1.21][1.22]. However, much effort has been devoted to alleviating (even eliminating) or getting around the above issues, and the results are encouraging. For example, an optimized chemical composition is demonstrated to possibly obtain a thermally stable film [1.18]. Insertion of an interfacial SiO_2 layer between high-k and Si substrate as well as use of "not-so-high-k" materials has been shown, both theoretically [1.20] and experimentally [1.16][1.23], to improve the carrier mobility effectively.

Fig. 1.2 [1.15] summarizes candidate high-k materials reported in International Electron Devices Meeting (IEDM) and Symposium on VLSI Technology from 2000 through 2002. Among them, Hf-based materials are most promising and their film chemistry [1.24][1.25], process optimization [1.23][1.26], as well as reliability assessment and analysis [1.27]-[1.29] are being extensively studied. Recently, HfSiON has been successfully integrated into CMOS devices as gate dielectric for low power applications with good reliability, comparable mobility (as SiO_2), and greatly reduced gate leakage [1.23][1.27].

Several reliability issues for high-k gate dielectrics have been identified:

threshold voltage (V_t) instability [1.29]-[1.32], stress induced film degradation [1.33]-[1.35], and dielectric breakdown [1.28][1.34][1.36][1.37]. Shanware et al. found that charge trapping induced drain current degradation in HfSiON exhibits logarithmic time dependence [1.29]. V_t instability in high-k gate dielectric CMOS was reported to be mainly controlled by the dynamics of electron charging/discharging in pre-existing high-k bulk defects [1.30]. Young et al. concluded that fast electron trapping is a significant source of observed device DC performance degradation [1.31]. It was concluded by Crupi et al. that stress induced leakage current (SILC) imposes no reliability constraint at room temperature in high-k devices [1.33]. Ref. [1.34] indicated that traps at shallow and deep energies are respectively responsible for V_t instability and SILC. Moreover, high-k bulk trap density, on the one hand, was demonstrated to strongly correlate to yield in terms of dielectric breakdown [1.36]. Thermo-chemical breakdown with a leakage current acceleration model, on the other hand, was proposed to explain high-k dielectric breakdown [1.37].

1.2 Description of the Problem

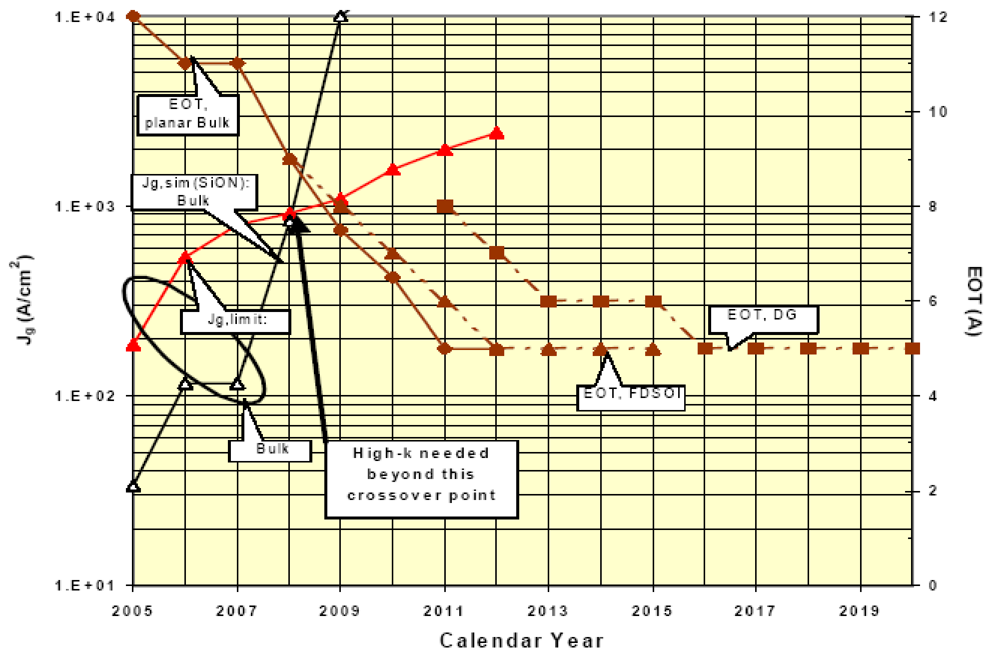
In most of the aforementioned studies, the assessment of high-k is benchmarked with SiO_2 control – mobility degradation, leakage current reduction, or reliability qualification such as charge-to-breakdown. The characterization methodology being used for high-k has been inherited from the experience with SiO_2, and the ways experimental data are collected are similar to those for SiO_2. For example, in a typical bias temperature instability (BTI) experiment, the devices are stressed with gate voltages at a

certain temperature. The stress is periodically interrupted to measure the parametric shift, i.e. the change in threshold voltage, in (linear or saturation) drain current, or in transconductance. A delay time on the order of seconds inherently exists for switching between stress and measurement. Nevertheless, recent literatures have shown that during this switching delay, significant recovery from degradation is taking place in SiO_2 [1.38][1.39] and in high-k [1.35][1.40], necessitating a modified characterization technique for accurate and complete analysis. The scope of this thesis thus focuses on the exploration into the transient phenomena. The organization is given in the following section.

1.3 Organization of the Dissertation

The organization of this dissertation is schematically illustrated in Fig. 1.3. A computer-automated measurement system is assembled to facilitate transient analysis and will be described in detail in Chapter 2. With the use of the measurement system, experimental data during the switching delay is retrieved. A series of reliability issues are identified and interpretations are made. Proposed in Chapter 3 is a novel technique for investigation of microscopic trap properties in advanced gate dielectrics involving direct measurement of single charge phenomena. Chapter 4 discusses the characteristics and physical mechanism for positive bias and temperature stress induced drain current instability (PBTI) in high-k nMOSFETs. In Chapter 5, an anomalous negative bias and temperature instability (NBTI) feature in high-k pMOSFETs is demonstrated and the responsible origins are discussed. Finally in Chapter 6, the contributions of this dissertation and

suggestions for future works are summarized.



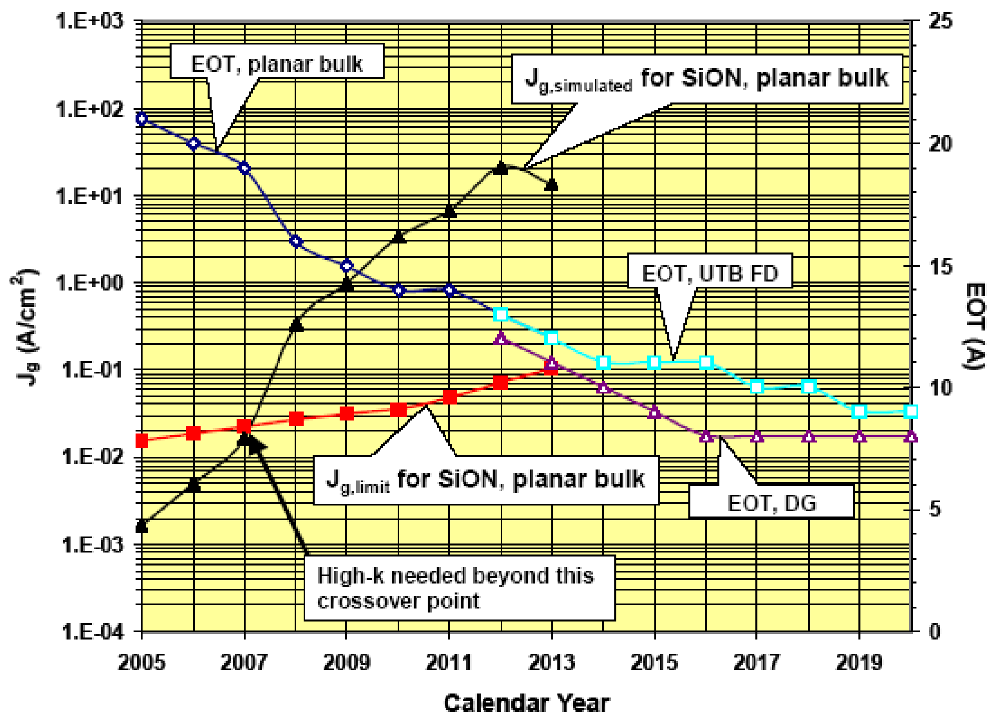
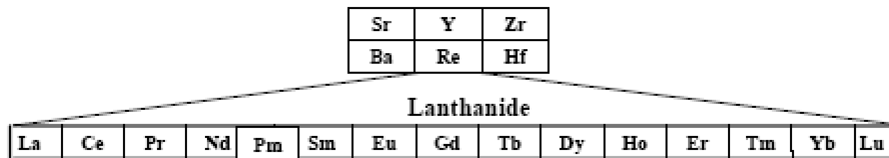
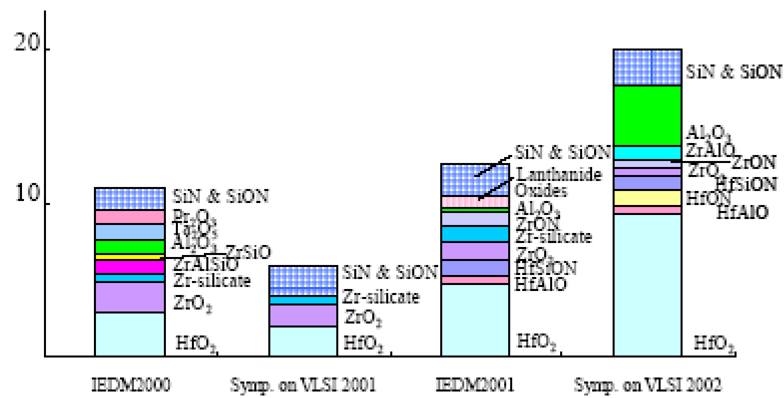


Fig. 1.1 Projections of gate leakage current and equivalent oxide thickness (EOT) from ITRS roadmap for high-performance (a) and low-standby-power (b) applications.

Material	k	$HfAl_xO_y$	10-15
NO stack	5-6	$HfSi_xO_yN_z$	10-15
Al_2O_3	8-9	ZrO_2, HfO_2	20-30
$HfSi_xO_y$	10-15	Lanthanide Oxides	15-30



(a)



(b)

Fig. 1.2 Summary of high-k materials being studied. Data quoted from [1.15].

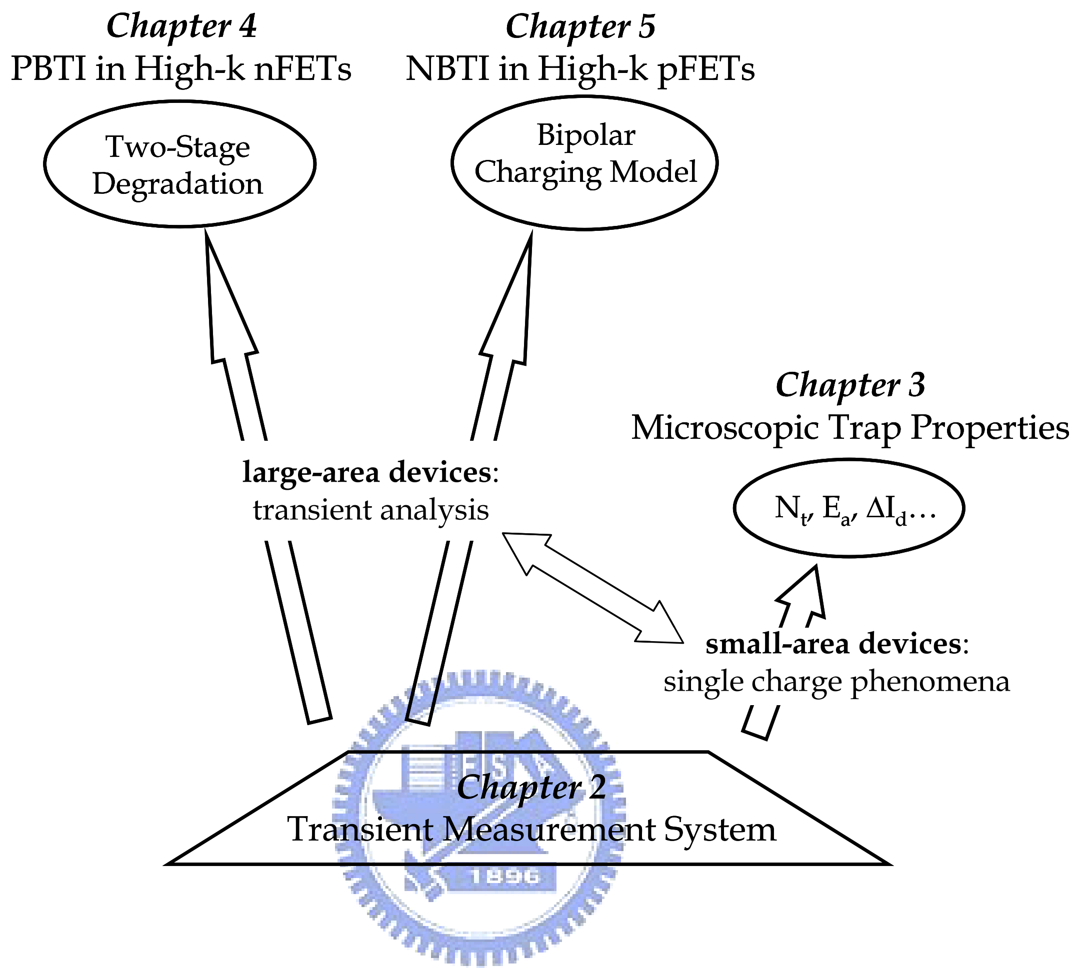


Fig. 1.3 The organization of the dissertation.