Chapter 3

Single Charge Emission: A Novel Technique to Investigate Trap Properties in Advanced Gate Dielectrics

3.1 Preface

Similar to NBTI effects in conventional SiO_2 gate dielectric, in high-k devices positive bias and temperature (PBT) stress induced degradation (parametric shift) and recovery (parametric retrieval) are both considered to be important in determining high-k device lifetime [3.1][3.2]. Conventionally, BTI characterization is carried out by periodically interrupting stress to measure electrical parameters, introducing a switching delay between stress and measurement which may give rise to an imprecise or even incorrect result [3.2]-[3.5]. Recently, a two-frequency charge pumping (CP) measurement has been utilized to characterize high-k trap properties [3.6][3.7]. However, the CP measurement still has the following drawbacks. First, the CP current may be too small to be reliably measured in small-size devices at a lower frequency required to probe into the high-k layer. Second, due to the mixture of interface and high-k bulk traps, the two-frequency CP method may not be viable when the high-k trap density is comparable to or even less than the interface trap density. Third, CP alone cannot provide detailed description for high-k trap behaviors such as trap activation energy.

In this chapter, a novel transient characterization technique for

exploration of high-k trap properties by measuring the post-stress recovery drain current transient in large- and small-area devices is presented in Section 3.2. In small-area devices, single charge phenomenon is observed. Based on the temperature and voltage dependence of the single charge effect, an analytical model for PBTI recovery is developed in Section 3.3 and high-k trap parameters are extracted. The model is further verified by comparison with measured transient characteristics in a large-area device. Finally in Section 3.4, applications of the technique are demonstrated.

3.2 Recovery Transient Measurement

3.2.1 Experimental

The devices used in this work are nMOSFETs with a poly-silicon electrode, and a bi-layered gate dielectric stack consisting of HfSiON (physical thickness of 2.5nm) and an interfacial SiO_2 layer (IL, 1nm~1.4nm). The gate width is 0.16μm ~100μm, and the gate length ranges from 80nm to 220nm. Detailed fabrication process and device characteristics can be found in [3.8][3.9]. The devices are first subjected to a positive gate bias (V_g) stress, and then "recover" at a lower V_g. In the "stress phase", electrons in the inversion channel are injected and trapped into pre-existing high-k traps, while in the "recovery phase" the trapped charges escape via thermally assisted tunneling (see Section 3.3.1). A conventional "sense-after-stress" method introduces a switching delay between phase transitions. This switching delay, as has been reported in literature for both NBTI in SiO_2 and PBTI in high-k, leads to inaccurate experimental results [3.1]-[3.5]. Thus, our measurement setup described in Chapter 2 [3.2][3.5] is used to monitor the

recovery I_d. The switching delay between stress and recovery is minimized down to μs. The sampling rate is 10^4 readings per second. Fig. 3.1(b) depicts the waveforms applied on gate and drain during stress and recovery. The system was tested on MOSFETs with SiO_2 as the gate dielectric and stable current-time characteristic was obtained as indicated in Fig. 3.2, ensuring that the system introduces no spurious transient effect.

3.2.2 Recovery Transient in Large-Area Devices

The recovery transient of the drain current at V_g/V_d=0.1V[1]/0.2V in a large area (100μmx0.08μm) nMOSFET is shown in Fig. 3.3 after stress[2] at V_g=0.7V for 0.2s. The pre-stress drain current is also plotted for comparison. The post-stress I_d increases with a logarithmic time dependence for about four decades of time from 1ms to 10s and is saturated at a level close to the pre-stress one, suggesting full recovery for the chosen stress condition. Note that a conventional measurement, which usually takes a few seconds for phase transition, is unable to measure the initial transient in the milli-second range in Fig. 3.3 and may significantly underestimate the magnitude of the transient effect. We repeat the same measurement (stress and recovery) on a SiO_2 control sample. The result is shown in Fig. 3.2 and no transient effect is noticed. This comparison implies that the observed transient should arise from the high-k gate dielectric rather than from the interfacial oxide layer.

---

[1] The current magnitude to be measured with the transient system is limited by the OpAmp. Therefore, for a device with a very large W/L value a V_g much smaller than V_t is selected. For a device with a small W/L, the V_g would be larger (e.g. Line 4 next page). For both cases, the V_g is such chosen that the devices are in subthreshold region (weak inversion) to magnify the effect of charge detrapping.

[2] A V_g as low as 0.7V actually dose not damage the device. The "stress" is to "fill" the traps with electrons. The readers should not be confused with the terms.

3.2.3 Single Electron Emission in Small-Area Devices

An identical stress condition is performed on a small-area device (W/L=0.16μm/0.08μm) where only a few initial traps are present in the high-k layer. The recovery I_d monitored at V_g/V_d=0.3V/0.2V, interestingly, exhibits a staircase-like evolution, as shown in Fig. 3.4. The post-stress drain current returns to the pre-stress level, suggesting again full recovery. Each current jump in Fig. 3.4 is believed to be due to single electron emission from traps in HfSiON gate dielectric for two reasons. Firstly, the discontinuous change in drain current implies the nature of discrete charge emission. Secondly, according to the theory of random telegraph signal [3.10], the current drift due to interchanging a single electron in the inversion channel with the dielectric traps can be approximated with $q\mu_n V_d/L_{eff}^2 \sim 10^{-8}(Amp)$[3], consistent with the measured value (for example, in Fig. 3.4, 40nA for the first current jump). Here, only three electrons are trapped in the measured device during stress. In Fig. 3.4, individual electron emission time τ_1, τ_2, and τ_3 can be clearly defined. We further explore the dependence of electron emission times on recovery gate voltage and temperature. An average of the electron emission times is taken from ten measurements on the same device by repeating stress and recovery. Fig. 3.5 shows the temperature dependence of τ_1. The extracted activation energy (E_a) from the Arrhenius plot is about 0.18eV. Fig. 3.6 indicates the recovery gate voltage dependence of the first two electron emission times. Both τ_1 and τ_2 increase with recovery V_g.

[3] q is the element electronic charge, μ_n the electron mobility, and L_{eff} the effective channel length.

3.3 Results and Discussions

3.3.1 Trapped Charge Emission Model

Three possible paths for electron de-trapping are illustrated in the energy band diagram in Fig. 3.7: (a) thermal excitation assisted by electric field, or Frenkel-Poole (F-P) emission, (b) Shockley-Read-Hall like (SRH-like) thermally assisted tunneling[4] (TAT) [3.11]-[3.13] to the gate electrode, and (c) TAT to the Si substrate. The energy band diagram for charge injection is drawn in Fig. 3.8. The most probable injection trap energy for the selected V_g is E_t~3.2-(0.54+1.3)=1.36eV. Because the electric field in the high-k layer is small, this value can be approximated constant through the whole high-k layer. In the F-P process, a trapped electron is thermally excited *from the trap to the conduction band* (the activation energy). The de-trapping path (a) can thus be ruled out since the corresponding activation energy E_a should be about the trap energy (>1eV) and the measured E_a is only 0.18eV[5]. Path (b) is also excluded because a larger (more positive) recovery V_g would accelerate de-trapping toward the gate electrode, giving a shorter charge emission time. The measured trend of τ versus V_g is just opposite (Fig. 3.6). As a result, (c) is identified as the dominant path of trapped charge emission under the chosen stress condition. Moreover, the temperature effect implies the role of thermal process in the charge tunneling process. As a result, an analytical model based on TAT is developed with the energy band diagram and trap distance illustrated in Fig. 3.9. According to the WKB approximation, the

[4] Tunneling by itself exhibits weak temperature dependence. The measured activation energy (E_a= 0.18eV) indicates that temperature plays a role, and thus TAT.

[5] Ribe et al. extracted an activation energy of 0.35eV for F-P mechanism in [3.14]. In their case, a V_g=2V is used to fill the high-k traps for subsequent detrapping measurement. Much shallower traps than in our experiments are filled because our filling V_g is smaller (0.7-1.2V). For smaller injected trap energies, F-P excitation is also a possible detrapping path.

trapped charge emission time is formulated as

$$\tau_i^{-1} = \upsilon \exp(-\alpha_{ox} T_{ox}) \exp(-\alpha_k x_i) \tag{3.1}$$

where

$$\upsilon = N_C (1 - f_c) \upsilon_{th} \sigma_0 \exp(-\frac{E_a}{kT}) \tag{3.1a}$$

$$\alpha_{ox} = \frac{2\sqrt{2m^*_{ox,e} q(E_t + \Phi_B)}}{\hbar} \; ; \; \alpha_k = \frac{2\sqrt{2m^*_k q E_t}}{\hbar}. \tag{3.1b}$$

The pre-factor ν in Eq. (3.1a) is a lumped parameter, often referred to as the "attempt-to-escape frequency", and can be expressed as Eq. (3.1a) where N_C is the effective density-of-states in the Si conduction band, f_c the Fermi-Dirac (FD) distribution function in the Si substrate at the energy aligned to the trapped charge, $N_C(1-f_c)$ the amount of available states in the Si substrate for out-tunneling electrons from high-k traps, and σ_0 and E_a the trap cross-section and the activation energy, respectively. Other variables have their usual definitions. The FD distribution (f_c) is a function of V_g in recovery. A smaller recovery V_g leads to a smaller channel electron density, or a smaller f_c, and thus a shorter electron emission time. As the recovery V_g reduces below the threshold voltage, f_c approaches zero and thus the electron emission time becomes independent of V_g, as shown in Fig. 3.6. The electron nearest to the interface of the Si substrate will be the first for de-trapping. In order to exclude the temperature effect resulting from the FD distribution, we chose a small recovery V_g (≤0.3V), i.e. f_c~0, in the measurement of trap activation energy E_a in Fig. 3.5.

3.3.2 High-k Trap Density

The high-k trap density (N_t) can be evaluated through the proposed analytical model. By comparing

$$\tau_1 = \upsilon^{-1} \exp(\alpha_{ox} T_{ox}) \exp(\alpha_k x_1) \tag{3.2a}$$

$$\tau_2 = \upsilon^{-1} \exp(\alpha_{ox} T_{ox}) \exp(\alpha_k x_2) \tag{3.2b}$$

, one obtains

$$\frac{\tau_2}{\tau_1} = \exp[\alpha_k (x_2 - x_1)] \ . \tag{3.3}$$

Assuming the high-k traps have a uniform distribution in space, the high-k trap density is readily calculated as

$$N_t = \frac{1}{WL(x_2 - x_1)} = \frac{\alpha_k}{WL \ln\left(\frac{\tau_2}{\tau_1}\right)}. \tag{3.4}$$

Equation (3.3) predicts that the ratio of emission times (τ_2/τ_1) is only related to the physical distance between trap sites. Fig. 3.10 indeed shows that τ_2/τ_1 (ten readings of each V_g on the same device; ten devices measured) is constant and is independent of recovery V_g. For measurement convenience, in Fig. 3.10 fixed recovery currents rather than recovery voltages were chosen, thus leading to scattered data points arising from threshold voltage variation. An average τ_2/τ_1 of 3.4 is obtained, corresponding to an average high-k trap density of N_t=3.5x10^{17}cm^{-3} (assuming $m_k^* = 0.18\, m_0$ [3.15]), or equivalently, an area density of 8.8x10^{10}cm^{-2}.

It should be pointed out that in the above analysis single trap energy was assumed. This assumption is reasonable since the trap energy range corresponding to stress V_g(=0.7V) and recovery V_g(=0.3V) is very small. Only traps in this small energy range are charged and discharged in the above measurement. For a larger stress V_g, the injected electrons may fill high-k traps at different positions and energies. This will be discussed later.

3.3.3 Modeling of Recovery Transient in Large-Area Devices

In a large area device, the high-k charge de-trapping rate is

$$Q(x,t) = Q(x,0)\exp[-t/\tau(x)] \tag{3.5}$$

where $Q(x,t)=qN_t(x,t)$ is the time-dependent trapped charge density and $\tau(x)$ is described in Eq. (3.1). The threshold voltage shift, ΔV_t, induced by trapped electron emission is written as

$$\Delta V_t(t) = -\sum_i \frac{\Delta Q(x_i,t)}{C(x_i)} = -\sum_i \frac{qN_t(x_i,0)}{\varepsilon_{HK}}(T_{HK} - x_i)[1 - \exp(\frac{-t}{\tau_i})] \tag{3.6}$$

where $C(x_i)$ is the corresponding capacitance for trapped charges located at x_i from high-k/IL interface, and ε_{HK} and T_{HK} are the permittivity and physical thickness of the high-k layer respectively. For a large amount of trapped charges, the summation in Eq. (3.6) is substituted by integration written as

$$\Delta V_t(t) = -\int \frac{qN_t(x,0)}{\varepsilon_{HK}}(T_{HK} - x)\{1 - \exp[-t/\tau(x)]\}dx \tag{3.7}$$

where $\tau(x)=A\exp(\alpha_k x)$ and $A=[N_C(1-f_c)\nu_{th}\sigma_0\exp(-E_a/kT)]^{-1}\exp(\alpha_{ox}T_{ox})$. Because the double exponential $\exp[-t/\tau(x)]=\exp[(-t/A)\exp(-\alpha_k x)]$ in the integrand changes abruptly from 0 to 1 around $x=(\alpha_k)^{-1}\ln(t/A)$, it can be approximated by a step-function:

$$\exp[(-\frac{t}{A})\exp(-\alpha_k x)] = \begin{cases} 0 & \text{for } x \le (\alpha_k)^{-1}\ln(t/A) \\ 1 & \text{for } x \ge (\alpha_k)^{-1}\ln(t/A) \end{cases}. \quad (3.8)$$

This approximation translates into a "clear-cut" picture: after time t, electrons with emission times shorter than t are completely de-trapped while all of the rest remain trapped. Therefore, Eq. (3.7) is further simplified as

$$\Delta V_t(t) \approx -\frac{qN_t}{\varepsilon_{HK}} \int_0^{(\alpha_k)^{-1}\ln(t/A)} (T_{HK} - x)dx. \quad (3.9)$$

The time window of interest for modeling is four decades as shown in Fig. 3.3. According to Eq. (3.3), the time span is equivalent to a physical distance of around 10Å in high-k, or an equivalent oxide thickness (EOT) of 2Å. Therefore, the term T_{HK}-x is approximated as a constant, or $\overline{x_{eff}}$, and Eq. (3.9) reduces to

$$\Delta V_t(t) \approx -\frac{qN_t\overline{x_{eff}}}{\varepsilon_{HK}\alpha_k}\ln(\frac{t}{A}). \quad (3.10)$$

The corresponding recovery drain current evolution in the measurement interval can be written as

$$\Delta I_d(t) \propto \frac{qG_m N_t \overline{x_{eff}}}{\varepsilon_{HK}\alpha_k} \ln(\frac{t}{A}) \tag{3.11}$$

where the transconductance, G_m(=dI/dV)[6], is obtained from measurement. The simulated recovery transient from Eq. (3.11) is in good agreement with measurement[7] as shown in Fig. 3.3. Eq. (3.11) also reveals that the recovery slope in Fig. 3.3 is linearly proportional to the high-k trap density.

As mentioned in Section 3.3.2, the injected electrons may fill different energy traps at a larger stress V_g. In this case, the trap energy distribution should be taken into account and Eq. (3.11) is modified as follows

$$\Delta I_d(t) \propto \left(\int_{\Delta E} \frac{qG_m N_t(E_t)\overline{x_{eff}}}{\varepsilon_{HK}\alpha_k(E_t)} dE_t \right) \ln(t) \tag{3.12}$$

where ΔE represents the energy range of trapped charges. Eq. (3.12) shows that at a larger stress V_g the recovery transient still follows logarithmic time dependence but has a larger slope because of a larger ΔE. Fig. 3.11 shows the measured recovery transients for two stress V_g's. As expected, the larger stress V_g has a larger slope.

Finally, the author would like to remark three points. *First*, a very short stress time (0.2sec) was selected because the purpose of this technique is to

---

[6] Subthreshold swing can also be used (with proper modifications in Eq.3.11) if the recovery transient is measured well below V_t.

[7] Deviation of calculation from measurement does exist, and stems from the assumptions of single trap energy and uniform trap distribution in space as well as from the fact that G_m may change during recovery as a result of modification of Coulomb scattering in response to charge detrapping. In spite of the deviation, for same charge filling and recovery conditions, the slope of drain current transient can serve as an indicator of trap density.

characterize the pre-existing traps in HfSiON gate dielectric. For a longer stress time and a larger stress V_g, additional high-k traps will be generated. The PBTI stress induced high-k trap creation will be explored in Chapter 4. *Second*, the extraction of trap density from small area devices or from large area ones described above is based on the assumptions of single energy for trapped charges and of uniform trap distribution in space. These assumptions are vulnerable to selection of stress (filling) and recovery conditions. One should be careful in choosing experimental conditions that validate the assumptions. *Third*, two factors that possibly influence the accuracy in modeling large-area transients should be mentioned. (a) In Eq. (3.10) a constant $\overline{x_{eff}}$ of the physical thickness of the high-k layer is used which overestimates the impact of the trapped charges and underestimates the trap density. (b) ΔI_d is determined by fluctuations in the number and in the mobility of the inversion charges. Eq. (3.11) considers only number fluctuation (which changes I_d through capacitance effect) and a constant G_m is used. However, the electrostatics the trapped charges built would be modified upon charge detrapping which correspondingly affects Coulomb scattering rate, and thus the carrier mobility. Separation of individual contributions from number fluctuation and mobility fluctuation necessitates Monte Carlo simulation which is beyond the scope of this work.

3.3.4 Gate Length Effect

The single charge effect is investigated on devices with gate lengths of 0.08μm, 0.14μm, and 0.22μm. Fig. 3.12 shows that the quantized feature in the recovery transient is still observable for all the three lengths. However, the

amplitude of the drain current step (ΔI_d) decreases with increasing gate length. This trend is consistent with the Random Telegraph Signal theory [3.10] and implies that the impact of the trapped electron in the high-k dielectric spreads over the entire channel.

3.4 Applications of the Technique

Applying the proposed technique, single hole charge emission is measured in high-k and SiO_2 pMOSFETs.

3.4.1 Study of NBTI in SiO_2 pMOSFETs

Debates on the species involved in NBTI effect in SiO_2 pMOS has been in literatures [3.5][3.16]-[3.19]. While some researchers concluded that *only* hydrogen-related species (neutral or charged) is responsible for NBTI degradation and recovery [3.16][3.17], others proposed the possibility of participation of hole charges [3.5][3.18][3.19]. To explore this problem, single hole emission in SiO_2-gated pMOSFETs during NBTI recovery is performed and the results are illustrated in Fig. 3.13. The stress condition is V_g= -3V, T=100C, and t=2s for the "weak stress" and t=300s for the "strong stress." The recovery drain current is measured at V_g= -0.3V (around threshold condition). "Strong stress" gives more frequent current jumps in the recovery period, implying a larger trap density. This is consistent with the fact that "strong stress" induces more oxide degradation (more trap generation). Furthermore, the recovery V_g dependence of the first two charge emission times (τ_1 and τ_2) and the temperature dependence of τ_1 are also shown in Fig. 3.15(c) and Fig. 3.16(c) respectively.

Since the channel current is stable between two consecutive current jumps, back diffusion of charged particles (no matter what they are) should be excluded for the observed NBTI recovery transient. In addition, although the experimental activation energy E_a=0.5eV is close to the values for neutral H_2 in literature (0.45 [3.17]), the measured recovery V_g dependence rules out back diffusion of neutral species. Therefore, the staircase-like current changes observed serve as the direct proof of hole charge emission during NBTI recovery which indirectly evidences that hole charges do play a role in degradation.

3.4.2 Comparison between High-k and SiO_2

Another application of the technique is to compare the trap properties in high-k and in SiO_2. Discrete charge emission induced staircase-like current jumps, and the recovery V_g and the temperature dependence of the charge emission times are shown in Fig. 3.14, Fig. 3.15, and Fig. 3.16 for high-k nMOS, high-k pMOS, and SiO_2 pMOS transistors. The activation energy E_a (extracted from the temperature dependence), the average τ_2-to-τ_1 ratio (extracted from the V_g dependence), and the trap density (calculated from Eq. 3.4) are summarized in Table 3.1. Two interesting findings are noticed: (a) the first charge emission time (τ_1 ~ tens of milli-seconds) and the amplitude of the current jumps (ΔI_d ~ tens of nA) are comparable for all three types of devices. (b) The activation energy is dependent on the dielectric material (high-k or SiO_2), not on the conduction carrier (electron or hole). Further study is required to clarify the root physics of this difference.

3.5 Summary

A novel transient measurement technique is proposed for characterizing high-k gate dielectric traps in HfSiON nMOSFETs. The quantized feature in recovery current evolution due to single charge detrapping is observed for the first time in a small area device. A SRH-like thermally-assisted-tunneling model for high–k trapped charge emission is developed. Our model can well explain the measured electric field and temperature dependence of single-charge emission times. The model also reveals that the recovery drain current transient in large-size devices should follow logarithmic time dependence. The high-k trap density can be extracted from charge emission times in a small device or from the drain current recovery slope in a large device. For trap activation energy, single charge emission measurement is necessary since the transient slope in a large device does not contain the activation energy. Applications of the technique are demonstrated. The proposed technique for single charge effect characterization can provide insight into trap properties in advanced gate dielectrics in the development of nano-scale CMOS devices.

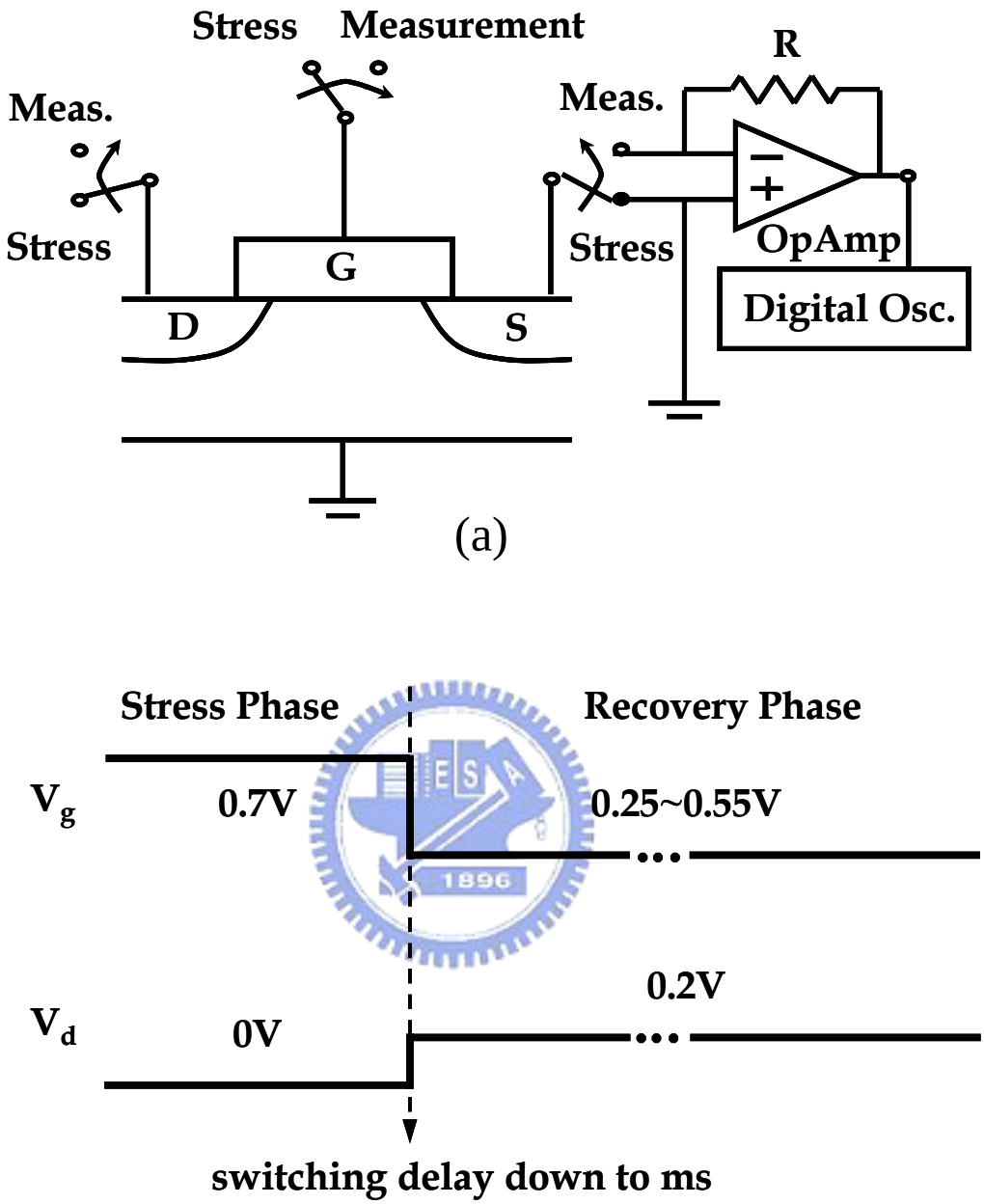

Fig. 3.1 (a) Schematic diagram for PBTI recovery transient measurement. (b) The waveforms applied to the gate and drain during stress and recovery phases.

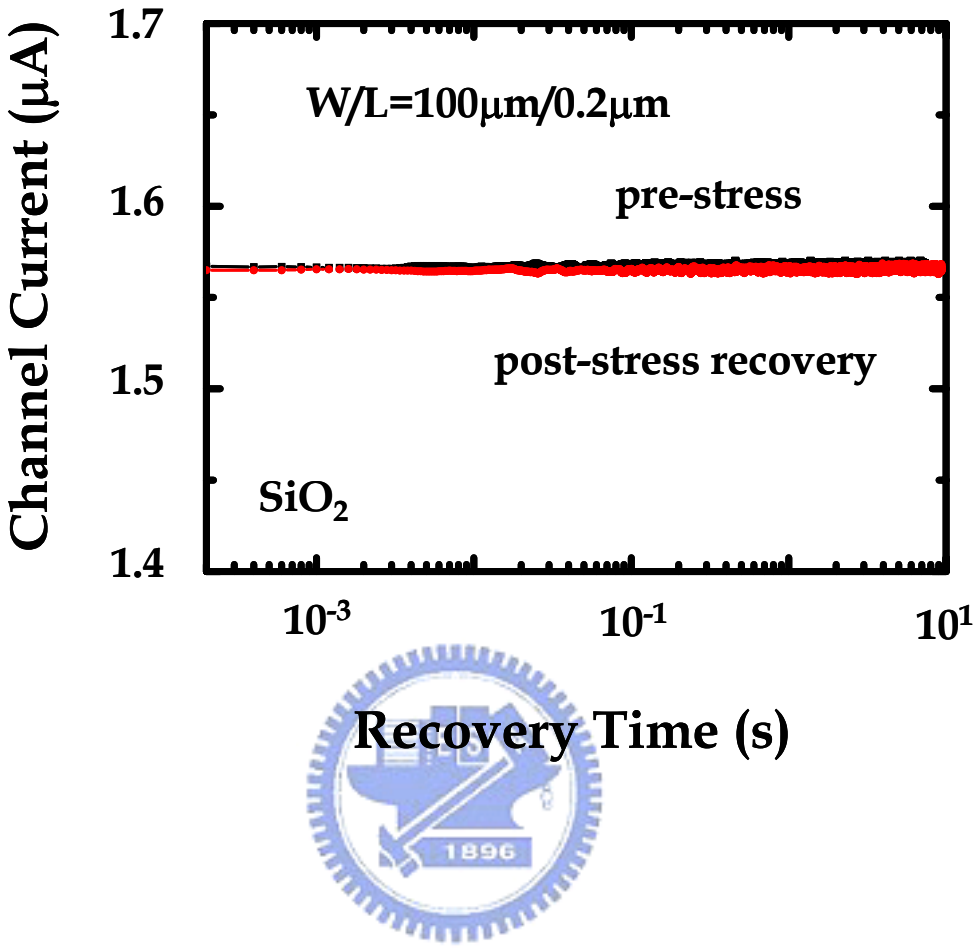

Fig. 3.2 Temporal evolutions of the drain current before and after stress in a nMOSFET with SiO_2 as the gate dielectric, measured by the experimental setup in Fig. 3.1.

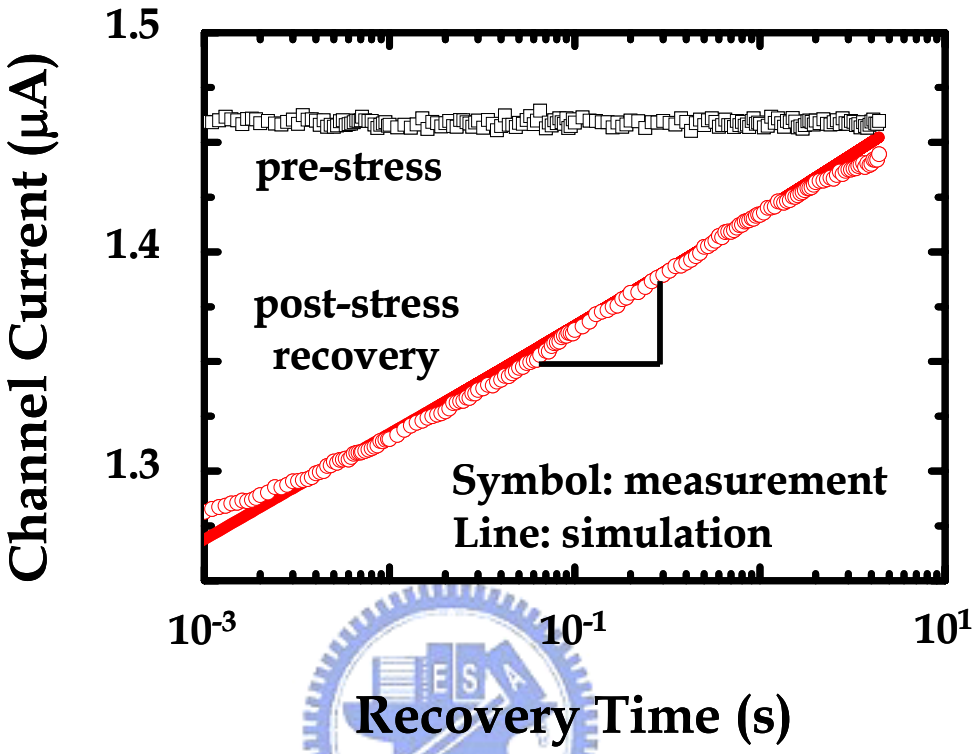

Fig. 3.3 Temporal evolutions of the drain current before and after stress in a large area high-k nMOSFET. V_g=0.7V, 0.2s for stress and V_g/V_d=0.1V/0.2V for recovery. The device dimension is W/L=100μm/0.08μm. The symbols represent measurement data and the line calculation.

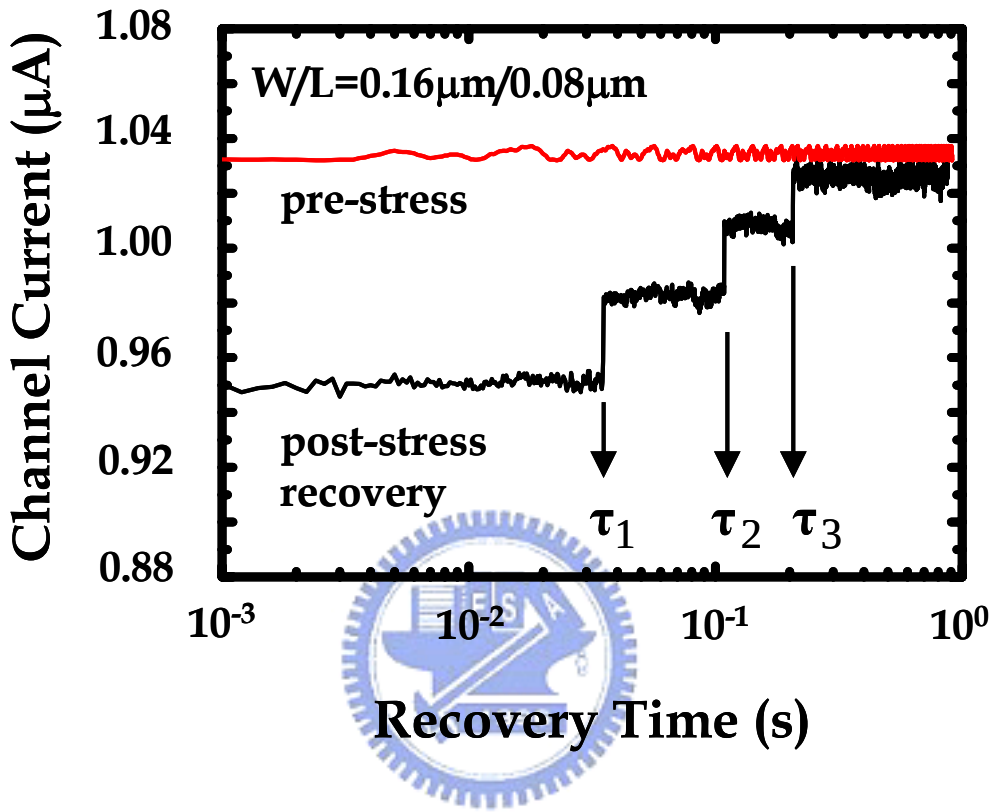

Fig. 3.4 Recovery drain current transients before and after stress in a small-area device. The bias condition for stress is the same as in Fig. 3.3, and for recovery V_g/V_d=0.3/0.2V. The device dimension is W/L=0.16μm/0.08μm. Each current jump is attributed to single trapped charge escape from high-k gate dielectric. Only three electrons are trapped during stress. The emission time of the three trapped electrons is denoted as τ_1, τ_2, and τ_3.

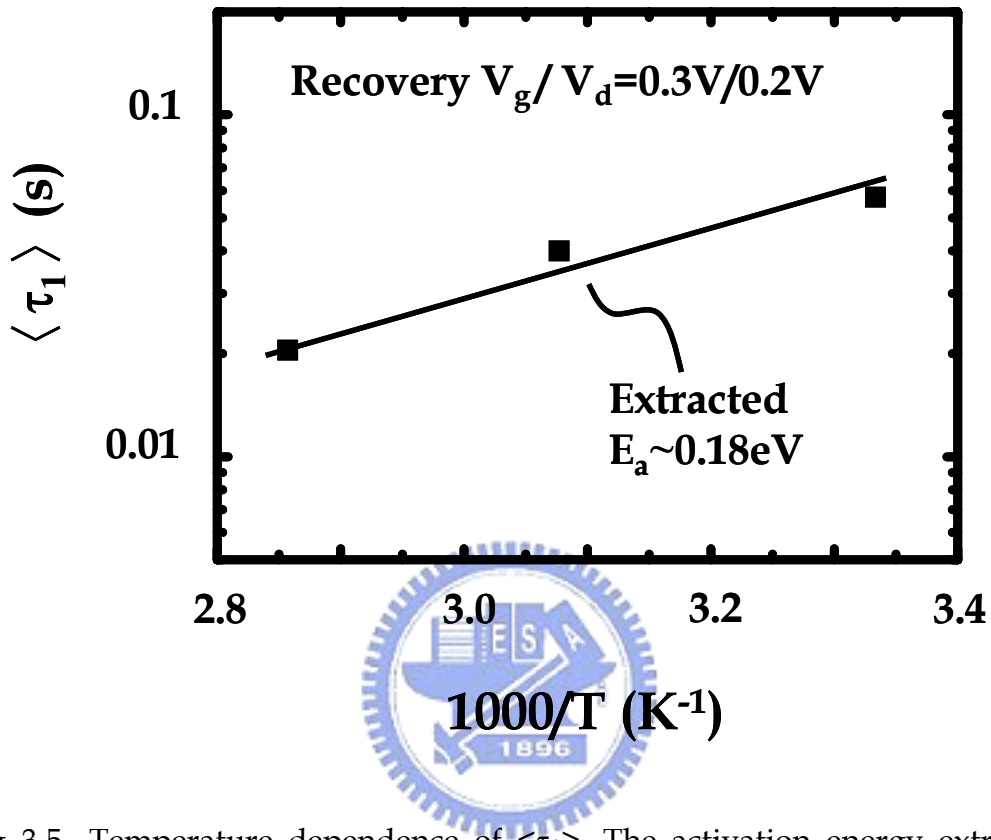

Fig. 3.5 Temperature dependence of $<\tau_1>$. The activation energy extracted from the Arrhenius plot is 0.18eV. Each data point is an average of ten readings.

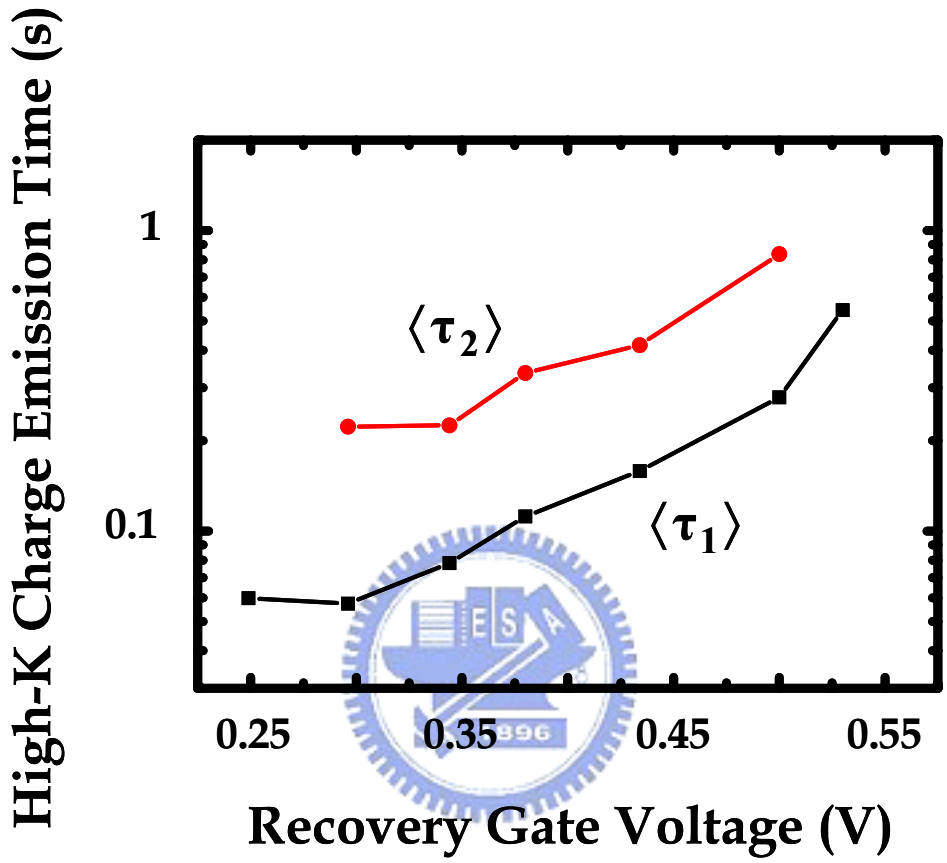

Fig. 3.6 Dependence of trapped electron emission times on recovery gate voltage. Ten measurements are made for each recovery V_g to take average.

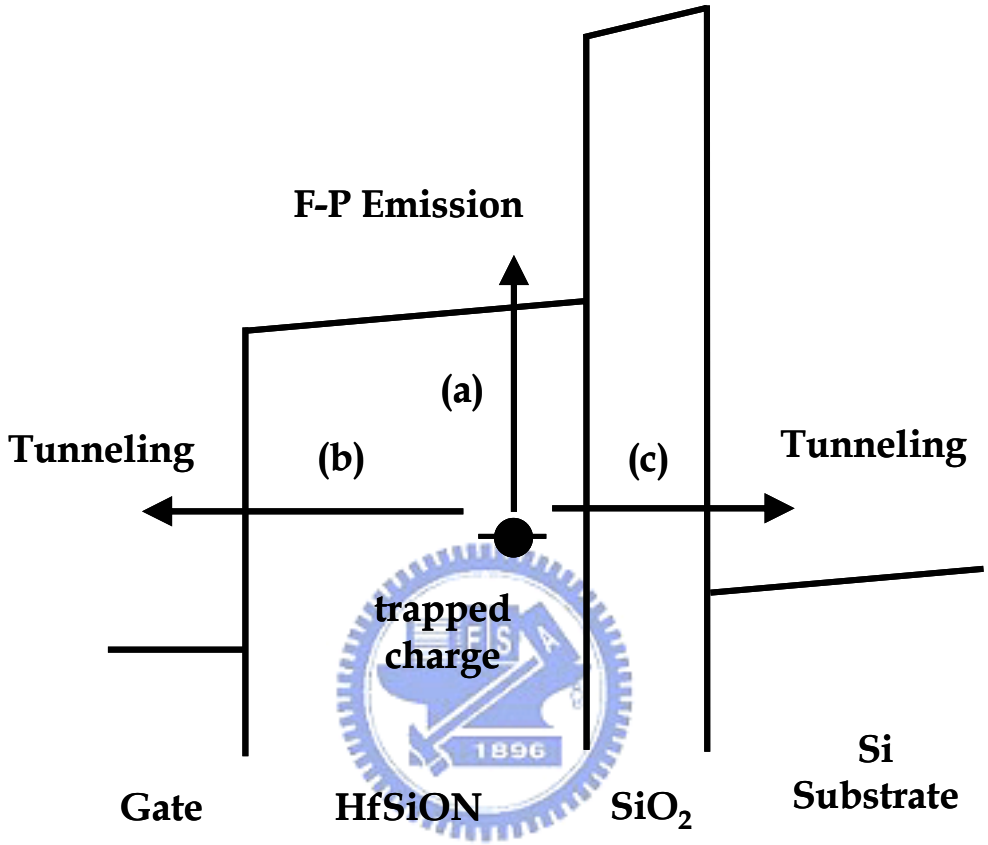

Fig. 3.7 The energy band diagram illustrating possible paths for trapped charge emission: (a) Frenkel-Poole (FP) emission, (b) tunneling to the gate, and (c) tunneling to the Si substrate.

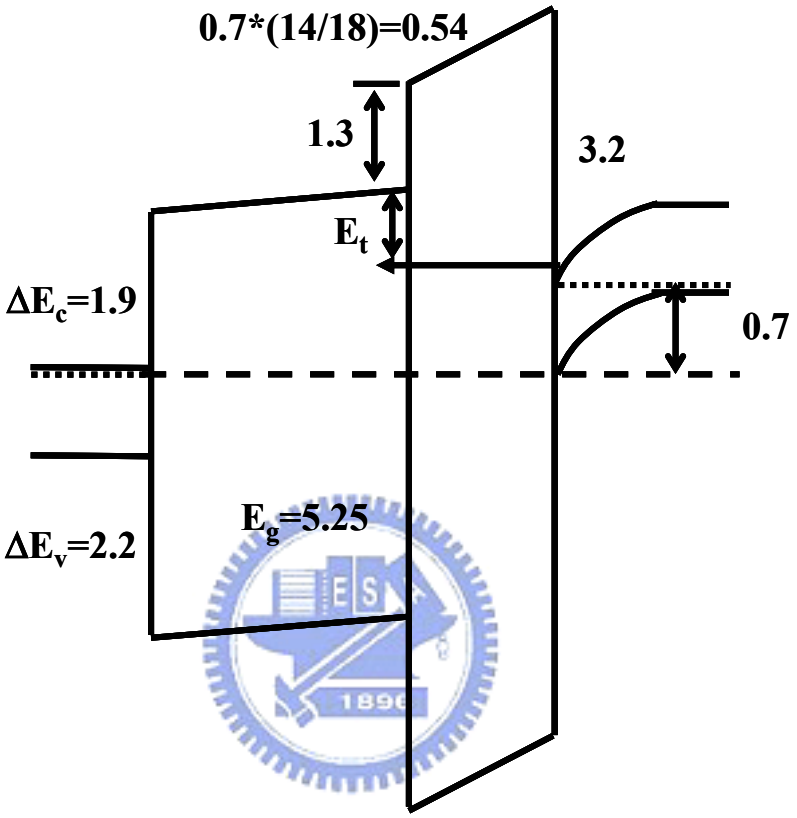

Fig. 3.8 The energy band diagram corresponding to the stress condition where V_g=0.7V is applied to inject electron into the high-k traps.

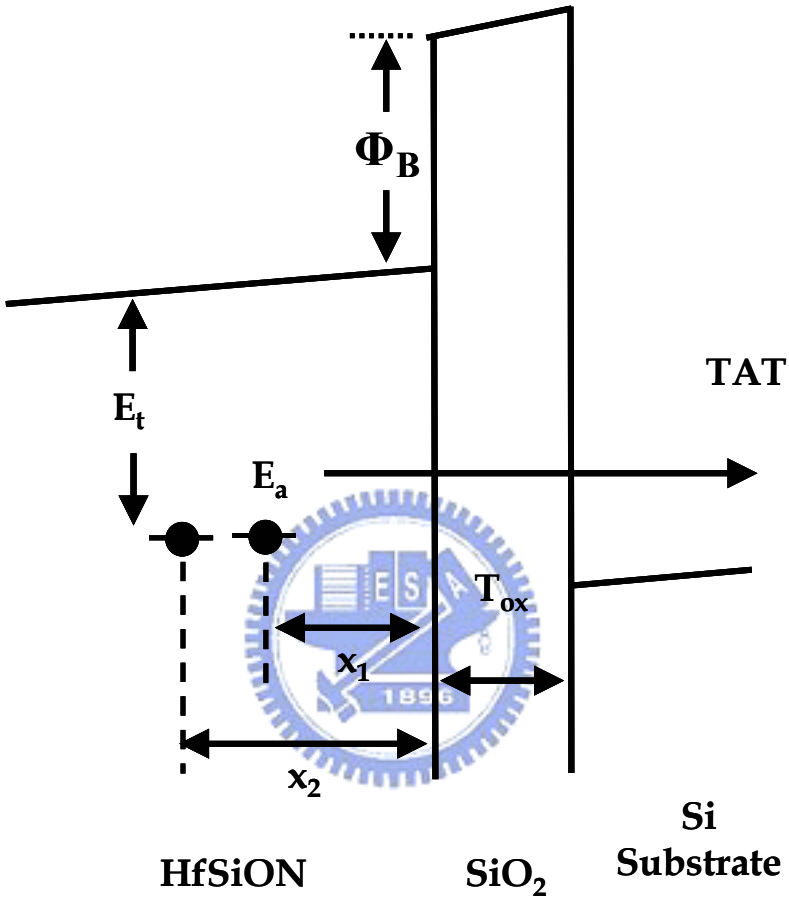

Fig. 3.9 Schematic representation of the band diagram in recovery phase and trap positions. E_a is the activation energy for SRH-like thermally assisted tunneling (TAT).

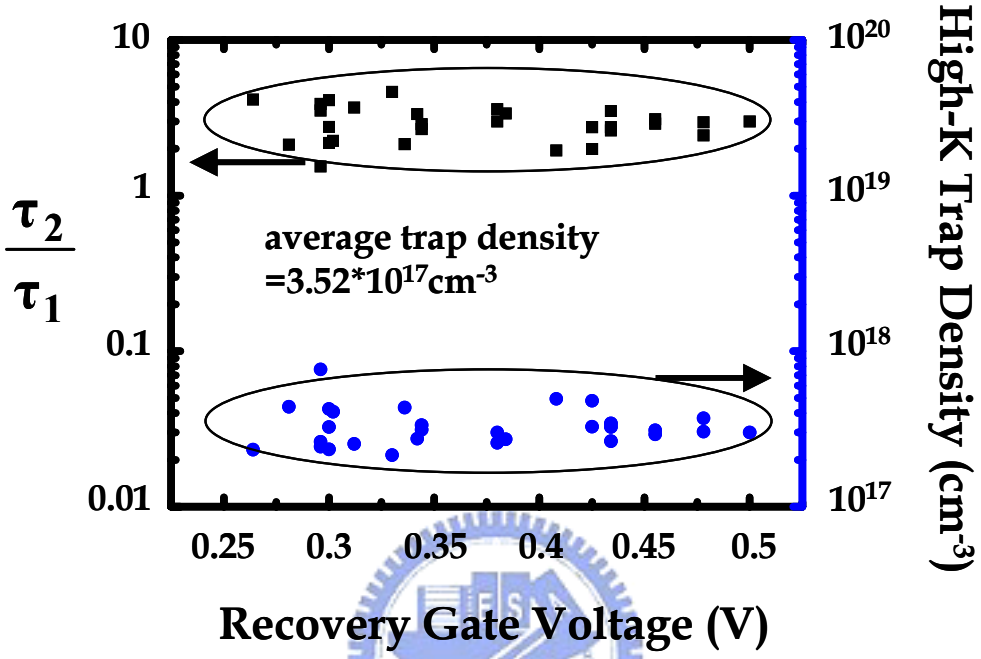

Fig. 3.10 The ratio of τ_2 to τ_1 versus gate voltage in recovery phase. Note that τ_2/τ_1 remains almost unchanged with respect to V_g, as predicted by Eq. (3.3). The extracted high-k trap density is $3.5\times10^{17}cm^{-3}$, or equivalently $8.8\times10^{10}cm^{-2}$.

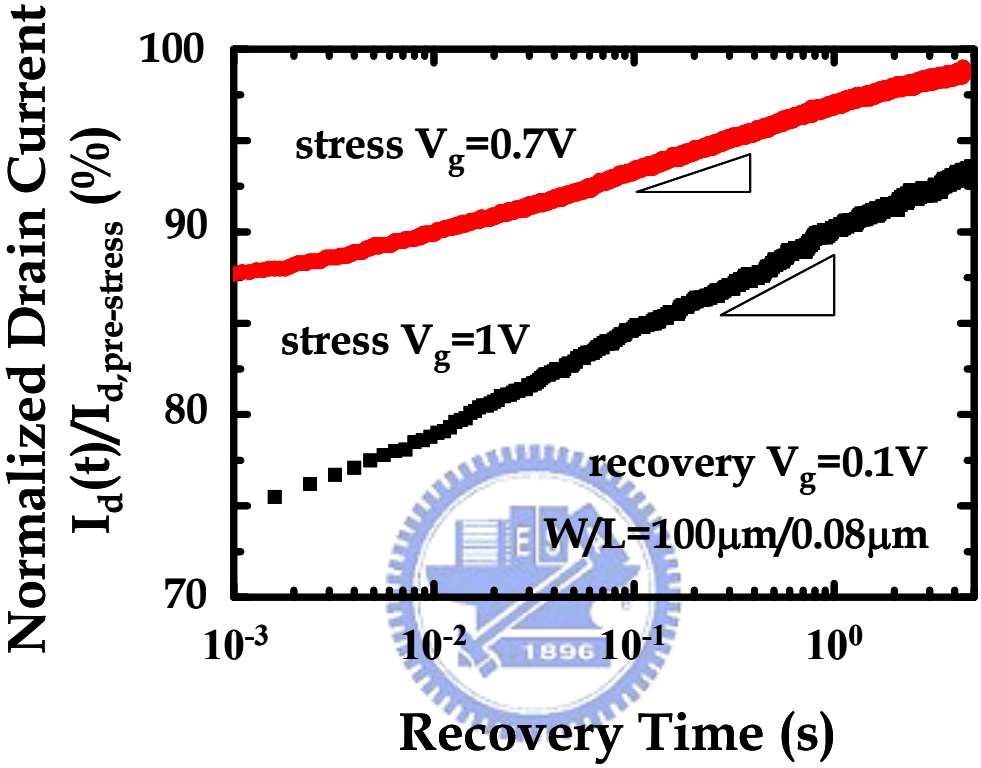

Fig. 3.11 Normalized drain current evolution with recovery time for two stress V_g's (0.7V and 1V). The V_g in recovery phase is 0.1V.

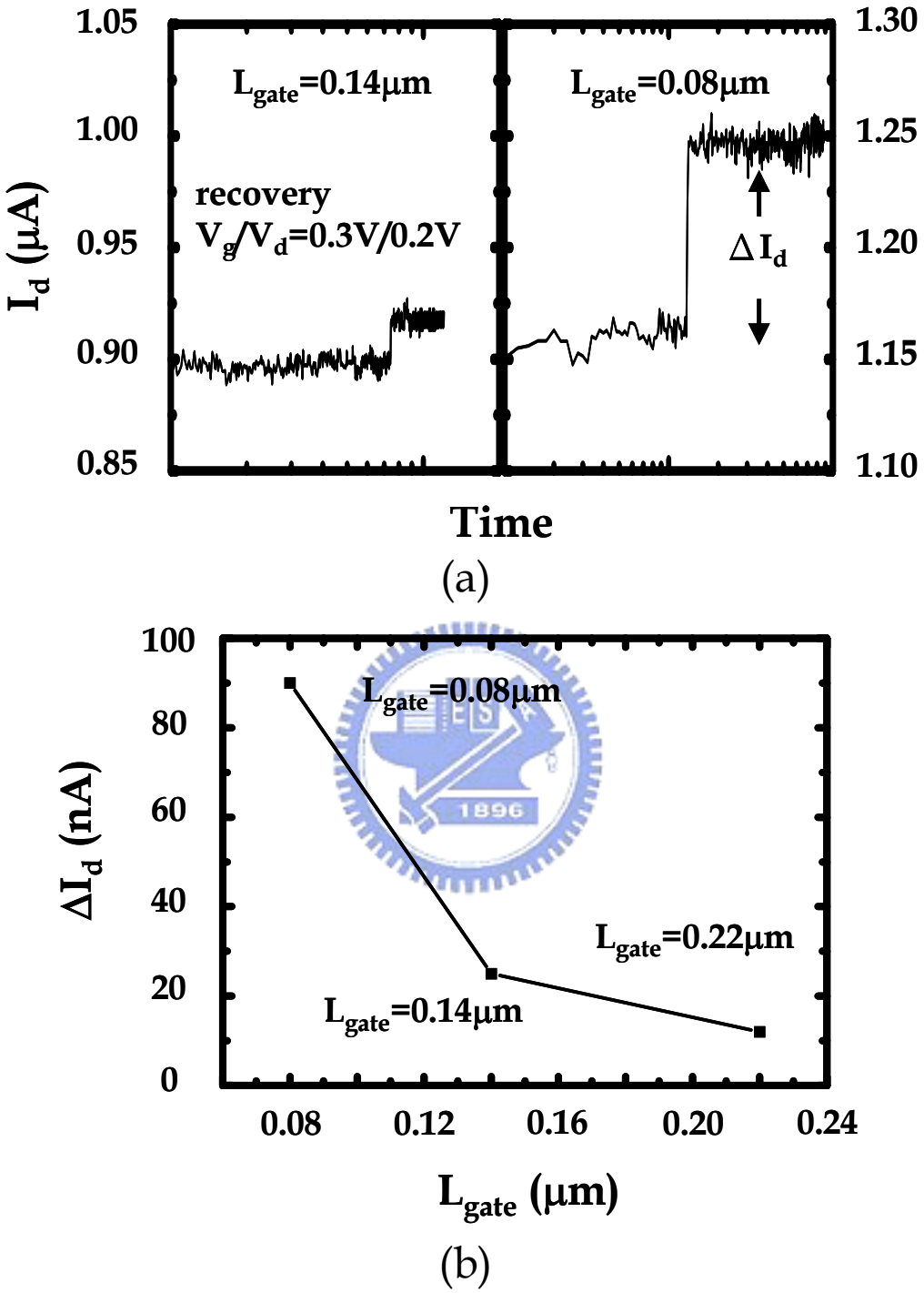

Fig. 3.12 (a) Comparison of the current jump amplitude for L_{gate}=0.14μm and L_{gate}= 0.08μm. Both devices are subject to identical stress and recovery conditions. (b) The amplitude of the current jump versus L_{gate}.

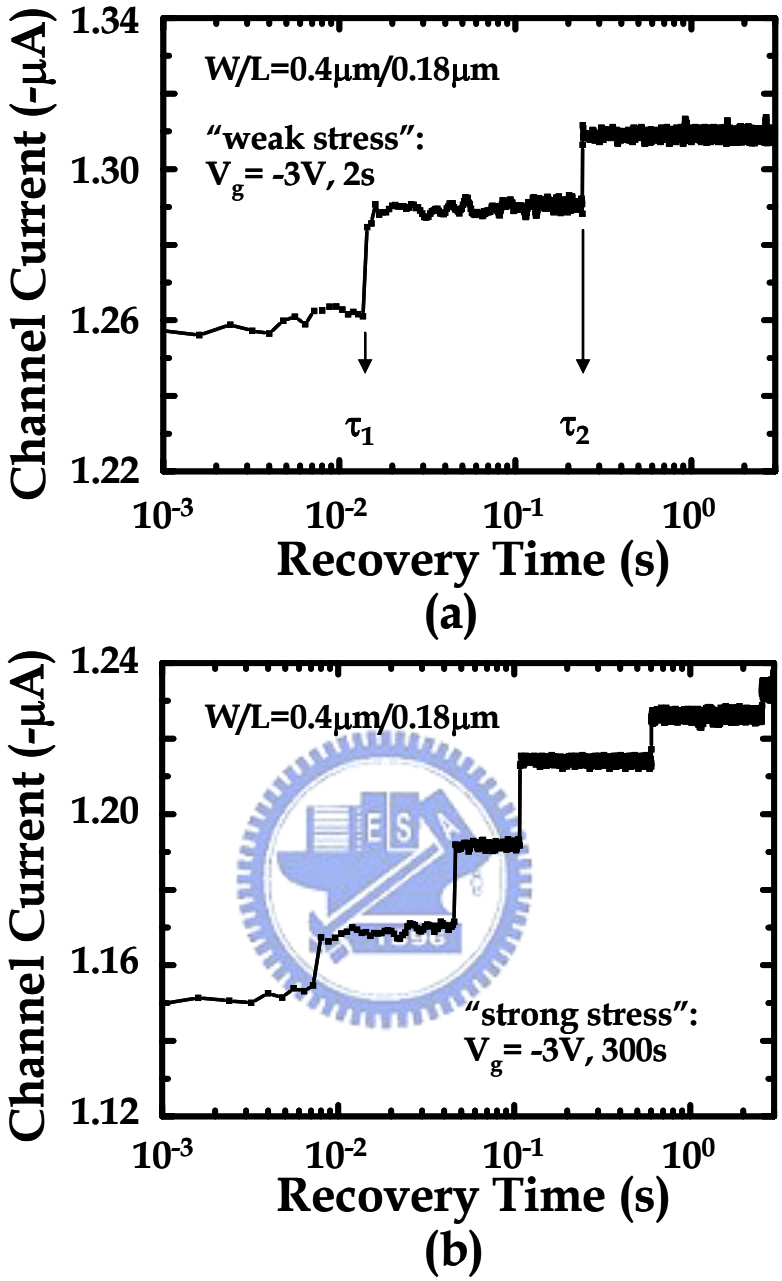

Fig. 3.13 (a) A typical step-like "quantum jump" observed in channel current during NBTI recovery in a SiO_2 pMOSFET. (b) Compared to a "weak stress" condition (V_g= -3V, 2s) in (a) in which only two quantum jumps are measured, a post "strong stress" (V_g= -3V, 300s) recovery has five jumps in the same time window.

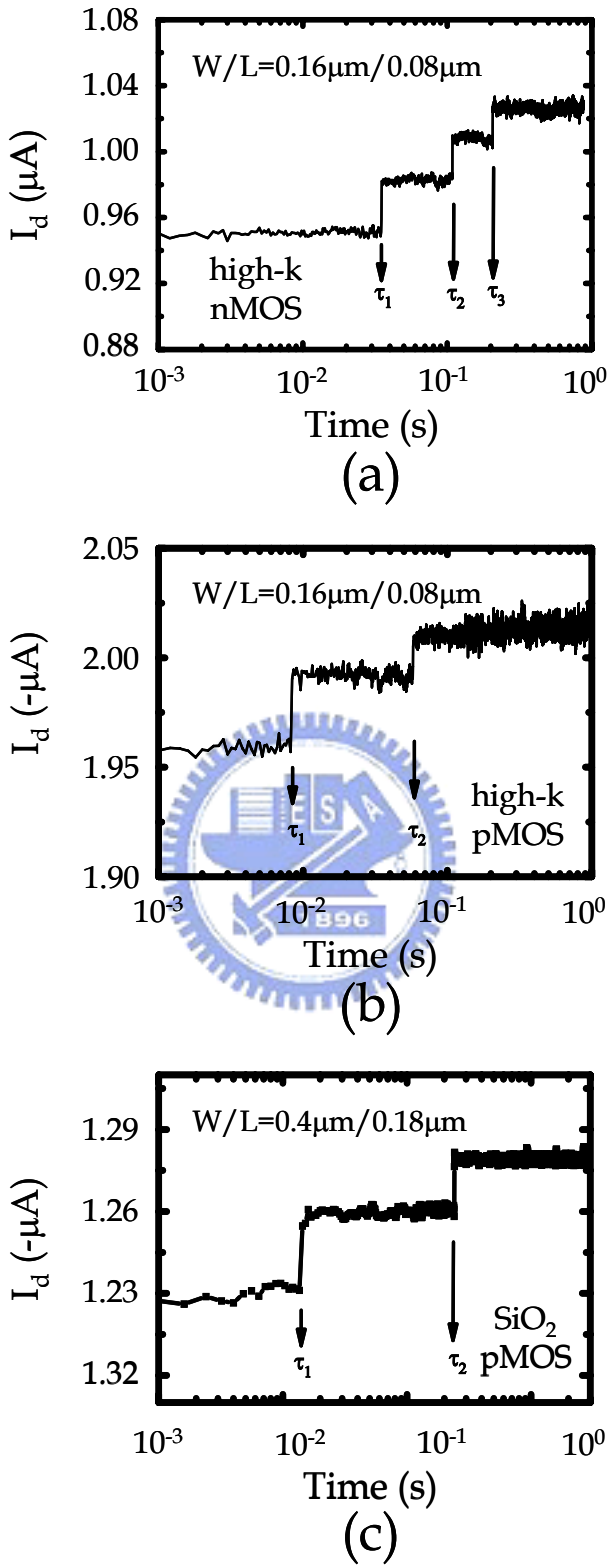

Fig. 3.14 Comparison of the staircase-like current jumps for a (a) high-k nMOS, (b) high-k pMOS, and (c) SiO_2 pMOS device.

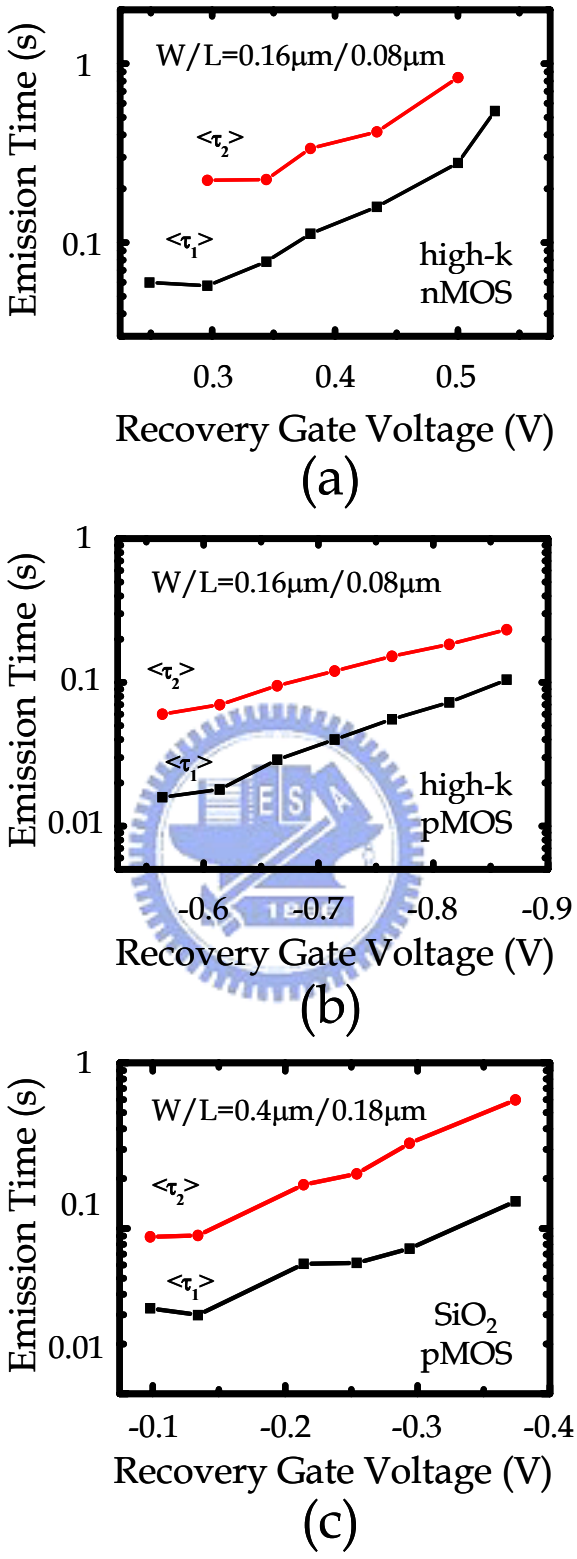

Fig. 3.15 Comparison of the recovery V_g dependence of charge emission times for a (a) high-k nMOS, (b) high-k pMOS, and (c) SiO_2 pMOS device.

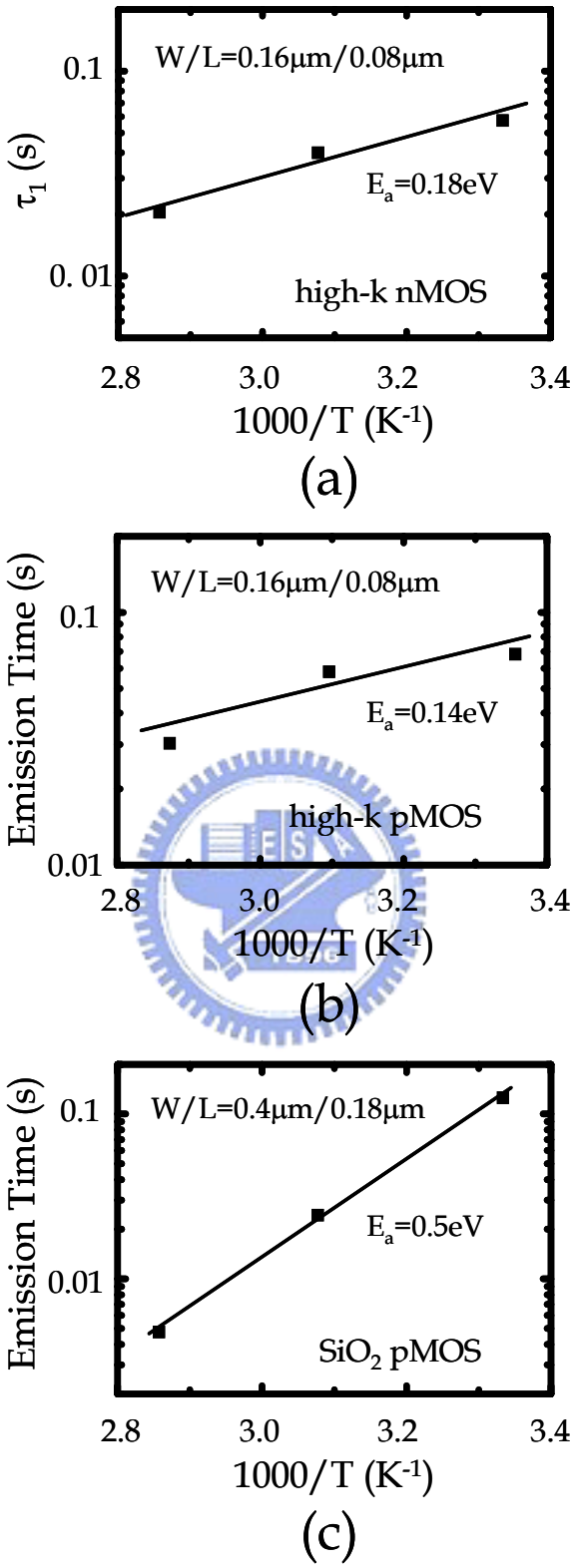

Fig. 3.16 Comparison of the temperature dependence of the first charge emission time. The activation energy E_a is extracted to be (a) 0.18eV for high-k nMOS, (b) 0.14eV for high-k pMOS, and (c) 0.5eV for SiO_2 pMOS device.

Table 3.1 Summary of E_a, τ_1, amplitude of the current jumps (ΔI_d), τ_2/τ_1, and the calculated N_t for high-k nMOS, high-k pMOS, and SiO_2 pMOS devices.

	High-k nMOS	High-k pMOS	SiO_2 pMOS
E_a (eV)	0.18	0.14	0.5
τ_1	on the order of 10^{-2}s		
ΔI_d	several tens of nA		
$<\tau_2/\tau_1>$	3.4	3.06	3.11
N_t ($*10^{10}cm^{-2}$)	8.8	N.A.#	3.5

Reliable hole effective mass in high-k is not reported in literature to date.

Table 3.2 Summary of the values used in the text.

Constant	Value	Note
$m^*_{ox,h}$	$0.42m_0$ [3.20]	hole effective mass in SiO_2
m^*_k	$0.18m_0$ [3.15]	
Φ_B	3.2eV	
E_t [&]	1.36eV	high-k nMOS
	4.7eV	SiO_2 pMOS Si/SiO_2 valence band offset

[&] Although the knowledge of exact trap energy is difficult to obtain, the energy aligned to the applied V_g (see Fig. 3.8) is used here for high-k devices. However, because around every 2.5eV change translates into a 10% variation in trap density, the effect of E_t uncertainty can be ignored. Furthermore, the intention of the work is to provide a theoretical basis for the proposed technique, not to give exact numbers.