Chapter 5

Negative Bias Temperature Instability in High-k pMOSFETs

5.1 Preface

Compared to their n-type counterparts, limited works have focused on the physics of negative bias temperature instability (NBTI) in high-k pMOSFETs [5.1]-[5.3]. The model Zafar et al. proposed [5.1] attributes the creation of positive oxide charges to de-passivation of Si/SiO_2 interface. As Si-H bonds break, hydrogen diffuses away and reacts with the oxide, creating positive charges in the interface and in the oxide. In [5.2][5.3], on the other hand, Houssa et al. presented the impact of forming gas annealing conditions and of Hf content on NBTI. According to their study, the responsible defects are hydrogen-induced overcoordinated oxygen centers induced by the transport and trapping of H^+ in the gate stack. However, in both works a conventional stress-and-sense method is used. De-trapping effect during the switching delay between stress and sense has been demonstrated to be significant in previous chapters and in [5.4]-[5.6]. Thus to investigate the NBTI, the transient measurement technique introduced in Chapter 2 is used in this chapter. An anomalous stress induced drain current (I_d) *enhancement* is observed and the effects of stress gate voltage, stress temperature, and stress duration are introduced in Section 5.3. The responsible physical mechanism – a bipolar charging model is proposed in Section 5.4. Two characterization techniques, charge pumping (CP) and single charge emission,

are performed in Section 5.5 to justify the model. Section 5.6 discusses the impact of high-k film integrity on the anomalous behavior followed by a summary in Section 5.7.

5.2 Devices

The pMOSFETs have a HfSiON layer as the high-k gate dielectric with a L_{eff} of 0.08~1.2μm, and a width of 0.16~10μm. The physical thickness of the high-k layer, thickness of interfacial SiO_2 layer, and the equivalent oxide thickness (EOT) are respectively 2.5nm, 1.4nm, and 1.8nm. Two sets of samples with different nitrogen treatment ("control" vs. "optimal", with "optimal" is known to have better robustness against trap creation[1]) are compared for evaluating the impact of high-k integrity, and the devices belong to the "optimal" set unless otherwise stated. Process details and the reliability characteristics can be found in [5.7][5.8].

5.3 Anomalous Drain Current Degradation

Fig. 5.1 shows a typical temporal evolution of NBT stress induced linear drain current instability ($\Delta I_{d,lin}$), measured by using a conventional stress-and-sense method with a switching delay and by using the transient technique. The stress gate voltage is -2.8V, and the linear drain current is measured at V_g/V_d= -1.2V/-0.2V. Subtle $\Delta I_{d,lin}$ is observed with the conventional method meaning, again, significant charge detrapping is taking place. In contrast, if the NBTI characterization is performed by using the transient measurement technique (with V_g/V_d waveforms depicted in Fig.

[1] Refer to Section 4.4.4 or to [5.7] for details

5.2), unexpected results are observed. Fig. 5.3 and Fig. 5.4 demonstrate $\Delta I_{d,lin}$ as a function of stress time. Stress gate voltage (V_g) ranges from -1.2V to -2.8V and temperatures from 25C to 125C are applied for NBT stress (selectively shown for clarity). Anomalously and intriguingly, stress induced I_d enhancement ($\Delta I_{d,lin}$>0) for larger $|V_g|$ and/or higher temperature is observed for the initial stage of stress. At prolonged stress times, a turn-around behavior is noticed, and the polarity of $\Delta I_{d,lin}$ changes from positive (enhancement) to negative (degradation). Fig. 5.5 and Fig. 5.6 summarize the effects of stress V_g, temperature, and stress duration. Shown in Fig. 5.5, for t=0.1s, low $|V_g\text{'s}|$ (-1.4V~-2V) induce I_d degradation which worsens as $|V_g|$ increases. As $|V_g|$ further increases, $|\Delta I_d|$ turns around and the polarity becomes positive, or enhancement. This trend remains for t=10s, but the turn-around $|V_g|$ is slightly larger. Interestingly for 1000s, the $|\Delta I_d|$ trend evolves to that as in SiO_2, i.e. a higher $|V_g|$ monotonically induces worse degradation. Moreover, for short stress periods, $|\Delta I_d|$ changes from negative for low T to positive for high T, as indicated in Fig. 5.6. For long stress periods, the trend, again, evolves to that as expected, or a higher T monotonically results in worse degradation. One point worth mentioning is that the I_d enhancement is observed mainly for t<10s. If the transient de-trapping effect cannot be avoided (as in a conventional method), there is a possibility that one fails to observe the abnormal phenomena.

5.4 The Bipolar Charging Model

Under a negative V_g stress, three possible factors lead to I_d instability[2]: (i)

[2] Both charge trapping in the gate stack and the interface degradation may give rise to drain

trapping of the valence electrons from the poly-gate into high-k traps ($\Delta I_d>0$); (ii) trapping of the holes from the inversion channel into high-k traps ($\Delta I_d<0$), and (iii) interfacial SiO_2 layer (IL) degradation and concomitant positive oxide charge (holes and/or hydrogen-related species) buildup ($\Delta I_d<0$). Fig. 5.7(a) depicts the energy band diagram at equilibrium. Trap sites whose energy depths (E_t) are below the Fermi level (E_F) are completely[3] occupied while those above E_F are empty[4]. When $|V_g|$ is low as shown in Fig. 5.7(b), the much smaller electric field in the high-k layer introduces a minute amount of empty trap states. Thus charge trapping into the high-k layer, i.e. (i) (the solid arrow) and (ii) (the open arrow) is negligible, and ΔI_d is dominated by (iii)[5] which leads to I_d degradation ($\Delta I_d<0$). In this regime, a larger $|V_g|$ aggravates $|\Delta I_d|$. As the $|V_g|$ is raised (Fig.5.5(c)), a significant amount of empty traps is now readily for trapping both electrons and holes. The presence of IL, however, delays the latter. Therefore, I_d initially increases due to dominant electron trapping. As the stress time extends, hole trapping (into traps in high-k and IL) and interface degradation outgrow, accounting for I_d degradation (Fig. 5.3). The role of temperature is described as follows. A higher T accelerates high-k trap creation [5.9] accommodating more charges (again, electrons respond faster than holes). The polarity of $|\Delta I_d|$ would

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current instability. Factors (i) and (ii) are effective through the former which changes the device threshold voltage, and factor (iii) through the latter which degrades carrier mobility. Additional trap creation in high-k layer enhances factors (i) and (ii) and is discussed in the next section.

[3] The thermal broadening of Fermi-Dirac distribution is ignored.

[4] At equilibrium, the Fermi levels of the gate electrode and the Si substrate are aligned ($E_{Fn}=E_{Fp}=E_F$, Fig. 5.7). The traps below this aligned E_F have very large trapping time constants as compared to detrapping time constants, thus leading to a trap occupation factor (the probability of a trap being filled with a charge) close to unity. For those above the aligned E_F, the situation is reversed and leads to a trap occupation factor close to none.

[5] For low $|Vg's|$, creation of interface states is hardly detectable (see Section 5.5 for charge pumping measurements). In this case, hole trapping into the initial traps of IL is the major source for I_d degradation.

even be reversed from negative to positive (Fig. 5.4 and Fig. 5.6). Meanwhile, a higher T aggravates IL degradation as well, introducing positive charges (holes and/or hydrogen-related species) into the gate dielectric as the theory for NBTI in SiO_2 predicts. Electron charging initially predominates, and hole charging gradually takes over, giving rise to Fig. 5.4. Furthermore, the effect of stress duration is manifested in Fig. 5.5 and Fig. 5.6. The drain current is only enhanced for t<10s no matter of stress V_g or temperature. The anomalous turn-around behavior is easily ignored if the transient measurement technique is not utilized. Charge pumping and single charge emission are measured to investigate generation of additional (interface and high-k bulk) traps in the next two sections.

5.5 Charge Pumping and Single Charge Emission

In previous chapters, direct measurement of single charge emission from dielectric traps have been reported in high-k nMOSFETs [5.4][5.9] as well as in SiO_2 pMOSFETs [5.10]. Fig. 5.8 shows the patterns of recovery drain current for low (-1.5V) and high (-2.2V) stress V_g which reveal charge species injected during stress. The measurement setup and experimental waveforms are identical with the one in Fig. 3.1. The recovery condition is V_g around the device threshold voltage to magnify the impact of single charge on drain current[6]. An upward jump in I_d (increase in $|I_d|$) corresponds to a single hole escape, and a downward shift (decrease in $|I_d|$) to a single electron. As can be clearly seen in Fig. 5.8(a), only holes are trapped during a low $|V_g|$ stress, while both electrons and holes during a high $|V_g|$ stress are

[6] The details of the single charge emission measurement are described in Chapter 3.

introduced into the trap states as indicated in Fig. 5.8(b). Direct observation of both electron and hole charges confirms the bipolar charging model proposed in Section 5.4.

In addition to single charge emission, charge pumping measurements are performed. The waveforms and corresponding values of CP parameters are given in Fig. 5.9. A two-frequency CP method is used to discriminate between high-k traps and interface traps[7]. The high frequency (1MHz in this experiment) results monitor interface traps. The difference between low frequency (5kHz) and high frequency is taken to monitor high-k bulk traps which, compared to the interface traps, are slow in response to high frequency pulses. Fig. 5.10(a) and Fig. 5.10(b) demonstrate CP results respectively for exploration of stress voltage effect and for the impact of gate stack integrity. As compared in Fig. 5.10(a), a low stress V_g (-1.5V) creates neither interface traps nor high-k bulk ones even for 1000s, verifying that hole charging into initial traps in IL[8] dominates ΔI_d. A high stress V_g (-2.2V) on the other hand, generates both interface states (IL degradation) and high-k bulk traps (N_{HK}).

5.6 Impact of High-k Integrity

Two sets of transistors with known relative robustness against high-k bulk trap generation are compared to study the impact of high-k integrity on the anomalous NBTI induced drain current instability. As consistently shown in Fig. 5.10(b), the "optimal" sample resists high-k trap creation more

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[7] The two-frequency CP technique is described in detail in Chapter 3 and Chapter 4.

[8] Undetectable high-k/interface trap generation implies that only pre-existing traps are involved. If charge trapping into the high-k layer plays a role, one should observe I_d enhancement followed by I_d degradation like Fig. 5.3 for electrons respond faster than holes due to the presence of IL (see Section 5.4). Since for low stress $|V_g$'s$|$, only degradation is measured, charging of high-k traps can be ruled out.

effectively whose I_d initially increases as dictated by electron trapping into high-k traps (ΔI_d>0) and then evolves toward degradation (ΔI_d<0) as dominated by hole charging/IL degradation (Fig. 5.3 through Fig. 5.6). On the contrary, additional interface and bulk traps are continually created in "control" devices. Thus electron trapping remains predominant[9], and ΔI_d keeps increasing positively as indicated in Fig. 5.11. Even for a stress time as long as 1000s, the V_g dependence still exhibits a turn-around feature (Fig. 5.12), as opposed to that for an optimal device shown in Fig. 5.5.

5.7 Summary

NBTI-induced drain current instability in HfSiON pMOSFETs featuring I_d enhancement followed by I_d degradation has been demonstrated. For all combinations of stress V_g and temperature in this chapter, the anomalous turn-around behavior takes place within ~10s; thereafter returns to monotonic degradation as in SiO_2. A conventional stress-and-sense characterization method may fail to capture this feature because of the switching delay lasting for seconds. A bipolar charging model along with trap generation is proposed to account for the experimental results as summarized in Table 5.1. Electron trapping is found to be predominant, leading to I_d enhancement for short term and/or a high $|V_g|$ stress. As the stress evolves with time, hole trapping/IL degradation eventually take over. For a low $|V_g|$ stress, hole trapping/IL degradation dictates throughout whole stress period. Even

[9] The effect of a large stress V_g is twofold: a) While electrical stress "creates" new trap sites, b) a large V_g "empties" a wider range of traps (a large ΔE_t, see Fig. 5.7(c)). No matter of newly generated or pre-existing, these trap sites accommodate more charges. As discussed in Section 5.4, electrons respond faster to the applied V_g than holes do. The magnitude and time duration of positive ΔI_d is thus expected to be larger and longer. These are justified by Fig. 5.3, Fig. 5.5, and Fig. 5.11.

under an identical stress condition, the polarity of ΔI_d in an optimized ($\Delta I_d>0$, I_d enhancement) and in a non-optimized ($\Delta I_d<0$, I_d degradation) high-k film may opposite as a result of additional trap generation. Dependence of the dominant mechanism on high-k integrity and stress conditions necessitates further study for extrapolating device lifetime with a correct methodology.

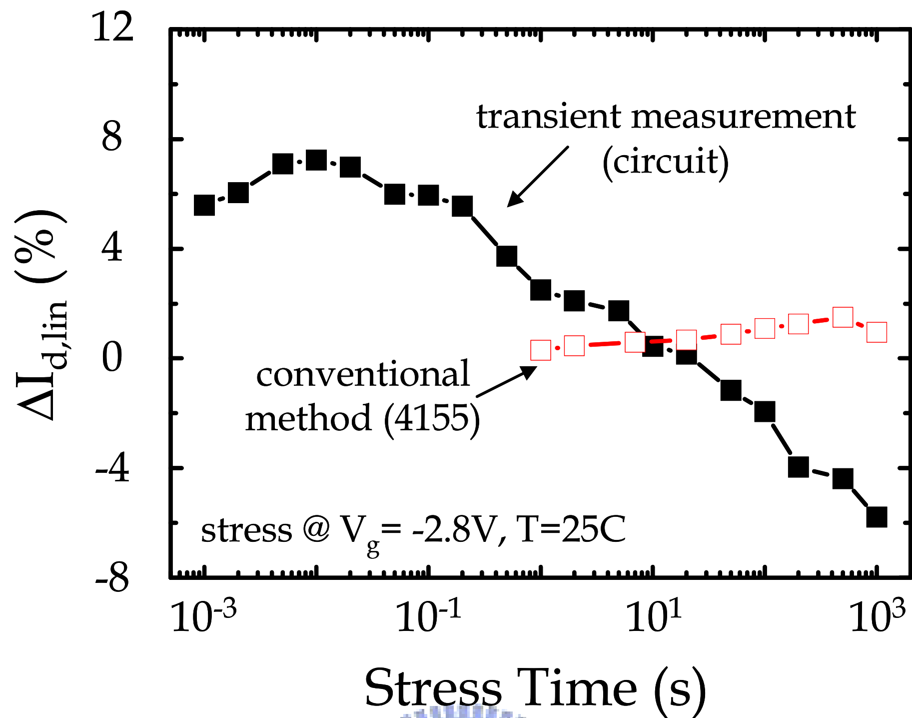


Fig. 5.1 NBTI degradation measured by using a conventional method and by using the transient measurement system described in Chapter 2. The transient measurement technique retrieves significant amount of I_d instability and anomalous characteristics.

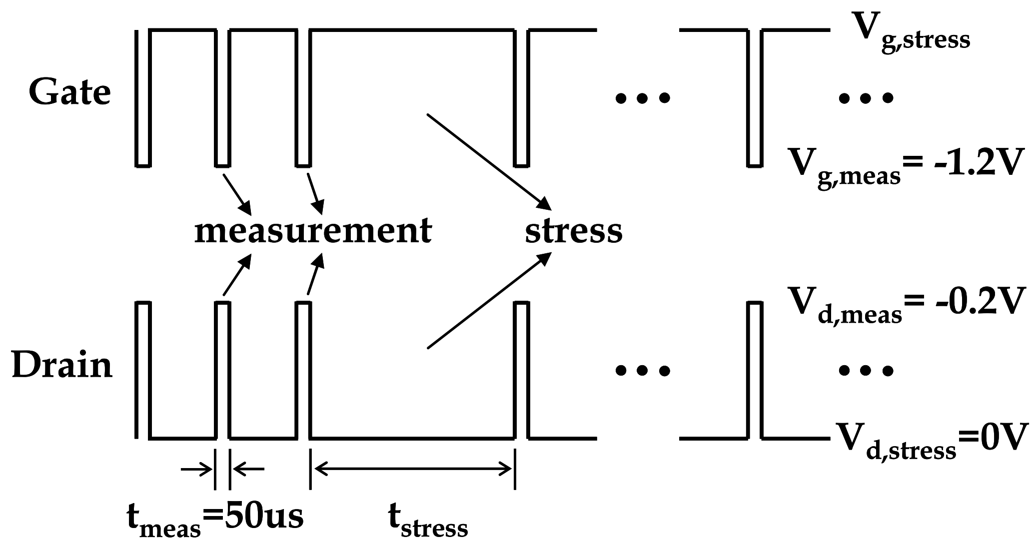
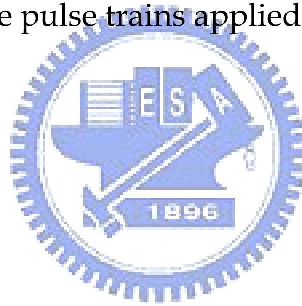


Fig. 5.2 The pulse trains applied to gate and drain.



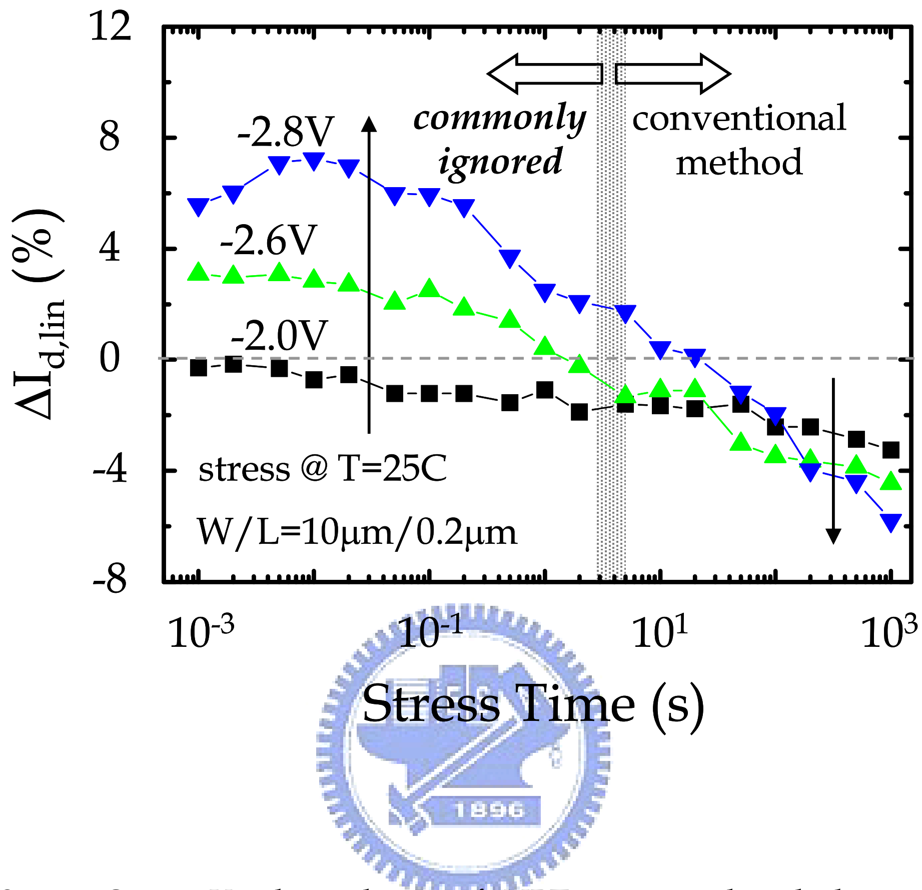


Fig. 5.3 Stress V_g dependence of NBT stress induced drain current change. Anomalous current enhancement during the initial stage of stressing and a turn-around behavior are observed for high $|V_g$'s$|$.

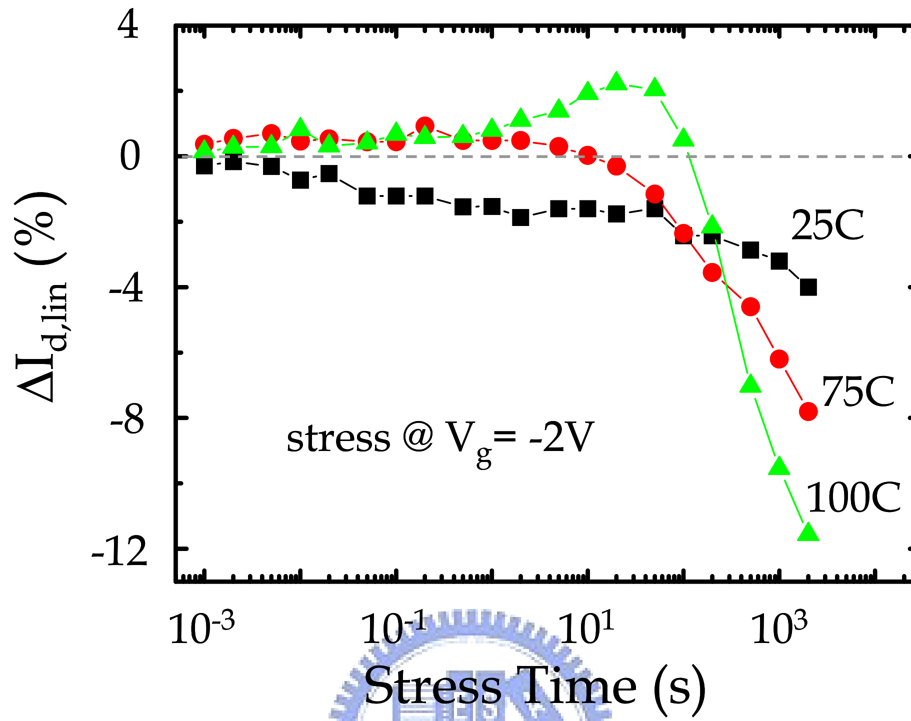


Fig. 5.4 Stress temperature dependence of NBT stress induced drain current change. Anomalous turn-around is also observed for high T.

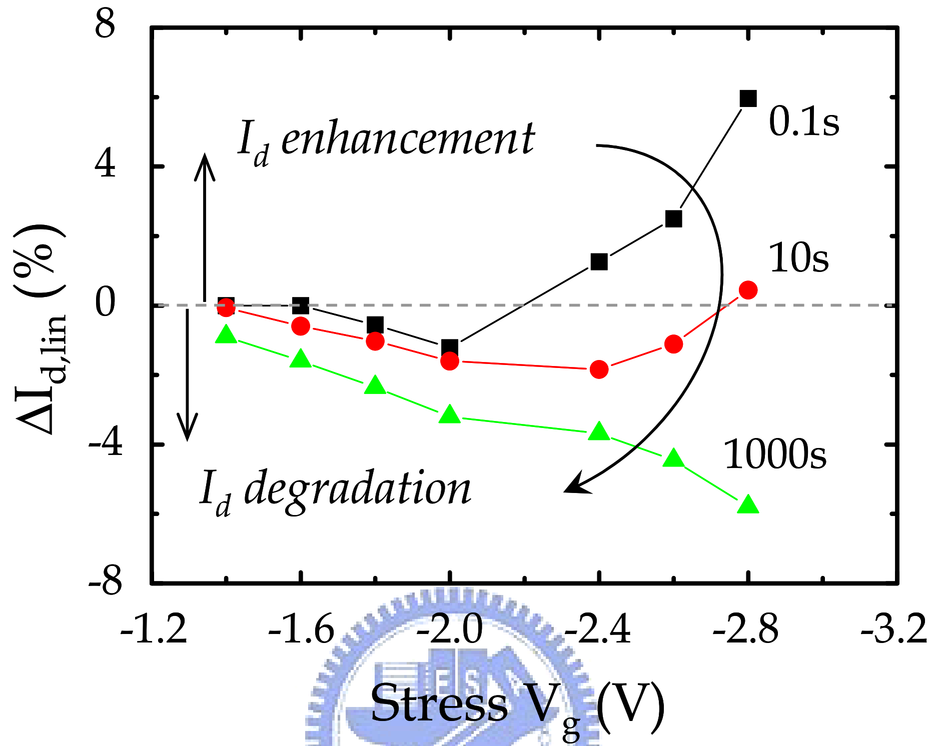


Fig. 5.5 Stress V_g effect at different stages of stressing. For short stress durations (0.1s, 10s), a concave-up V_g dependence is observed. For prolonged stressing (1000s), the trend evolves to that as expected, or a higher $|V_g|$ induces worse degradation.

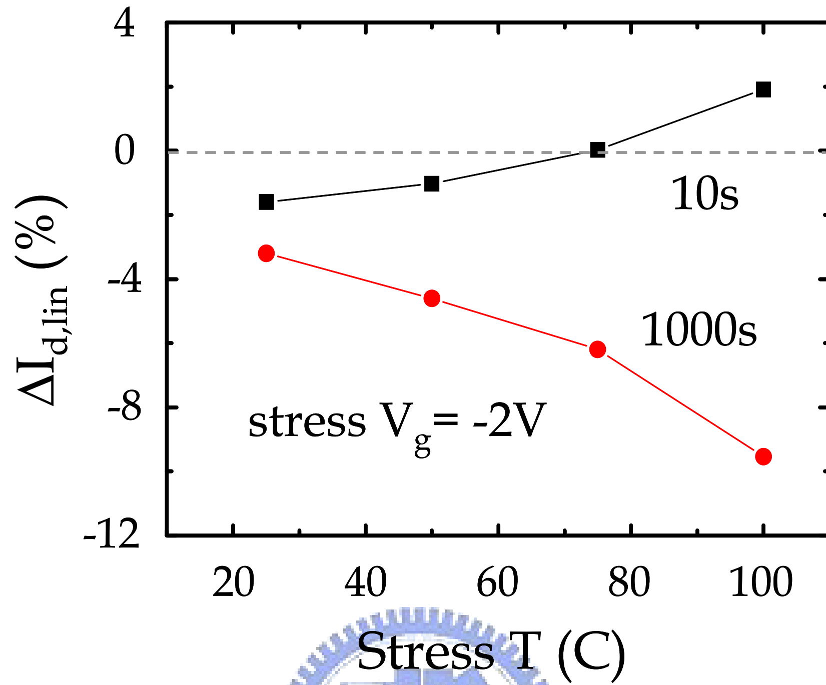


Fig. 5.6 Stress temperature effect at different stages of stressing. While for a short stress duration (10s) $\Delta I_{d,lin}$ changes from degradation for low T to enhancement for high T, a long stressing period (1000s) gives a trend as expected, or a higher T induces worse degradation.

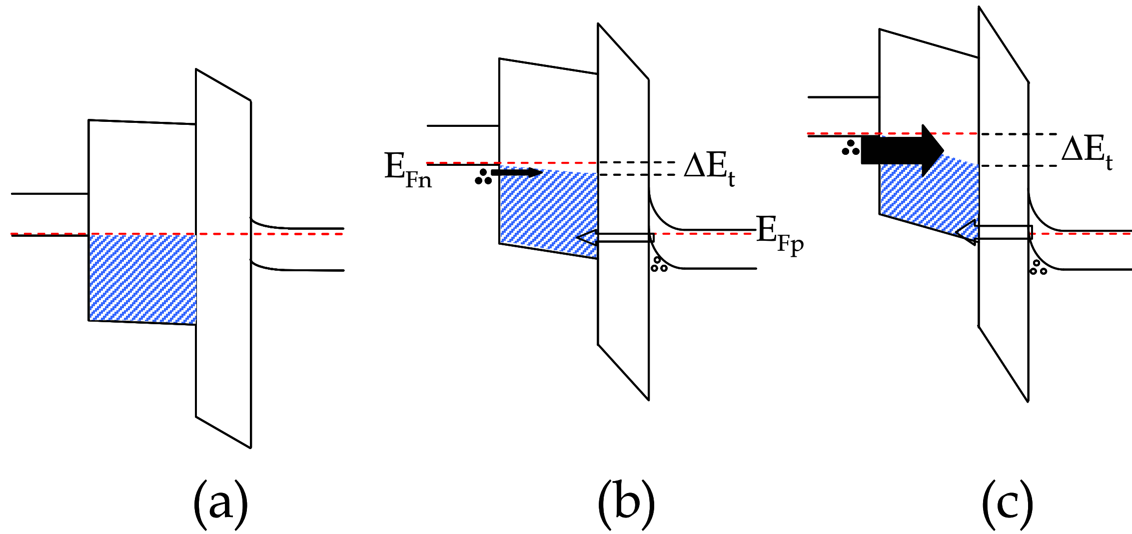
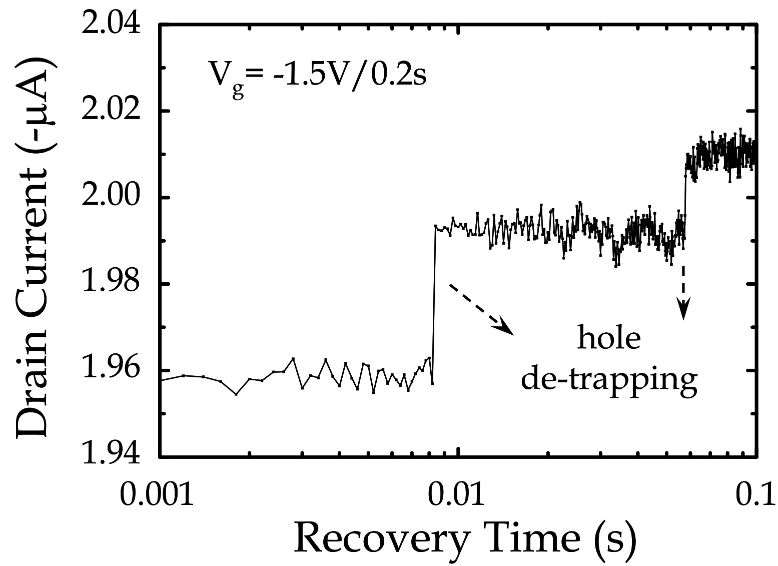
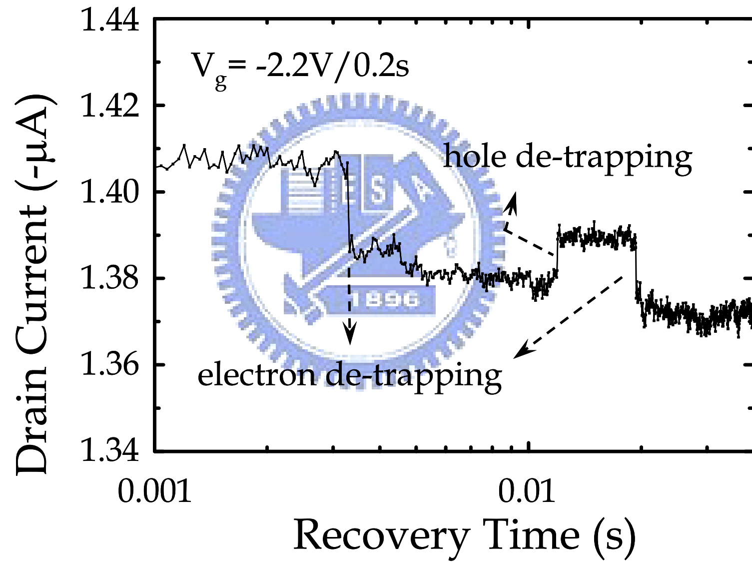


Fig. 5.7 Energy band diagram at equilibrium (a), for a low stress $|V_g|$ (b), and for a high stress $|V_g|$ (c). ΔE_t denotes the available trap sites in high-k readily for trapping valence electrons from the poly-gate, and increases significantly for a high stress $|V_g|$.



(a)



(b)

Fig. 5.8 Recovery transient I_d in small area devices for short stress time (0.2s) for a low $|V_g|$ (-1.5V) (a), and for a high $|V_g|$ (-2.2V). Discontinuous current changes represent charge escape from dielectric traps, revealing the charge species injected during stress. An upward jump corresponds to a single hole charge, and a downward shift to a single electron. For the low $|V_g|$ case, only two holes are trapped during stress, while for the high $|V_g|$ case both electrons and holes are introduced into dielectric traps during stress.

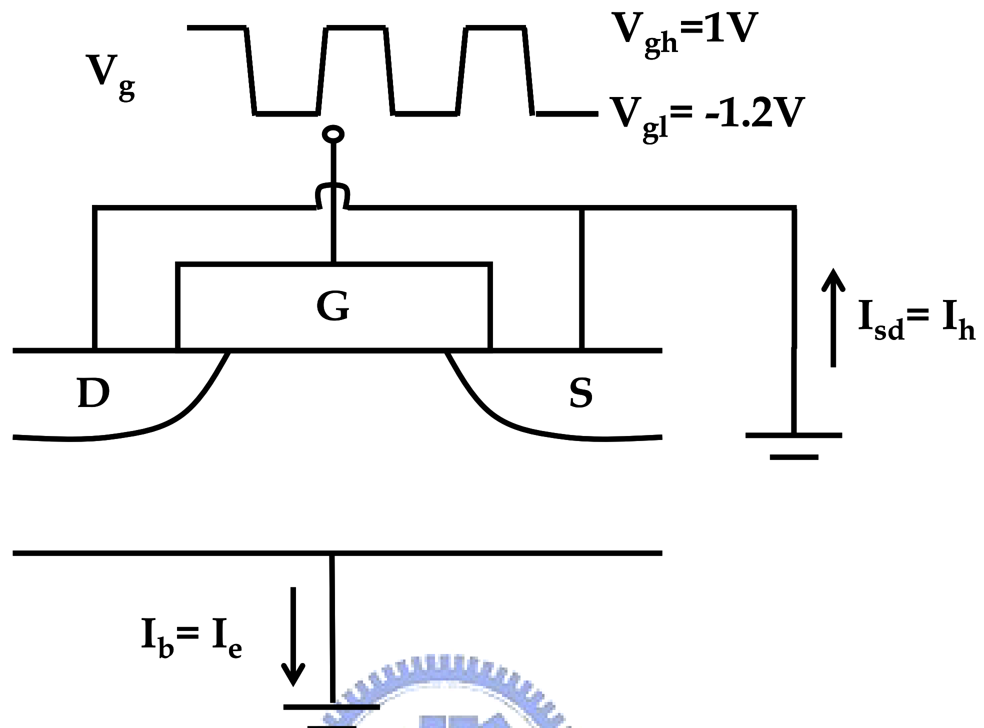
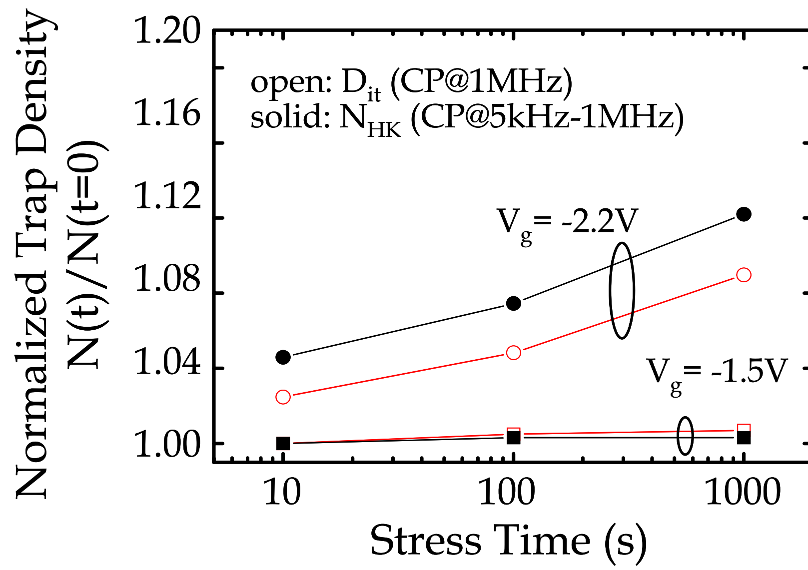


Fig. 5.9 A schematic diagram illustrating the bias conditions for charge pumping measurement in a pMOSFET.



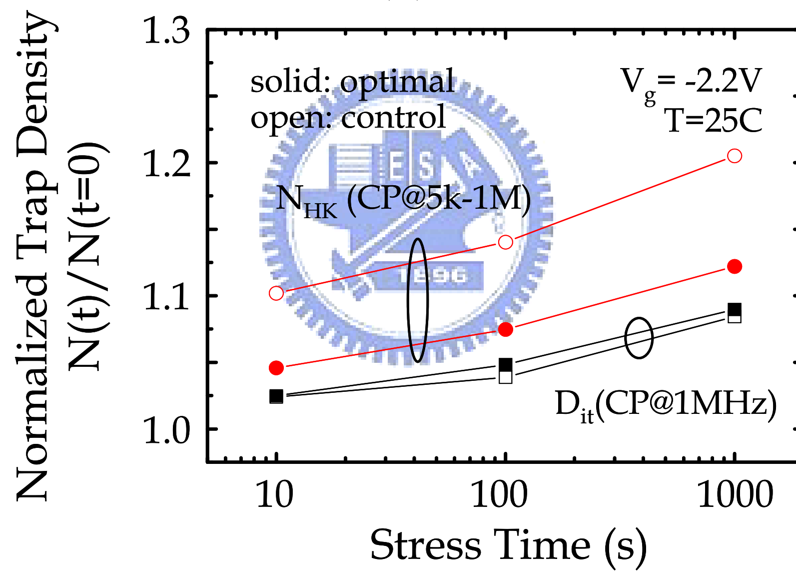


Fig. 5.10 Charge pumping measurement before and after stress. The effect of stress $|V_g|$ is indicated in (a). Impact of high-k integrity is compared in (b).

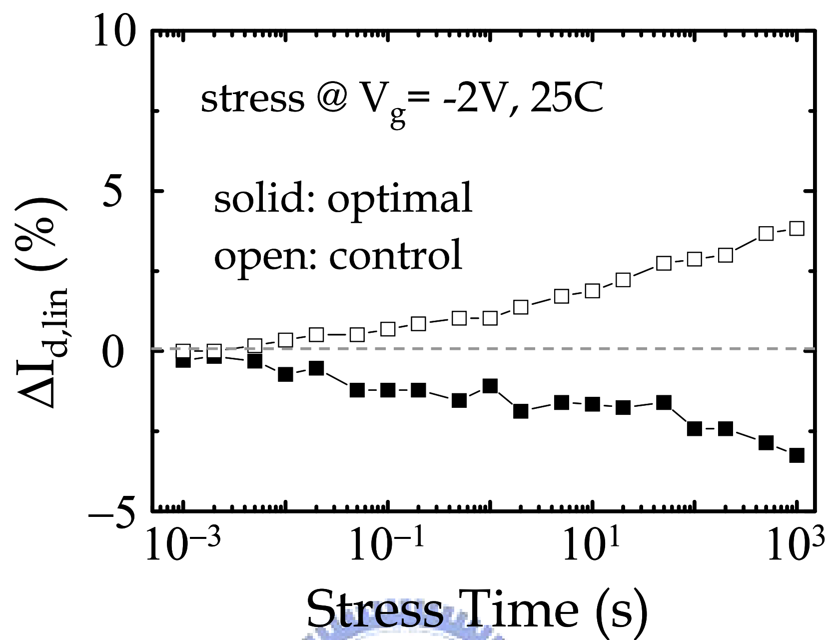


Fig. 5.11 Impact of high-k integrity on ΔI_d behavior. High-k integrity determines the polarity of ΔI_d.

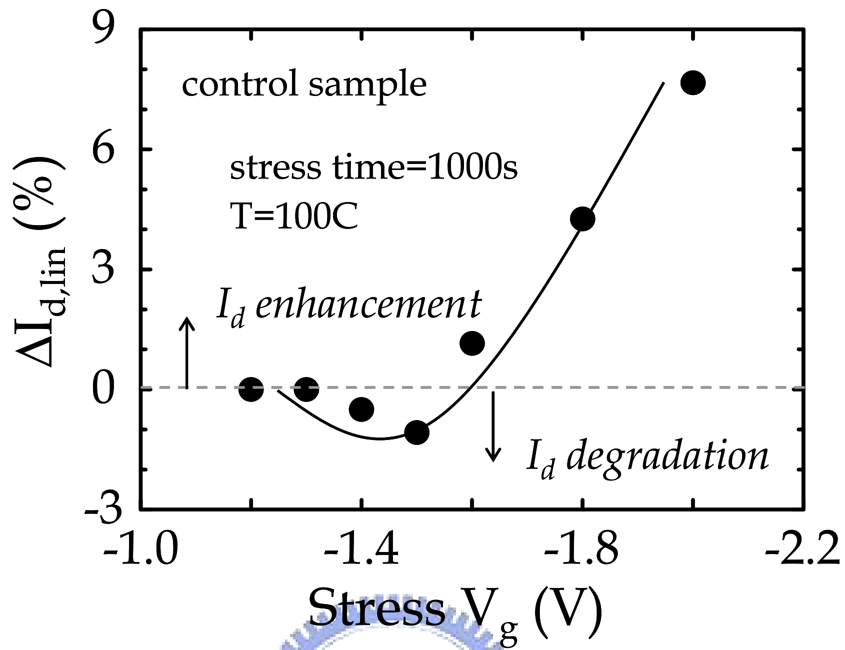


Fig. 5.12 Even for a stress time long as 1000s, the V_g dependence still exhibits a turn-around feature, as opposed to that for an optimal device as indicated in Fig. 5.5.

Table 5.1 Summary of dominant degradation mechanisms under various stress conditions. Detailed discussions are given in the text.

<table>
<tr><th>$\lvert V_g \rvert$ \ Time</th><th>Short-Term</th><th>Long-Term</th></tr>
<tr><td>Low</td><td>1.Hole trapping into IL</td><td>1.Hole trapping into IL
2.IL degradation*</td></tr>
<tr><td>High</td><td>1.Electron trapping into HK
2.Hole trapping into HK/IL
3.IL degradation*</td><td>1.Hole trapping into HK/IL and/or IL degradation*
2.Electron trapping into HK</td></tr>
<tr><td colspan="2">Considering additional high-k trap generation:</td><td rowspan="3">accommodating additional charges (preferably electrons) into stress created trap sites</td></tr>
<tr><td colspan="2">1.Temperature: raising T accelerates trap creation</td></tr>
<tr><td colspan="2">2.Processing: an optimal nitrogen treatment strengthens high-k against bulk trap creation</td></tr>
</table>

* The effect of IL degradation is twofold: generation of interface states and *concomitant* buildup of positive oxide charges in the SiO_2.