國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

前瞻非揮發性記憶體元件之研究

Study on Advanced Nonvolatile Memory Devices

研 究 生： 顏 碩 廷

指導教授： 施 敏 博士

張 鼎 張 博士

中 華 民 國 九 十 三 年 六 月

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事由：推薦電子研究所博士班研究生顏碩廷提出論文，參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生顏碩廷，業已修畢部訂所需課程學分，通過博士資格考之學科考試，並完成博士論文「前瞻非揮發性記憶體元件之研究」初稿，且有數篇相關之論文發表或送審，茲列舉如下：

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3. T. C. Chang, **S. T. Yan**, F. M. Yang, P. T. Liu and S. M. Sze, "Memory effect of oxide/SiC:O/oxide sandwiched structures", *Appl. Phys. Lett.*, **84**, 2094 (2004).
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5. T. C. Chang, **S. T. Yan**, C. H. Hsu, M. T. Tang, J. F. Lee, Y. H. Tai, P. T. Liu and S. M. Sze, "A distributed charge storage with GeO_2 nanodots", *Appl. Phys. Lett.*, **84**, 2581 (2004).
6. T. C. Chang, **S. T. Yan**, P. T. Liu, C. W. Chen, H. H. Wu, and S. M. Sze, "Leakage behavior of the quasi-superlattice stack for multilevel charge storage", accepted by Applied Physics Letters.

7. T. C. Chang, **S. T. Yan**, Y. T. Chen, P. T. Liu, S. M. Sze, “A Novel Distributed Charge Storage Element Fabricated by the Oxidation of Amorphous Silicon Carbide”, accepted by Electrochemical and Solid-State Letters (2004).

綜上所陳，顏君已具備國立交通大學電子研究所應有之教育及訓練水準，謹此推薦顏君參加交通大學電子研究所博士論文口試。

此致

國立交通大學電子研究所

電子研究所教授　施　敏 博士

張鼎張 博士

中 華 民 國 九 十 三 年 5 月 6 日

前瞻非揮發性記憶體元件之研究

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摘要

首先，在 SONOS 非揮發性記憶體的研究方面，本論文利用高密度電漿化學氣相沈積製作含有多能阱(trap)之載子儲存氮化矽層或其他介電質。由於高密度電漿化學氣相沈積薄膜，於沈積過程中具有較高的離子轟擊效應，導致形成的薄膜較緻密且斷鍵陷阱(trap)較多，對電子的捕獲效應較佳，期望達到較大的記憶窗，以改善記憶體元件的保存時間。高密度電漿氮化矽薄膜比傳統低壓化學氣相沉積氮化矽，具有較大的記憶窗口。由複立葉轉換紅外線光譜圖可以發現，高密度電漿氮化矽薄膜由於含有許多 N-H 鍵結作為載子捕獲的陷阱，證明其記憶窗口較大的原因。在電流-電壓特性方面，雖然高密度電漿能阱比傳統低壓化學氣相沉積氮化矽多，但漏電特性比較起來，僅大不到一個因次，另外儲存載子在高溫 150 度下的保存時間亦說明了高密度電漿氮化矽 SONOS 記憶體元件的可靠性。

此外，我們更針對傳統 ONO 結構的製程方式加以改善，例如在穿隧氧化層

上方沉積高密度電漿氮化矽薄膜，並加以高溫熱氧化，異於傳統利用低壓化學氣相沉積作為控制氧化層的直接沉積方式，使閘極堆疊介電層結構漏電極降低及崩潰電場提高，並獲得期望中具有較佳的介電特性及可靠性。

在載子儲存的介電層方面，除了 Si_3N_4 之外，以往的研究著重於 Al_2O_3，TiO_2，Ta_2O_5 等，本論文更進一步地在其它的介電材料中探索，預期找到一種適合的載子儲存單元絕緣層，例如含氧碳化矽(SiC:O)薄膜，並最佳化之。利用高密度電漿薄膜直接沉積的方式，製作二氧化矽/SiC:O/二氧化矽的三明治結構。藉由含氧碳化矽對於不同氧含量的電容-電壓特性圖及電流-電壓特性圖發現，當氧含量依序漸增時，含氧碳化矽之記憶窗口大小隨氧含量的增加而變小，另外藉由氧含量的控制，可達到較大的崩潰電壓值。我們亦提出了一個物理模型，解釋含氧量較少時，崩潰電壓較大的原因。本研究欲針對材料，製程及量測分析方面加以最佳化之。

關於含氧碳化矽作為載子儲存單元的記憶體元件方面，不同於上述利用高密度電漿化學氣相沉積的方式製作，我們亦提出了利用在穿隧氧化層上之碳化矽薄膜熱氧化的方式，使碳化矽薄膜氧化為含氧碳化矽薄膜，作為載子儲存的單元，最後覆蓋二氧化矽薄膜作為控制氧化層。在碳化矽薄膜的氧化研究方面，我們發現低溫(800 度)熱氧化比高溫(925 度)熱氧化的含氧碳化矽，具有更高的記憶窗口，亦即具有較高的載子儲存能力。利用複利葉轉換紅外線光譜儀(FTIR)等材料分析工具，我們提出了解釋具有較高記憶窗口含氧碳化矽行為的物理模型。

傳統的浮停閘快閃記憶體是利用連續的多晶矽半導體薄膜作為載子儲存的單元;SONOS 非揮發性記憶體係利用絕緣體氮化矽薄膜，作為載子儲存的單元。本論文提出了一種利用似超晶格(quasi-superlattice)結構，作為載子儲存的單元。在 2-3 奈米的穿隧氧化層上方，依序沉積氮化矽，非晶矽，氮化矽，非晶矽，各約 1-2 奈米，形成似超晶格結構，最後覆蓋氧化矽作為控制氧化層，形成非揮發性記憶體元件結構。在記憶體特性的表現上，記憶窗口有隨著寫入電壓增大而增大的趨勢，並且具有明顯的兩個起始電壓偏移抖增的現象。藉由適當的閘極電壓寫入，此元件具有每個記憶單元(memory cell)兩個位元(bit)的操作能力，只單純

由閘極利用 F-N 穿隧寫入，而不是像 SONOS 元件需利用源極與汲極雙向的寫入與讀取來定義每個記憶單元的兩個位元。本論文針對此似超晶格記憶體元件，提出了一個物理模型來解釋兩個位元的儲存，並且針對閘極堆疊結構室溫及低溫的漏電效應，做了物理性的探討。

在奈米晶體非揮發性記憶體之研究方面，首先，我們成功地利用矽化鍺薄膜熱氧化研製出包覆在氧化矽中的鍺奈米點。在穿隧氧化層上方沉積矽化鍺薄膜，爾後利用高溫乾氧化，使鍺向下析出於穿隧氧化層上方，矽氧化成二氧化矽作為控制氧化層(control oxide)，形成鍺奈米點包覆於二氧化矽中的結構。由穿透式電子顯微鏡可知鍺奈米點直徑大為 5.5 奈米，元件的記憶體特性以及可靠性也相當穩健。當上述鍺奈米點再加以過度熱氧化之後，鍺便會氧化為氧化鍺，形成氧化鍺奈米點。經由電性量測後發現，氧化鍺奈米點也確實有記憶體特性，另外經由 x-ray absorption near edge spectroscopy (XANES)也證實穿透式電子顯微鏡照片中的奈米點成分為氧化鍺，我們並且提出了一個物理模型來解釋此元件之記憶體效應。

除了半導體奈米點之外，本論文亦針對金屬奈米點做深入的研究。在金屬奈米點的製作方面，首先在穿隧氧化層上方沉積矽化鎢薄膜，並覆蓋上一層非晶矽薄膜約 8 奈米。當試片經過高溫熱氧化之後，成分矽會氧化為二氧化矽作為控制氧化層，而矽化鎢中的金屬成分鎢會傾向向下析出，成核於穿隧氧化層上方，形成鎢奈米點，作為載子儲存的單元。在氧化的過程中，氧化參數需嚴格控制，否則金屬矽化鎢可能會氧化不足仍為薄膜，或是氧化過度將金屬鎢全部氧化。關於金屬鎢奈米點記憶體元件的記憶體特性，其具有相當大的記憶窗口(memory window)可作為定義 0 或 1 的依據，另外，此元件反覆操作的忍耐度(endurance)也可以達到一百萬次以上。

Study on Advanced Nonvolatile Memory Devices

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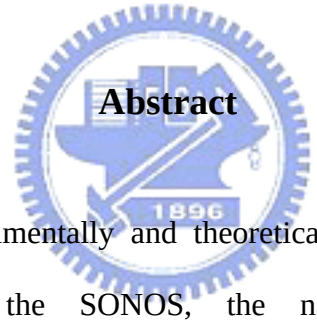

Abstract

We have studied experimentally and theoretically three types of nonvolatile semiconductor memories: the SONOS, the nanocrystal/nanodot, and the quasi-superlattice memory devices. On the study of the silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile memory technology, high density plasma chemical vapor deposition (HDPCVD) is used to fabricate trap-rich silicon nitride or other dielectrics as the charge storage element. It is observed that the densified and trap-rich silicon nitride film from HDPCVD possesses a larger memory window than that of the conventional low pressure chemical vapor deposited (LPCVD) silicon nitride. It is found from the Fourier Transform Infrared Spectrum (FTIR) that there are N-H bonds within the HDPCVD silicon nitride as the charge trapping sites, which certifies the reason of the larger memory window. The HDPCVD silicon nitride is deposited on the tunnel oxide, followed by a high temperature oxidation process. As

compared to the LPCVD deposition as the control oxide, the HDPCVD processes result in a lower leakage current and higher breakdown voltage.

In addition to silicon nitride as the storage layer, we have also studied the oxide/SiC:O/oxide sandwiched structures using HDPCVD processes. From the capacitance-voltage and current-voltage characteristics of oxygen-incorporated silicon carbide with different oxygen content, it is observed that the memory window is decreased with increasing the oxygen content. By controlling the oxygen content, a higher breakdown voltage can be achieved. A physical model is proposed to explain the higher breakdown voltage with less oxygen content of the oxygen-incorporated silicon carbide. We have also studied the thermal oxidation of SiC layer on the tunnel oxide as the charge storage layer followed by control oxide capped. In the study of the oxidation of SiC, it is found that low temperature (800 ℃) oxidized SiC shows a larger memory window than that of the high temperature (925 ℃) oxidized SiC. Using the FTIR spectroscopy, a physical model is proposed to explain the behavior of low temperature oxidized SiC with larger memory window.

On the study of the quasi-superlattice structure, we have sequentially deposited 1-2 nm silicon nitride and a-Si on a 2-3 nm tunnel oxide in two cycles to form the quasi-superlattice structure. Finally, SiO_2 is capped as the control oxide. The memory window is increased with the programming voltage. Also, two sudden rises of the threshold voltage shift are observed. By suitably operated gate voltage, this memory device shows the capability of the operation of 2-bit per cell. The 2 bits can be operated and defined by F-N tunneling rather than the source/drain bidirectional programming and reading of the conventional SONOS memory devices. A physical model is proposed to explain the 2-bit storage and the investigation of room and low temperature leakage behavior of the gate stack is also considered.

On the study of nanocrystal nonvolatile memory devices, we have successfully fabricated germanium nanocrystals embedded in silicon dioxide by the thermal oxidation of SiGe. SiGe layer is deposited on the tunnel oxide, followed by high

temperature thermal oxidation. The Ge element of the SiGe layer is downward segregated and precipitated on the tunnel oxide and the Si element is oxidized into silicon dioxide as the control oxide. From the analyses of the TEM micrograph, it is observed that the size of the Ge nanocrystals is around 5.5 nm. The memory effects and the reliability of the memory are characterized robust. As the germanium nanodots are over-oxidized, the germanium nanodots are oxidized into germanium oxide dots. It is found that the germanium oxide exhibits an apparent memory effects. Also, the x-ray absorption near edge spectroscopy (XANES) analysis certifies the composition of the GeO_2 nanodots in the TEM micrograph. A physical model is proposed to demonstrate the memory effects of the GeO_2 memory device.

In addition to semiconductor nanocrystals, metal nanodots are investigated. On the aspect of the fabrication of metal nanodots, tungsten nanodots are firstly demonstrated. The tungsten silicide layer is physically deposited on the tunnel oxide and an amorphous Si layer is capped on the silicide layer. As the sample is high temperature thermally oxidized, the silicon element is oxidized into silicon dioxide as the control oxide and the tungsten element tends to segregate downward and precipitate on the tunnel oxide. During the oxidation process, the parameters of the oxidation need to be well control or the tungsten silicide will be under-oxidized or over-oxidized. The tungsten nanocrystal memory device shows a large memory window to be defined as “1” or “0”. Also, the endurance characteristics of the memory device achieve 10^6 write/erase cycles which show the robustness of the memory device.

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執筆至此，表示論文寫作已告一段落，在寫作的過程中，一直在思索該如何寫致謝這一部分，偏偏到了現在開始動筆了，卻不知道如何用文字表達我的感謝之意。我一直覺得生命中充滿貴人，來到交大之後，師承的兩位師長也就是我的貴人。施敏教授給學生很自由的發揮空間，言談之中處處充滿啟發，讓我在做研究時，找到方向，更常藉著一些小故事，鼓勵我應該更努力；在待人處世上，施教授的風格業已成為學生心目中的人生導師。張鼎張教授對於我的研究方面的指導更是不遺餘力，不僅積極激發學生的創意，對於學生研究上的困難，張教授也非常用心協助學生解決問題。此外，張教授亦會親切的融入學生的生活，關心學生，與學生一同歡樂。在兩位老師的師門之下，那種充滿歡笑聲的環境與氣氛，是會令我終身難忘的。所謂「一日為師，終身為父」，對兩位老師的感激之情，竟像八月的桂花香一般，濃郁芬芳，久久無法散去。

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2004 年 盛夏

碩廷

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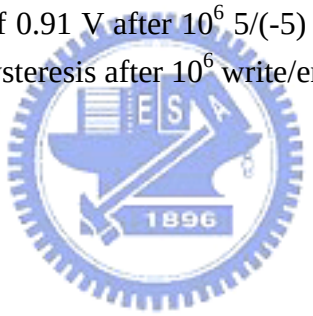

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Chapter 1

Introduction

1.1 General Background

In 1960's, due to the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1.1]. To date, the stacked-gate FG device structure, as shown in Fig. 1-1, continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a huge industry of portable electronic systems. The most widespread memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector "flash" erase.

Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. On the one hand, the tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. Once the tunnel oxide has been created a leaky path, all the stored charge in the floating gate

will be lost. When the tunnel oxide is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, there is a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry [1.2].

To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned, SONOS [1.3-1.5] and nanocrystal nonvolatile memory devices [1.6-1.8]. As for SONOS in Fig. 1-2, the nitride layer is used as the charge-trapping element. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory [1.5]. Tiwari et al. [1.6] for the first time demonstrated the Si nanocrystal floating gate memory device in the early nineties. As shown in Fig. 1-3, the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. Also, the nanocrystal memory device can maintain good retention characteristics when tunnel oxide is thinner and lower the power consumption [1.6-1.8].

1.1.1 SONOS nonvolatile memory devices

From mobile computer to wireless applications, silicon-oxide-nitride-oxide-silicon (SONOS) nonvolatile semiconductor memories (NVSMs) meet the memory challenges of a small-scale world. In general, NVSMs are required to withstand up to 10-100 K program/erase cycles (endurance) with 10-year memory retention at temperatures as high as 125 ℃. The term “endurance” refers to the ability of the NVSM to withstand repeated program cycles and still meet the specification in the

data sheet. The term “retention” describes the ability of the NVSM to store and recover information after a number of program cycles at a specified temperature. In applications where radiation hardness is an important issue, the technology requires radiation-hardened field dielectric processes to minimize the build-up of radiation-induced parasitic leakage. Advancements in ultra-thin tunnel oxides during the 1990s have opened the path to improve performance and reliability for NVSMs based on SONOS technology [1.9]. Figure 1-4 illustrates the progression of device cross section, which has led to the present SONOS device structure. The optimization of nitride and oxide films has been the main focus in recent years. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45 nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. Figure 1-5 illustrates the write/erase operation using an energy-band diagram. The electrons injected from the channel are trapped in the forbidden gap of the silicon nitride film. The electrons, which are not trapped in the nitride film, tunnel through the blocking oxide into the gate electrode. If the poly-Si gate is doped p^+, then holes may tunnel from the gate to the silicon nitride valence band, thereby compensating the trapped electrons and reducing the threshold voltage shift. During the erase operation, holes are injected from the substrate into the silicon nitride valence band where they are trapped in a manner similar to electrons. The free holes pile up at the blocking oxide interface because of the larger barrier height (5 eV). Electrons may tunnel from the gate electrode into the nitride compensating the injected holes. A larger barrier for holes (4.7 eV) requires tunnel oxides to be less than 2.5 nm for efficient tunneling and, therefore, “hole tunneling” depends strongly on the

tunnel oxide thickness. Additionally, electrons may tunnel from the valence band of the gate electrode; however, the barrier height for this process is increased by the silicon bandgap (1 eV) as compared with the tunneling from the conduction band. Thus, in summary, for SONOS device operation both carrier types are involved in the transport process.

There are a number of applications for SONOS NVSMs, with particular emphasis on “drop-in” modules for the application-specific integrated circuits (ASICs) such as wireless application, embedded NVSM in microcontrollers, and the so-called smart cards. Future smart cars in public transport schemes will be operated using RF data transmission without the need for external contacts and power supplies. SONOS NVSMs may be employed in mobile computing systems such as handheld PCs and notebook and subnotebook PCs; digital still picture cameras; smart digital phones; data acquisition systems for industry, commerce, and military; audio recorders; GPS systems for automobiles, ships, and planes; and communication equipments, including cellular base stations, PBS equipment, and digital routing switches. In addition, there are opportunities for programmable weights in adaptive signal processing and the replacement of DRAMs in dynamic memories since SONOS NVSMs have a small cell size and immunity to single event upset [1.10]. With one-transistor cell (1TC) and the isolation of the stored charge by an insulator, the SONOS device becomes a major challenge to DRAM technology.

To improve the device performance of the SONOS technology, the optimization of the ONO stack has been the main considerations currently. She *et al.* demonstrated jet vapor deposited (JVD) silicon nitride as a tunnel dielectric for flash memory device application. Compared to conventional devices with SiO_2 tunnel dielectric, faster programming speed as well as better retention time are achieved with low programming voltage [1.11]. Reisinger *et al.* [1.12] proposed a SONOS structure with

a p^+ doped silicon gate instead of the commonly used n^+ gate. In the erase mode, the p^+ gate prevents the Fowler Nordheim tunneling of electrons from the conduction band of the gate into the silicon nitride film. Eitan *et al.* [1.13] proposed a novel localized 2-bit nonvolatile memory cell named as NROM^{TM}. The two-bit operation is performed by charge storage on source- and drain-side silicon nitride layer. Programming is performed by channel hot electron injection and erased by tunneling enhanced hot hole injection. Their read methodology is very sensitive to the location of trapped charge above the source and the single device cell has a two physical bit storage capability. Currently, the 2-bit-per-cell device has become a significant impact for the nonvolatile memory industry.

In addition to the horizontal SONOS structure, Lee et al. demonstrated a multilevel vertical channel SONOS nonvolatile memory device on SOI substrate [1.14]. The vertical channel SONOS memory cell is fabricated using 0.12 μm SOI standard logic process for the next generation flash memory cell with ultra high density. With 57 nm wide vertical channel and 1.5 nm tunnel oxide, the vertical channel SONOS shows the scaling breakthrough beyond 0.10 μm flash memory and the multilevel operation with negative programming voltages. The consecutive scaling of the SONOS technology also drives the industry of flash memory approaching the high density, low power consumption, and improved data retention and endurance EEPROM's [1.15]. Differing from the storage element of silicon nitride of SONOS technology, King *et al.* proposed another charge storage element such as silicon rich oxide for dynamic or quasi-nonvolatile memory application [1.16]. Using the traps in the silicon rich oxide layer for charge storage, the symmetrical write/erase characteristics were achieved. Also, this memory cell has an erase time much shorter than the values of similar devices reported in the literatures.

Low-voltage (5-10 V) SONOS NVSMs may be scaled in cell size to $6F^2$ (F=feature

size) and perhaps even smaller in the years to come. The simplified ONO gate stack in SONOS memory transistors lends itself to the economics of scaled CMOS circuits. The compatibility of SONOS technology with advanced CMOS logic technology permits economical integration of NVSMs as embedded EEPROMs in ASIC chips. Finally, radiation hardness provides a unique and important feature for advanced military and space systems.

1.1.2 Nanocrystal nonvolatile memory devices

Storing charges on a single node (the FG node) makes the conventional memory structure particularly prone to failure of the FG isolation. One weak spot in the tunnel oxide is sufficient to create a fatal discharge path, compromising long-term nonvolatility. One way to alleviate the scaling limitation of the conventional FG device, while still preserving the fundamental operating principle of the memory, is to rely on distributed charge storage instead. Nanocrystal nonvolatile memories, first introduced in the early 1990s, are one particular implementation of that concept. In a nanocrystal NVSM device, charge is not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor.

As compared to conventional stacked gate NVSM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more

robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [1.7]. Quantum confinement effects (bandgap widening; energy quantization) can be exploited in sufficiently small nanocrystal geometries (sub-3 nm dot diameter) to further enhance the memory's performance.

There are other important advantages though. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVSM's by avoiding the fabrication complications and costs of a dual-poly process. Further, due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area (i.e., lower cost). Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the charge storage in the nanocrystal layer. There are, however, some intrinsic weaknesses as well. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, it also removes an important design parameter (the coupling ratio) typically used to optimize the performance and reliability tradeoff.

As for the fabrication processes, a first requirement is the aerial density of the nanocrystal dots. A typical target is a density of at least 10^{12} cm^{-2}. This is equivalent to approximately 100 particles controlling the channel of a memory FET with 100×100 nm^2 active area, and requires particle size of 5-6 nm and below. Second, the fabrication process should result in a planar nanocrystal layer, i.e., the thickness of the dielectric layer separating the nanocrystal and the substrate should be well controlled.

Poor control of the tunnel oxide thickness will result in wider threshold voltage distributions and will increase the number erratic bits. More generally, good process control is needed with regards to such nanocrystal features as: size and size distribution, inter-crystal interaction (lateral isolation), uniformity of aerial crystal density, and crystal doping (type and level). Finally, it is preferred that the fabrication process is simple and that it uses standard semiconductor equipments. Several nanocrystal fabrication processes have been demonstrated. Kim *et al.* [1.17] used conventional LPCVD reactor to fabricate Si nanocrystals at 620 ℃. A high density of about $5\times10^{11}/cm^2$ was obtained on nitride surface, and the density was more than three times larger than that on oxide [1.18-1.19]. Kanjilal *et al.* demonstrated a sheet of spherical, well-separated, crystalline Ge nanodots embedded in SiO_2 on top of p-(001) Si wafer, fabricated by molecular beam epitaxy (MBE) combined with rapid thermal processing and characterized structurally and electrically [1.20]. To fabricate Ge nanocrystals, the oxidation of SiGe contained films has been utilized [1.21]. As the SiGe layer is oxidized, the Ge element will be downward segregated and Si will be oxidized into SiO_2 [1.22-1.34]. Ostraat *et al.* proposed an aerosol silicon nanocrystal nonvolatile memory device with large threshold voltage shift ($>$ 3V), sub-microsecond program times, millisecond erase times, excellent endurance ($>10^5$ program/erase cycles), and long term nonvolatility ($>10^6$ sec) [1.35]. Differing from the required single planar nanocrystal layer, Ohba *et al.* proposed a novel Si dot memory whose floating gate consists of self-aligned doubly stacked Si dots. A lower Si dot exists immediately below an upper dot and lies between thin tunnel oxides. It is experimentally shown that charge retention is improved compared to the usual single layer Si dot memory. A theoretical model considering quantum confinement and Coulomb blockade in lower Si dot explains the experimental results consistently, and shows that charge retention is improved exponentially by lower dot size scaling [1.36].

Qu *et al.* presented an approach for synthesizing Ge nanocrystals embedded in amorphous silicon nitride films [1.37]. On the basis of preferential chemical bonding formation of Si-N and Ge-Ge, thin films with Ge clusters embedded in amorphous silicon nitride matrix have been prepared by plasma enhanced chemical vapor deposition (PECVD) with reactant gases of SiH_4, GeH_4, and NH_3 mixed in hydrogen plasma at 250 ℃. Park *et al.* [1.38] also utilized PECVD to form Si nanocrystals embedded in silicon nitride film. They presented the electron charging and discharging effects of the Si nanocrystals embedded in SiN_x film. Capacitance-voltage hysteresis is used to inspect the memory effects of the nanocrystal memory devices [1.39]. In addition to semiconductor nanocrystals, Liu et al. described the design principles and fabrication processes of metal nanocrystals [1.40-1.41]. The advantages of metal nanocrystals over their semiconductor counterparts include higher density of states, stronger coupling with the channel, better size scalability, and the design freedom of engineering the work functions to optimize the device characteristics. A self-assembled nanocrystal formation process by rapid thermal annealing of ultra thin metal film deposited on top of tunnel oxide is developed and integrated with NMOSFET devices. Due to the minimization of the surface energy of the metal film under rapid thermal annealing, the driving force results in a discrete layer of metal nanocrystals reside on tunnel oxide. As for the tunnel dielectric for the nanocrystal nonvolatile memory devices, Baik *et al.*, as shown in Fig. 1-6, proposed a tunnel barrier structure that is composed of silicon dioxide and amorphous carbon (a-C) to attain enhanced charge retention without degradation in the injection efficiency [1.42]. The deposition of ultra thin carbon layer as well as nanocrystal array was performed using photochemical vapor deposition (photo-CVD), because photo-CVD is known to have fine thickness controllability in nanometer scale [1.43-1.44]. The first tunnel barrier of SiO_2 is formed by oxidation at 400 ℃ under ultraviolet light irradiation

[1.45]. Additionally, high-k tunnel dielectrics were investigated for Si nanocrystal memory devices [1.46-1.48]. Results show that due to its unique band asymmetry in programming and retention mode, the use of high-k dielectric on Si channel offers lower electron barrier height at dielectric/Si interface and larger physical thickness, results in a much higher $J_{g,programming}/J_{g,retention}$ ratio than that in SiO_2 and therefore faster programming and longer retention.

The programming is considered as the electron injection from the channel under positive bias operation for an NMOSFET memory device. However, the programming and erasing mechanisms of p-channel nanocrystal memory devices were also investigated by Han *et al*. [1.49]. The comparison of retention between programmed holes and electrons shows that holes have longer retention time. As the size and size distribution of the nanocrystals have been considered, She *et al.* [1.50] made a conclusion on Ge nanocrystal memory device that nanocrystal size around 5 nm is preferred to achieve fast programming speed and longer retention time, and the size should not be scaled below that. The quantum confinement effect for Ge nanocrystals smaller than 5 nm is very significant so that the retention time is shorter and the programming time is longer.

Nanocrystal memories have been presented in the mid-nineties as a possible alternative to conventional FG NVSMs devices, by allowing a further decrease in the tunnel oxide thickness. In particular, nanocrystal memories promise to enable a further scaling of the tunnel oxide, by relying on Coulomb blockade effects in small semiconductor geometries and on the enhanced robustness and fault-tolerance of distributed charge storage. Research in this area has focused on the development of nanocrystal materials and fabrication processes, and on the integration of nanocrystal-based storage layers in actual memory devices. Promising device results have been presented, demonstrating low-voltage operation for comparable threshold

voltage windows and operating speeds, and thin tunnel oxide retention behavior that suggests meeting long-term nonvolatility requirements. In spite of these promising results, it is unclear whether nanocrystal memories will ever see commercialization. In order for that to happen, the uniformity of the nanocrystals needs to be improved, and the claimed benefits need to be more unambiguously substantiated.

1.2 Organization of the dissertation

This dissertation is divided into seven chapters. The contents in each chapter are described as follows.

In chapter 1, general background of SONOS nonvolatile memory and nanocrystal nonvolatile memory devices is introduced.

In chapter 2, the study on SONOS nonvolatile memory technology using high-density plasma chemical vapor deposited silicon nitride is investigated. In addition, a new method of fabricating superior oxide/nitride/oxide gate stack is also demonstrated in this chapter.

In chapter 3, the memory effect of oxide/SiC:O/oxide sandwiched structures is studied. Also, a novel distributed charge storage element fabricated by the oxidation of amorphous silicon carbide is also evaluated.

In chapter 4, a novel approach of fabricating germanium nanocrystals for nonvolatile memory applications is presented. Additionally, the distributed charge storage with GeO_2 nanodots is demonstrated in this chapter.

In chapter 5, the electron charging and discharging effects of tungsten nanocrystals embedded in silicon dioxide for low-power nonvolatile memory technology are demonstrated.

In chapter 6, the Quasi-Superlattice Storage (QS^2): a novel concept of multilevel charge storage is presented. Also, the leakage behavior of the quasi-superlattice stack for multilevel charge storage is studied.

Finally, the summarization of all experimental results in this dissertation and the suggestions for the future work are presented in chapter 7.

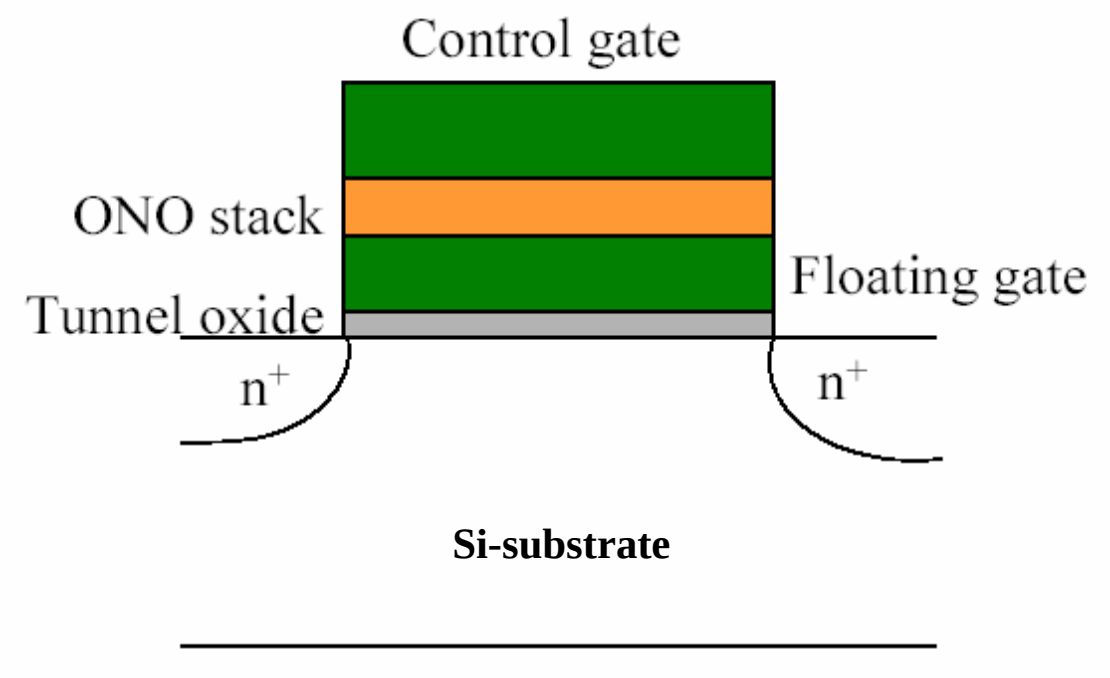

Figure 1-1 The structure of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element and ONO sandwiched structure is used as the control oxide.

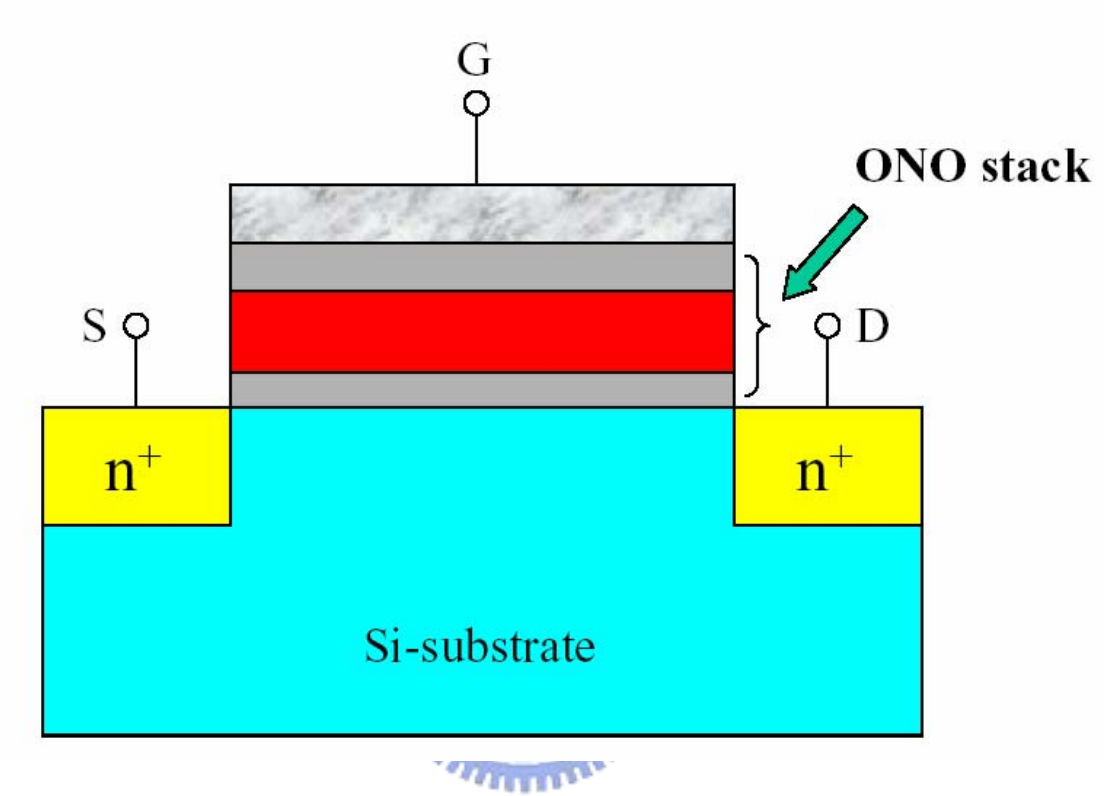

Figure 1-2 The structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge-trapping element.

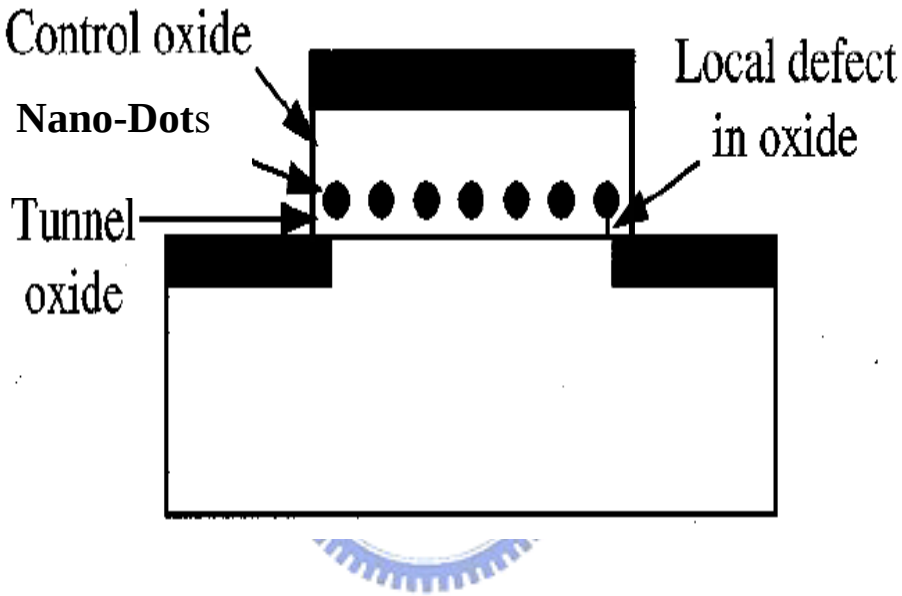

Figure 1-3 The structure of the nanocrystal nonvolatile memory device. The semiconductor nanocrystals or metal nano-dots are used as the charge storage element instead of the continuous poly-Si floating gate.

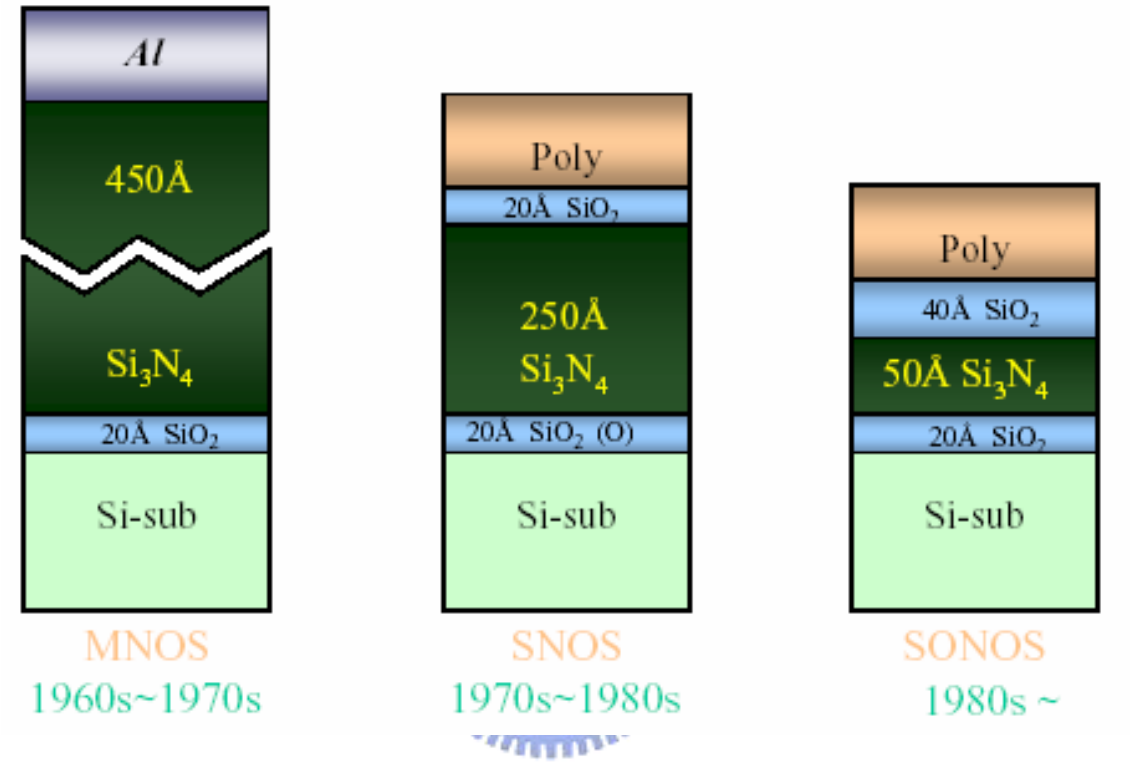

Figure 1-4 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

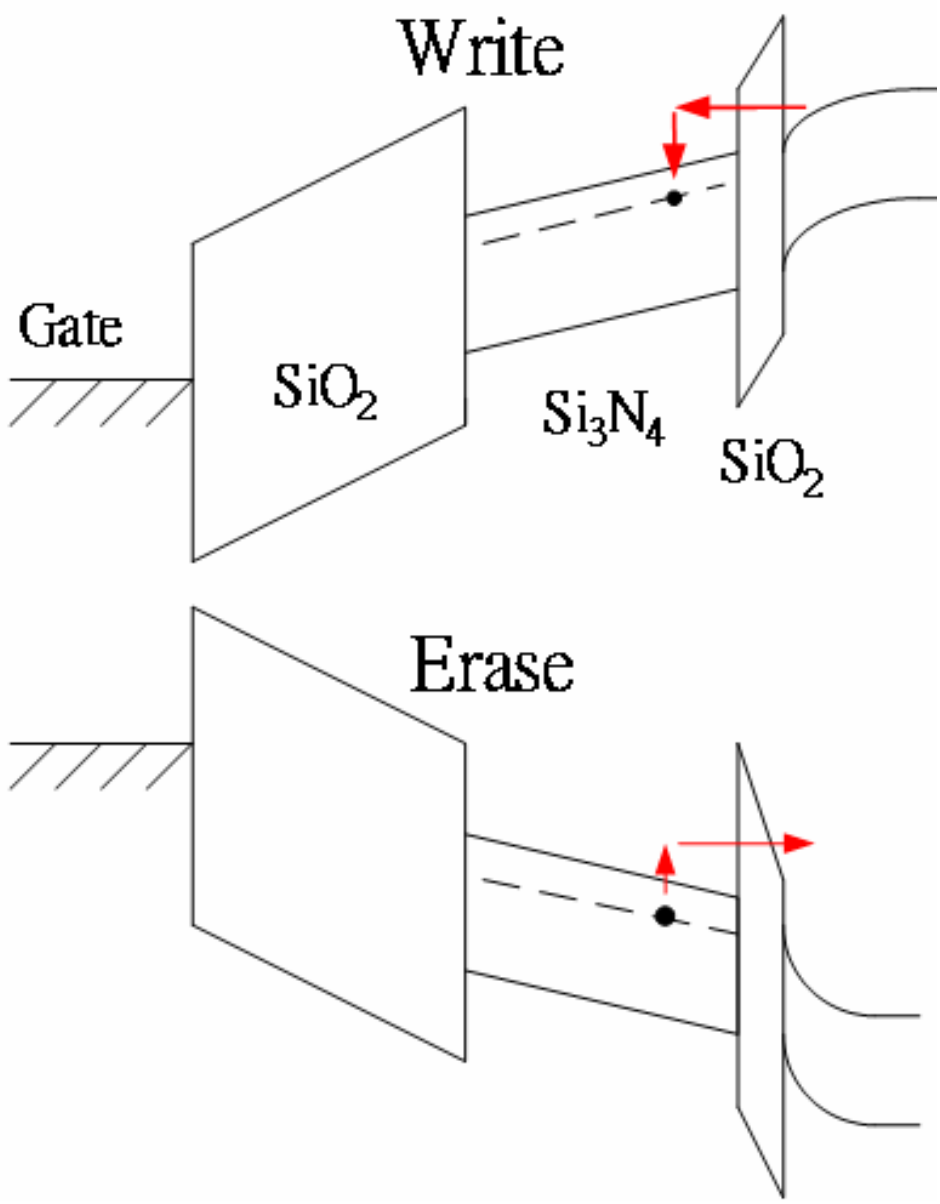

Figure 1-5 The energy band diagrams of the write/erase operation for a SONOS device.

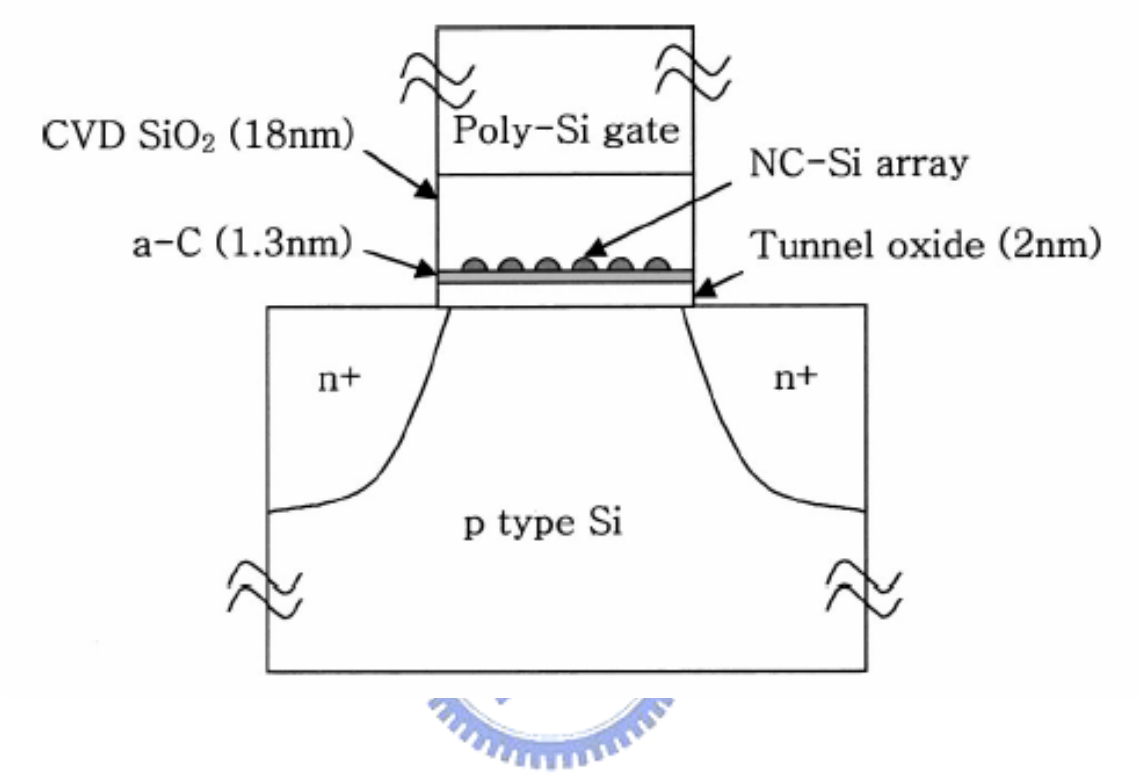

Figure 1-6 Schematic illustration of the device structure. Indicated structure dimensions are obtained by transmission electron microscopy and spectroscopic ellipsometry measurement. 18 nm layer of SiO_2 was deposited at 470 °C by low pressure chemical vapor deposition.

Chapter 2

Study on SONOS Nonvolatile Memory Technology Using High-Density Plasma Chemical Vapor Deposited Silicon Nitride

2.1 Motivation

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [2.1]. In the electrically-erasable-programmable-read-only-memory (EEPROM) semiconductor device area, there are essentially two dominant technologies which compete for an ever-expanding world market: (1) floating gate EEPROM's and (2) SONOS (historically MNOS) or floating-trap EEPROM's. The triple-dielectric SONOS structure (poly-Si gate/blocking oxide/silicon nitride/tunnel oxide/silicon substrate) is an attractive candidate for high density EEPROM's suitable for semiconductor disks and a replacement for high-density DRAMs [2.2]. An advantage of the SONOS device over the floating-gate device is its improved endurance, since a single defect will not cause the discharge of the memory [2.3]. However, the SONOS memories hardly reach a data retention for 10 years. This is why the actual use of SONOS memories is limited to military applications needing high radiation hardness [2.4]. When a memory device with a larger memory window is compared with a smaller one, it is easier to meet the requirement of retention of 10 years. This feature means that a memory device with a larger memory window will still possess an obvious difference of the threshold voltage (ΔV_t) higher than the

detecting limit of a typical sense amplifier while the memory device with a smaller memory window may lose its window in 10 years. A premise for this attention is that the leakage behavior of the memory device should be well tolerable. In this letter, for the purpose of providing a larger memory window to improve the data retention, we introduce the high-density plasma chemical vapor deposition (HDPCVD) silicon nitride to replace the conventional low pressure chemical vapor deposition (LPCVD) silicon nitride of the SONOS structure. A significant threshold-voltage shift due to the charge trapping in the HDPCVD SiN_x is observed with low leakage current of the ONO gate stack.

2.2 Experimental procedures

The ONO gate-stacked structure in this study is shown in the inset of Fig. 2-1(a). First, a 2-nm thermal oxide was grown on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide. Subsequently, a 15-nm HDPCVD silicon nitride was deposited on the tunnel oxide as a charge-trapping layer, followed by the deposition of a 20-nm HDPCVD silicon dioxide as the blocking oxide. The deposition of the HDPCVD silicon nitride was kept at 200 ℃ in a low pressure of 3 mTorr with SiH_4 : NH_3 = 12 sccm : 24 sccm and an inductively coupled plasma (ICP) power of 900 W. The low pressure of 3 mTorr during deposition makes the path length an electron travels without undergoing a collision with a gas atom (or mean free path) increased, which will improve the uniformity of the thin film [2.5]. The blocking oxide was deposited at 350 ℃ with SiH_4 : N_2O = 6 sccm : 150 sccm and a 900-W ICP power. Also, the conventional LPCVD silicon nitride ONO gate stack was fabricated as a comparison. The deposition of the LPCVD silicon nitride was kept at 780 ℃ in a 350-mTorr quartz

furnace with SiH_2Cl_2 : NH_3 = 30 sccm : 130 sccm. Finally, the Al gate was patterned and sintered to form a metal/oxide/nitride/oxide/silicon (MONOS) structure.

2.3 Results and discussions

The nitride layer of a SONOS memory device is utilized to capture the injecting carriers from the channel, which cause a variation of the threshold voltage of the memory device. Figure 2-1(a) shows the band diagrams of the “write” and “erase” operation of the MONOS structure with different gate polarities. When the device is written, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the nitride layer. When the device is erased, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the nitride layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. Figure 2-1(b) exhibits the capacitance-voltage (C-V) hysteresis after the MONOS capacitor is performed by bidirectional sweeping from 12 V ~ (-12) V and in reverse. It is clearly shown in Fig. 2-1(b) that the threshold-voltage shift (memory window, ΔV_t) of the MONOS structure of the HDPCVD SiN_x is prominent. The threshold-voltage shift of the HDPCVD SiN_x ONO stack, 5.3 V, is considerably larger than that of the LPCVD Si_3N_4 ONO stack, 3.2 V, after the 12-V write operation. To lower the operating voltage, the thickness of the nitride and blocking oxide layers should be reduced at the expense of decreasing the memory window. Although the threshold-voltage shift may be lower than that depicted above, a typical sense amplifier is designed to detect the threshold-voltage differences as low as 50 mV [2.3]. With the optimization of the thickness in the gate-stacked ONO structure, the low-voltage and reliable operation, lower than 5 V, is

possible. The HDPCVD silicon nitride is produced in a high-density-plasma chamber with a 900-W ICP power. The rf ICP power is used to increase the spiral motion of the charged particle. A charged particle will gain more energy the more times it moves around the spiral and the high density plasma is, hence, produced [2.5]. During the deposition of the nitride layer, the simultaneously slight etching due to the bombardment of the high-density plasma is processed, which forms a densified and trap-rich silicon nitride layer [2.5-2.6]. On the other hand, the LPCVD silicon nitride is deposited in a high temperature furnace, which forms a well-bonded silicon nitride layer with fewer traps. In Fig. 2-2, Fourier transform infrared spectroscopy (FTIR) of the nitrides is schematically shown. A broadened peak of N-H bonding mode is obviously observed at the wavenumber of 3350 cm^{-1} in the spectrum of HDPCVD nitride rather than the LPCVD one. The hydrogenated silicon nitride is formed due to the low-temperature deposition and the hydrogen cannot be completely outgassed as the high-temperature LPCVD nitride. The trap-rich HDPCVD SiN_x, therefore, results in a larger memory window (ΔV_t) which is probable to make the retention characteristics meet the tolerance of 10 years.

The term “retention” describes the ability of the nonvolatile memory device to store and recover information after a number of program cycles at a specified temperature [2.3-2.4]. A premise for this attention is that the leakage behavior of the memory device should be well tolerable. To maintain a good retention characteristic, the leakage current of the triple-dielectric ONO structure should be taken into account. Fortunately, as shown in Fig. 2-3, due to the well-densified silicon nitride layer [2.6-2.7], the leakage current of the HDPCVD SiN_x ONO structure is slightly higher than that of the conventional LPCVD Si_3N_4 within an order of magnitude. The leakage characteristics are still within a quite superior range compared with conventional approach. This property makes the HDPCVD silicon nitride be a good

candidate to replace the conventional nitride layer for providing a larger memory window.

To test the retention characteristics of our MONOS structure, a stricter environment of 150 ℃ is prepared. In Fig. 2-4, the threshold-voltage shift is measured with different periods of time when the samples are heated at 150 ℃ [2.8-2.9]. If there is any loss of the trapped charges after the 12-V write operation at 150 ℃ as time passes by, the threshold-voltage shift will gradually decrease. The ONO stack of HDPCVD silicon nitride retains a good retention property without a significant decline of the memory window up to 15 hours the same as the conventional LPCVD silicon nitride. This demonstrates the HDPCVD silicon nitride is robust to be adopted in the SONOS EEPROM technology.

2.4 Conclusion

With the replacement of silicon nitride in the oxide/nitride/oxide (ONO) gate-stacked structure, the trap-rich HDPCVD SiN_x shows a more significant threshold-voltage shift than that of the conventional LPCVD Si_3N_4. Also, the low-temperature (200℃) deposited HDPCVD silicon nitride shows a good retention characteristic the same as the high-temperature (780℃) LPCVD Si_3N_4. With the optimization of the thickness in the gate-stacked ONO structure, the low-voltage and reliable operation, lower than 5V, is realizable.

A New Method of Fabricating Superior Oxide/Nitride/Oxide Gate Stack

To date, the mass produced nonvolatile memory devices are based on the concept of a continuous layer of floating gate [2.10]. However, it has faced the difficulties of

consecutive scaling down by the compromise between long-term nonvolatility and high operating speed [2.11]. Recently, the concept of distributed storage of charge by a nitride layer [2.12] has caught much attention. Due to the intrinsic better endurance, the absence of erratic bits, and relatively higher radiation tolerance, the silicon/oxide/nitride/oxide/silicon (SONOS) structure has emerged as the most mature nonvolatile semiconductor memory (NVSM) currently in use for space applications. The SONOS structure has a great potential of scaling the thickness of the tunnel oxide down to 1.6 nm and reducing the programming voltage below 5 volts [2.3]. Therefore, the dielectric properties of the blocking oxide, charge-trapping nitride, and tunnel oxide (ONO) gate stack are concerned. In general, the nitride layer of the SONOS structure is fabricated by LPCVD and, afterwards, the blocking oxide is *deposited* on the nitride layer also by LPCVD followed by a steam densification at 900 ℃ [2.13]. In this study, HDPCVD is utilized to deposit a trap-rich silicon nitride layer, followed by a high-temperature dry oxidation to form a *thermally grown* oxide layer on the HDP nitride layer as a blocking oxide. This new method provides a superior ONO gate stack with larger memory window and higher breakdown field compared with conventional ONO gate stack for SONOS application.

First, a 2-nm-thick thermal oxide was grown at 925 ℃ on p-type (100) Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide. Subsequently, a 6-nm silicon nitride layer was deposited by high density plasma chemical vapor deposition on the tunnel oxide as a charge-trapping layer, followed by a dry oxidation at 982 ℃ for 30 min to form a blocking oxide layer, estimated to about 4 nm, on the nitride layer. The deposition of the HDPCVD silicon nitride was kept at 350 ℃ in a low pressure of 3 mTorr with the ratio of SiH_4 : NH_3 = 12 sccm : 24 sccm and an inductively coupled plasma (ICP) power of 900 W. The low pressure of 3 mTorr during deposition makes the path

length an electron travels without undergoing a collision with a gas atom (or mean free path) increased, which will improve the uniformity of the thin film. Differing from the prevailing SONOS technology, the blocking oxide in this study was thermally grown on the nitride layer instead of depositing on that. The oxidation was performed in APCVD at 925 ℃. Before and after the fabrication of the HDP nitride and blocking oxide, Fourier transfer infrared spectroscopy (FTIR) was utilized to investigate the quality of the HDP nitride and blocking oxide stack. After the aluminum gate electrode was patterned and sintered, the electrical measurements were performed by HP 4156 and Keithley capacitance-voltage (C-V) analyzer to examine the electrical characteristics and reliability of the ONO gate stack.

Figure 2-5 exhibits the FTIR spectrum of the HDP nitride and blocking oxide stack before Al gate deposition. The absorption of sharp Si-O bonds (~1075 cm^{-1} and 1255 cm^{-1}) and Si-N bonds (~820 to 900 cm^{-1}) are clearly observed. Also, the absorption of Si-O bonds at 1255 cm^{-1} indicates the formation of a high quality film [2.14-2.15]. To study memory effects of the ONO sandwiched structure, a bidirectional voltage sweeping between 5 and (-5) V was performed. Figure 2-6 shows the C-V hysteresis after forward (from inversion to accumulation region) and reverse voltage sweeping (from accumulation to inversion region). When the sample is operated in positive polarity, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the nitride layer. When the device is negatively operated, the electrons may tunnel back to the Si substrate. The different threshold voltages can be defined as “1” or “0” for a memory device. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. In Fig. 2-6, it is also found a counterclockwise direction of the hysteresis, which implies the substrate injection of carriers rather than gate injection [2.16]. In our previous results, the

trap-rich HDPCVD nitride contributes a larger threshold voltage shift, ΔV_t, (memory window) than the conventional LPCVD nitride. Under the low-voltage operation of 5 V, ΔV_t is estimated to around 1.3 V which is sufficient to be defined as "1" or "0" for a memory device. Figure 2-7 shows the current-voltage (I-V) characteristics of the ONO gate stack. From the point of view of low-voltage operation, the leakage current at 5 V is considerably low under both positive bias (write) and negative bias (erase). The breakdown voltage of the ONO gate stack is about 12 V under negative bias. Dramatically, the ONO stack is operated under positive bias without breakdown up to 80 V. This feature shows a superior dielectric property for the ONO gate stack. The HDPCVD silicon nitride is produced in a high-density-plasma chamber with a 900-W ICP power. The rf ICP power is used to increase the spiral motion of the charged particle. A charged particle will gain more energy the more times it moves around the spiral and the high density plasma is, hence, produced. During the deposition of the nitride layer, the simultaneously slight etching due to the bombardment of the high-density plasma is processed, which forms a more densified silicon nitride layer than LPCVD nitride [2.6]. After the densified nitride layer is thermally oxidized, the thermally grown oxide/HDP nitride stack possesses a higher breakdown voltage than other deposited oxide/nitride stacks. The asymmetry of the leakage current at low electric field is currently under investigation. In addition, the reliability of the memory device was also investigated. As shown in Fig. 2-8, the endurance of the memory device retains an obvious memory window of 0.91 V after 10^6 5/(-5) V write/erase cycles. The inset exhibits the C-V hysteresis after 10^6 write/erase cycles. A typical sense amplifier can easily detect the threshold voltage shift of 0.91 V to define the "1" or "0" for a logic memory device.

In summary, a superior ONO gate stack with a large memory window and high breakdown voltage was demonstrated. HDPCVD silicon nitride is deposited on the

tunnel oxide followed by a high temperature dry oxidation to form a blocking oxide layer on the nitride layer. This ONO stack with densified nitride layer and thermally grown oxide layer on the silicon nitride exhibits a reliable and viable approach for SONOS nonvolatile memory technology.

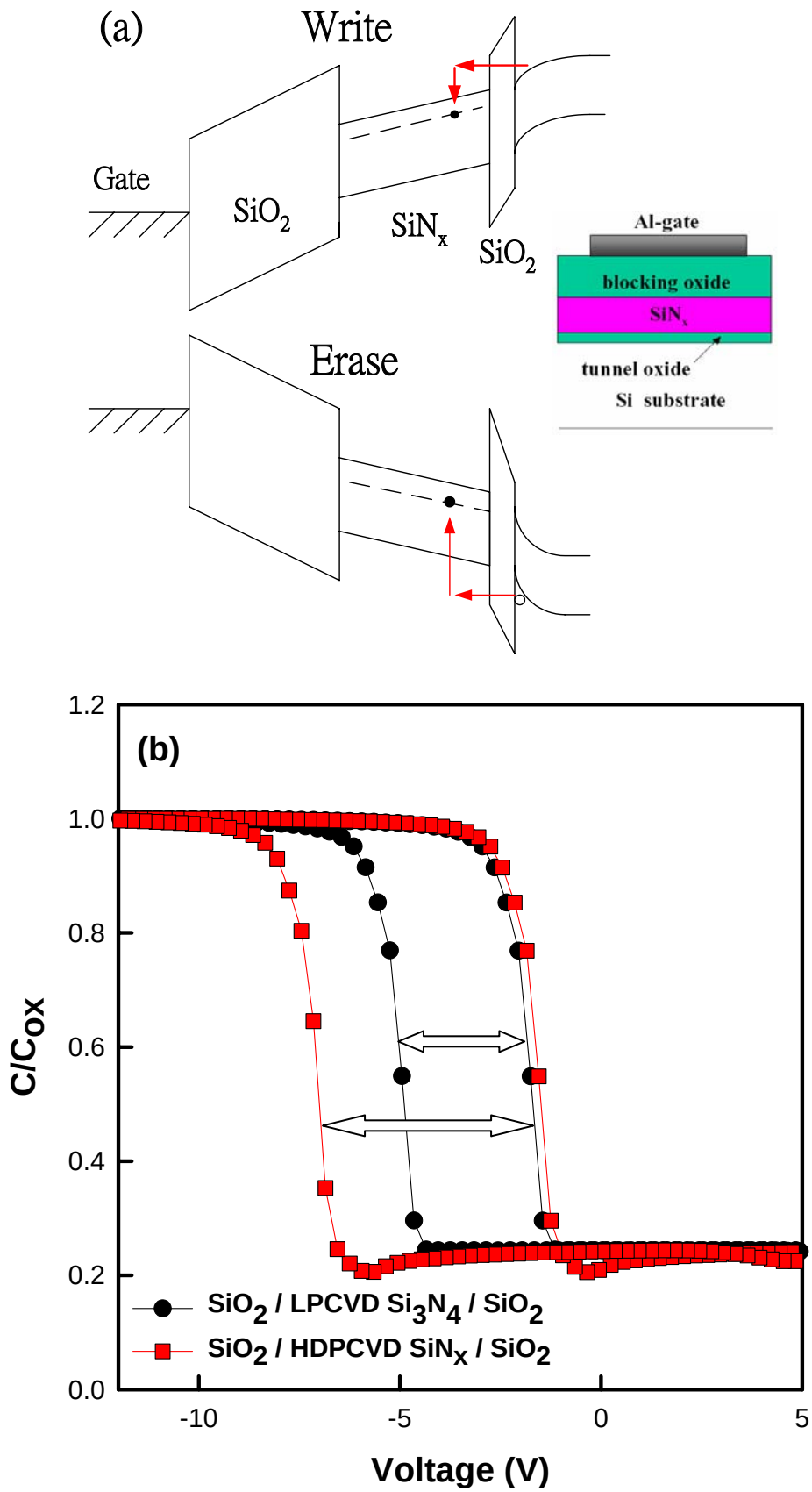

Figure 2-1 (a) The band diagrams of the write/erase operation of the MONOS structure with different gate polarities. The inset is the ONO gate-stacked structure in this study. (b) The C-V hysteresis of the capacitor is performed by sweeping from 12 V ~ (-12) V and in reverse.

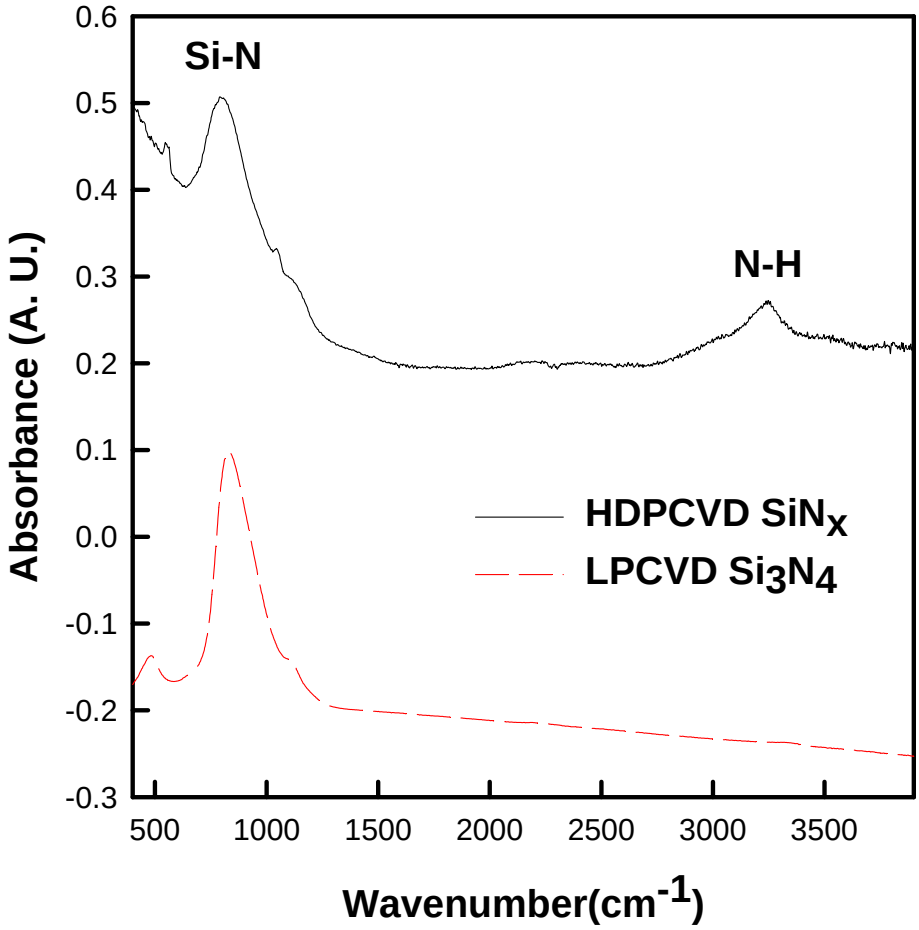

Figure 2-2 Fourier transform infrared spectroscopy (FTIR) of the HDPCVD and LPCVD nitrides.

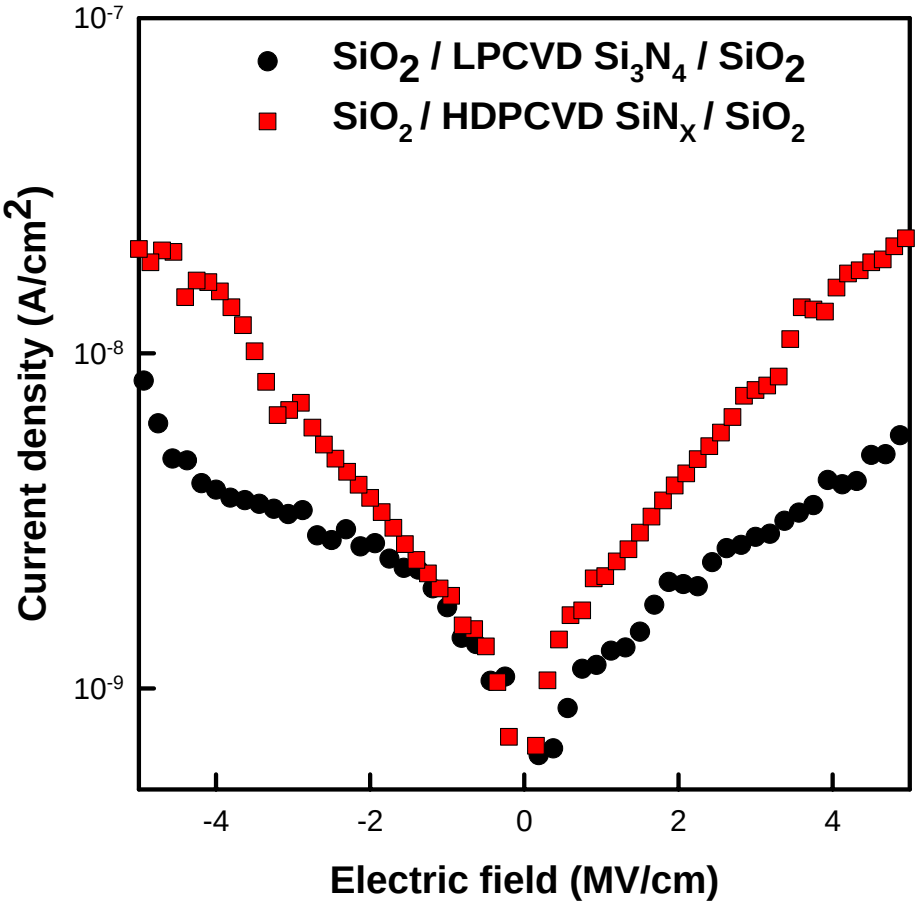

Figure 2-3 The leakage current of LPCVD and HDPCVD silicon nitride ONO gate stack. The leakage current of the HDPCVD SiN_x ONO structure is slightly higher than that of the conventional LPCVD Si_3N_4 within an order.

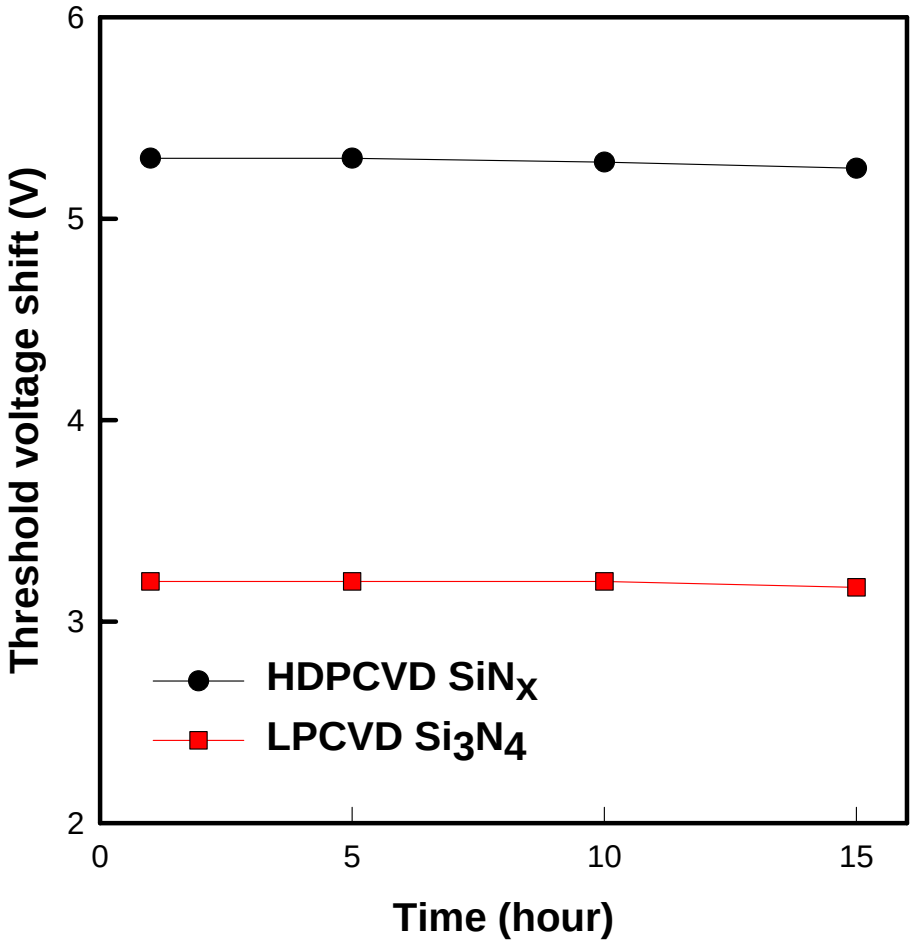

Figure 2-4 The threshold-voltage shift versus different periods of time when the samples are heated at 150 ℃.

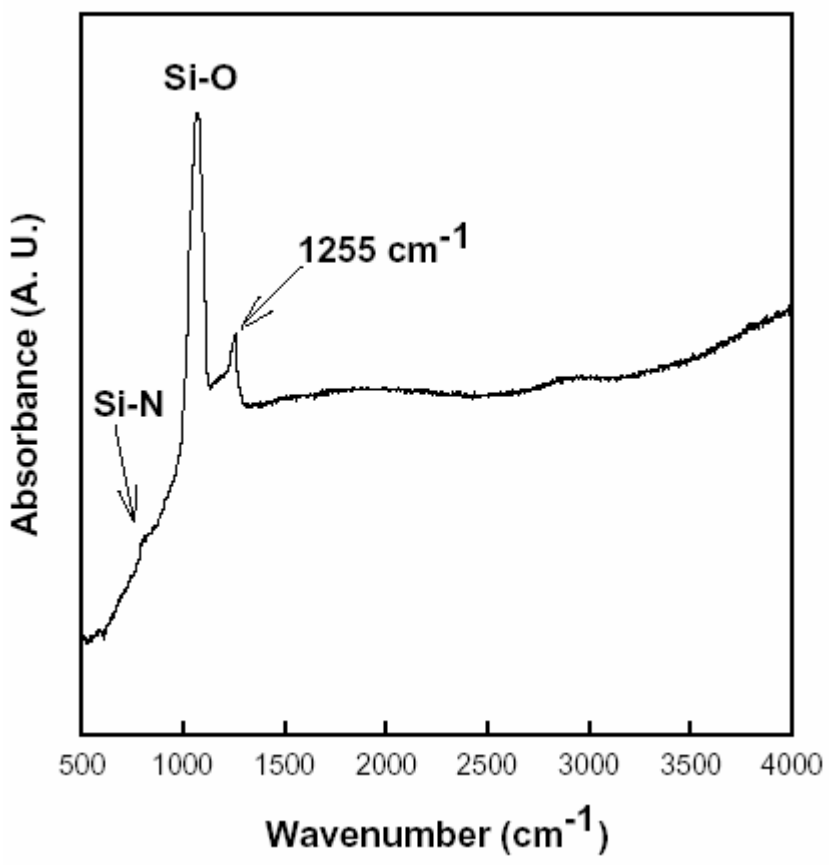

Figure 2-5 FTIR spectrum of the surface oxide layer and HDP nitride layer stack with the background spectrum of Si wafer and tunnel oxide deposited.

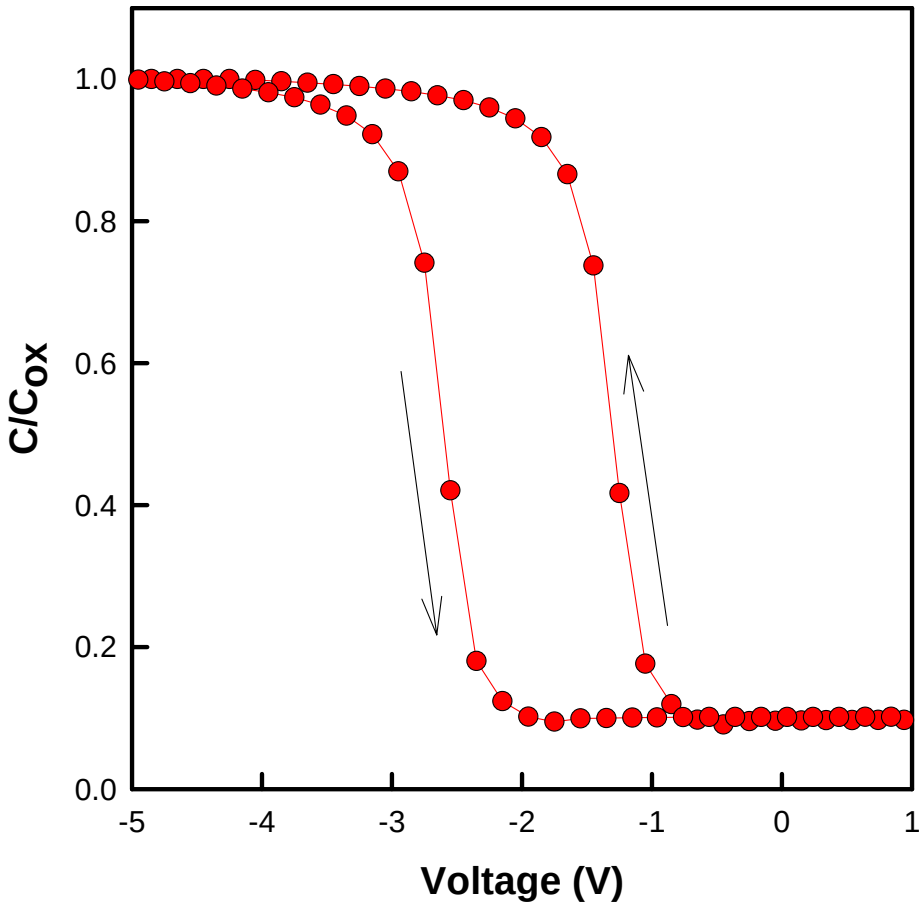

Figure 2-6 The C-V hysteresis after forward (from inversion to accumulation region) and reverse voltage sweeping (from accumulation to inversion region).

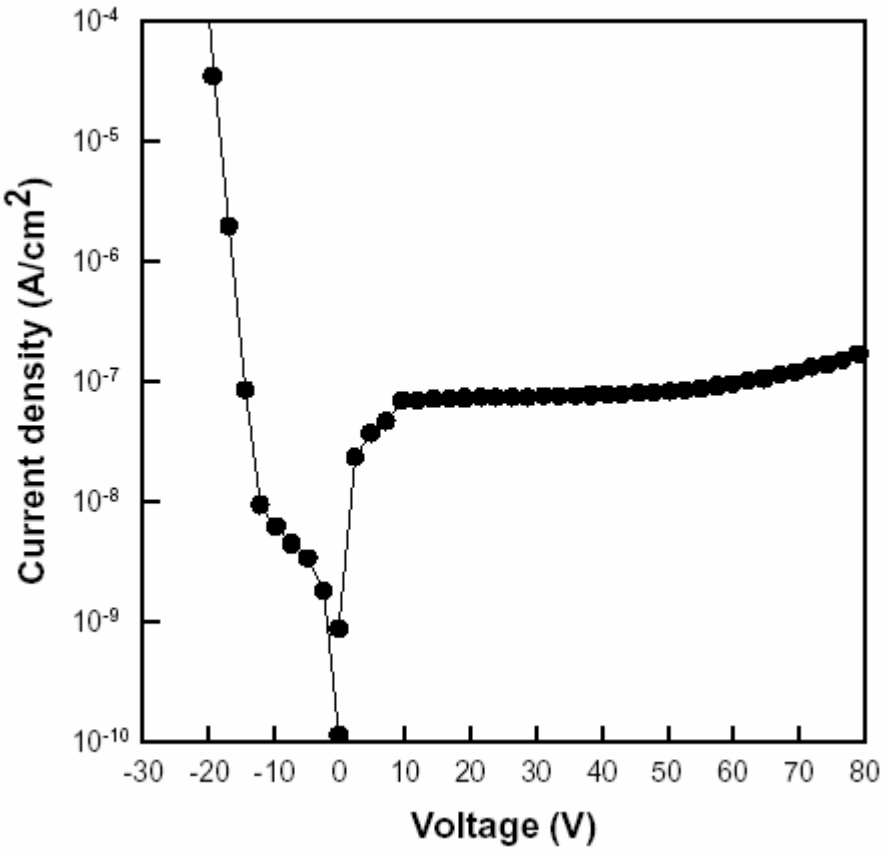

Figure 2-7 The current-voltage characteristics of the ONO gate stack.

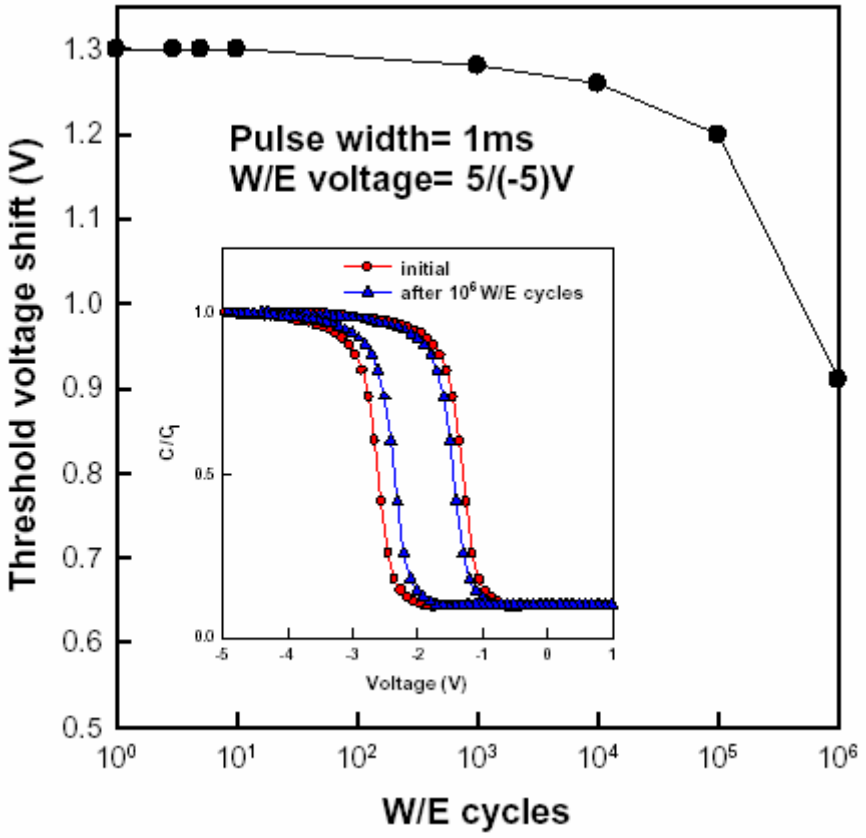

Figure 2-8 The endurance characteristics of the memory device retains an obvious memory window of 0.91 V after 10^6 5/(-5) V write/erase cycles. The inset exhibits the C-V hysteresis after 10^6 write/erase cycles.

Chapter 3

Memory Effect of Oxide/Oxygen-Incorporated Silicon Carbide/Oxide Sandwiched Structure

3.1 Motivation

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [3.1]. In the area of electrically-erasable-programmable-read-only-memory (EEPROM) semiconductor device, there are essentially two dominant technologies which compete for an ever-expanding world market: (1) floating-gate EEPROM's and (2) floating-trap SONOS, historically metal-insulator-SiO_2-Si (MIOS), EEPROM's. To date, the mass produced nonvolatile memory devices are based on the concept of a continuous layer of floating gate [3.2]. However, it has faced the difficulties of consecutive scaling down due to the compromise between long-term nonvolatility and high operating speed [3.3]. Recently, the concept of distributed storage of charge by an insulator, such as nitride layer, has caught much attention [3.4]. Among several kinds of MIOS memory devices, silicon nitride, as the charge-trapping insulator in the MIOS structure, is most widely used [3.5]. Other insulators are investigated to replace the silicon nitride film, such as titanium oxide, tantalum oxide, and aluminum oxide. However, these materials can not offer sufficient storage centers for the consideration of a large memory window. Therefore, the MIOS device has been made by metal ion

implantation (e.g., Au) into SiO_2 to form the interfacial charge-storage centers [3.6]. Also, to prevent the carriers from injecting into the charge-trapping insulating film from gate not from the channel, a blocking oxide is regularly used to cap on the insulator film, which forms an oxide/insulator/oxide sandwiched structure [3.7-3.8]. In this contribution, a novel metal-oxide-insulator-oxide-silicon (MOIOS) gate stack was investigated. The memory effects of the oxide/SiC:O/oxide sandwiched structure were demonstrated, which can be utilized as a high-performance MOIOS memory device.

3.2 Experimental procedures

Figure 3-1 shows the device structure in this study. First, a 2-nm-thick thermal oxide was grown on p-type (100) 6-in Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide layer. Subsequently, a 20-nm SiC:O layer was deposited by high density plasma chemical vapor deposition (HDPCVD) on the tunnel oxide as a charge-trapping layer, followed by the deposition of a 20-nm HDPCVD silicon dioxide as the blocking oxide. A steam densification at 982 ℃ was also performed for 180 sec to densify the blocking oxide [3.8]. The deposition of the SiC:O film was kept at 350 ℃ in a low pressure of 3 mTorr with precursors of SiH_4, CH_4 and O_2 and an inductively coupled plasma (ICP) power of 900 W. The parameters of the deposition of the SiC:O film are listed in Table 3-1. This study was divided into three samples. The deposition of SiC:O with least oxygen content (2 sccm) was defined as sample 1. From sample 1 to sample 3, the content of oxygen was increased with a decreased refractive index. The low pressure of 3 mTorr during deposition makes the path length an electron travels without undergoing a collision with a gas atom (or mean free path) increased, which

will improve the uniformity of the thin film [3.9]. The blocking oxide was deposited at 350 ℃ with the ration of SiH_4 : N_2O = 6 sccm : 150 sccm and a 900-W ICP power. Finally, the Al gate electrode was patterned and sintered to form a MOIOS structure.

3.3 Results and discussions

To study memory effects of the oxide/SiC:O/oxide sandwiched structure, a bidirectional voltage sweeping between 7 and (-7) V was performed. Figure 3-2 shows the capacitance-voltage (C-V) hysteresis in this study for different samples. It is clearly observed that as the content of oxygen is increased, the threshold voltage shift (memory window) is decreased from sample 1 to sample 3. The memory window of sample 1 is estimated to be about 1.1 V under 7-V operation. In Fig. 3-3, the band diagrams of the "write" and "erase" operation are exhibited. When the MOIOS structure is operated under positive polarity, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the SiC:O layer. When the device is negatively operated, the electrons may tunnel back to the Si substrate through tunnel oxide. The different threshold voltages before and after programming can be defined as "1" or "0" for a memory device. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. HDPCVD SiC:O is produced in a high-density-plasma chamber with a 900-W ICP power. The rf ICP power is used to increase the spiral motion of the charged particle. A charged particle will gain more energy the more times it moves around the spiral and the high density plasma is, hence, produced [3.9]. During the deposition of the carbide layer, the simultaneously slight etching due to the bombardment of the high-density plasma is processed, which forms a densified and trap-rich layer and contributes a larger

memory window than other processes to fabricate the SiC:O film [3.9-3.10].

To investigate the influence of the oxygen content on the memory window, as shown in Fig. 3-4, Fourier transform infrared spectroscopy (FTIR) was performed. Figures 3-5(a) and 3-5(b) exhibit the bonding types of Si-C and Si-H, respectively [3.11]. In Fig. 3-4 and Fig. 3-5, as the oxygen content is increased, the absorbance of Si-O bond is obviously increased and that of both Si-C and Si-H bonds is decreased. We proposed a model to describe the structural formula of the SiC:O film during deposition in Fig. 3-6. A trap-rich SiC:O film is composed of Si-O, Si-C, C-H, and Si-H bonds, and the dangling bonds, charge-trapping site, are attributed to the weak Si-H bonds which are easily broken and the C-H bonds which are not well-bound as the dotted line shown in Fig. 3-6. As the content of oxygen is increased, Si-H bonds may be easily broken by oxygen and the oxygen atoms bind with the Si dangling bonds to form the strong Si-O bonds. Also, the increased oxygen reacts with part of the Si-C and C-H bonds to form the volatile CO compound, which makes the dangling bonds decreased. It is inferred the magnitude of the memory window of the oxide/SiC:O/oxide sandwiched structure is in accordance with the amount of dangling bonds. Smaller memory window is attributed to less charge-trapping sites with more oxygen content.

Figure 3-7 shows the current-voltage characteristics of the oxide/SiC:O/oxide sandwiched structure. All the samples remain good leakage characteristics at the high voltage of 30 V. For sample 1, the breakdown voltage is up to 40 V. Also, it is clearly observed that the breakdown voltage is decreased with the increased content of oxygen. As shown in the band diagram of Fig. 3-8, when electrons are captured in a charge-trapping layer with rich charge-trapping sites [3.12], the conduction band of the charge-trapping layer will be lifted, which forms an energy barrier for conductive electrons. If more electrons are trapped in the SiC:O film, a higher barrier is generated

which results in lower leakage current and higher breakdown voltage of the gate-stacked structure. Therefore, the SiC:O film with less content of oxygen contributes to a larger memory window and a higher breakdown voltage, demonstrating the reliable characteristics as a candidate for the use of future MOIOS nonvolatile memory devices.

3.4 Conclusion

The memory effects of the oxide/oxygen-incorporated silicon carbide (SiC:O)/oxide sandwiched structure were investigated. The memory window is decreased with the increasing of the oxygen content in the SiC:O film due to the reduction of dangling bonds. A concise model is proposed to explain the reduction of dangling bonds with increasing oxygen content. Also, a higher breakdown voltage is observed with less oxygen content in the SiC:O film, which is attributed to the high barrier height induced by electron trapping in the SiC:O film.

A Novel Distributed Charge Storage Element Fabricated by the Oxidation of Amorphous Silicon Carbide

In the past few years, the portable electronic devices, such as mp3 players, digital cameras, laptops, and smart IC cards, significantly impact the markets of consumer electronic products. All of the commercially available portable electronic devices are constructed by the Flash memory devices which are mostly based on the structure of the continuous floating gate (FG). Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer [3.13-3.15]. To overcome the

scaling limits of the conventional FG structure, the SONOS (historically MNOS) or floating-trap structure has received much attention. The triple-dielectric SONOS structure (poly-Si gate/blocking oxide/silicon nitride/tunnel oxide/silicon substrate) is an attractive candidate for high density EEPROM's suitable for semiconductor disks and a replacement for high-density DRAMs. An advantage of the SONOS device over the floating-gate device is its improved endurance, since a single defect will not cause the discharge of the memory due to the distributed charge storage [3.16]. The charge storage element of the SONOS structure is an insulating layer of silicon nitride with many intrinsic traps. Recently, different charge storage elements instead of silicon nitride have been studied to achieve the robust distributed charge storage [3.17-3.19]. In this contribution, the oxygen-incorporated silicon carbide (SiCO) was investigated to be a novel distributed charge storage element. Different from well-bonded SiO_2, carbon-incorporated SiO_2 is deduced to show a charge storage effect. The charge-trapping layer of SiCO, fabricated by the oxidation of amorphous silicon carbide, exhibits obvious charge-trapping memory effects under electrical measurements. Also, material analyses such as Fourier transform infrared spectroscopy (FTIR) and transmission electron microscopy (TEM) were utilized to determine the composition and structure of the SiCO film.

Figure 3-9 exhibits the process flow in this work. First, a 5-nm-thick thermal oxide was grown as the tunnel oxide on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 16-nm amorphous silicon carbide layer was deposited by high-density plasma chemical vapor deposition (HDPCVD) on the tunnel oxide, followed by the dry oxidation at 925 ℃ or 800 ℃. The oxidation process was performed to fabricate the oxygen-incorporated SiCO and investigate the influence of different oxidation temperatures. The 7-nm-thick blocking oxide was capped by tetraethyl orthosilicate

(TEOS) oxide at 695 ℃. Afterward, a steam densification at 978 ℃ was also performed for 180 sec to densify the blocking oxide. The deposition of the SiC film was kept at 350 ℃ in a low pressure of 3 mTorr with precursors of SiH_4 (5 sccm), CH_4 (15 sccm), and He (10 sccm) and an inductively coupled plasma (ICP) power of 900 W. The low pressure of 3 mTorr during deposition makes the path length an electron travels without undergoing a collision with a gas atom (or mean free path) increased, which will improve the uniformity of the thin film. Finally, the Al gate was patterned and sintered to form a metal-oxide-insulator-oxide-silicon (MOIOS) structure with the charge trapping insulator of SiCO.

Figure 3-10 shows the TEM micrograph of the SiCO stack. The oxidized SiCO film shows a slightly dark contrast with the underlying tunnel oxide (SiO_2). The thickness of the SiCO film is estimated to be around 22.5 nm which is sandwiched between the thermally grown tunnel oxide and deposited control oxide. The SiCO layer of a MOIOS memory device is utilized to capture the injecting carriers from the channel, which cause a variation of the threshold voltage of the memory device. Figure 3-11 shows the capacitance-voltage (C-V) hysteresis of the MOIOS structure. The electrical C-V measurements are performed by bidirectional voltage sweeping from 5 V ~ (-7) V and (-7) V ~ 5 V. It is clearly shown in Fig. 3-11 that the threshold-voltage shift (memory window, ΔV_t) of the MOIOS structure is prominent for both 925 ℃ and 800 ℃ oxidation. When the device is written, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the forbidden gap of the SiCO layer. When the device is erased, the holes may tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the SiCO layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. The threshold-voltage shifts of the SiCO stack after the 5-V write operation are 0.9 V and 1.5 V for the

oxidation temperature of 925 ℃ and 800 ℃, respectively. The SiCO stack with low temperature oxidation process shows a larger memory window than that of the high temperature oxidation. A large memory window is preferred for a memory device to define “0” and “1” in the logic circuit. The larger threshold voltage shift of the low temperature oxidized SiCO stack is attributed to more charge-trapping sites in the SiCO film. When electrons are captured in the charge-trapping sites of the SiCO film, they will contribute a larger threshold voltage shift for a memory device.

In Fig. 3-12, FTIR spectra of the SiCO stack with different oxidation temperatures are schematically shown. Figure 3-12(a) shows the spectra of the Si-O bonds. The high temperature oxidized SiCO stack shows a higher absorbance of the Si-O bonds. Under the high temperature oxidation process, the SiC layer is oxidized drastically which forms an oxygen-rich SiCO film. In Fig. 3-12(b), the spectra of Si-C bonds show that under the condition of low temperature oxidation, the SiCO stack retains more Si-C bonding types with a larger area of the FTIR spectrum of the Si-C absorbance. It is well known that the fully oxidized high quality silicon dioxide (SiO_2) contains no charge-trapping sites which will not exhibit a memory window under bidirectional C-V sweeping. Since there are non-well-bonded dangling bonds or defects exist in the bulk of the SiCO film as those of the interface, the electrons trapped in the SiCO film can be trapped both in the bulk and the interface between SiCO and SiO_2. However, the electrons trapped near the channel influence the threshold voltage more significantly than those far from the channel. For the high temperature oxidized SiCO stack, the charge-trapping sites are decreased due to the reduction of dangling bonds and the increase of well-formed Si-O bonds. The oxygen-rich SiCO stack contributes a smaller memory window which is consistent with our previous results of directly deposited SiCO films [3.20]. The low temperature oxidized SiCO stack, therefore, contributes a larger memory window and

saves the thermal budget for the distributed charge storage nonvolatile memory device. The reliability issue of the MOIOS memory device is currently under investigation to promote the SiCO-based nonvolatile memory as a candidate of the distributed charge storage memory device.

In summary, a novel distributed charge storage element fabricated by the oxidation of amorphous silicon carbide is proposed in this work. For low temperature oxidation processes, the oxidized SiCO gate stack shows larger memory window due to the retainable dangling bonds with more Si-C bonding types and less Si-O bonds. Under 5-V write operation of the low temperature oxidized SiCO stack, a 1.5-V threshold voltage shift is exhibited which is sufficient for a memory device to define “0” and “1”. Also, the low temperature oxidation process of the SiCO layer saves the thermal budget for the manufacturing processes of nonvolatile memory devices.

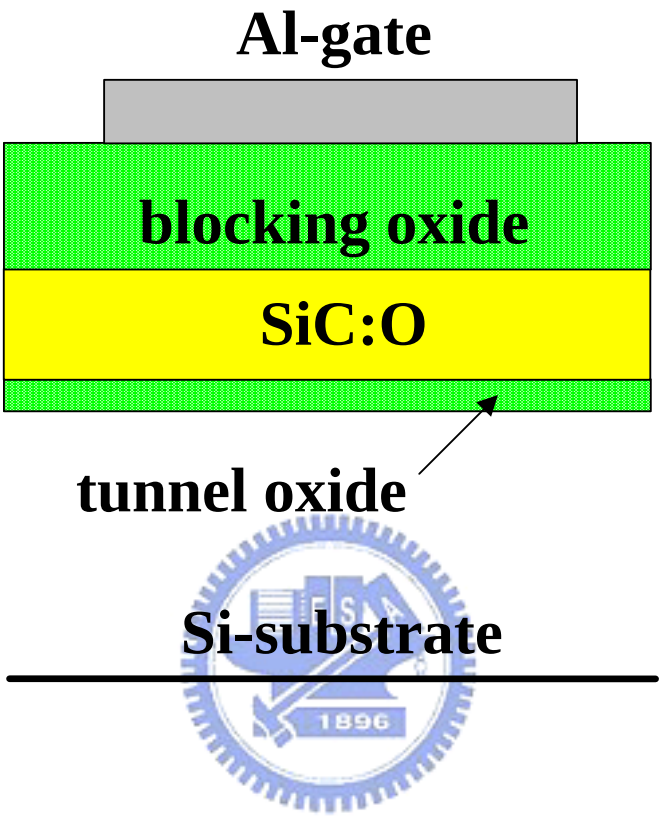

Figure 3-1 The structure of the MOIOS device shown in this work.

	SiH_4 (sccm)	CH_4 (sccm)	O_2 (sccm)	Refractive index
Sample 1	12	12	2	1.669
Sample 2	12	12	5	1.592
Sample 3	12	12	8	1.483

Table 3-1 The parameters of the deposition of the SiC:O films.

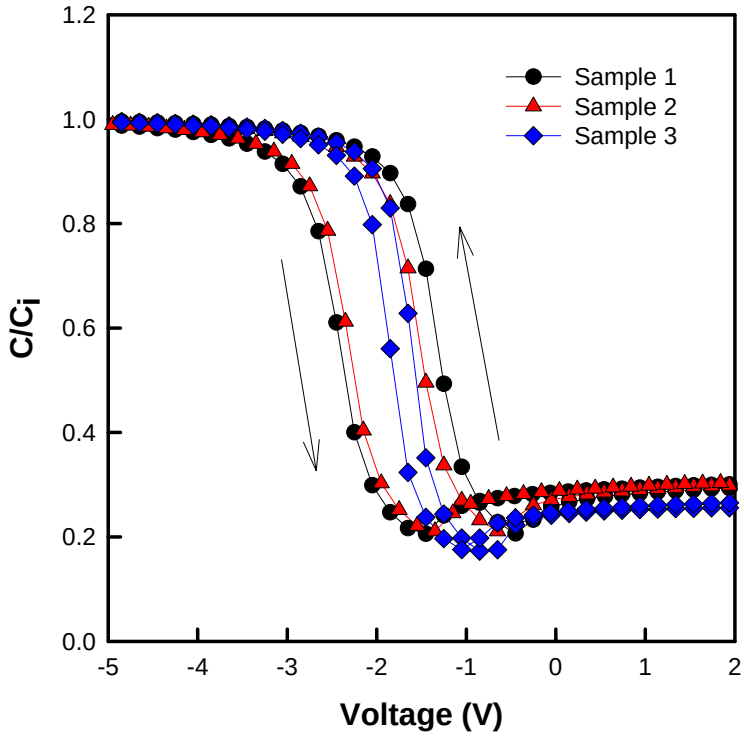

Figure 3-2 The C-V hysteresis for different samples under 7 and (-7) V bidirectional voltage sweeping.

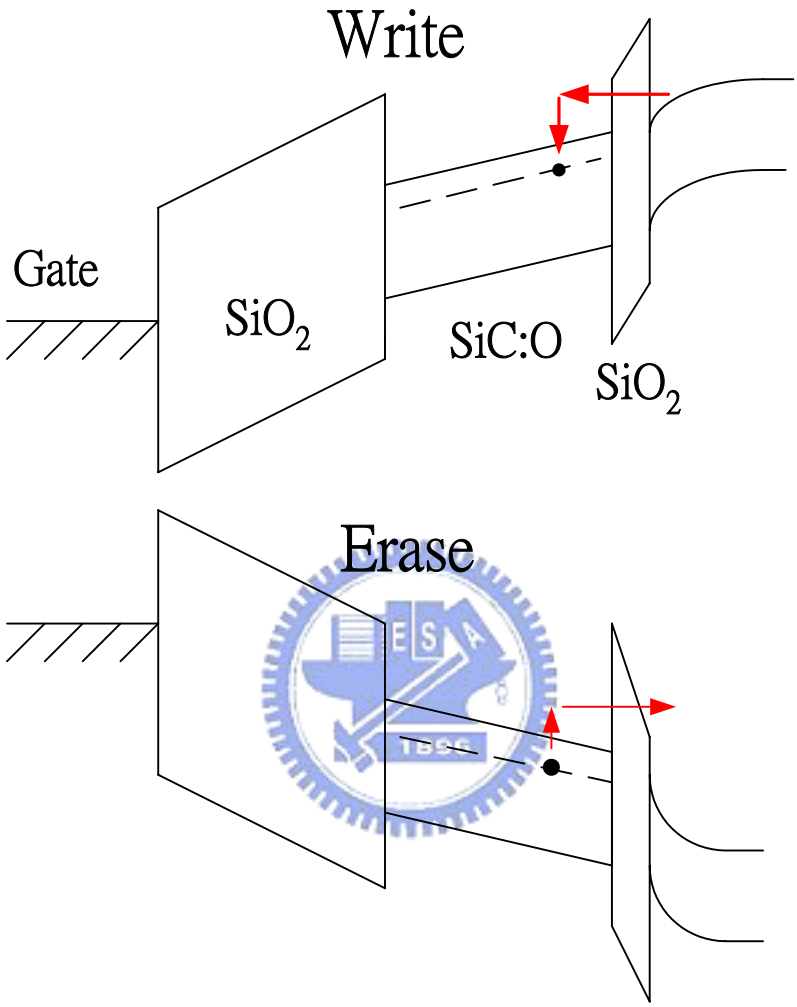

Figure 3-3 The band diagrams of the “write” and “erase” operation.

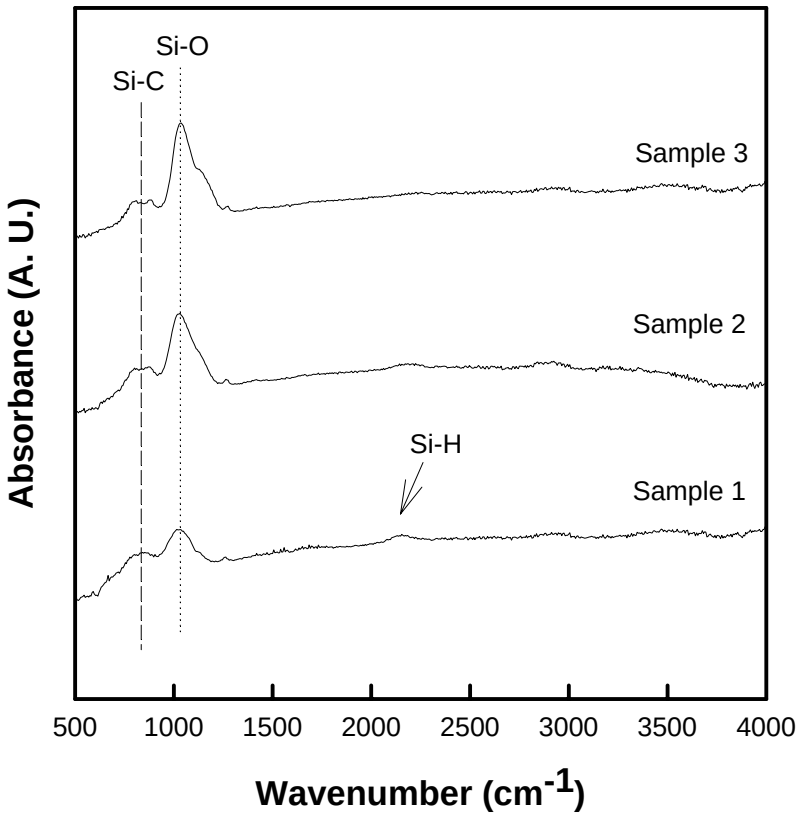

Figure 3-4 FTIR spectrum of the deposited SiC:O film.

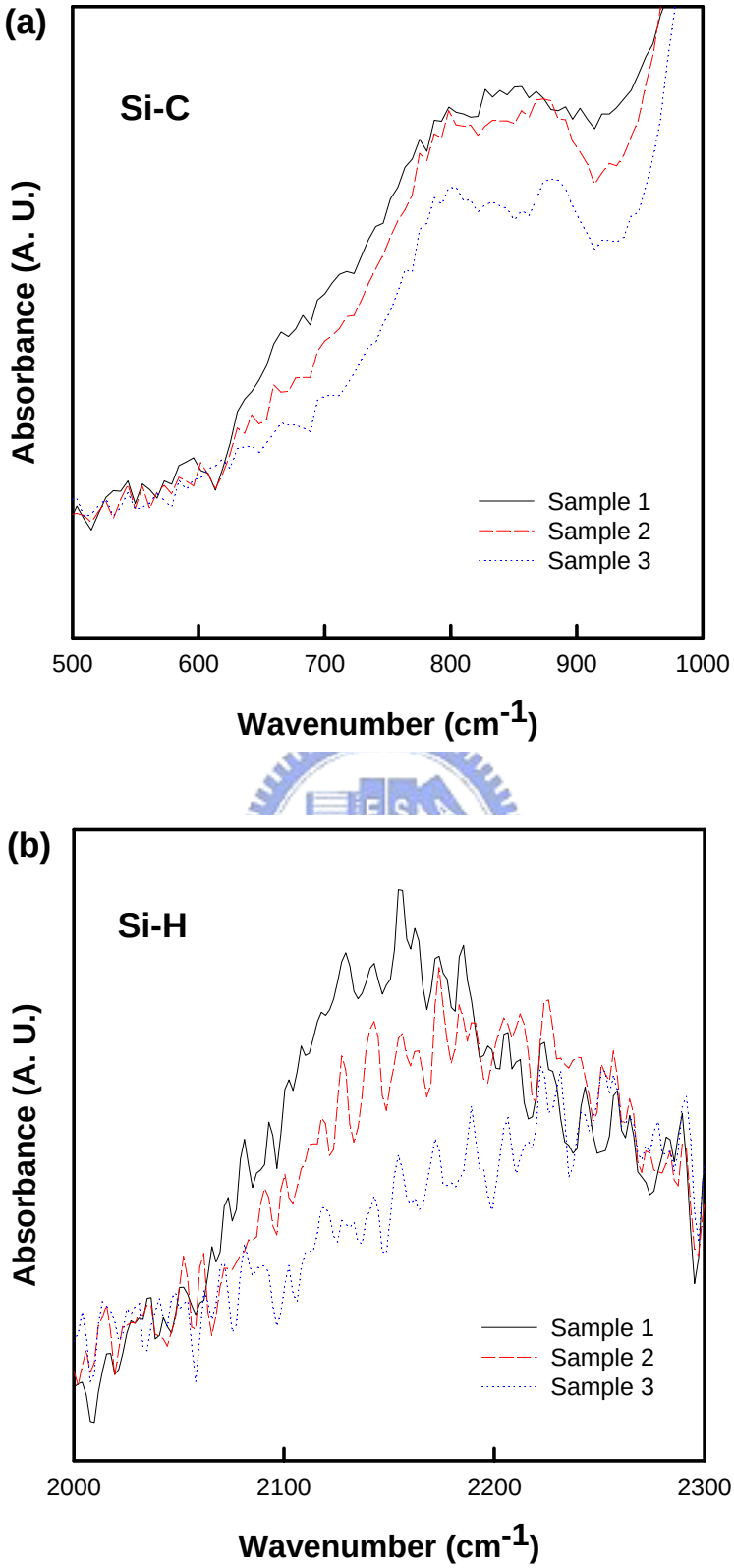

Figure 3-5 (a) The FTIR absorbance of Si-C bonds and (b) FTIR absorbance of Si-H bonds.

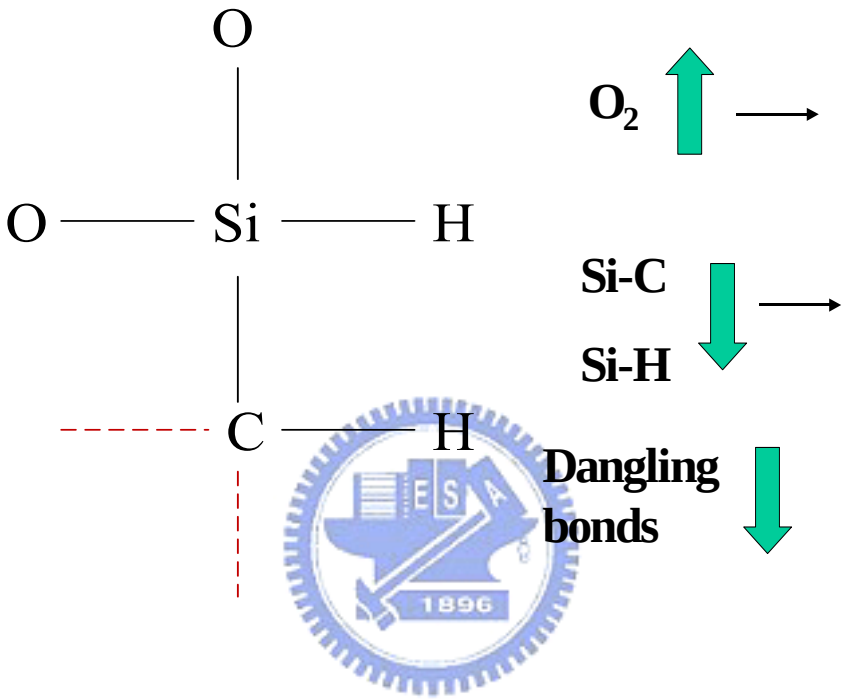

Figure 3-6 The structural formula of the proposed model. As the oxygen content is increased, both Si-C and Si-H bonds may be decreased, which renders the decrease of the dangling bonds. The dotted lines indicate the dangling bonds of the C-H bonds which are not well-bound.

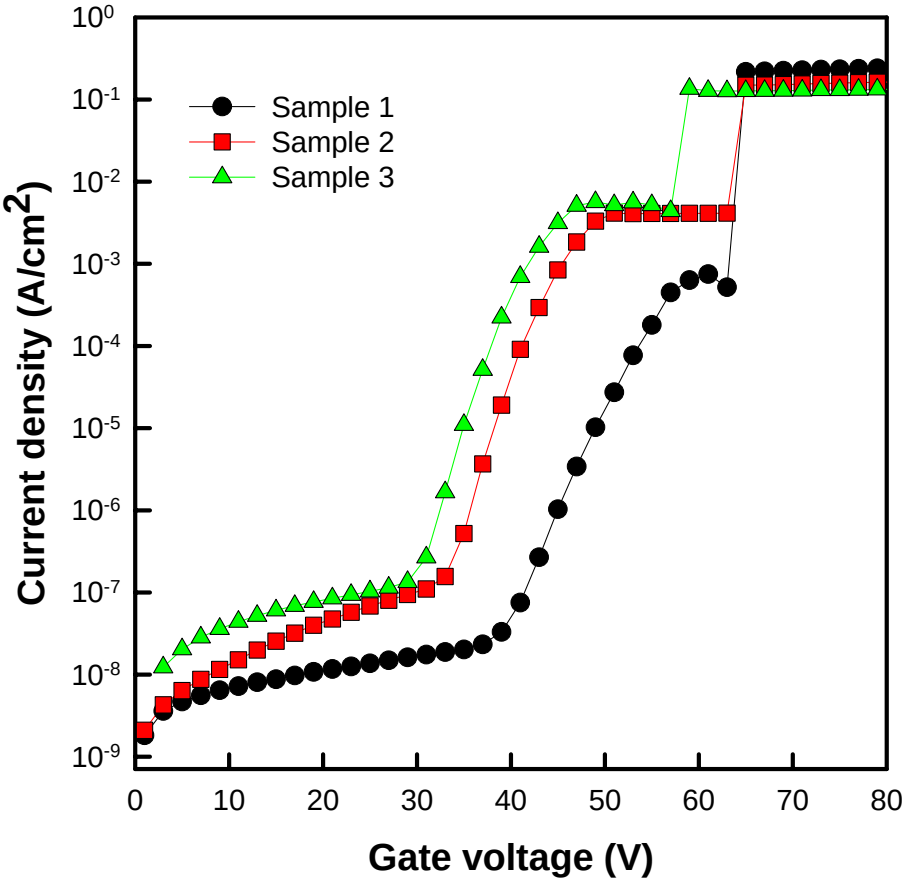

Figure 3-7 The leakage current characteristics of the sandwiched structure. The breakdown voltage is increased with the decrease of oxygen content.

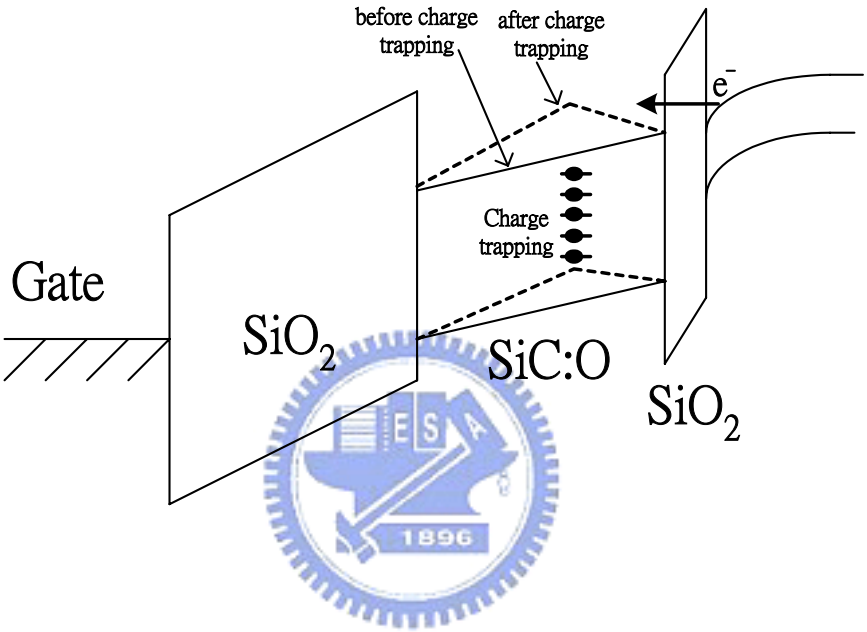

Figure 3-8 The band diagram shows that when the electrons are captured in a charge-trapping layer with rich charge-trapping sites, the conduction band of the charge-trapping layer will be lifted, which forms an energy barrier for the conductive electrons.

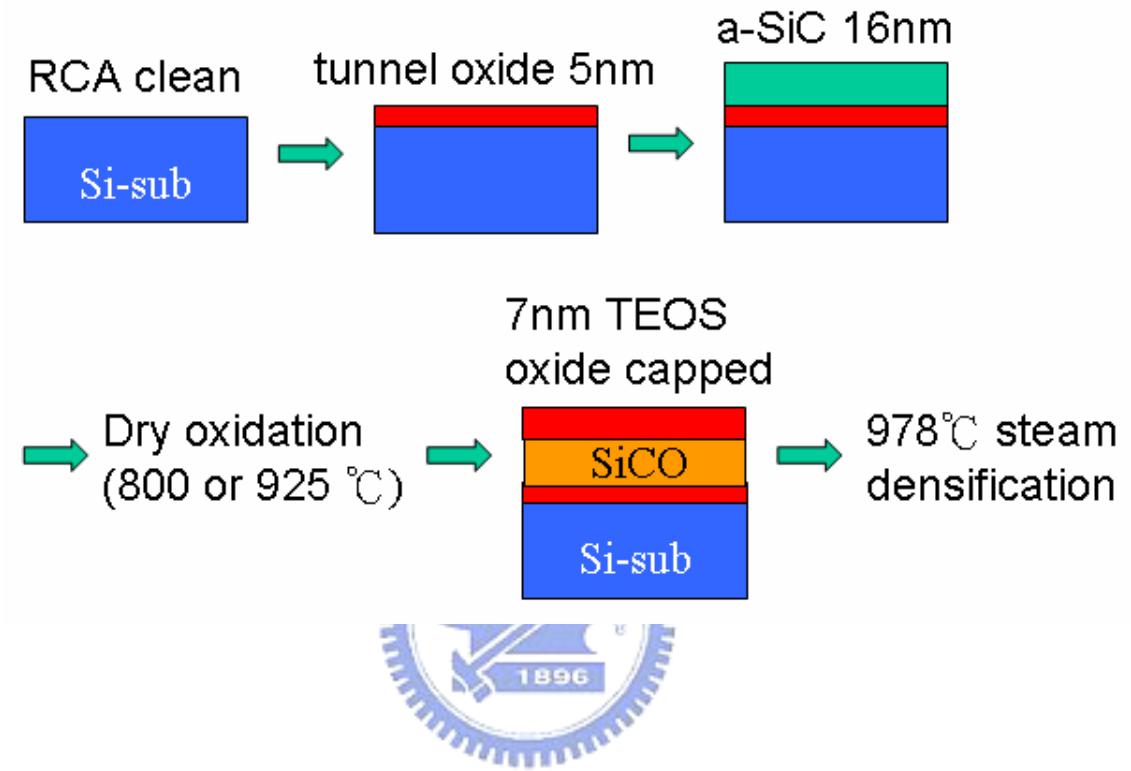

Figure 3-9 The process flow proposed in this work.

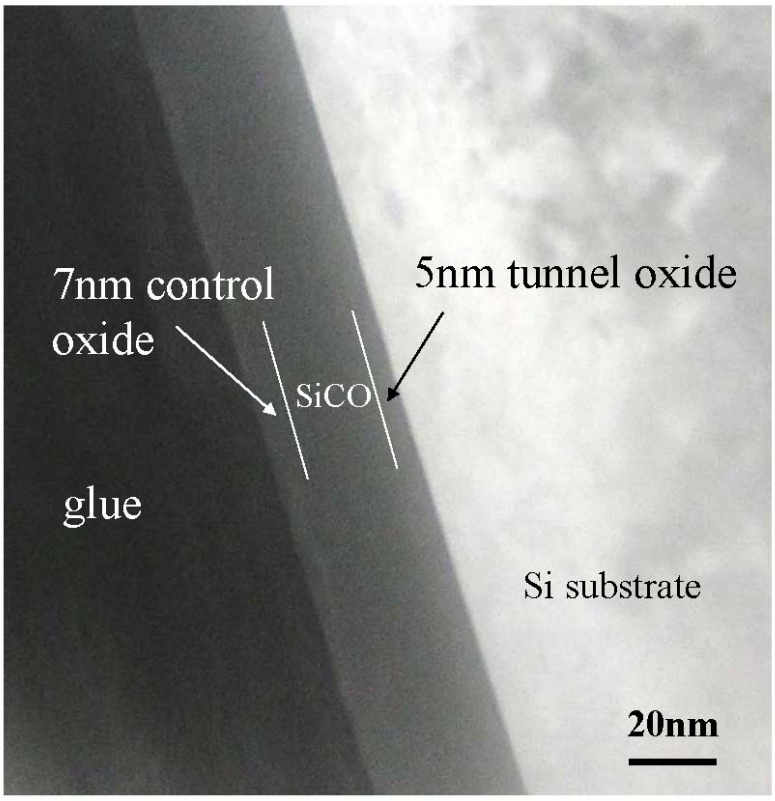

Figure 3-10 The TEM micrograph of the SiCO stack. The thickness of the oxidized SiCO layer is estimated to be around 22.5 nm.

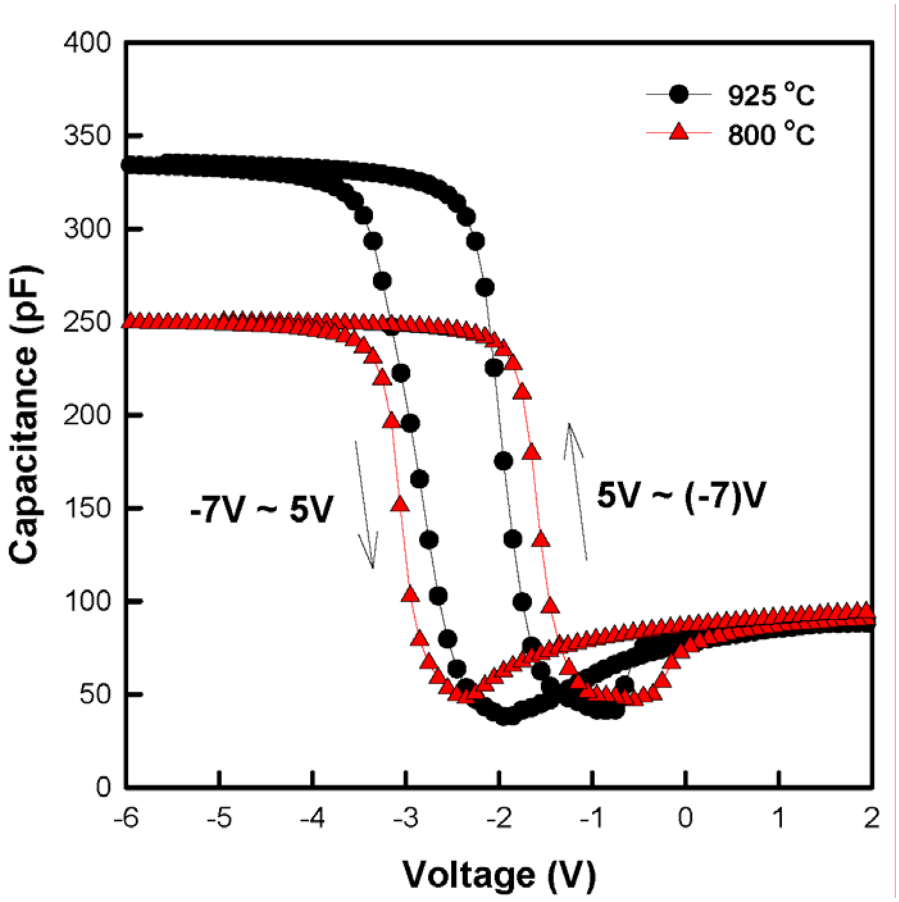

Figure 3-11 The capacitance-voltage (C-V) hysteresis of the MOIOS structure. The electrical C-V measurements are performed by bidirectional voltage sweeping from 5 V ~ (-7) V and (-7) V ~ 5 V.

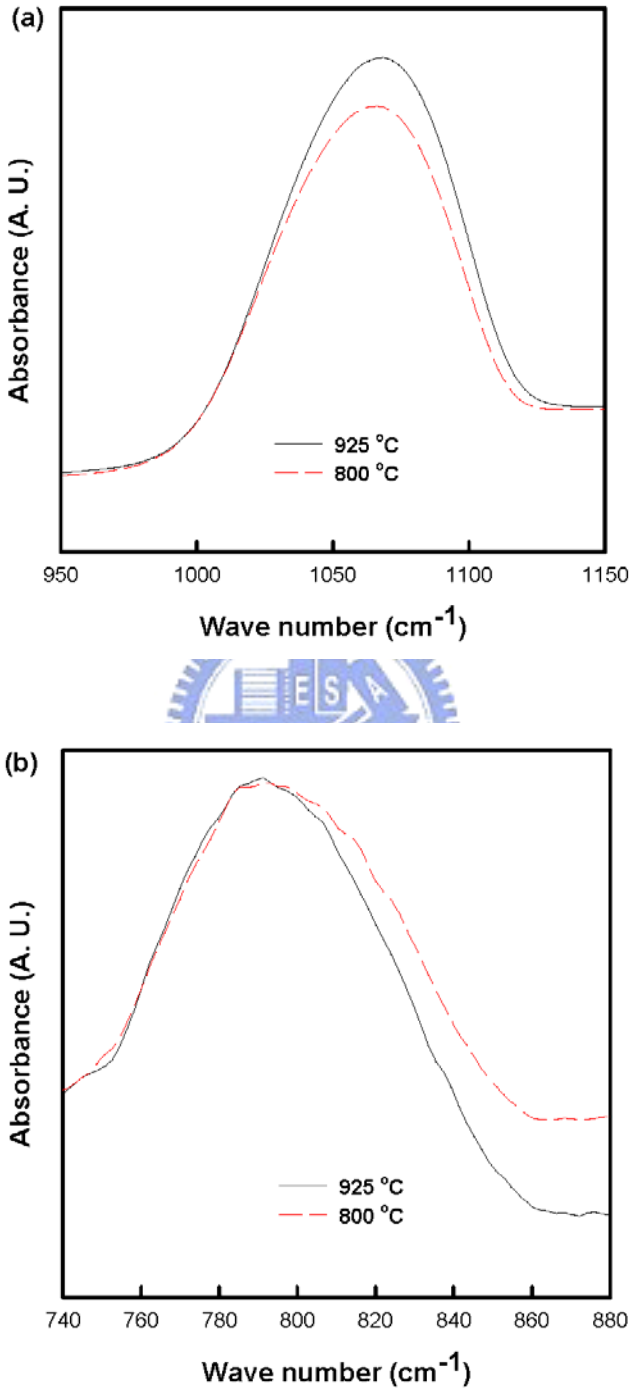

Figure 3-12 FTIR spectra of the SiCO stack with different oxidation temperatures (a) Si-O bonds (b) Si-C bonds.

Chapter 4

A Novel Approach of Fabricating Germanium Nanocrystals for Nonvolatile Memory Application

4.1 Motivation

In the age of 1960's, due to the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [4.1]. To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a moment of portable electronic systems. The most widespread memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector "flash" erase.

Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. On the one hand, the tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide

is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, there is a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry [4.2].

To overcome the scaling limits of the conventional FG structure, Tiwari et al. [4.3] for the first time demonstrated the Si nanocrystal floating gate memory device in the early nineties. Also, the nanocrystal memory device can maintain good retention characteristics when tunnel oxide is thinner and lower the power consumption [4.3-4.5]. In this letter, we proposed a Ge nanocrystal memory device with 4.5nm-thick tunnel oxide and a low operating voltage of 5V, and a significant threshold-voltage shift due to the charge trapping in the Ge dots is observed.

4.2 Experimental procedures

First, the 6-in Si wafer was cleaned with standard RCA recipes, followed by a thermal oxidation process to form 4.5nm-thick dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Right after the growth of tunnel oxide, poly-$Si_{0.8}Ge_{0.2}$ was formed on the oxide immediately by low pressure chemical vapor deposition (LPCVD). The deposition of $Si_{0.8}Ge_{0.2}$ was kept at 550℃ and the pressure was controlled to be 460 mTorr. The flow rate of the reaction gas of SiH_4 and GeH_4 was 60 and 8 sccm, respectively, and the Ge fraction was analyzed to be around 0.2 by Auger electron spectroscopy (AES). Subsequently, the $Si_{0.8}Ge_{0.2}$ layer was wet oxidized in an APCVD reactor and the Ge atoms would be segregated downward until they reach the tunnel oxide surface [4.6-4.8]. Then, a rapid

thermal annealing (RTA) at 950℃ in N_2 ambient was performed to form the Ge nanocrystals. The melting point of Ge was ~938℃. Therefore, the N_2 RTA at 950℃ transformed the Ge layer to liquid phase and the Ge nanocrystals formed after cooling down. In addition, it was well known that during the oxidation of SiGe, GeO_2, a weakly bonded molecule, was created. The 950℃ N_2 RTA would reduce the Ge atoms and the nanocrystals grew based on the Ostwald ripening mechanism [4.9], in which the larger dots grew at the expense of the smaller dots. From the analysis of transmission electron microscopy (TEM), the control oxide capped on the Ge nanocrystals was estimated to be about 40nm. Also, the sample without Ge nanocrystals was fabricated as a control sample. It is fabricated by depositing a poly-Si layer on the tunnel oxide, followed by the wet oxidation of poly-Si layer, the same process done as the silicon germanium layer. The thickness of the oxide fabricated by oxidizing the poly-Si is measured by n&k analyzer, and fine-tuned to be 40 nm. Finally, the Al electrode was patterned and sintered. The metal-insulator-semiconductor (MIS) structure with Ge nanocrystals embedded between tunnel and control oxide was fabricated. In this work, the formation of Ge nanocrystals is only by one step of oxidation of the silicon-germanium layer, which is simpler than the previous research [4.5] and high-throughput and low cost potentially for industrial consideration.

4.3 Results and discussions

A cross-sectional TEM of an oxide/Ge dots/oxide stacked structure is shown in Fig. 4-1. It is clearly shown the Ge nanocrystals are embedded between tunnel oxide and control oxide, which are oxidized from the $Si_{0.8}Ge_{0.2}$, and are separated from each other. The insert schematically shows the gate stack arrangement in this study. The

size of the dots is estimated to be about 5.5nm by TEM. She et al. [4.10] made a conclusion on Ge nanocrystal memory device that nanocrystal size around 5nm is preferred to achieve fast programming speed and longer retention time, and the size should not be scaled below that. The quantum confinement effect for Ge nanocrystals smaller than 5nm is very significant so that the retention time is shorter and the programming time is longer. In this work, the fabricated Ge dots satisfy the demand.

Figure 4-2 shows the hysteresis curves of capacitance-voltage (C-V) measurements after a bias sweeping from –5V to 5V. It is found that a low operating voltage, 5V, causes a significant threshold-voltage shift up to ~0.42V, which is enough to be defined as 1 or 0 for the circuit design. Due to the discrete distribution of the Ge dots and Coulomb blockade effect, the capacitance coupling of the nanocrystal memory device is lower than that of the conventional floating gate memory device. If the capacitive coupling is low to the Ge nanocrystals, the threshold-voltage shift may come from the oxide traps. To distinguish the blur, C-V measurement of sample without Ge dots was preformed (not shown therein). It is found after 5-V write operation that there is almost no V_t shift (lower than 0.01V) for the sample without Ge dots. The threshold-voltage shift resulted from oxide traps is thereby negligible. The density of Ge dots can be electrically calculated through the threshold-voltage shift, ΔV_t, by the following expression:

$$\Delta V_t = \frac{t_{control}}{\varepsilon_{ox}} \cdot Q_t$$

where ε_{ox} is the permittivity of SiO_2, $t_{control}$ the thickness of the control oxide, and Q_t is the density of the trapped charge (C/cm^2 in unit) in Ge nanocrystals. Setting $t_{control}$ = 40nm, ΔV_t = 0.42V, and $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}$ F/cm, the number of electrons trapped in the Ge nanocrystals was calculated to be 2.3×10^{11} cm^{-2}. Due to Coulomb Blockade effect, presumably only one electron was trapped in each Ge nanocrystal [4.3, 4.11];

hence, the aerial density of the Ge dots is about 2.3×10^{11} cm^{-2}.

Figure 4-3 (a) shows the leakage current of the gate dielectric with and without Ge nanocrystals under substrate and gate injection bias. It is clearly shown that under substrate injection bias the leakage of the gate oxide stack with Ge nanocrystals is lower than that without Ge dots. It can be deduced that when the first electron enters into the nanocrystal, the effect of Coulomb blockade [4.11] prevents further injection and storage of more electrons and decreases the leakage current. The reduction in leakage current makes the storage of charges more robust and fault-tolerant. That is, therefore, one of the reasons that nanocrystal memory devices exhibit more rugged retention characteristics than conventional FG ones [4.4]. As considering the leakage current under gate injection bias, there is only little difference between the samples with and without Ge dots due to the lack of Coulomb blockade effect. The conduction mechanism among the gate-dielectric stack with Ge dots is inferred from Fowler-Nordheim (F-N) tunneling [4.12] which can be expressed as follows:

$$J = E^2 \exp\left[-\frac{8\pi\sqrt{2m^*}(q\phi_B)^{3/2}}{3qhE}\right]$$

where E is the electric field which is defined as the applied voltage divided by total thickness of the tunnel and control oxide, m^* the electron effective mass, h the Planck's constant, ϕ_B the energy barrier at the injecting interface (3.1eV for Si-SiO_2), and $\ln(J/E^2)$ is proportional to (1/E). In Fig. 4-3 (b), after the transformation of Fig. 4-3 (a), it is clearly found there is a linear region in high field, which proves the conducting mechanism with Ge dots embedded in the oxide stack is F-N tunneling. The layer without Ge dots embedded also creates a well-fitted F-N plot at high field, which is not shown therein. Also, the insert exhibits the band diagrams of F-N tunneling for writing and erasing operation in this study.

In addition, to realize the retention characteristics of the structure, a stricter test

environment of 150 ℃ is conducted [4.13, 4.14]. In Fig. 4-4, the threshold-voltage shift is measured with different periods of time when the sample is heated at 150 ℃. It is found that the oxide stack with Ge dots embedded retains a good retention property without a significant decline of the memory window, ΔV_t, up to 15 hours, which is robust in the Flash nonvolatile memory technology.

4.4 Conclusion

A nonvolatile memory device embedded with Ge nanocrystal dots is fabricated by the thermal oxidation of $Si_{0.8}Ge_{0.2}$ combined with a rapid thermal annealing at 950℃ in N_2 gas. The tunnel oxide in the nonvolatile memory is controlled to be 4.5 nm-thick and embedded with 5.5-nm Ge nanocrystals. A low operating voltage, 5V, is implemented and a significant threshold-voltage shift, 0.42V, is observed. When the electrons are trapped in the Ge nanocrystals, the effect of Coulomb blockade prevents the injection and storage of more electrons and decreases the leakage current. Also, the retention characteristics are tested to be robust.

A distributed charge storage with GeO_2 nanodots

Due to the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory in the age of 1960's. In 1967, D. Kahng and S. M. Sze invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs. To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates an era of portable electronic

systems. The most widespread memory array organization is the so-called Flash memory, which has a byte-selectable write operation combined with a sector “flash” erase.

Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirement put on the tunnel oxide layer. On the one hand, the tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. There is, therefore, a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry. To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned, SONOS and nanocrystal nonvolatile memory devices. As for SONOS, the nitride layer is used as the charge-trapping insulator. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory. Tiwari *et al.* for the first time demonstrated the Si nanocrystal floating gate memory device in the early nineties. Also, the nanocrystal memory device can maintain good retention characteristics when tunnel oxide is thinner and lower the power consumption. In this contribution, we proposed a GeO_2 nano-dot memory device with 4.5nm-thick tunnel oxide and a low operating voltage of 5V. Insulating nano-dots are utilized as the storage elements rather than the semiconducting counterparts. The

concepts of SONOS and nanocrystal memories are combined and explored for the first time. A significant memory effect due to the charge trapping in the GeO_2 dots is observed.

First, the 6-in Si wafer was cleaned with standard RCA recipes, followed by a thermal oxidation process to form 4.5nm-thick dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Right after the growth of tunnel oxide, poly-$Si_{0.8}Ge_{0.2}$ was formed on the oxide immediately by low pressure chemical vapor deposition (LPCVD). The deposition of $Si_{0.8}Ge_{0.2}$ was kept at 550℃ and the pressure was controlled to be 460 mTorr. The flow rate of the reaction gas of SiH_4 and GeH_4 was 60 and 8 sccm, respectively, and the Ge fraction was analyzed to be around 0.2 by Auger electron spectroscopy (AES). Subsequently, the $Si_{0.8}Ge_{0.2}$ layer was oxidized in an APCVD reactor at 950℃ and the Ge atoms would be segregated downward until they reach the tunnel oxide surface. The Ge dots grew based on the Ostwald ripening mechanism, in which the larger dots grew at the expense of the smaller dots. After the Si elements of the $Si_{1-x}Ge_x$ layer are completely oxidized, the Ge nanocrystals tend to be oxidized into GeO_2 nano-dots as the oxidation process is not ceased. From the analysis of transmission electron microscopy (TEM), the control oxide capped on the GeO_2 nano-dots was estimated to be about 40 nm and the GeO_2 nano-dots were confirmed via x-ray absorption near-edge structure (XANES). Finally, the Al electrode was patterned and sintered. Electrical measurements were performed on the metal-insulator-semiconductor (MIS) structures with GeO_2 nano-dots embedded between tunnel and control oxide.

A cross-sectional TEM micrograph of an oxide/GeO_2 nano-dots/oxide stacked structure is shown in Fig. 4-5. It is clearly observed the GeO_2 nano-dots are embedded between the tunnel oxide and control oxide, oxidized from the $Si_{1-x}Ge_x$ layer, and are separated from each other. The insert schematically shows the gate stack arrangement

in this study. The mean size and aerial density of the dots are estimated to be about 5.5 nm and 4.3×10^{11} cm^{-2}, respectively, by TEM.

To confirm the existence of the composition of the GeO_2 nano-dots, x-ray absorption near-edge structure (XANES) is performed [4.15-4.17]. In XANES, a core electron is excited to higher bound or quasi-bound states, which contain information about coordination geometry and electronic aspects of the absorbing atom. Among most of the XANES studies, the standard materials with known valence is utilized as references, and compared with the unknown samples. Therefore, the measurements are frequently qualitatively-analyzed, not quantitatively. In this work, we used Ge powder, GeO_2 powder, and $Si_{0.8}Ge_{0.2}$ epitaxial layer on Si as the standard materials and our investigated sample with nano-dots observed as the unknown sample. The x-ray source is extracted from the National Synchrotron Radiation Research Center. As shown in Fig. 4-6, the shift of absorption edge (roughly the center of the intensity jump) is an index of the Ge oxidation state. The obvious edge shift from the Ge edge and the high degree of similarity between the XANES results of the sample with nano-dots and GeO_2 standard reveal that Ge is oxidized. Its oxidation state is very close to GeO_2.

Figure 4-7 shows the capacitance-voltage (C-V) hysteresis after the bidirectional bias sweeps between 5 V and (-5) V. It is found that a low operating voltage, 5 V, causes a significant threshold-voltage shift up to ~0.45 V, which is sufficient to be defined as “1” or “0” for the logic-circuit design. It is worth noting that the hysteresis is counterclockwise which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of the Si substrate.

Figure 4-8 demonstrates the band diagrams of the operation of the novel distributed charge storage with GeO_2 nano-dots. The “write” and “erase” operation with different gate polarities of the memory device are exhibited. When the device is written or

programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the GeO_2 nano-dots. When the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the GeO_2 nano-dots by Fowler-Nordheim (F-N) tunneling. It is believed that during the oxidation process of the Ge nanocrystals into GeO_2 nano-dots, there are defects or traps created in the interfaces between GeO_2 dots and tunnel and control oxide. When the device is under programming, the injected electrons will be captured in the interfacial traps of the GeO_2 dots and contribute to a threshold voltage shift (memory window). It is concerned about that if the storage of GeO_2 nano-dots is as reliable as other insulating thin films. The reliability issues such as endurance and retention of the memory device should be taken into account and are currently under investigation.

In summary, we have demonstrated the novel distributed charge storage with GeO_2 nano-dots. The mean size and aerial density of the dots are estimated to be about 5.5 nm and 4.3×10^{11} cm^{-2}, respectively. The composition of the GeO_2 dots is confirmed by the XANES measurements. In electrical analyses, a significant memory effect is observed with a threshold voltage shift of 0.45 V under 5-V operation. Also, a physical model is proposed to explain the charge storage via the interfacial traps of GeO_2 nano-dots. Further works about the research on the reliability issues are currently under investigation.

(Supplement)

In addition to the fabrication method of forming Ge nanocrystals demonstrated in this chapter, a more flexible and direct approach is proposed in the supplement. Figure 4-9 illustrates the process flow of fabricating Ge nanocrystals by rapid thermal oxidation. After the p-type Si wafer was RCA cleaned, a 5nm-thick dry oxide was

thermally grown as the tunnel oxide at 925 ℃ in an atmospheric pressure chemical vapor deposition furnace. Subsequently, a 7nm-thick SiGe layer was deposited at 450 ℃ by low pressure chemical vapor deposition, followed by a rapid thermal oxidation at 925 ℃. During the oxidation process, the oxidation of SiGe will be conducted faster along the grain boundary than that of the grain of the SiGe layer and the oxidation mechanism of SiGe is as described as the beginning of this chapter. After the oxidation of SiGe was performed, a 35nm-thick TEOS oxide is capped as the control oxide, followed by the process of steam densification to densify the control oxide. In this approach, the rapid oxidation of SiGe was intended to fabricate SiGe nanodots embedded in silicon dioxide after the oxidation along the grain boundary of the SiGe layer. Until the silicon element was completely consumed to SiO_2 during the oxidation process, the Ge nanodots were precipitated and reside on the tunnel oxide layer. It is deduced that under an appropriate control of the rapid oxidation of the SiGe layer, SiGe or Ge nanodots can be fabricated as expected. As shown in Fig. 4-10, the Raman spectrum of the gate stack of the SiGe as-deposited sample and that after the capping of control oxide exhibits that the germanium precipitation is formed at wave number of ~ 300 cm^{-1} and there is no absorption of SiGe precipitation at ~ 400 cm^{-1} after the oxidation process of SiGe layer. It is deduced that the oxidation time is sufficiently long to fully oxidize the Si element of the SiGe layer and the Ge nanodots are segregated. Figure 4-11 shows the C-V hysteresis of the gate stack after the densification of the control oxide. The pronounced memory effects of the Ge nanocrystals embedded in silicon dioxide are shown with different programming voltages. The memory window of the memory device is increased with the programming voltage. To ensure the realization of the memory device, further investigation of the memory device needs to be taken into account.

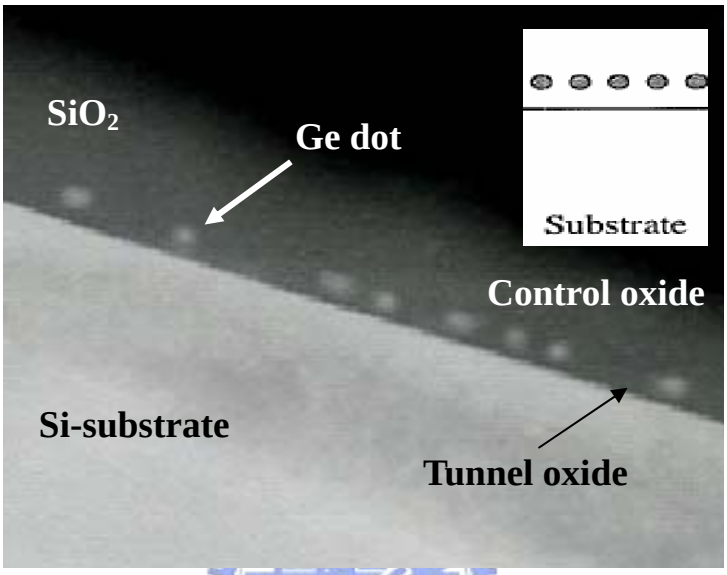

Figure 4-1 Ge nanocrystals formed after high temperature rapid thermal annealing in N_2 gas. The insert shows the gate stack in this study.

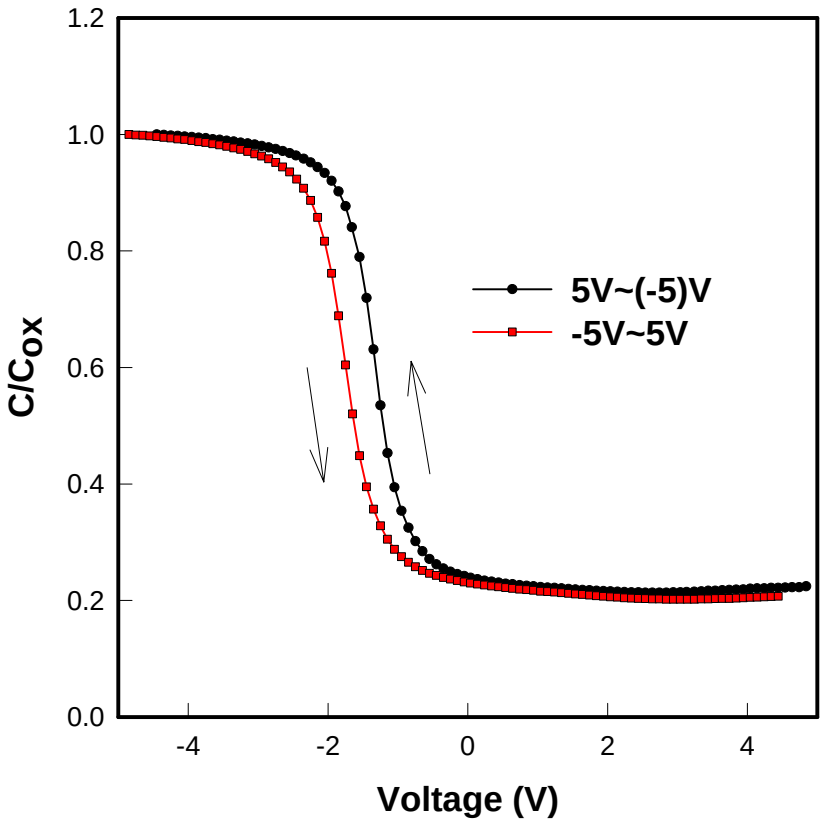

Figure 4-2 The hysteresis of capacitance-voltage (C-V) measurements after 5V and –5V sweeping.

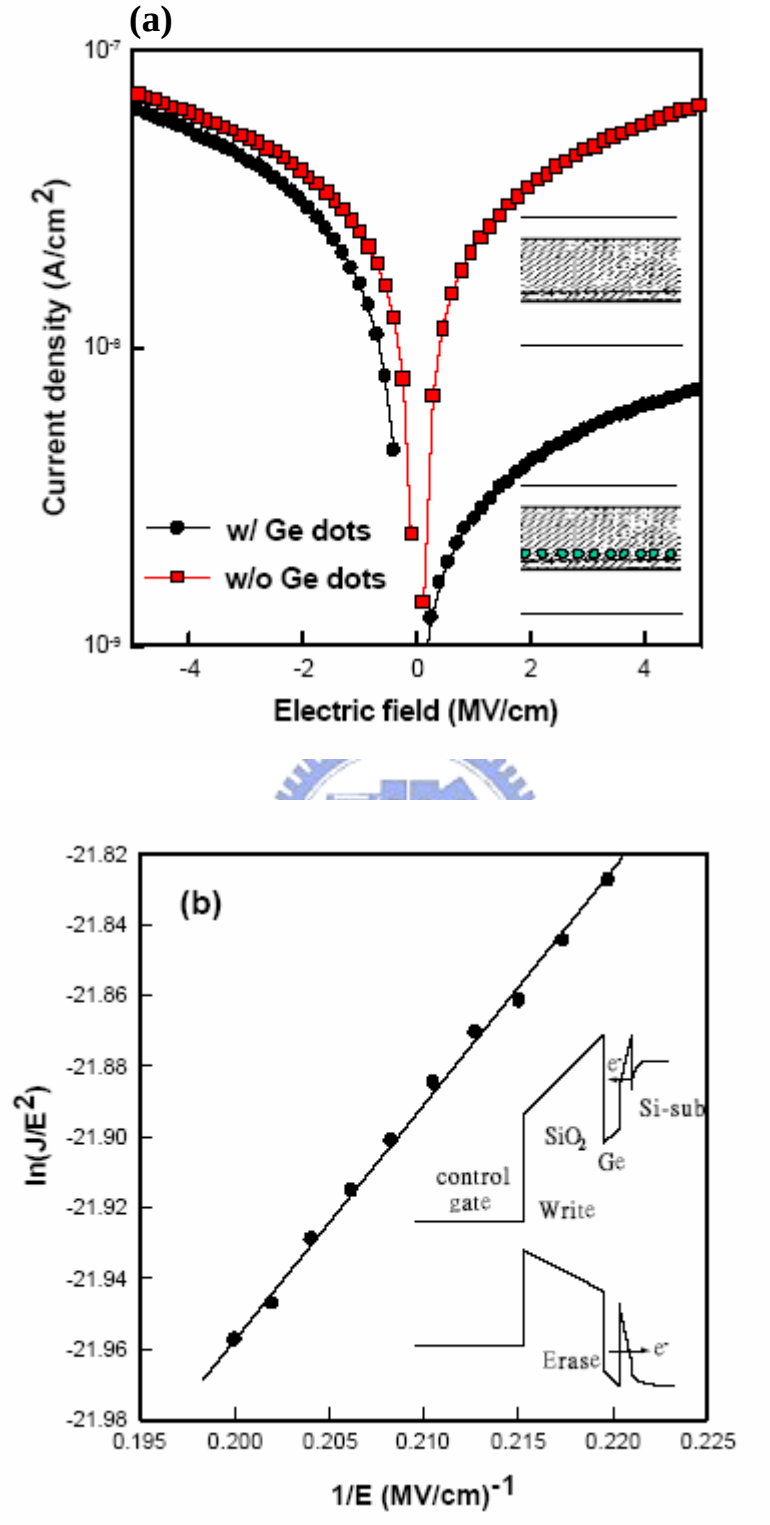

Figure 4-3 (a) The leakage current of the gate dielectric with and without Ge nanocrystals (b) The relation of $\ln(J/E^2)$ versus (1/E) shows the conduction mechanism is F-N tunneling and the insert shows the band diagrams of writing and erasing operation.

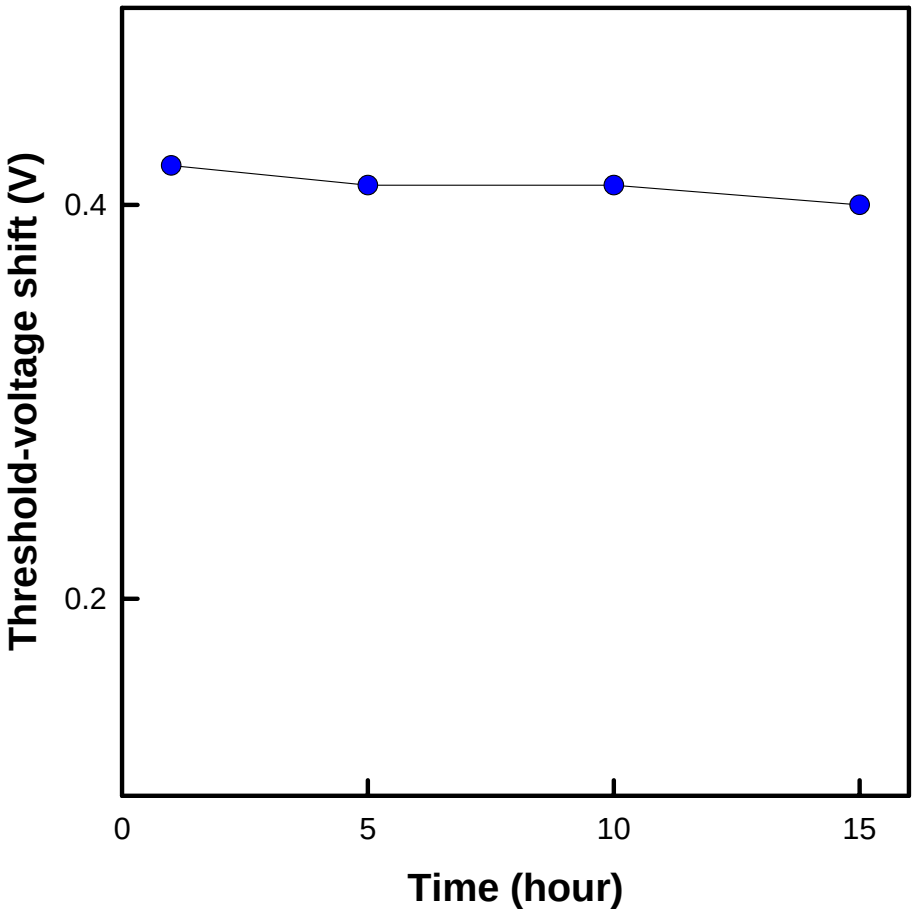

Figure 4-4 The threshold-voltage shift is measured with different periods of time when the sample is heated at 150 ℃.

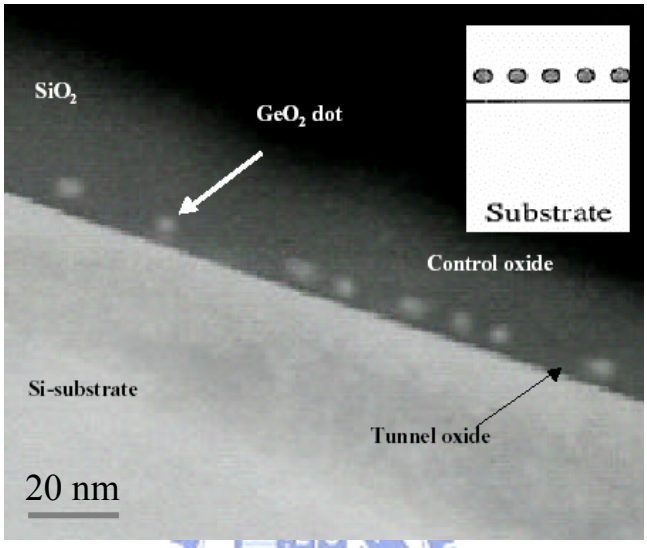

Figure 4-5 The cross-sectional TEM micrograph of an oxide/GeO_2 nano-dots/oxide stacked structure.

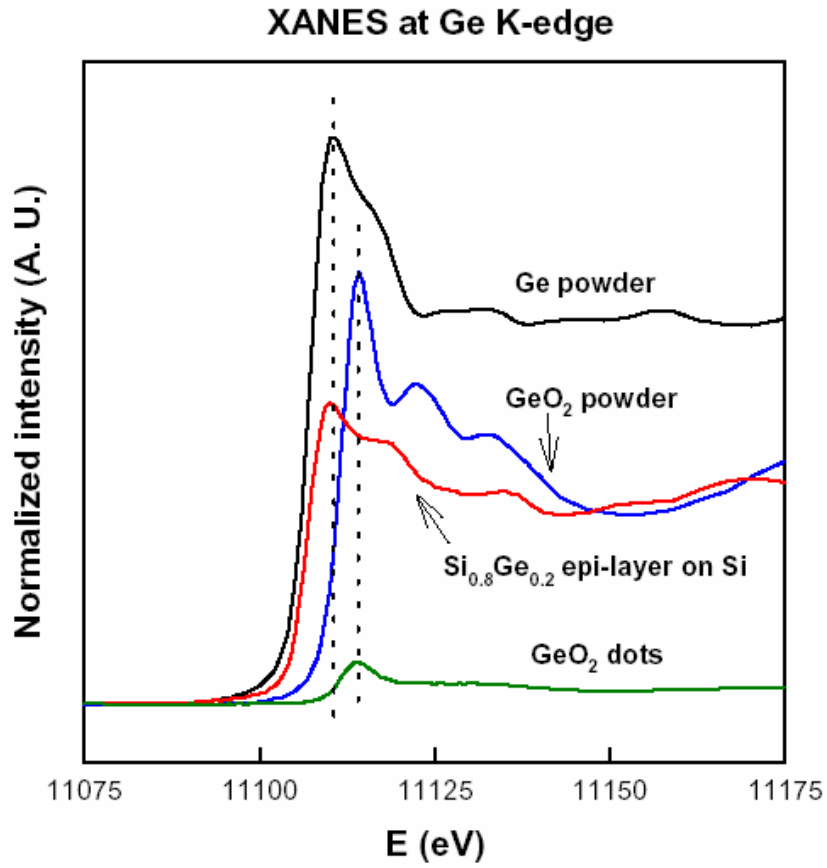

Figure 4-6 The XANES spectra of the investigated sample and standard samples.

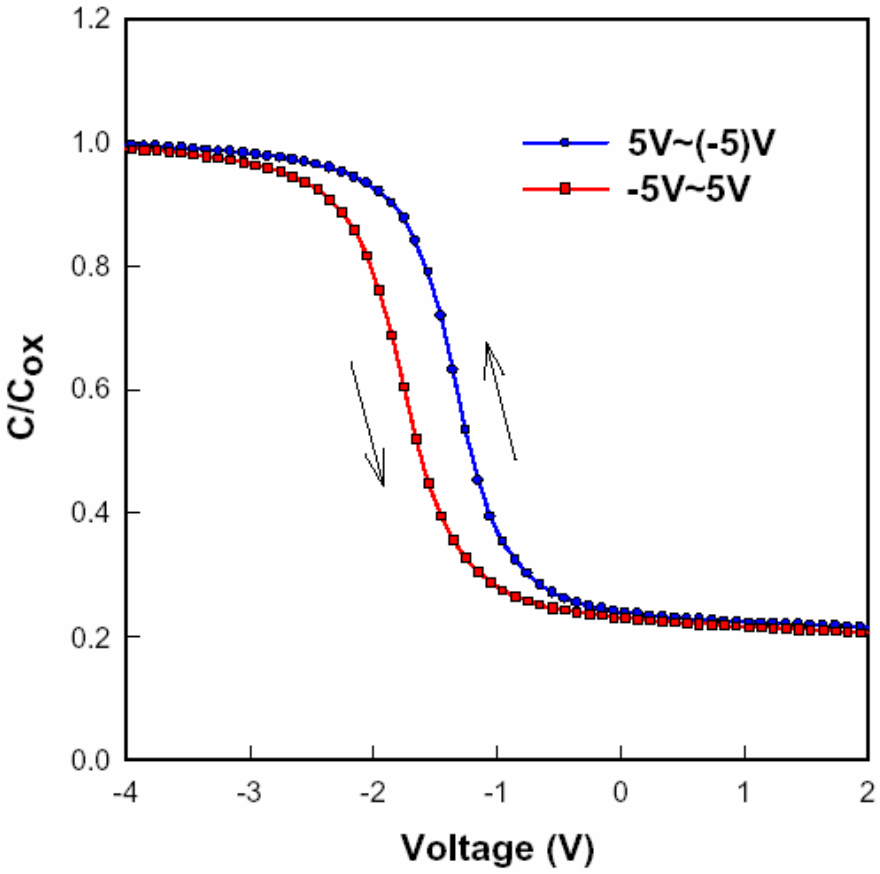

Figure 4-7 The capacitance-voltage hysteresis after the bidirectional bias sweeps between 5 V and (-5) V.

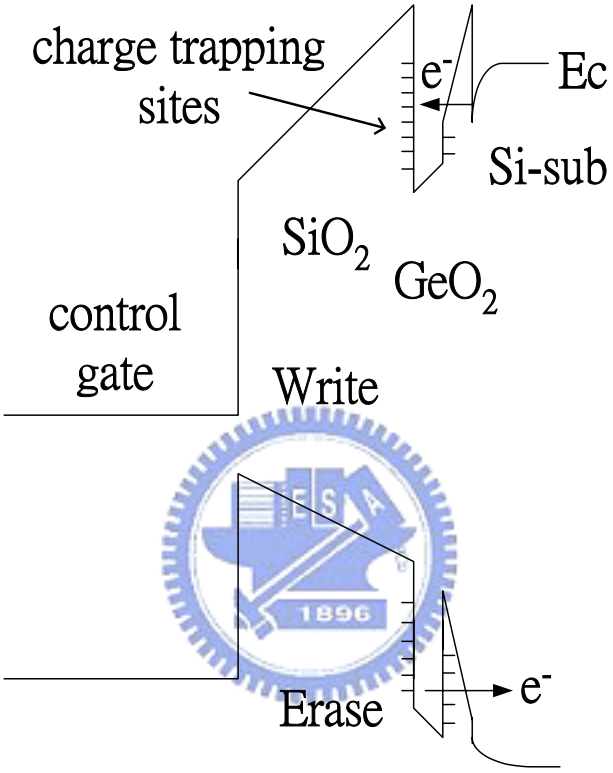

Figure 4-8 The band diagrams of the operation of the novel distributed charge storage with GeO_2 nano-dots.

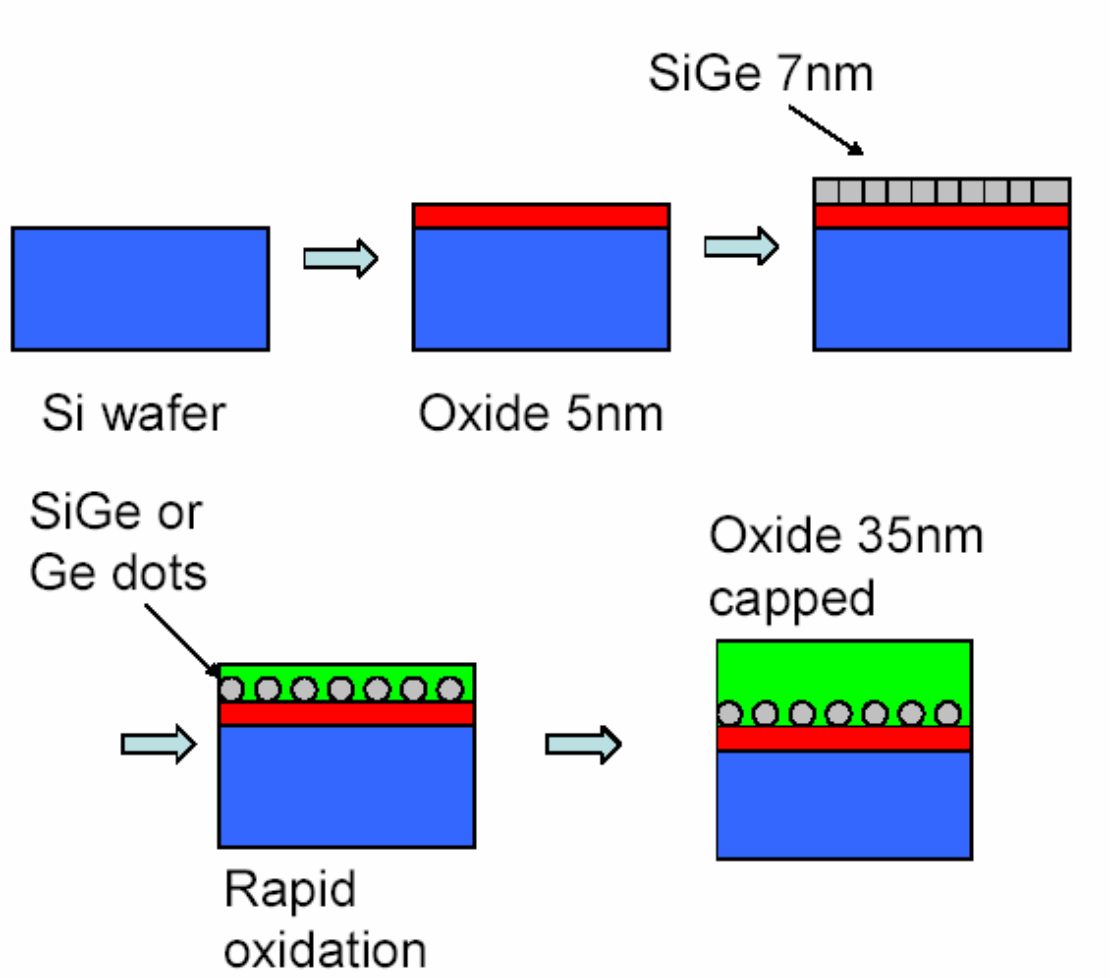

Figure 4-9 The process flow of fabricating Ge nanocrystals by rapid oxidation.

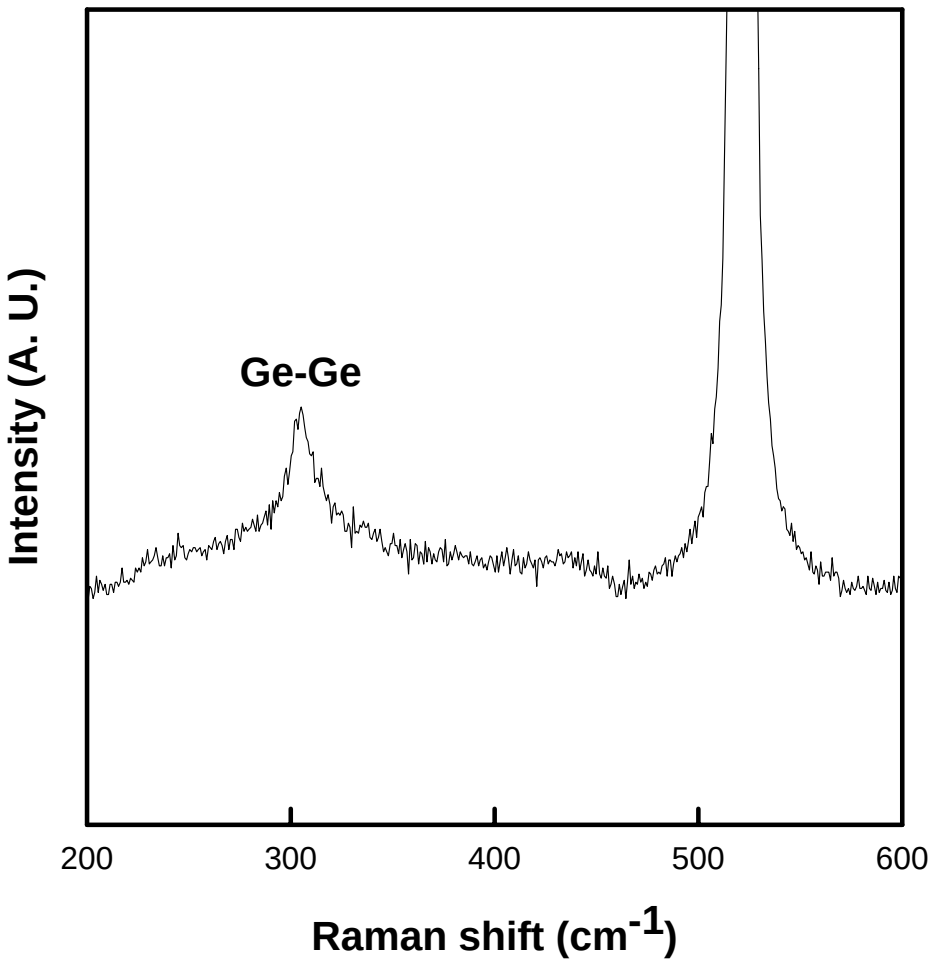

Figure 4-10 The Raman spectrum of the gate stack after the capping of control oxide. It is clearly observed that germanium precipitation is formed after the oxidation process of SiGe layer.

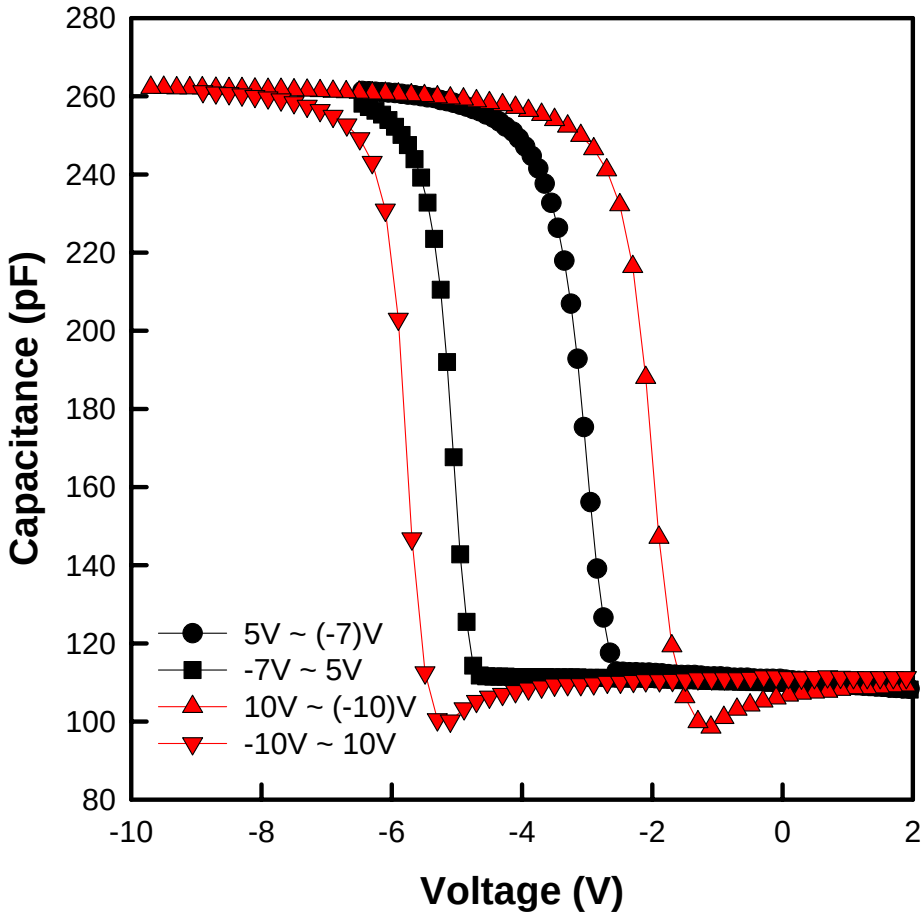

Figure 4-11 The C-V hysteresis of the gate stack after the densification of the control oxide. The pronounced memory effects of the Ge nanocrystals embedded in silicon dioxide are shown with different programming voltages.

Chapter 5

Electron charging and discharging effects of tungsten nanocrystals embedded in silicon dioxide for low-power nonvolatile memory technology

5.1 Motivation

Recently, considerable attention has been focused on semiconductor or metal nanocrystals embedded in the silicon dioxide of a metal-oxide-semiconductor (MOS) device for future high speed and low power consuming memory device [5.1-5.2]. The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate EEPROM memories, allowing for thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed [5.3-5.5]. The self-assembling of silicon or germanium nanocrystals embedded in SiO_2 layers has been widely studied, and strong memory effects in MOS devices were reported [5.6-5.8]. There are, however, quite few reports on the memory effects of metal nanocrystals during the past years. The major advantages of metal nanocrystals over their semiconductor counterparts include (1) higher density of states around the Fermi level, (2) stronger coupling with the conduction channel, (3) a wide range of available work functions, and (4) smaller energy perturbation due to carrier confinement [5.2]. In this study, we demonstrated the electron charging and discharging effects of tungsten (W) nanocrystals embedded in SiO_2, which is of special interest for applications of low-power nonvolatile memory (NVM) technology. Its implementation is compatible with the current manufacturing

technology of semiconductor industry and represents a viable candidate for low-power sub-100 nm nonvolatile memory nodes.

5.2 Experimental procedures

Single-crystal, 6 in. in diameter, (100) oriented p-type silicon wafers were used in the present study. The wafers were chemically cleaned by a standard RCA cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace to form a 4.5-nm tunnel oxide. Subsequently, an 8-nm tungsten-rich tungsten silicide layer, W_5Si_3, was physically sputtered onto the tunnel oxide. The W_5Si_3 layer was capped by a 10-nm amorphous Si layer deposited also by sputtering. The stacked structure was, afterwards, dry oxidized at 900 ℃ to form a layer with control oxide on the top and tungsten nanocrystals precipitated and embedded between tunnel oxide and control oxide. For tungsten silicide films deposited on SiO_2, in the initial stage of the thermal oxidation, the removal of Si from the silicide layer (to form SiO_2) leads directly to the formation of free tungsten [5.9]. The capped amorphous Si was utilized to compensate for the insufficiency of the control oxide derived only from the oxidation of the tungsten-rich tungsten silicide. Al gate electrode was finally patterned and sintered. The structural analyses were performed by transmission electron microscopy (TEM). Also, Fourier transform infrared spectroscopy (FTIR) was used to determine the bonding type of the sample. The capacitance-voltage (C-V) measurements were performed by a precision LCR meter HP 4284A to study the electron charging and discharging effects of the tungsten nanocrystals. To examine the reliability issue of the tungsten nanocrystal memory device, the endurance characteristics were demonstrated. The HP 8110A pulse generator was connected to the HP 4284A through a switch and the C-V

measurements were performed after the stress of the periodic pulses to identify the relationship of threshold voltage shift (memory window) versus pulse cycles.

5.3 Results and discussions

Figure 5-1 represents a typical bright-field, cross-section TEM image. The W nanocrystals show a dark contrast on a gray background. Spherical and well-separated W nanocrystals embedded in the SiO_2 layer are clearly observed. The mean size and aerial density of the W nanocrystals are found to be 4.5 nm and $3.7\times10^{11}/cm^2$, respectively. During the oxidation process of the tungsten silicide, it is concerned that if the tungsten nanocrystals are formed rather than being completely oxidized. As shown in Fig. 5-2, the FTIR spectrum of the gate dielectric exhibits a sharp Si-O bonding type at around 1075 cm^{-1} and a W-W bonding type at around 714 cm^{-1}, indicating no apparent W-O (1000 cm^{-1}), W-O-W (684 cm^{-1}), or O-W-O bonds (800 cm^{-1}) [5.10-5.13]. The W-O, W-O-W, and O-W-O bonds may be covered in the FTIR spectrum and not obviously observed in contrast to other pronounced bonding types. If the tungsten elements are completely oxidized, the absorption of W-W bonds may not be observed and the absorption of W-O, W-O-W, or O-W-O becomes significant. It is inferred that tungsten oxide would only partially form and mantle around the tungsten nanocrystals after the oxidation process of W_5Si_3. Si-O and W-W bonds are, therefore, predominant in the gate dielectric. Also, the absorption of Si-O bonds at 1255 cm^{-1} indicates the formation of high quality films [5.14-5.15]. A premise for the oxidation of the tungsten silicide to fabricate and improve the uniformity of the W dots is to control and optimize the oxidation process otherwise the tungsten elements would be fully oxidized.

Figure 5-3(a) shows the capacitance-voltage (C-V) hysteresis after bidirectional

sweeps, which implies the electron charging and discharging effects of tungsten nanocrystals embedded in SiO_2. The bidirectional C-V sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited a threshold voltage shift, ΔV_t, indicating electron charging effect. In Fig. 5-3(a), with the voltage swept from 3 to (-4) V and back to 3 V, a significant threshold voltage shift of 0.95 V is observed. As the swept voltage is increased to 8 or 10 V, a more pronounced C-V shift is observed. It is worth noting that the hysteresis is counterclockwise which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of Si substrate [5.16]. Figure 5-3(b) shows the band diagrams of "write" and "erase" operations with different gate polarities of the memory device. When the device is written or programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the tungsten nanocrystals. When the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the tungsten nanocrystals by Fowler-Nordheim (F-N) tunneling. Thanks to the large work function of the tungsten nanocrystals (4.55 eV) compared with the electron affinity of Si channel (4.05 eV), the electrons tunneling from the inversion layer of the silicon substrate are easily trapped in the nanocrystals and not easy to escape by tunneling back to the channel. This feature improves the retention characteristics of the memory device and implies the slower erasing than programming [5.17]. In addition, the tungsten nanocrystals do not bear a voltage drop from gate voltage, which means all the voltages provided from control gate are dropped to tunnel oxide and control oxide and gains profit over their semiconductor counterparts. In conventional floating gate nonvolatile memory devices, the operating voltage is above 7 V which is not easy to scale down due to the thick gate-stacked structure. In our approach to fabricate the tungsten nanocrystals

embedded in SiO_2, a lower programming voltage of 3 V and erasing voltage of (-4) V actualize a significant threshold voltage shift, 0.95 V, which is sufficient to be defined as "1" and "0" by a typical sense amplifier for a memory device.

Figure 5-4 exhibits the endurance characteristics, after different write/erase cycles, of the tungsten nanocrystal memory device. The write and erase voltages are 3 and (-4) V, respectively. The memory window is hardly reduced until 10^6 W/E cycles are performed. Even though 10^9 pulse cycles are performed, it retains a large memory window of ~ 0.71 V without catastrophic decline as the previous reports on nanocrystal memory devices [5.1, 5.6]. This demonstrates the rugged nature of the tungsten nanocrystal memory device with the suitability for low-power nonvolatile memory devices.

5.4 Conclusion

In summary, we have demonstrated the electron charging and discharging effects of tungsten nanocrystals embedded in the SiO_2 layer. Spherical and well-separated tungsten nanocrystals embedded in the SiO_2 layer are fabricated with a mean size and aerial density of 4.5 nm and $3.7\times10^{11}/cm^2$, respectively. The tungsten dots are formed by the thermal oxidation of the tungsten silicide. A significant C-V hysteresis of V_t shift of 0.95 V is observed and the endurance of the memory device is not degraded up to 10^6 write/erase cycles. The implementation in this study is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power sub-100 nm nonvolatile memory nodes.

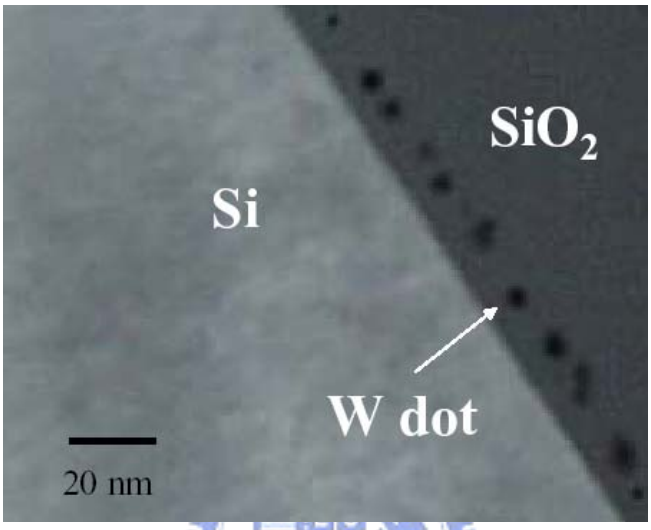

FIG. 5-1 A typical bright-field, cross-section TEM image. The W nanocrystals show a dark contrast on a gray background.

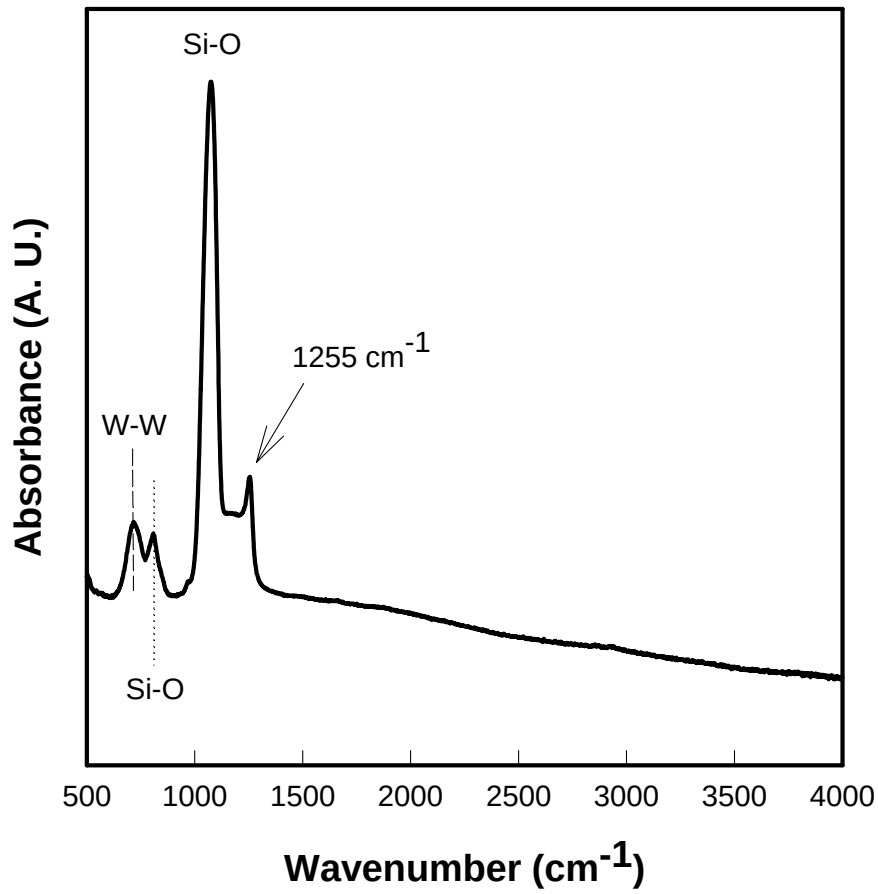

FIG. 5-2 The FTIR spectrum of the gate dielectric exhibits a sharp Si-O bonding type at around 1075 cm^{-1} and a W-W bonding type at around 714 cm^{-1}, indicating no apparent W-O, W-O-W, or O-W-O bonds.

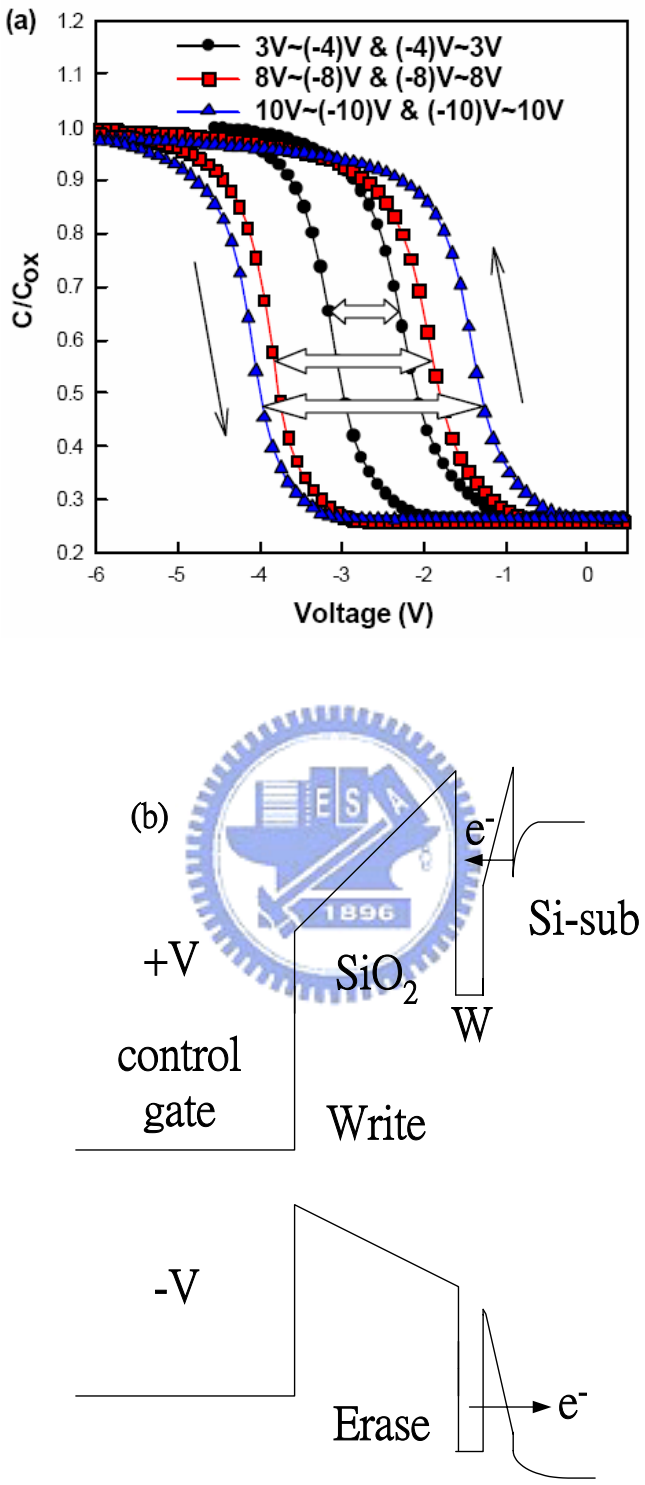

FIG. 5-3 (a) The capacitance-voltage (C-V) hysteresis after bidirectional sweeps, which implies the electron charging and discharging effects of tungsten nanocrystals embedded in SiO_2 and (b) the band diagrams of "write" and "erase" operations with different gate polarities of the memory device.

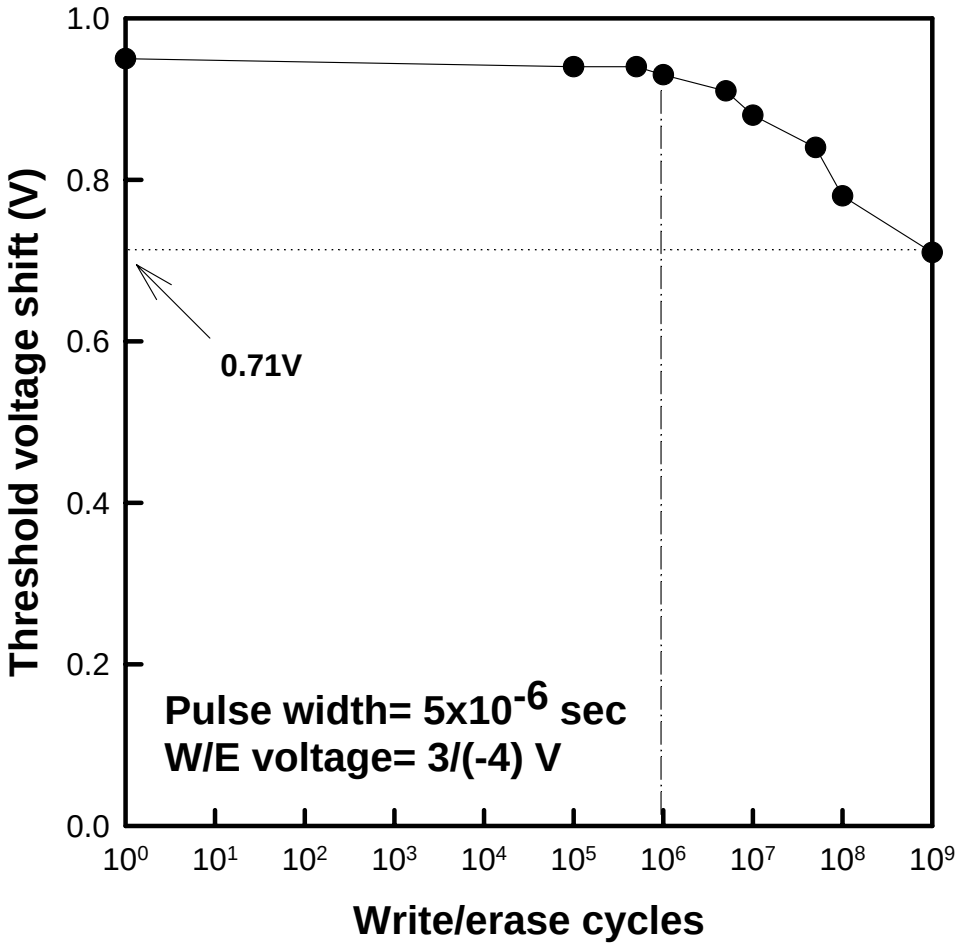

FIG. 5-4 The endurance characteristics, after different write/erase cycles, of the tungsten nanocrystal memory device. The write and erase voltages are 3 and (-4) V, respectively.

Chapter 6

Quasi-Superlattice Storage (QS^2): A Novel Concept of Multilevel Charge Storage

6.1 Motivation

Recently, portable electronic devices such as digital cameras, laptops, smart cards, mp3 players, USB Flash, have received much attention in the market and significantly impacted the semiconductor industries. All the abovementioned products are based on the device of Flash nonvolatile memory. The commercially available Flash memory contains the structure of a poly-Si floating gate (FG), which is served as a charge-trapping layer [6.1]. Since the difficulties of consecutive scaling have been faced, [6.2] the candidate, SONOS nonvolatile memory device, arose and positioned an important part of the industry [6.3-6.6]. SONOS possesses a structure similar to FG memory device but silicon nitride is adopted as the charge-trapping layer rather than poly-Si layer [6.7-6.8]. The SONOS structure has a great potential of scaling the thickness of the tunnel oxide down to 1.6 nm and reducing the programming voltage below 5 volts [6.7, 6.9]. That, hence, improves the performance of speed of the memory device. In this study, both Si and silicon nitride are utilized as the charge-trapping layers and a Si/silicon nitride quasi-superlattice structure is proposed as the multilevel charge storage for the first time. Through the electrical measurements, 2-bit per cell Fowler-Nordheim (F-N) tunneling operation has been proposed. The leakage behavior of the quasi-superlattice stack for the multilevel charge storage has also been demonstrated and a concise model is proposed to deduce

and explain the leakage behavior of the quasi-superlattice gate stack.

6.2 Experimental procedures

Single-crystal, 6 in. in diameter, (100) oriented p-type silicon wafers were used in the present study. The wafers were chemically cleaned by a standard RCA cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace at 925 ℃ to form a 3-nm tunnel oxide. Subsequently, silicon nitride (Si_3N_4) and amorphous Si (a-Si) quasi-superlattice of two periods were deposited by low pressure chemical vapor deposition (LPCVD) at 780 ℃ and 550 ℃, respectively. Each of the four LPCVD layers was controlled to be about 2 nm. A 10-nm-thick tetraethyl orthosilicate (TEOS) oxide was deposited on the quasi-superlattice as the control oxide layer. To densify the control oxide layer, a steam densification was performed at 982 ℃ [6.10]. Via the TEOS oxide deposition and steam densification, the two a-Si layers will be crystallized into micro-crystal or poly-crystal, which depends on the grain size of the Si layers. After the Al electrodes were patterned and sintered, capacitance-voltage (C-V) measurements were performed to investigate the memory effects of the quasi-superlattice storage (QS^2) memory device.

6.3 Results and discussions

Figure 6-1 shows the device structure in this work. The quasi-superlattice of Si_3N_4 and a-Si, sandwiched between tunnel oxide and control oxide, is utilized as a charge storage element for a memory device instead of poly-Si FG or Si_3N_4 single layer. Figure 6-2 shows the ideal energy band diagram of the QS^2 memory device at V=0.

The quasi-superlattice of Si_3N_4 and a-Si clearly shows the band offsets that can easily trap electrons as the storage elements. The undoped a-Si layers are with a wider bandgap than that of the Si substrate. To write the memory device, a positive gate voltage has to be applied to make electrons directly tunnel through the tunnel oxide by F-N tunneling. The tunneling electrons may be trapped in the trap states of the nitride layers, the interface states between Si_3N_4 and a-Si layers, or the quantum wells of the a-Si layers. The trapped electrons cause a threshold voltage shift (ΔV_t), memory window, of the memory device, which can be defined as "1" or "0" according to the different threshold voltages. To erase the memory device, negative gate polarity is applied to make the trapped electrons tunnel back to the channel. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the charge trapping sites by F-N tunneling.

Figure 6-3 exhibits C-V hysteresis after the bi-directional voltage sweeping. The voltage is swept between 4 and (-7) V or 7 and (-7) V. The erasing voltage is fixed at (-7) V. Under the programming voltage of 4 and 7 V, the memory window is 0.1 and 0.93 V, respectively, and increasing with the programming voltage. It is worth noting that the hysteresis is counterclockwise which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of Si substrate [6.11].

Under varied programming voltages and fixed erasing voltage, the relationship between threshold voltage shift and programming voltage is of special interest. Figure 6-4 exhibits the gate voltage dependence of the memory window. The threshold voltage shift is increased with the gate voltage. However, there are two sudden rises of the threshold voltage shift observed, which are taken place at around 5 and 9.5 V.

As the memory device is written with different programming voltages, the tunneling electrons will be captured at the trap states of the Si_3N_4 layer, the interface states between Si_3N_4 and a-Si layers, and/or the quantum well of a-Si. During low-voltage programming, the electrons are captured at the charge-trapping sites of trap states of the Si_3N_4 layer and the interface states between Si_3N_4 and a-Si layers. The sudden rise implies the charge storage of the a-Si quantum well. Figure 6-5 shows the band diagram of the memory device under programming. The first sudden rise in Fig. 6-4 is attributed to the charge storage in the a-Si quantum well between two nitride layers. The second sudden rise is deduced that under high-voltage programming the electrons may be written in to the a-Si quantum well between nitride and control oxide layers. It is also observed that in Fig. 6-4 the increments of the two sudden rises are obviously different from each other. The increment of the second sudden rise is smaller than that of the first one. The threshold voltage shift is due to the electrons trapped in the gate dielectrics and the trapped electrons away from the channel influence the threshold voltage less. Therefore, more considerable threshold voltage shift is observed among the first low-voltage charge storage in the a-Si quantum well. The threshold voltage of a MOS capacitor is described as

$$V_t = V_{FB} + 2\psi_B + \frac{\sqrt{4\varepsilon_s q N_A (2\psi_B)}}{C_i} \quad (1)$$

where V_{FB} is the flat-band voltage shift, ϕ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i, ε_s the permittivity of the semiconductor, N_A the density of the acceptors, and C_i the capacitance of the insulator.[12] In this study, the threshold voltage shift ΔV_t is mainly determined by the flat-band voltage shift ΔV_{FB}. $\Delta V_t \approx \Delta V_{FB} = Q_t / C_i$, where Q_t is the charge trapped in the quasi-superlattice structure after programming. As inferred in Fig. 4, the trapped charge Q_t is increased with the programming voltage. Under low-voltage programming below 5 V, the injecting charges can tunnel through the tunnel oxide and be trapped in the forbidden gap of the first nitride layer and the interface between Si and Si_3N_4. It is not easy for the electrons to cross the barrier height of 3.1 eV between Si channel and tunnel oxide via Schottky emission under low-voltage programming. As the programming voltage reaches 5-7 V, the first sudden rise of the threshold voltage shift occurs, which contributes the memory window from 0.2 V to 0.93 V. The injecting electrons occupy the energy levels of the Si quantum well during the first sudden rise of the threshold voltage shift. Beyond the programming voltage of 7 V, the increased memory window is attributed from the charge storage in the forbidden gap of the second nitride layer, overcoming the barrier height of ~2.0 eV between Si and nitride. The programming voltage of 9.5 V and above is needed to lead to the second rise of the threshold voltage shift. In this work, the quasi-superlattice storage implies a 2-bit-per-cell operation by F-N tunneling.[13] In the design of the multilevel storage, bit-1 can be operated in the a-Si quantum well between the nitride layers at low voltage about 5~7 V. Bit-2 can be operated in the a-Si quantum well between nitride and control oxide layers at around 10 V. The 2-bit-per-cell operation is performed by F-N tunneling instead of the conventional channel hot electron injection.

Also, the dual read operation of source side and drain side for conventional SONOS 2-bit/cell device is not necessary, which simplifies the circuit design engineering.

To investigate the leakage behavior of the quasi-superlattice stack structure, current-voltage electrical measurements are performed. Figure 6-6 exhibits the current density-voltage (J-V) characteristics for both room temperature and 50 K. It is clearly shown the leakage current at 50 K is lower than that at room temperature as a factor of two orders due to the alleviation of thermionic emission [6.14]. The leakage current at room temperature, dominated by thermionic emission and trap-assisted tunneling, remains low when 10-V gate voltage is applied. Additionally, there is negative differential resistance observed at different gate biases for the measurements of 50 K. The inset shows the local amplification of the J-V curve at 50 K. The negative differential resistance occurs at around 2, 5.2, and 7 V. It is inferred that the current-voltage characteristics behave like that of the resonant tunneling diode (RTD) at low temperature [6.15-6.17]. To clarify the similarity between RTD and our quasi-superlattice stack of insulators, a model is proposed based on the energy band diagrams of tunneling. Figure 6-7 shows the ideal energy band diagram of the quasi-superlattice stack under zero bias with split energy levels. The quasi-superlattice of Si_3N_4 and a-Si clearly shows the band offsets that can easily trap electrons as the memory elements. The undoped a-Si layers are with a wider bandgap than that of the Si substrate. In the a-Si quantum wells, discrete energy levels, E_1, E_2, …, and E_n, are formed due to quantum confinement effect [6.18-6.19]. Consider the resonant tunneling between the two a-Si layers under biases applied. As can be seen in Fig. 6-8 (a), after the electrons tunnel from the channel, it is not easy for the electrons to surmount the energy barriers of nitride and control oxide at 50 K. Therefore tunneling effects dominate the leakage mechanism. As the applied voltage is around 2 V, a resonant tunneling of E_1 occurs between the two a-Si quantum wells.

The first resonant tunneling contributes the peak current density at 2 V as shown in the inset of Fig. 6-6. As the voltage is applied between 2 and 5.2 V as Fig. 6-8 (b), there is no energy level existed in the a-Si quantum well for the electrons to resonantly tunnel through. A sudden decrease of the leakage current occurs, followed by the gradual increase of the leakage current, and the second resonant tunneling of E_2 is reached at around 5.2 V. The peak current density at 7 V in Fig. 6-6 is inferred to be the resonant tunneling of E_3 between the two a-Si quantum wells. At low temperature operation, the leakage behavior is dominated by the tunneling effects which can be described as $J \propto V^2 \exp[-\frac{C}{V}]$, where V is the programming voltage and C is a constant.[20] Considering the quantum confinement of the Si quantum wells, the energy levels are approximated as $E_n = \frac{n^2 \pi^2 \hbar^2}{2m^* L^2}$, where n=1, 2, 3…, m* is the effective mass of the electrons in the quasi-superlattice structure, and L is the thickness, ~2 nm, of the Si quantum wells. As n=1, 2, and 3, E=E_1, E_2, and E_3, the resonant tunneling occurs at the programming voltage of 2 V, 5.2 V, and 7 V, respectively. To calculate the resonant voltage drop of the Si quantum wells, m* is estimated to be around 0.19 m_0 for the electrons transport in the Si layer. The first resonant tunneling voltage drop V_{1r} of the Si quantum wells can be calculated by $V_{1r} = \frac{2E_1}{q} = 0.98V$, where q=1.6×$10^{-19}$C. Also, V_{2r} and V_{3r} can be calculated as V_{2r}=3.92V and V_{3r}=8.82V. The first resonant tunneling is occurred when the programming voltage reached about 2 V. Therefore, the voltage difference of 2-0.98=1.02 V is dropped on the tunnel oxide, control oxide, and nitride layers. To motivate the second resonant tunneling, additional voltage dropped on the Si quantum wells, V_{2r}-V_{1r}, needs to be supplied. The additional voltage drop is calculated as 2.94 V, which is close enough to the voltage difference, 3.2 V, of the programming voltage between first and second resonant tunneling. As the programming voltage is increased to 7 V to stimulate the

third resonant tunneling, it is deduced that the third resonant tunneling is due to the instability of the two amorphous silicon layers where there should be at least 8.82 V to motivate the third resonant tunneling between the Si quantum wells. The investigation of the leakage mechanism of the quasi-superlattice stack will help the multilevel charge storage develop the considerations of operating voltage for the 2-bit-per-cell nonvolatile memory device. Further study about the reliability characteristics is being taken into account and currently under investigation.

6.4 Conclusion

In this work, a novel concept of the quasi-superlattice storage has been demonstrated for the first time. Under suitably operated voltage, two apparent states of charge storage can be distinguished. The memory effects are due to the multilevel charge storage within the quasi-superlattice. The multilevel charge storage provides a feasible design for the 2-bit-per-cell nonvolatile memory devices. Also, the leakage behavior of the quasi-suprlattice structure has also been characterized by current-voltage measurements at room temperature and low temperature. The resonant tunneling-like leakage characteristic is observed at low temperature. A concise physical model is proposed to characterize the leakage mechanism of tunneling for the quasi-superlattice structure and suggests that the considerations of operating voltage for the 2-bit per cell nonvolatile memory device need to be taken into account.

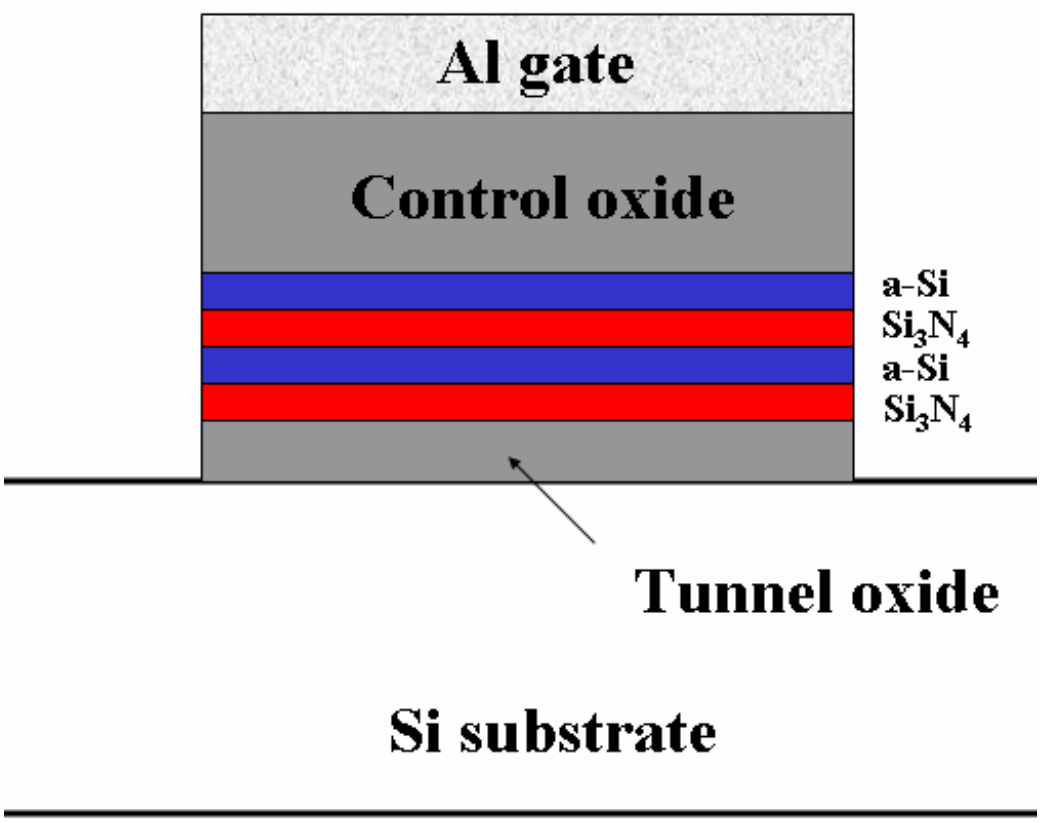

Figure 6-1 The cross-sectional figure of the quasi-superlattice structure.

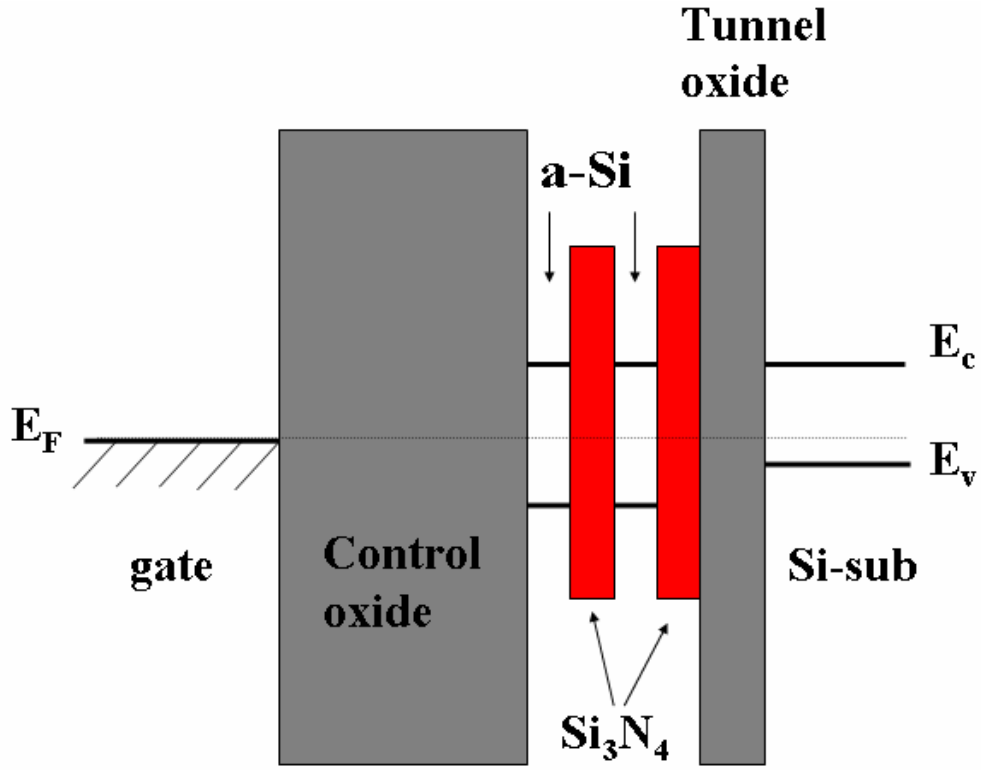

Figure 6-2 The ideal energy band diagram of the QS^2 memory device at V=0.

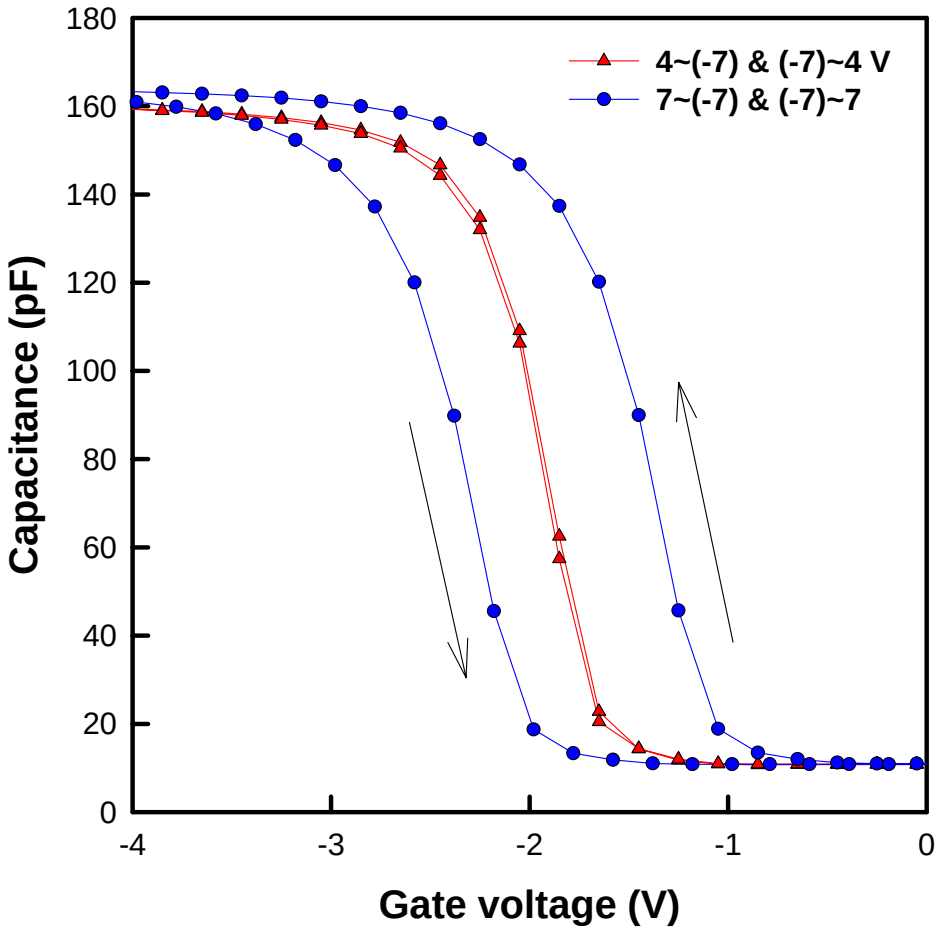

Figure 6-3 C-V hysteresis after the bi-directional voltage sweeping. The erasing voltage is fixed at (-7) V.

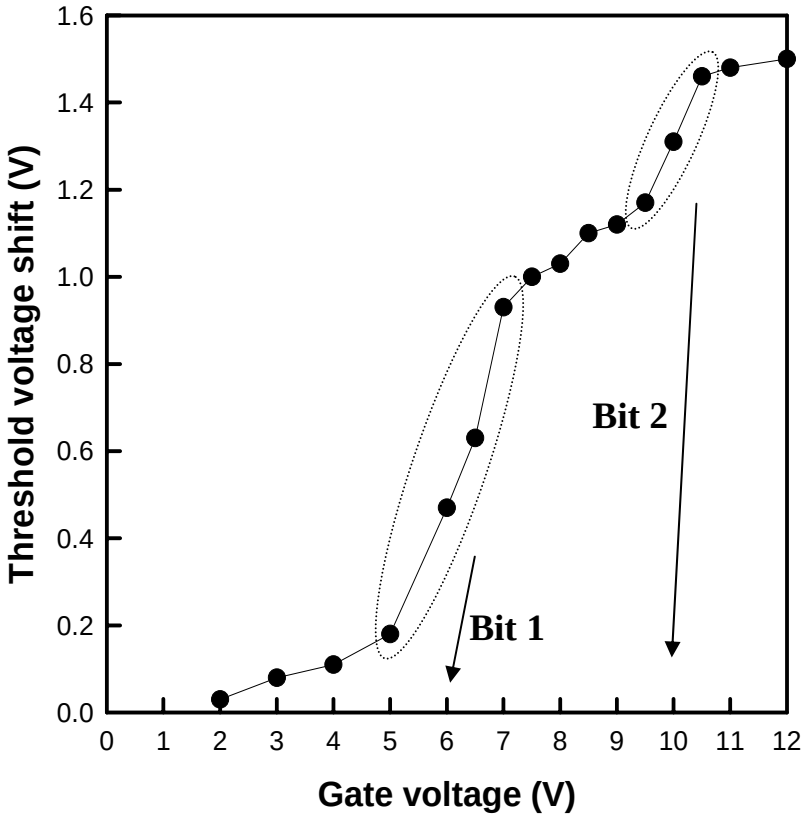

Figure 6-4 Gate voltage dependence of the memory window. There are two sudden rises of the threshold voltage shift observed, which are taken place at around 5 and 9.5 V.

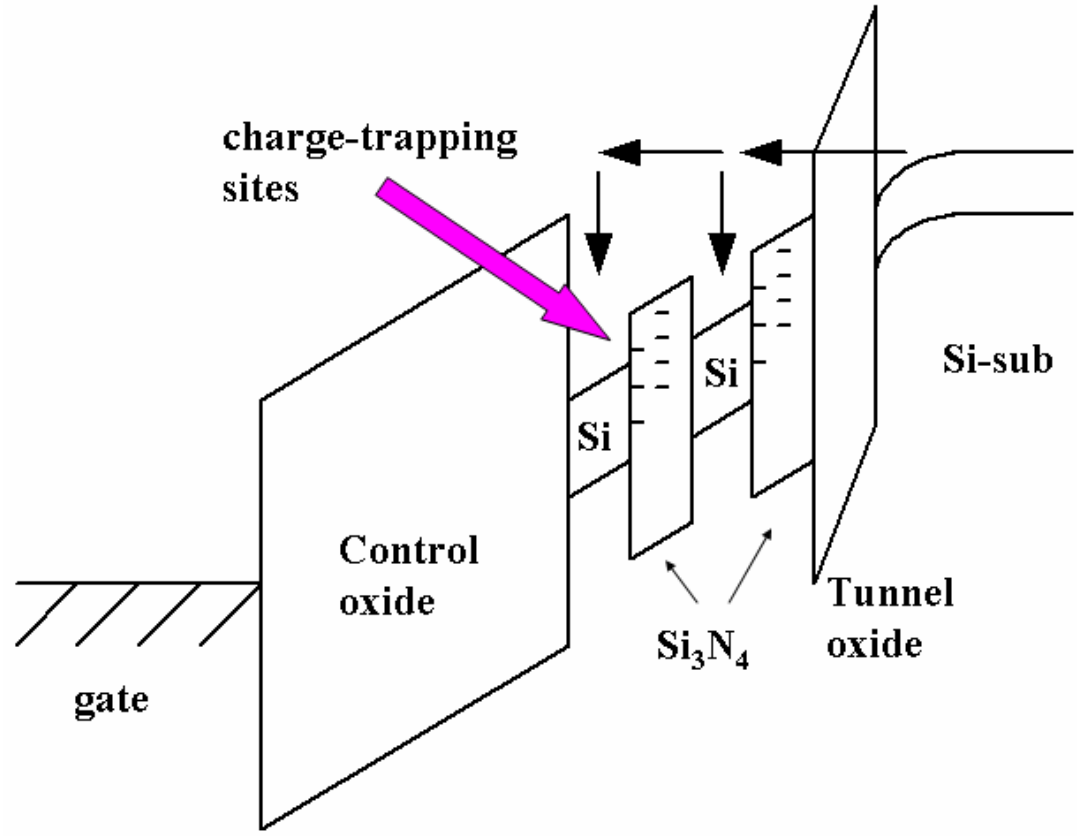

Figure 6-5 The band diagram of the memory device under programming. Under suitably operated voltage, two apparent states of charge storage can be distinguishable.

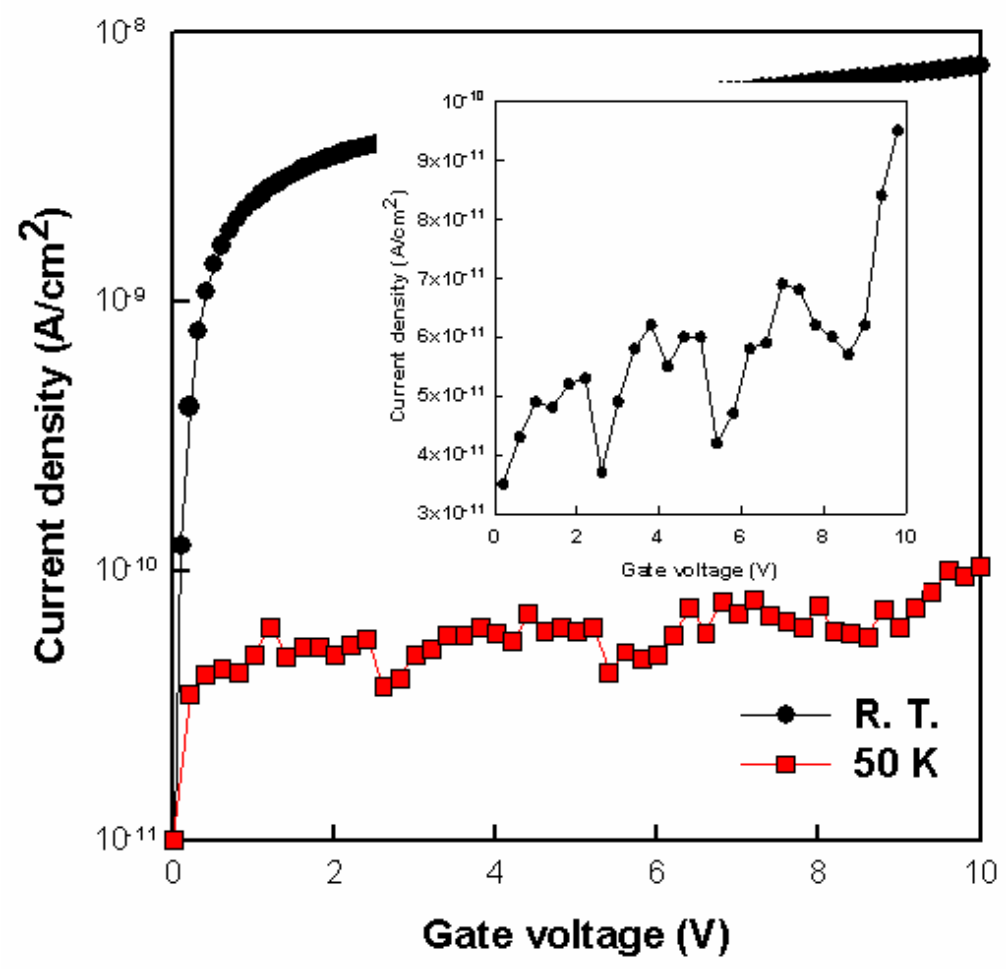

Figure 6-6 The current density-voltage (J-V) characteristics for both room temperature and 50 K. The inset shows the local amplification of the J-V curve at 50 K.

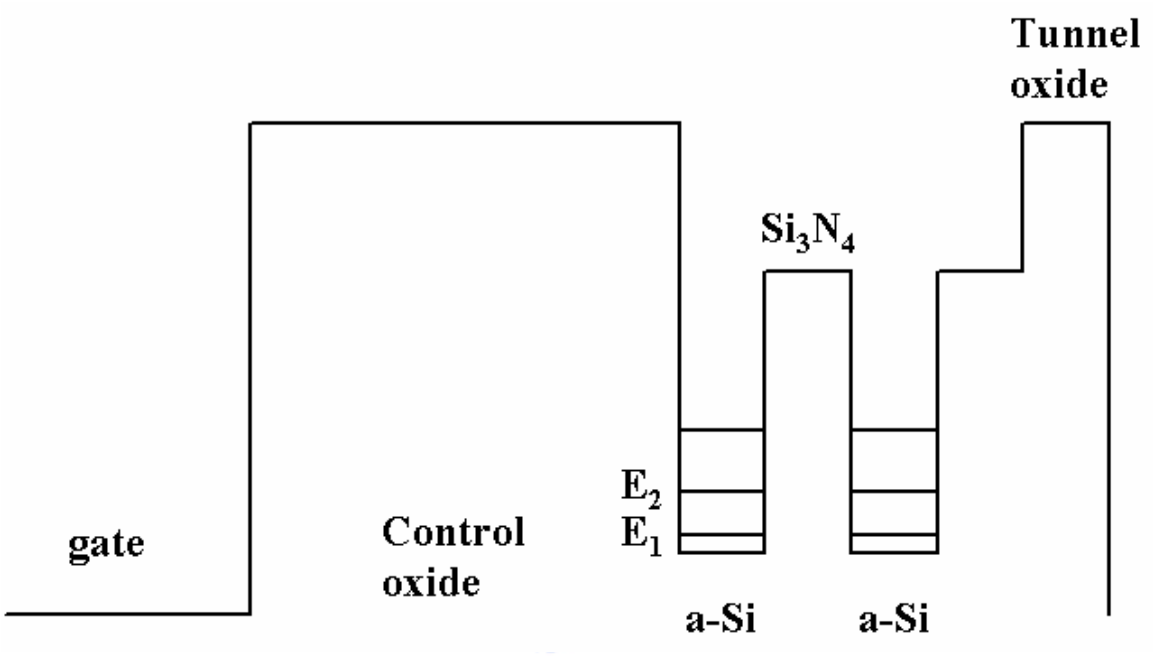

Figure 6-7 The ideal energy band diagram of the quasi-superlattice stack under zero bias with split energy levels.

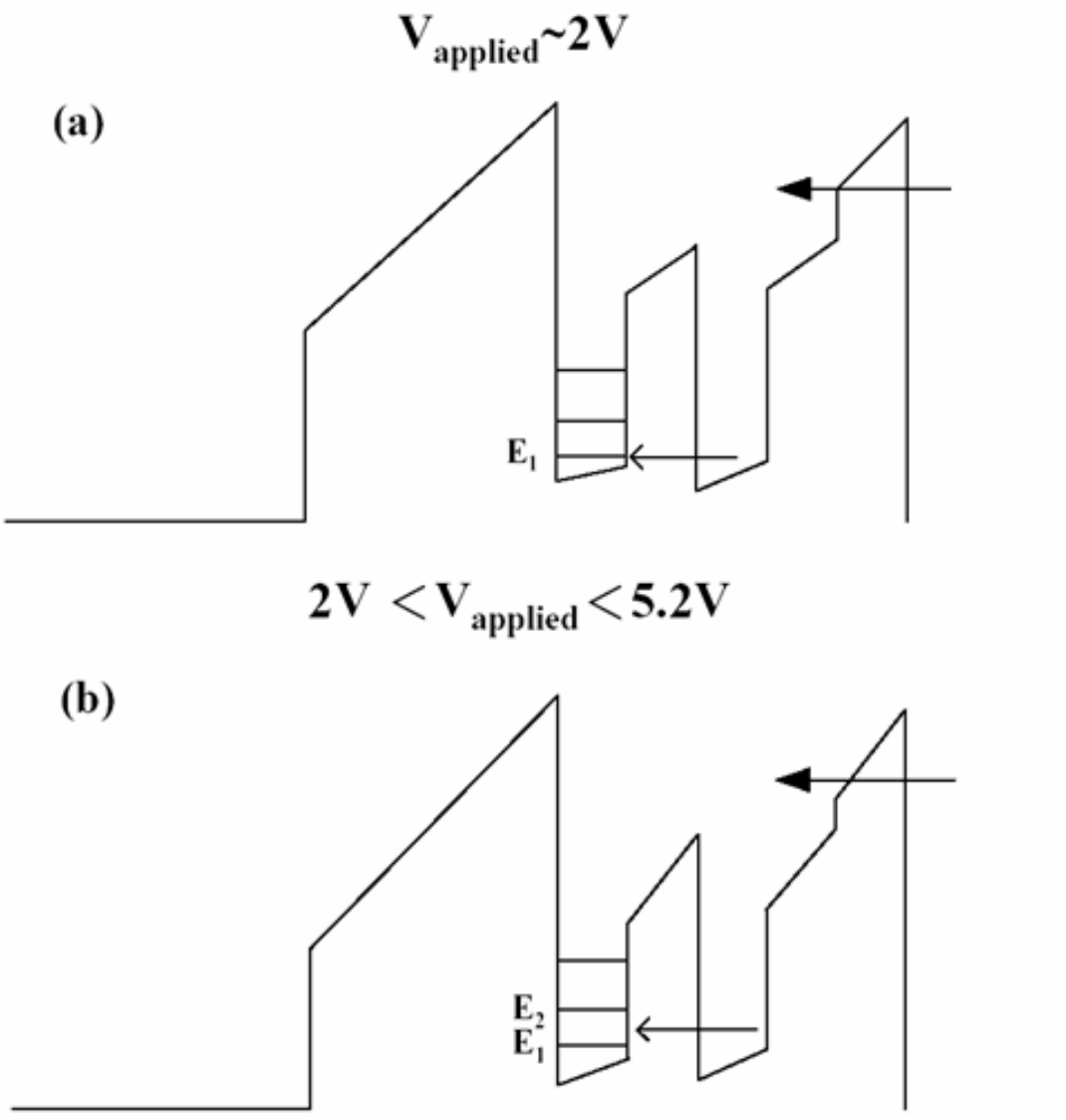

Figure 6-8 (a) The energy band diagram of resonant tunneling at around 2 V between the two a-Si layers (b) the band diagram for 2 V ＜ applied gate voltage ＜5.2 V.

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Conclusions

In this dissertation, the study on the advanced nonvolatile memory devices, including SONOS nonvolatile memory and nanocrystal nonvolatile memory devices, has been demonstrated. The study on SONOS nonvolatile memory technology using high-density plasma chemical vapor deposited silicon nitride was investigated. In addition, a new method of fabricating superior oxide/nitride/oxide gate stack is also demonstrated. The memory effect of oxide/SiC:O/oxide sandwiched structures was studied. Also, a novel distributed charge storage element fabricated by the oxidation of amorphous silicon carbide was also evaluated.

As for the nanocrystal memories, a novel approach of fabricating germanium nanocrystals for nonvolatile memory applications was presented. Additionally, the distributed charge storage with GeO_2 nanodots was demonstrated. Also, the electron charging and discharging effects of tungsten nanocrystals embedded in silicon dioxide for low-power nonvolatile memory technology were demonstrated. Finally, the Quasi-Superlattice Storage, a novel concept of multilevel charge storage, was presented. And the leakage behavior of the quasi-superlattice stack for multilevel charge storage was studied in this dissertation.

7.1.1 Study on SONOS Nonvolatile Memory Technology Using High-Density Plasma Chemical Vapor Deposited Silicon Nitride

With the replacement of silicon nitride in the oxide/nitride/oxide (ONO) gate-stacked structure, the trap-rich HDPCVD SiN_x shows a more significant threshold-voltage shift than that of the conventional LPCVD Si_3N_4. Also, the low-temperature (200℃) deposited HDPCVD silicon nitride shows a good retention characteristic the same as the high-temperature (780℃) LPCVD Si_3N_4. With the optimization of the thickness in the gate-stacked ONO structure, the low-voltage and reliable operation, lower than 5V, is realizable.

7.1.2 A New Method of Fabricating Superior Oxide/Nitride/Oxide Gate Stack

A superior ONO gate stack with a large memory window and high breakdown voltage was demonstrated. HDPCVD silicon nitride is deposited on the tunnel oxide followed by a high temperature dry oxidation to form a blocking oxide layer on the nitride layer. This ONO stack with densified nitride layer and thermally grown oxide layer on the silicon nitride exhibits a reliable and viable approach for SONOS nonvolatile memory technology.

7.1.3 Memory Effect of Oxide/Oxygen-Incorporated Silicon Carbide/Oxide Sandwiched Structure

The memory effects of the oxide/oxygen-incorporated silicon carbide (SiC:O)/oxide sandwiched structure were investigated. The memory window is

decreased with the increasing of the oxygen content in the SiC:O film due to the reduction of dangling bonds. A concise model is proposed to explain the reduction of dangling bonds with increasing oxygen content. Also, a higher breakdown voltage is observed with less oxygen content in the SiC:O film, which is attributed to the high barrier height induced by electron trapping in the SiC:O film.

7.1.4 Effectiveness of TMCS and HMDS Post-treatments

A novel distributed charge storage element fabricated by the oxidation of amorphous silicon carbide is proposed in this work. For low temperature oxidation processes, the oxidized SiCO gate stack shows larger memory window due to the retainable dangling bonds with more Si-C bonding types and less Si-O bonds. Under 5-V write operation of the low temperature oxidized SiCO stack, a 1.5-V threshold voltage shift is exhibited which is sufficient for a memory device to define "0" and "1". Also, the low temperature oxidation process of the SiCO layer saves the thermal budget for the manufacturing processes of nonvolatile memory devices.

7.1.5 A novel approach of fabricating germanium nanocrystals for nonvolatile memory applications

A nonvolatile memory device embedded with Ge nanocrystal dots is fabricated by the thermal oxidation of $Si_{0.8}Ge_{0.2}$ combined with a rapid thermal annealing at 950 ℃ in N_2 gas. The tunnel oxide in the nonvolatile memory is controlled to be 4.5 nm-thick and embedded with 5.5-nm Ge nanocrystals. A low operating voltage, 5V, is implemented and a significant threshold-voltage shift, 0.42V, is observed. When the electrons are trapped in the Ge nanocrystals, the effect of Coulomb blockade prevents

the injection and storage of more electrons and decreases the leakage current. Also, the retention characteristics are tested to be robust.

7.1.6 The distributed charge storage with GeO_2 nanodots

In this study, a distributed charge storage with GeO_2 nanodots is demonstrated. The mean size and aerial density of the nanodots embedded in SiO_2 are estimated to be about 5.5 nm and 4.3×10^{11} cm^{-2}, respectively. The composition of the dots is also confirmed to be GeO_2 by x-ray absorption near-edge structure analyses. A significant memory effect is observed through the electrical measurements. Under the low voltage operation of 5 V, the memory window is estimated to ~0.45 V. Also, a physical model is proposed to demonstrate the charge storage effect through the interfacial traps of GeO_2 nanodots.

7.1.7 Electron charging and discharging effects of tungsten nanocrystals embedded in silicon dioxide for low-power nonvolatile memory technology

The electron charging and discharging effects of tungsten nanocrystals embedded in the SiO_2 layer have been demonstrated in this study. Spherical and well-separated tungsten nanocrystals embedded in the SiO_2 layer are fabricated with a mean size and aerial density of 4.5 nm and $3.7\times10^{11}/cm^2$, respectively. The tungsten dots are formed by the thermal oxidation of the tungsten silicide. A significant C-V hysteresis of V_t shift of 0.95 V is observed and the endurance of the memory device is not degraded up to 10^6 write/erase cycles. The implementation in this study is compatible with the current manufacturing technology of semiconductor industry and represents a viable

candidate for low-power sub-100 nm nonvolatile memory nodes.

7.1.7 Quasi-Superlattice Storage (QS^2): A Novel Concept of Multilevel Charge Storage

In this work, a novel concept of the quasi-superlattice storage has been demonstrated for the first time. Under suitably operated voltage, two apparent states of charge storage can be distinguished. The memory effects are due to the multilevel charge storage within the quasi-superlattice. The multilevel charge storage provides a feasible design for the 2-bit-per-cell nonvolatile memory devices. Also, the leakage behavior of the quasi-suprlattice structure has also been characterized by current-voltage measurements at room temperature and low temperature. The resonant tunneling-like leakage characteristic is observed at low temperature. A concise physical model is proposed to characterize the leakage mechanism of tunneling for the quasi-superlattice structure and suggests that the considerations of operating voltage for the 2-bit per cell nonvolatile memory device need to be taken into account.

7.2 Suggestions for Future Work

There are a number of topics relevant to this thesis which deserves further studies. The following topics are suggested for future work.

(1) Further study on the reliability issues, such as endurance, retention, disturbs, and retention after write/erase cycles of the memory devices.

(2) Development of new methodology to improve the uniformity of metal or semiconductor nanocrystals.

(3) Investigation of the segregation of Ge nanodots in SiGeO and SiGeON films.

(4) Study on the fabrication methods using dry etching to fabricate Si, Ge, or/and metal nanodots.

(5) Investigation the memory effects of the SiC-based films such as SiCN and/or SiCON.

(6) Investigation of radiation hardness of the nanocrystal memory devices.

(7) Investigation of quantum confinement and opto-electronic effects of the nanocrystal memory device.

(8) Investigation of the formation of metal nanodots fabricated by the oxidation of metal silicide.

(9) Investigation of the memory effects of the metal oxide thin films and nanodots.

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Publication List

International Regular Journals：

[1] T. C. Chang, **S. T. Yan**, P. T. Liu, Z. W. Lin, H. Aoki, and S. M. Sze, "Extraction of Electrical Mechanisms of Low-Dielectric Constant Material MSZ for Interconnect Applications", *Thin Solid Films*, Vol. 447-448, January 30, pp. 516-523 (2004).

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International Conferences：

[1] T. C. Chang, **S. T. Yan**, P. T. Liu, Z. W. Lin, and S. M. Sze, "Electrical characteristics of low-dielectric constant material MSZ for interconnect applications", *International Electron Devices and Materials Symposium*, Taipei, Taiwan, p. 433-436, 2002.

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Patents:

1. "一種增進 SONOS 非揮發性記憶體元件記憶窗之製程方式", 中華民國及美國專利 (申請中)。
2. "一種形成奈米點記憶體的方法", 中華民國及美國專利 (申請中)。
3. "一種矽奈米點非揮發性記憶體的製作方法", 中華民國及美國專利 (申請中)。
4. "一種利用絕緣體作為 SOIOS 記憶體電荷儲存單元的方法", 中華民國及美國專利 (申請中)。
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6. "一種新的非揮發性記憶體電荷儲存單元製作方法", 中華民國及美國專利 (申請中)。
7. "一種多層結構的非揮發性記憶體電荷儲存單元", 中華民國及美國專利 (申請中)。

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