國立交通大學

電子工程學系 電子研究所

博士論文

應用高介電常數絕緣層與矽奈米微晶粒於超大型積體電路元件之研究

A Study of High-κ Dielectrics and Si Nano-crystals for ULSI Devices

研 究 生：陳 建 豪

指導教授：雷 添 福 博士
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研　究　生：陳建豪　　　　Student: Jian-Hao Chen

指導教授：雷添福 博士　　Advisor: Dr. Tan-Fu Lei
　　　　　趙天生 博士　　Dr. Tien-Sheng Chao

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摘要

Abstract (in Chinese)

本論文首先對於高介電常數鈷鈦酸(CoTiO$_3$)絕緣層穩定性的改善，提出三種摻雜氮的方法。利用氮氣分子(N$_2^+$)或原子(N$^+$)離子，以低能量植入鈷鈦金屬堆疊之中，接著進行氧化，利用電子顯微鏡與 X 光繞射(X-Ray Diffraction)方法均觀察到結晶狀態被氮摻雜抑制，電性量測亦證明了可以降低漏電，提高崩潰電壓，並在電壓加壓下有較佳穩定性。或利用一氧化二氮(N$_2$O)之電漿進行氮摻雜，先以較低的氧化溫度形成鈷鈦酸氧化物，接著進行一氧化二氮電漿處理，之後再經一道高溫熱退火步驟。我們發現以此方法可以有效改善鈷鈦酸絕緣層的熱穩定性，同時提升絕緣層的電性可靠度，絕緣層漏電可以降低大約 4 個數量級，而其崩潰電壓也可提高約 2 V。

本論文接著利用兩種新穎的矽前驅物(precursor)以金屬有機氣相沉積法製備高介電常數鉿的矽酸鹽。兩種矽前驅物分別是叔丁基二甲基矽醇(*tert*-butyldimethyl silanol)，與三叔戊氧基矽醇(tris(*tert*-pentoxy) silanol)。此論文研究的兩種矽前驅物在常溫常壓下為液態，因此可以提供足夠的蒸氣壓。兩種前驅物中，實驗發現三叔戊氧基矽醇此前驅物不需要氧氣介入反應即可生成矽酸鉿薄膜，而且可以在 250 °C 的低溫下生成平坦的矽酸鉿絕緣層。在此研究中，我們使用一組具備臨場(*in situ*)製程能力的高真空系統，沉積過程中利用臨場橢圓儀(Ellipsometer)觀察絕緣層成長，探討其成長機制，並利用臨場熱退火與電子能譜儀(XPS)研究薄膜材料特性。其後製作電容元件探討絕緣層之電特性，將薄膜結構變化與電特性比較。此絕緣層被製作成電容探討其電特性，在氫氮混和氣體

下(4 % H_2 + 96 % N_2)經過 450 °C 退火，絕緣層介面特性獲得良好的改善。

利用臨場製程系統，本論文接著研究矽奈米微晶粒的製備。使用電子束蒸鍍法可在薄氧化層上沉積均勻且平坦的超薄(0.9–3.5 nm)非晶矽層。隨後在未破壞真空的條件下進行臨場快速熱退火(850 °C, 5min)，可以形成自組裝半球狀矽奈米微晶粒。原子力顯微鏡，電子顯微鏡與電子能譜儀被使用於觀察晶粒結構。在較低溫度下(750 °C)可以觀察到未完成的奈米點聚合現象。奈米晶粒先在非晶矽表面成核，接著聚合成較大的晶粒並消耗周圍的非晶矽層，直到其底部與二氧化矽基底層接觸。較薄的非晶矽層可形成較小且較密的晶粒。此研究中得到最小的晶粒半徑約是 5.1 nm，同時亦得到最高的晶粒密度 3.9×10^{11} cm^{-2}。本論文亦利用臨場電子能譜觀測方法建立一套模型，以信號的強度估計矽奈米微晶粒的尺寸與密度，與實驗結果比較下，驗證出此方法十分具有實用性。

最後我們將此種新穎的半球狀矽奈米微晶粒製作成記憶體元件。製作矽奈米微晶粒於 4nm 之穿隧氧化層上，再覆蓋以 17 nm 之阻擋氧化層，製作完成之電容元件觀察到高的電荷儲存密度 4.1×10^{12} cm^{-2} (電子+電洞)。將此矽奈米晶粒製作成非揮發性記憶體元件可得到良好的記憶體特性。在±10 V，0.02/0.1 s 的閘極操作電壓下，可以得到約 0.9 V 之臨限電壓變化，在讀寫操作 10000 次之後亦保持住同樣的電壓記憶窗(memory window)。在±15 V 的操作下則可以得到約 2.8 V 的臨限電壓變化量，驗證此矽奈米微晶粒在記憶元件上之實用性。實驗證明這種真空聚合法形成之矽奈米晶粒可應用於非揮發記憶體的製作。

A Study of High-κ Dielectrics and Si Nano-crystals for ULSI Devices

Student: Jian-Hao Chen

Advisors: Dr. Tan-Fu Lei
Dr. Tien-Sheng Chao

Department of Electronics Engineering and Institute of Electronics
National Chiao-Tung University

Abstract

In this dissertation, three approaches to incorporating nitrogen in $CoTiO_3$ high-κ dielectric films, including the ion implantation of N_2^+, ion implantation of N^+, and N_2O plasma treatment, have been investigated. Nitrogen incorporation by ion implantation of N_2^+ can improve the electrical properties in terms of gate leakage, breakdown voltage and time-to-breakdown (T_{BD}). To reduce the impinging mass of implanted ion species, N^+ ion implantation has been used. The same trends can be found as those produced using N_2^+. A N_2O plasma treatment is also an excellent method to improve the electrical properties, exhibiting better-behaved C-V curves, lower gate leakage currents and higher breakdown voltages.

Two silanol precursors, *tert*-butyldimethyl silanol (BDMS) and tris(*tert*-pentoxy) silanol (TPOS), are evaluated as silicon precursors for hafnium silicate deposition with tetrakis-(diethylamido) hafnium (TDEAH). BDMS has one OH group, which should react with chemisorbed TDEAH. However, the other *t*-butyl and methyl groups can passivate the substrate surface, and stop the further absorption of TDEAH. Carbon-free hafnium silicate thin-films are deposited by MOCVD using alternative pulses of TDEAH and TPOS precursors. Hafnium silicates with high silicon contents ($Hf_{1-x}Si_xO_2$, $x > 0.5$) are deposited at 250 °C without additional oxidants. MOS capacitors are fabricated for electrical characterizations. A forming gas anneal can improve the hafnium silicate interface quality. This low-temperature process could be promising for TFT or optoelectronic applications.

Hemispherical Si nanocrystals are self-assembled using an *in-situ* thermal agglomeration technique. Ultrathin (0.9–3.5 nm) *a*-Si films are deposited on a 4-nm tunnel-oxide layer using electron-beam evaporation. An *in-situ* annealing can then activate the thermal agglomeration of Si and transform the ultrathin *a*-Si films into Si nanocrystals. The Si agglomeration process is evaluated with various processing parameters such as annealing temperatures, surface oxide conditions, and initial Si film thickness. Also, it is demonstrated that XPS measurements can effectively provide the information of the nanocrystal agglomeration. Calculations are made based on the photoelectron attenuation theories, and a simple model is proposed. Comparisons between the calculated results and the experimental data have shown a fairly good match.

The fabrication of a Si nanocrystal-embedded nonvolatile memory has been demonstrated using a thermal agglomeration technique. MOS capacitors and MOSFETs embedded with hemispherical Si nanocrystals are fabricated and characterized. A stored charge density of 4.1×10^{12} cm^{-2} (electron + hole) is obtained with a highest nanocrystal density of 3.9×10^{11} cm^{-2}. Uniform FN tunneling is used to program and erase the Si nanocrystal floating-gate n-MOSFETs. A V_t window of 0.9 V is achieved under P/E voltages of ±10 V for 0.02/0.1 s. The memory device also shows good endurance and charge retention behaviors after 10000 P/E cycles. Increasing P/E voltages to ±15 V creates a large memory window (>2.7 V) with the proposed memory device. After a retention test for 100 hours, a memory window of 1 V is maintained. The retention characteristics have shown little temperature dependence with the Si nanocrystal memories, indicating that the charge-loss process is determined by the direct tunneling from nanocrystals into the oxide/Si-substrate interface states.

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Chapter 1

Introduction

1.1 General Background

Significant progress in complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology has been made since the late 1980's. This was promoted by microelectronic revolution in which people's life style turned from a dream world into reality. However, in order to maintain this revolution, the industry has to solve several technological requirements that are related to performance and production cost. To satisfy the need of growing complexity of systems such as computer and multimedia devices, functionality in microprocessors and capacity in memory chips must be continuously expanded. According to Moore's law [1], an exponential growth in the number of transistors per very large scaled integration (VLSI) chip was predicted and has been proven true as shown at Figure 1.1 [2].

To maintain a competitive edge in the microelectronic business, a tremendous effort in reducing production costs is also required. These challenges have been overcome by scaling down the unit components in VLSI chips, the metal oxide semiconductor field effect transistor (MOSFET). Device scaling prompted consumer's increased demand to maximize performance and minimize production cost of VLSI chips, resulting in the acceleration of miniaturization in microelectronic devices. The International Technology Roadmap for Semiconductors (ITRS) predicts the scaling technology over the next 15 years and identifies technical challenges for the global semiconductor industry. According to ITRS 2005, several limitations to device scaling are being encountered in the sub-0.1 μm technology regime [3]. Gate dielectric thickness (*d*) for MOSFET is one of the most critical dimensions to be surmounted, and it is expected to reduce to less than 1 nm of *EOT* (Equivalent Oxide Thickness; equivalent SiO_2 gate thickness with corresponding dielectric performance) very soon.

One reason that Si-based devices have been dominant in microelectronic fabrication is that Si has a stable multi-functional oxide, SiO_2, easily produced by furnace oxidation or deposition. In spite of the excellent properties of SiO_2 as a gate dielectric material, such as high band gap energy, low interface defect density and stable oxide formation on Si, it exhibits a significant amount of tunneling leakage current when its thickness is scaled to below 2 nm [3-5]. This tunneling current produce noticeable power consumption at the standby condition of the device. Dynamic and passive power density (leakage power) trends shown in Figure 1.2 suggest that passive power consumption per unit gate area induced by gate tunneling current and sub-threshold current will continuously increase with device scaling and surpass active power density in several years [4].

Therefore, the replacement of SiO_2 with a high dielectric constant (*k*) material has been motivated for the deep sub-micron regime [6, 7]. High-*k* gate dielectric material can generate the equivalent charge in the channel region while allowing a sufficiently thick layer to be used. This will lead to a substantial reduction in tunneling leakage current.

Nitrogen incorporated SiO_2 has already replaced SiO_2 for more than 3 years in advanced devices with *EOT* of sub-3 nm. Silicon oxy-nitride is, however, regarded as a temporary solution until the reliability of high-*k* gate dielectric material is completely verified at the 1 nm-*EOT* device, because of the limitation in scalability as shown in Figure 1.3 [8]. The implementation of high-*k* gate dielectrics is expected to be a must for the after the silicon oxy-nitride reaches its limit.

Because of the fast development of IC technology, the consumer electronic products have become more affordable and been widely adopted. People have been more and more relying on digitalized mobile devices, for example the cell phones, digital cameras, and PDAs. In the needs of running digitalized electronic devices and data storage, semiconductor memory devices have become important components [9]. While the portable devices quickly summon a huge popularity, low-cost large-volume nonvolatile memories are eagerly needed by the users for their office documents, research data, high-resolution photos and newest music, among all the other digitalized information to be kept. Nonvolatile memory devices can keep their final electrical states without continuous power supply. Therefore they reduce the power consumption of portable devices, which leads to a longer operation time between recharging. Just like the CMOS logic IC, the nonvolatile memory devices also need to be down-scaled to increase the storage volume per chip and reduce the cost of ownership.

Conventional polycrystalline-silicon-based floating-gate (FG) nonvolatile memory devices use a single FG layer to store charges [9]. However, the data reliability is strongly limited by the isolation oxide quality. One charge leakage path created in the isolation oxide can discharge the entire FG and cause a fatal data loss. Therefore it is critical to maintain the oxide robustness, which casts difficulties in scaling the oxide thickness. In recent years, nanocrystal-based memory devices have drawn great attention due to their scaling advantages over the conventional nonvolatile memories [10]. The nanocrystal memory device has many discrete nanocrystal dots as distributed storage nodes. A local leaky path can only affect a few storage nodes (dots) near it, which prevents a serious charge loss. Therefore, nanocrystal floating-gate memories can alleviate the tunnel-oxide scaling issues and as a result, enhance the device operating speeds with thin tunnel-oxide layers [10].

1.2 Motivation

Nitrogen incorporation in $CoTiO_3$ gate dielectrics

According to recent reports [11-25], optimized treatments which incorporate nitrogen have resulted in a significant improvement in the high-κ dielectric properties. Nitridation of the silicon surface can reduce the growth of an interfacial layer. Plasma nitridation after deposition of the high-κ dielectric can recover the degraded mobility. The advantages of nitrogen incorporation are the increase of the κ-value, the increase of the temperature of crystallization, the reduction of the leakage, reasonable V_{FB}, and reduced boron penetration [11-24].

The material and electrical properties of $CoTiO_3$ high-κ dielectrics have been investigated in earlier reports [26, 27]. In present work, nitrogen incorporation using N_2^+/N^+ ion implantation or N_2O plasma treatment to improve this $CoTiO_3$ films are investigated. It is found that the nitrogen incorporation using either ion implantation or plasma treatment can significantly improve the electrical performance of $CoTiO_3$ high-κ dielectrics.

Hf-silicate gate dielectrics deposited by MOCVD

HfO_2 crystallizes at low temperatures and it is desirable to find a gate dielectric which remains amorphous during device processing where temperatures can reach as high as 1050 °C [28]. Increasing the Si concentration in hafnium silicate increases the crystallization temperature and the silicon/dielectric barrier height but reduces the dielectric constant. It has been estimated that SiO_2 mole fractions, $([SiO_2]/([SiO_2]+[HfO_2]))$ will be required to be > 75 mol% to avoid phase separation and crystallization [29] and films with 81 mol% SiO_2 were shown to be amorphous and thermally stable in a silicon-capped structure upon heating to 1050 °C [30]. The incorporation of nitrogen reduces significantly the required mole fraction of SiO_2 [31] but it remains to be demonstrated that such high N concentrations can be incorporated without introducing other electrical defects [32].

Gordon *et al*. [33] have shown that tetrakis-(diethylamido) hafnium (TDEAH) can be used with tris(*t*-butoxy)silanol (TBOS) to produce Hf silicate by atomic layer deposition (ALD) and surmised that similar reactions would occur between other alkylamides and tris(*t*-alkoxy) silanols. Deposition rates, higher than expected from a bulky precursor like TBOS, were reported along with SiO_2 mole fractions as high as 75 mol%. This was explained by a mechanism that involves the absorption of two TBOS molecules for each molecule of the alkylamide [34]. However, TBOS is difficult to use because it is a solid at room temperature with a vapor pressure of ~15 Torr at 115 °C [35].

In this work, we report the use of two novel silanol precursors for metal-organic chemical vapor deposition (MOCVD) and ALD with TDEAH. Both silanol precursors are liquids at room temperature and were vaporized using a simple bubbler. The first, *t*-butyldimethyl silanol (BDMS), has been used to produce low silica content hafnium silicate films by MOCVD [36]. The second, tris(*t*-pentoxy) silanol (TPOS), is an analogue of TBOS but with a higher vapor pressure. In fact, TBOS is a solid at room temperature which melts at 63-65 °C and boils at 205-210 °C while TPOS is a liquid which boils at 96-99 °C (at 2.5 Torr).

Self-assembled Si nanocrystals

The surface coalescence of *a*-Si during an ultra-high vacuum (UHV) annealing was first observed by Sakai *et al* [23]. The growth of hemispherical grained (HSG) Si islands on the *a*-Si surface was explained by the segregation of diffusive Si atoms around surface nucleation centers [23]. Since then the resulted HSG structure has been widely adopted in the dynamic random-access-memory (DRAM) devices [37] to enhance their capacitive charge-storage densities [38]. Recent studies by Akazawa have suggested that, after a long annealing time (3 hours), the growth of HSG Si would saturate, and a self-limiting, highly-uniform size distribution could be obtained regardless of the annealing temperature [39, 40].

In this study, Si nanocrystals fabricated by the thermal agglomeration technique are investigated. Ultrathin *a*-Si layers are deposited on a thin tunnel-oxide layer and then annealed *in situ* using a rapid thermal annealing (RTA) setup under UHV. The *a*-Si deposition and the thermal agglomeration behaviors are monitored by an *in-situ* x-ray photoelectron spectroscopy (XPS) machine. The surface morphology and the nanocrystal structures are analyzed by atomic force microscopy (AFM), scanning electron microscope (SEM), and transmission electron microscope (TEM). A theoretical model is then established to fit the *in-situ* XPS results and estimate the agglomerated dot size and density.

Nonvolatile memories with hemispherical Si-nanocrystal floating gates

In this chapter, Si-nc nonvolatile memory devices are fabricated using a thermal agglomeration technique. Si islands have been produced by annealing ultrathin *a*-Si [41-43] or silicon-on-insulator (SOI) [23, 37, 44-47] films under UHV conditions. It is suggested that the surface energy instabilities play an important role in the thermal agglomeration, or de-wetting, of the ultrathin films. A thermodynamic model based on the calculation of surface energy has been developed by Danielson *et al.* [48], in which the agglomeration instabilities observed in ultrathin SOI films were discussed. The general implications of their surface-energy-driven de-wetting theory are also suitable to explain the agglomeration behavior of *a*-Si thin films and the nanocrystal formation. Although theoretical studies have provided insights of the agglomeration mechanism [42, 48], the electrical characterizations of such agglomerated Si dots are still lacking.

In this study, ultrathin *a*-Si films are deposited using electron-beam evaporation and then annealed *in situ* under UHV. Hemispherical Si nanocrystals are obtained through the thermal agglomeration process. The nanocrystals are formed on a thin tunnel-oxide layer and then covered by a control-oxide layer. Memory devices including metal-oxide-semiconductor (MOS) capacitors and field effect transistors (MOSFETs) are fabricated with the embedded Si-nanocrystal floating gates. Their electrical characteristics are investigated. This thermal agglomeration method is considered compatible with the conventional top-down process because the ultrathin *a*-Si film can be patterned prior to the vacuum annealing. In between the *ex-situ* processing and the vacuum annealing, however, the *a*-Si surfaces need to be cleaned and kept free of native oxide in order to ensure the Si agglomeration.

1.3 Organization of the Thesis

In chapter 1, the general background and the research motivation of the dissertation are reviewed and elucidated.

In chapter 2, the experimental apparatuses are introduced. The MOCVD system used to deposit high-κ gate dielectrics is described. Meanwhile, XPS, TEM, and MEIS employed for physical analysis are discussed. The setting of electrical analysis is also included.

In chapter 3, three approaches to incorporating nitrogen in $CoTiO_3$ high-κ dielectric films, including the ion implantation of N_2^+, ion implantation of N^+, and N_2O plasma treatment, have been investigated. Nitrogen incorporation by ion implantation of N_2^+ can improve the electrical properties in terms of gate leakage, breakdown voltage and time-to-breakdown (T_{BD}). To reduce the impinging mass of implanted ion species, N^+ ion implantation has been used. The same trends can be found as those produced using N_2^+. A N_2O plasma treatment is also an excellent method to improve the electrical properties, exhibiting better-behaved C-V curves, lower gate leakage currents and higher breakdown voltages.

In chapter 4, two silanol precursors, BDMS and TPOS, are evaluated as silicon precursors for hafnium silicate deposition with TDEAH. BDMS has one OH group, which should react with chemisorbed TDEAH. However, the other *t*-butyl and methyl groups can passivate the substrate surface, and stop the further absorption of TDEAH. Carbon-free hafnium silicate thin-films are deposited by MOCVD using alternative pulses of TDEAH and TPOS precursors. Hafnium silicates with high silicon contents ($Hf_{1-x}Si_xO_2$, x >0.5) are deposited at 250 °C without additional oxidants. MOS capacitors are fabricated for electrical characterizations. A forming gas anneal can improve the hafnium silicate interface quality. This low-temperature process could be promising for TFT or optoelectronic applications.

In chapter 5, hemispherical Si nanocrystals are self-assembled using a thermal agglomeration technique. Ultrathin (0.9–3.5 nm) *a*-Si films are deposited on a 4-nm tunnel-oxide layer using electron-beam evaporation. XPS analysis has verified a layer-by-layer deposition mode for the *a*-Si film. After the deposition, an *in-situ* annealing can activate the thermal agglomeration of Si and transform the ultrathin *a*-Si films into Si nanocrystals. The Si agglomeration process is evaluated with variables such as annealing temperatures, surface oxide conditions, and initial Si film thickness. Also, it is demonstrated that XPS measurements can effectively provide the information of the nanocrystal agglomeration. Calculations are made based on the photoelectron attenuation theories [49], and a simple model is proposed. Comparisons between the calculated results and the experimental data have shown a fairly good match. Therefore the nanocrystal features can be reasonably estimated by this model using *in-situ* XPS measurements.

In chapter 6, the fabrication of a Si nanocrystal-embedded nonvolatile memory has been demonstrated using a thermal agglomeration technique. MOS capacitors and MOSFETs embedded with hemispherical Si nanocrystals are fabricated and characterized. A stored charge density of 4.1×10^{12} cm^{-2} (electron + hole) is obtained with a highest nanocrystal density of 3.9×10^{11} cm^{-2}. Uniform FN tunneling is used to program and erase the Si nanocrystal floating-gate n-MOSFETs. A V_t window of 0.9 V is achieved under P/E voltages of ±10 V for 0.02/0.1 s. The memory device also shows good endurance and charge retention behaviors after 10000 P/E cycles. Increasing P/E voltages to ±15 V creates a large memory window (>2.7 V) with the proposed memory device. After a retention test for 100 hours, a memory window of 1 V is maintained. The retention characteristics have shown little temperature dependence with the Si nanocrystal memories, indicating that the charge-loss process is determined by the direct tunneling from nanocrystals into the oxide/Si-substrate interface states.

Finally, the important experimental results of each chapter are summarized in chapter 7. Some thoughts and suggestions for future research work are also provided.

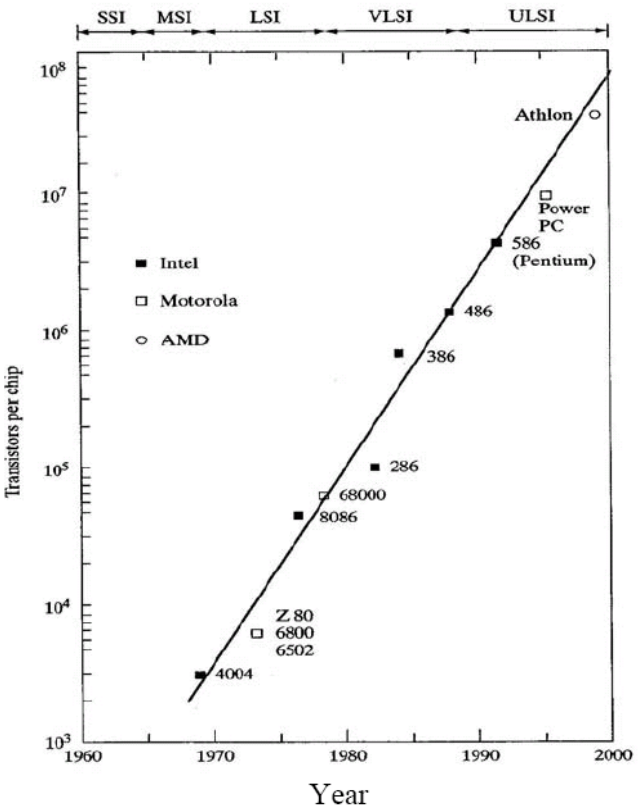


Fig. 1.1 Moore's law for microprocessors. Exponential increase of transistor counts as a function of time for generations of microprocessors has been substantiated [2].

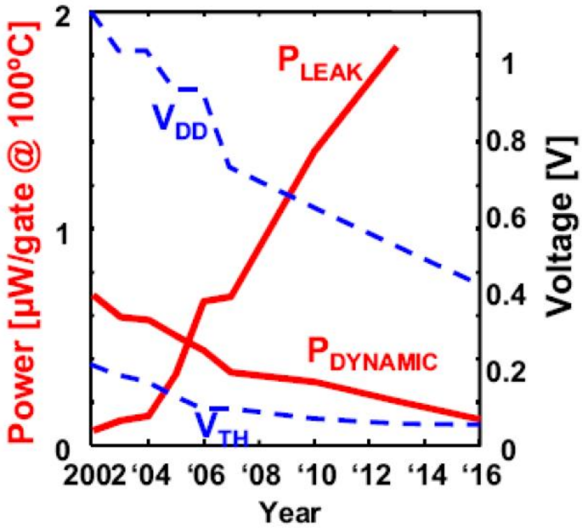


Fig. 1.2 Estimated voltage (V_{dd} : input voltage / V_{th} : threshold voltage) and power consumption (P_{LEAK} : power induced by leakage current / $P_{DYNAMIC}$: dynamic power consumption) trends. All parameters are taken from ITRS 2001 [4].

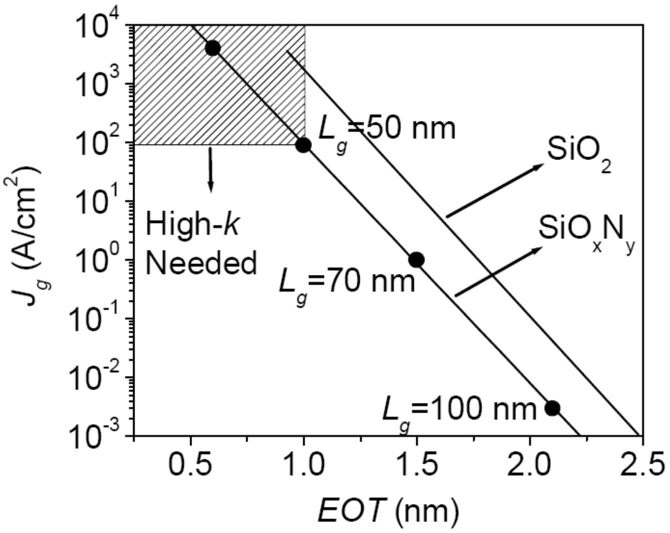


Fig. 1.3 Gate leakage current density (J_g) versus equivalent oxide thickness (EOT) of the SiO_xN_y and SiO_2 gate dielectrics [8]. Corresponding gate channel lengths of the data points (L_g) are marked.

Chapter 2

Experimental Techniques

2.1 Ultrahigh Vacuum *in-situ* Processing (ISP) System

An ultra-high vacuum (UHV) system is essential for the surface study on ultra-thin films, because surface reaction is mostly affected by gas exposure. 100 mm Si(100) wafers were used as substrates for the Hf silicate depositions and for the Si nanocrystal agglomeration experiments. Normally samples were prepared by a standard HF-last RCA clean prior to insertion into an UHV multi-chamber *in-situ* processing (ISP) system depicted in Figure 2.1.

The UHV system consists of an entrance load-lock, an MOCVD chamber, an *in-situ* XPS chamber, a chamber for *in-situ* high vacuum rapid thermal annealing and Si e-beam evaporation, and a metal evaporator chamber. All working chambers are separated by three high vacuum tunnels and the CVD and e-beam evaporation chambers have ion-pumped buffer chambers. The vacuum of the UHV system is maintained at the level of 10^{-10} Torr by ion pumps. Deposition processing, post-deposition treatments, and XPS analysis can be done without any vacuum break.

2.2 Metal Organic Chemical Vapor Deposition (MOCVD)

The hafnium precursor used for this work is tetrakis (diethylamido) hafnium (TDEAH, $[(C_2H_5)_2N]_4Hf$) with a chemical structure illustrated in Figure 2.2. Hf metal is bonded with four nitrogen atoms that have two ethyl radicals. No oxygen is contained in this precursor, but nitrogen in it. This nitrogen is expected to incorporate into the high-*k* film during CVD growth.

Figure 2.3 shows the schematic structure of the MOCVD system. The TDEAH precursor dissolved in octane with the concentration of 0.1 M was introduced into the reactor with a liquid injection system (LDS-300B produced by ATMI). The liquid injection system pumped the liquid solution through a nickel frit into the vaporizer of which temperature was held at 140 °C. The precursor was pumped at a rate of 0.2 ml/min (the lowest stable flow rate in our system) and carried by 50 sccm of Ar through the vaporizer. The other gases (N_2 and O_2) or precursors (BDMS or TPOS) were introduced into a separate gas distribution ring. The hafnium silicates were grown by pulse-mode deposition in which each deposition cycle consists of several steps controlled by solenoid valves. Gas flows were controlled by mass flow controllers present just before the gas inlet into the CVD chamber. The Si precursors were introduced by delivering the carrier gas (N_2) through a heated bubbler containing the precursor. The total deposition pressure was in the range 3-11 mTorr where gas-phase collisions were rare. The sample stage temperature was controlled with a quartz-halogen heater-thermocouple combination. The base pressure of the MOCVD chamber was around 10^{-9} Torr.

2.3 Material Characterization Techniques

2.3.1 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) was used to characterize the chemical bonding and film composition. Since the photon energy range of interest for material analysis corresponds to the x-ray energy (1-10 keV), photoelectron spectra with specific binding energies produced by x-ray radiation of a sample present chemical bonding information about given elements. Figure 2.4 shows relevant energy levels for XPS measurements [50]. Binding energies of photoelectrons can be obtained from Equation (2.1), based on Figure 2.4.

$$E_{kin} = hv - E_b - \O_{spec}, \tag{2.1}$$

where E_{kin} is kinetic energy of the photoelectron, h is Plank's constant, v is the frequency of the photon, E_b is the binding energy, and $\O_{spec}$ is the work-function of the spectrometer.

The *in-situ* XPS system is a PHI 5000 instrument with a non-monochromatic Mg $K\alpha$ X-ray (hv = 1253.6 eV) source in the standard 54 ° geometry (X-ray source 9 ° off-normal and the electron spectrometer 45 ° off normal). The pass energy for XPS survey spectra is 117.4 eV, and that for multiplex is 46.95 eV. Films were also analyzed *ex-situ* by XPS depth profiling using a PHI 5500 system with a mono chromatic Al $K\alpha$ X-ray (hv = 1486.6 eV) source in standard 90 ° geometry (X-ray source and electron spectrometer 45 ° off normal). Depth profiling was performed with intermittent Ar^+ sputtering at 4 keV or 1 keV, 50 nA and 45 ° incidence. The peak positions were referenced to the substrate Si $2p_{3/2}$ peak at 99.3 eV or C 1s from atmospheric contamination at 284.8 eV [51, 52]. *In-situ* XPS was used to determine chemical bonding and compositions of the films using standard sensitivity factors of O, N, Hf for the O 1s, N 1s, and Hf 4f peaks, respectively, which were obtained from the empirical data of the spectrometer equipped with an Omni Focus III lens supplied by Perkin-Elmer.

2.3.2 High Resolution Transmission Electron Microscopy (HRTEM)

HRTEM was utilized for structural analysis. Cross-sectional bar shaped samples were taken from the wafer and glued together surface-to-surface. The sample is cut and placed into a 3 mm – diameter titanium disk, and then dimpled from both sides with 3 μm diamond paste until the center of the disc is ~20 μm thick. Polishing with 1 μm diamond paste follows to get a smooth surface. The final step in sample preparation is a low-angle ion milling with a beam-energy of 6 keV for perforation. A Philips EM-430T microscope was used. The maximum electron beam energy and magnification is 300 keV, and ×650000 respectively and the corresponding point resolution is 0.228 nm. A JEOL 2100F TEM/STEM with a Schottky field emission gun was also used. This microscope is operated at 200 keV and equipped with a Gatan Tridiem energy filter for electron energy loss spectroscopy (EELS) analysis and an Oxford Instrument energy dispersive spectrometer (EDS). An annular dark-field (ADF) imaging and spatially resolved spectroscopy were performed with a scanning transmission electron microscope (STEM) probe size of approximately 0.2-0.3 nm. Figure 2.5 shows a schematic view of a STEM system equipped with EDS and EELS.

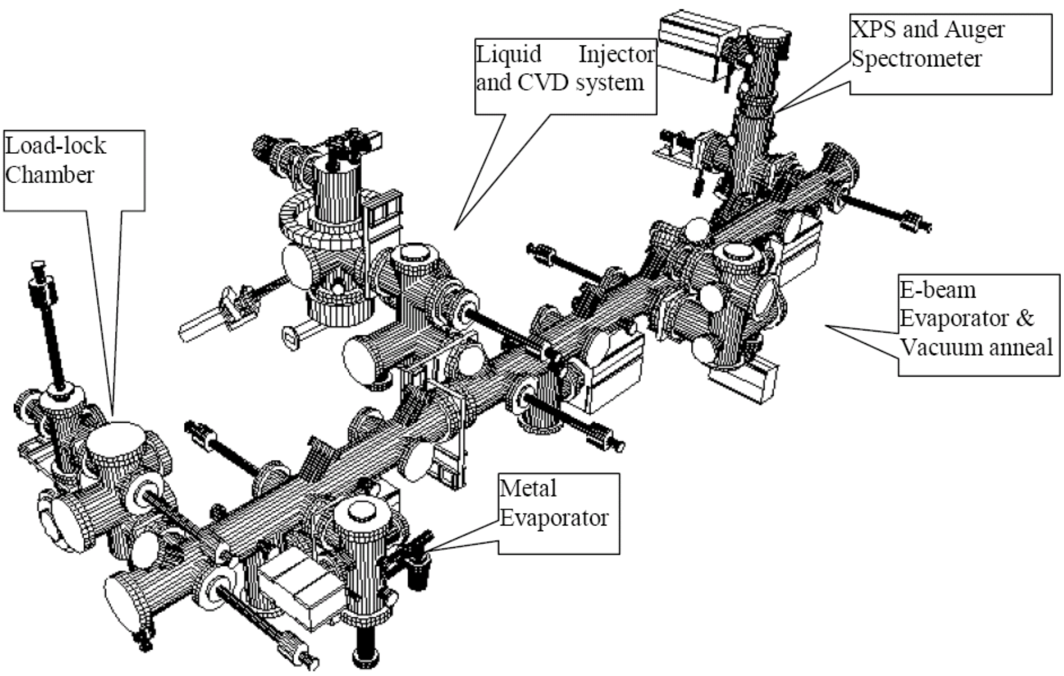


Fig. 2.1 UHV processing facility for 4 inch wafer.

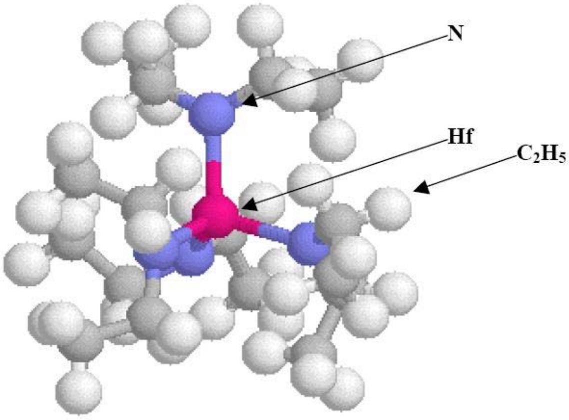


Fig. 2.2 Chemical bonding structure of the tetrakis diethyl-amido hafnium (TDEAH) precursor.

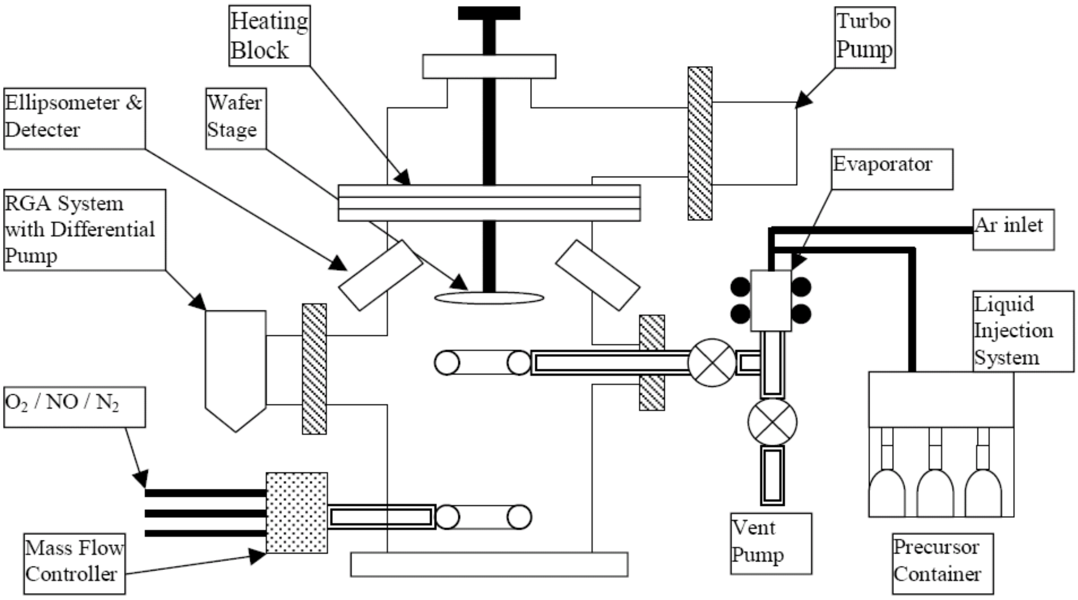


Fig. 2.3 Schematic view of MOCVD system.

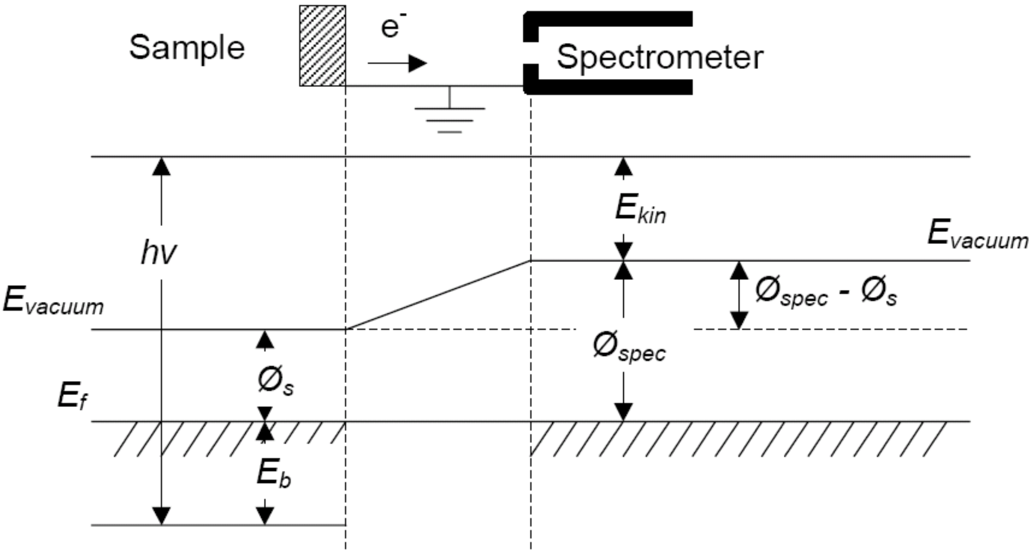


Fig. 2.4 Schematic of the relevant energy levels for XPS binding energy measurements. E_{kin} is kinetic energy of the photoelectron, h is Plank's constant, v is the photon frequency, E_b is the binding energy, $Ø_s$ is the work-function of the sample, and $Ø_{spec}$ is the work-function of the spectrometer. Note that a conducting specimen and spectrometer are in electrical contact and thus have common Fermi levels. Kinetic energies of photo-ejected electrons are given by Equation (2.1) [50].

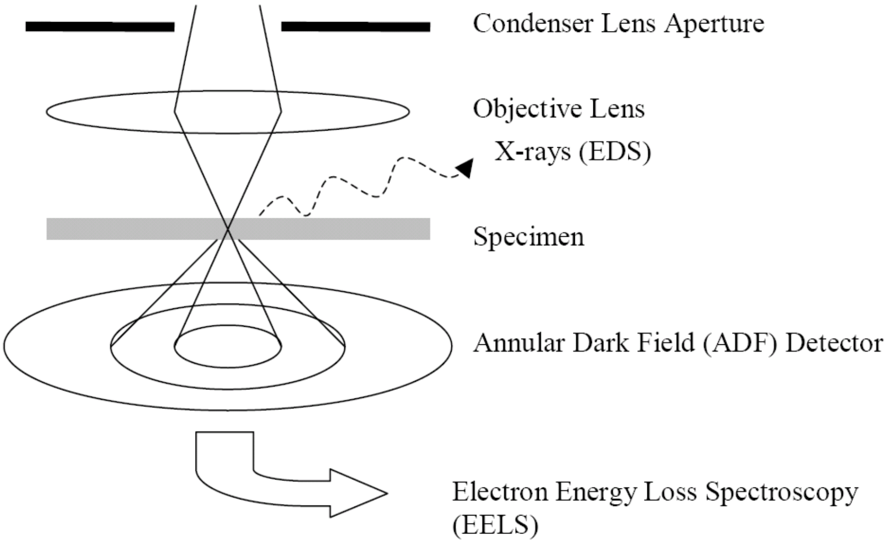


Fig. 2.5 Schematic view of the STEM system equipped with EDS and EELS.

Chapter 3

Performance Improvement of CoTiO3 High-κ Dielectrics with Nitrogen Incorporation

3.1 Introduction

The thickness of the conventional silicon dioxide (SiO_2) gate dielectrics has been scaled down to around 1.5 nm to meet the high drive requirements of high-performance (CMOS) [53]. The most serious problem we face today for this ultrathin gate dielectric is the huge gate leakage due to the direct tunneling of carriers from the channel of metal oxide semiconductor field-effect transistors (MOSFET)s [54], which reduces the transconductance of devices, and increases the standby power. This is not adequate for low-power applications in portable equipment. For a long time, high dielectric constant (high-κ) gate materials such as Si_3N_4 [55, 56], Al_2O_3 [57-59], HfO_2 [60-62], and ZrO_2 [63-65] have been proposed to replace the conventional ultrathin SiO_2 to solve this problem. For the same equivalent-oxide-thickness (EOT), the thickness of high-κ gate dielectrics can be increased many times. Hence, the direct tunneling current can be significantly reduced. The choice of high-κ material is based on the following requirements:

1. The κ-value should be in the range 20–50, as high as possible but low enough to avoid the fringing-induced barrier lowering effect in sub-100-nm n-MOSFETs [66].
2. The bandgap energy should be larger than 4.5 eV and barrier height larger than 1 eV to avoid increased leakage current at elevated temperature [67, 68].

3. The interface state density should be less than 10^{11} cm^{-2} eV^{-1} to maintain a well-behaved sub-threshold characteristic.
4. Low trap densities are required in the film to avoid Frankel-Poole tunneling.
5. The dielectric should have good thermal stability during the high-temperature processing.
6. It should have high breakdown voltage, low-leakage, and small hysteresis.

In previous work, a new high-κ dielectric $CoTiO_3$ has been proposed for application in MOSFETs and dynamic random access memories (DRAMs) [38]. The dielectric constant for this $CoTiO_3$ with the bottom oxide layer can be as high as 50, which makes this high-κ dielectric become very promising after the current medium κ value (15–25) materials, such as HfO_2 and ZrO_2, have reached their useful limit. However, some issues still remain when high-κ materials are used. The most important issues are:

1. The interfacial layer of SiO_2 or silicate remaining after deposition of high-κ materials.
2. The high fixed charge in the bulk of high-κ dielectrics which results in flat-band voltage (V_{FB}) shifts.
3. The degradation of mobility.
4. A low crystallization temperature.
5. Boron penetration for p-MOSFETs.

According to recent reports [11-25], optimized treatments which incorporate nitrogen have resulted in a significant improvement in the high-κ dielectric properties. Nitridation of the silicon surface can reduce the growth of an interfacial layer. Plasma nitridation after deposition of the high-κ dielectric can recover the degraded mobility.

The advantages of nitrogen incorporation are the increase of the κ-value, the increase of the temperature of crystallization, the reduction of the leakage, reasonable V_{FB}, and reduced boron penetration [11-24]. The material and electrical properties of $CoTiO_3$ high-κ dielectrics have been investigated in earlier reports [26, 27]. In present work, nitrogen incorporation using N_2^+/N^+ ion implantation or N_2O plasma treatment to improve this $CoTiO_3$ films are investigated. It is found that the nitrogen incorporation using either ion implantation or plasma treatment can significantly improve the electrical performance of $CoTiO_3$ high-κ dielectrics.

3.2 Experimental

Capacitors were fabricated on n-type 150 mm Si(100) wafers with a resistivity of 2-7 Ω-cm. After the growth of a 550 nm thick field oxide, the active region of capacitors were defined and etched by buffered oxide etch (BOE, NH_4F: HF = 6:1). Wafers underwent a standard RCA cleaning process and were put into the low-pressure chemical vapor deposition (LPCVD) tube in a pure NH_3 ambient to grow an ultra-thin nitride ~1.0 nm thick on the Si-surface. The thickness of the nitride was measured by Ellipsometry. The purpose of this NH_3-grown ultrathin nitride film is to prevent the reaction of the following sputtered Ti and then Co (Co/Ti) metal films, and also to retard the oxidation of silicon during the oxidation of Co/Ti layer. The Co (5 nm) and Ti (5 nm) films were deposited by sputtering at a power of 500 W and a sputtering rate of 0.9 nm/sec. Then wafers underwent the N_2^+ or N^+ ion implantation. To avoid the nitrogen penetration through the metal films and to reduce damage of the metal films, low ion energy of 10 keV was used with nitrogen doses of 2×10^{14} and 2×10^{15} atom/cm^2. Wafers were then oxidized in a furnace using flows of 5000 sccm each of O_2 and N_2. Splits were done for oxidation temperatures of 800, 850 and 900 °C, and the oxidation time was 10 min.

Some wafers without nitrogen implantation underwent N_2O plasma treatment in a plasma enhanced chemical vapor deposition (PECVD) system. The flow rate of N_2O was 60 sccm, the temperature was 350 °C, the power was set at 10, 15, or 20 W, and the processing time was 5 minutes. The purpose of this N_2O plasma treatment is to passivate the oxygen vacancies in the bulk film, and also to incorporate nitrogen in the dielectrics. Then the plasma-treated samples (and the untreated control sample as well) went through an additional rapid thermal annealing (RTA) at 880 °C for 40 seconds in N_2 ambient. This RTA step was aimed to repair any plasma-induced damages in the $CoTiO_3$ dielectrics. The top electrode for electrical measurements was a 500 nm Al film which was deposited by physical vapor deposition (PVD). The capacitance-voltage (C-V) curves of the capacitors were measured with an HP 4284A impedance meter at 100 kHz. The areas of the capacitors were 2.5×10^{-5} cm^2 (50 × 50 μm) and 1×10^{-4} cm^2 (100 × 100 μm). The current-voltage (I-V) curves were measured using an HP 4156A semiconductor parameter analyzer. The physical properties of $CoTiO_3$ high-κ dielectrics with and without nitrogen incorporation were analyzed by transmission electron microscopy (TEM), secondary-ion mass spectrometry (SIMS), and x-ray diffraction (XRD).

3.3 Results and Discussion

A. N_2^+ Ion Implantation

The thickness of all $CoTiO_3$ samples was first measured by TEM. Figures 3.1(a) and (b) show one set of the TEM pictures for samples of $CoTiO_3$ oxidized at 800 °C for 10 min without and with nitrogen ion implantation, respectively. The physical thickness of both samples was in the range 24–25 nm. It was observed that the oxidation of the Co/Ti films increases the thickness of the interfacial layer. This indicates that the ultrathin nitride film was not thick enough to retard the diffusion of oxygen. Compared with the sample without nitrogen implantation, smaller grains and a less diffuse boundary profile between high-κ and interfacial layers were found for the N_2^+-implanted sample. C-V curves at a high frequency of 100 kHz are shown in Fig. 3.2. The C-V curve of the sample oxidized at 800 °C for 10 min without nitrogen implantation was not obtained due to a large leakage current during measurement. This may be due to the non-fully oxidized Co/Ti in the bulk of dielectrics at lower temperature for a short oxidation time of 10 min. It is found that the capacitance C_{ox} in the accumulation region decreases with the increasing oxidation temperature, which is due to the abundant oxygen incorporation during the oxidation step. The extracted equivalent-oxide-thickness (EOT), interfacial silicate thickness, high-κ dielectric thickness, total thickness, effective κ-value and flat-band voltage are summarized in Table 3.1. The existence of interfacial layers degrades the effective κ-value. However, the intrinsic bulk dielectric constant for $CoTiO_3$ has been estimated using the same processes [38]. The intrinsic bulk dielectric constant was estimated as high as 50 [38], excluding the interfacial layer. It is found that the EOT increases as the oxidation temperature increased. As a result, the effective κ-value deduced from the C-V results and TEM measurements decreases as the temperature is increased. The flat-band voltage shifts to a negative value for the sample oxidized at 900 °C with nitrogen implantation. This may be due to nitrogen diffusion into the interfacial layer which creates positive charges in the film.

Figure 3.3 shows the electrical properties of samples oxidized at 900 °C for 10 min. Figure 3.3(a) shows that capacitors with nitrogen ion implantation exhibit a lower leakage current and a higher breakdown voltage. This phenomenon is the same for samples oxidized at 800 and 850 °C. Figure 3.3(b) shows the Weibull distribution of gate leakage currents at V_g = 1 V. Capacitors with nitrogen implantation have a tighter distribution and smaller leakage currents than those without. Figure 3.3(c) shows the Weibull distribution of breakdown voltages. Once again, the capacitors with nitrogen implantation have higher breakdown voltages.

The samples with and without nitrogen implantation are also subjected to a constant-voltage (V_g = 2V) stress, and the results are shown in Figures 3.4(a) and (b). For the capacitors without nitrogen implantation, a significant increase of gate leakage was found after stressed for 100 s, as shown in Fig. 3.4(a). On the other hand, the samples with nitrogen implantation exhibited no significant increase in gate leakage currents, as shown in Fig. 3.4(b), when compared to those without nitrogen implantation.

Figure 3.5 shows the x-ray diffraction spectra for a $CoTiO_3$ film oxidized at 850 °C with and without nitrogen implantation. For the sample without nitrogen implantation, a clear peak intensity was found around 34° for the $CoTiO_3$ (311) phase. However, the peak is not so clear for the sample with nitrogen implantation. This implies that the nitrogen implantation of the Co/Ti films can retard the crystallization of $CoTiO_3$.

B. N^+ Ion Implantation

To reduce the possible damages caused by the nitrogen ion implantation, two approaches can be adopted. The first approach is to reduce the mass of implanted species by using N^+ ions instead of N_2^+. Figure 3.6(a) shows the result. The oxidation temperature was 850 °C with a reduced oxidation time of 5 min. This can reduce the oxygen encroachment during the high temperature oxidation. The leakage current decreased as the nitrogen dose increased. The Weibull distributions of gate leakage currents and breakdown voltages are shown in Figures 3.6(b) and (c), respectively. It can be seen that high nitrogen doses improve the electrical properties of the capacitors.

C. N_2O Plasma Treatment

The second approach to avoid the damage from ion implantation is generally to use the N_2O plasma treatments [69, 70] or post-deposition annealing (PDA) in nitrogen-related ambient, such as N_2, NO, N_2O , or NH_3 [71, 72]. In present study, the N_2O plasma treatment (at powers of 10, 15, and 20 W) was applied after the oxidation step. Some samples without nitrogen ion implantation underwent the N_2O plasma treatment before the gate-metal deposition. This treatment can passivate the oxygen vacancies (by oxygen radicals in N_2O plasma) in the dielectric bulk and also introduce nitrogen (radicals of nitrogen in the N_2O plasma) into the bulk.

Figures 3.7 shows SIMS profiles for a sample treated with N_2O plasma (20 W). It is found that nitrogen atoms pile up at the high-κ/Si interface after the N_2O plasma treatment. This profile is different from the report using N_2 plasma in which the nitrogen has diffused uniformly into the bulk after annealing at 700 °C [70]. However, this result is similar to the resultant nitrogen profile in ultrathin gate oxide (or oxy-nitride) formed by N_2O oxidation or annealing [73]. Another advantage using N_2O plasma instead of N_2 plasma is the oxygen radicals introduced into the bulk of the high-κ film.

The oxygen profiles for all samples are measured and shown in Fig. 3.8. It is clear that samples with N_2O plasma treatments exhibit higher oxygen concentrations compared to the one without. From the previous report [22], leakage currents of nitrogen-incorporated high-κ dielectrics can be significantly reduced by 3–4 orders of magnitude. Recently, it has been widely accepted that the reason for leakage current reduction by nitrogen incorporation is that nitrogen anneals oxygen vacancies [71, 72].

As a result, the increase of oxygen by the N_2O plasma treatment is also helpful to reduce the oxygen vacancies in the bulk which is strongly related to the leakage current in high-κ dielectrics [69-72, 74].

Figure 3.9 presents the electrical characteristics for all samples with or without N_2O plasma treatments. Figure 3.9(a) shows the C-V curves for all samples. The N_2O plasma-treated samples have shown better-behaved C-V curves than the control sample. This result implies that the interfacial properties have been improved by the N_2O plasma treatment [75]. Capacitors with N_2O plasma treatments have shown higher accumulation capacitances (C_{ox}) than the control sample has. This is possibly due to the oxygen and nitrogen passivation at the high-κ/Si interface, which stabilizes the interfacial layer and effectively prevents the interfacial oxide re-growth during the following 880 °C N_2 annealing. Figure 3.9(b) shows the gate leakage. The N_2O plasma-treated samples show a great improvement compared with the untreated sample. The Weibull distributions of gate leakage currents and breakdown voltages are shown in Fig. 3.9(c) and (d), respectively. Capacitors with N_2O plasma treatments demonstrate much lower gate leakage currents and higher breakdown voltages.

3.4 Summary

Three approaches to incorporating nitrogen in $CoTiO_3$ high-κ dielectric films, including the ion implantation of N_2^+, ion implantation of N^+, and N_2O plasma treatment, have been investigated. Nitrogen incorporation by ion implantation of N_2^+ can improve the electrical properties in terms of gate leakage, breakdown voltage and time-to-breakdown (T_{BD}). To reduce the impinging mass of implanted ion species, N^+ ion implantation has been used. The same trends can be found as those produced using N_2^+. Higher doses of N^+ can improve the performance further. An alternative

N_2O plasma treatment is also an excellent method to improve the electrical properties, exhibiting better-behaved C-V curves, lower gate leakage currents and higher breakdown voltages while compared with the untreated samples.

Table 3.1 The resultant equivalent-oxide-thickness (EOT), interface layer, $CoTiO_3$ dielectric thickness, total thickness, effective κ-value, and flatband voltage for all samples.

	EOT (Å)	Interface layer (Å)	Dielectric film (Å)	Total film (Å)	Effective κ-value	Flatband voltage (V)
800 N_2^+	21.9	58.8	188.2	247.0	43.9	0.3
850 no	25.4	85.7	128.6	214.3	32.9	0.15
850 N_2^+	27.2	66.7	176.2	242.9	34.8	0.38
900 no	30.3	82.4	155.9	238.2	30.6	0.45
900 N_2^+	29.4	90.0	153.3	243.3	32.2	-0.23

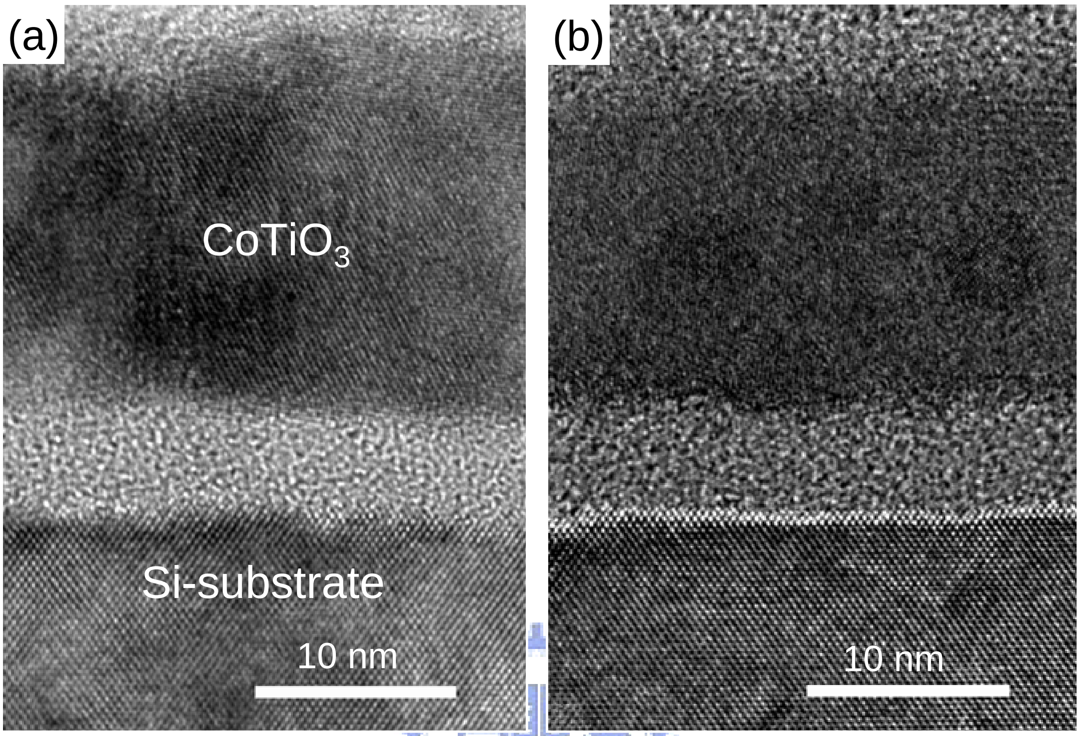


Fig. 3.1 TEM pictures for samples of CoTiO$_3$ oxidized at 800 °C for 10 min (a) without and (b) with nitrogen ion implantation.

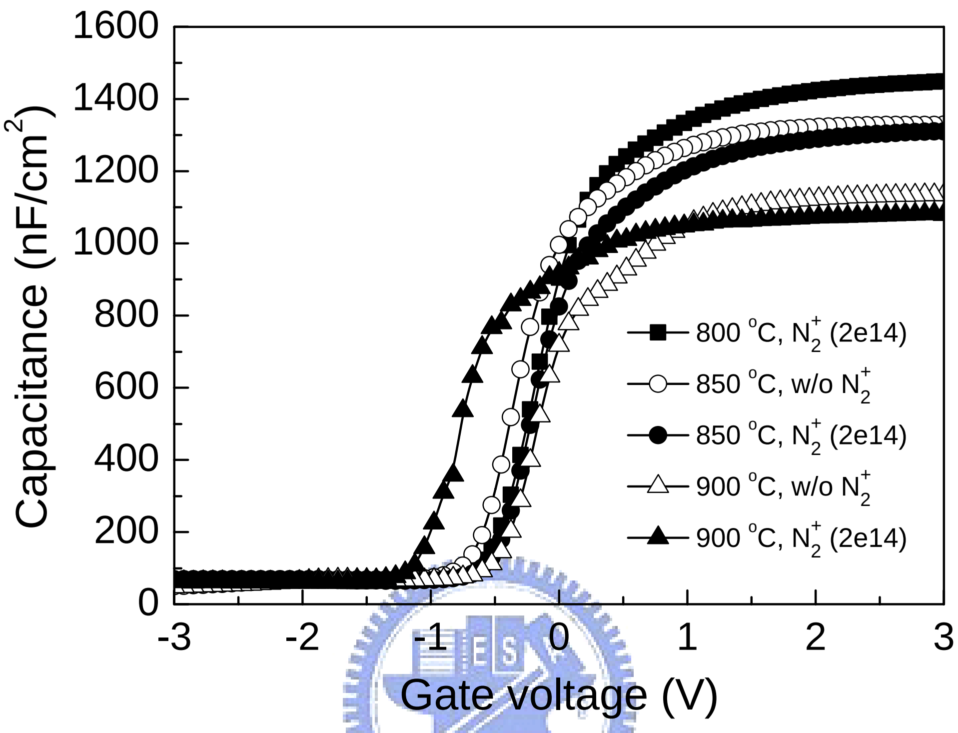


Fig. 3.2 High frequency C-V curves measured at 100 kHz for all samples oxidized at 800, 850 and 900 °C with or without nitrogen implantation.

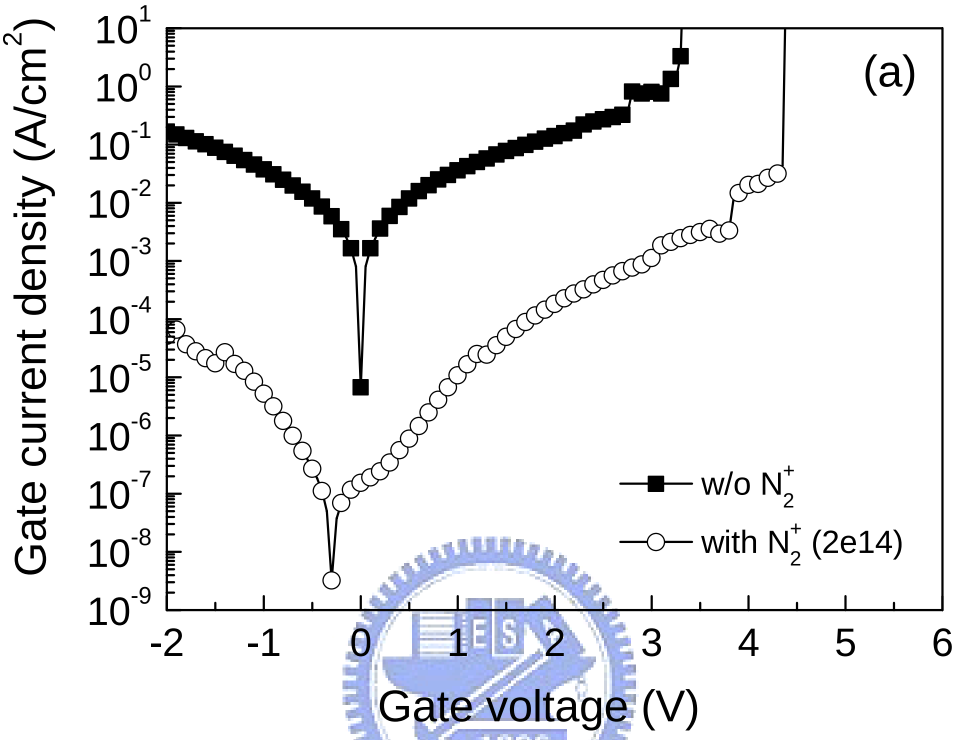


Fig. 3.3 Current-voltage characteristics of samples oxidized at 900 °C for 10 min with and without nitrogen implantation. (a) Gate leakage current density vs. gate voltage. (b) Weibull distribution of gate leakage current density at V_g = 1V. (c) Weibull distribution of breakdown voltage

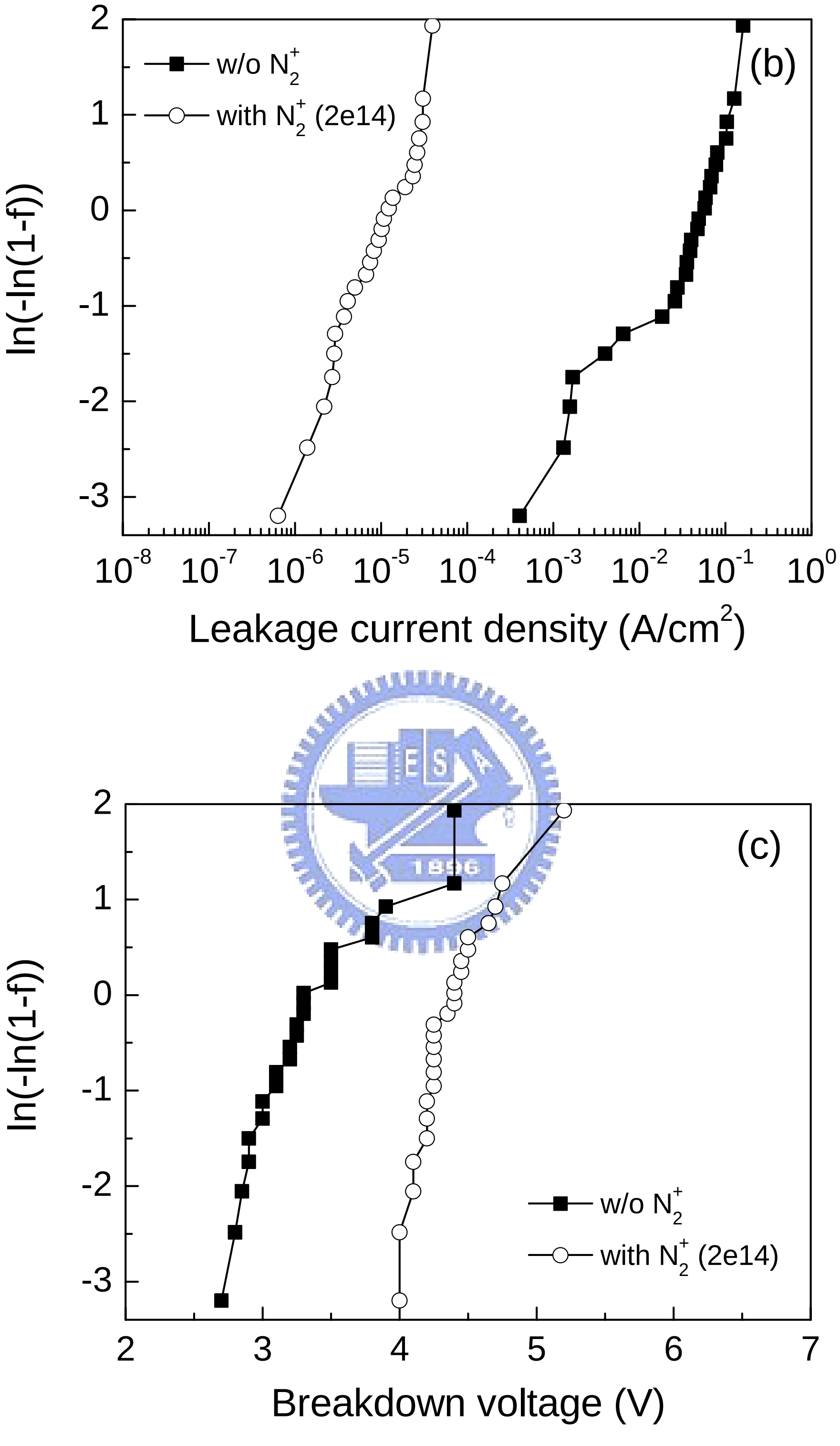


Fig. 3.3 Current-voltage characteristics of samples oxidized at 900 °C for 10 min with and without nitrogen implantation. (b) Weibull distribution of gate leakage current density at V_g = 1V. (c) Weibull distribution of breakdown voltage.

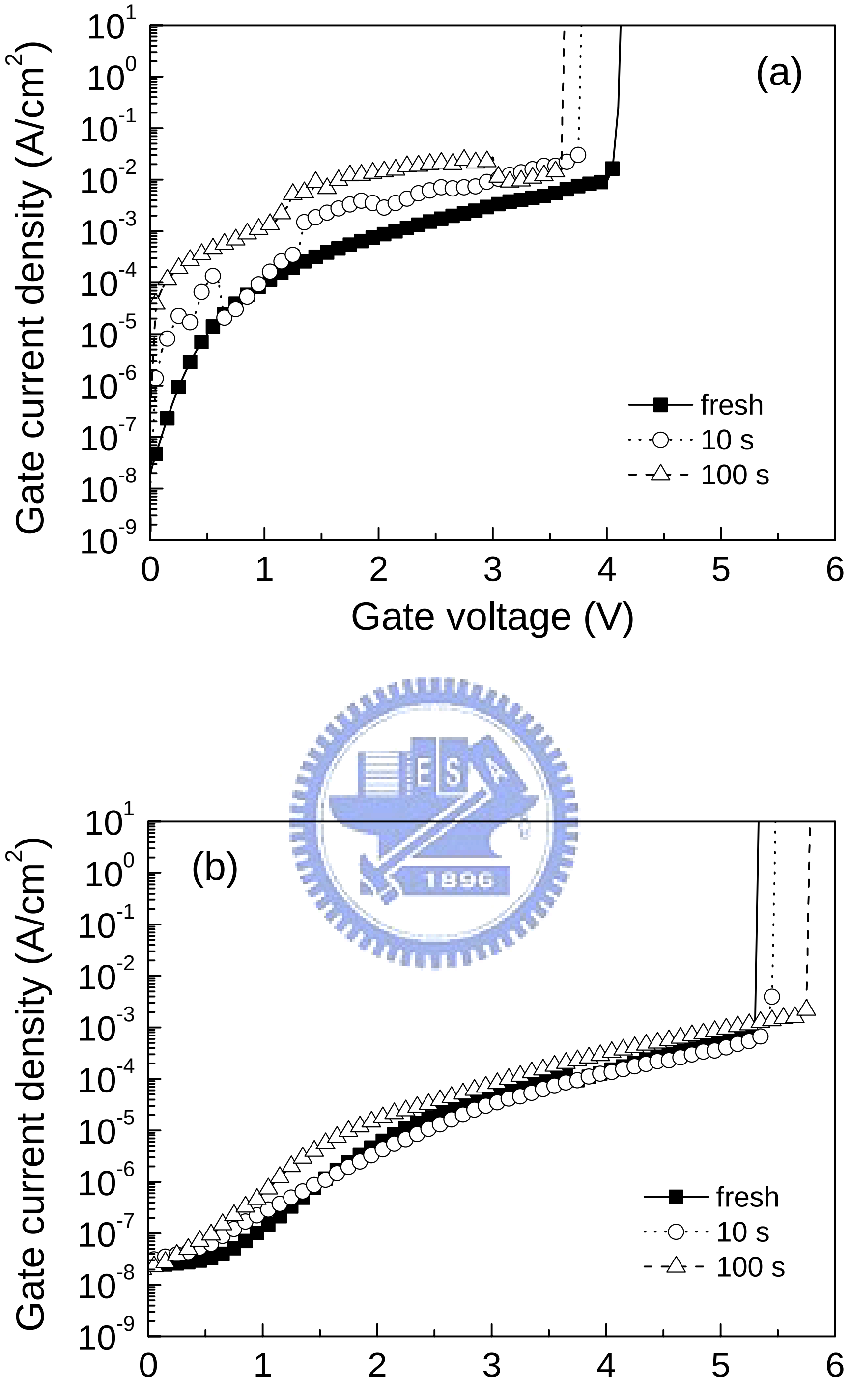


Fig. 3.4 Current-voltage characteristics for samples oxidized at 850 °C for 10 min (a) without and (b) with nitrogen implantation after constant voltage stress at $V_g = 2V$ for 100 s.

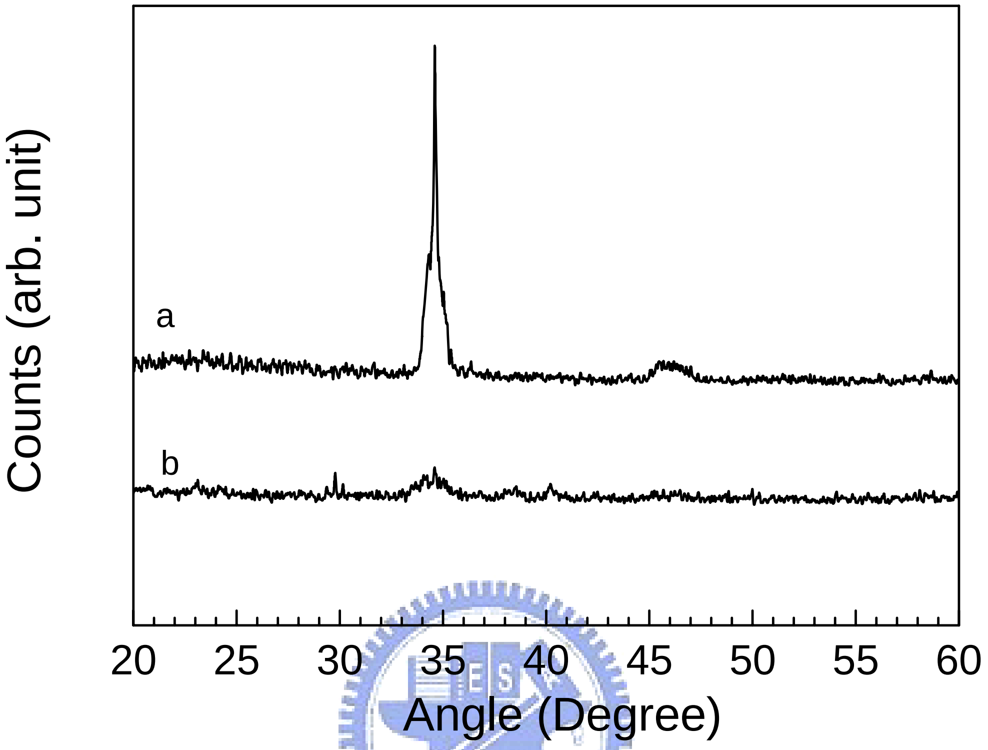


Fig. 3.5 XRD spectra for a $CoTiO_3$ films oxidized at 850 °C without (line a) and with (line b) nitrogen implantation.

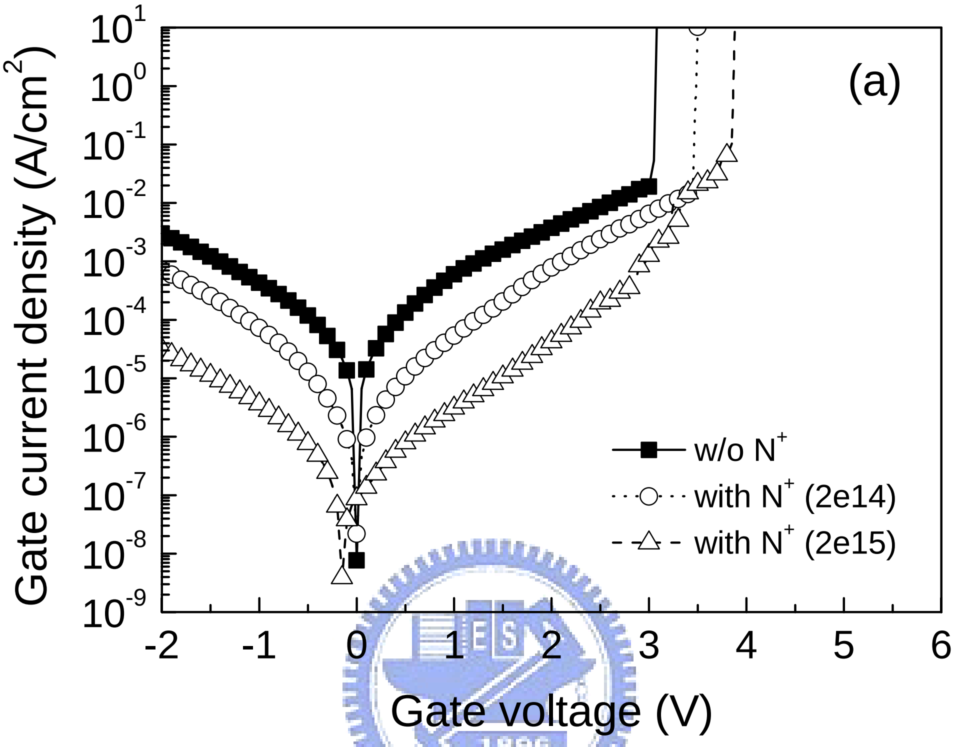


Fig. 3.6 Electrical measurements for samples oxidized at 850 °C for 5 min with and without N$^+$ ion implantation. (a) Gate current density vs. gate voltage. (b) Weibull distribution of gate leakage current-density at $V_g = 1V$. (c) Weibull distribution of breakdown voltage.

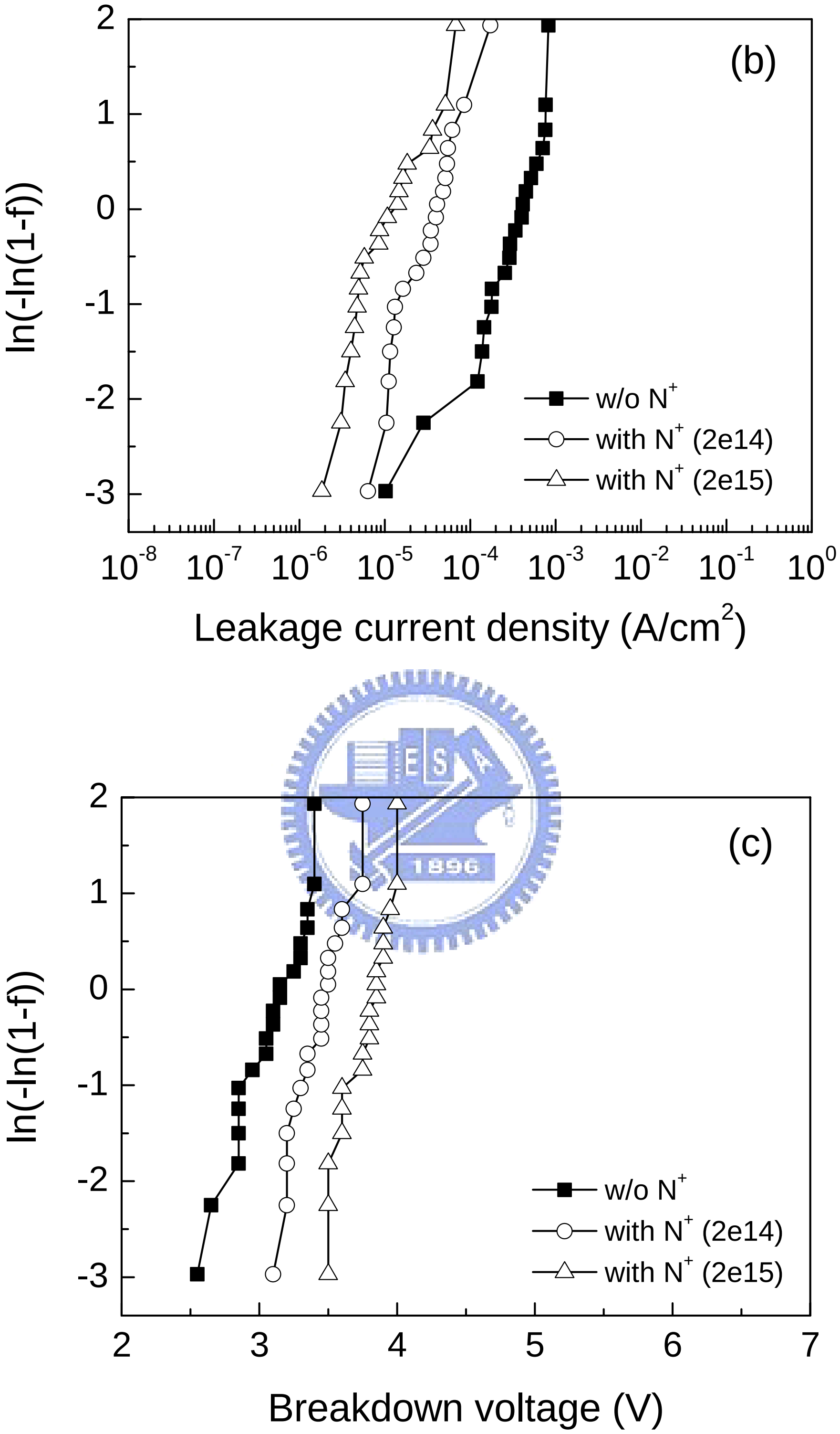


Fig. 3.6 Electrical measurements for samples oxidized at 850 °C for 5 min with and without N^+ ion implantation. (b) Weibull distribution of gate leakage current-density at V_g = 1V. (c) Weibull distribution of breakdown voltage.

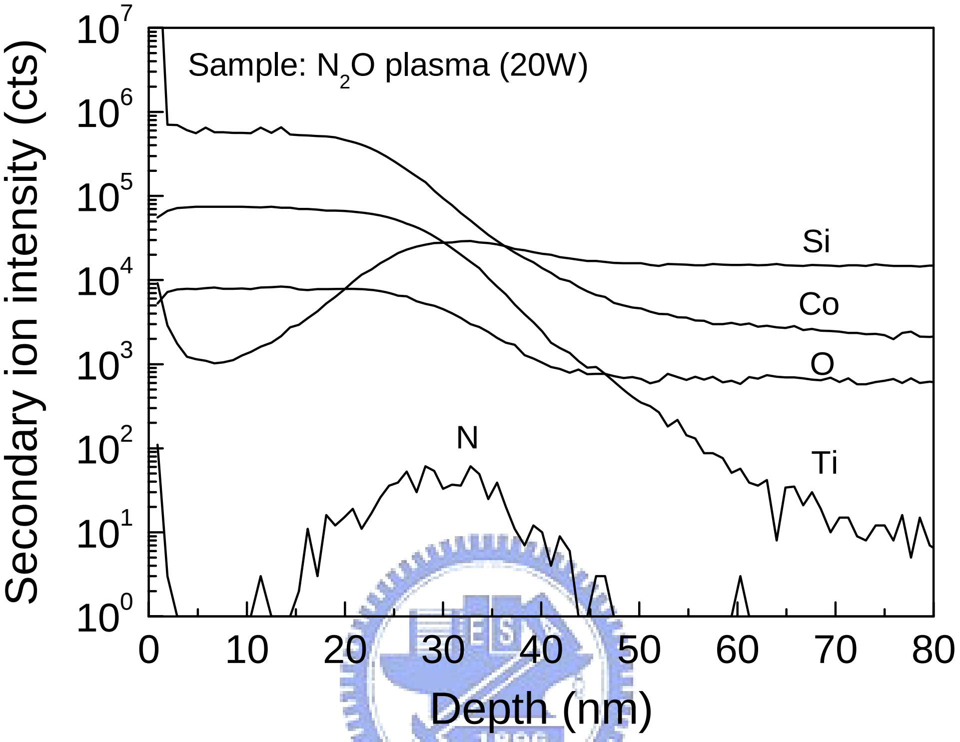


Fig. 3.7 SIMS profiles for a sample with 20 W N_2O plasma treatment.

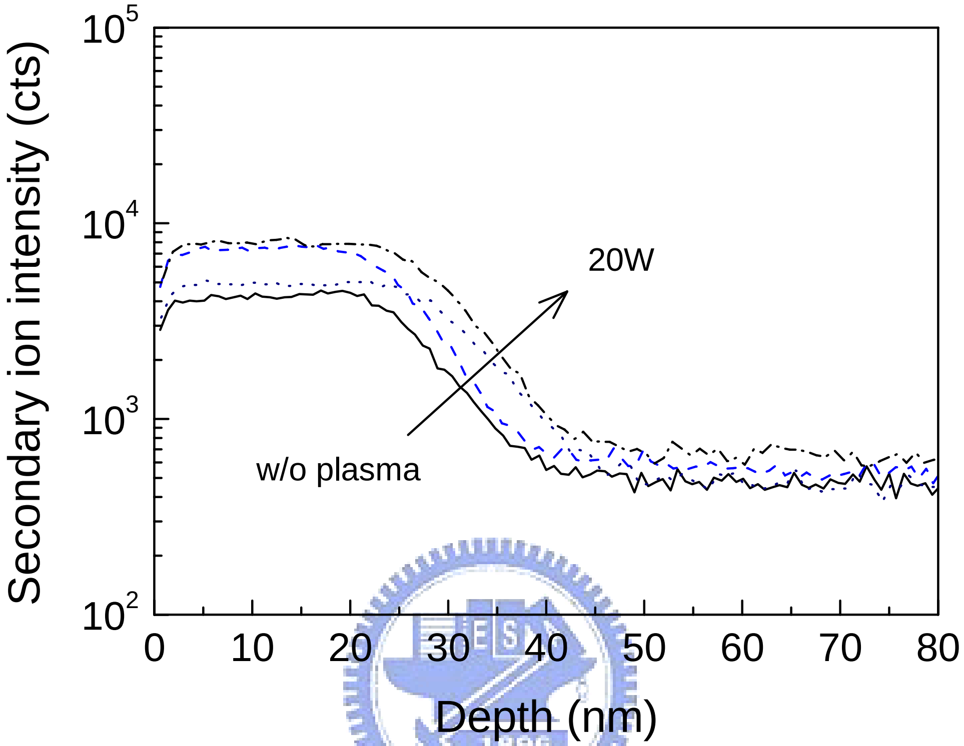


Fig. 3.8 Oxygen SIMS profiles for samples without N_2O plasma or with N_2O plasma treatments using powers of 10, 15, and 20 W.

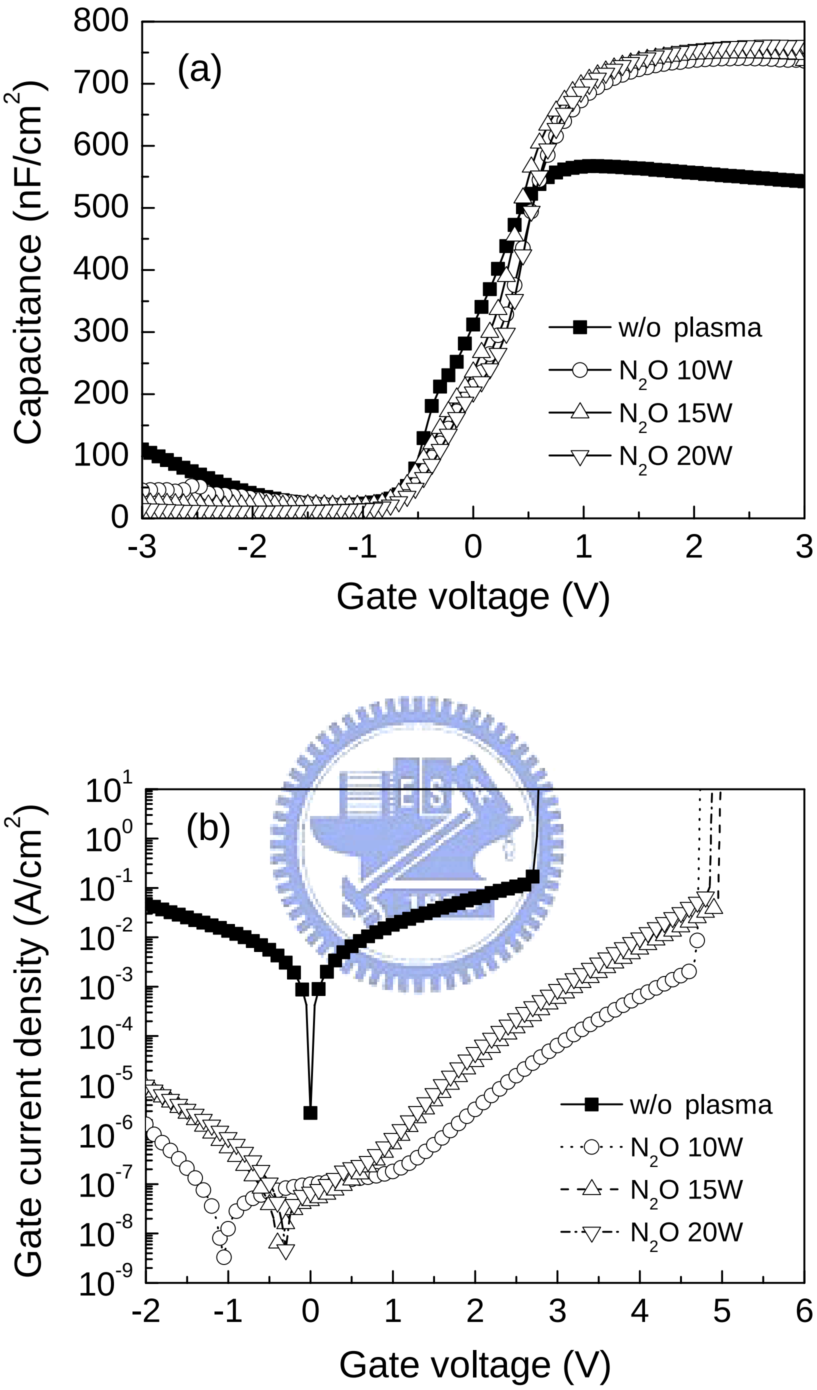


Fig. 3.9 Electrical characteristics for samples with and without N_2O plasma treatment: (a) C-V characteristics, (b) Gate current density vs. gate voltage, (c) the Weibull distribution of gate leakage current-densities at V_g = 1V, and (d) the Weibull distribution of breakdown voltages.

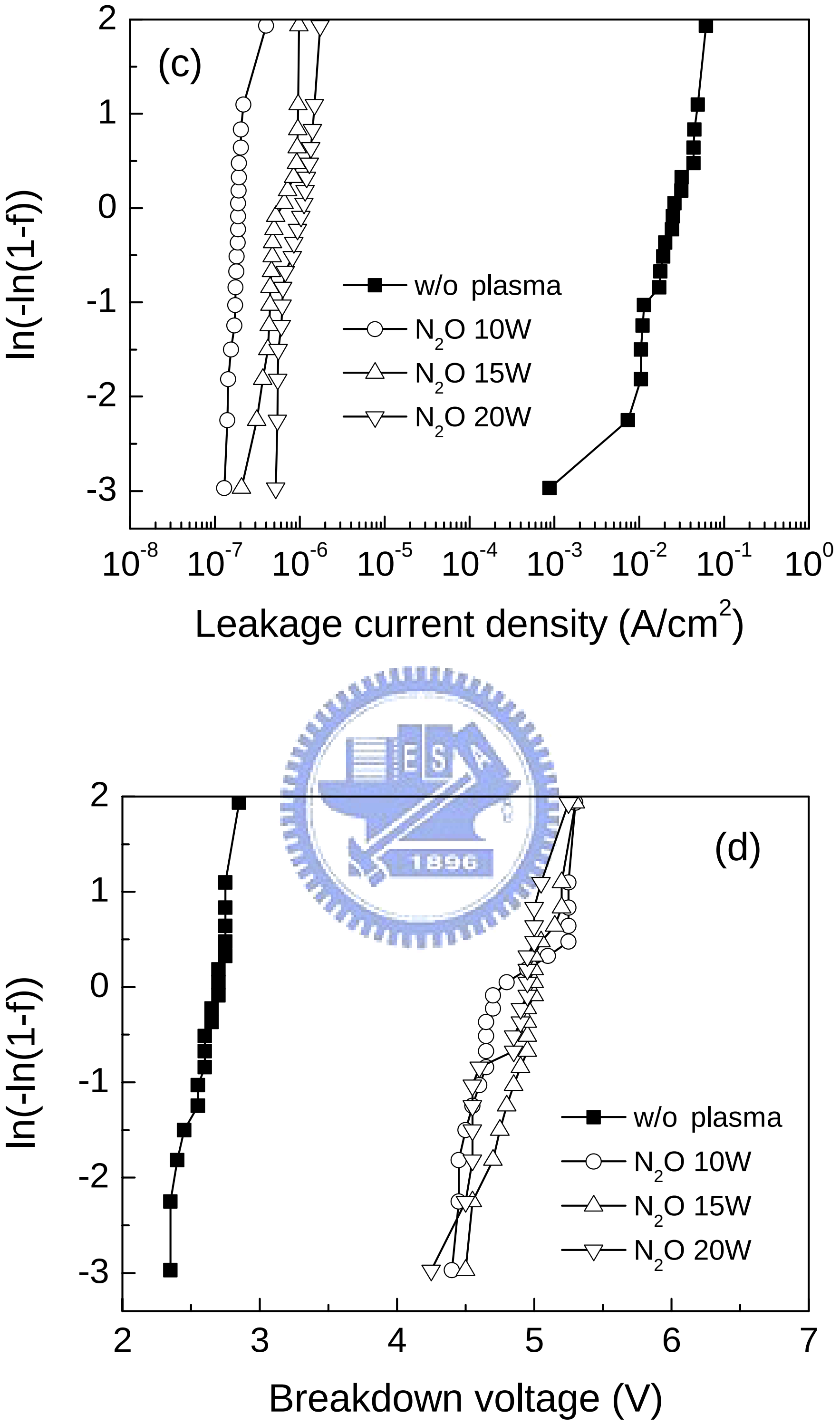


Fig. 3.9 Electrical characteristics for samples with and without N_2O plasma treatment: (c) the Weibull distribution of gate leakage current-densities at V_g = 1V, and (d) the Weibull distribution of breakdown voltages.

Chapter 4

Characterization of Hafnium Silicates by Pulse-Mode MOCVD using $[(C_2H_5)_2N]_4Hf$ and $(C_4H_9)(CH_3)_2SiOH$ or $[(C_5H_{11})O]_3SiOH$ for Advanced High-κ Gate Dielectrics

4.1 Introduction

As the gate lengths in metal-oxide-silicon field-effect transistors (MOSFET) decrease the required thickness of the gate dielectric, < 1 nm of SiO_2, is making leakage currents through the gate prohibitive [3]. This has lead to the search for a replacement for SiO_2 with a higher dielectric constant, which would enable the use of thicker layers with lower leakage. Hafnium oxide (HfO_2) is one of the most important replacement candidates being considered because it is thermodynamically stable on Si [76], especially against silicide formation [77]. With a higher dielectric constant than SiO_2, HfO_2 is promising as an alternative gate dielectric material for advanced MOS devices; however, it starts re-crystallizing at relatively low temperatures (~600 °C) [78]. The crystallization results in grain boundaries in the hafnium oxide films which could provide paths for leakage currents. Hence, the high temperature process involved in device fabrication can cause crystallization of hafnium oxide and degrade its insulation properties. To increase the crystallization temperature of HfO_2, nitrogen, aluminum, and silicon incorporation is being considered [78-80]. Considering the high thermal stability of traditional silicon dioxide, hafnium silicate has been looked into as a compromise between high dielectric constant and high crystallization temperature.

Chemical vapor deposition (CVD) techniques, either atomic layer deposition (ALD) or metal-organic CVD (MOCVD), are the most likely routes to a fully production-compatible process because they provide superior conformality and uniformity. ALD was traditionally performed with $HfCl_4$ and H_2O [81], but the possibility of halide contamination and the poor nucleation on H-terminated silicon surfaces, which requires the use of an interfacial buffer layer, has impeded its use for gate dielectrics. HfI_4 may provide a route to more stable deposition rates at lower temperatures [82, 83] but very low I incorporation has not yet been reported. Although the Cl contamination [84] and nucleation [85] problems are being addressed, resistance to the use of halides in production persists. A carbon and halogen-free precursor, $Hf(NO_3)_4$, has been used for ALD [86] but this produced oxygen-rich films with thick interfacial layers and lower than expected dielectric constants. Because they are halide-free and can be reliably delivered by direct liquid injection with low vaporizer temperatures of 140-150 °C, the alkylamides of hafnium have received a great deal of attention recently. They can be used to deposit HfO_2 films by ALD with H_2O [87] and carbon-free films have been obtained with tetrakis(diethylamido) hafnium (TDEAH) [88].

HfO_2 crystallizes at low temperatures and it is desirable to find a gate dielectric which remains amorphous during device processing where temperatures can reach as high as 1050 °C [28]. Increasing the Si concentration in hafnium silicate increases the crystallization temperature and the silicon/dielectric barrier height but reduces the dielectric constant. It has been estimated that SiO_2 mole fractions, $([SiO_2]/([SiO_2]+[HfO_2]))$ will be required to be > 75 mol% to avoid phase separation and crystallization [29] and films with 81 mol% SiO_2 were shown to be amorphous and thermally stable in a silicon-capped structure upon heating to 1050 °C [30]. The incorporation of nitrogen reduces significantly the required mole fraction of SiO_2 [31]

but it remains to be demonstrated that such high N concentrations can be incorporated without introducing other electrical defects [32].

The work of Ritala *et al*. [89] showed that mixed oxides could be produced by ALD using alternate pulses of chloride or alkyl precursors with alkoxides and used this technique to deposit zirconium silicate films using alternate pulses of $ZrCl_4$ and $Si(OEt)_4$ and $ZrCl_4$ with $Si(O^nBu)_4$. Other studies using this technique revealed Cl contamination levels >1 at.% and SiO_2 mole fractions as high as 77 % for $ZrCl_4$ with $Si(O^nBu)_4$ [90] while the corresponding numbers were Cl >0.1 at.% and SiO_2 < 53% when $SiCl_4$ was used with $Zr(O^tC_4H_9)_4$ [91]. The levels of halide contamination would be a concern if these precursors were used to produce the Hf silicate films required for gate dielectrics.

Gordon *et al*. [33] have shown that TDEAH can be used with tris(*t*-butoxy)silanol (TBOS) to produce Hf silicate by ALD and surmised that similar reactions would occur between other alkylamides and tris(*t*-alkoxy) silanols. Deposition rates, higher than expected from a bulky precursor like TBOS, were reported along with SiO_2 mole fractions as high as 75 mol%. This was explained by a mechanism that involves the absorption of two TBOS molecules for each molecule of the alkylamide [34]. TBOS is difficult to use because it is a solid at room temperature with a vapor pressure of ~15 Torr at 115 °C [35].

In present study we report the use of two novel silanol precursors for ALD with TDEAH which are liquids at room temperature and were vaporized using a simple bubbler. The first, *t*-butyldimethyl silanol (BDMS), has been used to produce low silica content hafnium silicate films by MOCVD [36]. The second, tris(*t*-pentoxy) silanol (TPOS), is an analogue of TBOS but with a higher vapor pressure. In fact, TBOS is a solid at room temperature which melts at 63-65 °C and boils at 205-210 °C while TPOS is a liquid which boils at 96-99 °C (at 2.5 Torr). (2003-2004 catalogue, Aldrich Chemical Company, Milwaukee, WI).

ALD precursors can also be used to deposit films by MOCVD, which is usually done at higher substrate temperatures and does not require a self-limiting adsorption of precursor molecules. Since MOCVD precursors are generally introduced into the chamber together, they must be more resistant to gas phase reactions at pressures in the 0.1-1 Torr range and so H_2O is not generally used as the oxidant and the silanols would be very reactive with the TDEAH in the gas phase at the process pressures usually encountered during MOCVD. However, the applicability of these precursors to pulse-mode MOCVD will also be discussed here.

The MOCVD technique is widely used in the semiconductor industry, and has been proven a reliable method for thin-film deposition. HfO_2 films deposited by MOCVD using tetrakis-(diethylamido) hafnium (TDEAH) have been reported [80, 87]. However, for the hafnium silicate deposition, there are some requirements for the silicon precursor. It has to be volatile so it can provide enough vapor pressure. Some precursor like tetra-ethyl-oxysilane (TEOS) is not suitable because their reaction rates at the temperatures suitable for TDEAH are not high enough to get sufficient silicon incorporation. Ozone or plasma techniques can reduce the temperature requirements but these can result in the growth of significant interface layers which negate the advantage of a high-k dielectric. Thus good Si precursors are still being sought for the deposition of high-quality Hf silicate films. In this work, *tert*-butyldimethylsilanol (BDMS) was evaluated as a silicon precursor for hafnium silicate deposition by MOCVD with TDEAH. The vapor pressure of BDMS is high enough to introduce its vapor into the MOCVD chamber using a simple bubbler arrangement.

Recently it was shown that films with high silica contents can be deposited by atomic layer deposition (ALD) at low temperatures using metal alkylamides with tris(*t*-alkoxy) silanols [33]. Other low temperature processes for the deposition of silicon dioxide require the use of plasmas which can result in damage from ion-bombardment. Thus the ALD technique could be useful for many applications in electronic and optoelectronic devices. The following work also describes the deposition of high quality hafnium silicate ($HfSi_xO_y$) thin films by ALD and metal-organic chemical vapor deposition (MOCVD) with process temperatures below 250 °C. Tetrakis(diethylamido) hafnium (TDEAH) and tris(*t*-pentoxy) silanol (TPOS) vapors were used as Hf and Si precursors, respectively. Alternative pulses of these two precursors allow a silicon-rich $HfSi_xO_y$ thin film to grow without additional oxidation steps. The low-temperature deposited $HfSi_xO_y$ films were then annealed in a rapid thermal annealing (RTA) system with different ambient or temperature conditions. MOS capacitors were fabricated for I-V and C-V measurements.

The atomic composition and bonding information were analyzed by *in-situ* and *ex-situ* X-ray photoelectron spectroscopy (XPS). The physical thickness was calibrated by high-resolution transmission electron microscopy (HRTEM) and the effective dielectric constant was then extracted from the C-V data. After a forming gas anneal, the Hf silicate films exhibited low leakage currents, relatively low interface-state densities (mid-gap D_{it} ~3×10^{11} $eV^{-1}cm^{-2}$), and negligible hysteresis (<20 mV). This would make them useful as gate dielectrics in thin-film transistors or as wave-guiding and passivation layers in optoelectronic applications. After high-temperature annealing the electrical characteristics were further improved, showing that these films could also meet the requirements for a replacement gate-dielectric for SiO_2 in CMOS technology.

4.2 Experimental

4.2.1 MOCVD Hf Silicates using TDEAH and BDMS with O_2

The MOCVD chamber (Fig. 4.1) is equipped with a liquid injection system (ATMI LDS-300B) which is used to deliver a 0.1 molar solution of TDEAH in octane at a rate of 0.2 ml/min. The hafnium precursor was pumped into a vaporizer which was held at 140 °C during the deposition, and the vapor along with 50 sccm of argon entered MOCVD chamber through a gas ring. The silicon precursor (BDMS) was stored in a bubbler and delivered into the CVD chamber by purging a carrier gas (100 sccm N_2) through the bubbler. The N_2 flow can bypass the bubbler and enter the chamber directly if only nitrogen purging is needed.

An *in-situ* Ellipsometer (Fig. 4.2) was attached to the chamber to monitor the growth of the films in real time. A differentially pumped mass spectrometer (HAL RC RGA 1000) was connected to the main chamber through an orifice. The orifice between the chamber and mass spectrometer resulted in a pressure drop of approximately 4 orders of magnitude. This differential RGA system monitored the gaseous components during film growth. Fig. 4.3 shows the mass spectrum of the BDMS. The peak at 59 atomic mass units (amu) was selected as an indicator for monitoring the BDMS vapor.

The TDEAH vaporizer, along with the downstream gas line/ring were all heated and held at 140 °C. The BDMS bubbler was held at 40 °C. 4-inch Si(100) wafers were used. The sample underwent a standard RCA cleaning procedure followed by a dilute-HF dip before its entry to the CVD chamber. The H termination on the Si wafer was then replaced by ~2 monolayers of SiO_2 by oxidizing the wafer *in-situ* using O_2 at 500 °C for 5 min. During the oxidation the chamber was purged by pure O_2 (150 sccm) and N_2 (100 sccm) flows, and the chamber pressure was ~11 milli-Torr.

The silicate was then deposited using a pulse-mode MOCVD, during which molecular oxygen, BDMS, and TDEAH were introduced into the chamber in alternative pulses. The pulse-mode deposition consisted of cycles of pulses of hafnium precursor, silicon precursor, and molecular oxygen, separated by nitrogen purge steps. The growth of hafnium silicate films was recorded by the *in-situ* Ellipsometer. After the deposition, *in-situ* XPS analysis was performed without exposing the wafer to atmosphere. The composition of the hafnium silicate was then calculated with the Si 2*p*, Hf 4*f*, and O 1*s* intensities. High resolution transmission electron microscopy (HRTEM) and atomic force microscopy (AFM) were utilized to verify the physical thickness and examine the surface morphology.

4.2.2 Low-Temperature MOCVD Hf Silicates using TDEAH and TPOS

The MOCVD chamber is equipped with a liquid injection system (ATMI LDS-300B) for the hafnium precursor. A bubbler is installed to transport the silicon precursor into the chamber. Experimental substrates were HF-dipped Si (100) wafers, with the H termination replaced by 1-2 monolayers of SiO_2 formed by oxidizing the wafers in O_2 at 500 °C. The TDEAH, a 0.1 M solution in octane, was used as the Hf precursor. The TDEAH was vaporized at 140 °C and then delivered into the chamber. The TPOS bubbler was held at 50 °C during the deposition. A pulse-mode deposition technique was used to produce hafnium silicate films. In one deposition cycle the TDEAH and TPOS vapor pulses were delivered alternatively into the chamber. The precursor pulses were separated by nitrogen purging steps. The TPOS precursor was carried by a nitrogen flow of 20 sccm flowing through the TPOS bubbler. Depositions were done at a substrate temperature of 250 °C. The Hf silicate film was then analyzed by XPS and TEM. Gate electrodes were deposited by evaporating aluminum through a shadow mask. Electrical measurements were made by probing the MOS diodes in a probe-station attached to two instruments, a multi-frequency LCR meter (HP 4275A) for capacitance-voltage (C-V) characteristics, and a pico-ammeter/DC voltage source (HP 4140B) for current-voltage (I-V) characteristics. The images of probed aluminum gates were taken by an optical microscope equipped with a digital camera, and the gate areas were then obtained using a digitalized program. The estimated gate-area errors were of or less than ±3%. The equivalent oxide thickness (EOT) was obtained from the 100 kHz C-V characteristics by using the NCSU C-V fitting routine [92] which took quantum effects into considerations.

4.3 Results and Discussion

4.3.1 MOCVD Hf Silicates using TDEAH and BDMS with O_2

In an effort to see if the BDMS could be used for atomic layer deposition (ALD), depositions were done with substrate temperatures in the 250~550 °C range. Because of the low pressure (10~20 mTorr) during deposition, rather long pulse times of 5~12 seconds were used for the BDMS. It was found that the first TDEAH pulse would saturate on the SiO_2 surface at 250~300 °C. At temperatures higher than 350 °C, the TDEAH decomposes on the substrate leading to coverage greater than one monolayer per step. In fact, HfO_2 ultrathin films have been successfully deposited by pulse-mode MOCVD in the same apparatus using TDEAH with O_2 or NO at 400 °C [78]. After the first pulse of TDEAH precursor, a BDMS pulse resulted into saturated surface which prohibited further chemisorptions during the subsequent TDEAH pulse. It was found that in the low temperature range the TDEAH did not react with the surface-absorbed BDMS molecules. Adding oxygen-purging steps did not enhance the surface decomposition of BDMS at a temperature ≤ 500 °C.

Using only the BDMS and molecular oxygen, no growth of SiO_2 was observed for substrate temperatures up to 550 °C. While the TDEAH and the BDMS pulses were introduced alternatively, the sequence of precursor pulses became crucial. When the sequence was an O_2 pulse followed with BDMS then TDEAH pulses, or just alternating pulses of TDEAH and BDMS without oxygen, almost no growth was observed. However, when the sequence was an O_2 pulse followed with a TDEAH pulse then a BDMS pulse, a repeatable growth occurred. Additional pump-down steps were found useful to make the growth more stable, with the drawback of increased cycle time.

Fig. 4.4 shows a thickness profile measured by the *in-situ* Ellipsometer. The thickness values on the Y-axis were not calibrated. Instead the differential thickness was referenced. This profile showed that the first TDEAH pulse had the largest growth among the deposition cycles. In the first cycle, a growth of approximately 0.58 nm was observed during the first TDEAH pulse, and the BDMS pulse increased the thickness by ~0.08 nm. The following TDEAH pulses, however, never showed as large a growth as the first one. This indicated that BDMS has retarded the surface reaction of the TDEAH. XPS analysis was performed *in situ* after the deposition. The calculation based on XPS results showed a [Si]/([Si]+[Hf]) ratio of 0.38 in the silicate film.

At a deposition temperature ranging from 300 to 550 °C, BDMS sub-monolayer coverage occurred when the BDMS pulse followed right after the TDEAH injection. However, an oxidation step using O_2 at temperatures higher than 500 °C was needed to allow the subsequent absorption and/or reaction of TDEAH.

Figures 4.5(a) and (b) show synchronized Ellipsometric and mass spectrometric traces at temperatures of 450 and 550 °C, respectively. The injection of TDEAH was indicated by increases of the octane partial pressure. Octane is the solvent used for TDEAH. The BDMS pulses were also monitored by the partial pressure of related species. In Fig. 4.5(a), when the substrate temperature was held at 450 °C, the films growth halted after the first cycle. A growth of 0.2 nm was observed for the first TDEAH pulse. The first BDMS pulse resulted in a thickness increase of ~0.1 nm. After the first cycle, no more growth was observed, even when the precursor pulses were repeated.

When the substrate temperature was increased to 550 °C, the deposition cycle became repeatable. In Fig. 4.5(b) the growth occurred when the TDEAH and the BDMS pulses were introduced. And again, the first TDEAH pulse got the highest growth rate.

By using TDEAH and BDMS, the pulse-mode deposition was strongly dependent on the sequence of precursor pulses and on the substrate temperature. The surface decomposition and/or reaction of the BDMS played an important role during the deposition, as illustrated in Fig. 4.6. The BDMS molecule has one OH group which can react with the chemisorbed TDEAH [35], and hence attach the BDMS molecule to the surface. Then the *t*-butyl and methyl groups of the BDMS molecules will passivate the surface with alkyl groups, and inhibit the TDEAH absorption in the next pulse. In order to remove the alkyl groups and reconstruct the surface, a higher oxidation temperature is needed. However, the increased temperature leads to a fast decomposition of TDEAH, and therefore the TDEAH chemisorptions are no longer self-limiting. To ensure self-limiting TDEAH chemisorptions, there would have to be a significant temperature ramp up and down between cycles. Since this is impractical for most CVD systems, this precursor combination is not likely suitable for the hafnium silicate growth by atomic layer deposition (ALD).

AFM and HRTEM analyses show that hafnium silicate films deposited at 550 °C have rough surfaces. Figure 4.7 shows an AFM image of a 4-nm thick hafnium silicate film. The film thickness is estimated by *in-situ* Ellipsometric measurements. The rms roughness is 1.42 nm measured in the 1×1 μm area and 1.39 nm in 5×5 μm. The AFM measurement made with an 8.5-nm thick film reveals an rms roughness of 2.77 nm (5×5 μm), essentially doubled from that of the 4-nm-thick film. Thus rougher surfaces are observed with thicker silicate films. These rough surfaces are possibly the results of non-uniform growth during the deposition. Initially there would be some reaction sites where the BDMS molecules were not fully oxidized and prohibitive for following TDEAH chemisorptions. These areas then provided less chances for the silicate to grow, and became the thinner areas. At other reaction sites where the TDEAH molecules got chemisorbed the rapid decomposition of TDEAH and uncontrolled HfO_2 growth could happen at 550 °C. Figure 4.6 illustrates the possible routes for such nonuniform reaction. Figure 4.8 shows the HRTEM results with silicate films deposited using TDEAH and BDMS with O_2 at 550 °C. It is clear that nonuniform depositions have caused rough and needle-like surface morphologies. In Fig. 4.8(b) there are small grains with clear lattice fringes. The film compositions are possibly nonuniform. Parts of the film can be hafnium-oxide rich and tend to re-crystallize after the high temperature annealing at 1000 °C. Although the nonuniform morphology and the tendency to phase separation may be utilized for some nanocrystal applications [93, 94], the rough silicate films are not very applicable to the ultrathin gate dielectrics for advance devices.

4.3.2 Low-Temperature MOCVD Hf Silicates using TDEAH and TPOS

A hafnium silicate film was deposited by MOCVD using alternative pulses of TDEAH and TPOS precursors. No additional oxidant gases were used during the deposition. A relatively thicker (~8 nm by *in-situ* Ellipsometry) film was deposited, and the composition analysis by *in-situ* XPS showed a Hf:Si ratio of 0.18:0.82. To look into the carbon-contamination issues, the silicate film was analyzed by XPS depth profiling. After a few minutes of surface sputtering, the carbon signals became lower than the detection limits (Fig. 4.9), which suggested that most of the carbon signals were coming from surface contaminations. After several sputter cycles, the hafnium signals increased with silicon and oxygen signals decreasing. This can be attributed to a non-uniform Hf distribution in the film. The large hafnium atoms can also be knocked-in by the impinging Ar ions during the sputtering, hence causing the increase of Hf 4*f* signals.

HRTEM analysis (Fig. 4.10) shows the amorphous structure of an as-deposited $Hf_{0.18}Si_{0.82}O_2$ film. The upper portion is darker, which implies a higher hafnium concentration in the upper layer. An energy dispersive X-ray spectrometer (EDS) line scan was performed along the film's cross-section. A slight increase of the silicon concentration was detected in the middle, corresponding to the bright layer in the TEM picture. The EDS line-scan also indicated that the aluminum gate may have reacted with the silicate films during the evaporation and created a top interfacial layer.

The 100 kHz C-V characteristics (scanned from inversion to accumulation) are shown in Figure 4.11(a). The C-V curve of the as-deposit sample showed a hump toward accumulation. It is believed that the appearance of the hump is likely due to P_b centers at the interface. The extracted EOT is 5.73 nm. Considering the ideal flat-band voltage ($V_{FB} \sim -0.25$ V with a substrate doping density ~ 10^{16} cm^{-3} [95]), the flat-band voltage $V_{FB} = -0.88$ V of the as-deposited film corresponds to a positive fixed charge density $N_f = 2.36 \times 10^{12}$ cm^{-2}. After an annealing in forming gas (FG, 4% H_2 + 96% N_2), the hump diminished and the flat-band voltage shifted to −0.59 and −0.28 V for the annealing temperature at 380 and 450 °C, respectively. The forming gas anneal

(FGA) thus passivated the P_b centers and the defects in the silicate. After a 450 °C forming gas anneal, the hysteresis in C-V curves can be effectively reduced. The EOT, flat-band voltage, and estimated N_f are summarized in Table 4.1. The extracted effective dielectric constants are also listed. Figure 4.11(b) shows the C-V hysteresis and the frequency dispersion for the sample annealed in FG at 450 °C for 20 min. The C-V curves measured at 100 kHz showed a negligible (<1.5 mV) hysteresis. Noticeable frequency dispersion is observed below mid-gap, indicating the existence of donor-like interface states. The dispersion due to the remaining interface states might be further reduced with a post-metallization annealing. Figure 4.12 shows J-V curves of the $Hf_{0.18}Si_{0.82}O_2$ samples. The breakdown voltage was enhanced after a 380 °C forming gas anneal. When the annealing temperature was raised to 450 °C, however, the soft breakdown phenomenon became more severe in the high electric-field region.

4.4 Summary

tert-butyldimethyl silanol (BDMS)was evaluated as a silicon precursor for hafnium silicate deposition with tetrakis-(diethylamido) hafnium (TDEAH). BDMS has one OH group, which should react with chemisorbed TDEAH. However, the other *t*-butyl and methyl groups can passivate the substrate surface, and stop the further absorption of TDEAH. To remove the alkyl ligands or reconstruct the surface, a deposition temperature >500 °C is needed while using BDMS and TDEAH with O_2. This led to a deposition without the self-limiting properties of TDEAH. And it became difficult to control the uniformity and the surface roughness. High resolution transmission electron micrographs show that the films produced at 550 °C are rough. To better utilize the BDMS in silicate deposition, an oxidant, such as water or ozone that could react with the BDMS at a lower temperature would be needed. Otherwise, a dynamic temperature control during the deposition may be needed, which is prohibitive for most CVD systems.

Carbon-free hafnium silicate thin-films were deposited by using MOCVD with alternative pulses of TDEAH and TPOS precursors. Hafnium silicates with high silicon contents ($Hf_{1-x}Si_xO_2$, $x > 0.5$) were deposited at 250 °C without additional oxidants or plasma-enhanced techniques. Chemical compositions (XPS date) of the $HfSi_xO_y$ remained stable when an 800 °C vacuum RTA was performed after the deposition. A forming gas anneal at a temperature ranging from 380 °C to 450 °C could further improve the hafnium silicate interface quality. This low-temperature process could be promising for TFT or optoelectronic applications.

Table 4.1 Flat-band voltages (V_{FB}), positive fixed charge densities (N_f), the equivalent oxide thickness (EOT) and effective dielectric constant (κ_{eff}) extracted from C-V characteristics in Fig. 4.11. The $Hf_{0.18}Si_{0.82}O_2$ film was deposited by pulse-mode MOCVD using TDEAH and TPOS alternative pulses. The forming gas annealing (FGA) was performed after the deposition. Aluminum-gate electrodes were used.

FGA conditions:	w/o	380 °C, 20 min	450 °C, 20 min
V_{FB} (V)	-0.88	-0.59	-0.28
N_f (cm^{-2})	2.36×10^{12}	1.27×10^{12}	1.16×10^{11}
EOT (nm)	5.73	5.74	5.59
κ_{eff}	6.35	6.34	6.50

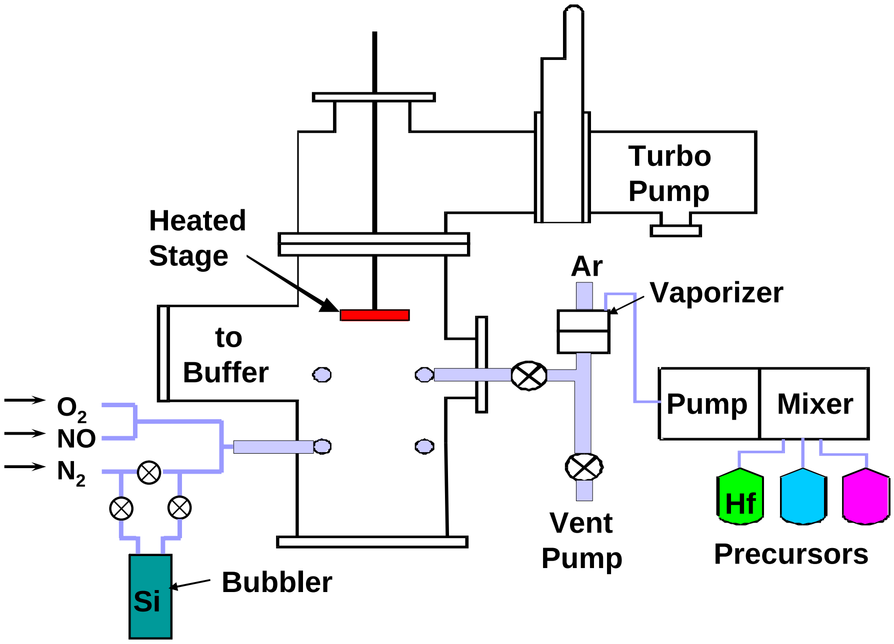


Fig. 4.1 Illustration of the MOCVD chamber equipped with a liquid injection system (for Hf precursor) and a bubbler (for Si precursor); the sample wafer is sitting face-down on a quartz-ring holder and heated by a set of halogen lamps.

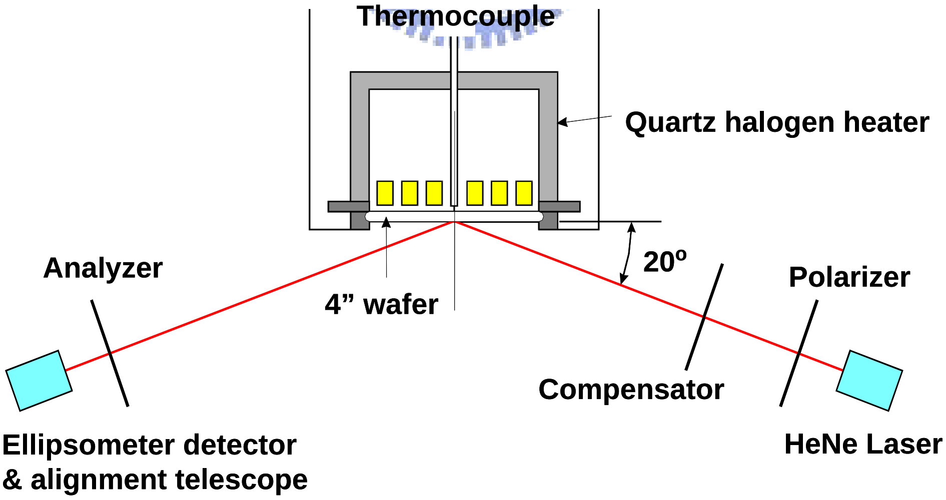


Fig. 4.2 Illustration of the sample stage in MOCVD chamber; an *in-situ* Ellipsometer system is also mounted to the chamber for real time thickness measurements.

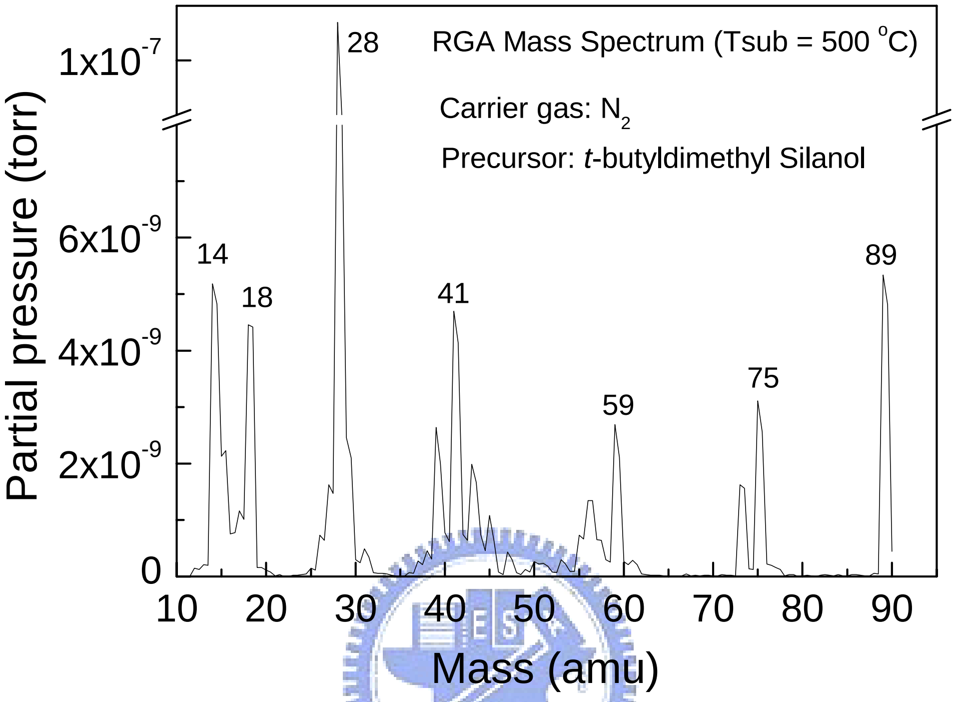


Fig. 4.3 The BDMS mass spectrum. A molecular nitrogen flow of 100 sccm was purged through the BDMS bubbler. A silicon wafer was loaded onto the stage and heated to 500 °C during the measurement. The bubbler and the CVD chamber walls were held at 40 °C and ~120 °C, respectively.

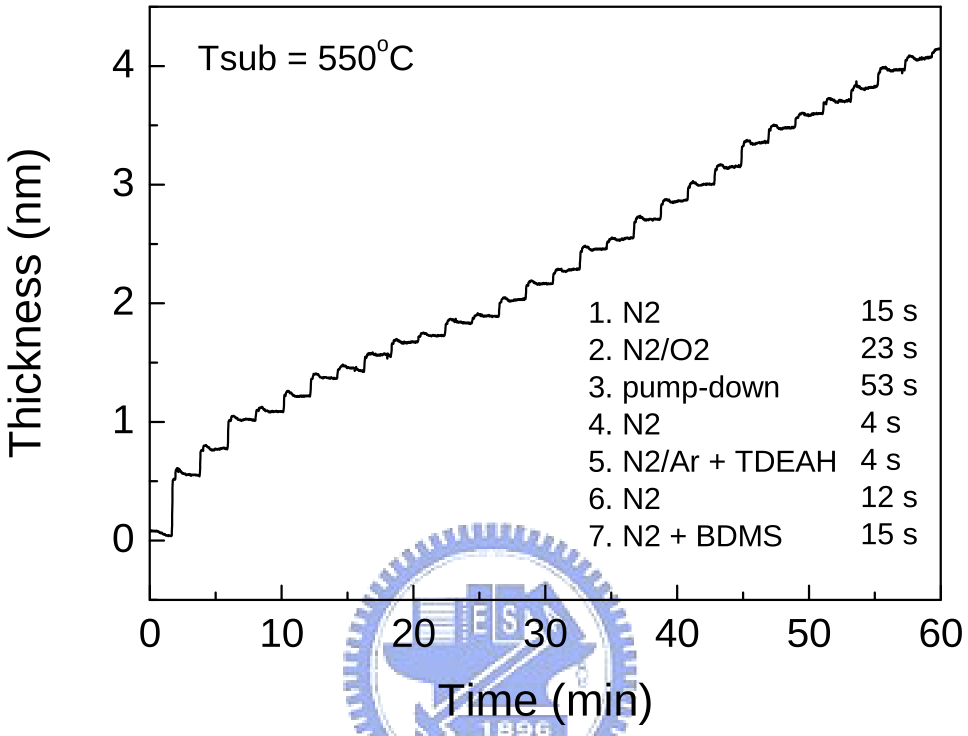


Fig. 4.4 Trace of *in-situ* Ellipsometric measurements for a pulse-mode deposition. There are 7 steps in a deposition cycle. After the molecular oxygen pulse, a long pump-down step was added. The substrate temperature was 550 °C for this deposition.

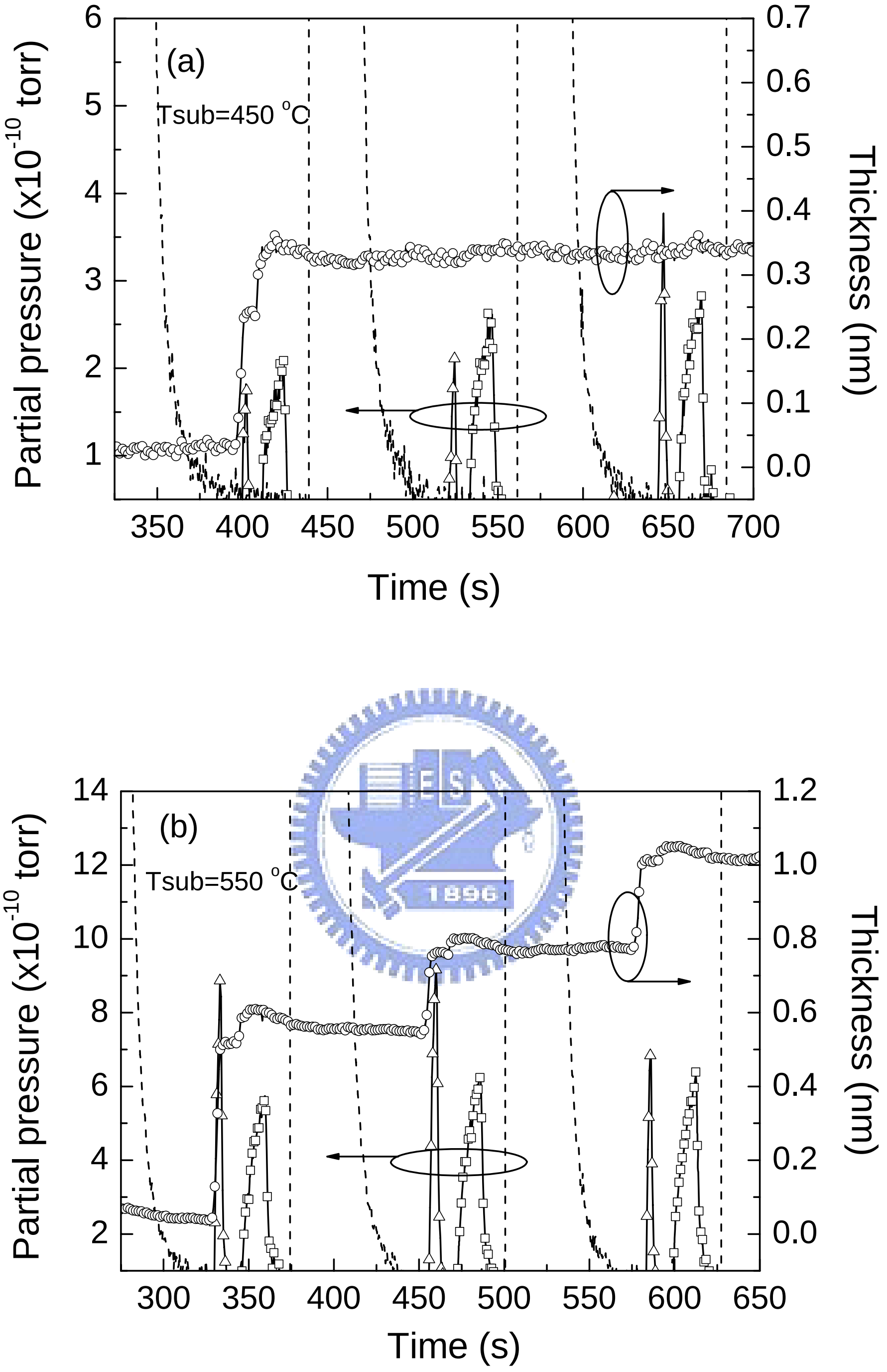


Fig. 4.5 Traces of *in-situ* Ellipsometric measurements and mass spectra readings for depositions at (a) 450 and (b) 550 °C: (dash line) O_2, (△△△) octane, (□□□) species from BDMS, (○○○) film thickness.

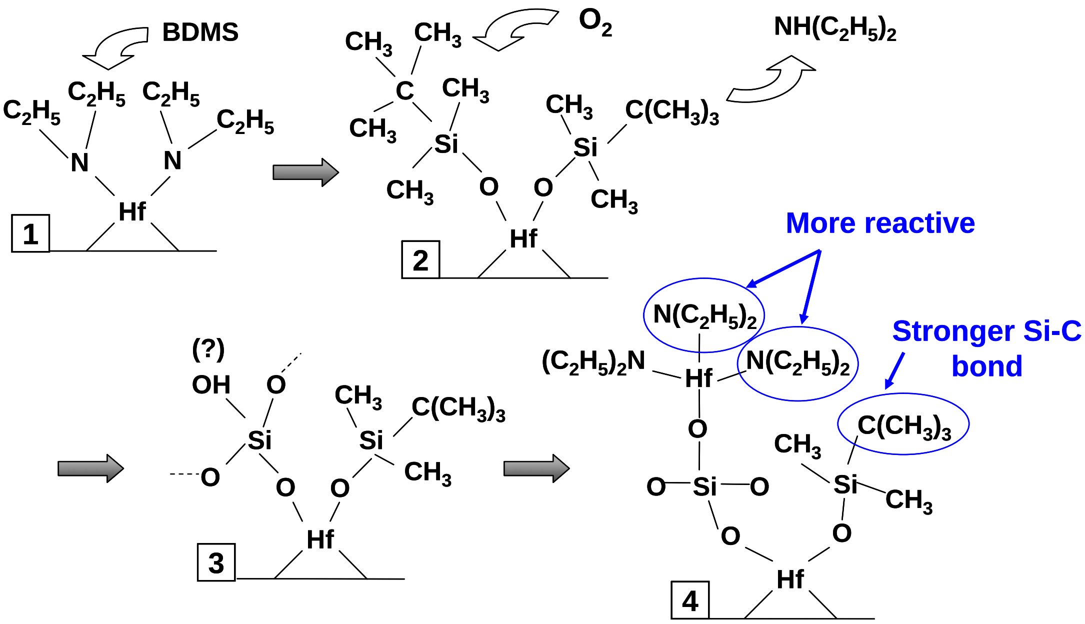


Fig. 4.6 Illustration showing the possible reaction routes for chemisorbed TDEAH and BDMS precursors. The oxidation step can replace the Si-C bonds with Si-O bonds which are more reactive with TDEAH precursors.

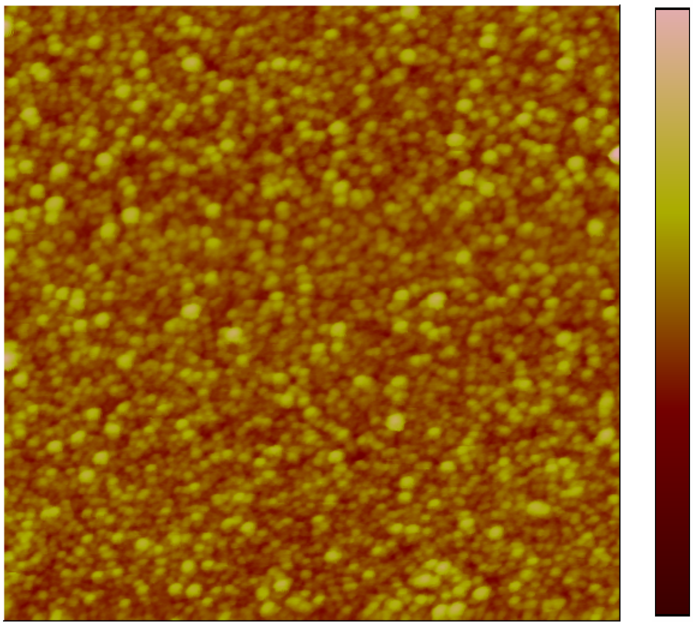


Fig. 4.7 AFM image of a 4-nm Hf silicate film deposited at 550 °C using TDEAH and BDMS with O_2. The rms roughness is 1.42 nm measured in the scan area. The image size is 1 μm × 1 μm. The color scale indicates the contrast range for a 20 nm height.

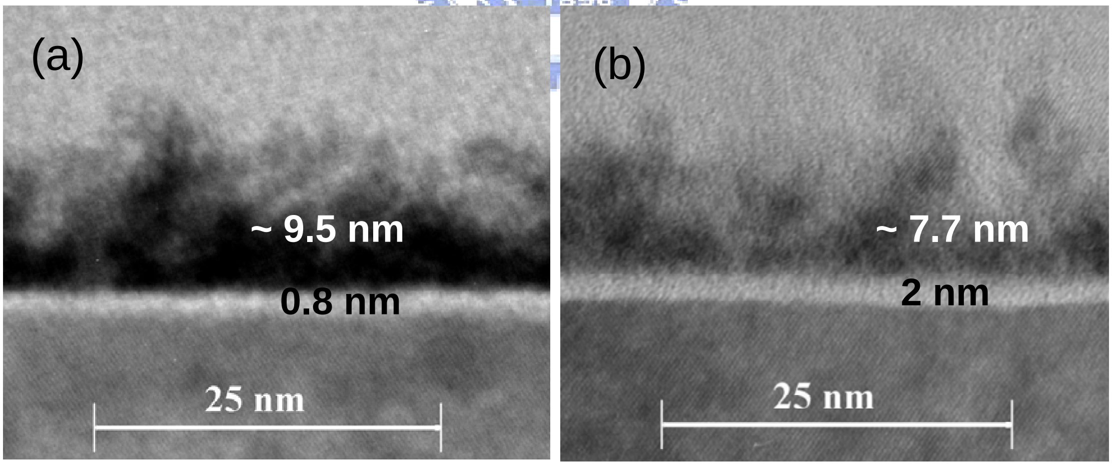
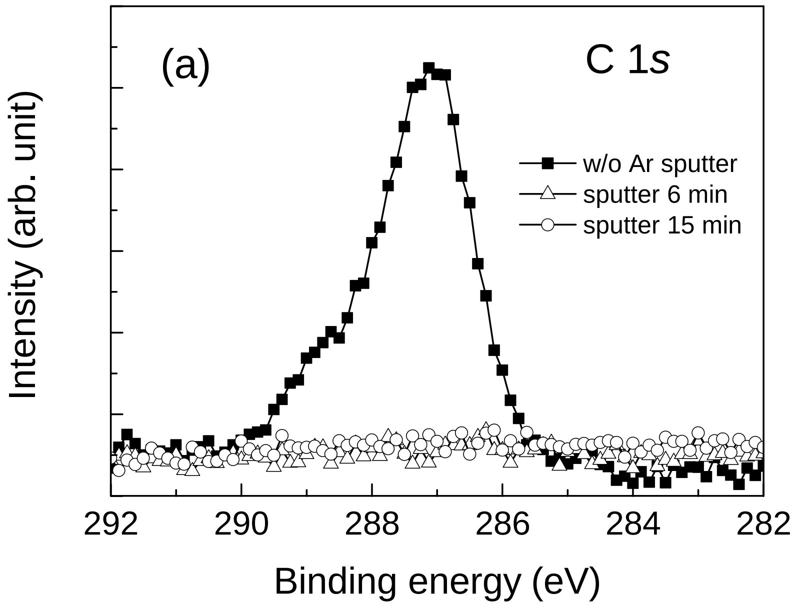
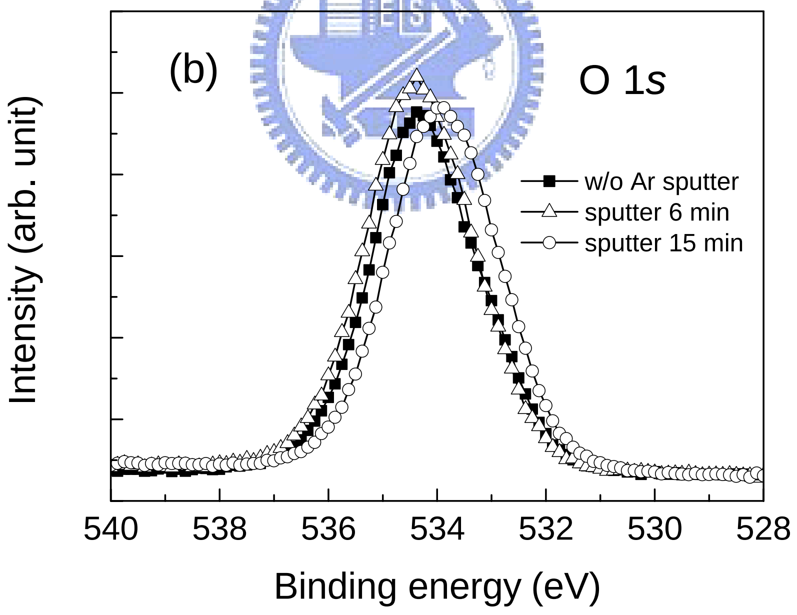


Fig. 4.8 TEM micrographs of Hf silicate films deposited at 550 °C using TDEAH and BDMS with O_2: (a) spike annealed at 800 °C in vacuum and then capsulated *in situ* with an amorphous silicon layer; (b) the same sample with an additional *ex-situ* N_2 anneal at 1000 °C for 30 seconds.


(a)
C 1s
w/o Ar sputter
sputter 6 min
sputter 15 min
Intensity (arb. unit)
292
290
288
286
284
282
Binding energy (eV)


(b)
O 1s
w/o Ar sputter
sputter 6 min
sputter 15 min
Intensity (arb. unit)
540
538
536
534
532
530
528
Binding energy (eV)

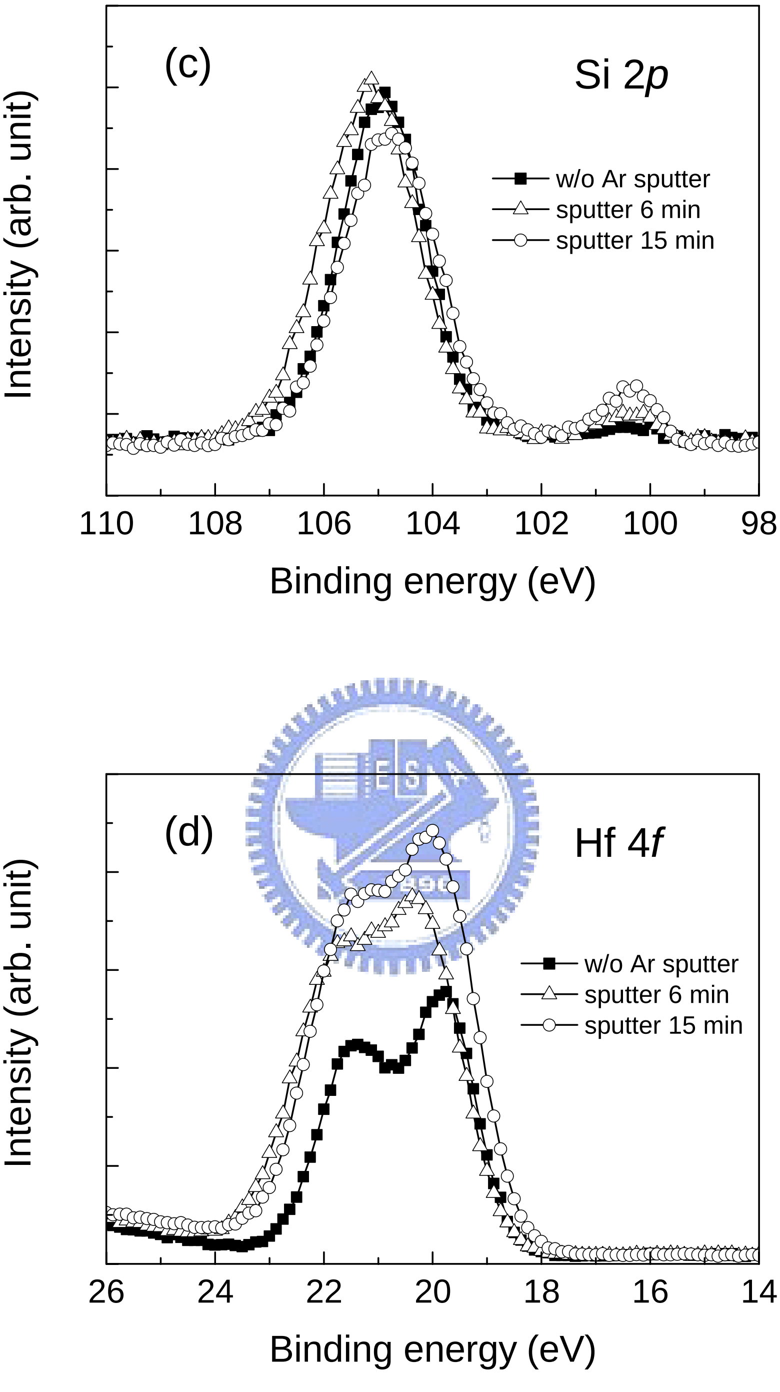


Fig. 4.9 (a) C 1*s*, (b) O 1*s*, (c) Si 2*p*, and (d) Hf 4*f* XPS spectra for an $Hf_{0.18}Si_{0.82}O_2$ film deposited by pulse-mode MOCVD using TDEAH and TPOS alternative pulses. After a surface sputtering, the carbon signals became lower than the detection limits.

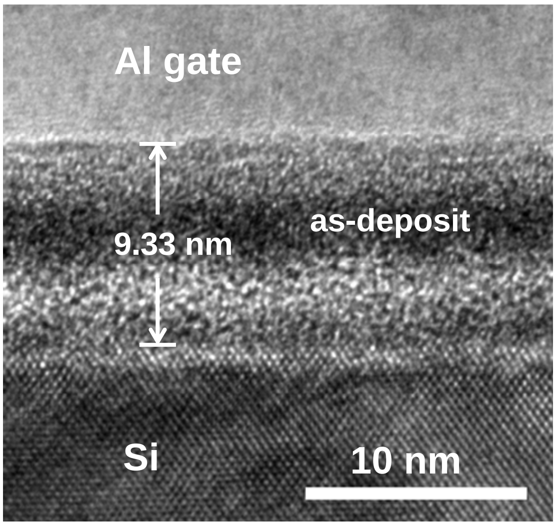


Fig. 4.10 HRTEM picture of the as-deposit $Hf_{0.18}Si_{0.82}O_2$ film deposited by pulse-mode MOCVD using TDEAH and TPOS alternative pulses.

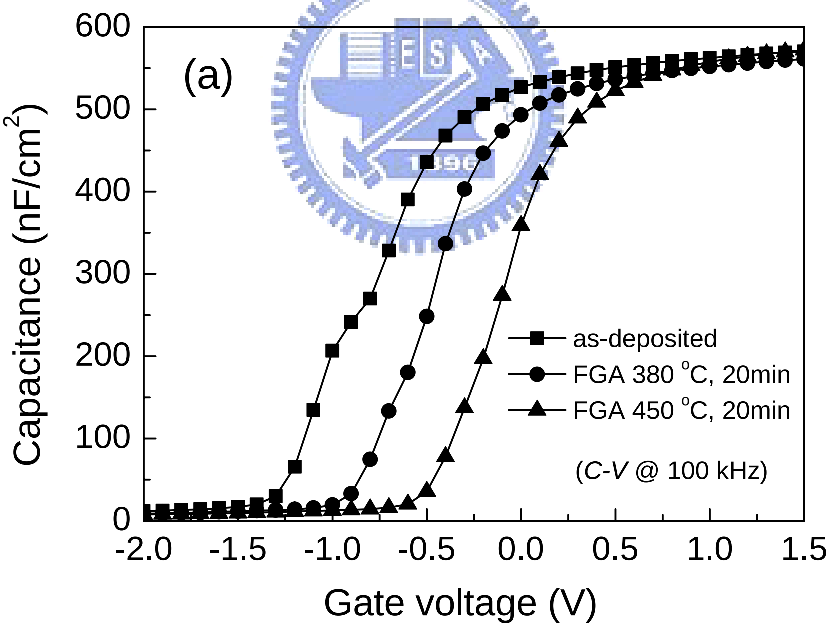


Fig. 4.11 (a) C-V curves of the $Hf_{0.18}Si_{0.82}O_2$ films with and without a forming gas annealing. The gate bias was swept from negative to positive during the measurement. (b) Bi-directional C-V curves of the $Hf_{0.18}Si_{0.82}O_2$ film annealed in forming gas at 450 °C for 20 min. Noticeable frequency dispersion is observed below midgap.

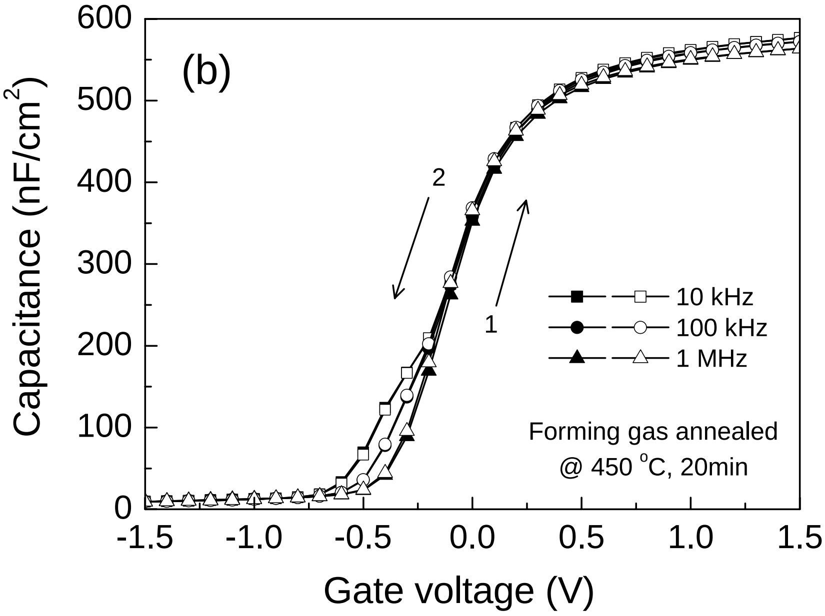


Fig. 4.11 (b) Bi-directional C-V curves of the $Hf_{0.18}Si_{0.82}O_2$ film annealed in forming gas at 450 °C for 20 min. Noticeable frequency dispersion is observed below midgap.

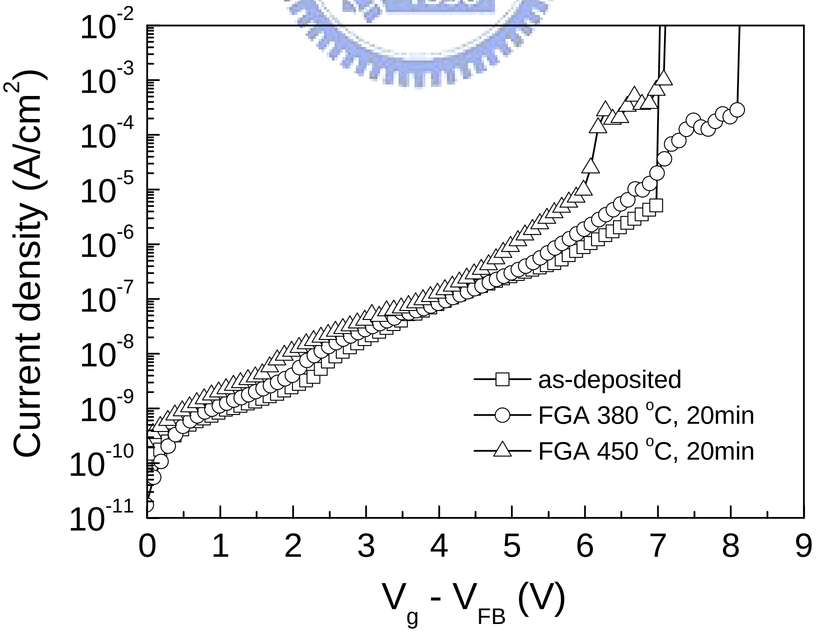


Fig. 4.12 Gate current density vs. oxide bias for the $Hf_{0.18}Si_{0.82}O_2$ samples; post deposition annealing was performed in forming gas.

Chapter 5

Physical Characterization of Si Nanocrystals Self-assembled by *in-situ* Rapid Thermal Annealing of Ultrathin *a*-Si on SiO_2

5.1 Introduction

Recently, silicon nanocrystals have drawn serious attentions because of their great potential for the semiconductor memory device applications [10, 96, 97]. In years, various techniques have been developed to produce Si nanocrystals, including the chemical vapor deposition (CVD) techniques [10, 62, 97-101], the oxidation of a Si thin-film [102], the high-temperature Si-precipitation in Si-rich SiO_x [103-105] or Si-implanted SiO_2 layers [106-110], and an aerosol deposition technique [96, 111, 112].

Among Si-nanodot techniques, the CVD method has been widely used to grow Si nanoparticles with small sizes and high densities. Though the bottom-up nature of CVD method and the random distribution of nanocrystals may introduce challenges in the device fabrication process, for example the etch uniformity of the Si-dot layer [97]. In addition, the chemical properties of the oxide layer, including the Si-O-Si bond strain and the Si-OH groups on the surface, were found critical in the nucleation of Si nanocrystals and therefore affecting the Si-dot density [113, 114]. Therefore, oxide surface functionalizations have been studied to selectively control the CVD of Si nanodots on SiO_2 [115, 116]. Thermal oxidation of a thin Si layer also has been used to produce Si nanocrystals [102] or amorphous Si (*a*-Si) nanoclusters [117] in a SiO_2 matrix. However, the oxidation time is critical because it must be long enough to separate the Si dots but meanwhile short enough to keep the dots from diminishing.

The additional oxidation step also introduces challenges in the tunnel-oxide thickness control for memory devices. Another technique, using the thermal precipitation to produce Si quantum dots in sub-stoichiometric SiO_x [104, 105] or Si-implanted SiO_2 [107-109] layers, needed a prolonged high temperature annealing above 1000 °C, which added a significant thermal budget to the process. An aerosol technique has been demonstrated [96, 111] to fabricate a densely packed array of Si nanocrystals. However, the unconventional equipments used by this aerosol technique still draw concerns about the compatibility with conventional semiconductor manufacturing process [96].

The surface coalescence of *a*-Si during an ultra-high vacuum (UHV) annealing was first observed by Sakai *et al* [23]. The growth of hemispherical grained (HSG) Si islands on the *a*-Si surface was explained by the segregation of diffusive Si atoms around surface nucleation centers [23]. Since then the resulted HSG structure has been widely adopted in the dynamic random-access-memory (DRAM) devices [37] to enhance their capacitive charge-storage densities [38]. Recent studies by Akazawa have suggested that, after a long annealing time (3 hours), the growth of HSG Si would saturate, and a self-limiting, highly-uniform size distribution could be obtained regardless of the annealing temperature [39, 40].

The agglomeration of Si on SiO_2 has also been reported. Si islands were produced by annealing ultrathin *a*-Si [41-43] or silicon-on-insulator (SOI) [23, 37, 44-47] films under UHV conditions. Theoretical studies have provided insights in the mechanism of Si-dot agglomeration from an ultrathin Si film [42, 48]. It is suggested that the surface energy instabilities play an important role in the thermal agglomeration, or de-wetting, of the ultrathin films. For example, a thermodynamic model based on the calculation of surface energy has been developed by Danielson *et al.* [48], in which the agglomeration instabilities observed in ultrathin SOI films were discussed. Their work predicted that ultrathin strained SOI, germanium-on-insulator, and III-V-on-insulator should be all susceptible to the agglomeration instability behaviors. The general implications of their surface-energy-driven de-wetting theory are also suitable to explain the agglomeration behavior of *a*-Si thin films and the nanocrystal formation.

In this chapter, Si nanocrystals fabricated by the thermal agglomeration technique are investigated. Ultrathin *a*-Si layers are deposited on a thin tunnel-oxide layer and then annealed *in situ* using a rapid thermal annealing (RTA) setup under UHV. The *a*-Si layers and the thermal agglomeration behaviors are monitored by an *in-situ* x-ray photoelectron spectroscopy (XPS) machine. The surface morphology and the nanocrystal structures are analyzed by atomic force microscopy (AFM), scanning electron microscope (SEM), and transmission electron microscope (TEM).

Also in this chapter, a theoretical model is established to fit the *in-situ* XPS results and estimate the agglomerated dot size and density. In past years, the XPS analysis of the SiO_2/Si system has been widely studied [118] and also found useful in the oxide thickness methodology [119]. Here we demonstrate how XPS measurements would reflect the *a*-Si deposition and the nanocrystal agglomeration. Calculations are made based on the photoelectron attenuation theories [49], and a simple model is proposed for the XPS measurements with Si nanocrystal samples. Comparisons between the calculated results and the experimental data have shown a fairly good match. Therefore the nanocrystal features can be reasonably estimated by this model using *in-situ* XPS measurements.

5.2 Experimental

4-inch, p-type Si(100) wafers with a resistivity of 5–10 Ω-cm were used as the substrates in this study. After a standard RCA cleaning procedure and a dilute-HF dip, an ultrathin tunnel-oxide/oxinitride layer was thermally grown at 900 °C for 970 s in an atmospheric-pressure furnace purged by pure N_2O gas with a flow rate of 7200 sccm. The N_2O oxidation provided a slower oxidation rate and hence a thinner oxide layer than what the O_2 oxidation would have provided under the same process conditions. X-ray photoelectron spectroscopy (XPS) analysis showed that less than one atomic percentage (< 1 at. %) of nitrogen was incorporated in the oxide thin film. The as-grown thickness of this tunnel-oxide layer was 4.7±0.1 nm measured by spectroscopic Ellipsometry. After the tunnel-oxide growth, the wafers were shipped to another laboratory for the formation of silicon nanocrystals.

The silicon nanocrystal formation was done in an ultrahigh vacuum (UHV) system which comprises an electron-beam evaporation system, an *in-situ* rapid thermal annealing (RTA) chamber, and an *in-situ* XPS (PHI 5000) system with a non-monochromatic Mg $K\alpha$ x-ray ($h\nu$ = 1253.6 eV) source. Before their entry into the UHV system, the samples were rinsed by deionized (DI) water, partially etched in dilute HF for 10 s, rinsed in DI water again, and blown dry with pure nitrogen. The final tunnel-oxide thickness was measured 4.0±0.1 nm across the wafer by a stand-alone spectroscopic Ellipsometer (J.A. Woollam).

After loaded into the UHV environment, the samples were annealed *in situ* at 400 °C for 10 minutes to remove absorbed water and hydrocarbon contaminations. And then a 0.9–3.5 nm thin amorphous silicon (*a*-Si) layer was deposited at room temperature by e-beam evaporation. The evaporation source was a silicon rod 0.25 inch in diameter. The tip of the silicon rod was approximately 75 cm away from the sample stage, and a shutter was installed in between to start/stop the deposition. The e-beam current was kept at 110 mA, and the silicon deposition rate was about 0.01 nm per second estimated by a crystal thickness monitor.

After the *a*-Si deposition, the samples were heated *in situ* by a set of halogen lamps. The temperature ramping rate was 500 °C/min, and a vacuum of 4×10^{-8} Torr or less was maintained throughout the annealing. A variety of annealing temperature (700–850 °C) and annealing durations (1–10 min) were evaluated for the silicon agglomeration and nanocrystal formation. *In-situ* XPS analysis was performed after each step to investigate the surfaces of interests. Figure 5.1 illustrates the main steps of the thermally-induced silicon agglomeration process. The experimental conditions are summarized in a split table (Table 5.1).

After the *in-situ* processing in vacuum, samples were removed from the UHV system and then analyzed *ex situ*. Atomic force microscopy (AFM) measurements were made on samples using a Digital Instruments Nanoscope III system which operated under a tapping mode with silicon probes (typical tip radius <7 nm). A Hitachi S-4700 scanning electron microscope (SEM) was used to take micrographs of the agglomerated Si dots on the surface. The dot size and density were estimated by a digitalized program with the SEM or AFM images. Cross-sectional samples were made using a low-angle ion-milling technique. Structures of the ultrathin *a*-Si film and agglomerated silicon nanocrystals were investigated by a JEOL JEM-2100F field-emission transmission electron microscope (FE-TEM) operating at 200 keV. Some samples were also analyzed by an *ex-situ* XPS (PHI 5500) system with a monochromatic Al $K\alpha$ x-ray ($h\nu$ = 1486.6 eV) source.

In order to clarify the effects of surface-oxide passivation on silicon agglomeration behaviors, several post-deposition treatments were tested. Table 5.2 lists three samples treated with *ex-situ* and/or *in-situ* oxidation steps. The detailed experimental procedures for each sample are described as follows.

One control sample (ISP1316) was deposited with a 3.5-nm *a*-Si layer and then removed from UHV without taking the *in-situ* RTA step. This wafer was then cut into small pieces for the surface analyses. One of the cut samples was annealed *ex situ* in N_2 ambient at 850 °C for 5 min using an AG Associates Heatpulse 410 rapid thermal processor. The wafer was firstly heated at 250 °C for 1 min to remove the surface moisture, and then the temperature was ramped to 850 °C with a ramping rate of 9 °C/s. After *ex-situ* RTA the surface morphology of the top silicon layer was measured by AFM. *Ex-situ* XPS measurements were also made to explore the surface before and after the N_2 RTA step.

In another test, a sample (ISP1328) was removed from the UHV chamber after depositing a 5-nm-thick *a*-Si film on the tunnel-oxide/Si(100) substrate. The sample was then immersed into a freshly prepared sulfuric acid hydrogen peroxide mixture (SPM) of H_2SO_4 and H_2O_2 (3:1) for 10 min, which led to a chemical-oxide growth on the *a*-Si layer. Afterward, the chemical oxide was removed by a dilute-HF dip for 2 min. The exposure of a clean silicon surface was verified by its hydrophobic property. After a DI water rinse and N_2 blow dry, the wafer was put back into the UHV system and annealed *in situ* at 850 °C for 5 min. The sample was then investigated by AFM and SEM surface analyses.

The *in-situ* oxidation of the ultrathin *a*-Si layer was also tested. A 3.5-nm-thick *a*-Si layer was deposited on a tunnel-oxide/Si(100) substrate (sample ISP1329) and subsequently oxidized *in situ* under a low pressure condition. The oxidation was done at 650 °C for 20 min. During the oxidation, pure oxygen gas was purged into the chamber with a flow rate of 0.25 SLM, and the chamber was maintained at a low pressure of 12 milli-Torr by a turbo-molecular pump. After the low-pressure oxidation, the sample was annealed under UHV at 850 °C for 5 min. The effects of the surface oxidation on the silicon agglomeration were then investigated by AFM measurements.

5.3 Results and Discussion

5.3.1 *in-situ* XPS Investigation of the Si-Nanocrystal Self-Assembly

Figure 5.2 shows the evolution of the O 1*s* and Si 2*p* XPS spectra during the *a*-Si deposition on SiO_2/Si and the following *in-situ* annealing. All peaks were referenced to the Si^{4+} 2*p* (Si-O) peak at binding energy of $E_B = 103.3$ eV. The energy separations between the O 1*s* and Si^{4+} 2*p* peaks remained the same ($\Delta E_B = 429.3$ eV) throughout the process, indicating no chemical or structural changes in the tunnel oxide layer [118]. The initial spectrum (line 1 in Fig. 5.2) features the O 1*s* and Si^{4+} 2*p* peaks for the tunnel-oxide and a smaller Si^0 2*p* peak at $E_B = 99.1$ eV for the Si substrate. In the next spectrum (line 2) recorded with a 3.5-nm *a*-Si overlayer, the O 1*s* and Si^{4+} 2*p* peaks attenuated while the Si^0 2*p* signals increased. The reduction of the oxide signals was caused by the photoelectron scattering in the top *a*-Si layer which also provided additional Si^0 2*p* signals.

The attenuation in O 1*s* signals can be weighed to assess the Si deposition uniformity. In the following calculations a straight-line approximation is adopted, in which the XPS signal attenuation through a material is described by the exponential decay [49]. This assumption has been confirmed experimentally [120] and theoretically by a Monte Carlo simulation [81]. Considering a two-layer *a*-Si/oxide structure on a Si substrate, the XPS intensity of signals from the oxide interlayer can be given by the following equation [121]:

$$I = \Phi A \sigma y D T(E) \cos(\theta) x N \lambda_{ox} \times \{1 - \exp[-T_{ox}/\lambda_{ox}\cos(\theta)]\} \times \exp[-T_{a\text{-Si}}/\lambda_{a\text{-Si}}\cos(\theta)]. \quad (5.1)$$

In this equation, Φ is the x-ray dose at the surface of the sample; A is the asymmetry parameter, dependent on the angle between the axis of the analyzer and the x-ray source; σ is the cross section for the photoelectric effect; y is the efficiency of production in the photoelectric process to give photoelectrons of normal energy in the tunnel-oxide layer; $DT(E)$ is the detector efficiency and transmission function for the kinetic energy corresponding to the specific chemical state (x-ray photoelectron transition); x is the fraction of atoms in the tunnel-oxide layer responsible for the photoelectron transition; N is the atomic density in the oxide interlayer; λ_{ox} and $\lambda_{a\text{-Si}}$ are the photoelectron effective attenuation lengths in the tunnel-oxide and in the *a*-Si, respectively; T_{ox} and $T_{a\text{-Si}}$ represent the tunnel-oxide thickness and the *a*-Si thickness, respectively; and θ is the angle between the axis of the analyzer and the normal to the surface [121].

Considering that only the *a*-Si thickness would vary during its deposition, equation 5.1 can be simplified into the following form:

$$I = I_0 \times \exp[-T_{a\text{-Si}}/\lambda_{a\text{-Si}}\cos(\theta)], \qquad (5.2)$$

or

$$I/I_0 = \exp[-T_{a\text{-Si}}/\lambda_{a\text{-Si}}\cos(\theta)]. \qquad (5.3)$$

In these equations, I_0 represents the intensity of XPS signals acquired before the *a*-Si top-layer deposition. Equation 5.3 is derived based upon the assumption that the *a*-Si layer is continuous and uniform without any pinholes or hillocks. If pinholes or hillocks do exist in the film, the XPS intensity will be an integral of signals from localized areas on which the *a*-Si thickness varies and can not be represented by a single term.

Figure 5.3(a) shows the XPS core-level O 1*s* spectra recorded during the *a*-Si deposition on the tunnel-oxide/Si substrate. The O 1*s* peak intensity, which is obtained by integrating the peak area, attenuates with the increase of *a*-Si thickness. By plotting the normalized O 1*s* intensities as a function of the *a*-Si thickness on a logarithmic scale, as shown in Fig. 5.3(b), a linear dependence for the silicon deposition is observed. This observation indicates a layer-by-layer growth of the *a*-Si thin films [122]. The cross-sectional TEM micrograph in Fig. 5.3(c) confirms the uniformity of a 3.5-nm as-deposited Si layer. AFM measurements made on the *a*-Si surface have shown a root-mean-squared roughness of 0.12 nm, which is close to the original tunnel-oxide surface roughness (~0.1 nm). Therefore the e-beam evaporation of Si has resulted into smooth and uniform *a*-Si layers on top of the tunnel-oxide/Si substrates.

After *in-situ* RTA of the ultrathin *a*-Si layer, however, the XPS intensity of the oxide-interlayer signals was partially recovered, as indicated by the last three spectra (3–5) in Fig. 5.2. After *in-situ* annealing a 3.5-nm *a*-Si layer on the tunnel-oxide/Si substrate at 850 °C for 1 minute, the O 1*s* and Si^{4+} 2*p* intensities rebounded while the Si^{0} 2*p* signal decreased (line 3 in Fig. 5.2). This observation can be explained by the Si coalescence and subsequent nanoparticle formation which, as a result, partially exposed the tunnel-oxide surface and hence increased the O 1*s* and Si^{4+} 2*p* photoelectron yields. The decreased Si^{0} 2*p* photoelectron yield was due to the reduced surface coverage by Si and the signal attenuation in taller Si islands. SEM analyses later confirmed the formation of separated Si nanoparticles, as shown in Fig. 5.4. Samples annealed for different durations (1–10 min) had nearly identical O 1*s* and Si^{4+} 2*p* peaks in the spectra 3–5 of Fig. 5.2, implying few changes in the nanoparticle topology. Indeed their SEM images revealed similar dot sizes and densities. For example, Figs. 5.4(a) and 5.4(b) present SEM images of samples annealed *in situ* at 850 °C for 1 min and 10 min, respectively. The dot densities and base radii extracted by analyzing SEM micrographs are summarized in Figure 5.5. In correspondence to the *in-situ* XPS results, different annealing periods have resulted into similar nanoparticle densities of approximately 8×10^{10} cm^{-2} with average base radii around 11 nm. Therefore it is believed that most of the silicon agglomeration has completed after the first minute of annealing. It should be noted that in Fig. 5.2(b) a larger Si 2*p* chemical shift was observed between the Si^{4+} and Si^{0} peaks after the *in-situ* annealing. This is possibly due to the differential charging between the Si nanoparticles and the tunnel-oxide surface during the x-ray irradiation [118]. The broadened Si^{0} 2*p* peaks along with the change of the Si^{0} 2*p* peak shape (for example a shoulder at the lower E_{B} side) are also indicative of possibly nonuniform charging among the Si nanoparticles.

5.3.2 Effects of the Annealing Temperature on the Silicon Agglomeration and Nanocrystal Formation

In order to investigate the Si agglomeration behaviors, different RTA temperatures have been tested for the *in-situ* annealing. 3.5-nm-thick *a*-Si layers were annealed at different temperatures (700, 750, 800, and 850 °C) for 5 min. A constant annealing duration of 5 min was used in order to limit the thermal budget in the process. The capability of the UHV system was also considered while setting the experimental variables. For example, the annealing temperature at 850 °C was close to the highest temperature that could be handled by the currently-used *in-situ* RTA system.

The dot densities and mean sizes were taken by SEM as a function of the annealing temperature, as shown in Fig. 5.6. Figures 5.6(a), 5.6(b), and 5.6(c) show SEM images of samples annealed at 750, 800, and 850 °C, respectively. The sample annealed at 700 °C did not reveal resolvable features in the SEM analysis. When the annealing temperature was at 750 °C or higher, however, evidence of Si-dot agglomeration was observed in the SEM results. Figure 5.7 summarizes the dot densities and base radii as a function of the annealing temperature. The first impression was that using a reduced annealing temperature would result into a smaller

Si-dot density and a larger averaged dot size, although the changes in the dot densities and sizes were not significant.

However, AFM analysis with the sample annealed at 750 °C has revealed an incomplete agglomeration of silicon, as shown in Fig. 5.8(b). Therefore the dot size and density observed by SEM for this specific sample can not represent the real results of a complete dot agglomeration process.

Figures 5.8(a)–5.8(d) show AFM scan images (1 μm by 1 μm) for samples annealed at different temperatures. When the annealing temperature was ≥800 °C, dense dots were observed after 5-min RTA, as shown in Figures 5.8(c) and (d). When the annealing temperature was ≤700 °C, no silicon dot could be found under SEM, and AFM analysis showed an rms surface roughness less than 0.2 nm. Figure 5.8(a) shows the AFM image of a sample annealed at 700 °C for 5 min, and the rms roughness is measured 0.18 nm, which is only 50% higher than the as-deposited *a*-Si roughness (0.12 nm). This observation suggests that an annealing temperature lower than 700 °C either is not enough to trigger the thermal agglomeration or needs an annealing duration much longer than 5 min to complete the process.

In Fig. 5.8(b) the Si-dot agglomeration is found evident after annealing at 750 °C. However, darker regions surrounding the Si dots are spotted in the AFM image, indicating recessed areas which are possibly exposed tunnel-oxide surfaces. The intermediate areas between the bright dots and the dark spots are therefore representing the flat Si surface, and it becomes clear that the agglomeration process is incomplete with this sample. The *in-situ* annealing at 750 °C did start the Si-dot formation in a 3.5-nm *a*-Si film, but the annealing time of 5 min was not enough for the entire film to completely agglomerate into nanoparticles. Figure 5.9(a) shows a magnified portion of the AFM image, with the cross-sectional surface profile along the Y–Y' line plotted in Fig. 5.9(b). The recessed area is labeled and correspondingly marked in the cross-sectional plot by two dashed lines. The height differences between the recessed areas and the flat silicon surfaces are approximately 2–4 nm, showing consumption of Si top layer. Considering the original Si thickness of 3.5 nm, the surface coalescence of the Si film can contribute to a rougher surface and a less uniform thickness. It is noteworthy that a slightly thicker edge can be observed along the remaining Si film, which coincides with the void-edge thickening observed and discussed in the thermally-induced de-wetting of ultrathin SOI films [48, 123, 124].

Some small dots on the flat-Si regions are observed in Fig. 5.8(b), which suggest the nucleation of Si nanoparticles on a clean surface. Figure 5.10(a) shows a magnified AFM image, with a cross-sectional profile along the X–X’ line plotted in Fig. 5.10(b). The X–X’ line is placed through the middle of a small dot on the Si surface. It is obvious in the AFM profile that a Si dot has agglomerated on a relatively flat silicon surface, possibly due to the surface migration and nucleation of Si atoms. The surface diffusion and nucleation of Si have been studied in explaining the HSG formation on a thick *a*-Si film [23, 39, 40]. In present study, the dot formation on the Si surface can be also resulted from similar mechanisms.

Figure 5.11 shows cross-sectional high-resolution TEM (HR-TEM) images of the sample appeared in Fig. 5.8(b). A separated Si nanocrystal on the tunnel-oxide layer is observed. The nanocrystal is formed after annealing a 3.5-nm *a*-Si film *in situ* at 750 °C for 5 min, and the self-assembly of crystallized Si nanoparticles is evident under HR-TEM. Because there seems no remaining *a*-Si layer in Fig. 11(a), the image is supposedly taken from within the dark (recessed) areas in Fig. 5.9, where the Si top layer has been consumed and transformed into nanoparticles. The shape of the nanocrystal is nearly hemispherical or like a truncated-sphere [125]. The Si nanocrystal, which has a lateral size of 17 nm, clearly shows a twin boundary in its structure. Figure 5.11(b) shows a blown-up image and marks the twin boundary with a dash line, with two arrows indicating two mirrored arrays of Si atoms. When thinner *a*-Si layers were annealed, smaller Si nanocrystals with single-crystal structures would be obtained. The effects of initial *a*-Si thickness on the agglomerated nanocrystal properties will be discussed later in section 5.3.4.

Figure 5.12 shows another HR-TEM image of the same sample appeared in Fig. 5.8(b). Different from what is observed in Fig. 5.11, there is a remaining *a*-Si layer beneath the Si nanocrystal in this micrograph. Therefore one can assume that Fig. 5.12 is more representative of a partially agglomerated Si dot on the silicon surface, as being the case in Fig. 5.10. There are two observations of Fig. 5.12 which may provide insights of the Si agglomeration behavior. First, there are amorphous regions at the sides of the hemispherical crystal. The diffusing Si atoms may migrate along the Si-dot surface and accumulate near the edge before eventually aligned and crystallized with the nucleated core. Second, the crystallized structure in the middle of the dot has propagated into the underlying *a*-Si layer, forming a curved interface between the crystal and the *a*-Si layer. This suggests that the nanocrystal growth could have started at nucleation sites near the *a*-Si surface. After the surface nucleation the nanocrystal can grow along two fronts. One is the re-crystallization process propagating into the underlying *a*-Si thin film. The other is the alignment of impinging Si atoms, which can migrate on a clean surface while thermally activated, to the crystalline structure.

Briefly, a 5-min RTA at 750 °C did start the thermal agglomeration process in a 3.5-nm *a*-Si layer, but it was not enough to transform the entire film into separate nanocrystals. A longer annealing time should be needed if the thermal agglomeration process had to be completed at 750 °C. In the following experiments, an *in-situ* RTA at 850 °C for 5 min was used for the Si-nanocrystal formation, unless specified otherwise.

5.3.3 Effects of the Native Oxide Growth on the Silicon Agglomeration and Nanocrystal Formation

If the thermal agglomeration technique is to be integrated into the Si-based semiconductor manufacturing process, it will be important to consider its integration capabilities with other processing steps. Unlike the bottom-up CVD techniques, which randomly deposit Si dots all over the wafer surface, the thermal agglomeration technique has the potential of selectively patterning the initial *a*-Si layer prior to the vacuum annealing. Therefore it becomes possible to confine the dot formation in selected areas with a top-down, subtractive process. However, adding process steps in between the *a*-Si deposition and vacuum annealing steps would expose the wafer to air and therefore grow a thin native oxide on the *a*-Si surface. It has been emphasized that a clean surface is critical for the HSG formation, and surface oxide passivation can severely inhibit the surface diffusion and nucleation of Si atoms [23, 126]. In this section, different oxidation/annealing conditions are tested, and effects of the surface oxide growth on the nanocrystal agglomeration are discussed. It is found that a dilute-HF dip before the vacuum RTA is efficient to remove the surface oxide and ensure Si-dot agglomeration.

Ex-situ RTA in N_2 ambient

A 3.5-nm *a*-Si layer was deposited on a tunnel-oxide/Si substrate and then annealed *ex situ* at 850 °C for 5 min in N_2. AFM measurements were made to determine the silicon surface roughness before and after the N_2 RTA. Table 5.3 lists the rms roughness data. The roughness is approximately 0.09 nm after the N_2 RTA, close to the as-deposited *a*-Si roughness (~0.12 nm). It is believed that a native oxide layer grown in air or during the N_2 RTA has prevented the *a*-Si film from coalescence and agglomeration.

Figure 5.13 shows O 1s and Si 2 p spectra acquired by *ex-situ* XPS analysis before and after the N_2 RTA. Normally after a silicon sample is exposed to air, a native oxide layer growth occurs on the surface. Therefore it is reasonable to assume that a native oxide on *a*-Si has contributed to the oxide signals in the XPS spectrum for the as-deposit sample. Intensities of the oxide peaks (O 1*s* and Si^{4+} 2*p*) slightly increased after the N_2 RTA. This implies an oxide re-growth during the RTA procedure. A small amount of residual oxygen may have existed in the RTA processor chamber and reacted with the *a*-Si surface during the N_2 RTA. Atmosphere moisture, which is usually absorbed on the wafer surface or on the chamber walls, can also contribute to the oxide re-growth. In Fig. 5.13(b) the silicon peak (Si^0 2*p*) shows no distinguishable changes, which indicates that only a very small amount of *a*-Si is oxidized during the RTA. The XPS analysis is more sensitive to the native oxide re-growth than it is to the silicon consumption because the native oxide is the very top layer which has the most efficient photoelectron response.

In-situ oxidation in low-pressure O_2

In order to verify that the silicon agglomeration is hindered by the surface oxide bonding, an *in-situ* oxidation test was performed. A sample was deposited with a 3.5-nm *a*-Si layer and then moved to another chamber without breaking vacuum. The sample was then oxidized under a low-pressure condition. The oxidation was performed at 650 °C for 20 min, while the chamber was purged with pure O_2 flow (250 sccm) and maintained at 12 milli-Torr. After the low-pressure oxidation, the sample was moved back to the RTA chamber (without breaking vacuum) for an *in-situ* annealing at 850 °C for 5 min.

Figure 5.14 shows O 1s and Si 2 p spectra acquired by *in-situ* XPS analysis after each step. Measurements on the as-deposited *a*-Si have shown small oxide peaks (O 1*s* and Si^{4+} 2*p*) which can be attributed to the tunnel-oxide interlayer. The energy separation (ΔE_B) between the O 1*s* and Si^{4+} 2*p* peaks reads 429.3 eV. The same ΔE_B value is also observed with the *a*-Si/oxide/Si samples discussed in section 5.3.1. After the low-pressure oxidation at 650 °C, the O 1*s* intensity increases significantly due to oxide growth. The decrease of the Si^0 2*p* peak intensity is also a result of the silicon consumption and the top-oxide growth. After the oxidation the O 1*s* peak position shifts toward a smaller binding energy. The Si 2*p* oxide peak also appears to have a tail on the lower-E_B side after the oxidation. These observations can be attributed to the existence of sub-oxides, or sub- stoichiometric SiO_2 (SiO_x or Si^{n+} where n=1, 2, 3) [118]. A multi-peak fit of the Si 2*p* spectrum recorded after oxidation reveals a combination of Si^0, Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+} peaks, as shown in Fig. 5.15. It appears that the oxidation at a relatively low temperature has produced a transition layer of sub-oxides.

After *in-situ* annealing of the partially oxidized silicon film, the XPS spectrum only shows a small increase in the peak intensities for all peaks in Fig. 5.14. The peak shapes and positions stay the same. AFM analysis on the sample shows no Si-dot formation. The rms roughness is measured 0.16 nm (sample 1329 in Table 5.3), which is only a little rougher than the as-deposited *a*-Si surface (0.12 nm). The surface may have been roughened by the *a*-Si crystallization during RTA. A slightly rougher morphology can hence provide more surface responses to the XPS detector and increase the peak intensities. In brief, the surface oxide layer, even a low quality one, can effectively inhibit the agglomeration of silicon nanodots.

Surface cleaning prior to the *in-situ* RTA

A 5-nm *a*-Si film was immersed into an SPM solution to grow chemical oxides on it and then dipped in dilute-HF for the oxide removal. The sample was then immediately loaded back into the UHV system for the vacuum RTA at 850 °C for 5 min (see sample 1328 listed in Table 5.3).

Figure 5.16 shows O 1s and Si 2 p spectra taken by *in-situ* XPS analysis before and after the chemical-oxide growth/removal treatments. A decrease of the Si^0 $2p$ peak (E_B = 99.3 eV) and increases of the oxide peaks (O $1s$ and Si^{4+} $2p$) are observed after the SPM+HF treatments. These observations are attributed to the *a*-Si thickness reduction, which also allows more photoelectrons from the oxide interlayer to be detected. Obvious the growth of chemical oxides has consumed the *a*-Si top layer and reduced its thickness. It is worth noting that a tail of the O $1s$ peak (on the lower-E_B side) is found after the SPM+HF treatments. Figure 5.17 shows curve-fitting results for the O $1s$ peak. Two components are extracted (peaks at 532.8 and 531.4 eV) while the entire spectrum is referenced to the Si^0 $2p$ line at E_B = 99.3 eV. The O $1s$ peak component at 532.8 eV is attributed to the tunnel-oxide interlayer. The other O $1s$ component at the peak position of 531.4 eV can be indicating hydroxyl groups or hydroxide contaminations on the *a*-Si surface [52].

Figures 5.18 and 5.19 show the SEM and AFM results taken on the sample after the 850 °C vacuum RTA. The rms roughness is approximately 4.9 nm measured by AFM, as listed in Table 5.3 (sample 1328). The thermal agglomeration of silicon dots is evident, even though the sample has been through *ex-situ* treatments prior to the vacuum RTA. Therefore one can conclude that this agglomeration technique is applicable even after the sample has been exposed to air for additional process steps, provided that the native oxide is removed prior to the vacuum annealing. One can also envision the possibility of removing the *a*-Si in selected areas by a subtractive process before the vacuum annealing; thus Si agglomeration and nanocrystal formation can be confined in selected areas. Though the additional photolithography and *a*-Si etching steps may increase the manufacturing costs, which is a trade-off.

5.3.4 Dependence of Nanocrystal Sizes and Densities on the Initial *a*-Si Thickness

Figure 5.20(a) shows an SEM image of Si nanoparticles agglomerated after *in-situ* annealing of a 3.5-nm-thick *a*-Si layer. The size distribution of Si dots observed under SEM is summarized in Fig. 5.20(b). There is one group of larger dots, with their base radii around 10–14 nm. Also there is another group of smaller dots with base radii around 4–8 nm. This bimodal size distribution has been reported in studies of the thermally-induced island formation with *a*-Si [42, 43] or SOI [47] thin films, and it can be explained by a multi-stage agglomeration process.

In the first stage nucleation centers (seeds) are created on the silicon surface by strain relaxation in the form of defects or micro-roughness [40]. Then the three-dimensional aggregation of Si atoms forms small hemispherical crystallites on the Si surface, as shown in Figures 5.10 and 5.12. The aggregation requires surface atoms to migrate; therefore it is critical to maintain a clean Si surface. The hemispherical crystallites grow laterally when the impinging atoms merge into the crystal structure [23]. The crystallites also act as seeds and re-crystallize the underneath *a*-Si. In other word, the growth of crystallites also propagates from the *a*-Si surface toward the *a*-Si/oxide interface. The crystal growth eventually reaches down to the *a*-Si/oxide interface and depletes the surrounding *a*-Si film, which partially exposes the oxide surface. Thermodynamically the amorphous-crystal phase transition decreases the free energy, but the creation of crystalline-Si/oxide interfaces also increases the interface energy. In addition, the surface migration of Si atoms is limited by the thermal diffusion length. Therefore a critical nanocrystal size will be obtained when the free energy changes no longer favor the crystal growth. A group of larger Si dots are formed when Si atoms are sufficiently supplied until the critical size is approached. Some remaining *a*-Si will then agglomerate into a second group of nanocrystals whose sizes are smaller because of inadequate Si atoms.

Figures 5.21(a) and 5.22(a) present SEM images of Si dots agglomerated from initially 2.5-nm and 1.8-nm *a*-Si layers, respectively. The dot size distributions are plotted in Figures 5.21(b) and 5.22(b). It appears that thinner *a*-Si layers have resulted into smaller and denser nanoparticles, in agreement with the experimental and theoretical studies on the thermal agglomeration of ultrathin silicon films [42, 48]. The bimodal size distribution can still be seen, for example, in Fig. 5.22(b).

Cross-sectional TEM analysis has again verified the hemispherical shape of Si nanocrystals. Figure 5.23(a) shows an annular dark-field scanning TEM (ADF-STEM) image of the Si dots self-assembled from a 1.8-nm-thick *a*-Si film. It is clearly shown that hemispherical Si dots are distributed on the tunnel-oxide layer and separated from each other. Some seemingly merged dots are actually separated but with their images overlapped in the plane of focus. HR-TEM images of nanocrystals are also taken, as shown in Figures 5.23(b)–(d). Clear lattice fringes are observed. For example, in Fig. 5.23(c) the lattice spacing of 0.313 nm coincides with that of the Si (111) planes. The single-crystal structures in these photos suggest that more single-grain nanocrystals are formed with the thinner (1.8 nm) *a*-Si layer.

Figure 5.24 shows an AFM image of Si dots self-assembled after annealing a 0.9-nm-thick *a*-Si film. The rms roughness is 0.55 nm. The Si dots on this sample are so small that SEM encounters difficulties resolving the features. Therefore AFM analysis is used to evaluate the dot size and density. Si nanoparticles with a density as high as 3.9×10^{11} cm^{-2} and a mean radius of 5.1 nm were observed by using AFM. However, it should be noted that AFM technique can potentially introduce probe artifacts. When an pyramidal AFM tip goes over a nanoparticle attached to a flat surface, the side of the tip may interact with the nanoparticle and hence cause broadening features in the image [127]. Besides, the proximity of neighboring small nanoparticles can appear as a larger dot in scanning probe microscopic images [62]. Thus the mean size obtained by AFM is possibly overestimated, with the density possibly underestimated.

Figure 5.25 summarizes the nanocrystal dot densities and base radii as a function of the initial *a*-Si layer thickness. After an *in-situ* RTA at 850 °C for 5 min, the thinner *a*-Si resulted into denser and smaller Si nanocrystals. This result provides a simple route of the nanocrystal size and density control. Studies on the surface-energy instabilities have also suggested that the size and density of agglomerated dots are mainly determined by the initial Si thickness [42, 48]. Wakayama *et al*. [42] have discussed the mechanism of Si-island formation from a thin silicon film in relation to the free energy of the Si/SiO_2 system. Agglomeration of the Si crystallite occurred forming Si islands, thus preventing a further increase in free energy. In our work, however, a higher dot density has been obtained, which can be attributed to the use of RTA instead of the equilibrium annealing conditions used by Wakayama and co-workers. In addition, Nuryadi *et al*. [45] have studied the thermal agglomeration of single-crystalline silicon-on-insulator (SOI) layers. They also found that the size of agglomerated islands increased with increasing SOI film thickness, and that the critical agglomeration temperature was lower for the thinner SOI film. In our study, a much higher dot density was obtained by annealing a thin *a*-Si layer. The crystalline structure of SOI has fewer defects and stronger atom-to-atom bonding energy, which could alter the localized agglomeration behavior of Si.

5.3.5 Estimation of the Si-Nanocrystal Size and Density by *in-situ* XPS Analysis

In this section a simple model is established to estimate the Si-dot size by using *in-situ* XPS analysis results. After the nanocrystal size is extracted from XPS data, the dot density can be calculated accordingly.

Figure 5.26 is a schematic showing one unit area of a silicon film. The *a*-Si film is deposited over a tunnel-oxide layer, and therefore any photoelectron signals from the oxide interlayer must go through the Si top-layer. After *in-situ* annealing, presumably all the *a*-Si atoms in the unit area agglomerate into one hemispherical dot, and the oxide surface becomes partially exposed. Figure 5.27 shows schematics of an agglomerated dot in the unit area.

To simplify the discussion, some assumptions are made here:

1. The mass conservation of the Si top layer holds true during the annealing process. There is neither reaction nor evaporation in the Si/SiO_2 system but only the deformation of the top Si film.
2. Silicon densification during the amorphous-crystal phase transition is neglected. A constant ratio can be added to the equations in order to address the volume reduction due to *a*-Si re-crystallization. It should be noted, however, that the electron attenuation lengths in *a*-Si and crystalline-Si may differ.
3. The nanocrystals are considered as perfect hemispheres in one size. The crystal facets and the dot-size/shape variations are neglected. However, if a certain size-distribution function has to be considered, the calculations can be easily modified into a statistical sum of different terms.
4. The assumed photoelectron take-off angle is 90 degree, i.e., the axis of the XPS analyzer is normal to the sample surface. Therefore in equation 5.1 the variable θ can be substituted with a zero. This is not really the

case for our *in-situ* XPS setup. Though this assumption can help dodging some surface-scattering issues in the following calculations.

Using equation 5.2 with the assumptions mentioned above, XPS signals coming from the oxide interlayer which is covered by a Si cap can be expressed by the intensity I_1:

$$I_1 = I_0 \times \exp(-T_{Si}/\lambda_{Si}), \tag{5.4}$$

where T_{Si} is the Si-capping thickness, as shown in Fig. 5.26, and λ_{Si} is the attenuation length for photoelectrons of a specific kinetic energy in silicon. After *in-situ* annealing, the geometry in the unit area is changed (see Fig. 5.27), and the oxide signals can be expressed by the intensity I_2:

$$I_2 = I_0 \times \left(\frac{L^2 - \pi R^2}{L^2} \right) + \int_{r=0}^{r=R} I_0 \times \exp\left(\frac{-\sqrt{R^2 - r^2}}{\lambda_{Si}} \right) \times \frac{2\pi r \cdot dr}{L^2}, \tag{5.5}$$

where R is the Si-dot radius, and the radial integral of r starts from the base center of the dot towards its edge. According to the schematic plot in Fig. 5.27(b), the variable r can be substituted using the following relation:

$$r = R \times \cos(\alpha). \tag{5.6}$$

Therefore, equation 5.5 can be modified and become the following form:

$$\frac{I_2}{I_0} = 1 - \pi \left(\frac{R}{L} \right)^2 - 2\pi \left(\frac{R}{L} \right)^2 \times \int_{\alpha=\frac{\pi}{2}}^{\alpha=0} \cos(\alpha)\sin(\alpha) \times \exp\left[\frac{-R\sin(\alpha)}{\lambda_{Si}} \right] \times d\alpha. \tag{5.7}$$

A temporary variable $x = \sin(\alpha)$ can be used here, and equation 5.7 becomes this:

$$\frac{I_2}{I_0} = 1 - \pi \left(\frac{R}{L} \right)^2 - 2\pi \left(\frac{R}{L} \right)^2 \times \int_{x=1}^{x=0} x \times \exp\left(-\frac{R}{\lambda_{Si}} x \right) \times dx. \tag{5.8}$$

Using the formula $xe^{cx}dx = d\,[c^{-2}e^{cx}(cx-1)]$, where c is a constant, one can obtain the following result:

$$\frac{I_2}{I_0} = 1 - \pi \left(\frac{R}{L} \right)^2 + 2\pi \left(\frac{\lambda_{Si}}{L} \right)^2 \times \left[1 - \left(\frac{R}{\lambda_{Si}} + 1 \right) \times \exp\left(-\frac{R}{\lambda_{Si}} \right) \right]. \tag{5.9}$$

Here we assume that silicon atoms have been conserved during the thermal agglomeration process, i.e., the volume of the hemispherical dot equals the original film volume within the unit area:

$$L^2 \times T_{\mathrm{Si}} = 2\pi R^3/3,\ \text{or}\ L^2 = (2\pi/3)\times(R^3/T_{\mathrm{Si}}). \qquad (5.10)$$

In order to simplify the calculations, the dot radius R is defined as a multiplication of original Si thickness T_{Si}:

$$R = (k \times T_{\mathrm{Si}}), \qquad (5.11)$$

where k is a constant. Substituting equations 5.4, 5.10, and 5.11 into equation 5.9 results into the following expression:

$$\frac{I_2}{I_0} = 1 - \frac{3}{2k} + \frac{3}{k^3} \times \left[\ln\left(\frac{I_1}{I_0}\right)\right]^{-2} \times \left\{1 - \left[1 - k \cdot \ln\left(\frac{I_1}{I_0}\right)\right] \times \left(\frac{I_1}{I_0}\right)^k\right\}. \qquad (5.12)$$

The XPS intensities I_0, I_1, and I_2 can be obtained by recording the O 1*s* spectrum before the *a*-Si deposition, after the deposition, and after the *in-situ* RTA, respectively. Then a constant k can be found by fitting equation 5.12 with the measured XPS data, and the size of agglomerated Si-dots can be estimated by equation 5.11. After inspecting Fig. 5.27(a), one can define the Si-dot surface coverage ratio, S, in the expression of $\pi R^2/L^2$ and use equations 5.10 and 5.11 to draw the following result:

$$S = \frac{\pi R^2}{L^2} = \frac{3}{2} \times \frac{T_{Si}}{R} = \frac{3}{2k} \times 100\%. \qquad (5.13)$$

As equation 5.13 shows, this simple model can estimate the surface coverage ratio of Si dots once the constant k becomes available. Also the dot density, D, can be stated as the reciprocal of the unit area and transformed into the following equation:

$$D = \frac{1}{L^2} = \frac{3}{2} \times \frac{T_{Si}}{\pi R^3} = \frac{3}{2\pi k R^2}. \qquad (5.14)$$

Figure 5.28 shows calculated results based on the model and *in-situ* XPS data. A silicon layer of 1.8 nm was deposited. The XPS O 1*s* intensities were measured before and after the *a*-Si deposition to fill in I_0 and I_1 in equation 5.12. After *in-situ* RTA of the film, Si nanodots were formed and the intensity of the O 1*s* peak was measured again. Comparing the measured data with the calculated results plotted in Fig. 5.28, a k ratio of 4.4 is obtained, and a dot radius of 7.92 nm with a dot density of 1.73×10^{11} cm^{-2} are predicted by this model. SEM analyses on the same sample have revealed an averaged dot radius of 6.65 nm and a dot density of 1.71×10^{11} cm^{-2}. The predicted dot size is larger than the dot size measured by SEM. This may be explained by the volume reduction of *a*-Si re-crystallization. One should note that the volume densification during the amorphous-crystal transition is not taken into consideration by current model. However, it is noteworthy that we have observed a 15–16 % thickness reduction after a 13-nm *a*-Si film was annealed *ex situ* and crystallized into an 11-nm poly-crystalline Si film. As being demonstrated, this XPS model shows a fairly good match with the experimental data, even though the model uses relatively simplified assumptions. For example, the XPS model assumes a photoelectron take-off angle of 90°, but the experimental data are actually measured at a 45° take-off angle.

Several remarks should be added here. First at all, the assumption of dot formation in a square unit area does not consider the most densely packed array which has one circular dot in contact with six others of the same circular size. Because the surface coverage ratio of Si dots is usually less than 40%, this assumption of a square-sized film is still reasonable. Actually the calculations can also begin with a hexagonal unit area and take the most-densely packed array into considerations. One can also use the mass conservation law to correlate the dot size with the area of consumed silicon film and completely ignore the shape of the area. Another interesting observation in the Si agglomeration process is the formation of smaller dots. In present model, however, dot radii smaller than the original film thickness are not addressed. Because there is only one hemispherical dot considered in the unit area, the dot radius must be higher than the initial film thickness to conserve the total silicon mass. This can be solved if multiple dots are considered in a single unit area. A distribution function can be used to define sizes for a group of dots, and adding up their XPS responses as a sum of several integral terms. Eventually a bimodal size distribution can be taken into consideration in order to find a better fit between the calculated results and measured XPS data.

5.4 Summary

In summary, hemispherical Si nanocrystals are self-assembled using a thermal agglomeration technique. Ultrathin (0.9–3.5 nm) *a*-Si films are deposited on a 4-nm tunnel-oxide layer using electron-beam evaporation. XPS analyses recorded during the *a*-Si deposition has verified a layer-by-layer deposition mode. AFM and TEM analyses have also confirmed a smooth and uniform deposition of the *a*-Si thin film. After the deposition, an *in-situ* annealing can activate the thermal agglomeration of Si and transform the ultrathin *a*-Si films into Si nanocrystals. *In-situ* XPS is used to monitor the evolution of Si deposition and agglomeration. Evidence shows that Si nanocrystals can be obtained at a moderate temperature (850 °C) within a short period of time (1–10 min), which is also confirmed by AFM and SEM analyses.

Different annealing temperatures have been tested for the Si agglomeration. Samples annealed at 700, 750, 800, and 850 °C for 5 min are checked by AFM and SEM. Annealing temperatures ≤700 °C are found inadequate to activate the dot agglomeration in a 3.5-nm thin film, at least not in the 5-min RTA period. When the *a*-Si film is annealed at 750 °C for 5 min, some incomplete agglomeration of dots is observed by AFM. Results of AFM and TEM analyses suggest that small dots are first nucleated on the surface of *a*-Si and then grow into hemispherical nanocrystals and deplete the surrounding *a*-Si. Surface analyses of samples annealed at 800 and 850 °C show densely distributed Si dots and suggest the completion of Si agglomeration after a 5-min annealing.

In order to evaluate how the surface oxide affects the Si agglomeration behaviors, different oxidation conditions are tested. For example, an *ex-situ* N_2 RTA on an ultrathin *a*-Si layer has shown no evidence of the surface coalescence and dot agglomeration. It is believed that a native oxide layer grown in air or during the N_2 RTA has prevented the *a*-Si film from coalescence and agglomeration. In another *in-situ* oxidation test, a low pressure condition was used to oxidize the surface of a 3.5-nm *a*-Si film at 650 °C. *In-situ* XPS revealed that the surface oxide was with inferior quality. The sample was then annealed in UHV at 850 °C for 5 min, but AFM analysis on this sample showed no Si-dot formation. Therefore, even an inferior surface oxide layer can still severely hinder the agglomeration of Si nanodots.

Although surface oxides can strongly affect the Si agglomeration, it is found that a dilute-HF dip before the vacuum RTA is efficient to remove the surface oxide and ensure Si-dot agglomeration. In one test, an SPM immersion was utilized to grow a chemical-oxide layer on a 5-nm *a*-Si film. Afterward, the sample was dipped in dilute-HF to remove the chemical oxides and then immediately loaded into the UHV system for the vacuum RTA. The Si-dot agglomeration is observed with this sample, even though it has been exposed to *ex-situ* treatments before the vacuum RTA. Therefore this agglomeration technique is applicable even after the thin *a*-Si film is treated with *ex-situ* processing steps, as long as the native oxide is carefully removed prior to the vacuum annealing.

In-situ annealing of *a*-Si layers with different thickness has resulted into Si nanocrystals with different sizes and densities. It appears that thinner *a*-Si layers have resulted into smaller and denser nanoparticles. This result provides a simple route of the nanocrystal size and density control. TEM analysis shows that single-crystal Si nanodots can be obtained when a thinner (1.8 nm) *a*-Si film is annealed. The *in-situ* annealing of a 0.9-nm *a*-Si layer results into Si nanodots with a mean radius of 5.1 nm and a dot density as high as 3.9×10^{11} cm^{-2}. In addition, the SEM analyses have shown a bimodal size distribution with the agglomerated nanocrystals, which can be explained by a multi-stage agglomeration process.

In the final section, a simple model is established to estimate the Si-dot size by using *in-situ* XPS analysis. The dot density and the surface coverage ratio can also be extracted with this model. In order to verify the feasibility of this model, XPS results acquired during the deposition and annealing of a 1.8-nm Si layer are used. The calculated dot density matches pretty well with the experimental result measured by SEM. The dot size predicted by this model also provides a fairly reasonable estimation while comparing it with the SEM results. As being demonstrated, the XPS model provides a method to estimate the agglomerated dot size and density *in situ*, even though the model uses relatively simplified assumptions.

There are several advantages possessed by the thermal agglomeration method for the Si-nanocrystal formation. First, well-separated hemispherical nanocrystals can be formed in a single layer. The hemispherical geometry, normally obtained only by the CVD method [96], exposes the largest cross section to the tunnel-oxide layer and leads to the most efficient charge injection when used for memory applications [10]. It is noteworthy that a 23~32% surface coverage ratio by nanocrystals was obtained in the present work, higher than the normally 15~20% coverage on SiO_2 using conventional CVD methods [128]. Second, the dot separation is completed by the agglomeration process. There is no need for an oxidation step to separate the dots, so the total silicon volume is not compromised for sufficient dot separation. Although an additional oxidation step after the dot formation may be helpful in passivating the dot surfaces [129]. Studies on the surface-energy instabilities have suggested that the size and density of agglomerated dots are mostly determined by the initial Si thickness [42, 48]. The tunnel-oxide chemical properties, which are critical for the CVD Si nanocrystal growth [113, 114], can be less crucial in this technique. Furthermore, the vacuum RTA is applicable even after the *a*-Si layer has been exposed to air and patterned by a subtractive process, as long as the Si surface is kept clean and free of native oxide before annealing. Therefore, the agglomeration of Si can be limited in selected areas, which allows nanocrystals to be selectively deployed by a top-down method fully compatible with state-of-the-art CMOS technologies. Besides, studies on the thermal agglomeration of thin silicon-on-insulator (SOI) films have shown a pattern-induced alignment of Si dots [23]. This pattern-dependent agglomeration behavior can be also expected for the ultrathin *a*-Si films on SiO_2 [48], which provides a possible route for localized Si-dot deployment.

Table 5.1 Split conditions for the Si agglomeration experiments. This table has been re-arranged for the ease of viewing. The samples are actually numbered in sequence.

ISP Sample No.		1316	1317	1339	1318	1319	1342	1326	1341	1330	1340
Initial *a*-Si thickness	3.5 nm	●	●				●	●	●	●	●
	2.5 nm			●							
	1.8 nm				●						
	0.9 nm					●					
In-situ RTA conditions	850 °C		●	●	●	●				●	●
	800 °C						●				
	750 °C							●			
	700 °C								●		
	1 min									●	
	5 min		●	●	●	●	●	●	●		
	10 min										●

Table 5.2 *Ex-situ* and/or *in-situ* post-deposition treatments. The process steps are in sequence from top to bottom. For example, the sample 1328 was removed from the UHV system after the *a*-Si deposition, immersed into freshly prepared SPM for 10 min, treated with a dilute-HF dip, and then reloaded into UHV for the *in-situ* RTA.

ISP Sample No.		1316	1328	1329
Initial *a*-Si thickness	5.0 nm		●	
	3.5 nm	●		●
Ex-situ Processing	Chemical oxide growth in SPM[*] (10 min)		●	
	Surface oxide removal (dilute-HF dip)		●	
	N_2 RTA, 850 °C, 5 min	●		
In-situ processing	Low pressure O_2 oxidation (650 °C, 20 min, under 12 mTorr)			●
	In situ RTA (850 °C, 5 min, under UHV)		●	●

[*] SPM: Sulfuric acid hydrogen peroxide mixture (3 parts H_2SO_4 + 1 part H_2O_2)

Table 5.3 Surface roughness (root-mean-squared) measured by AFM. The roughness data were obtained from 1-μm^2 AFM measurements. The experimental conditions for each sample are also listed.

Sample	Initial *a*-Si thickness	Surface treatments after *a*-Si deposition	Rms* roughness
Oxide	n/a	n/a (tunnel-oxide surface)	0.104 nm
1316	3.5 nm	n/a (as-deposited *a*-Si)	0.119 nm
1316	3.5 nm	*Ex-situ* RTA: 850 °C, 5 min in N_2 (1 atm)	0.086 nm
1329	3.5 nm	**1**. *In-situ* oxidation: 650 °C, 20 min in O_2 (12 mTorr) **2**. *In-situ* RTA: 850 °C, 5 min in UHV	0.164 nm
1328	5.0 nm	**1**. *Ex-situ* chemical-oxide growth & removal **2**. *In situ* RTA: 850 °C, 5 min in UHV	4.874 nm
1317	3.5 nm	*In situ* RTA: 850 °C, 5 min in UHV	5.038 nm
1341	3.5 nm	*In situ* RTA: 700 °C, 5 min in UHV	0.181 nm

[*] Rms: Root mean square

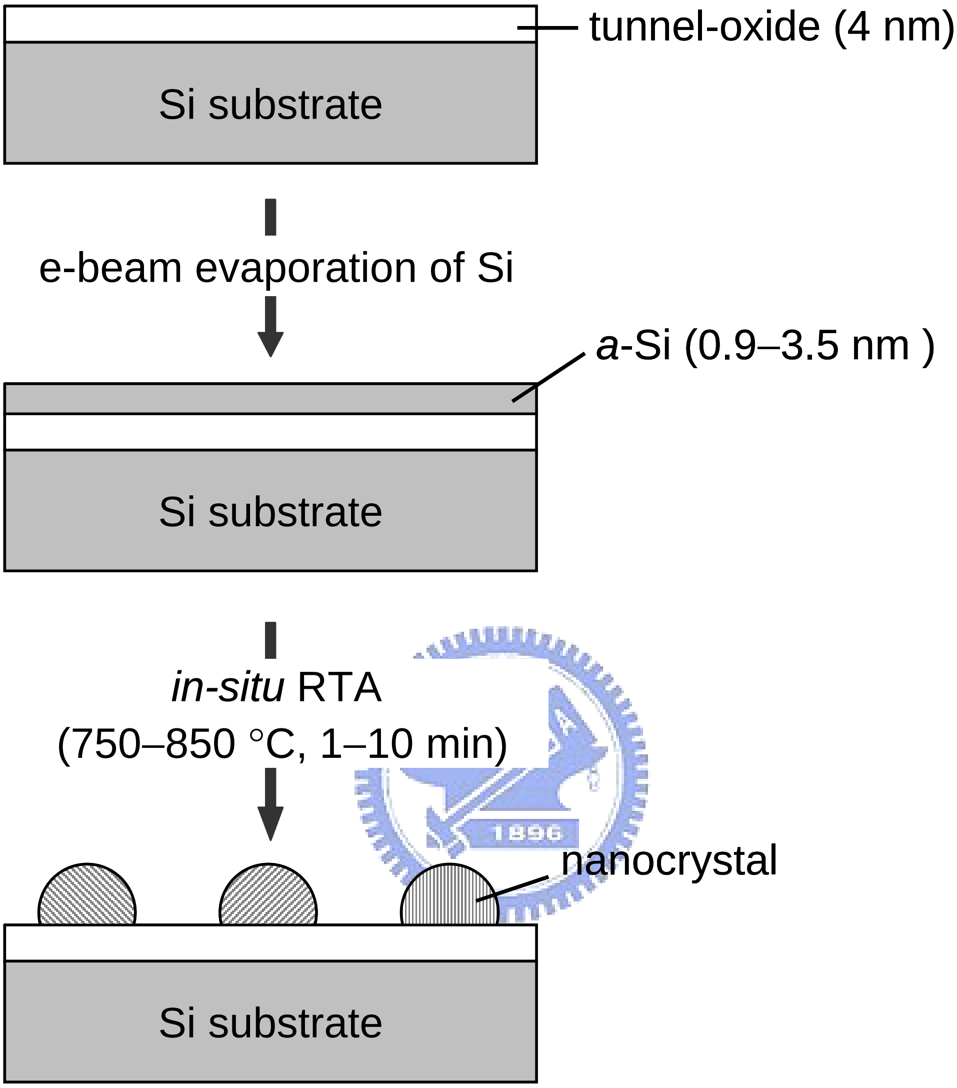


Fig. 5.1 Illustration of the thermally-induced Si agglomeration; an ultrathin *a*-Si layer was deposited by electron-beam evaporation under vacuum and then annealed *in situ* to form silicon nanocrystals. The duration of the *in-situ* rapid thermal annealing was 1–10 min. With the annealing temperature at 750 °C or higher, evidence of Si-dot agglomeration could be observed.

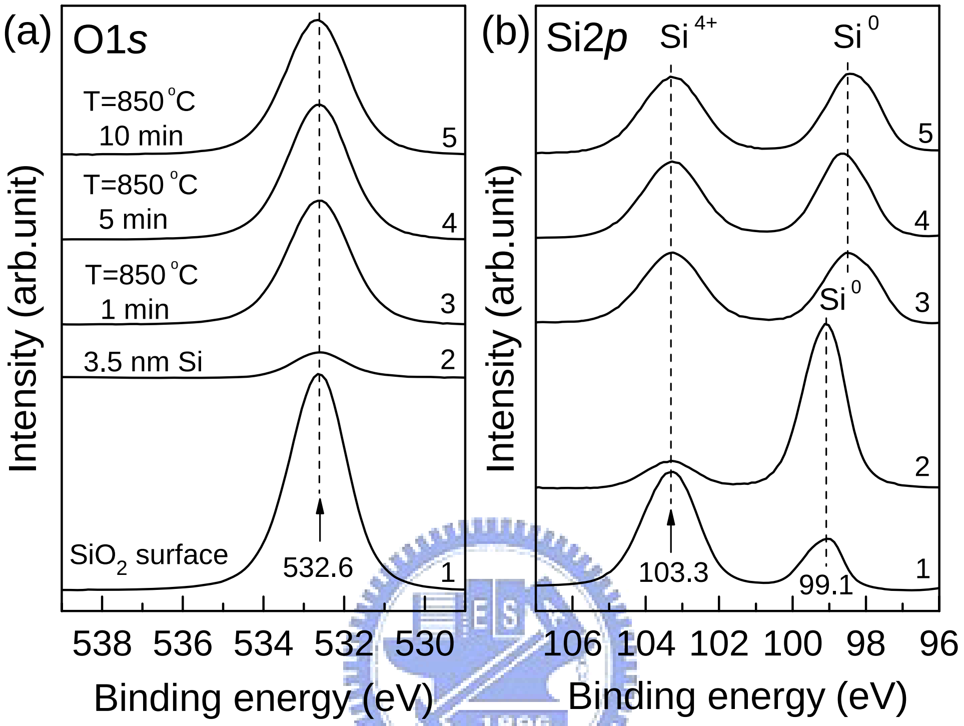


Fig. 5.2 (a) O 1*s* and (b) Si 2*p* XPS core-level spectra acquired before (1) and after (2) the 3.5-nm *a*-Si deposition and during the subsequent *in-situ* annealing (3–5).

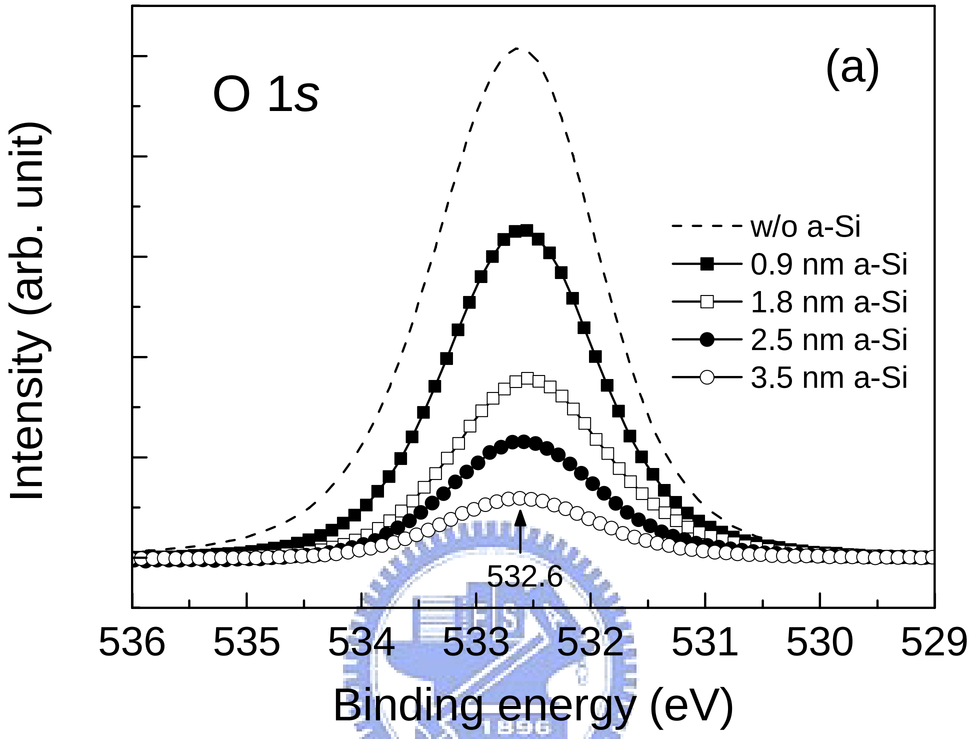


Fig. 5.3 (a) Evolution of the XPS O 1*s* spectra recorded *in situ* during the *a*-Si deposition. All peaks were referenced to the Si^{4+} 2*p* (Si-O) peak at binding energy of E_B = 103.3 eV. (b) O 1*s* peak intensity attenuation versus the deposited *a*-Si thickness. The intensities (peak areas) were taken from Fig. 5.2a, and normalized to the initial O 1*s* spectrum recorded before the *a*-Si deposition. (c) Cross-sectional TEM micrograph of the *a*-Si/tunnel-oxide/Si(100) structure.

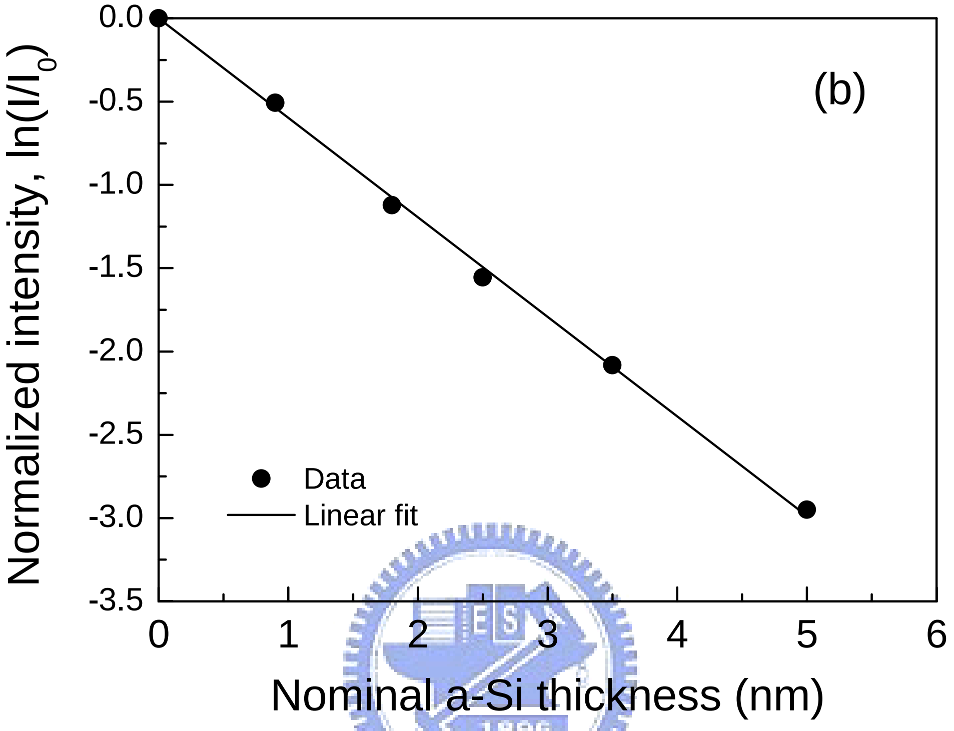


Fig. 5.3 (b) O 1*s* peak intensity attenuation versus the deposited *a*-Si thickness. The intensities (peak areas) were taken from Fig. 5.2a, and normalized to the initial O 1*s* spectrum recorded before the *a*-Si deposition.

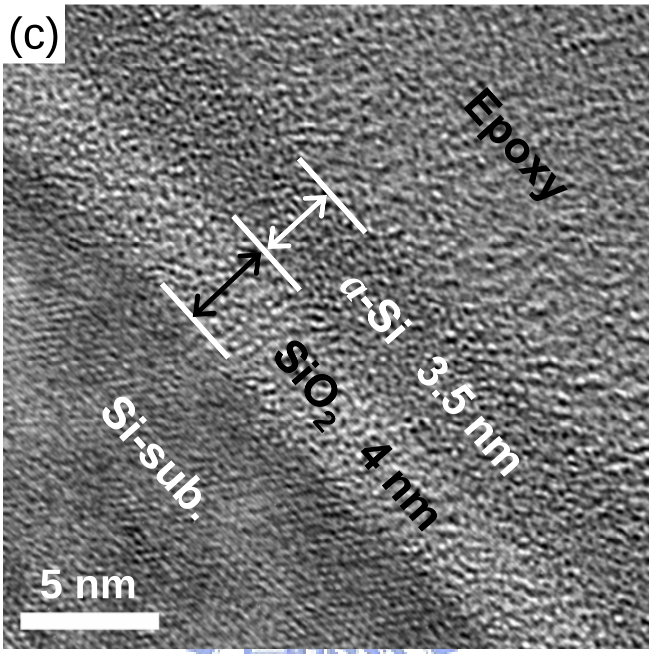


Fig. 5.3 (c) Cross-sectional TEM micrograph of the *a*-Si/tunnel-oxide/Si(100) structure.

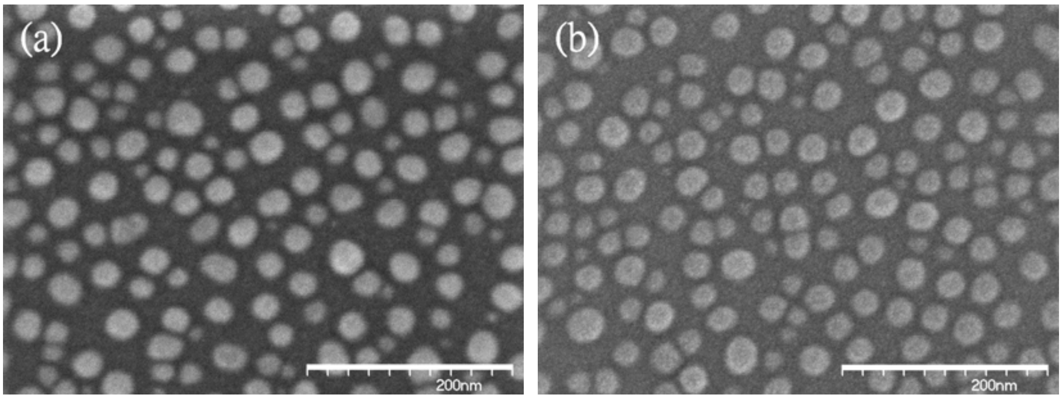


Fig. 5.4 SEM micrographs of Si-dots agglomerated from a 3.5-nm-thick *a*-Si layer after *in-situ* annealing at 850 °C for (a) 1 and (b) 10 min. The scale bar is 200 nm.

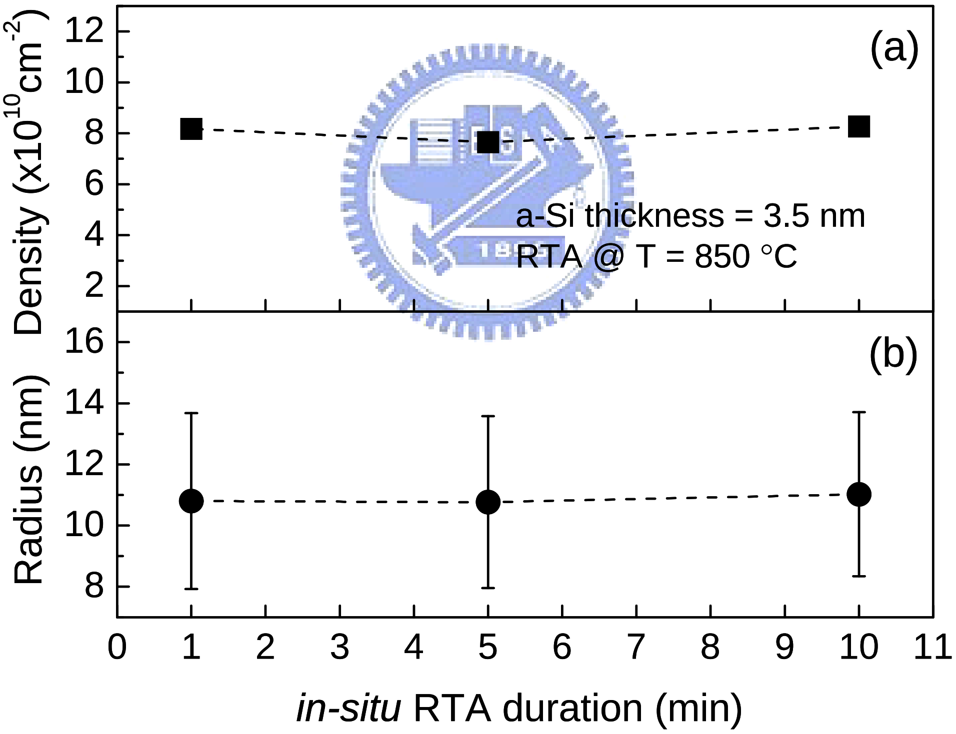


Fig. 5.5 (a) Densities and (b) base radii of Si-dots agglomerated from a 3.5-nm-thick *a*-Si layer after *in-situ* annealing at 850 °C for different periods. The data are obtained by analyzing SEM images using a digitalized program. The error bars in (b) indicate one standard deviation. The lines are drawn to guide the eyes.

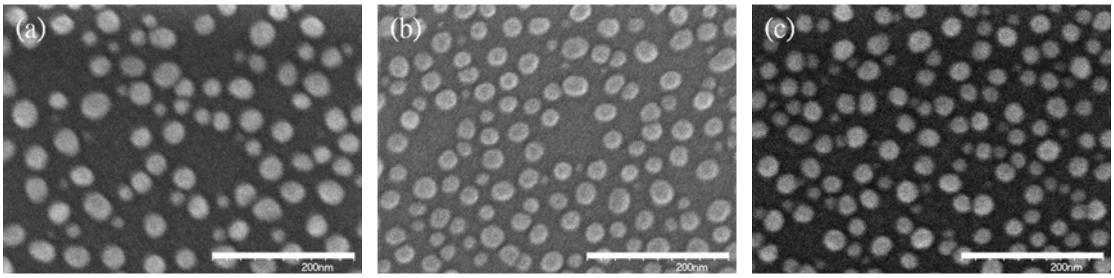


Fig. 5.6 SEM images of Si-dot agglomeration in a 3.5-nm *a*-Si layer after *in-situ* RTA at (a) 750 °C, (b) 800 °C, and (c) 850 °C for 5 min. The scale bars indicate 200 nm.

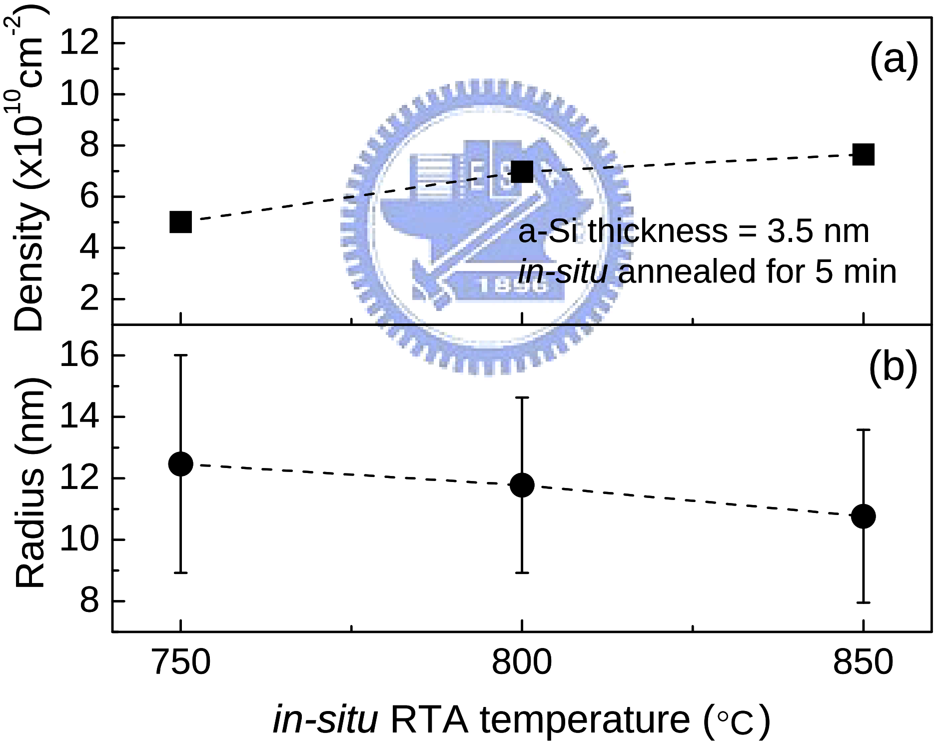


Fig. 5.7 (a) Densities and (b) base radii of Si-dots agglomerated in a 3.5-nm *a*-Si layer after *in-situ* RTA at 750, 800, and 850 °C for 5 min. The data are obtained by analyzing SEM images using a digitalized program. The error bars in (b) indicate one standard deviation. The lines are drawn to guide the eyes.

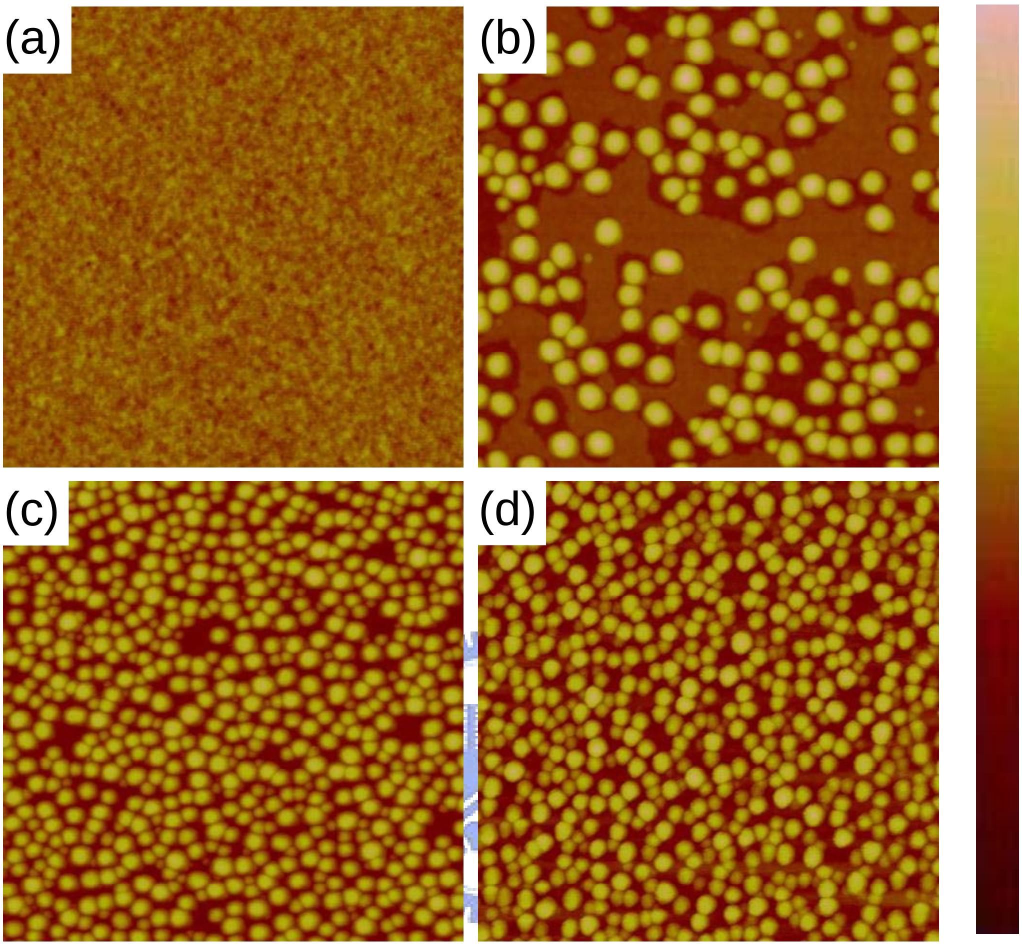


Fig. 5.8 AFM images of samples annealed at (a) 700, (b) 750, (c) 800, and (d) 850 °C for 5 min. A 3.5-nm-thick *a*-Si layer was deposited prior to the *in-situ* RTA. The sizes of all AFM images are 1 μm by 1 μm. The color scale indicates a full range of 5 nm for (a) and a full range of 40 nm for others. The rms roughness results for the annealed samples are (a) 0.181, (b) 5.286, (c) 4.759, and (d) 5.038 nm.

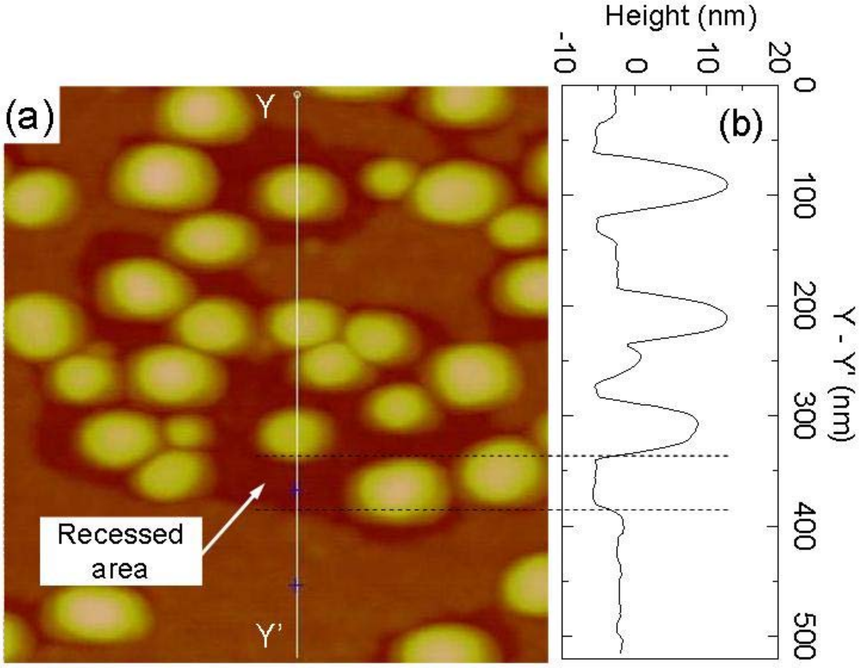


Fig. 5.9 (a) An magnified portion of Fig. 5.8b and (b) the AFM profile along the Y–Y' cross-section. Recessed areas are observed near the agglomerated Si-dots.

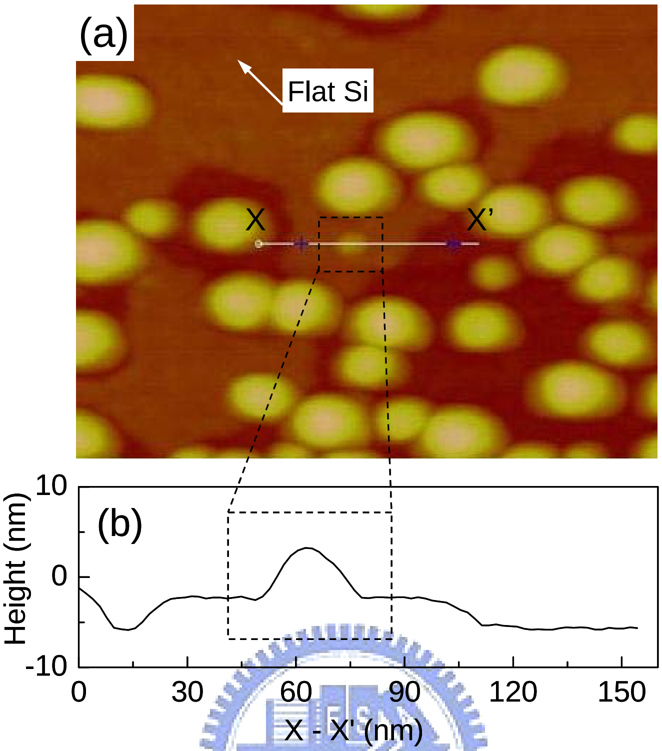


Fig. 5.10 (a) An magnified portion of Fig. 5.8b and (b) the AFM profile along the X–X’ cross-section. The silicon coalescence and the beginning of agglomeration caused the dot formation on a flat silicon surface.

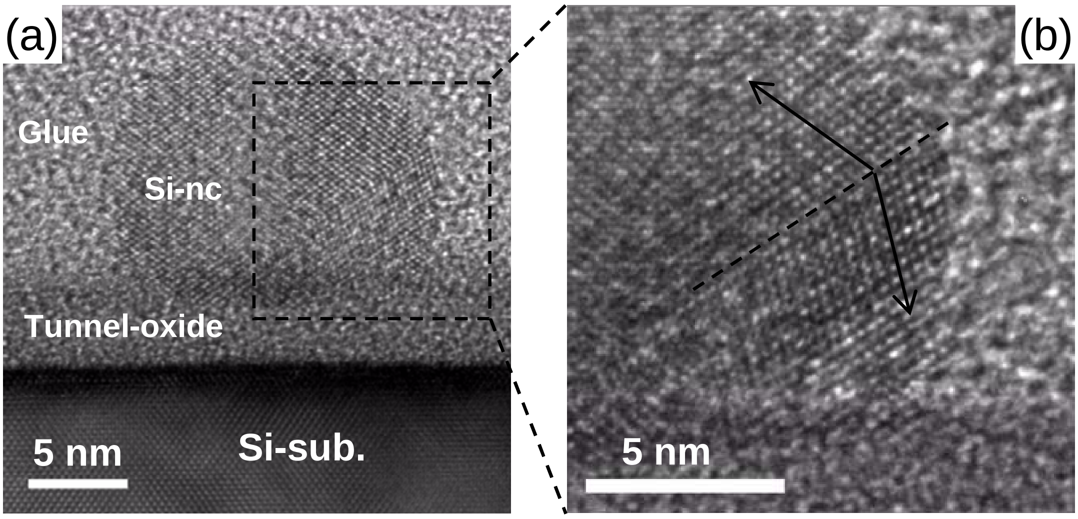


Fig. 5.11 (a) Cross-sectional TEM micrograph of the sample in Fig. 5.8b. (b) Magnified image shows a twin boundary (indicated by a dash line) in the Si nanocrystal.

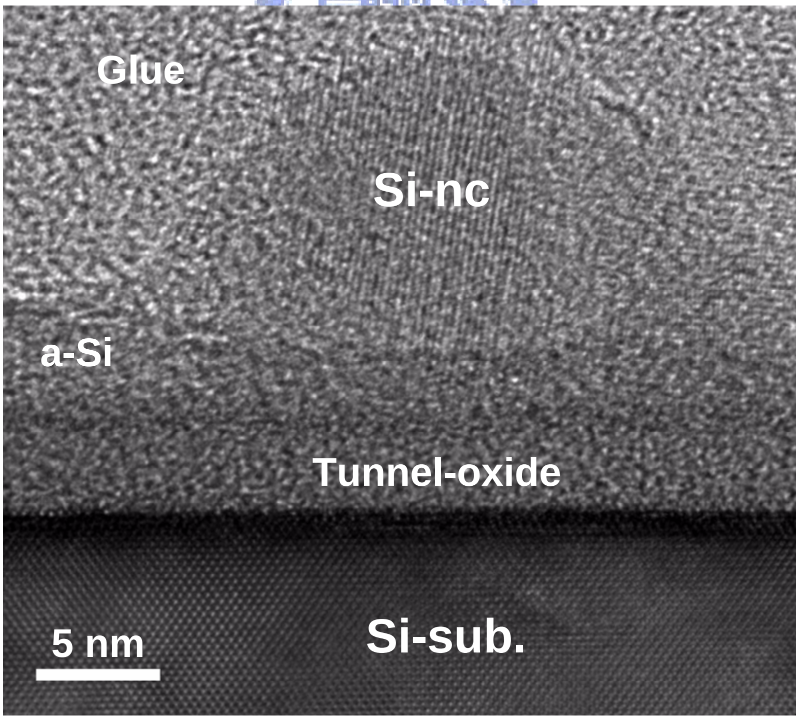


Fig. 5.12 Cross-sectional TEM micrograph of the sample in Fig. 5.8b; a nanocrystal partially-agglomerated on the remaining *a*-Si layer is clearly revealed.

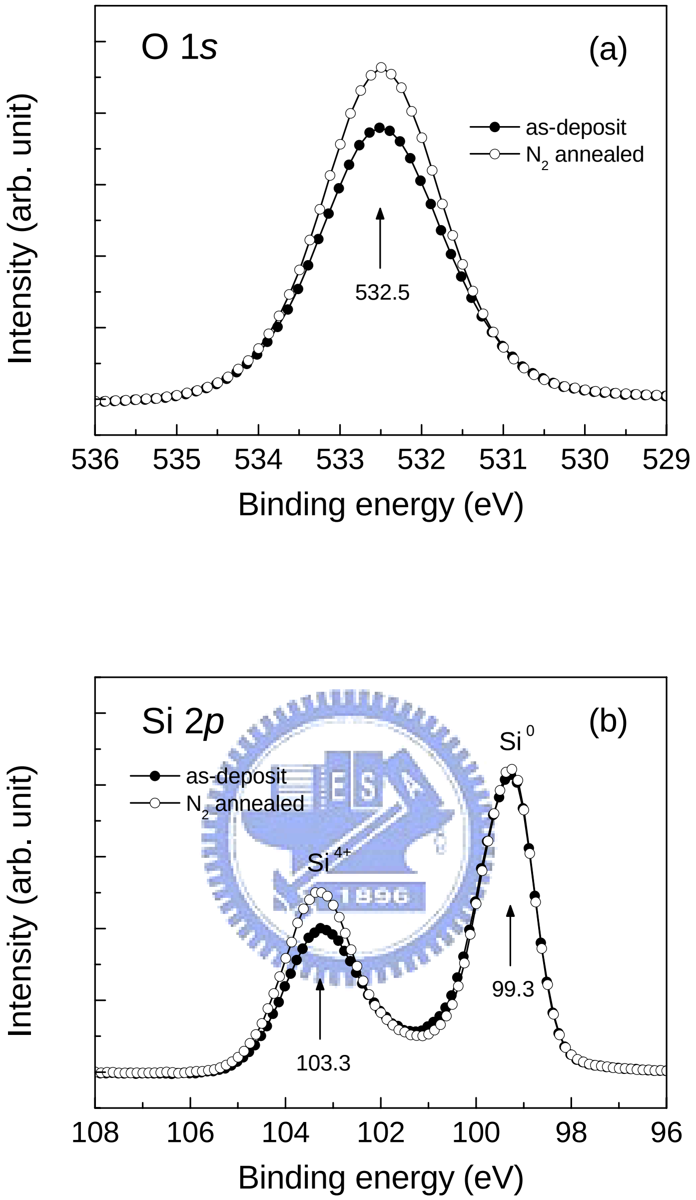


Fig. 5.13 (a) O 1*s* and (b) Si 2*p* core-level spectra measured by *ex-situ* XPS with the as-deposited (●) and nitrogen annealed (○) *a*-Si samples. An ultrathin *a*-Si (3.5 nm) film was deposited on the tunnel-oxide/Si(100) substrate and then annealed *ex situ* at 850 °C for 5 min in N_2 ambient. All peaks are referenced to the Si^0 2*p* (Si substrate) peak at binding energy of E_B = 99.3 eV.

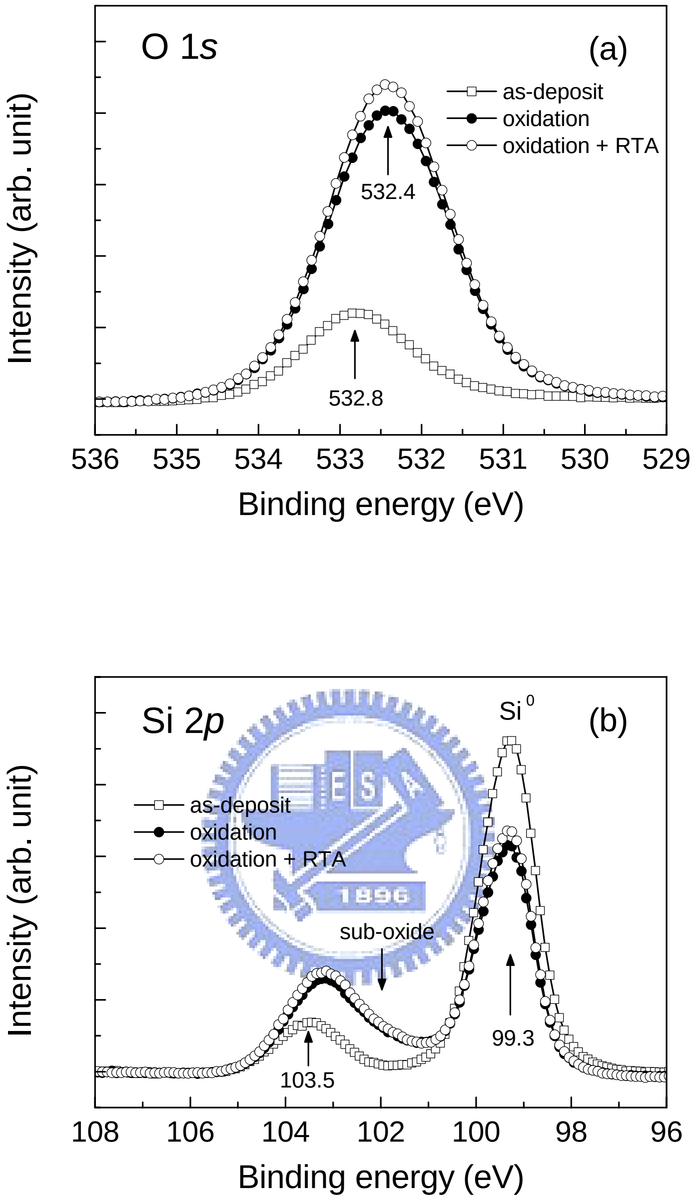


Fig. 5.14 (a) O 1*s* and (b) Si 2*p* core-level spectra measured by *in-situ* XPS with the as-deposited (□), *in-situ* oxidized (●), and then *in-situ* annealed (○) sample. A 3.5-nm *a*-Si layer was deposited on the tunnel-oxide/Si(100) substrate followed with a low-pressure (12 milli-Torr) oxidation step at 650 °C for 20 min, and then annealed under UHV at 850 °C for 5 min. All peaks are referenced to the Si^0 2*p* (Si substrate) peak at binding energy of $E_B = 99.3$ eV.

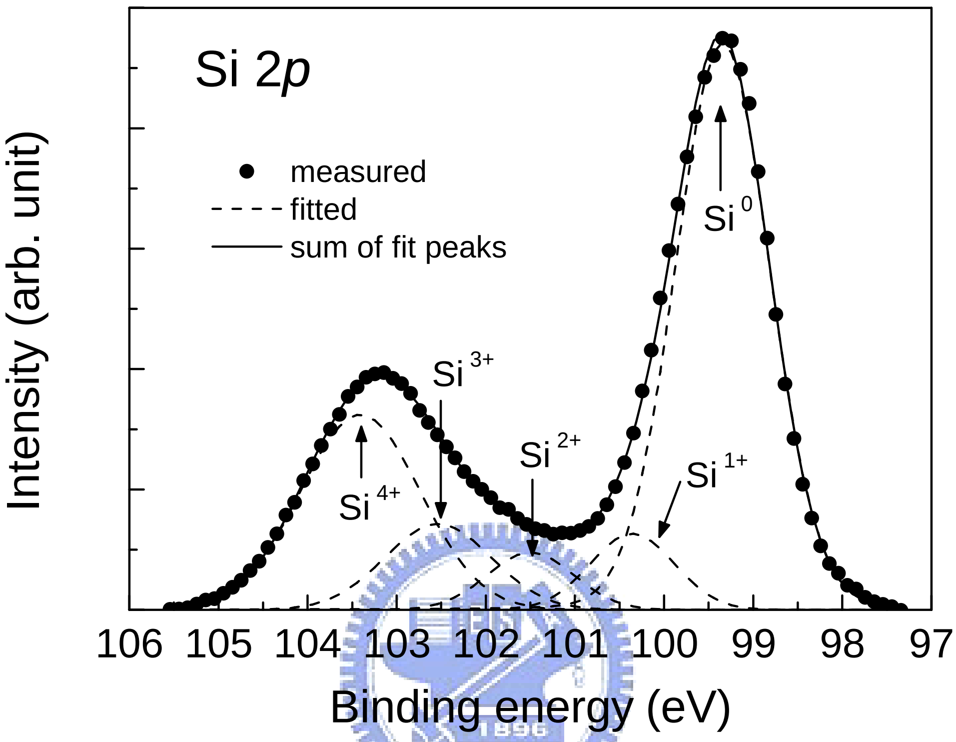
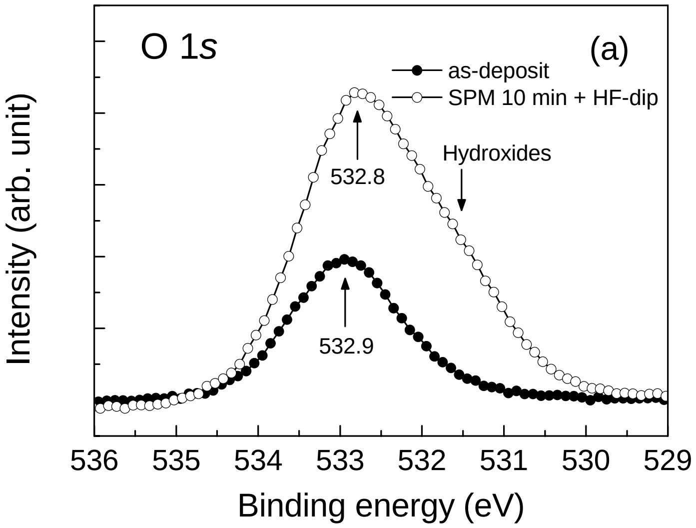


Fig. 5.15 XPS Si 2*p* spectrum for the oxidized sample in Fig. 5.14b: (solid circle) measured, (dash lines) fitted peaks, (solid line) sum of fitted peaks. A 3.5-nm *a*-Si layer was deposited on tunnel-oxide/Si(100) and then oxidized *in situ* at 650 °C for 20 min under a low-pressure (12 milli-Torr) O_2 ambient prior to the *in-situ* XPS measurement.



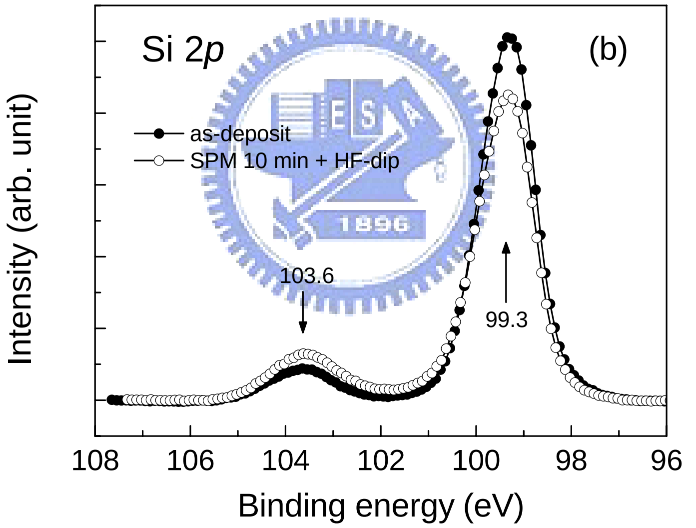


Fig. 5.16 (a) O 1*s* and (b) Si 2*p* spectra measured by *in-situ* XPS after a 5-nm *a*-Si layer was deposited (●) and then treated with SPM and a dilute-HF dip (○). The *a*-Si film was deposited on a tunnel-oxide/Si(100) substrate and then immersed into a sulfuric acid hydrogen peroxide mixture (SPM: 3 parts H_2SO_4 + 1 part H_2O_2) for 10 min prior to a 2-min dilute-HF dip. All peaks are referenced to the Si^0 2*p* (Si substrate) peak at binding energy of $E_B = 99.3$ eV.

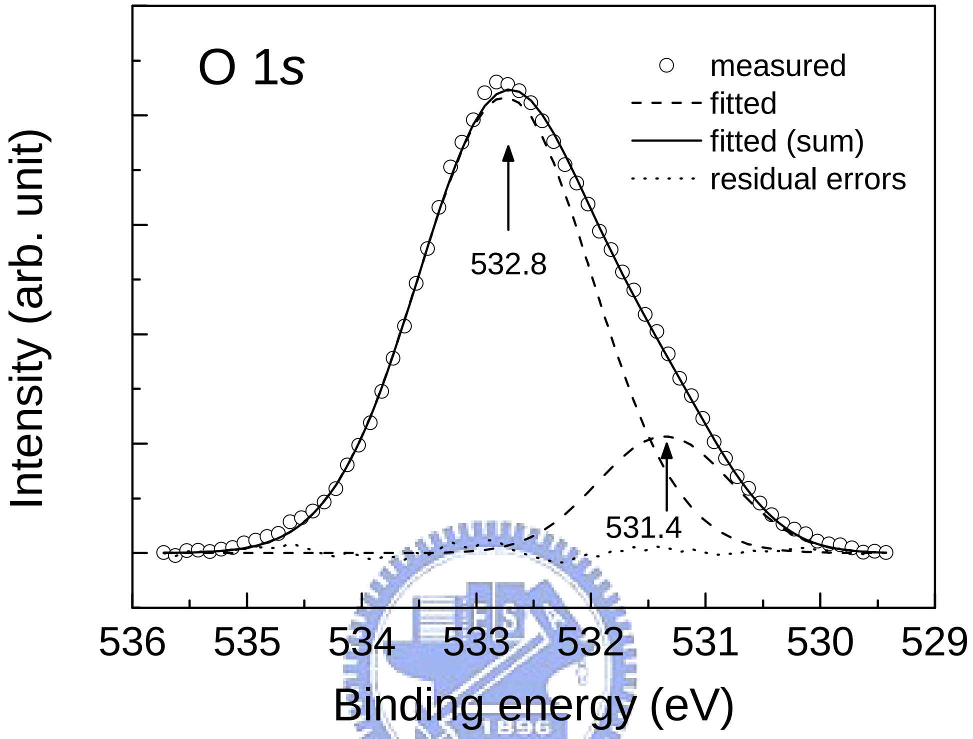


Fig. 5.17 O 1*s* spectrum for the SPM and HF treated sample shown in Fig. 5.16a: (blank circle) measured, (dash lines) fitted peaks, (solid line) sum of fitted peaks, (dot line) residual errors between measured and fitted data. A 5-nm *a*-Si film was deposited on a tunnel-oxide/Si(100) substrate and then treated in a sulfuric acid hydrogen peroxide mixture (SPM: 3 parts H_2SO_4 + 1 part H_2O_2) for 10 min. A 2-min dilute-HF dip was performed to remove the surface oxide prior to XPS measurement.

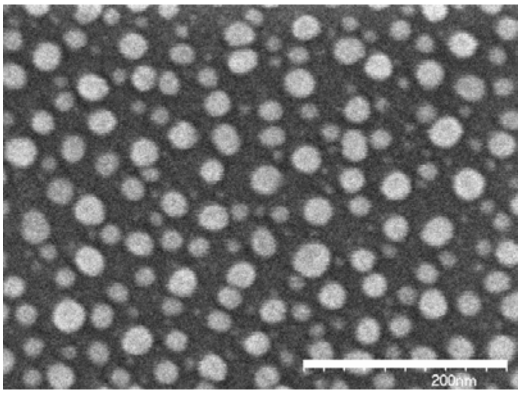


Fig. 5.18 SEM micrograph of Si agglomeration after an amorphous Si layer (initially 5-nm-thick) was treated with an SPM immersion step, a dilute-HF dip, and then an *in-situ* annealing at 850 °C for 5 min.

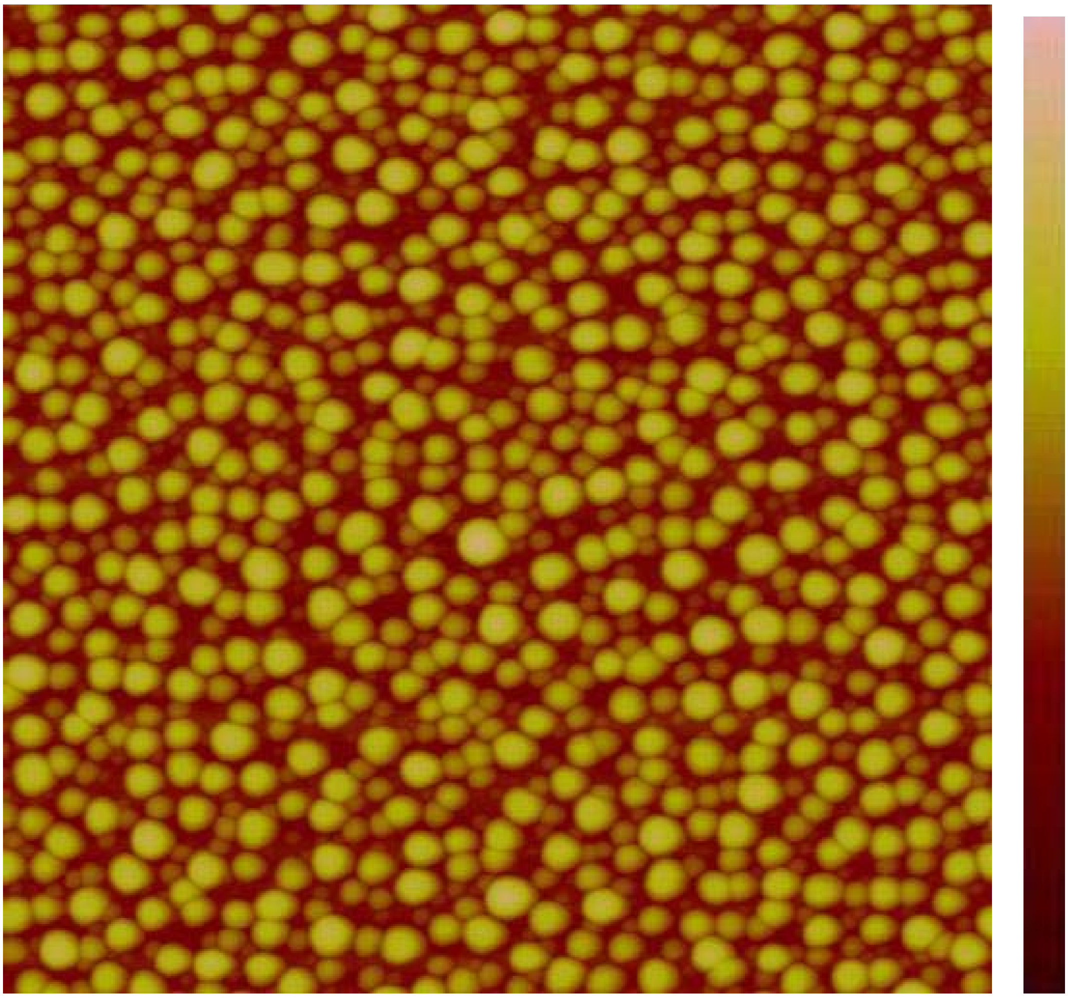


Fig. 5.19 AFM image of Si agglomeration after an amorphous Si layer (initially 5-nm-thick) was treated with an SPM immersion step, a dilute-HF dip, and then an *in-situ* annealing at 850 °C for 5 min.

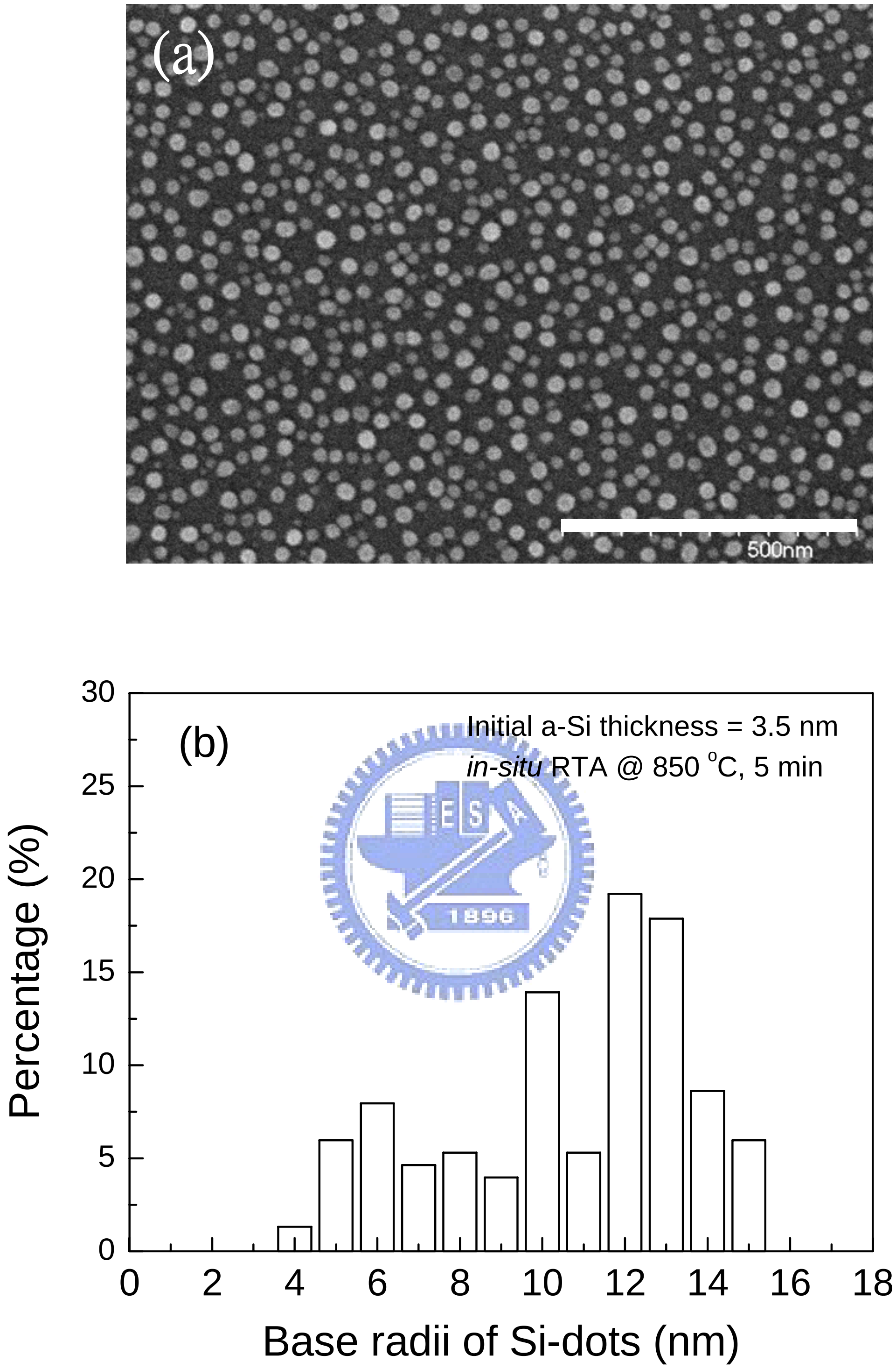


Fig. 5.20 (a) SEM image and (b) dot-size distribution of Si nanocrystals agglomerated after *in-situ* rapid thermal annealing of a 3.5-nm-thick *a*-Si layer at 850 °C for 5 min. The scale bar in the SEM image indicates 500 nm in length.

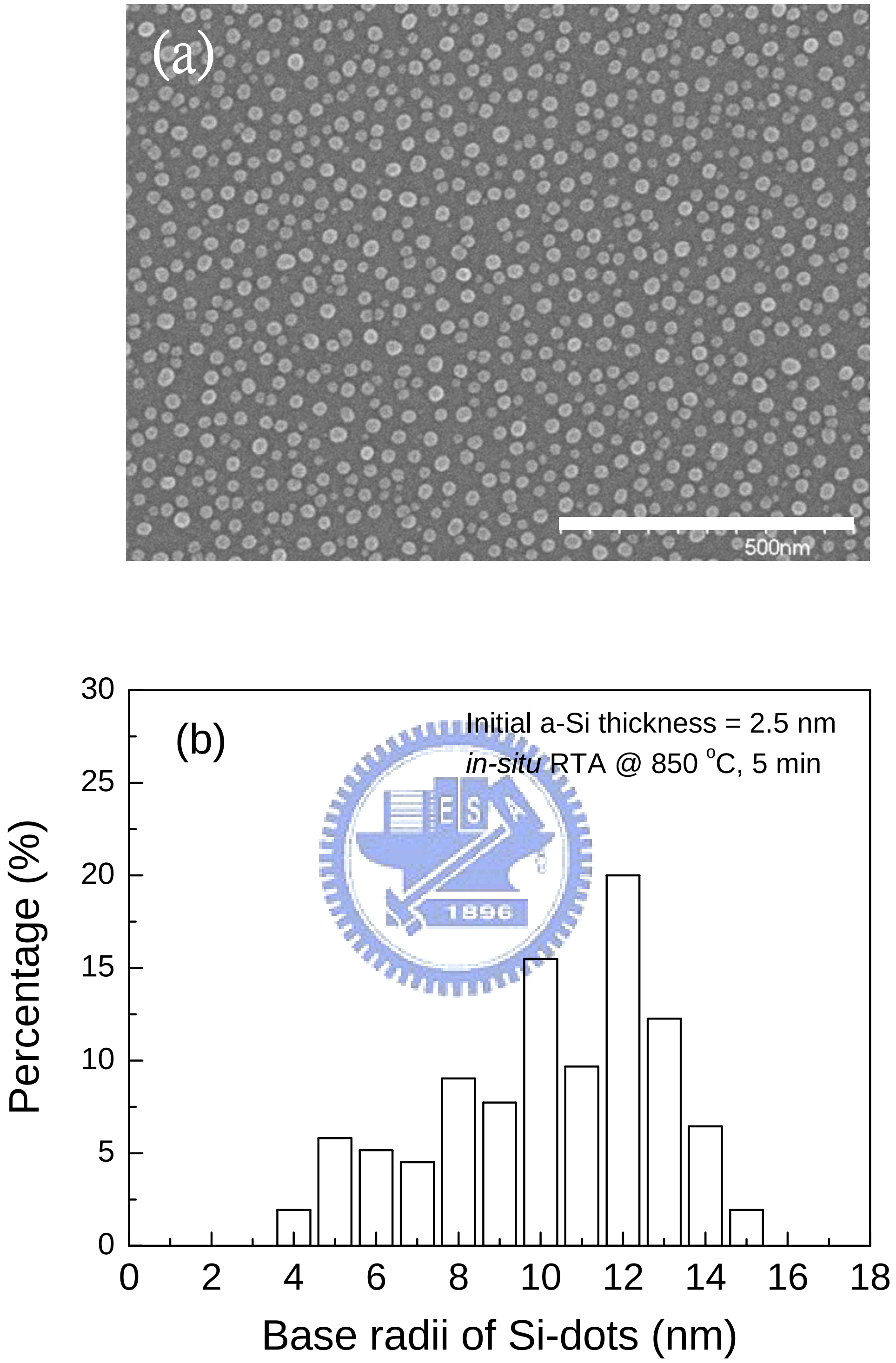


Fig. 5.21 (a) SEM image and (b) dot-size distribution of Si nanocrystals agglomerated after *in-situ* rapid thermal annealing of a 2.5-nm-thick *a*-Si layer at 850 °C for 5 min. The scale bar in the SEM image indicates 500 nm in length.

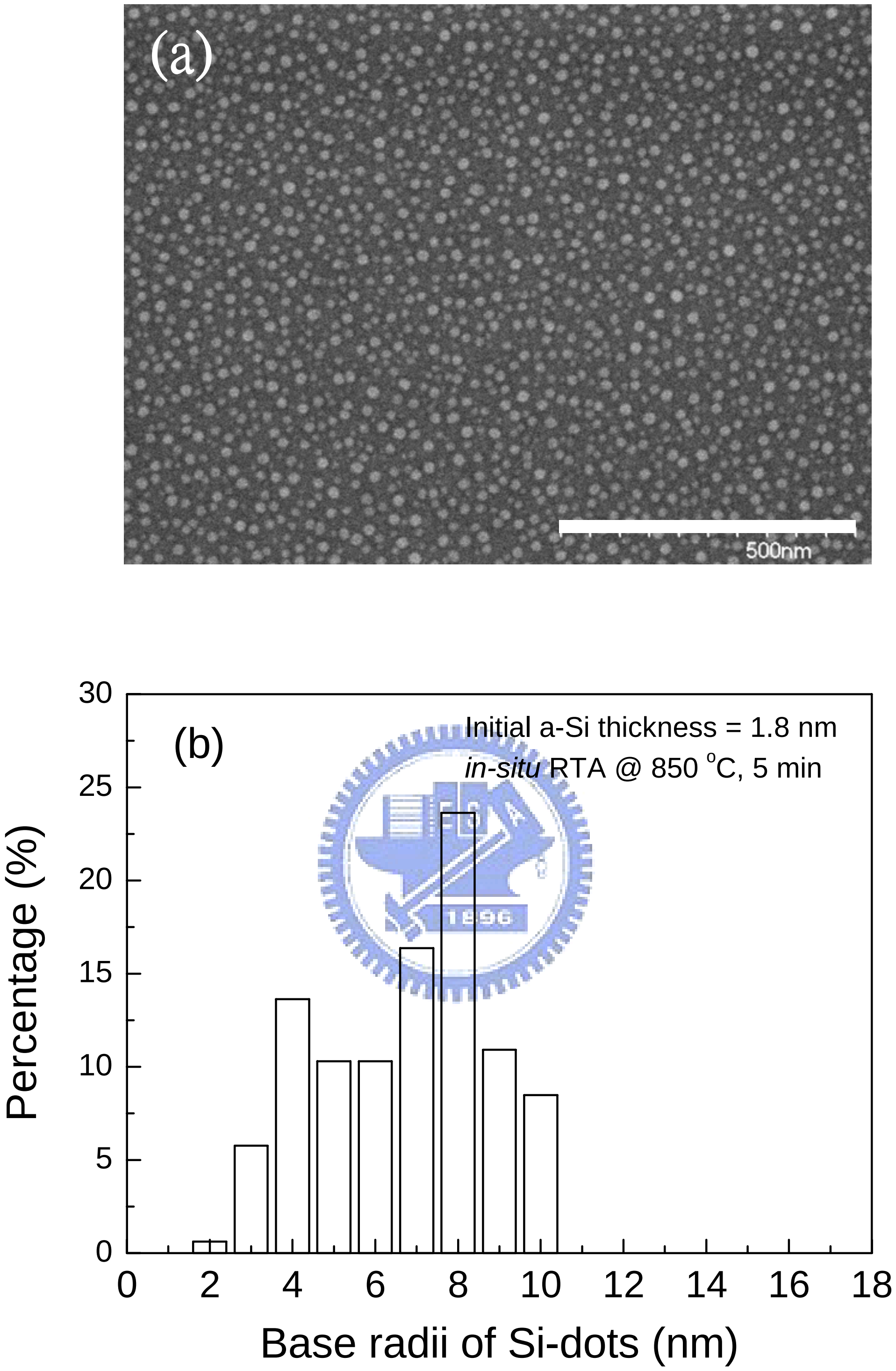


Fig. 5.22 (a) SEM image and (b) dot-size distribution of Si nanocrystals agglomerated after *in-situ* rapid thermal annealing of a 1.8-nm-thick *a*-Si layer at 850 °C for 5 min. The scale bar in the SEM image indicates 500 nm in length.

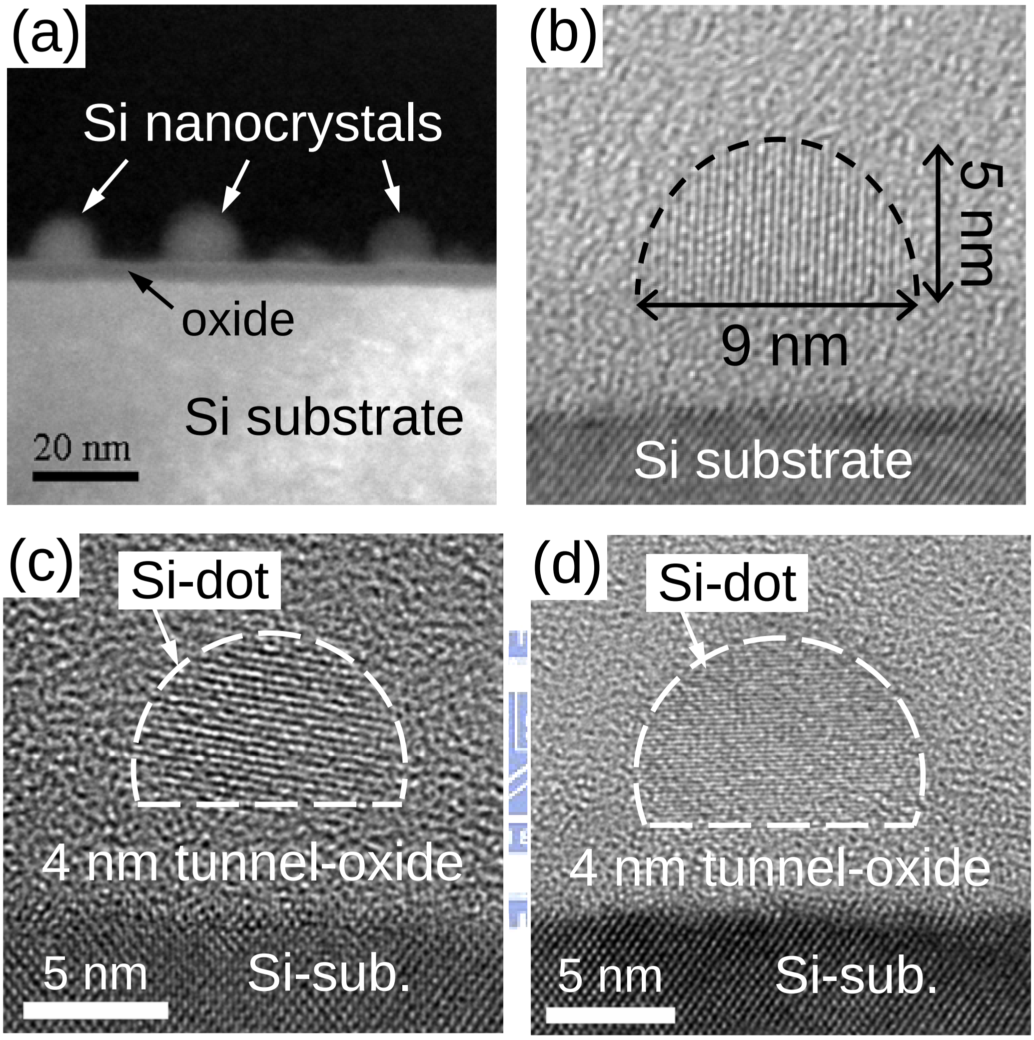


Fig. 5.23 (a) ADF-STEM image of hemispherical Si nanocrystals on a thin oxide layer; (b), (c), and (d) HRTEM micrographs. The Si-nanocrystals were obtained by *in-situ* annealing of a 1.8-nm *a*-Si thin layer at 850 °C for 5 min.

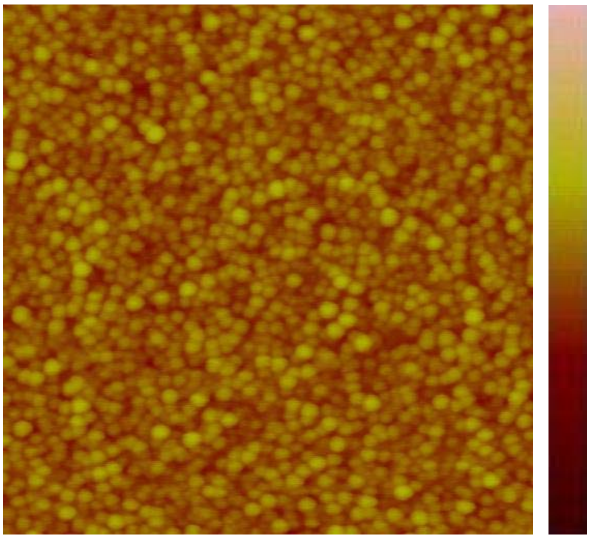


Fig. 5.24 AFM image of the Si-dot agglomeration after *in-situ* annealing of an ultrathin (0.9 nm) *a*-Si layer at 850 °C for 5 min. The AFM scan area is 500 nm by 500 nm, and the root-mean-square roughness is measured 0.549 nm. The color scale indicates a full range of 10 nm.

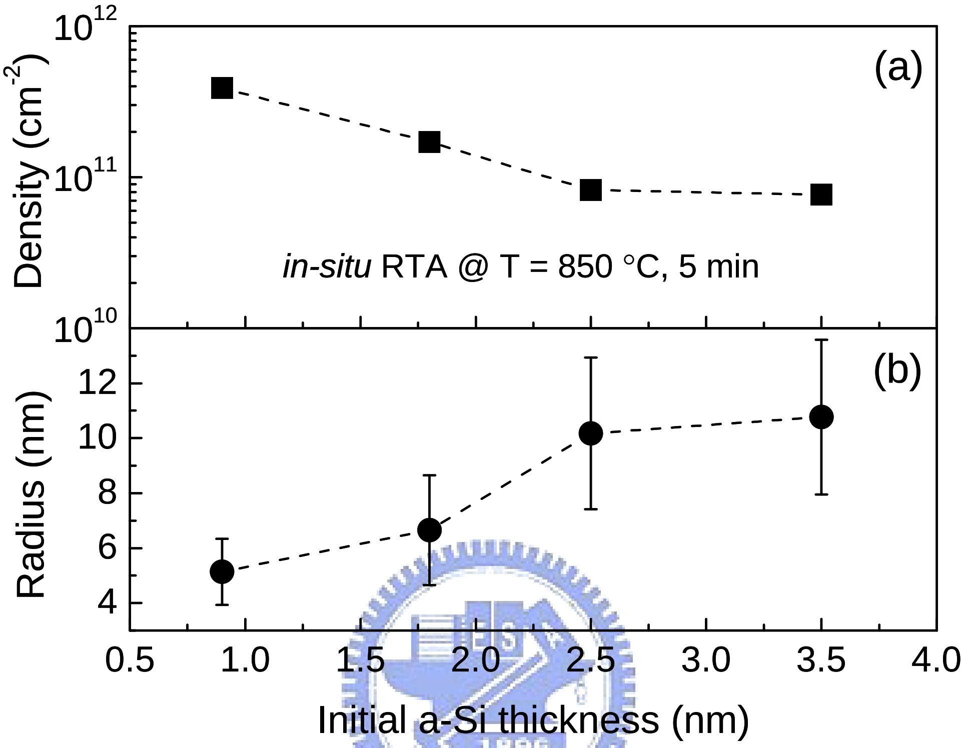


Fig. 5.25 (a) Densities and (b) base radii of Si dots as a function of the initial *a*-Si thickness; the nanocrystal dots were thermally agglomerated after *in-situ* annealing of ultrathin *a*-Si layers at 850 °C for 5 min. The data were obtained by analyzing SEM or AFM images using a digitalized program. The error bars in (b) indicate one standard deviation. The lines are drawn to guide the eyes.

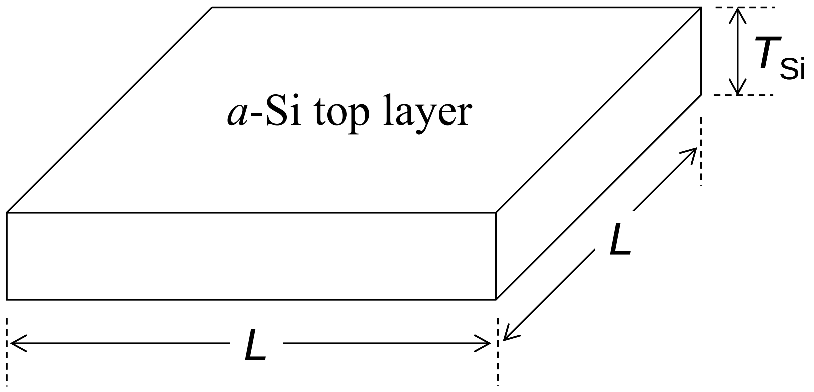


Fig. 5.26 Schematic showing a square unit area of the *a*-Si film; the length and width of the unit area are both *L*. The initial thickness of the *a*-Si layer is T_{Si}.

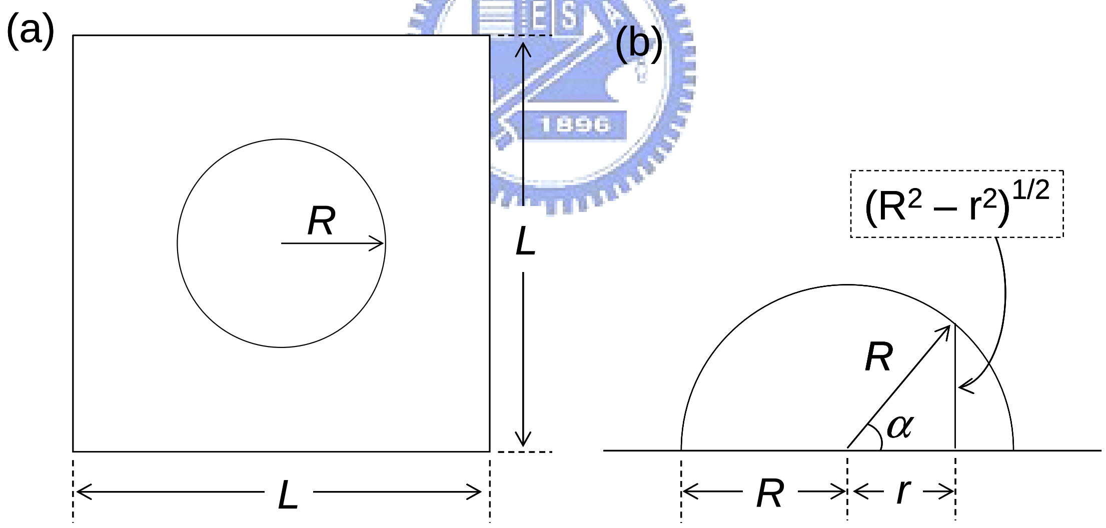


Fig. 5.27 (a) Top-view and (b) cross-sectional schematics of a hemispherical Si-dot on the tunnel-oxide surface; the dot radius is *R*, and the dot formation occurs in a square unit area sized L^2.

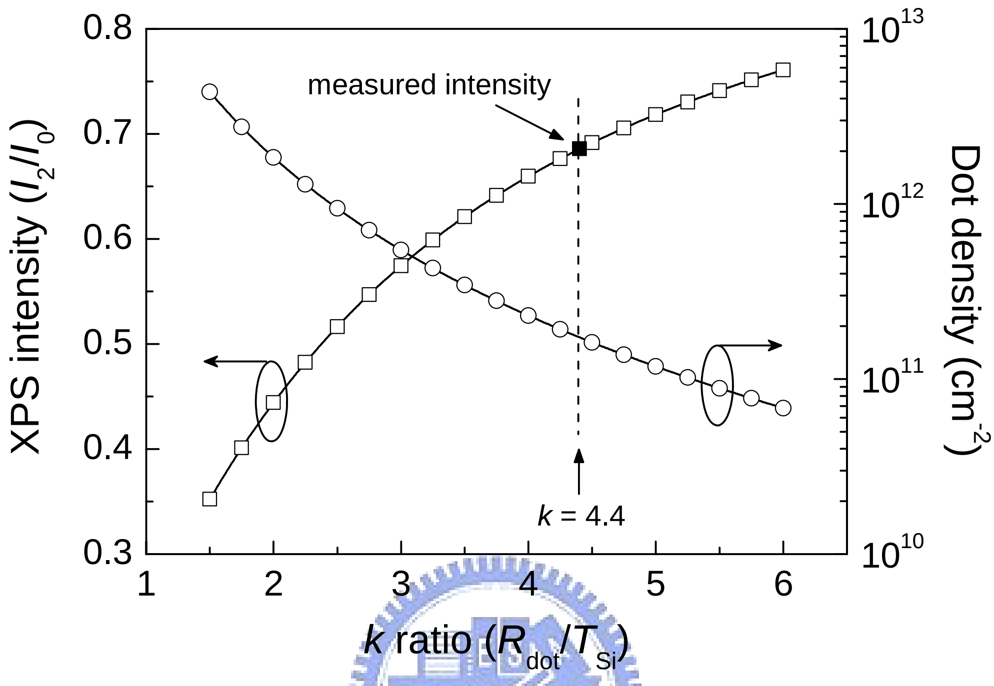


Fig. 5.28 Normalized XPS peak intensity (□) and dot density (○), both calculated based on a simple attenuation model, as a function of the *k* ratio; the *k* ratio is defined as the dot radius divided by the initial Si thickness. The normalized intensity measured by *in-situ* XPS (■) is also indicated. Experimental XPS data were obtained during the deposition of a 1.8-nm *a*-Si thin film and the subsequent *in-situ* annealing at 850 °C for 5 min.

Chapter 6

Electrical Characteristics of Nonvolatile Memory Devices with Embedded Hemispherical Si Nanocrystals

6.1 Introduction

In recent years, nanocrystal-based memory devices have drawn great attention due to their scaling advantages over the conventional polycrystalline-silicon-based floating-gate (FG) nonvolatile memory (NVM) devices [96]. The conventional NVM device, with charges stored in a single FG layer, is prone to failure of the FG isolation. One charge leakage path created in the tunnel oxide can discharge the entire FG and cause a fatal data loss. Therefore it is critical to maintain the tunnel-oxide robustness, which casts difficulties in scaling the tunnel-oxide thickness. The nanocrystal memory device, however, has many discrete nanocrystal dots as distributed storage nodes. A local leaky path can only affect a few storage nodes (dots) near it, which prevents a serious charge loss. Therefore, nanocrystal floating-gate memories can alleviate the tunnel-oxide scaling issues and as a result, enhance the program and erase speeds with thin tunnel-oxide layers [10].

Among nanocrystal-embedded devices, silicon nanocrystal (Si-nc) memories [10, 97, 128] have attracted much attention because of the material compatibility with current complementary metal-oxide-semiconductor (CMOS) technologies. Various techniques have been developed to produce Si nanocrystals, including the chemical vapor deposition (CVD) techniques [62, 98, 101, 116], the oxidation of a Si thin film [102], the thermal precipitation in Si-rich SiO_x [103, 105] or Si-implanted SiO_2 layers [106, 108, 110], and an aerosol deposition technique [112].

The CVD method has been widely used to fabricate Si-nc memory devices. However, the bottom-up method results into a random distribution of nanocrystals on the surface and introduces challenges in the device fabrication. One of the challenges is the gate-stack etching for the removal of nanocrystals from the source/drain regions without causing any silicon recess (micro-trenches) in the source/drain [97]. Other Si-nc techniques also face processing issues. For example, the thermal oxidation of a thin Si film can produce Si nanocrystals in a SiO_2 matrix [102], although the control of oxidation time is essential for both separating the Si dots and maintaining an adequate charge-trap density. The oxidation step also introduces challenges to the tunnel-oxide thickness control. The thermally-induced Si precipitations in substoichiometric SiO_x [105] or Si-implanted SiO_2 [108] films can also produce Si quantum dots, but a high temperature annealing ($\geq$1000 °C) is normally required. The annealing, sometimes with a prolonged period, can significantly increase the process thermal budget.

In this chapter, Si-nc nonvolatile memory devices are fabricated using a thermal agglomeration technique. The surface coalescence of amorphous Si (*a*-Si) during an ultra-high vacuum (UHV) annealing was first observed by Sakai *et al* [23]. Since then the resulted hemispherical grained Si (HSG) structure has been widely adopted in the dynamic random-access-memory (DRAM) manufacturing [130]. When a thin *a*-Si or silicon-on-insulator (SOI) film was annealed in vacuum, Si-island formation was reported [42, 45]. Although theoretical studies have provided insights of the agglomeration mechanism [42, 48], the electrical characterizations of such agglomerated Si dots are still lacking.

In present study, ultrathin *a*-Si films are deposited using electron-beam evaporation and then annealed *in situ* under UHV. Hemispherical Si nanocrystals are obtained through the thermal agglomeration process. The nanocrystals are formed on a thin tunnel-oxide layer and then covered by a control-oxide (blocking-oxide) layer. Memory devices including metal-oxide-semiconductor (MOS) capacitors and field effect transistors (MOSFETs) are fabricated with the embedded Si-nc floating gates. Their electrical characteristics are investigated. This thermal agglomeration method is considered compatible with the conventional top-down process because the ultrathin *a*-Si film can be patterned prior to the vacuum annealing. In between the *ex-situ* processing and the vacuum annealing, however, the *a*-Si surfaces need to be cleaned and kept free of native oxide in order to ensure the Si agglomeration.

6.2 Experimental

6.2.1 Si-Nanocrystal Embedded MOS Capacitors

4-inch, p-type Si(100) wafers with a resistivity of 5–10 Ω-cm were used as substrates. At first, a 4.0±0.1 nm tunnel-oxide layer was prepared on the Si wafer by thermal oxidation followed with a dilute-HF etch-back. After rinsed by de-ionized water and N_2 blown dry, the wafer was put into an ultrahigh vacuum system which comprises an electron beam evaporation chamber and a rapid thermal annealing (RTA) setup. The wafer was heated *in situ* to remove absorbed water and hydrocarbon contaminations, and then deposited with a 0.9–3.5 nm thin *a*-Si layer at room temperature by electron-beam evaporation. The silicon deposition rate was about 0.01 nm per second. Subsequently an *in-situ* RTA was performed at 850 °C for 5 minutes under a pressure $<4\times10^{-8}$ Torr. Si nanocrystals were formed on the tunnel-oxide surface after RTA. Details of the sample preparation procedure and the thermal agglomeration process can be found in the previous chapter.

The wafer was then taken out of the vacuum chamber. Some samples went through an *ex-situ* oxidation step at 700–900 °C for 60 s in O_2 ambient using a commercial rapid thermal processor (AG Associates Heatpulse 410). After that, a 17-nm-thick control-oxide layer was deposited by plasma-enhanced CVD (PECVD) using SiH_4 and N_2O precursors. The control-oxide was deposited at a substrate temperature of 390 °C, with a process pressure of 2 Torr and incident RF power of 19 W. The fabrication of capacitors was completed with aluminum gate/substrate electrodes deposited by using a thermal coater. Figure 6.1 shows a schematic of the MOS capacitor structure. A control sample, which had the tunnel-oxide and control-oxide layers but no Si nanocrystals, was also fabricated. Capacitance-voltage (C-V) curves were measured at 1 MHz with either an HP 4275A LCR meter or an Agilent 4284A LCR meter.

6.2.2 Si-Nanocrystal Embedded MOSFETs

N-channel MOSFETs (n-MOSFETs) embedded with Si-nc floating gates were fabricated. A p-type Si(100) wafer with a resistivity of 5–10 Ωcm was used as the substrate. A gate-last process was used for the device fabrication. At first, a thick field-isolation oxide was grown using thermal wet oxidation. The device source/drain areas were defined by photolithography and etching, and then source/drain junctions were formed by phosphorus ion implantation at energy of 35 keV and a dose of 5×10^{15} cm^{-2}. A dopant-activation annealing was followed using a nitrogen-purged quartz furnace. The annealing was done at 950 °C for 30 min. The remaining field-oxide on the gate regions was removed by photolithography and etching, and thus the device active areas were defined. The wafer was then shipped to another institute for the following steps.

After a standard RCA cleaning procedure with the patterned wafer, a 4-nm tunnel-oxide layer was grown by rapid-thermal oxidation (RTO) at 850 °C in O_2 using a commercial processor (AG Associates Heatpulse 410). The wafer was then loaded into an UHV system. A 1.5-nm thin *a*-Si layer was deposited and then annealed *in situ* at 850 °C for 5 min. Si-nc dots were formed as a result of thermally-induced Si agglomeration. On top of the Si-nc floating gates a 17-nm-thick control-oxide layer was deposited by PECVD using SiH_4 and N_2O gases. Finally, aluminum metal was deposited using a thermal coater and patterned for the gate and contact electrodes. Figure 6.2 shows a schematic of the nanocrystal-embedded memory device. It should be noted that a polycrystalline-silicon-gate process with self-aligned source/drain is also applicable for the Si-nc memory fabrication. The memory devices were characterized using a Keithley 4200 semiconductor characterization system and an Agilent 81110A pulse generator, both through a Keithley 708A switching matrix. Devices having a gate length of 10 μm and a width of 100 μm were tested.

6.3 Results and Discussion

6.3.1 Si-Nanocrystal Embedded MOS Capacitors

Figure 6.3 shows *C*-*V* measurements of different bias-sweep ranges for a MOS capacitor embedded with Si nanocrystals. The nanocrystal dots are formed by the *in-situ* RTA of a 3.5-nm *a*-Si film at 850 °C for 5 min. The bias delay time is 1 s at each gate bias step during the *C*-*V* sweeps. The amount of *C*-*V* hysteresis increases with larger gate-bias sweeps, demonstrating the charge storage in the Si nanocrystal floating gates. The capacitance measured at the accumulation regime for the MOS capacitor represents an equivalent oxide thickness (EOT) of 18 nm, which is smaller than the sum of the tunnel-oxide thickness (4 nm) and the control-oxide thickness (17 nm), both measured by spectroscopic Ellipsometry. It is possible that the Si nanocrystals have caused changes in the control-oxide surface morphology. The control-oxide surface may resemble the underlying Si-dots/tunnel-oxide morphology. Therefore, a larger effective surface-area than the nominal gate size is possible for the MOS capacitor, and therefore a larger capacitance and a smaller equivalent oxide thickness are obtained by the *C*-*V* measurement.

Figure 6.4 shows *C*-*V* curves of MOS diodes embedded with Si nanocrystals that have been oxidized in an *ex-situ* RTO step. After nanocrystals were agglomerated on the tunnel-oxide layer, the sample was oxidized in O_2 ambient at 700, 800, and 900 °C for 1 s. The control-oxide layer was then deposited on top of sample. The oxidation of Si nanocrystals can create oxide shells around the dots and reduce the Si volumes in dots [129]. The oxidation can also add thickness to the thin tunnel-oxide layer. Both effects can reduce the charge injection from the substrate into the Si nanocrystals. In Fig. 6.4 smaller *C*-*V* hysteresis can be found with the sample oxidized at higher temperature. It is believed that RTO at higher temperature has consumed more volume of the nanocrystals and thus prohibited more charges to be stored in the nanocrystals. The tunnel-oxide re-growth during RTO is also possible, as the accumulation capacitance values presented in Fig. 6.4 suggest that there is an approximately 1 nm EOT increase between the 900 and 700 °C oxidized samples. In Fig. 6.4(c) a noticeable *C*-*V* hysteresis window is found even when the sweeping bias voltages (±5 V) are too small for the Fouler-Nordheim (FN) tunneling to occur. It is speculated that trap states at the tunnel-oxide/Si-substrate interface may contribute to nanocrystal charging/discharging through the trap-assisted tunneling of electrons under low electric fields.

Figure 6.5 presents *C*-*V* curves of MOS capacitors with and without Si nanocrystals. The gate bias is swept from 10 to -10 and back to 10 V, with a 0.1 V step voltage and a step bias delay of 1 s. The control sample, which has the tunnel-oxide and control-oxide layers but no Si nanocrystals, shows a small hysteresis of 40 mV. The flatband voltage (V_{fb}) of the control sample is near -2 V. It is speculated that the PECVD control-oxide layer has a certain amount of fixed oxide charges which attribute to the negative V_{fb} of the control sample. The oxide charges are primarily due to the structural defects in the oxide layer and are positively charged, which introduce a negative V_{fb} shift to the ideal *C-V* model [131]. Oxide layers deposited by PECVD using SiH_4 and N_2O have been reported to exhibit a negative V_{fb} shift in the *C-V* measurements [126]. Similar V_{fb} shifts toward the negative direction were also observed with a nanocrystal-embedded MOS diode in which a control-oxide layer was deposited by PECVD using SiH_4 and N_2O [101]. The PECVD method is used in present study simply because of the facility availability. It should be stressed, however, that the control sample shows negligible *C-V* hysteresis in this work, which indicates that the memory effects observed in the nanocrystal-embedded MOS capacitors are not caused by the charge trapping or de-trapping in the oxides.

In Fig. 6.5, large flat-band voltage shifts (ΔV_{fb} >2.7 V) are observed for the nanocrystal-embedded MOS capacitors, suggesting the memory effects of nanocrystal charging and discharging. V_{fb} shifts toward the negative direction are found larger than the positive V_{fb} shifts, indicating a larger amount of hole-charging than electron-charging during the bidirectional *C-V* sweeps. It is speculated that donor-type traps at and near Si nanocrystals have contributed to the V_{fb} shift by holes [132]. A larger negative V_{fb} shift is found when the nanocrystals are agglomerated from a thinner *a*-Si layer, i.e., when the nanocrystal density is higher. This indicates more hole-charging with the denser Si nanocrystals. The stored charge densities (electron + hole) are extracted from the ΔV_{fb} data [10] and summarized in Table 6.1. A charge density of 4.1×10^{12} cm^{-2} has been achieved with the Si-nanocrystal density of

3.9×10^{11} cm^{-2}. It is worth noting that while the stored charge density increases with the higher Si-dot density, the average charges per nanocrystal decrease due to the reduced nanocrystal mean size.

6.3.2 Si-Nanocrystal Embedded MOSFETs

In present work, uniform Fouler-Nordheim (FN) tunneling is used to program and erase memory devices, although programming with channel hot-electron injection is also possible. Figures 6.6(a) and 6.6(b) present the program/erase (P/E) transient characteristics of Si-nc memory devices. Gate voltages of ±8, ±10, ±12, and ±15 V are pulsed while the source/drain/body grounded. Before the test of a certain P/E voltage, the device is initialized by applying a voltage of the same level but opposite polarity for 1 s. Then the P/E pulses are applied, with the device V_t recorded as a function of the pulse width. The threshold voltage (V_t) shift is strongly dependent on the pulse-voltage level and duration. A V_t window of ~0.5 V can be obtained in milliseconds under ±10 V P/E operations. A higher P/E pulse voltage results in faster P/E time and a larger memory window. When P/E voltages of ±15 V are applied, a large memory window (>2.7 V) can be achieved.

Figure 6.7(a) shows the cycling endurance of a Si-nc memory operating at room temperature. A relatively low P/E voltage of ±10 V is used here to reduce the possible oxide damage under high-field stressing, with a slower P/E speed as the tradeoff. A memory window of 0.9 V is created by programming at +10 V for 0.02 s and erasing at -10 V for 0.1 s. After 10000 P/E cycles, the threshold voltages of programmed and erased states drift up by approximately 0.2 V. This observation can be attributed to charge trapping in the control oxide. Due to the partial area coverage of the nanocrystal layer, some electrons injected from the substrate may not be captured by the Si-nc dots but trapped in the control-oxide layer [97]. The gradually positive drift of the V_t window is indicative of the electron buildup in the oxide layer during P/E cycling. However, this charge buildup can be removed by applying a larger erase voltage or using a longer erase time.

Data retention characteristics are evaluated after the endurance test, as shown in Fig. 6.7(b). The V_t is monitored at different periods of time for both programmed and erased states. After 10000 P/E cycles, the V_t window of 0.9 V is substantially maintained. During the charge retention, however, the memory window starts to decrease with logarithmic time dependence after 10 s and reduces to 0.53 V after 10000 s. It is believed that electrons are stored in the deep traps at the nanocrystals and tunneling back into the interface states at the tunnel-oxide/Si-substrate during the charge retention process [132, 133]. One should note that the tunnel-oxide growth conditions used in present study were not optimized for the best interface quality. Further gate dielectric stack optimization is necessary to improve the nonvolatile behavior of the Si-nc memory.

Figure 6.8 shows the retention characteristics of a Si-nanocrystal memory device. A gate voltage of ±15 V and a pulse width of 1 s are used in this test. Initially a memory window (V_t shift) of 2.8 V is observed between the programmed and erased states, as indicated in the inset transfer characteristics. The V_t values then start to decay toward the original V_t (-0.2 V) of a fresh sample, and a memory window of 1 V has remained after 100 hours. The logarithmic time dependence in the charge-loss process can be explained by the direct tunneling of the stored charges to the trap states at the SiO_2/Si-substrate interface [132]. Furthermore, a faster hole-loss rate is observed, suggesting that more hole-traps are located at the Si-dot/oxide interfaces and prone to fast de-trapping through the trap-assisted tunneling. It is believed that the data retention can be further improved by optimizing the oxidation process and reducing the interface-state densities.

Figure 6.9 shows the temperature dependence of the charge retention characteristics. Large P/E voltages (+15/-15 V) are used here and the memory window is increased accordingly. At room temperature the charge-loss behavior is same as that observed in Fig. 6.8. When the device is operated at 85 °C, the programmed V_t is found smaller than that obtained at room temperature. This can be explained by the reduced electron-trapping possibilities at the Si nanocrystals due to the increased electron thermal energy at elevated temperature. The retention characteristics show only little dependence on the temperature, with a slightly increased hole-detrapping rate at 85 °C for the erased state. This suggests that the charge-loss behaviors of present samples are mainly determined by charges tunneling from the Si-nc trap centers to the interface states at the SiO_2/Si-substrate, which is less temperature dependent.

Figure 6.10 shows that, when a less-negative erasing voltage is used, a smaller initial V_t shift is obtained, but a similar memory window can be maintained after 10000 s retention (compared with those in Figure 6.9). At the erased status, holes are possibly retained in the Si-nanocrystal/tunnel-oxide interface states or in some oxide traps created by the high-field stressing. The fast hole-loss rate makes it difficult to utilize the storage of holes for the nonvolatile memory applications. In present study, the device should be operated in a voltage window where only the electron storage is taken into consideration. Figure 6.11 shows the data retention when a device is programmed at 15 V for 1 s and erased at -12 V for 0.1 s. The memory window of 1 V is sustained after approximately 100 hours. The long-term data retention is comparable with that shown in Fig. 6.8.

It has been reported that interface charges exist within the silicon forbidden band due to the interruption of the periodic lattice structure at the crystal surface [131].

Therefore the interface traps at the nanocrystal surfaces can also contribute to the charging/discharging behaviors of the memory devices. In present work, the significant hole-injection observed in *C-V* measurements suggests a large number of hole-traps. Furthermore, the retention test reveals a faster hole-loss rate than the electron-loss rate, which suggests that more hole-traps are located at the Si-dot/oxide interfaces and prone to fast de-trapping through trap-assisted tunneling into the tunnel-oxide/Si-substrate interface-states. The hole-traps are possibly produced by trivalent silicon atoms [95] at the nanocrystal surfaces. The charge retention characteristics have shown little temperature dependence (Figures 6.9 and 6.10), indicating that the thermally-activated de-trapping of electrons (holes) from shallow states to the nanocrystal conduction (valence) band is not the dominant charge-loss process with present samples [132].

It is also worthwhile to add some notes about the shapes of Si nanocrystals here. Thean and Leburton [125] have made numerical simulations in search for the quantum confinement levels of silicon dots with different shapes. Three dot shapes were investigated in their report, including spherical, truncated-sphere, and hemispherical nanocrystal dots. Their study showed that a higher gate bias was needed to inject a certain number of electrons into the less spherical dots, because the truncated-sphere and hemispherically shaped dots induced greater confinement within them. When the strain was taken into considerations, lower-energy states in hemispherical dots were found insensitive to the strain. The simulation results provided useful insights of the single-electron charging behaviors in a Si nanocrystal dot. However, the study by Thean and Leburton only considered the electrons charging into the conduction band or more precisely, into the quantum-mechanically confined energy states. In a more practical case, the silicon defects and surface states within the band gap can still come in play. It has been proposed that the electron storage in deep traps inside the band gap must be considered to explain the long retention time observed with nanocrystal memory devices [134]. Studies by Campera and Iannaccone [135] have also proposed that the interface quality between silicon dots and the surrounding oxide is more relevant than the dot size and shapes in determining the program and erase behavior. Therefore it remains arguable that how and how much the device characteristics would be affected by the nanocrystal geometry.

6.4 Summary

In summary, the fabrication of a Si nanocrystal-embedded nonvolatile memory has been demonstrated using a thermal agglomeration technique. Hemispherical nanocrystal dots are self-assembled after annealing an ultrathin (0.9–3.5 nm) *a*-Si film in vacuum at 850 °C for 5 min, with their size and density controlled by the *a*-Si thickness. A dot density as high as 3.9×10^{11} cm^{-2} is obtained on the oxide surface, which achieves a stored charge density of 4.1×10^{12} cm^{-2} (electron + hole).

Floating-gate n-MOSFETs are fabricated with Si nanocrystals embedded between a 4-nm tunnel-oxide layer and a 17-nm control-oxide layer. Uniform FN tunneling is used to program and erase the Si nanocrystal floating gates. A V_t window of 0.9 V is achieved under P/E voltages of ±10 V for 0.02/0.1 s. The memory device also shows good endurance and charge retention behaviors after 10000 P/E cycles. Increasing P/E voltages to ±15 V creates a large memory window (>2.7 V) with the proposed memory device. After a retention test for 100 hours, a memory window of 1 V is maintained, exhibiting promising potential for nonvolatile memory applications. The retention characteristics have shown little temperature dependence with present samples, indicating that the charge-loss process is determined by the direct tunneling of stored charges into the tunnel-oxide/Si-substrate interface states. The nonvolatile memory characteristics of hemispherical Si nanocrystals are demonstrated using an agglomeration technique. The top-down process compatibility and self-assembly features of this technique show its potential for the nanocrystal memory applications.

We believe this thermal agglomeration technique will be suitable for the memory device manufacturing. The vacuum annealing of *a*-Si has been widely adopted by the dynamic-random-access-memory (DRAM) industry for producing the hemispherical grained-silicon (HSG) structure [130]. The concepts of clustered tools are also widely accepted and used in the semiconductor manufacturing. Considering the integration of metal-gate/high-κ materials for the advanced devices, *in-situ* processing techniques are currently gaining more attention. With all the facts mentioned above, the proposed thermal agglomeration technique has shown great potential for the advanced memory applications.

Table 6.1 Flat-band voltage shifts and stored charge densities extracted from *C*-*V* results in Fig. 6.5; the densities and base radii of Si nanocrystals are also listed.

Initial *a*-Si thickness $T_{a\text{-Si}}$ (nm)	2.5	1.8	0.9
Flat-band voltage shift ΔV_{fb} (V)	2.73	3.34	3.58
Stored charge density (cm^{-2})	2.9×10^{12}	3.8×10^{12}	4.1×10^{12}
Nanocrystal density (cm^{-2})	8.2×10^{10}	1.7×10^{11}	3.9×10^{11}
Mean base radius (nm)	10.2	6.6	5.1

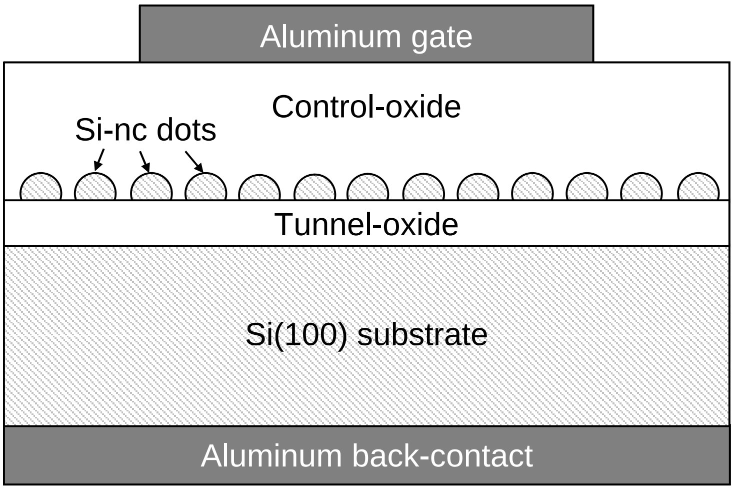


Fig. 6.1 Schematic of a MOS capacitor with embedded Si nanocrystals.

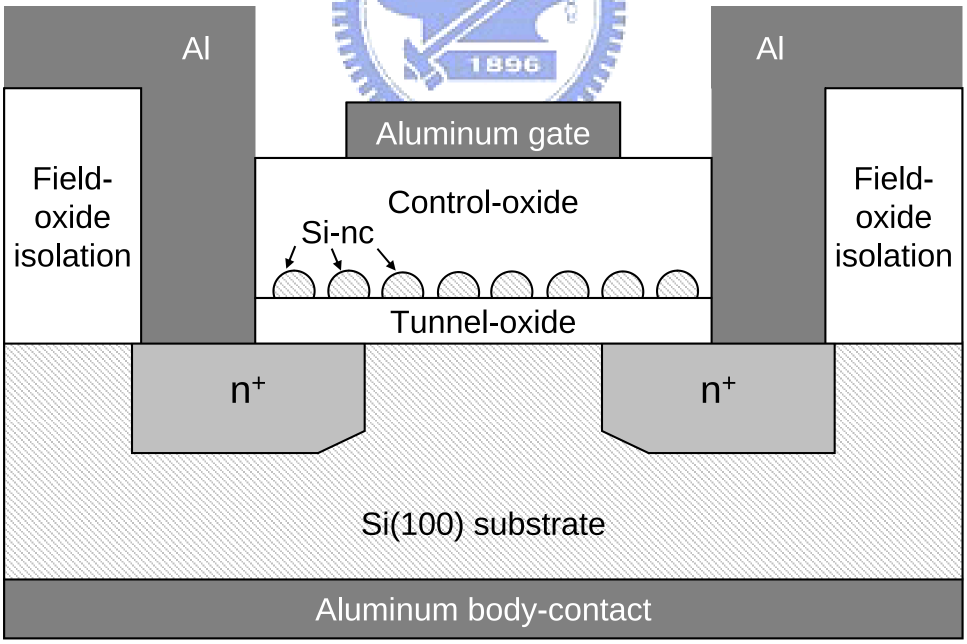


Fig. 6.2 Schematic of a MOSFET device with embedded Si nanocrystals.

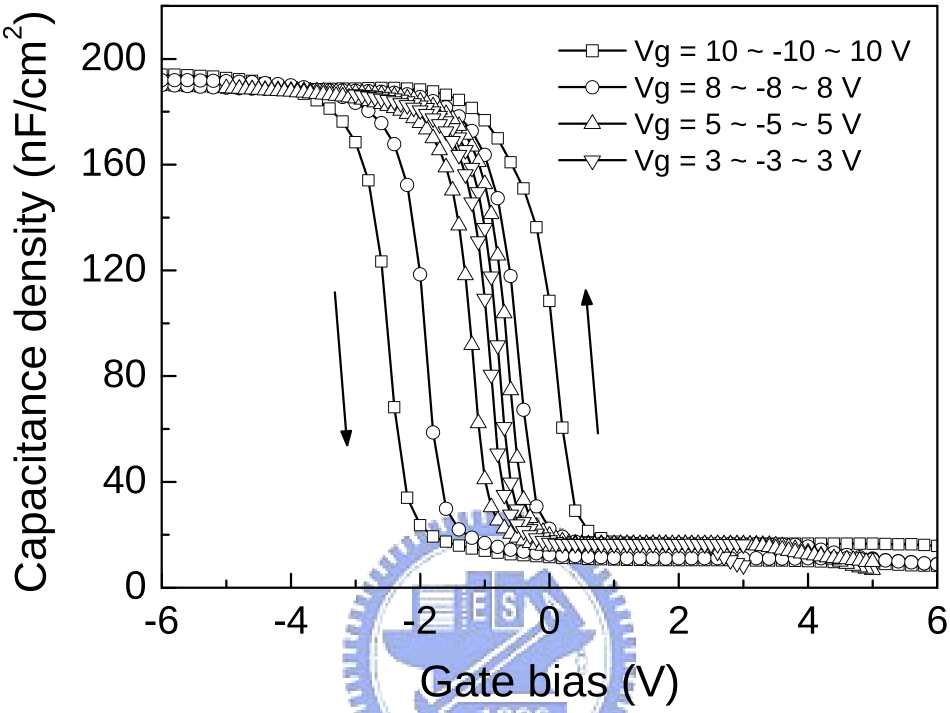
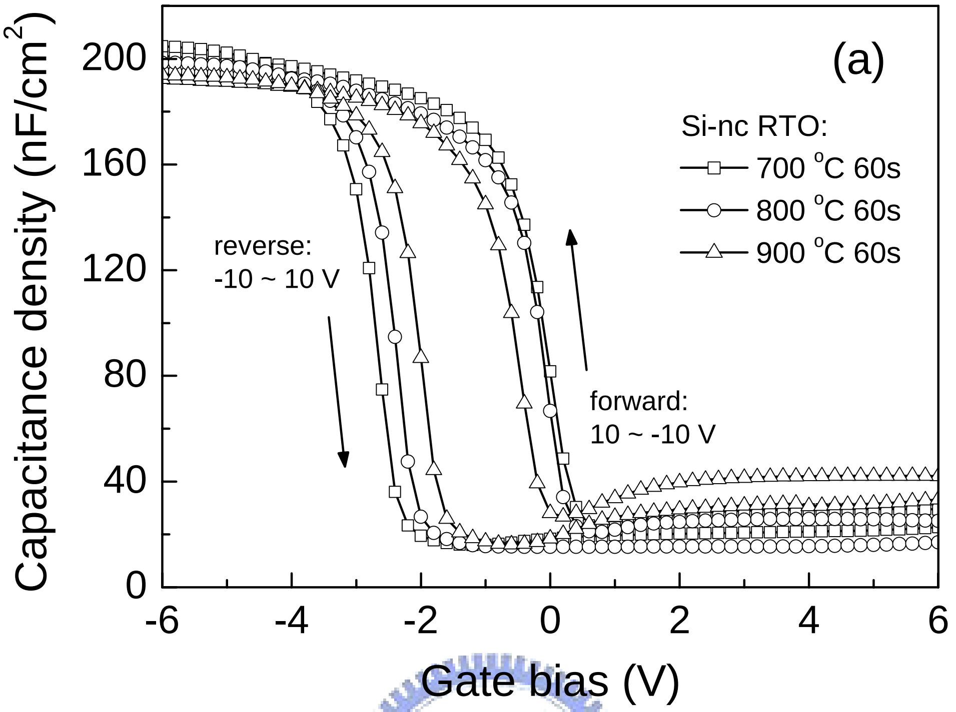
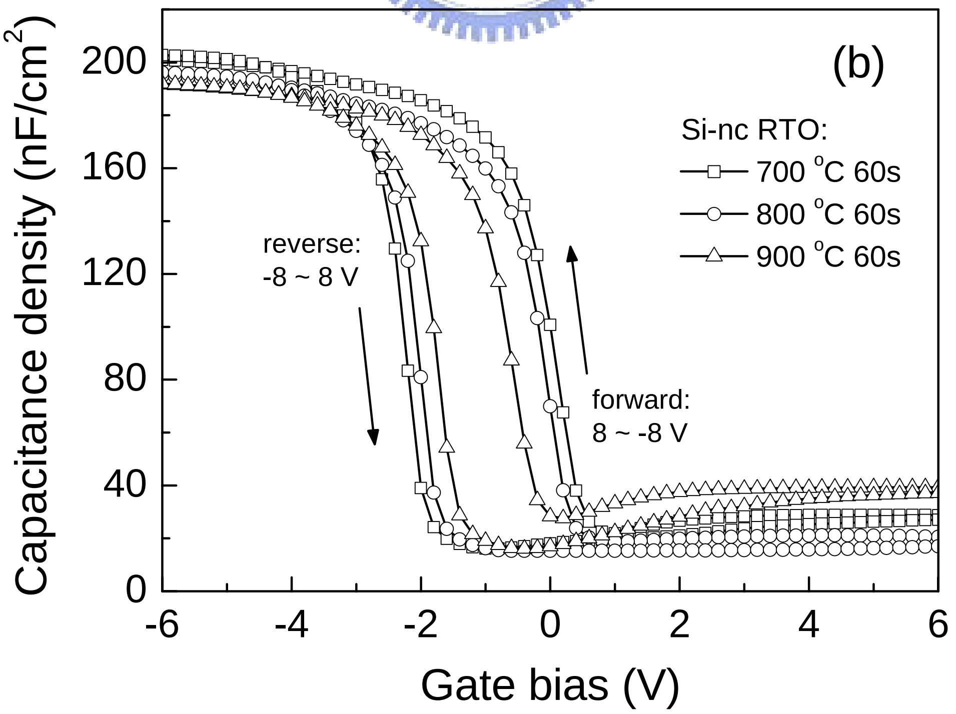


Fig. 6.3 *C*-*V* traces of a MOS capacitor embedded with Si nanocrystals; the gate-bias sweeps are ±10 V (□), ±8 V (○), ±5 V (△), and ±3 V (▽). The nanocrystal dots are formed by the *in-situ* RTA of a 3.5-nm *a*-Si film at 850 °C for 5 min.


(a)
Si-nc RTO:
700 °C 60s
800 °C 60s
900 °C 60s
reverse:
-10 ~ 10 V
forward:
10 ~ -10 V
Capacitance density (nF/cm²)
0
40
80
120
160
200
-6
-4
-2
0
2
4
6
Gate bias (V)


(b)
Si-nc RTO:
700 °C 60s
800 °C 60s
900 °C 60s
reverse:
-8 ~ 8 V
forward:
8 ~ -8 V
Capacitance density (nF/cm²)
0
40
80
120
160
200
-6
-4
-2
0
2
4
6
Gate bias (V)

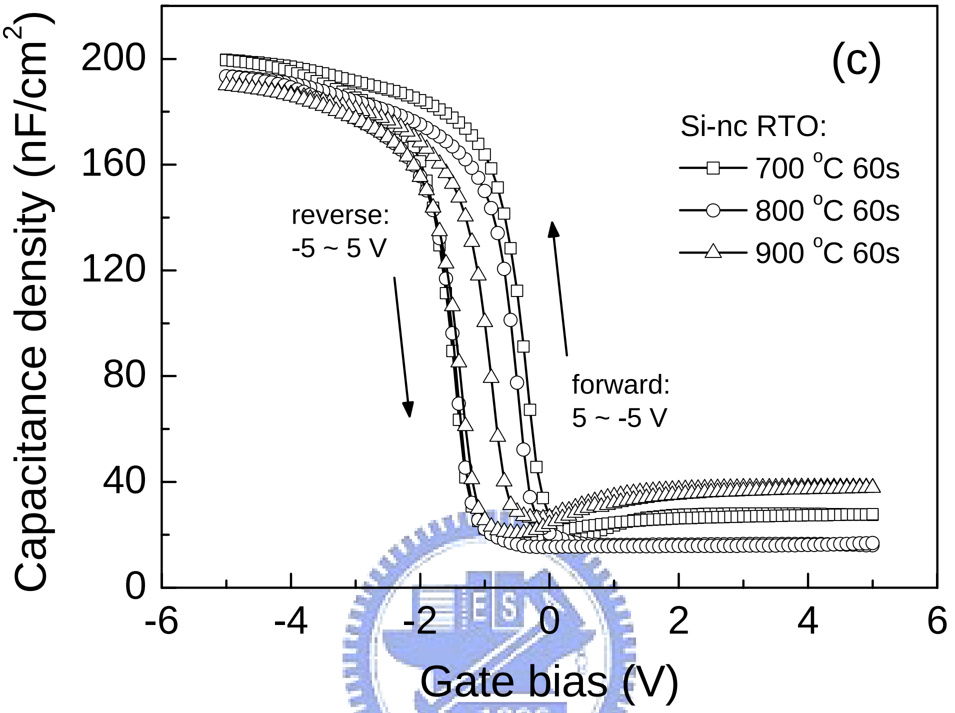


Fig. 6.4 *C*-*V* traces of MOS capacitors embedded with Si nanocrystals; the bias sweeps are of (a) ±10 V, (b) ±8 V, and (c) ±5 V. The nanocrystal dots are formed by *in-situ* RTA of a 3.5-nm *a*-Si film at 850 °C for 5 min and followed with *ex-situ* rapid thermal oxidation at 700 °C (□), 800 °C (○), and 900 °C (△) for 60 s.

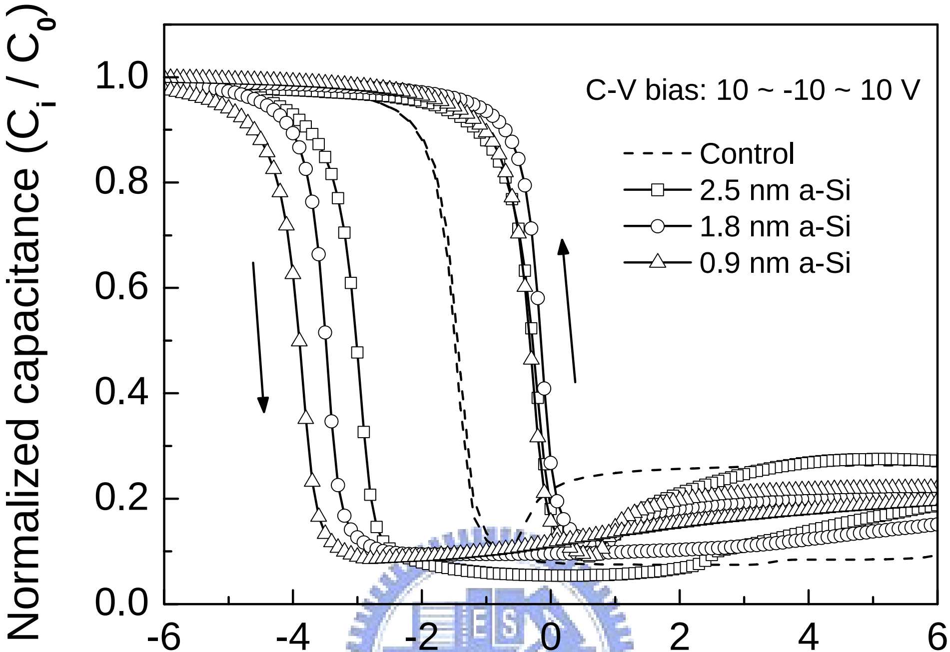


Fig. 6.5 *C-V* traces of MOS capacitors with (line+symbol) and without (dashed line) Si nanocrystals agglomerated from (□) 2.5 nm, (○) 1.8 nm, and (△) 0.9 nm thin *a*-Si layers. The gate bias is swept from 10 V to -10 V and back to 10 V.

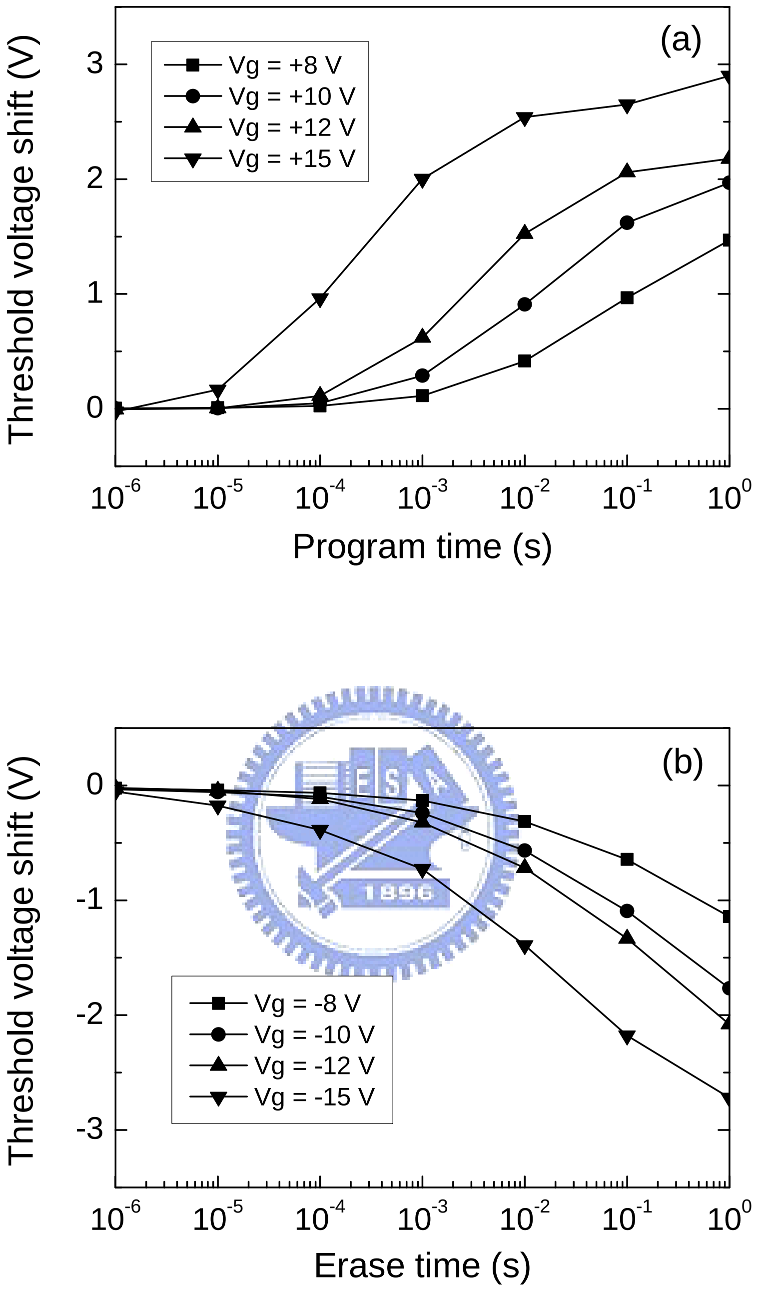


Fig. 6.6 Threshold voltage shifts as a function of (a) program and (b) erase time for a Si-nanocrystal floating-gate memory; different program/erase gate voltages (±8, ±10, ±12, and ±15 V) are used. The memory device is erased (programmed) at the corresponding negative (positive) gate bias for 1 s before the programming (erasure) starts.

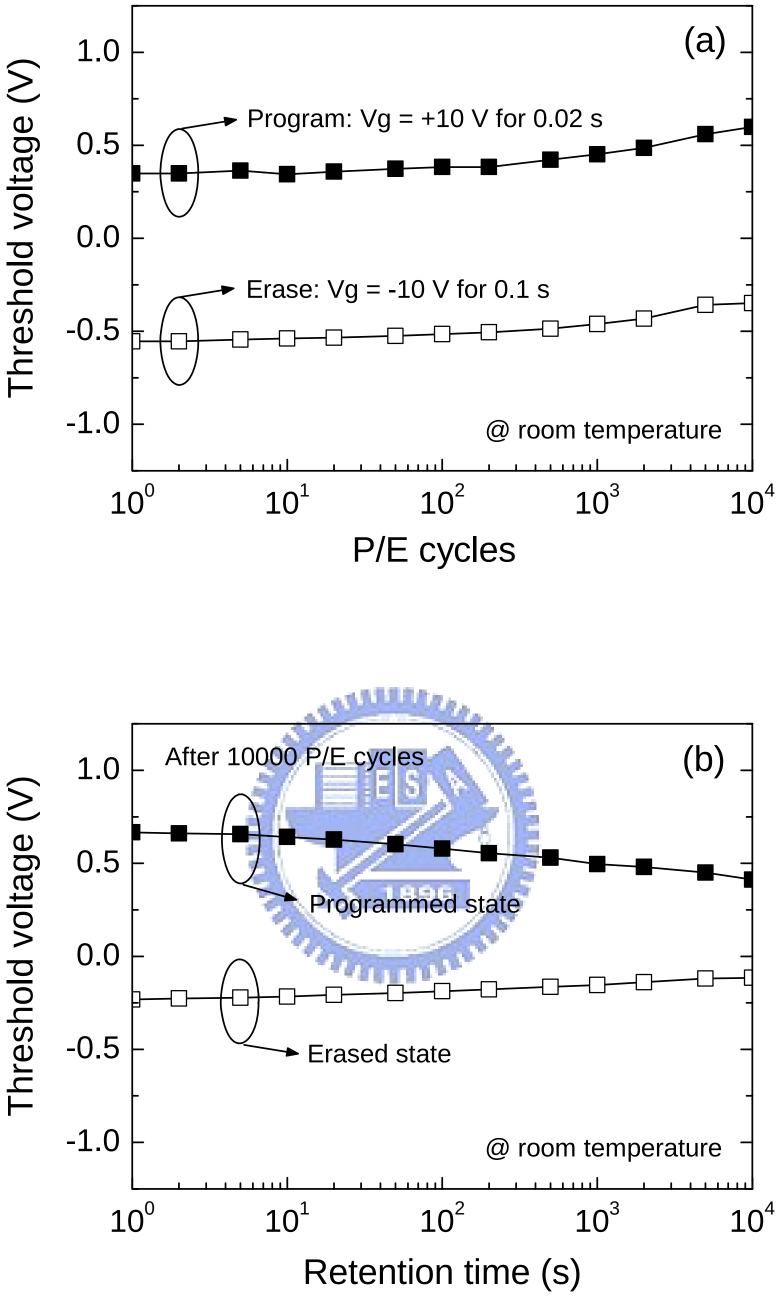


Fig. 6.7 (a) Endurance characteristics of nanocrystal-embedded MOSFETs; program and erase voltages of ±10 V were pulsed for 0.02 and 0.1 s, respectively. (b) Data retention characteristics after 10000 program/erase cycles. The programming and erasing conditions are the same as those in (a).

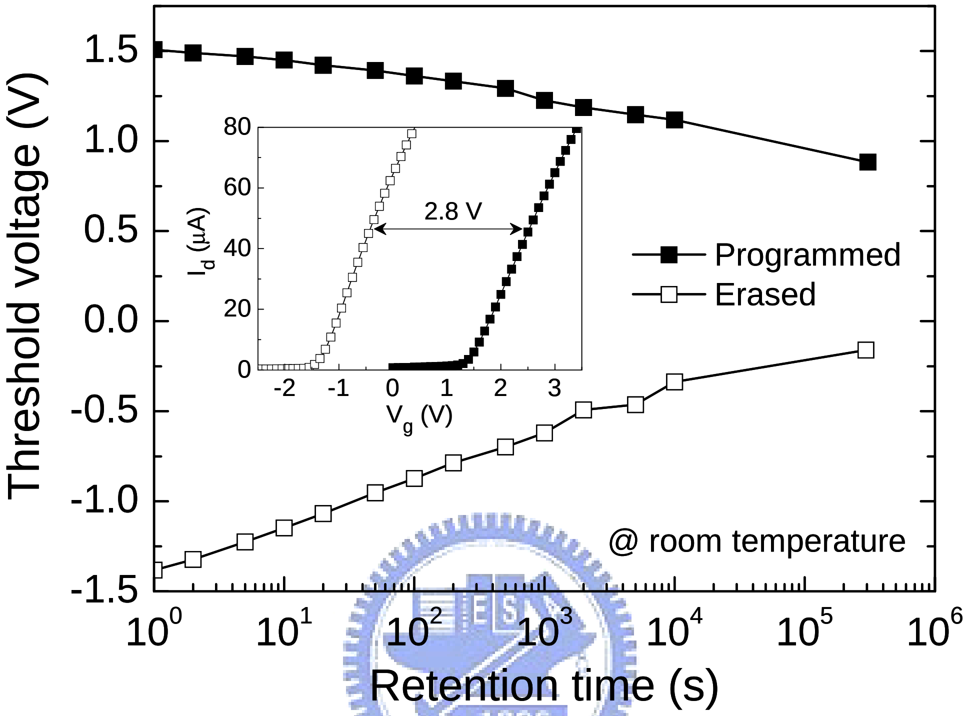


Fig. 6.8 Data retention characteristics for (■) programmed and (□) erased nonvolatile memory devices; (inset) corresponding drain current-gate voltage (I_d-V_g) curves. The gate pulse voltages are ±15 V for 1 s.

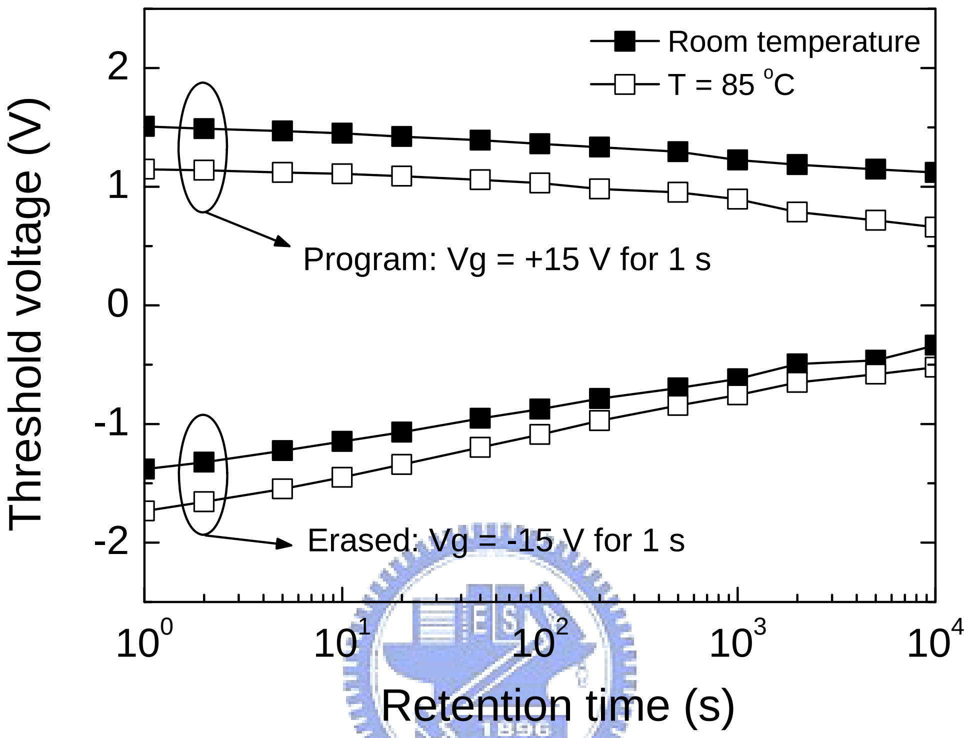


Fig. 6.9 Retention characteristics tested at room temperature and at 85 °C; the devices are programmed/erased at a gate bias of ±15 V for a pulse width of 1 s.

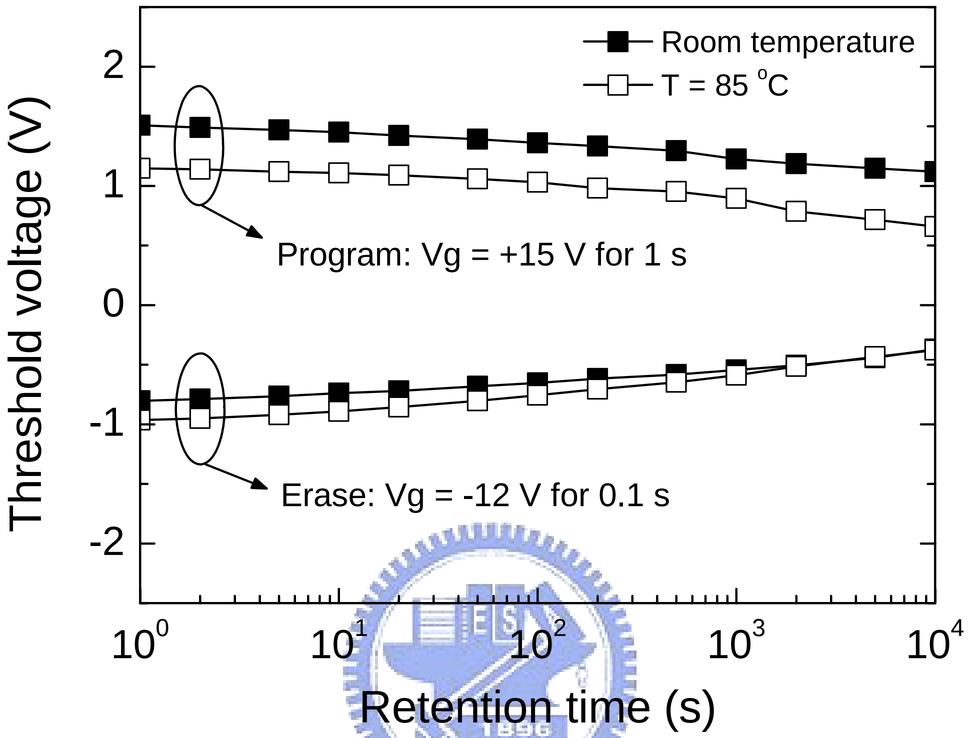


Fig. 6.10 Retention characteristics tested at room temperature and at 85 °C; the devices are programmed/erased at +15 and -12 V with a pulse width of 1 and 0.1 s, respectively.

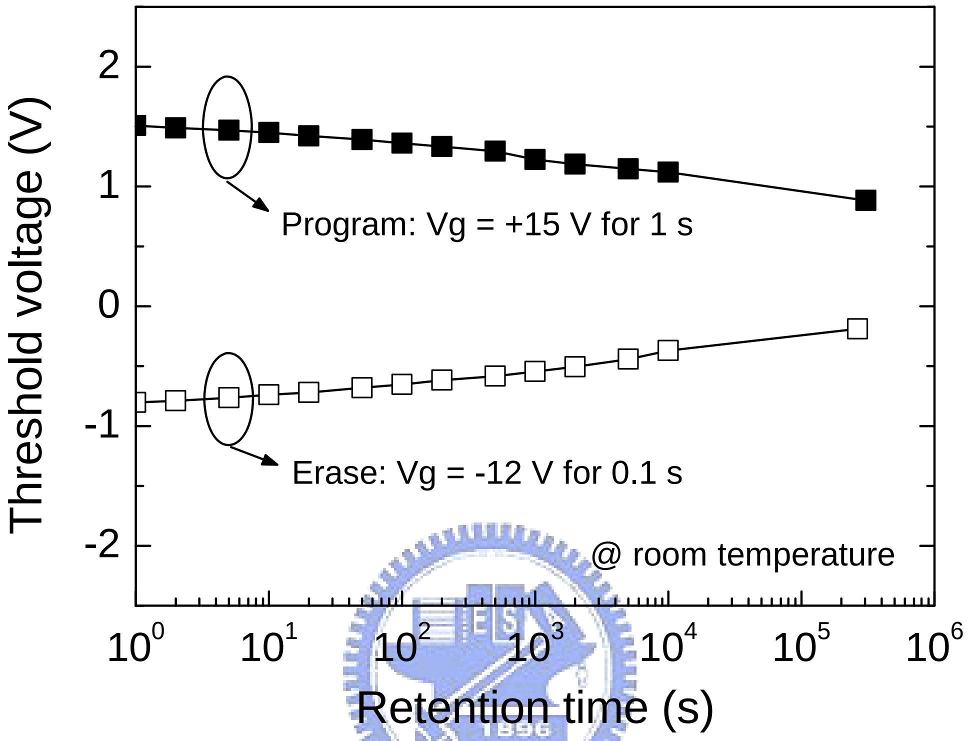


Fig. 6.11 Retention characteristics tested at room temperature; the devices are programmed/erased for 1 s at a gate bias of +15 and -12 V, respectively.

Chapter 7

Conclusions and Recommendations for Future Work

7.1 Conclusions

Three approaches to incorporating nitrogen in $CoTiO_3$ high-κ dielectric films, including the ion implantation of N_2^+, ion implantation of N^+, and N_2O plasma treatment, have been investigated. Nitrogen incorporation by ion implantation of N_2^+ can improve the electrical properties in terms of gate leakage, breakdown voltage and time-to-breakdown (T_{BD}). To reduce the impinging mass of implanted ion species, N^+ ion implantation has been used. The same trends can be found as those produced using N_2^+. Higher doses of N^+ can improve the performance further. An alternative N_2O plasma treatment is also an excellent method to improve the electrical properties, exhibiting better-behaved C-V curves, lower gate leakage currents and higher breakdown voltages while compared with the untreated samples.

tert-butyldimethyl silanol (BDMS)was evaluated as a silicon precursor for hafnium silicate deposition with tetrakis-(diethylamido) hafnium (TDEAH). BDMS has one OH group, which should react with chemisorbed TDEAH. However, the other *t*-butyl and methyl groups can passivate the substrate surface, and stop the further absorption of TDEAH. To remove the alkyl ligands or reconstruct the surface, a deposition temperature >500 °C is needed while using BDMS and TDEAH with O_2. This led to a deposition without the self-limiting properties of TDEAH. And it became difficult to control the uniformity and the surface roughness. High resolution transmission electron micrographs show that the films produced at 550 °C are rough.

To better utilize the BDMS in silicate deposition, an oxidant, such as water or ozone that could react with the BDMS at a lower temperature would be needed. Otherwise, a dynamic temperature control during the deposition may be needed, which is prohibitive for most CVD systems.

Carbon-free hafnium silicate thin-films were deposited by using MOCVD with alternative pulses of TDEAH and TPOS precursors. Hafnium silicates with high silicon contents ($Hf_{1-x}Si_xO_2$, x >0.5) were deposited at 250 °C without additional oxidants or plasma-enhanced techniques. Chemical compositions (XPS date) of the $HfSi_xO_y$ remained stable when an 800 °C vacuum RTA was performed after the deposition. A forming gas anneal at a temperature ranging from 380 °C to 450 °C could further improve the hafnium silicate interface quality. This low-temperature process could be promising for TFT or optoelectronic applications.

Hemispherical Si nanocrystals are self-assembled using a thermal agglomeration technique. Ultrathin (0.9–3.5 nm) *a*-Si films are deposited on a 4-nm tunnel-oxide layer using electron-beam evaporation. XPS analyses recorded during the *a*-Si deposition has verified a layer-by-layer deposition mode. AFM and TEM analyses have also confirmed a smooth and uniform deposition of the *a*-Si thin film. After the deposition, an *in-situ* annealing can activate the thermal agglomeration of Si and transform the ultrathin *a*-Si films into Si nanocrystals. *In-situ* XPS is used to monitor the evolution of Si deposition and agglomeration. Evidence shows that Si nanocrystals can be obtained at a moderate temperature (850 °C) within a short period of time (1–10 min), which is also confirmed by AFM and SEM analyses.

Different annealing temperatures have been tested for the Si agglomeration. Samples annealed at 700, 750, 800, and 850 °C for 5 min are checked by AFM and SEM. Annealing temperatures ≤700 °C are found inadequate to activate the dot agglomeration in a 3.5-nm thin film, at least not in the 5-min RTA period. When the *a*-Si film is annealed at 750 °C for 5 min, some incomplete agglomeration of dots is observed by AFM. Results of AFM and TEM analyses suggest that small dots are first nucleated on the surface of *a*-Si and then grow into hemispherical nanocrystals and deplete the surrounding *a*-Si. Surface analyses of samples annealed at 800 and 850 °C show densely distributed Si dots and suggest the completion of Si agglomeration after a 5-min annealing.

In order to evaluate how the surface oxide affects the Si agglomeration behaviors, different oxidation conditions are tested. For example, an *ex-situ* N_2 RTA on an ultrathin *a*-Si layer has shown no evidence of the surface coalescence and dot agglomeration. It is believed that a native oxide layer grown in air or during the N_2 RTA has prevented the *a*-Si film from coalescence and agglomeration. In another *in-situ* oxidation test, a low pressure condition was used to oxidize the surface of a 3.5-nm *a*-Si film at 650 °C. *In-situ* XPS revealed that the surface oxide was with inferior quality. The sample was then annealed in UHV at 850 °C for 5 min, but AFM analysis on this sample showed no Si-dot formation. Therefore, even an inferior surface oxide layer can still severely hinder the agglomeration of Si nanodots.

Although surface oxides can strongly affect the Si agglomeration, it is found that a dilute-HF dip before the vacuum RTA is efficient to remove the surface oxide and ensure Si-dot agglomeration. In one test, an SPM immersion was utilized to grow a chemical-oxide layer on a 5-nm *a*-Si film. Afterward, the sample was dipped in dilute-HF to remove the chemical oxides and then immediately loaded into the UHV system for the vacuum RTA. The Si-dot agglomeration is observed with this sample, even though it has been exposed to *ex-situ* treatments before the vacuum RTA. Therefore this agglomeration technique is applicable even after the thin *a*-Si film is treated with *ex-situ* processing steps, as long as the native oxide is carefully removed prior to the vacuum annealing.

In-situ annealing of *a*-Si layers with different thickness has resulted into Si nanocrystals with different sizes and densities. It appears that thinner *a*-Si layers have resulted into smaller and denser nanoparticles. This result provides a simple route of the nanocrystal size and density control. TEM analysis shows that single-crystal Si nanodots can be obtained when a thinner (1.8 nm) *a*-Si film is annealed. The *in-situ* annealing of a 0.9-nm *a*-Si layer results into Si nanodots with a mean radius of 5.1 nm and a dot density as high as 3.9×10^{11} cm^{-2}. In addition, the SEM analyses have shown a bimodal size distribution with the agglomerated nanocrystals, which can be explained by a multi-stage agglomeration process.

A simple XPS model is established to estimate the Si-dot size by using *in-situ* XPS analysis. The dot density and the surface coverage ratio can also be extracted with this model. In order to verify the feasibility of this model, XPS results acquired during the deposition and annealing of a 1.8-nm Si layer are used. The calculated dot density matches pretty well with the experimental result measured by SEM. The dot size predicted by this model also provides a fairly reasonable estimation while comparing it with the SEM results. As being demonstrated, the XPS model provides a method to estimate the agglomerated dot size and density *in situ*, even though the model uses relatively simplified assumptions.

The fabrication of a Si nanocrystal-embedded nonvolatile memory has been demonstrated using a thermal agglomeration technique. Hemispherical nanocrystal dots are self-assembled after annealing an ultrathin (0.9–3.5 nm) *a*-Si film in vacuum at 850 °C for 5 min, with their size and density controlled by the *a*-Si thickness. A dot density as high as 3.9×10^{11} cm^{-2} is obtained on the oxide surface, which achieves a stored charge density of 4.1×10^{12} cm^{-2} (electron + hole).

Floating-gate n-MOSFETs are fabricated with Si nanocrystals embedded between a 4-nm tunnel-oxide layer and a 17-nm control-oxide layer. Uniform FN tunneling is used to program and erase the Si nanocrystal floating gates. A V_t window of 0.9 V is achieved under P/E voltages of ±10 V for 0.02/0.1 s. The memory device also shows good endurance and charge retention behaviors after 10000 P/E cycles. Increasing P/E voltages to ±15 V creates a large memory window (>2.7 V) with the proposed memory device. After a retention test for 100 hours, a memory window of 1 V is maintained, exhibiting promising potential for nonvolatile memory applications. The retention characteristics have shown little temperature dependence with present samples, indicating that the charge-loss process is determined by the direct tunneling of stored charges into the tunnel-oxide/Si-substrate interface states. The nonvolatile memory characteristics of hemispherical Si nanocrystals are demonstrated using an agglomeration technique. The top-down process compatibility and self-assembly features of this technique show its potential for the nanocrystal memory applications.

7.2 Recommendations for Future Work

The $CoTiO_3$ dielectrics have shown high dielectric constant and improved electrical characteristics after nitrogen incorporation. However, it is difficult to extract the band energy levels using electrical characterizations because of the relatively thick, possibly silicate interfacial layer. This is also an issue for other high-κ gate dielectrics when it comes to the band energy extractions. Perhaps it is not that critical because the gate stack structure will eventually inherits the interfacial layer and take into consideration the overall performance of the gate stack. However, it can be still interesting to figure out the electronic energy band structure. One possible route is to deposit high-κ films on a stable material and then use photoelectron techniques to measure the band offsets between the dielectric films and the substrate. XPS technologies have been utilized to measure the valence band offset for dielectrics on semiconductor substrates. Although the question still remains that if there is an interfacial layer between the metal oxide layer and the semiconductor substrate, how to make sure the band offset measured by XPS is not affected? Depositing CoTiO3 films on a thermally stable metal film, for example Au or Pt may be able to eliminate the thick interfacial layer. Metal-oxide-metal (MIM) can be fabricated this way and the electrical characterizations of the MIM structure can provide information of the conduction band structure of the high-κ oxide layer. A sable metal with well-known work function is also needed for the gate electrode in order to have reliable band level extractions. The spin-on method may be worth a try if the adhesion is not raising another issue.

The MOCVD and ALD techniques for high-κ dielectrics are very important, especially when the implementation of high-κ dielectrics in the newest devices is actually an ongoing thing. The gas phase and surface reactions strongly affect the deposition mechanisms and may still need a lot of work, though it can be very tough to establish a stable and well-controllable system and take all possible parameters into consideration, especially for low temperature ALD. The moisture can be easily absorbed by the chamber walls or in the vapor tube, and then the emission of water or hydroxyl groups can differ the deposition parameters. The system maintenance can be a challenge, too. Most MOCVD precursors are reactive with the atmosphere moisture; thus a reliable design for the precursor delivery system can be crucial for making reproducible depositions.

The composition control of the Hf silicate thin film is the key to success in terms of implementing the Hf silicate to devices. Nitrogen incorporation has been found useful for preventing thermally-induced phase separation and re-crystallization.

The nitrogen can passivate the vacancies in the silicate matrix and increase the activation energy for the atoms to diffuse and reconstruct themselves. Though it may be more important to have the Hf, Si, and O atoms to be distributed uniformly through out the film at the very beginning, and then the nitrogen atoms come in play after post-deposition nitridation treatments. *In-situ* investigations for the deposition dynamics can be useful.

The hemispherical Si nano-dots have shown some interesting physical and electrical properties. There are several things that may worth further work. First is to investigate the agglomeration mechanism in more details. In the present work the nucleation of small dots on the *a*-Si surfaces were observed. *In-situ* investigations about how they grow into larger dots and finally touch down to the underlying oxide surfaces can be useful for establishing a more thorough thermodynamic model of the agglomeration process. Another issue is to consider the effects of oxide surface properties on the Si agglomeration behaviors. Although it has been suggested that the dot sizes and densities are mainly predicted by the initial Si thickness, the oxide surface bonding can still be a factor. In present study some blanket oxide films went through a dilute-HF dip and a DI water rinse, which possibly created an OH-terminated surface. The hydroxyl surface passivation may change the interface energy between the e-beam evaporated Si layer and the oxide interlayer. If the bonding strength or interface strains between the *a*-Si and SiO_2 layers have been altered, the critical temperature for thermal agglomeration may also differ. Studies by others on the thermal agglomeration of SOI films have shown self-aligned dot formation along patterned narrow features. It has been reported that SOI fins with their width less than 1 μm have agglomerated into well aligned dot arrays. This may be useful for self-assembled electronic devices. Furthermore, the interface strains between agglomerated hemispherical dots and the tunnel-oxide may be an important factor that affects the charge injection from the substrate to the Si dots. If there are accumulated strains (because of the structural deformation of silicon) remained at the Si-dot/oxide interfaces, more interface states may have been created at the interfaces. This will cause reliability issues for the Si-nanocrystal nonvolatile memories.

As to the XPS model for monitoring the nanocrystal dot sizes and densities, it would be more useful if a thermodynamic model could be incorporated also. The thermodynamic model can be used to predict the dot size based on the initial *a*-Si thickness. The predicted dot size then can be added into a statistical distribution function (for example a Gaussian or lognormal function). This distribution function along with the theoretically estimated dot size can be fitted to the XPS model and the XPS results. Therefore the other coefficients of the distribution function can be obtained for a better fit to the experimental results.

The nanocrystal nonvolatile memory devices presented in this work are pretty simple. Because of some practical limits there were little opportunities to try more sophisticated memory structures. One interesting topic would be the combination of high-κ dielectrics with the agglomerated nanocrystals. Preliminary tests have shown that the thermal agglomeration process has little effects on the Hf silicate films. *In-situ* XPS suggested that Hf silicates were stable even an ultrathin *a*-Si film was deposited on top and then annealed in situ at 850 °C for 5 min. Therefore the Hf silicate can be integrated into the memory fabrication process. Hf silicate films can be deposited as the tunnel-oxide layer and the Si dots can be formed on the silicate films without exposing the sample to atmosphere. Multilayer structure consisting of HfO_2, Hf silicate and Si nanocrystal layers is also achievable.

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學經歷

Curriculum Vitae

姓名: 陳建豪

性別: 男

出生: 西元 1976 年 11 月 3 日

籍貫: 台灣省雲林縣

住址: 新竹市光復路二段 298 巷 9 弄 9 號 5 樓

學歷: 國立台灣大學電機系

[1995 年 9 月 - 2000 年 6 月]

國立交通大學電子研究所碩士班

[2000 年 9 月 - 2001 年 6 月]

國立交通大學電子研究所博士班

[2001 年 9 月 - 2007 年 9 月]

博士論文題目: 應用高介電常數絕緣層與矽奈米微晶粒於超大型積體電路元件之研究 (A Study of High-κ Dielectrics and Si Nano-crystals for ULSI Devices)

Publication List

1. International Journal:

[1] **J. H. Chen**, T. B. Huang, X. Wu, D. Landheer, T. F. Lei, and T. S. Chao, "Performance Improvement of $CoTiO_3$ High-k Dielectrics with Nitrogen Incorporation," *J. Electrochem. Soc.*, vol. 154, no. 1, pp. G18-G23, 2007.

2. International Letter:

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[4] X. Wu, M. Couillard, M.-S. Lee, **J.-H. Chen**, G. A. Botton, D. Landheer, Z.-H. Lu, W.-T. Ng, and T.-S. Chao, "Spatially-resolved EELS and EDS Analysis of HfO_xN_y Gate Dielectrics Deposited by MOCVD using $[(C_2H_5)_2N]_2Hf$ with NO and O_2," in *Microscopy and Microanalysis*, (Extended abstracts of paper presented at Microscopy and Microanalysis in Savannah, Georgia, USA, August 1-5, 2004), vol. 10, no. S02, pp. 606-607.

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