國立交通大學

光電工程研究所碩士班

碩士論文

具有輕摻雜汲極之複晶矽

薄膜電晶體電性模型建立

The I-V Model of Poly-Si TFTs with LDD Structure

研 究 生：高士欽

指導教授：冉曉雯　教授

中 華 民 國 九 十 四 年 六 月

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中文摘要

複晶矽薄膜電晶體在面板技術的應用上，由於其具有高遷移率，可以實現系統面板(System on Panel)的技術，也就是可以將周邊電路直接以複晶矽薄膜電晶體實現在玻璃基板上，與面板矩陣電路結合成所謂的系統面板。然而，在這樣的技術發展中，準確的元件模型是SPICE tool中最重要的基礎，在本論文中，我們特別針對具有輕摻雜汲極(Lightly-Doped Drain, LDD)結構之N型低溫複晶矽薄膜電晶體建立DC電性模型。

首先，我們研究輕摻雜汲極寄生電阻的萃取方法。利用變化不同的通道長度和不同的輕摻雜汲極長度，可以萃取出不同的寄生電阻。然後我們建立包含寄生電阻效應的元件等效電路，根據等效電路，推導出元件的電性模型。模型產生的電性，可以準確描述元件在通道長度6 μm – 30 μm以及LDD長度0 μm – 3 μm的輸出特性。除了基本的電流輸出特性，我們也分析元件的轉導特性以及輸出阻抗特性在不同偏壓下的變化，並利用前述的模型解釋寄生阻抗所造成的影響；另外，由於複晶矽薄膜特有的DIGBL(Drain-Induced Grain Barrier Lowering)效應，LDD區域的阻抗效應其實會在LDD長度越長通道長度越短的狀況下影響到元件的線性區特性，我們也針對LDD結構在不同偏壓下的等效阻抗變化做了初步的模型；最後，我們並結合了元件在變溫量測下定義出的晶粒邊界位障，成功建立了包含薄膜差異性、元件LDD結構差異對元件特性影響的模型。

The I-V Model of Poly-Si TFTs with LDD Structure

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Abstract

To realize the system-on-panel (SOP) technology, in which we combine the peripheral circuit and panel array circuit on the same glass substrate, it is essential to develop accurate device *I-V* model for Poly-Si TFTs. In this thesis, we especially focus on the modeling of n-channel devices with LDD(Lightly-Doped Drain) structure.

Firstly, parasitic resistance parameters were extracted from devices with various channel length and LDD length. Then, the device equivalent circuit had been developed including the extracted parasitic resistance parameters. An accurate I-V model was established by combining basic TFT model and the parasitic resistance effects. The model had been verified for devices with channel length varied from 6 μm to 30 μm. The transconductance and output resistance behavior are also well explained by our proposed model. The special DIGBL effect of poly-Si film is also observed when the devices with large LDD length and short channel length. We used testkey structure to clarify this effect and established adequate model to explain this phenomena. Finally, the model was combined with the grain barrier height model by extracted the grain barrier height from the Arrenhius plot. Good agreements are found when comparing the simulated results and the experimental results.

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高士欽 2005 仲夏 於交大電資大樓

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Chapter 1

Introduction

1-1. Overview of Polysilicon TFT Technology

In recent years, polycrystalline (poly-Si) silicon thin film transistors (TFTs) become more noticeable because of their widely applications in active matrix liquid crystal displays[1-3], some memory devices such as dynamic random access memories (DRAMs)[4], static random access memories (SRAMs)[5], electrical programming read only memories (EEPROMs)[6], electrical erasable programming read only memories (EPROMs)[7], linear image sensors[8], thermal printer heads[9], photodector amplifier[10], scanner, neutral network[11] and three dimension LSIs[12].

Commercially, amorphous silicon (a-Si) TFTs has been used in large area LCDs and the pixel array, but the connection of the external driving circuits and pixel array is necessary. This increases the assembly complexity. For poly-Si TFTs, carrier mobility larger than 100 cm^2/V-s is easily achieved by present mature technology, which is enough to be used as peripheral driving circuits [5]. Therefore, it is possible to integrate the pixel array and the driving circuits on the same glass to reduce the assembly complexity and cost. In addition, because of the higher mobility of poly-Si TFTs, the dimension of the poly-Si TFTs can be made smaller than that of amorphous silicon TFTs for high density' high resolution AMLCDs.

1-2. Defects in Poly-Si Film

The poly-Si material is a heterogeneous material made of very small crystals of silicon of silicon atoms in contact with each other constituting a solid phase material.

These small crystals are called crystallites. The main difference with a monocrystalline material is the presence of these crystallites that have any type of orientation that means a break in the crystal from one crystallite to the other. Because the material remains solid, the atoms at the border of a crystallite are also linked to the neighbor crystallite ones. However, these atom bonds are disoriented in comparison with a perfect lattice of silicon. This border is called a grain boundary. The break in the lattice at grain boundary creates a break in the periodicity of the potential in the material, and as a mater of fact, creates new energy states in the band gap of the silicon. In other words, this means that energy states are created at grain boundaries, which can govern the electrical behavior of the film and consequently of the devices based on the polycrystalline material. These states can be spread all over the band gap in function of the nature of the break. For example dangling bonds create deep states in the band gap that can be very electrically active. They can act as acceptor-like traps or donor-like ones depending on the position of the Fermi level in the band gap. This type of defect has to be minimized in the layer. Some special treatments such as hydrogen plasma can decrease the number or the equivalent density of these defects.

The poly-Si material is, as previously mentioned, a heterogeneous material due the presence of grain boundaries. These grain boundaries act as energy barriers that the carriers have to overcome. The conduction is affected by the grain boundaries in comparison with its monocrystalline counterpart. To describe the conduction in the polycrystalline material, the first point is to calculate the energy barrier present at grain boundaries, which limits the transport of carriers from one crystallite to the other. J.Y. Seto proposed the first credible model.[13]

Seto's model assumptions

The Seto's model is based on the following assumptions:

- Poly-Si film has small grain size,
- The single crystalline silicon energy band structure is assumed to be applicable inside the crystallites,
- Doping concentration in poly-Si is uniform,
- All the doping atoms are ionized,
- All the grains have the same size, cubic shape,
- The representation is mono-dimensional,
- The grain boundaries have no thickness,
- The defects are carrier traps that are located in the grain boundaries. In this condition, the trap concentration is defined per surface unit. The trap is assumed to be initially neutral and become charged by trapping carriers,
- The traps are acceptors in the n-type and donors in the p-typed semiconductor,
- The trap energy level is unique and located more or less in middle of the forbidden band.

Barrier height calculation:

We consider the different following parameters: X, extension of the space charge region; N_D, donor doping atom concentration; N_{TA}, acceptor like trap surface density at grain boundaries; ε_0, permittivity in vacuum; ε_s, semiconductor permittivity; L_G, size of the grain; φ, the electrostatic potential; x, the position coordinate.

The distribution of the charges in the material is schematically described Figure 1-2-1. At grain boundaries, the surface trap charge density is qN_{TA}, which thus compensates the charge of the volume ionized doping atom concentration (qN_D). An abrupt depletion approximation is used to calculate the energy band diagram in the crystallite.

In the space charge region, for $0<x<\frac{X}{2}$ $\quad \frac{d^2\varphi}{dx^2}=-\frac{qN_D}{\varepsilon_r\varepsilon_0}$ (1-2-1)

Out of the space charge region, $\frac{X}{2}<x<\frac{L_G}{2}$ $\quad \frac{d^2\varphi}{dx^2}=0$ (1-2-2)

Considering that at the border of the space charge region the electric field is null:

$$\left[\frac{d\varphi}{dx}\right]_{X/2}=0 \text{ for } 0<x<\frac{X}{2} \;:\; \frac{d\varphi}{dx}=-\frac{qN_D}{\varepsilon_s\varepsilon_0}x+cst=\frac{qN_D}{\varepsilon_s\varepsilon_0}\left(\frac{X}{2}-x\right)$$

$$\frac{X}{2}<x<\frac{L_G}{2} \;:\; \varphi(x)=\varphi\left(\frac{X}{2}\right) \;:\; \varphi(x)=-\frac{qN_D}{2\varepsilon_s\varepsilon_0}\left(\frac{X}{2}-x\right)^2+\varphi\left(\frac{X}{2}\right)$$

Thus the energy barrier height (E_B) is defined at grain boundaries as the energy difference between the positions $x = 0$ and $x = \frac{X}{2}$.

$$E_B=-\left(q\varphi(0)-q\varphi\left(\frac{X}{2}\right)\right)=+\frac{q^2N_D}{2\varepsilon_s\varepsilon_0}\left(\frac{X}{2}\right)^2 \quad E_B=+\frac{q^2N_D}{8\varepsilon_s\varepsilon_0}X^2 \qquad (1\text{-}2\text{-}3)$$

The value of X has to verify for the electrical neutrality of the global material, which means $XqN_D^+=qN_{TA}^-$. N_{TA}^- is the ionized part of N_{TA}.

The Seto's model defines a critical concentration (N_D^*), which corresponds to this limit: $\frac{X}{2}=\frac{L_G}{2} \rightarrow X=L_G \rightarrow N_D^*=\frac{N_{TA}}{L_G}$ (1-2-4)

For a fixed trap density, if the effective doping concentration is higher than the critical concentration, the space charge extension is lower than the crystallite site. On the contrary, the crystallite is fully depleted.

$N_D>N_D^*$: $X=\frac{N_{TA}}{N_D}$ and $E_B=+\frac{q^2}{8\varepsilon_s\varepsilon_0}\frac{N_{TA}^2}{N_D}$ (1-2-5)

The expressions of the potential in the both regions are shown as follows:

$$0<x<\frac{X}{2} \qquad \varphi(x)=-\frac{qN_D}{2\varepsilon_s\varepsilon_0}\left(\frac{N_{TA}}{2N_D}-x\right)^2 \tag{1-2-6}$$

$$\frac{X}{2}<x<\frac{L_G}{2} \qquad \varphi(x)=0 \tag{1-2-7}$$

$N_D<N_D^*$: $X=L_G$ with $L_GN_D=N_{TA}$ $\quad E_B=+\frac{q^2N_D}{8\varepsilon_s\varepsilon_0}L_G^2$ (1-2-8)

The potential variation in the crystallite is expressed by the following:

$$\varphi(x)=-\frac{qN_D}{2\varepsilon_s\varepsilon_0}\left(\frac{L_G}{2}-x\right)^2 \tag{1-2-9}$$

1-3. RPI Model for Poly-Si TFT

The poly-Si TFT models could be divided into three categories: the models that try to incorporate the physics related to individual grain boundaries[14], the models that use close form analytical expressions for current-voltage characteristics[15,16], and the models based on effective medium. In recent years, several models for poly-Si TFTs have been proposed. Lin et al. obtained an expression for grain barrier height as a function of gate bias and the lateral electric field from a quasi-two-dimensional formulation of Poisson's equation. This solution was incorporated in an expression for the drain current in poly-Si TFTs. Further insight relating the characteristics to the poly-Si material parameters was provided by Fortunato and Magliorato [17]. Other solutions use Poisson's equation with the inclusion of space charge due to traps. Still others seek formulations with a minimum of empirical approximations. Although useful for the insight they provide, these expressions tend to be too complication for implementation in circuit simulators. The effective medium approach permits the development of comparatively simple models with only a few easily extractable parameters. Although these parameters cannot always be directly related to material

properties, such models are attractive for use in SPICE type circuit simulators.

The above models are mainly developed for long-channel poly-Si TFTs although later versions by Jacunski et al. [18,19] have included physics based formulations of important mechanisms such as the kink effect, the field effect mobility in moderate inversion, and the subthreshold current. Finally, the most recent models based on these semi-empirical effective medium approach also include short-channel effects, drain induced barrier lowering (DIBL), velocity saturation, temperature effects, and mobility degradation at high gate bias.[18,20-22]

The poly-Si TFT models developed by Jacunski et al.[18] are essentially unified models for long-channel devices. Above threshold, the conducting channel (I_a) in the non-saturated regime is given by an expression similar to that used for long-channel crystalline MOSFETs:

$$I_a=\mu_{FET}C_{ox}\frac{W}{L}\left(V_{gt}-\frac{V_{dse}}{2\alpha_{sat}}\right)V_{dse} \qquad (1\text{-}3\text{-}1)$$

Here, μ_{FET} is the gate voltage dependent field-effect mobility that includes the effects of the trap states; $C_{ox}=\varepsilon_i/d_i$ is the oxide capacitance per unit area, where ε_i is the dielectric permittivity and d_i is the thickness of the gate oxide; W and L are the gate width and length, respectively; α_{sat} is the body constant; $V_{gt} \equiv V_{gs}-V_T$ is the effective extrinsic gate voltage swing, where V_{gs} and V_T are extrinsic gate-source voltage and threshold voltage given by the following interpolation function that tends to V_{ds} in the linear regime and to the saturation voltage V_{sat} in saturation.

$$V_{dse}=\frac{V_{ds}}{\left(1+\left(\frac{V_{ds}}{V_{sat}}\right)^{m_{ss}}\right)^{1/m_{ss}}} \qquad (1\text{-}3\text{-}2)$$

The parameter m_{ss} controls the transition at saturation. The above threshold saturation voltage in this model is defined as the value of V_{ds} for which $\frac{\partial I_a}{\partial V_{ds}}=0$,

which gives

$$V_{sat}=(2)^{1/m_{ss}}\,\alpha_{sat}V_{gt}$$

For the long-channel case, we typically have $m_{ss}>>1$, in which case $V_{sat}\sim\alpha_{sat}\,V_{gt}$. Below threshold, the current is dominated by diffusion and is given by:

$$I_{sub}=\mu_s C_{ox}\frac{W}{L}(\eta V_{th})^2\exp\left(\frac{V_{gs}-V_T}{\eta V_{th}}\right)\left[1-\exp\left(\frac{-V_{ds}}{\eta V_{th}}\right)\right] \qquad (1\text{-}3\text{-}3)$$

where η is the subthreshold ideality factor, and μ_s is subthreshold mobility, and $V_{th}=k_BT/q$ is thermal voltage.

A unified model can be obtained for the drain current (I_d) by combining the above-threshold and the subthreshold currents as follows:

$$\frac{1}{I_d}=\frac{1}{I_{sub}}+\frac{1}{I_a} \qquad (1\text{-}3\text{-}4)$$

To make this possible, we extend the range of equation (1-3-1) into the subthreshold regime and retain equation (1-3-3) into the above-threshold regime in such a way that I_d approaches the correct limiting behavior in both regimes. This is possible if V_{gt} in equation (1-3-1) is replaced by the following effective gate voltage overdrive, which is valid above and below threshold:[25,26]

$$V_{gte}=\eta V_{th}\left[1+\frac{V_{gt}}{2\eta V_{th}}+\sqrt{\delta^2+\left(\frac{V_{gt}}{2\eta V_{th}}-1\right)^2}\right] \qquad (1\text{-}3\text{-}5)$$

where δ is a transition parameter with a typical value of about 2. From Eq. (1-3-5), we have $V_{gte}\sim\eta V_{th}$ below threshold and $V_{gte}\sim V_{gs}$-V_T above threshold.

In poly-Si TFTs, not all charge carriers induced in the channel by the gate voltage will be free to contribute to the drain current. Instead, a significant of the carriers will be captured by traps associated with the grain boundaries, especially near and below

threshold. This effect can be taken into account by proposing so-call field effect mobility as follows:

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_1 \left| \frac{2V_{gte}}{\eta V_{th}} \right|^{m_u}} + \frac{1}{\mu_0} \tag{1-3-6}$$

where m_μ, μ_0 and μ_1 are extractable mobility parameter.

Semi-empirical, accounting for feedback and using results from the impact ionization rate theory, the increase of the drain current caused by the kink effect can be modeled as follows[19,22]:

$$I_{kink} = \left(\frac{L_{kink}}{L} \right)^{m_{kink}} \left(\frac{V_{ds} - V_{dse}}{V_{kink}} \right) exp\left(\frac{-V_{kink}}{V_{ds} - V_{dse}} \right) I_d \tag{1-3-7}$$

where V_{kink}, L_{kink} and m_{kink} are model parameters, and Id is the primary drain current discussed above.

1-4. Motivation

Because the mobility is high as 150 cm^2/V-s, the impact ionization current is needed to suppress. Usually we use LDD structure to suppress the Kink effect, the parasitic resistance can lowing the electrical field at drain region. Above these models for Poly-Si Thin Film Transistor, they did not detail to discuss the effect of parasitic resistance. If we use existing SPICE tool to simulate *I-V* of Thin Film Transistor with LDD structure, the characteristic of drain current would be inaccuracy. We can say that inaccuracy of drain current is due to the lack of the parameters of parasitic resistance. For this reason, we plan to investigate parasitic resistance in different temperature and electrical field. We would analyze the measured data to obtain useful parameters to define some fundamental physical phenomenon such as threshold voltage and effective channel length. In this study, the model of poly-Si TFTs with

LDD structure had been proposed.

1-5. Thesis Outline

In the chapter 1, we discuss the effect of trap in the grain boundary and explain the meaning of grain barrier height. The grain barrier height equation is deduced based on the Seto's model. But it is inapposite for big grain size of thin film transistor. Then we discuss RPI model that is for implementation in a SPICE circuit simulator. The intrinsic DC model describes all four regimes of operation: leakage, subthreshold, above threshold, and kink.

In the chapter 2, first we briefly describe poly-Si thin film transistor structure in this study and the main steps of process. We measured different structures of thin film transistor with LDD. The study shows the characteristics of different LDD structure, for example, self align LDD and gate overlap LDD. And we extracted sufficient parameters of parasitic resistance for our model.

In the chapter 3, we deduce the LDD model for Poly-Si TFT by using equivalent circuit. In 3-2, the parasitic resistance model was using simulate the characteristic of current in the linear region. Then we discuss the grain barrier model and describe the current model.

In the chapter 4, we would discuss the limit of voltage region about these parasitic resistance models.

Chapter 2

Characteristics of thin film transistor with different LDD structures

2-1. Device structure and fabrication process

The figure 2-1-1 shows that cross-sectional view of a poly-Si TFT with self-align LDD. These devices were fabricated on glass substrate with the channel film deposited as amorphous silicon to a thickness of 50 nm. The film was crystallized by excimer laser annealing (ELA). After the device islands were defined, a 100-nm gate oxide was deposited. In this study we need gate overlap LDD and self-align LDD. Therefore, gate overlap region is defined by mask and self-align region is defined by gate metal. We can manufacture different length of GOLDD and SALDD.

2-2. Parameter extraction

In this study, the parasitic resistances dominated by the LDD regions are extracted from device characteristics directly. It is well known that the turn-on resistance (R_{ON}) for devices operated in linear region can be express as:

$$R_{ON} = \left.\frac{\partial V_D}{\partial I_D}\right|_{V_D \to 0}^{V_G} = R_{ch} + 2R_P \qquad (2\text{-}2\text{-}1)$$

where R_{ch} and R_p represent channel resistance and parasitic resistance. The channel resistance in the linear region can be given approximately by:

$$R_{ch} = \frac{L}{W\mu_0 C_{ox}(V_G - V_T)} \qquad (2\text{-}2\text{-}2)$$

where C_{ox} is the capacitance per unit area, W, L, and V_T are intrinsic channel width, length, threshold and voltage, respectively. V_T is defined, for devices with long

channel length, as the gate voltage when the normalized drain current equal to 10^{-8} A under small drain bias.

With characteristics of devices with different channel length, the parasitic resistance R_p can be extracted by plotting $R_{on} \cdot W$ versus L as in figure 2-2-1 [23, 24]. It is found that all the lines merge at $L = \ell_0$ and has a residual value of gate-voltage independent R_p. ℓ_0 can be considered as a characteristic length that replaces the L to be L_{mask}- ℓ_0 in our model. The physical meaning of ℓ_0 relates to the carrier redistribution effect when ℓ_0 being larger than zero and represents the current spreading effect when ℓ_0 being negative. The extracted R_p and ℓ_0 for devices with various LDD lengths are listed in Table I. It is found that the extracted R_p value is almost proportional to the LDD lengths.

By replacing the extracted R_p and $L = L_{mask}$- ℓ_0 into equation 2-2-2, under small drain bias, the transconductance can be written as [23]

$$G_M \equiv \frac{\partial I_{lin}}{\partial V_G} \cong A V_D \left(\frac{R_{ch}}{R_p + R_{ch}}\right)^2 = A V_D [A R_p (V_G - V_T) + 1]^{-2} \quad (2\text{-}2\text{-}3)$$

where $A \equiv \frac{W \mu_0 C_{ox}}{L_{mask} - l_0}$. As a result, the intrinsic mobility μ_0 can be defined by comparing the calculated transconductances and the measured ones under large gate bias and small drain bias as shown in Figure 2-2-2.

2-3. Characteristics of device with GOLDD structure

In the section, we would discuss the characteristics of devices with gate overlapped lightly doped drain architecture (GOLDD) structure. For device with

GOLDD in this experiment, the length of gate overlapped lightly doped drain region is 0.75 μm and total lightly doped drain region have seven variable lengths: 0, 0.5, 1, 1.5, 2, 2.5 and 3 μm. In figure 2-3-1 the output characteristics, measured at $V_G = 4\ V$, are shown. As can be noted the output characteristics show that there are a second saturation of the drain current for $10\ V < V_D < 15\ V$. The second saturation of the drain current previously was discussed [27], and they used two subtransistors model to simulate the output characteristics of the GOLDD TFT. In figure 2-3-2 (a) and (b) show that the transconductance G_M of the GOLDD TFT and the two peak were observed at $V_D = 9\ V$. In the same way, we also can observe the second saturation of drain current in output resistance, as shown in figure 2-3-3 (a) and (b). In figure 2-3-4 (a) and (b), the length of LDD region would affect the transconductance G_M. For both channel length L = 6 μm and 12 μm, the transconductance G_M decreased with increasing LDD length.

2-4. Characteristics of device with SALDD structure

In this paper, the structure of device that was used to develop TFT model with LDD structure which is self align lightly doped drain structure. First, we introduce the characteristics of TFT with SALDD structure. In figure 2-4-1 (a) and (b), the effect of LDD length and channel length was shown. We found that the transconductance G_M would trend to a same value with increasing drain voltage, as shown in figure 2-4-1 (b). The output characteristics of drain were shown in figure 2-4-2 (a), and we observed the effect of grain barrier height dependent on temperature, as shown in figure 2-4-2 (b).

2-5. Comparison between self-aligned devices and GOLDD devices

After briefly introducing, the characteristics of TFT with SALDD and GOLDD were obviously compared. The GOLDD architecture is more effective in reducing the electrical field of drain region and second saturation of drain current only was observed in GOLDD structure. Therefore, we can understand that the parasitic transistor in gate overlap region can suppress drain field and induce the second saturation. However, the process of GOLDD structure is more complicated than SALDD structure. In order to simplify the analysis of electrical field, we adopted the SALDD structure in this paper. In chapter 3, the LDD model was developed based on SALDD TFT.

Chapter 3

Poly-Silicon Model for LDD Structure

3-1. Above-Threshold Model

3-1-1. Equivalent Circuit of Polysilicon Thin Film Transistor with LDD Structure

For devices with LDD structure, the lightly doped regions give rise to large series resistance. The lateral voltage drop across the inversion channel region is therefore not the external drain to source voltage drop (represents by V_D when the source is connected to ground) anymore. As a result, the device output characteristics should be modified with this parasitic resistance influence in the LDD regions. By taking into account that the devices are fabricated by a self-aligned process, the source and drain side LDD regions should be almost identical. Therefore, in this proposed model, the source side parasitic resistance and the drain side parasitic resistance are of the same value R_p. From the equivalent circuit as shown in Figure 3-1-1, the internal bias condition across the inversion channel region (e.g., V_{ds} and V_{gs}) can be express as

$$V_{ds} = V_D - 2R_P I_D \tag{3-1-1}$$

$$V_{gs} = V_G - R_P I_D \tag{3-1-2}$$

Therefore, the linear region drain current (I_{lin}) can be modified as:

$$I_{lin} = \frac{W}{L}\mu_{FET}C_{ox}\left[(V_{GT} - I_D R_P)(V_D - 2I_D R_P) - \frac{1}{2}(V_D - 2I_D R_P)^2\right] \tag{3-1-3}$$

where $\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu_1(\frac{2qV_{GT}}{\eta kT})^{m_\mu}}$ is the empirical mobility model considering the gate voltage dependence on effective mobility [28]. μ_1, η and m_μ are fitting

parameters. μ_0 is the intrinsic mobility under high gate bias when the grain barrier no longer influences the carrier transport. The deviation of μ_{FET} from μ_0 mostly occur when gate voltage is smaller than 10 V and the deviation is about 10~20%.

After expansion of Eq. (3), the linear region drain current can be rewritten as

$$I_{lin} = \frac{\frac{W}{L}\mu_{FET}C_{ox}(V_G - V_T - \frac{1}{2}V_D)\cdot V_D}{1+\frac{W}{L}\mu_{FET}C_{ox}(V_G - V_T - \frac{1}{2}V_D)\cdot 2R_P} \quad (3\text{-}1\text{-}4)$$

The output current in saturation region (I_{sat}) should take into account the velocity saturation effect and also the channel length modulation effect. According to the simple velocity saturation model proposed by M. Shur [28] for MOSFET devices, the saturation current can be express as:

$$I_{sat} = \frac{\frac{W}{L}\mu_{FET}C_{ox}(V_G - V_T)^2(1+\lambda V_D)}{1+\frac{W}{L}\mu_{FET}C_{ox}R_P(V_G - V_T)+\sqrt{1+2\frac{W}{L}\mu_{FET}C_{ox}R_P(V_G - V_T)+\left(\frac{V_G - V_T}{V_L}\right)^2}} \quad (3\text{-}1\text{-}5)$$

Here, V_{sat} is the saturation voltage. $V_L = F_sL$, where F_s is the saturation field and L is the channel length. λ is the fitting parameter that represents the channel length modulation effect.

After the saturation current was decided, V_{sat} can be defined by

$$V_{sat} = V_G - V_T - V_L\left[\sqrt{1+\left(\frac{V_G - V_T}{V_L}\right)^2} - 1\right] + 2R_P I_{sat} \quad (3\text{-}1\text{-}6)$$

The total drain current is therefore can be written as

$$I_{DS} = \frac{\frac{W}{L}\mu_{FET}C_{ox}(V_G - V_T - \frac{1}{2}V_{DSE})\cdot V_{DSE}(1+\lambda V_D)}{1+\frac{W}{L}\mu_{FET}C_{ox}(V_G - V_T - \frac{1}{2}V_{DSE})\cdot 2R_P} \quad (3\text{-}1\text{-}7)$$

with

$$V_{DSE} = \frac{V_D}{\left[1+\left(\frac{V_D}{V_{sat}}\right)^{m_{ss}}\right]^{\frac{1}{m_{ss}}}} \quad (3\text{-}1\text{-}8)$$

where m_{ss} is a parameter that determines the shape of the characteristics in the knee region.

Then, the channel length modulation coefficient λ can be defined by comparing saturation current I_{sat} with measured one. After calculating the corresponding saturation voltage V_{sat}, the total output drain current is obtained. Figure 3-1-2 (a) and 3-1-2 (b) depict the calculated results and the measured results for devices with different LDD length (LDD length = 1μm and 3 μm, respectively). Good agreements are found when comparing these two results. The related parameters are listed in Table II. Figure 3-1-3 (a) and 3-1-3 (b) compares the calculated and the measured conductance G_D and ON resistance R_{ON}, respectively. It is found that the parameters related to kink effect can be defined more accurately by comparing the calculated R_{ON} and the measured one as shown in figure 3-1-3 (b). The results are listed in Table III for devices with different LDD length.

Finally, the kink effect was considered by adding

$$I_{kink} = \left(\frac{L_{kink}}{L}\right)^{m_{kink}} \left(\frac{V_D - V_{DSE}}{V_{kink}}\right) \exp\left(\frac{-V_{kink}}{V_D - V_{DSE}}\right) I_{DS} \quad (3\text{-}1\text{-}8)$$

into Equation 3-1-7 [28, 29], where V_{kink}, L_{kink} and m_{kink} are model parameters. For devices with channel length longer than 6 μm, the kink effect is not a pronounced factor. It should be taken into consideration only when comparing the calculated R_{ON} and the measured one.

Noticeably, the scattering effect is not included in this model. The calculated and

simulated G_M for devices with different channel lengths are depicted in figure 3-1-4 (a) and 3-1-4 (b). It is found that the degradation of G_M under large gate bias is more pronounced for devices with short channel length. This is due to the influence of large parasitic resistance for short-channel devices. It can be concluded that our model reproduces device characteristics very well not only in a large range of bias condition but also for devices with various LDD length and channel length.

3-2. DIBL in LDD region

Although we use simple equivalent circuit to obtain LDD model in 3-1, we can not explain some phenomenon. For example, at high gate voltage and low drain voltage condition, we found that the *I-V* characteristic of device which was operated in linear region is curved. If parasitic resistance is constant, the characteristic of linear region would be straight. Therefore parasitic resistance may be not constant. In 3-2, we try to prove that the value of resistance is variable and dependent on temperature. First, we focus on the measurement of resistant testkey at different temperature. Figure 3-2-1 show that current vs. voltage plots for with W/L = 3 (μm)/3 (μm) and W/L = 6 (μm)/6 (μm). In figure 3-2-1 (a) and (b) show current as a function of voltage at different temperature. We found that the value of resistance would change depend on voltage and temperature. The figure 3-2-2 (a) and (b) show that plot of R_{ON} as a function of voltage for resistance testkeys with W/L = 3 (μm)/3 (μm) and W/L = 6 (μm)/6 (μm). We observed for all devices that R_{ON} decrease with increasing temperature. It is obvious that the grain barrier exists in resistance. We can construct a plot of activation energy at a function of gate voltage, as given in figure 3-2-3 (a) and (b).

Therefore, the resistance equation which includes the grain barrier height model was considered to be defined as:

$$R=R_0 exp\left(\frac{E_B}{kT}\right) \tag{3-2-1}$$

We found E_B that it depends on electrical field, as shown in figure 3-2-4. Hence, E_B can be extracted from that activation energy barrier slope varies with applied voltage in figure 3-2-5. We defined E_B equation as:

$$E_B=E_a-S\frac{V}{LDD} \tag{3-2-2}$$

where E_a is the barrier height at voltage V = 0, S is the slope of the linear regression and LDD is the length of resistance. On the side, when the value of extra voltage V is very high, the value of resistance would be tending towards a constant. Finally, we need an equation to combine the different regions. The effective resistance was calculated according to the following equation:

$$R_{EFF}=R_0 exp\left(\frac{E_a-S\frac{V}{LDD}}{kT}\right)\left[1+\left(\frac{R_{LOW}}{R_0 exp\left(\frac{E_B}{kT}\right)}\right)^3\right]^{1/3} \tag{3-2-3}$$

R_{LOW} was defined as the lowest of resistance value. R is the effective resistance given by the following interpolation function that tends to R in low voltage and to R_{LOW} in high voltage.

In the following, we need the correct voltage which drops across the parasitic resistance in TFT device with LDD structure. Because the value of drain current which passes LDD region and channel region is same, we use equation (3-2-3) and MOSFET current equation to deduce the value of voltage in the LDD region. The figure 3-2-6 shows that voltage in LDD region dependent on drain voltage. The variation of parasitic resistance dependent on drain voltage was showed in the figure 3-2-7.

$$\frac{V}{R_0 exp\left(\frac{E_a - S\frac{V}{LDD}}{kT}\right)} * \left[1 + \left(\frac{R_{LOW}}{R_0 exp\left(\frac{E_a - S\frac{V}{LDD}}{kT}\right)}\right)^3\right]^{-1/3} - \frac{W}{L} * \mu_{FET} * \left[(V_G - V_T - V)(V_D - 2V) - \frac{1}{2}(V_D - 2V)^2\right] = 0$$

(3-2-4)

Resistance R is replaced by R_{EFF} (3-2-3) in equation (3-1-4).

$$I = \frac{\frac{W}{L}\mu_{FET} C_{OX}\left(V_G - V_T - \frac{1}{2}V_D\right)V_D}{\frac{W}{L}\mu_{FET} C_{OX}\left(V_G - V_T - \frac{1}{2}V_D\right) * 2R_0 exp\left(\frac{E_B}{kT}\right) * \left[1 + \left(\frac{R_{LOW}}{R_0 exp\left(\frac{E_B}{kT}\right)}\right)^3\right]^{1/3} + 1} \quad (3\text{-}2\text{-}5)$$

The results were shown in figure 3-2-8 (a) and (b). We can observe that the characteristics of linear region match measured data. Therefore, we prove that the value of parasitic resistance is variable and depends on the voltage and temperature.

3-3. Grain Barrier Height Model

Equation (3-3-1) is the well-know grain boundary barrier height model proposed firstly by Seto et al.[13]. E_B represents the grain boundary barrier energy in above-threshold region. N_T represents the effective grain boundary trap density and n is the gate-induced carrier density. When there is no other temperature-sensitive mechanism, the measured activation energy could be served as the grain boundary energy barrier.

$$E_B = \frac{qN_T^2}{8\varepsilon n} \quad (3\text{-}3\text{-}1)$$

In our experiment, the measured activation energy versus bias drain voltage is plotted

in figure 3-3-1. When drain voltage is high, it has been proposed that the drain-induced grain barrier lowering (DIGBL) effect would influence carrier transport seriously [30, 31, 32]. When the device is operated in the linear region and the drain voltage is low, the barrier increases with increasing drain voltage. This can be explained by the influence of drain bias on the surface potential along the channel. The average carrier density is therefore expressed as:

$$n=\frac{C_{ox}\left(V_G-V_{fb}-\alpha V_D\right)}{qt_{ch}} \tag{3-3-2}$$

where C_{ox} is capacitance per unit area, V_{fb} is the flatband voltage, and α is a parameter indicating the influence of drain voltage. t_{ch} is the channel thickness. According to the grain boundary barrier height given by Ref. [33], the barrier height considering the influence of the drain voltage and the DIGBL effect is given by

$$E_B=\frac{t_{ch}[(qN_T)^2-4qN_T\varepsilon_s\eta\frac{V_D}{L}]}{8\varepsilon_s C_{ox}(V_G-V_T-\alpha V_{DSe})} \tag{3-3-3}$$

For MOSFET devices, the channel thickness is reversely proportional to the gate bias and can be expressed as:

$$t_{ch}=8\frac{V_{th}}{V_G-V_T}t_{ox}\sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}}} \tag{3-3-4}$$

where t_{ox} is the oxide thickness and V_{th} is thermal voltage. However, in poly-Si TFTs, the channel thickness would be further affected by the screening effect of trapped charges. So we modified the channel thickness as:

$$t_{ch}=8\left(\frac{V_{th}}{V_G-V_t}\right)^{\gamma-1}t_{ox}\sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}}} \tag{3-3-5}$$

where γ is the parameter that represents the trapped charge screening effect. Finally,

grain barrier height model of polysilicon TFT is expressed as:

$$E_B = \frac{t_{ox}\left(q^2 N_T{}^2 - 4qN_T\varepsilon_s\eta\frac{V_D}{L}\right)V_{th}{}^{\gamma-1}}{\sqrt{\varepsilon_{ox}\varepsilon_s}\,C_{ox}\left(V_G - V_T - \alpha V_{DSe}\right)^{\gamma}} \qquad (3\text{-}3\text{-}6)$$

Parameter extraction:

***γ, V_T, N_T* extraction:** using long channel length device (ex. L = 30 *um*). Under small V_D bias. Firstly, γ can be defined by best fitting of the E_B vs. V_G curve as in figure 3-3-2 (a) and figure 3-3-2 (b). It is found that γ is closer to 2 when the film property is better. This prove the above screening effect mechanism. Table IV lists values of γ for different grain growth conditions. Then the plot of $E_B{}^{-1/\gamma}$ vs. V_G is shown in figure 3-3-3. The V_T and N_T can be extracted from the x-axis intersection and the slope of the curve. Figure 3-3-4 (a) shows that the line merges at x-axis. The value of x-axis is defined as threshold voltage V_T.

***α,η* extraction:** By increasing V_D bias, the x-axis intersection of the $E_B{}^{-1/\gamma}$ vs. V_G curve will shift to larger x value. This relationship gives the α value. As seen in figure 3-3-4 (b) the value which merges at x-axis is defined as α. After the determination of γ, V_T, N_T and α, η can be obtained by calculation from the experimental data. The related parameters are listed in Table *IV*.

After defining the grain boundary barrier height model, the mobility model can be defined as $\frac{1}{\mu_{FET}} \equiv \frac{1}{\mu_G} + \frac{1}{\mu_0 \exp\left(\frac{-E_B}{kT}\right)}$ (3-3-7)

μ_0 represents the intrinsic mobility in the grain region; μ_G stands for the influence of scattering effect on mobility under large gate voltage. As temperature increases, the field effect mobility μ_{FET} increases without incorporating other empirical equations.

Finally, we combine the proposed mobility model in equation (3-3-7) into the *I-V* model in equation (3-1-7). The calculated results and the measured results for devices

with different LDD lengths are depicted in figure 3-3-5 (a) and figure 3-3-5 (b). Good agreement is found in figure 3-3-5 (a), which verifies our proposed model. Some under-estimation is observed in figure 3-3-5 (b). This is due to the voltage dependence of LDD resistance that need to be further studied in our future work.

Chapter 4

Conclusion

The Poly-Si TFT model with self-align LDD was successfully developed and the parameters of parasitic resistance and grain barrier height were extracted from characteristics of devices. The results would be obtained and discussed as follows:

4-1. Parameters of parasitic resistance in device

We used the characteristic of TFT device which was operated at linear region to extracting the parasitic resistance value. In order to ignore the effect of drain voltage, we needed a large gate voltage. However, excessive gate voltage would cause the decreasing of parasitic resistance and damage the gate oxide interface. The range of gate voltage has to carefully be determined. In different devices, we have different range of gate voltage to extract the parasitic resistance. On the side, the resistance was extracted from low drain voltage which can not represent correct at any drain voltage.

4-2. LDD model of TFT device

First we tried to use the present mobility model to combine our model. But present mobility model can not dependent on gate voltage very well. Therefore we adopted the empirical mobility model to fit the real mobility. In 3-1 section, we can saw that the empirical mobility model predict correctly the characteristics of TFT device with LDD structure. Next step, the variable resistance was used to simulate the characteristic of TFT with LDD structure. The grain barrier height was observed in resistance testkey and we extracted the E_B from *I-V* plots. Because the resistance model includes exponential term, we can not obtain an analytical solution. The modified LDD model can improve accuracy of linear region. Finally, we consider the

grain barrier which exits in channel region of device. We demonstrated the poly-Si TFT modeling incorporating with the experimentally defined grain barrier height model. It was also found that bias condition and film property had influences on grain barrier and therefore strongly affected the device characteristics. When comparing the experimental results and the simulated results, good agreements were found for devices with different channel length and LDD lengths.

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Table 3-1

Extracted R_P and l_0 for devices with different LDD lengths

LDD	*0 μm*	*1 μm*	*2 μm*	*3 μm*
R_P *(ohm)*	1000	2500	16000	32000
L_0*(μm)*	2.5	0.5	-1	-1.5

Table 3-2

Key parameters extracted for the proposed model

Parameter	Definition	Units	Value
μ_0	High field long-channel zero-bias mobility	cm^2/Vs	150
V_t	Long-channel zero-bias threshold voltage	V	1.7
m_{ss}	V_{dse} transition parameter		4
μ_1	Low field mobility	cm^2/Vs	15
m_μ	Low field mobility exponent		1.4
η	Zero-bias ideality factor		7
$v_s = \mu_0 F_s$	Saturation velocity	cm/s	1.5×10^6

Table 3-3

Parameters related to kink effect for devices with different LDD lengths

LDD	1 μm	2 μm	3 μm
L_{kink}	1.5 μm	1.5 μm	1.5 μm
m_{kink}	0.01	0.01	0.1
V_{kink}	11 V	11 V	9V

Table 3-4

Key Parameters of Grain Barrier Model for devices with different film properties

	γ	N_T ($10^{12}cm^{-2}$)	V_T (V)
As-Deposited (plasma=0 Hrs)	1	2.33	5.945
As-Deposited (plasma=2 Hrs)	1	1.95	3
SPC (plasma=0 Hrs)	1.3	1.93	2.98
SPC (plasma=1 Hrs)	1.3	1.89	0.41
SPC (plasma=2 Hrs)	1.3	1.51	0.27
ELA	1.55	0.6	0.26

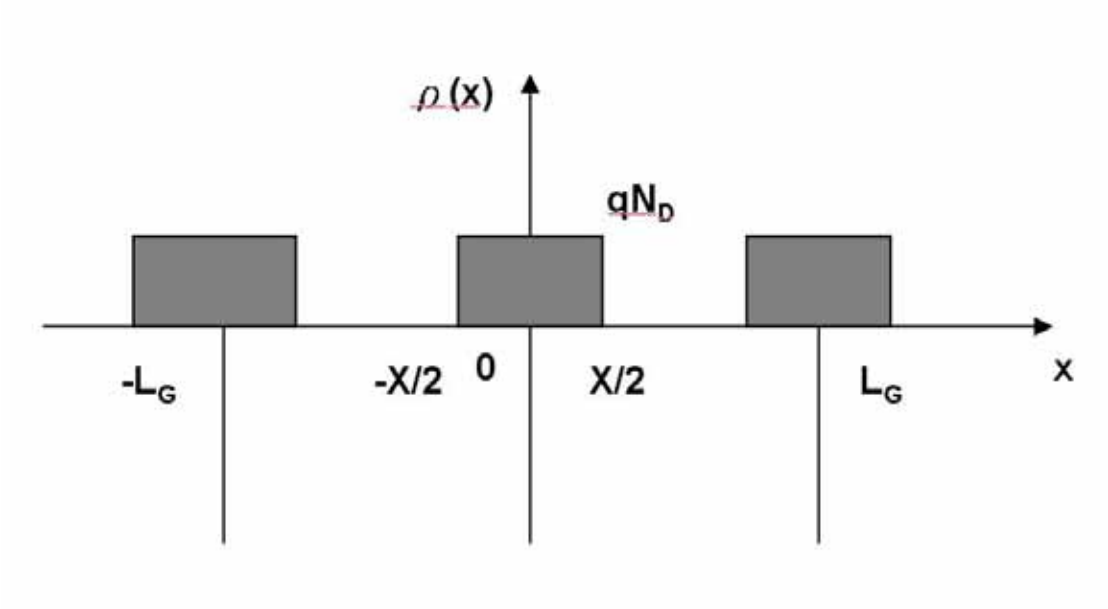


Figure 1-2-1. Simplified distribution of charges within the grain and at grain boundaries. At grain boundaries, the trap state density is defined per surface unit, while N_D is a doping volume concentration.

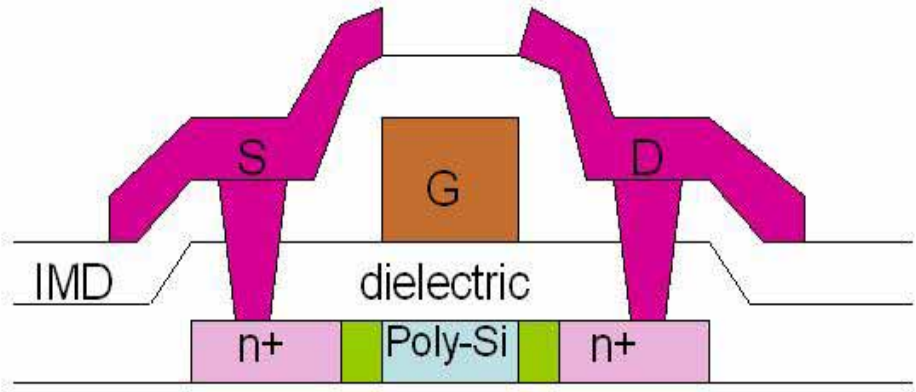


Fig. 2-1-1.Polysilicon TFT device structure

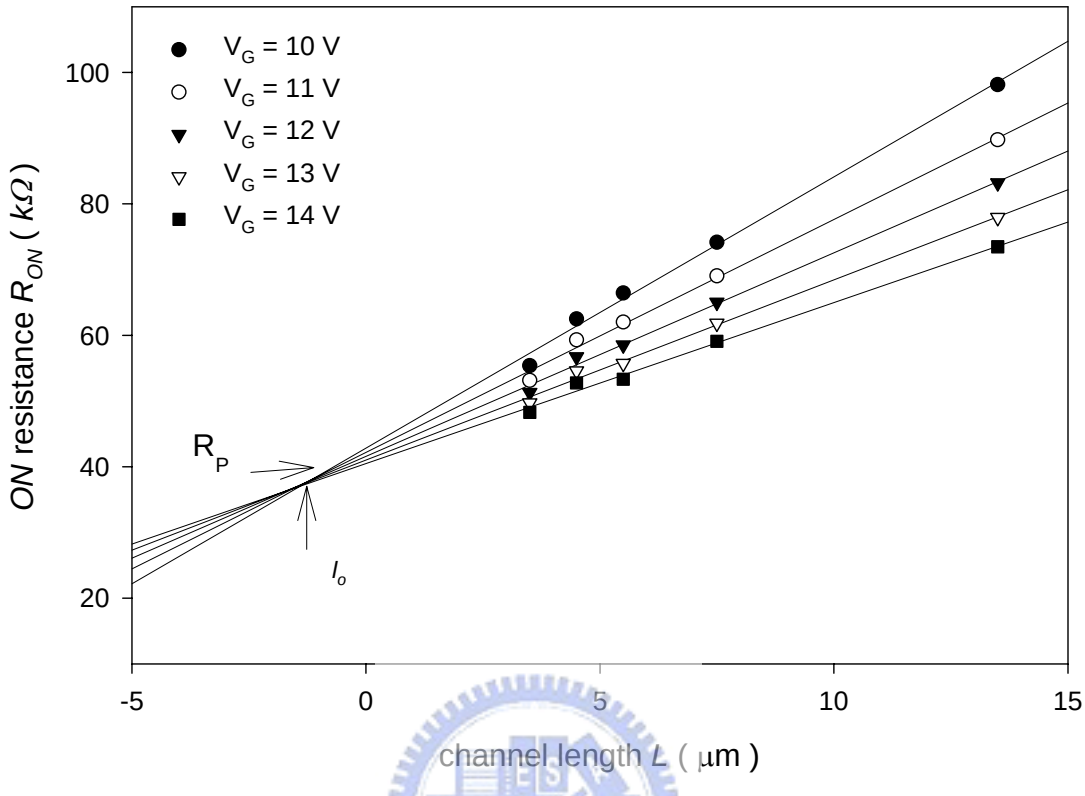


Fig. 2-2-1.*ON* resistance as a function of channel length at different gate voltages

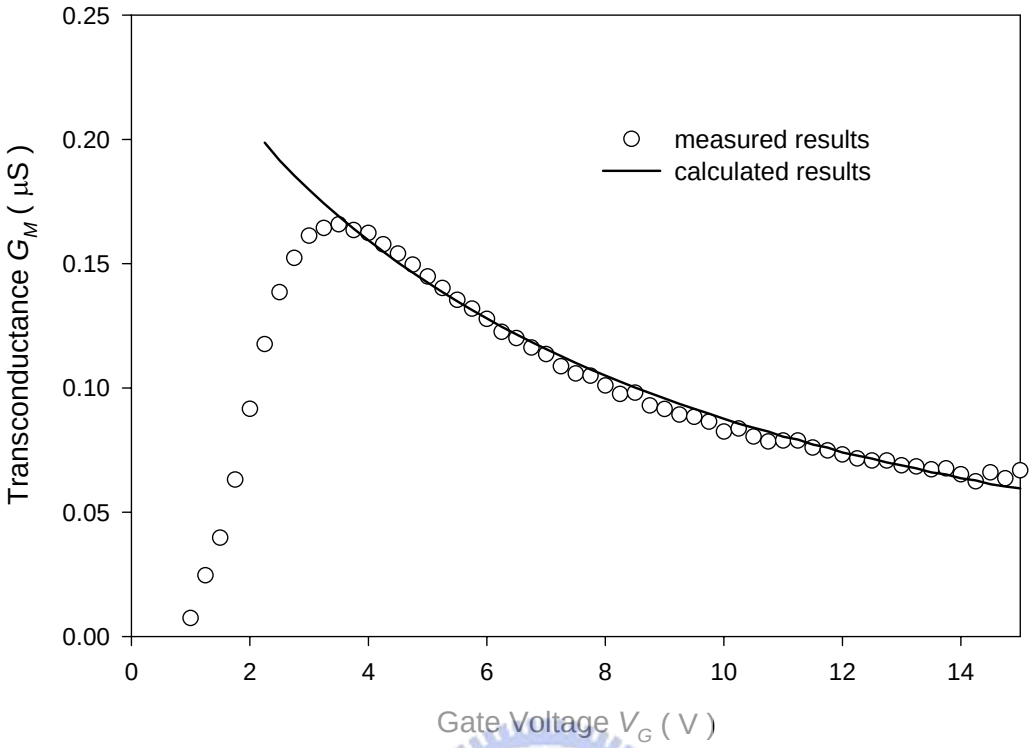
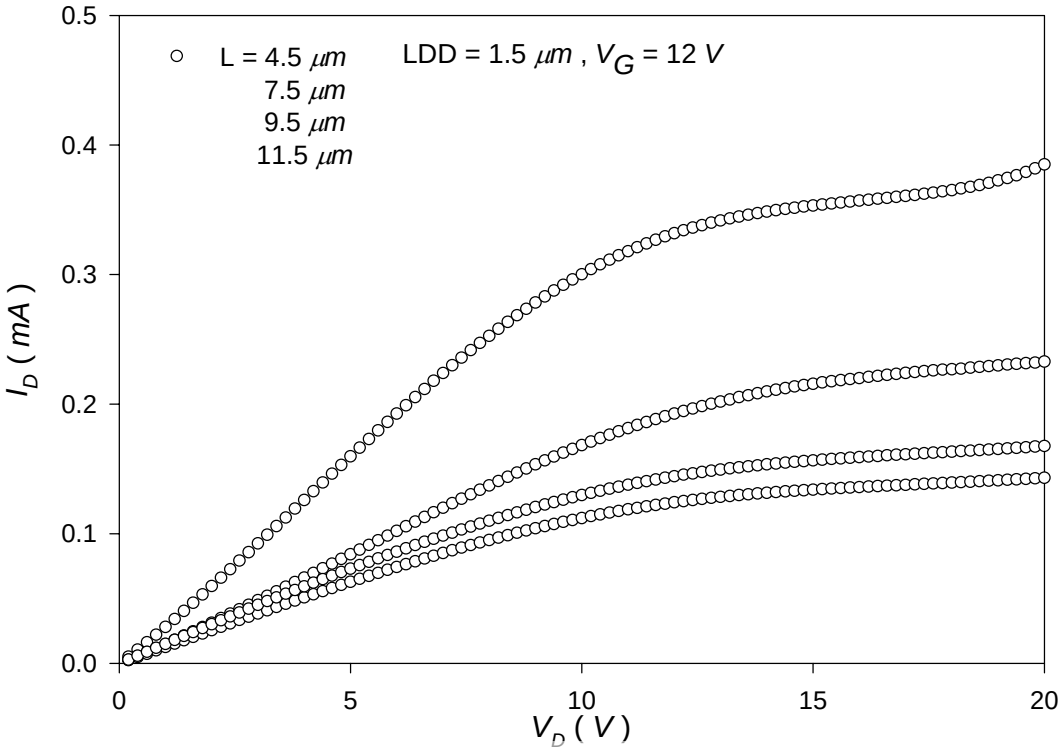
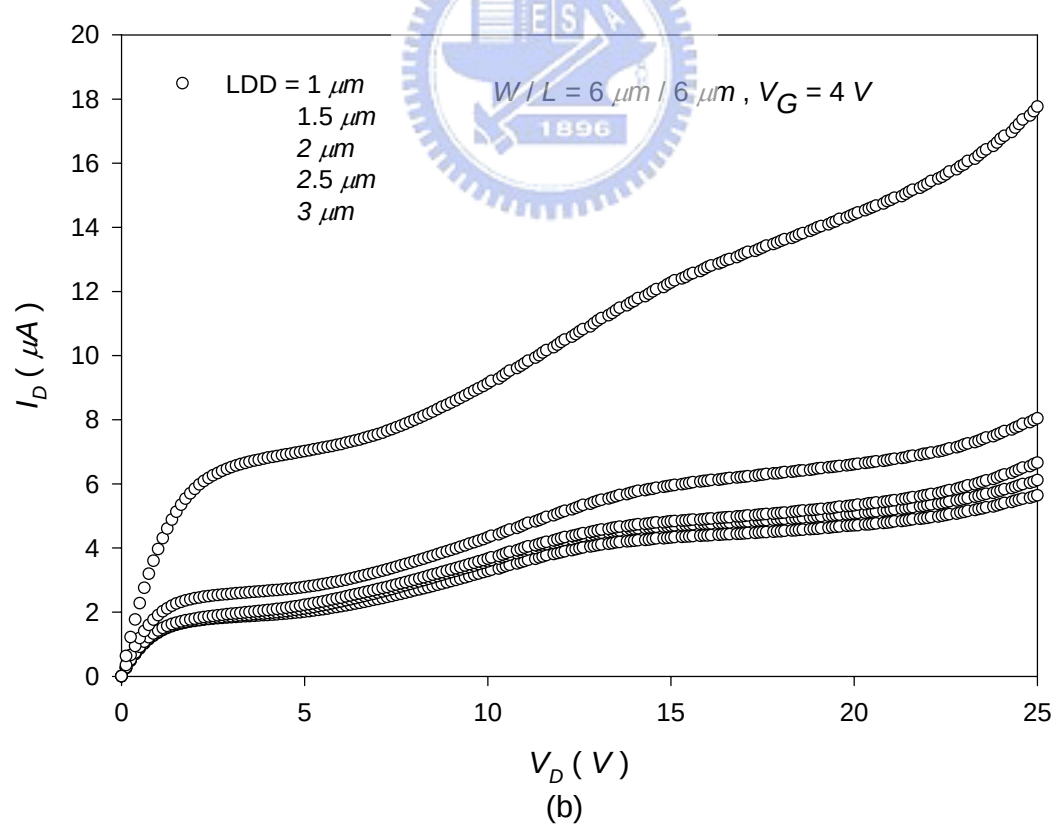


Fig. 2-2-2 the comparison of calculated and measured transconductance. W / L = 6 μm / 13.5 μm, LDD length = 3 μm, and V_D = 0.1 V.



(a)



(b)

Fig. 2-3-1 (a) and (b) we found that second saturation of drain current at $V_G = 4\ V$

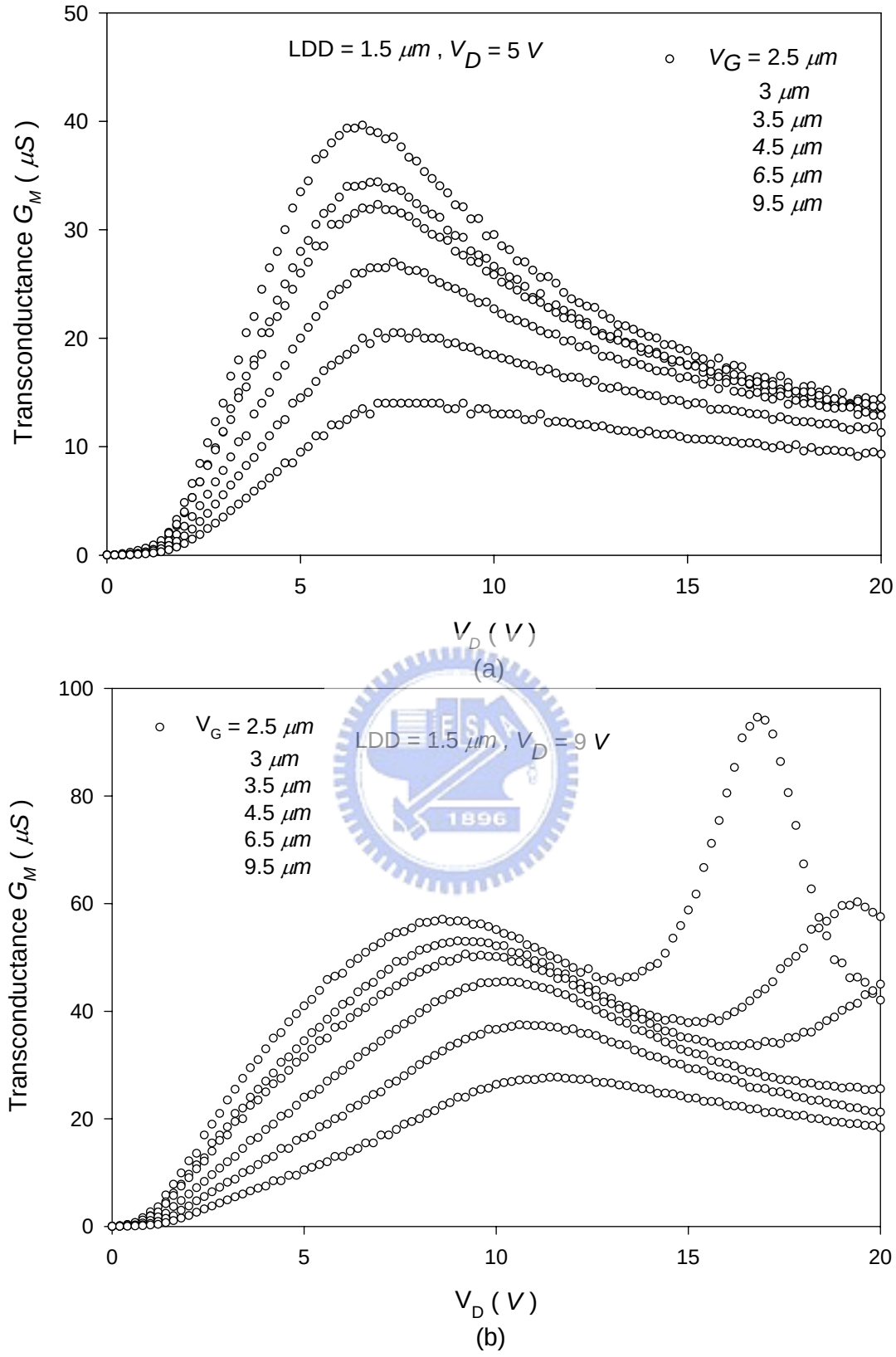


Fig. 2-3-2 show that the transconductance G_M of the GOLDD TFT and the two peak were observed at V_D = 9 V.

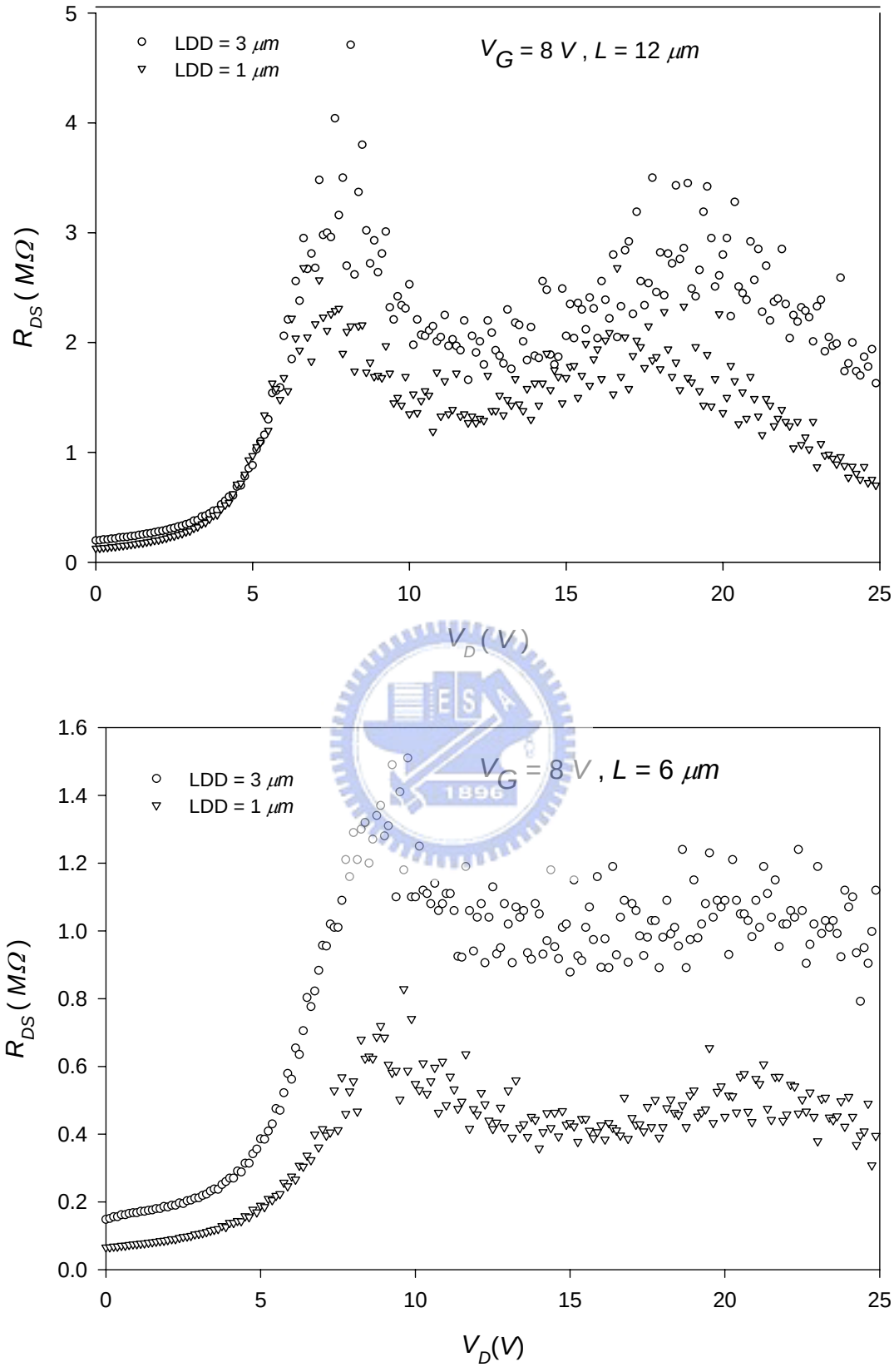


Fig. 2-3-3 we can observe the second saturation of drain current in output resistance

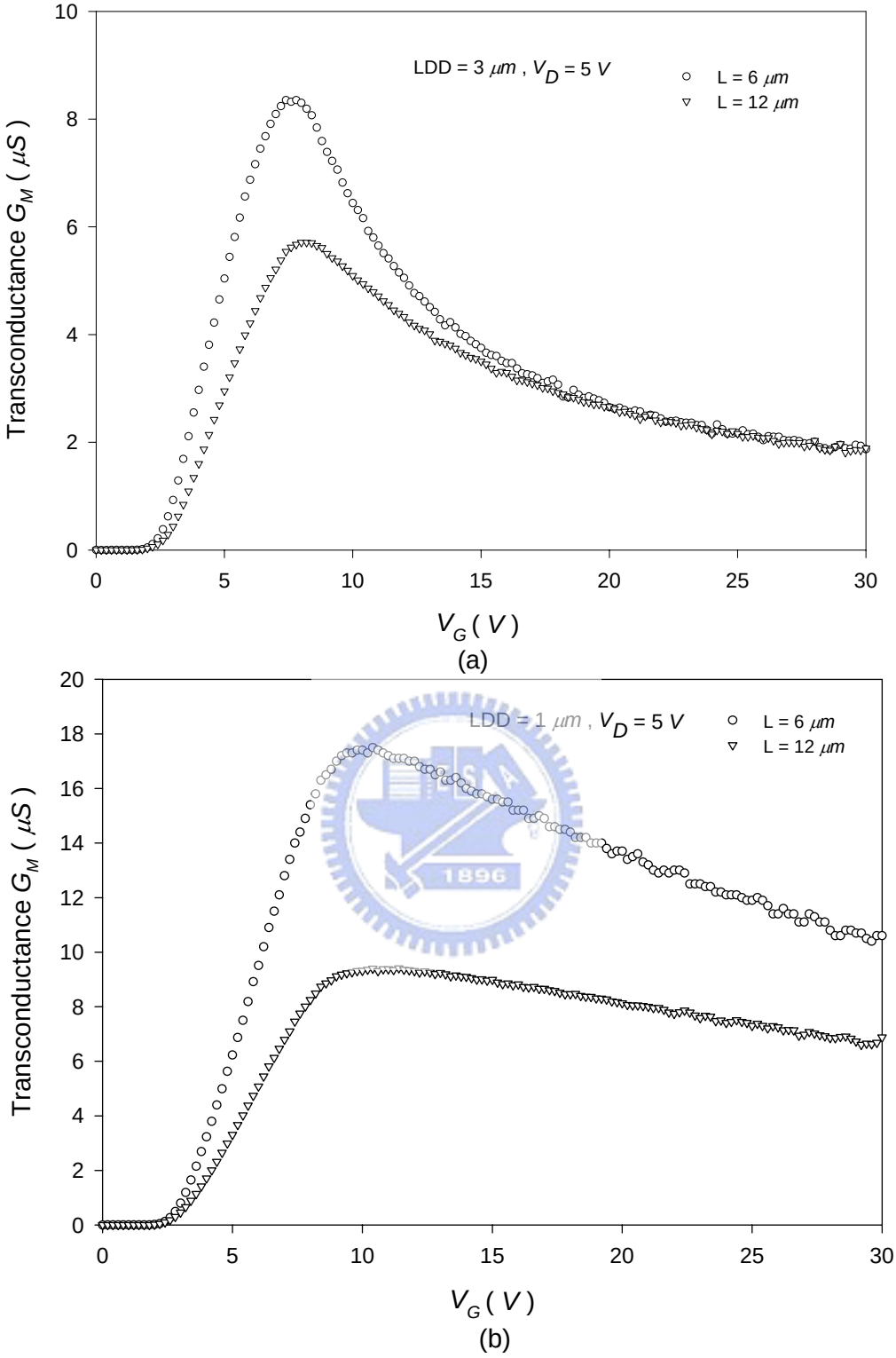


Fig. 2-3-4

the length of LDD region would affect the transconductance G_M. For both channel length L = 6 μm and 12 μm, the transconductance G_M decreased with increasing LDD length

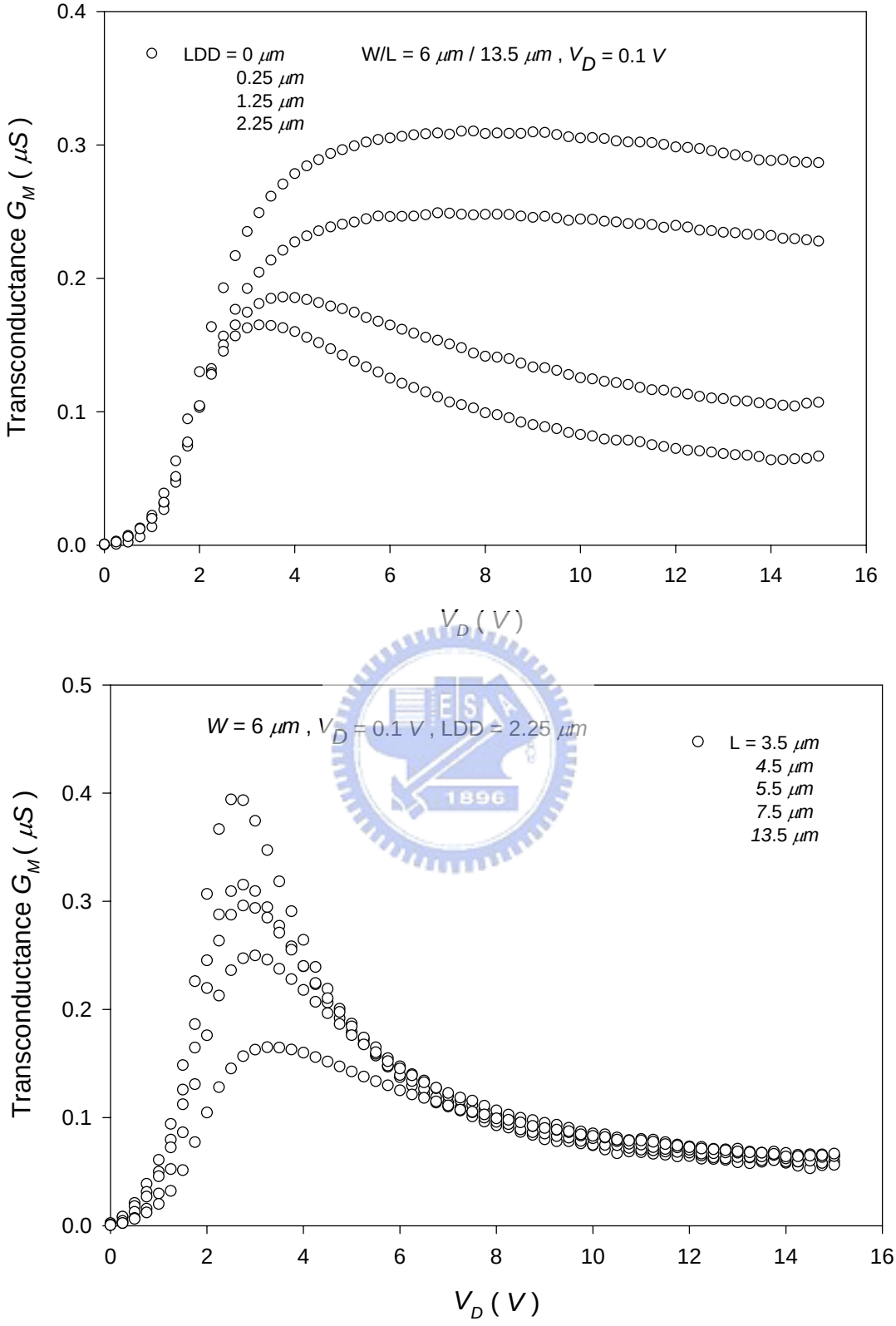


Fig. 2-4-1 the effect of LDD length and channel length was shown

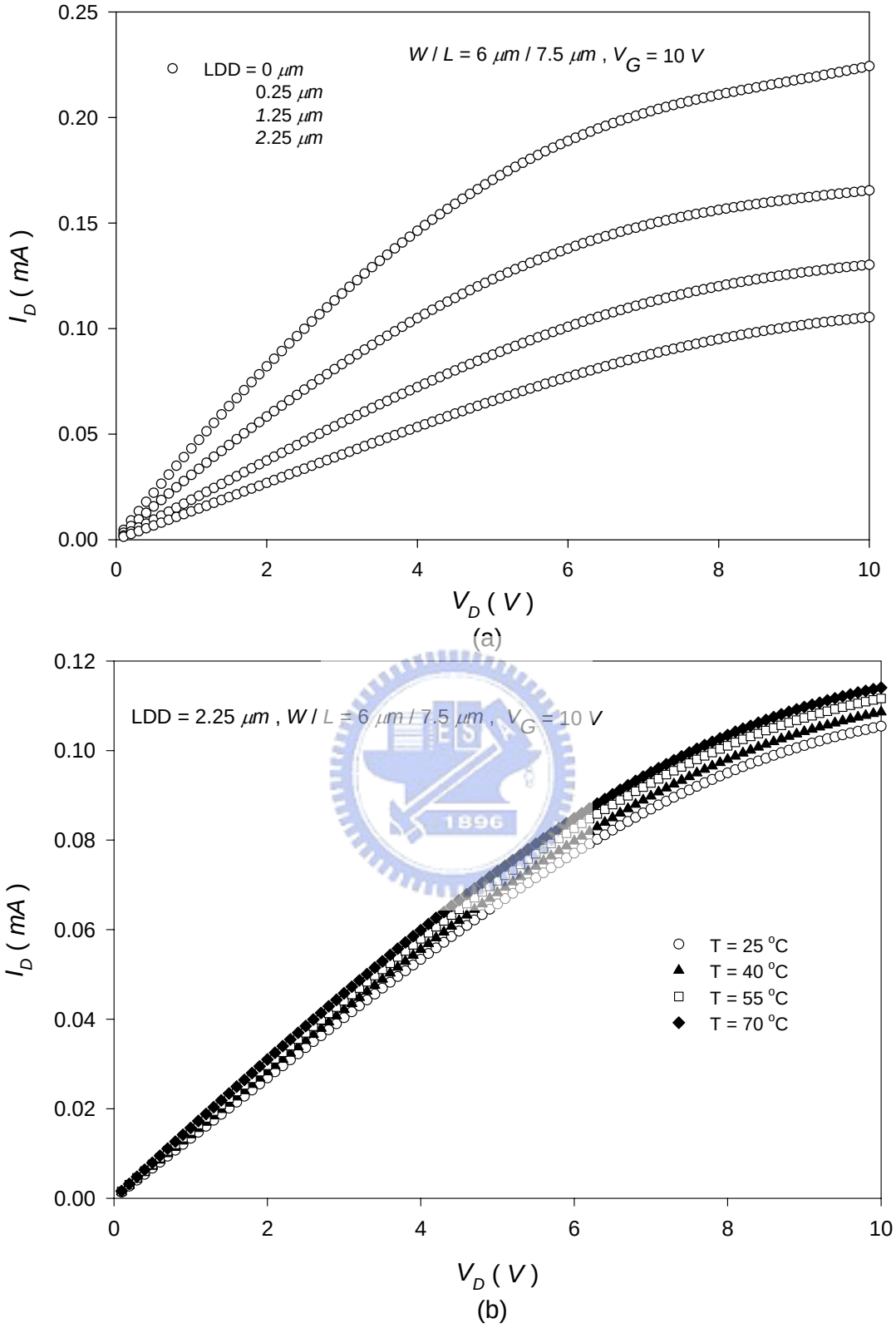


Fig. 2-4-2 (a) show that the I-V curve of drain current with different LDD length and (b) show that drain current increases with increasing temperature.

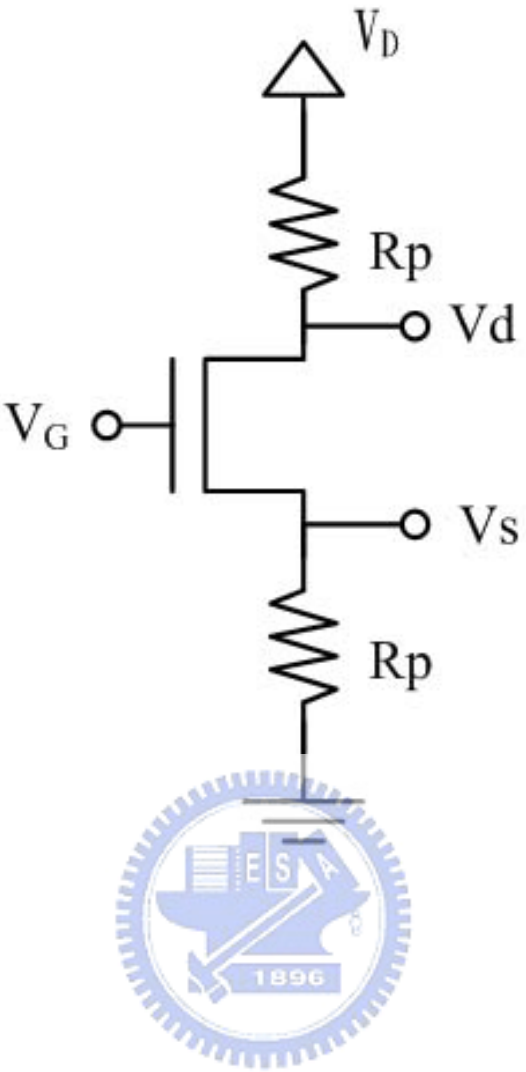
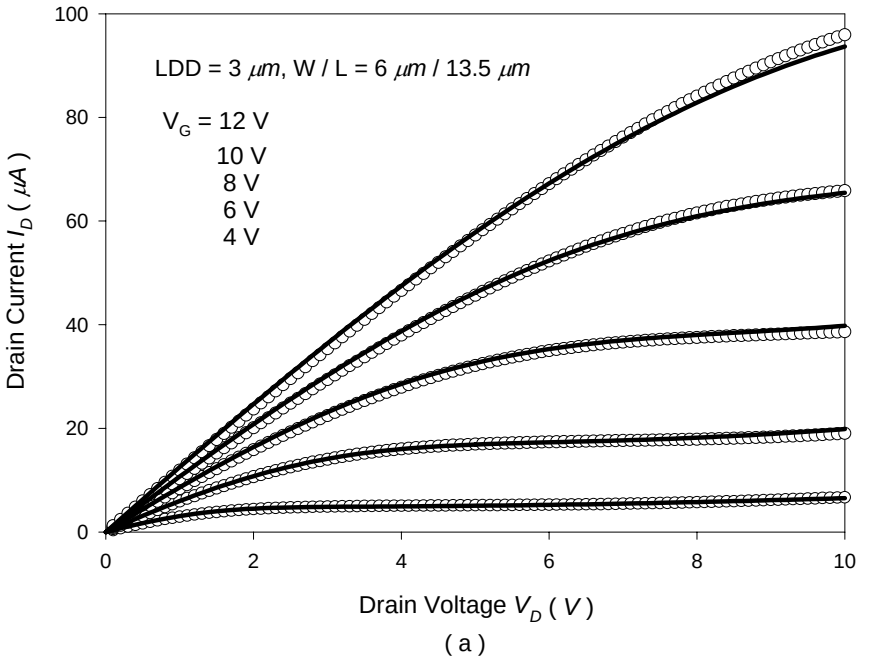
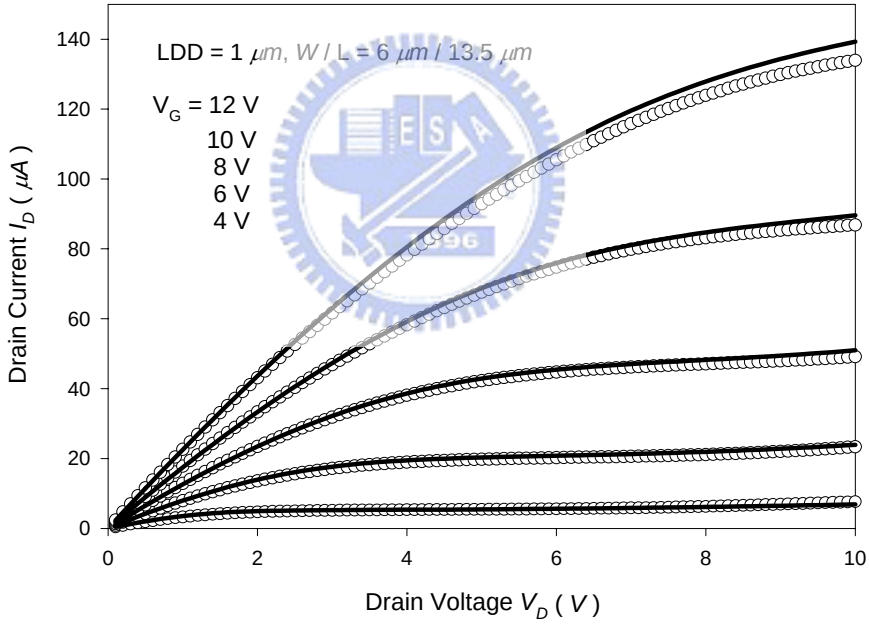


Fig.3-1-1 equivalent circuit

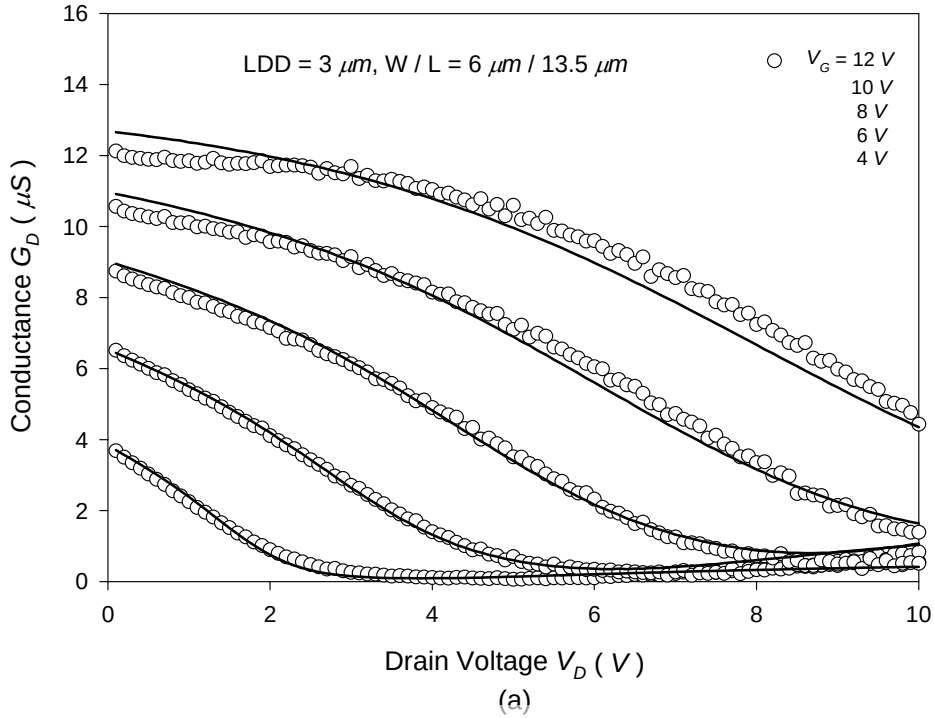


(a)



(b)

Fig.3-1-2 Above-threshold experimental (symbols) and simulated (solid line) *I-V* characteristics for poly-Si TFTs with different LDD lengths



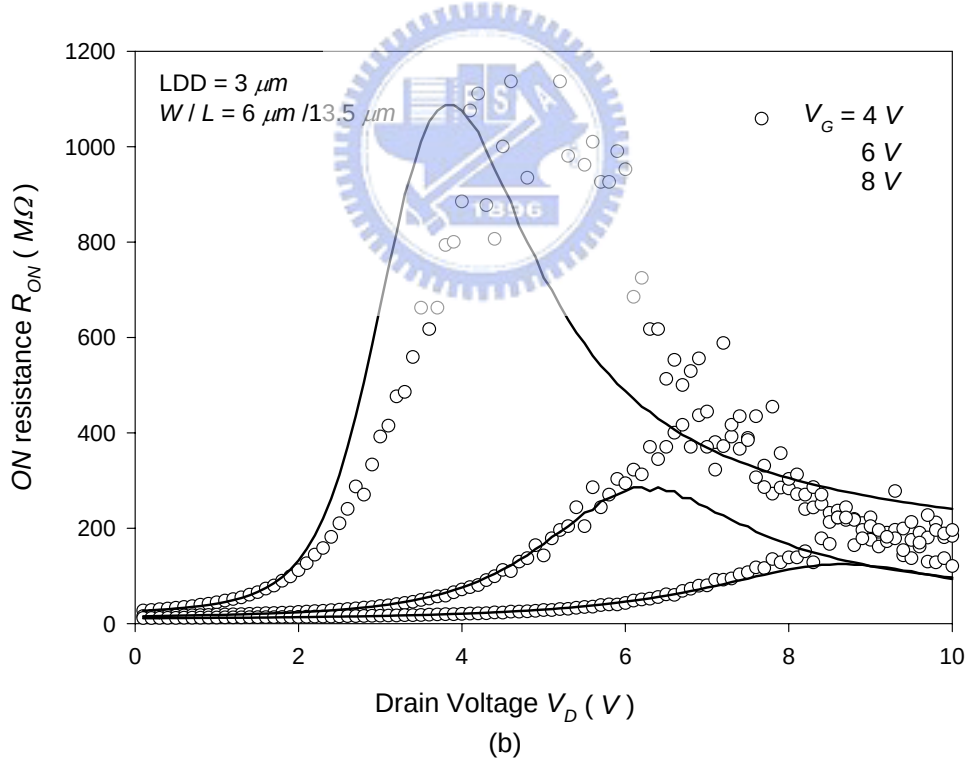
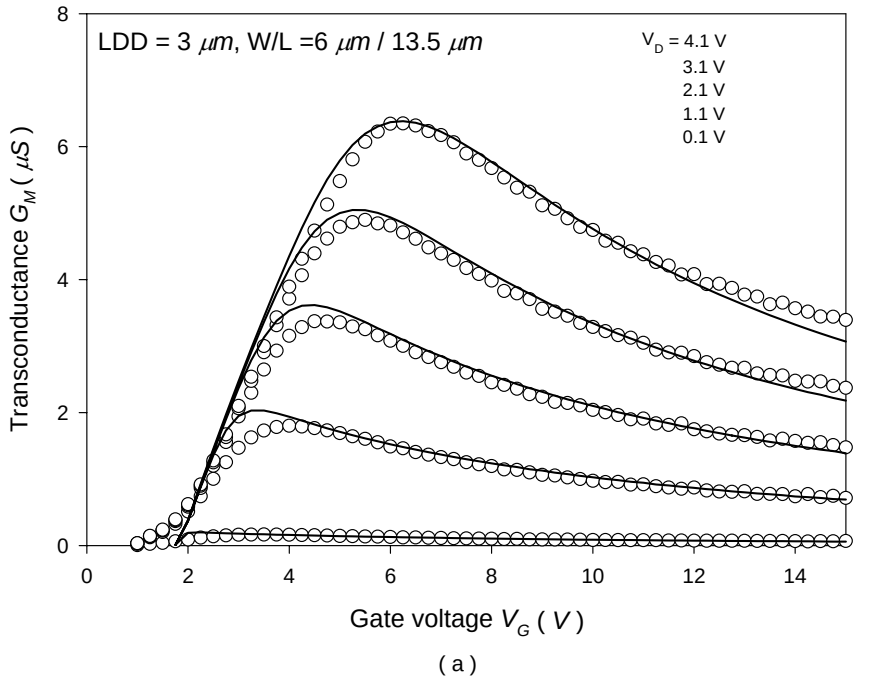
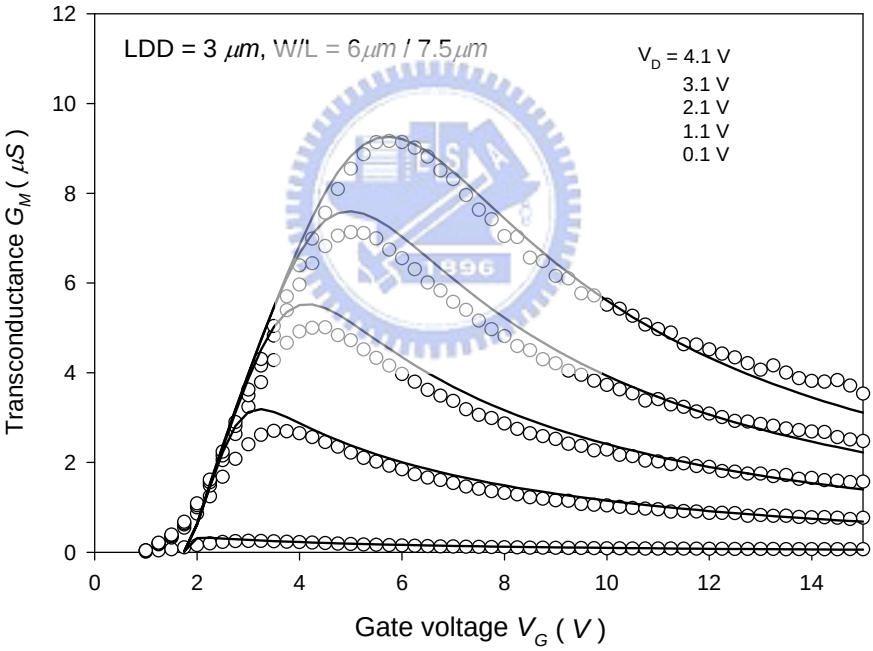


Fig.3-1-3 The calculated and measured conductance G_D and ON resistance R_{ON}.



(a)



(b)

Fig.3-1-4 Above-threshold experimental (symbols) and calculated (solid) transconductance of LDD-TFTs with different channel length.

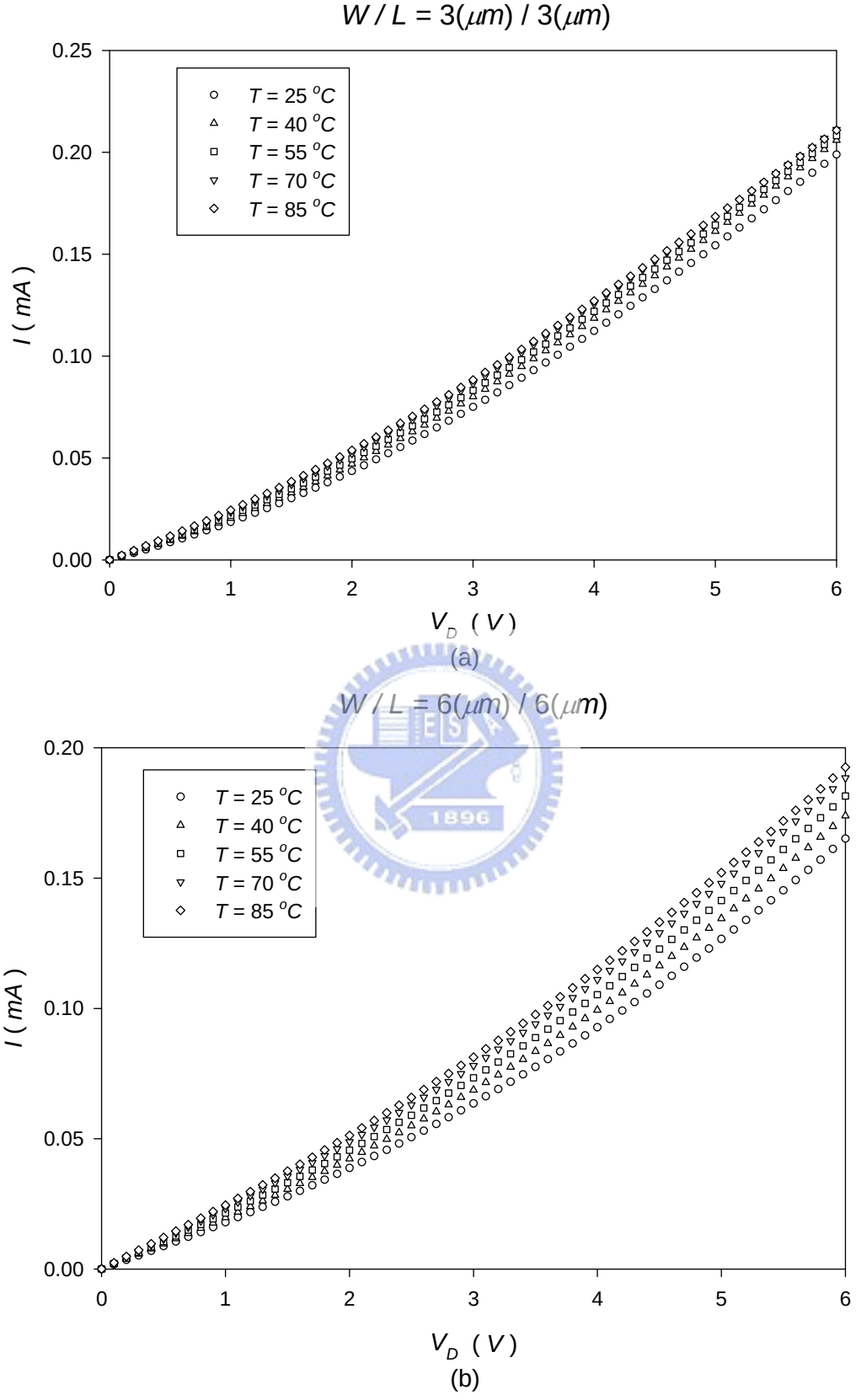


Fig.3-2-1 (a) and (b) show that drain current increase with increasing temperature

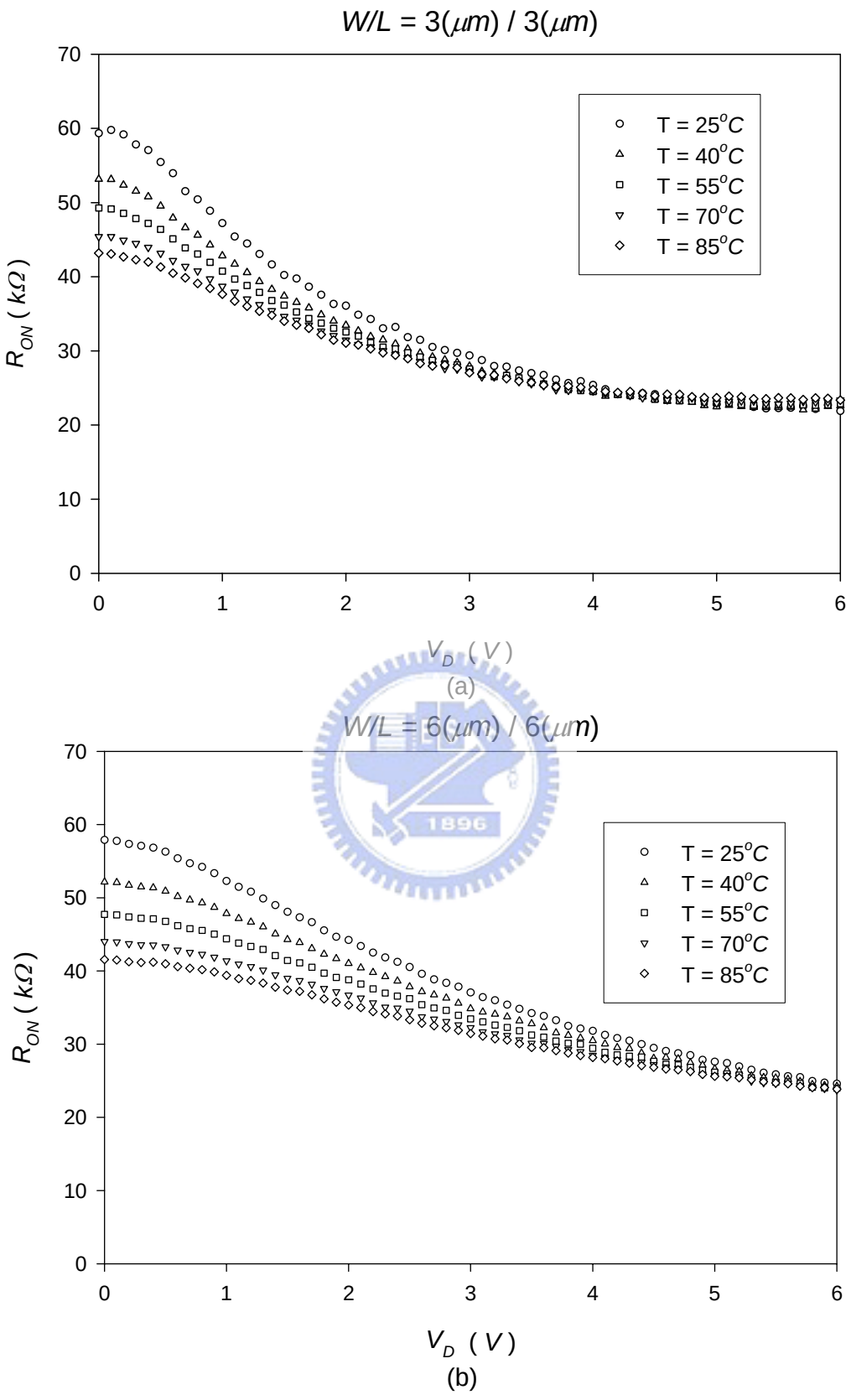


Fig.3-2-2 (a) and (b) show that *ON* resistance increase with increasing temperature

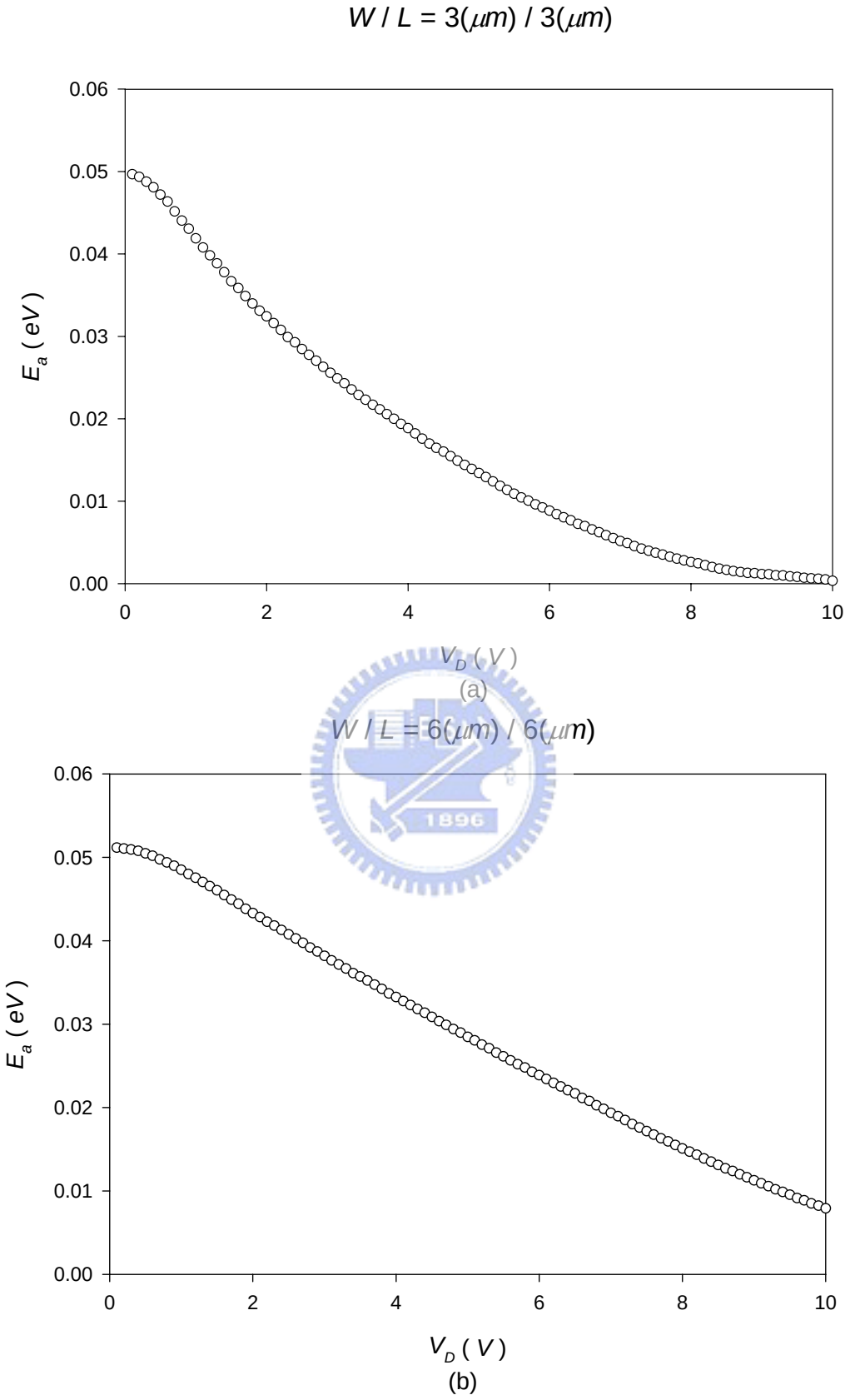


Fig.3-2-3 the barrier height can be extracted from *I-V* at different temperature

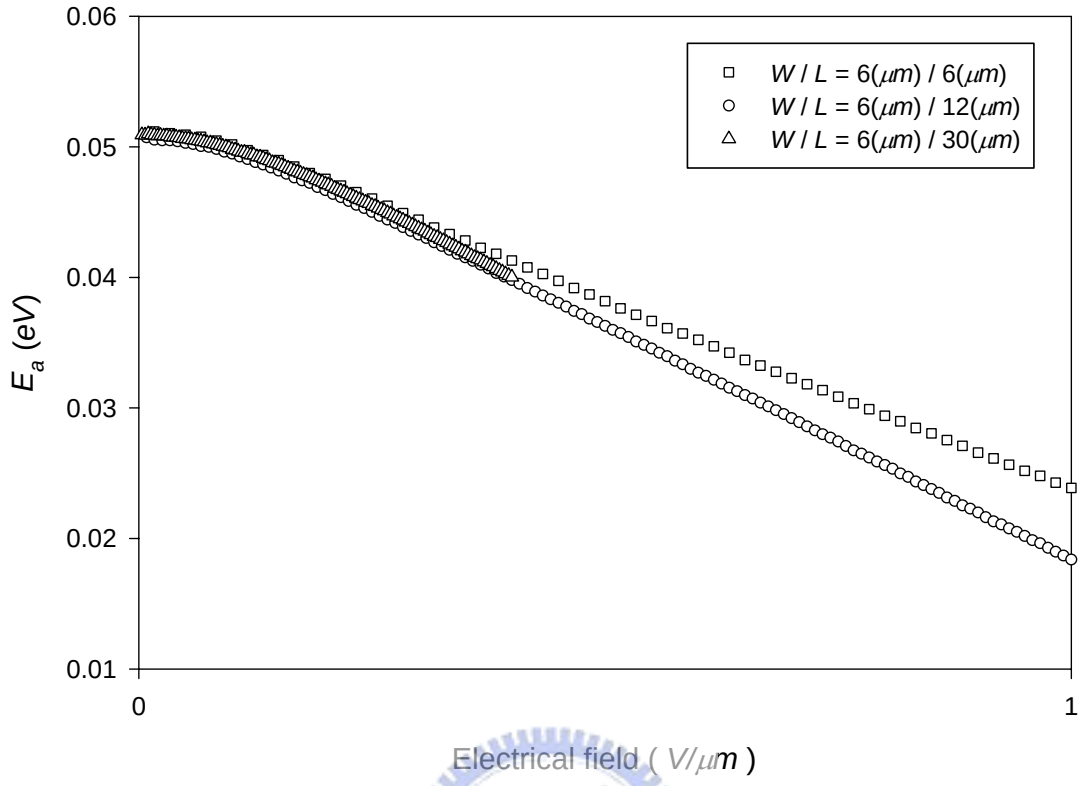


Fig. 3-2-4 the barrier height dependents on electrical field

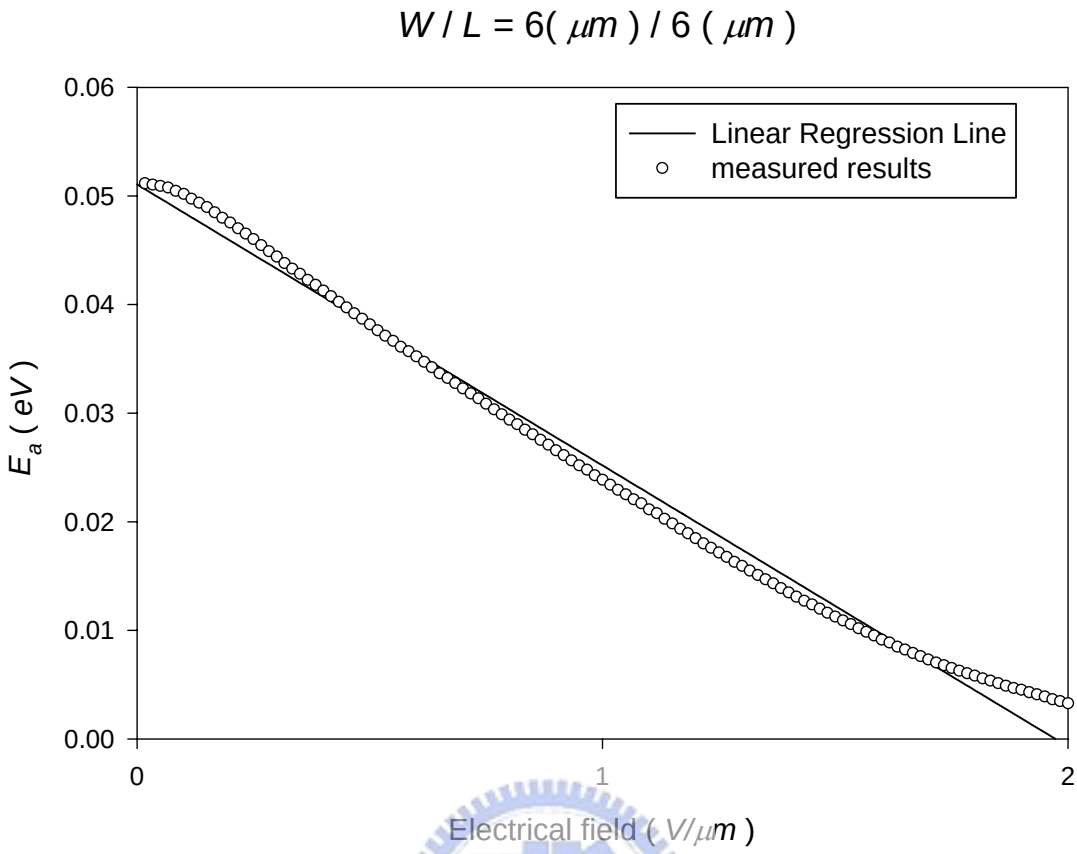
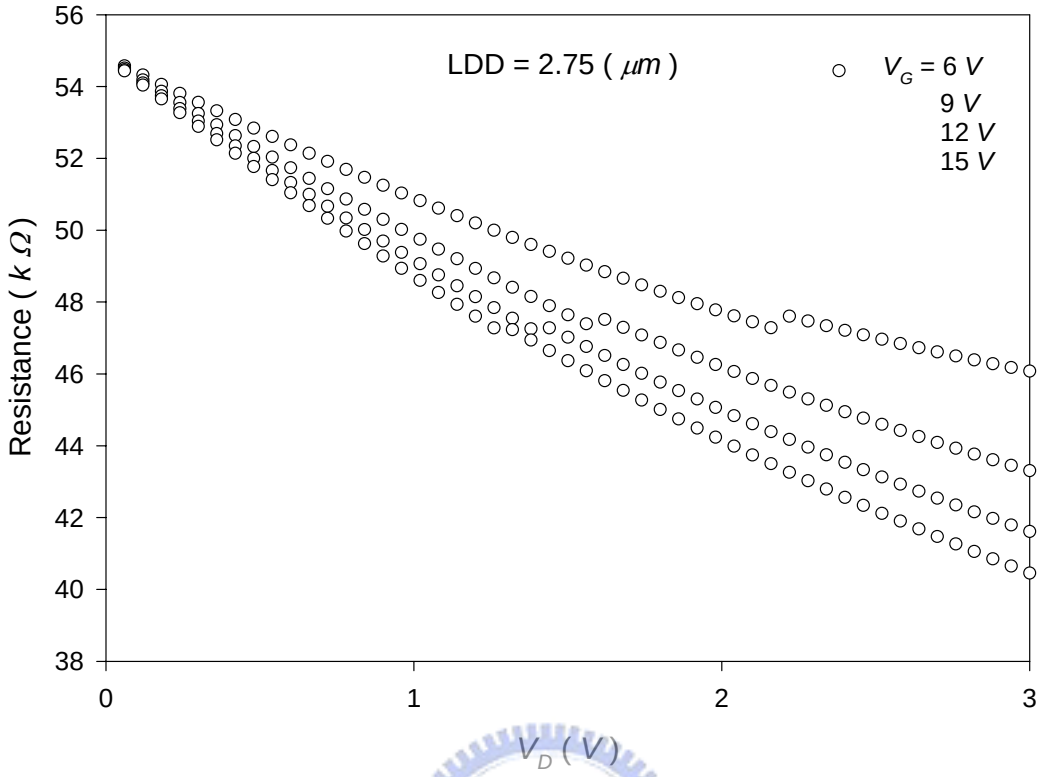


Fig.3-2-5 parameters of barrier height were extracted from linear regression line



The Fig. 3-2-6 shows that voltage in LDD region dependent on drain voltage

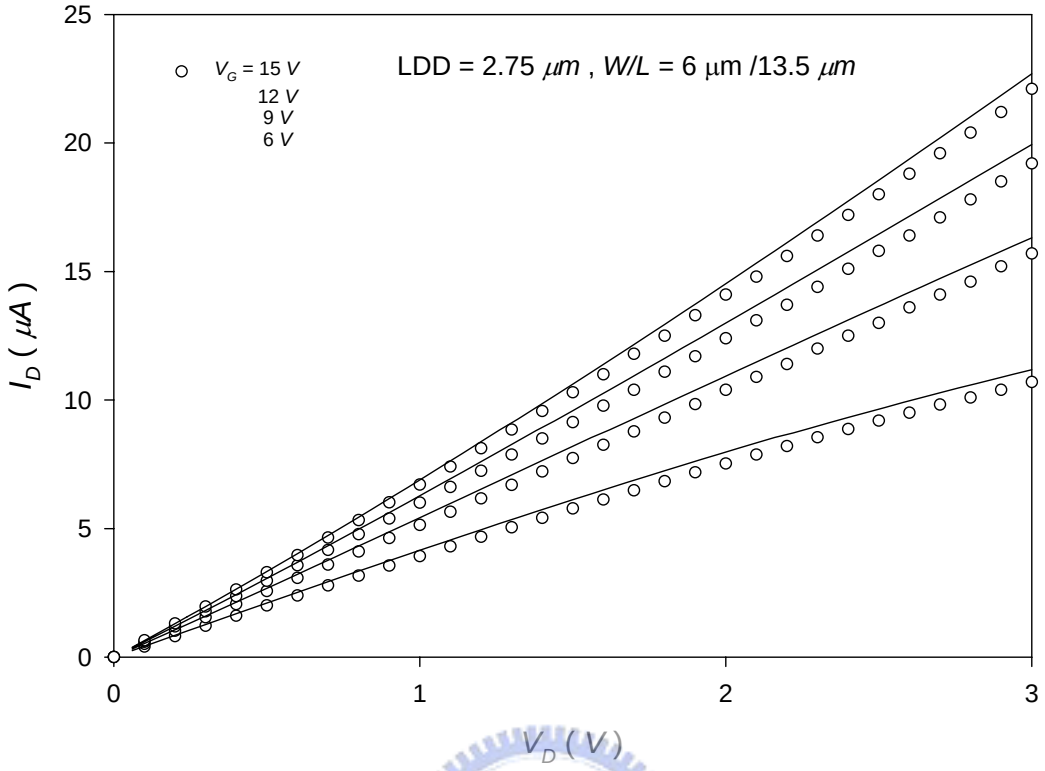


Fig. 3-2-7 the variation of parasitic resistance dependent on drain voltage was showed

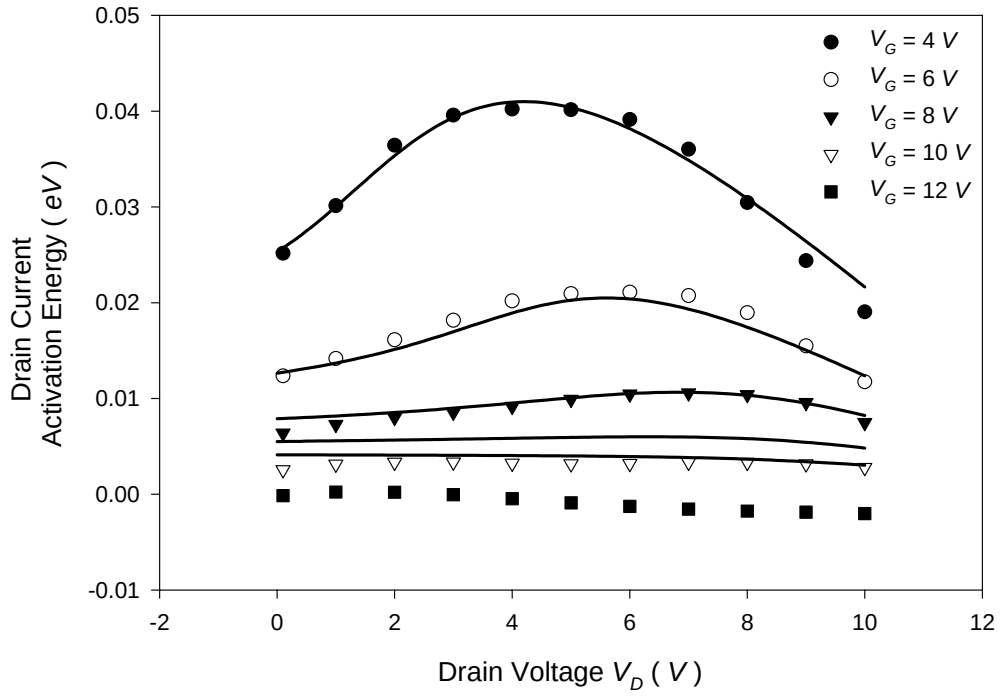
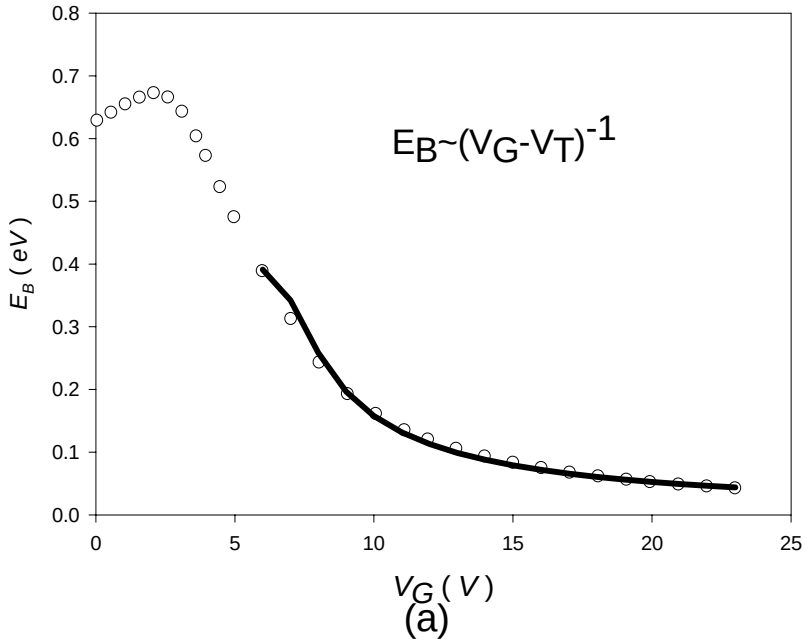
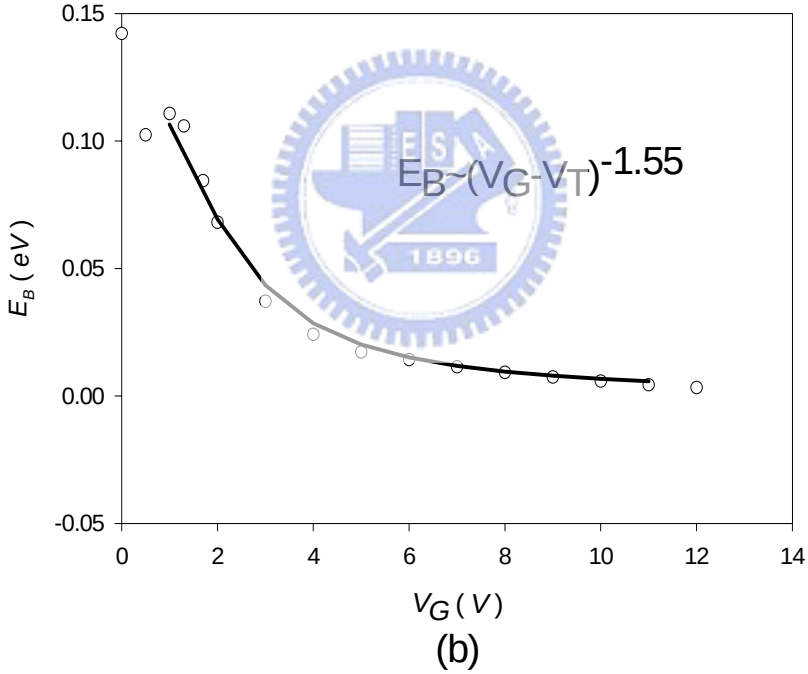


Figure 3-3-1 The relationship of activation energy versus drain voltage for different gate voltages. The solid lines represent the simulated result and the symbols represent the experimental data ($W/L = 6\mu m / 13.5\mu m$)



(a)



(b)

Fig.3-3-2. Barrier height as a function of gate voltage for (a) devices with as-deposited poly-Si film and (b) devices with ELA poly-Si film. The symbols are experimental data and the solid line is the simulated result.

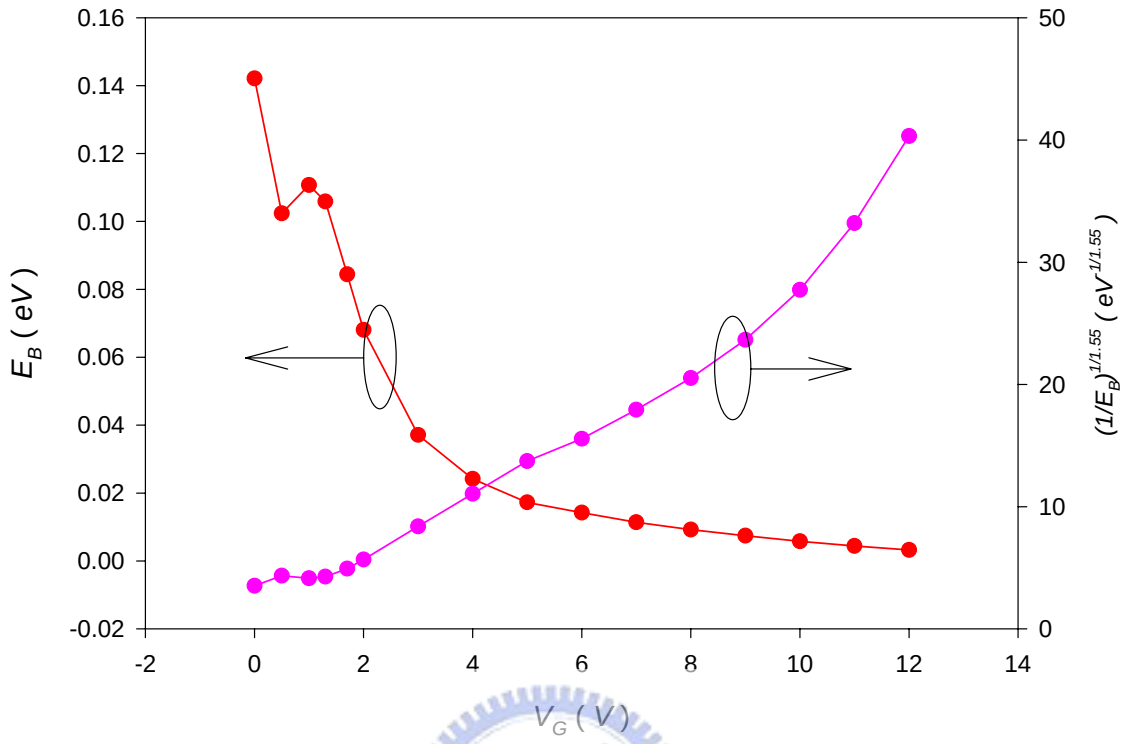
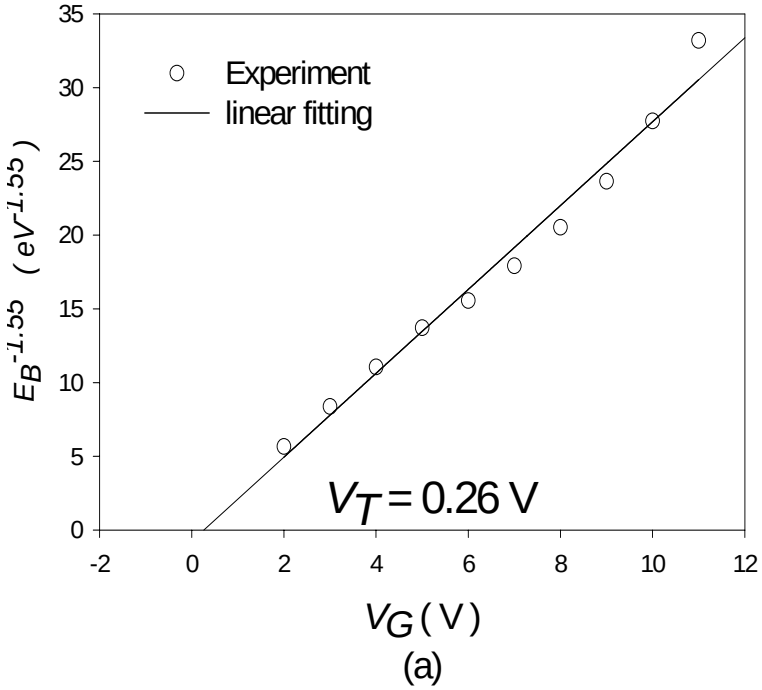


Fig.3-3-3 N_T was extracted from curve in the plot of $E_B^{-1/\gamma}$ vs. V_G (W/L = 6μm/10.5μm, ELA sample, V_D = 0.1V)



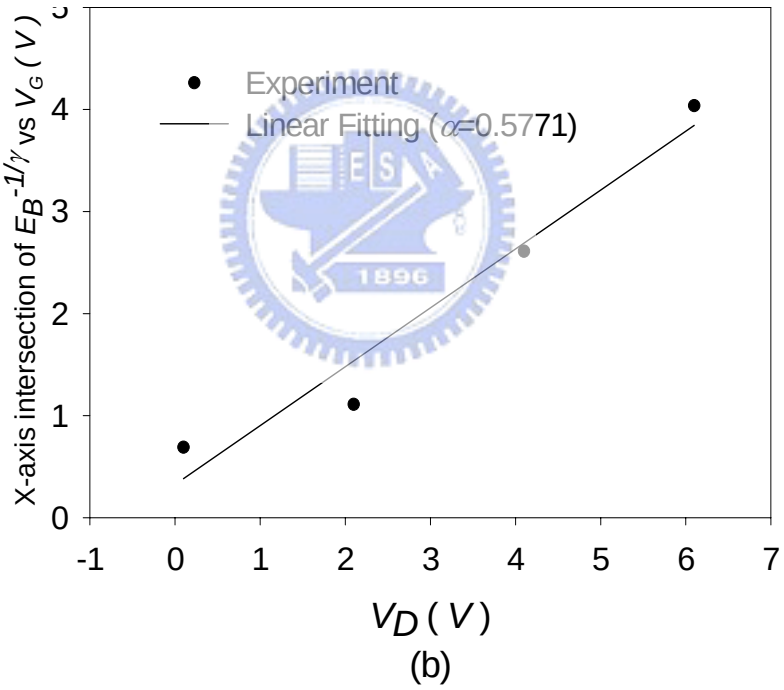


Fig.3-3-4 (a) V_T was extracted from x-axis intersection in the plot of $E_B^{-1/\gamma}$ vs. V_G (W/L = 6μm/10.5μm, ELA sample, V_D = 0.1V) (b) α was extracted from the intersection of $E_B^{-1/\gamma}$ vs. V_G at different drain voltage conditions (W/L = 6μm/10.5μm, ELA sample)

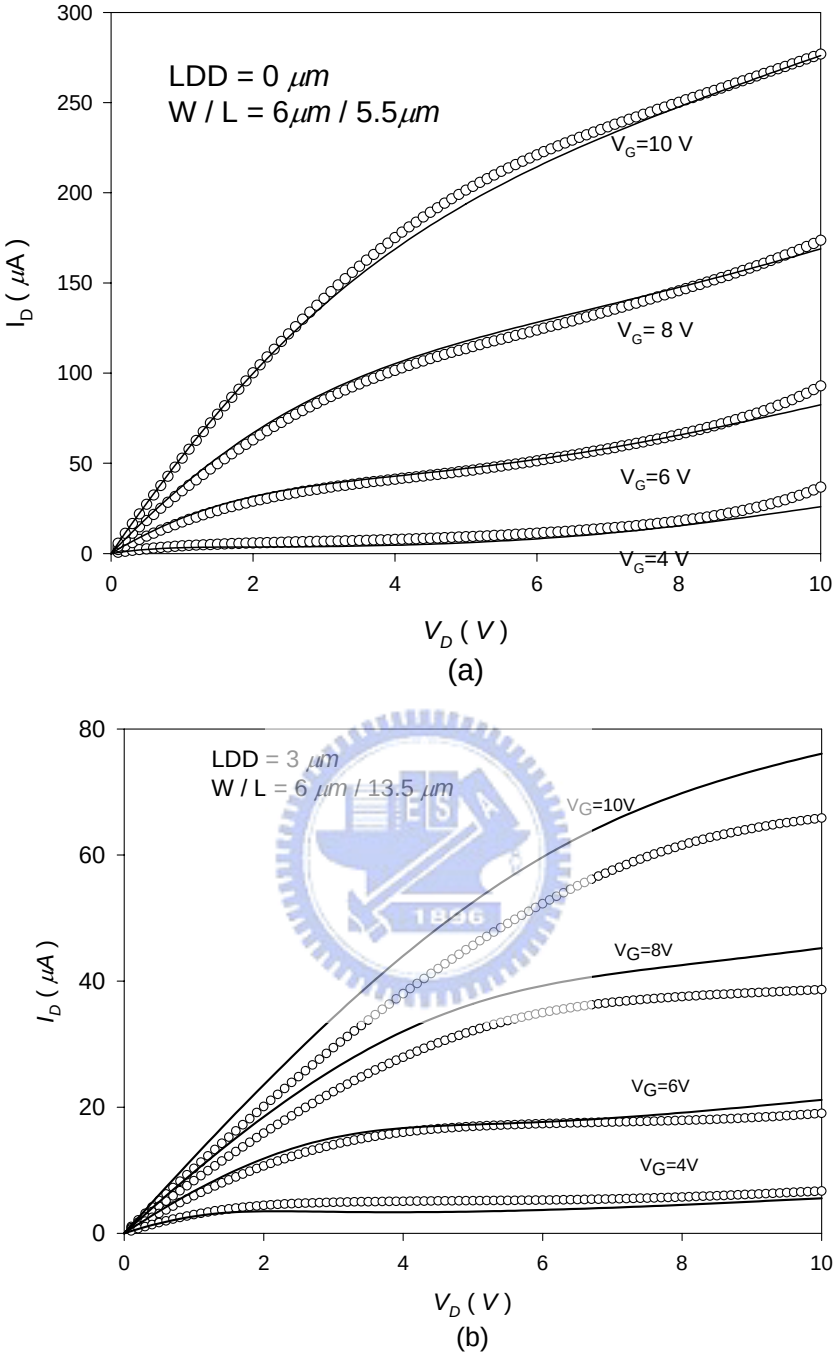


Fig.3-3-5. The comparison of experimental (symbols) and simulated (solid line) *I-V* output characteristics for poly-Si TFTs with (a) no LDD and (b) 3-μm-thick LDD structures.

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論文題目：

具有輕摻雜汲極之複晶矽薄膜電晶體電性模型建立

The I-V Model of Poly-Si TFTs with LDD Structure